Novel Amorphous Silicon Thin-Film Transistor Structure for Flat-Panel Displays

By

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Dedication

To my parents Florence and Tzu-Lien, and sisters Michelle and Claudia.

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List of Abbreviations/Acronyms

A1	Low deposition rate (600 Å/min) hydrogenated amorphous silicon
A2	High deposition rate (1200 Å/min) hydrogenated amorphous silicon
BCE	Back channel etch
BHF	Buffered hydrofluoric acid
BTS	Bias temperature stress
CTS	Current temperature stress
DOS	Density of states
G1	Low deposition rate (900 Å/min) N-rich amorphous silicon nitride
G2	High deposition rate (1800 Å/min) N-rich amorphous silicon nitride
PECVD	Plasma-enhanced chemical vapor deposition
PR	Photo-resist
RIE	Reactive ion etch
S/D	Source/drain
TFT	Thin-film transistor

Glossary

a-Si:H	Hydrogenated amorphous silicon
$a\text{-}SiN_X{:}H$	Hydrogenated amorphous silicon nitride
CF_4	Tetrafluoromethane
C_2F_6	Hexafluoroethane
CCl_2F_2	Dichlorodifluoromethane
HBr	Hydrobromic acid
I_{OFF}	Off-current
KOH	Potassium hydroxide
L	Transistor channel length
μ_{EFF}	Field-effect mobility
μ_i	Intrinsic mobility
n+ a-Si:H	Phosphorous doped (1%) hydrogenated amorphous silicon
S	Subthreshold swing
SF_6	Sulfur hexafluoride
TMAH	Tetramethyl-ammonium hydroxide
V_T	Threshold voltage
$V_{T\text{-}i}$	Intrinsic threshold voltage
W	Transistor channel width

Abstract

In the fabrication of active-matrix liquid crystal display (AM-LCD) and active-matrix organic light-emitting diode (AM-OLED), the amorphous silicon thin-film transistor (a-Si:H TFT) technology forms the backbone of the driving electronics for the large-size displays. Transistors for such application need to have high electrical performance and stability, as well as a high production output. In this dissertation we present an advanced multi-layer amorphous silicon thin-film transistor structure with a tailored channel region for the flat-panel display application. This specially tailored channel allows the rapid deposition of the TFT's gate insulator and active material without significantly altering its electrical performance and characteristics. We first investigate the nominal film geometry that maximizes the production throughput of the transistor. We fabricate transistors with the conventional structure, and they show a field-effect mobility of 0.95 $cm^2 V^{-1} s^{-1}$, threshold voltage of 1.18 V, and subthreshold swing of 0.46 V/dec. We are able to produce multi-layer a-Si:H TFTs that show a field-effect mobility of 0.93 $cm^2 V^{-1} s^{-1}$, threshold voltage of 1.07 V, and subthreshold swing of 0.51 V/dec. However, our proposed TFT structure has a 40% shorter deposition time, which provides it with a competitive edge due to its higher throughput.

In order to further improve the applicability of our a-Si:H TFTs, we present a novel, recess contact TFT aimed to reduce the off-current level. We are able to produce TFTs with an off-current level below 10^{-14} A. Compared to a conventional TFT, this low

off-current TFT has a comparable electrical performance in the on-regime of operation, but approximately one order of magnitude lower off-current.

Finally, we tested the electrical stability of the multi-layer a-Si:H TFTs with the tailored channel. This transistor has similar threshold voltage shift as the conventional transistors, even though the gate insulator is deposited at a high rate. Under 10,000 s of constant current bias (5.5 μA) at an elevated temperature (353 K), our TFT (W/L=24/6) has a threshold voltage of less than 4 V.

Chapter 1

Introduction

1.1. Background and Motivation

In 1963, Richard Williams of the RCA David Sarnoff Research Center published the first observed electro-optic effect in liquid crystal [1, 2]. At the time RCA decided to commercialize liquid crystal displays (LCD) in mid-1960, capacitors and semiconductor diodes evaporated on glass were used for the addressing of each pixel. This addressing scheme, now known as the passive matrix, suffers various limitations from small display size to low frame rate. The introduction of the active-matrix addressing scheme in the mid-1970s realizes the possibility of making higher quality LCD's [3]. For the displays utilizing the active-matrix technology, each pixel contains independent semiconductor-based logic switching, and even memory elements. Consequently, there was a pressing need for a semiconductor material that can be deposited on the substrates used for the fabrication of LCD's. A very promising candidate appeared 10 yrs after the discovery of the liquid crystal, when Malhotra and Neudeck demonstrated the field effect conductance change in an evaporated amorphous silicon film [4]. This structure is the predecessor of the modern-day amorphous silicon thin-film transistor (a-Si:H TFT). In the early 1980's, researchers began to recognize the possibility of using a-Si:H TFT for the pixel electrode circuit of an active-matrix liquid crystal display (AM-LCD) [5-7]. Currently, the

amorphous silicon, together with the low-temperature polycrystalline silicon (LTPS) and cadmium selenide (CdSe) TFT technologies, form the backbone of the driving electronic in the TFT LCD industry. LTPS and CdSe technologies, despite having relatively high electrical performance, require extensive research to overcome uniformity and yield – related issues. The a-Si:H technology is leading the market due to its fabrication flexibility, low cost, and readiness to be used for large size displays. Today the entire TFT LCD industry amounts to an $83 billion business, selling more than 400 million units of displays around the world every year [8]. Along with the recent emergence of the active matrix organic light emitting displays (AM-OLED), it is more important than ever for the realization of high performance a-Si:H TFTs.

The first a-Si:H TFT was fabricated by depositing aluminum source and drain, and electron-beam evaporated a-Si:H on top of heavily doped oxidized silicon wafers. Both hole and electron transports could be observed between the source and drain terminals. In 1977 and 1978, Fritzsche and Deneuville separately began using PECVD as a tool to deposit amorphous silicon film to be used for field-effect transistor, [9] and bipolar junction transistor [10], respectively. The operation and theory of a-Si:H TFT was confirmed and further analyzed by Matsumura and Nara [11], when they explicitly indicate both p and n channel conductions of the device. However, in both cases the apparent mobility is quite low and a large voltage is required to turn on the transistor. Hayama and Matsumura deposited an n+ a-Si:H layer between the a-Si:H and the metal, and this causes a great increase in on-and-off-current ratio due to the reduction of the TFT contact resistance [6]. Powell *et al* used silicon nitride as the gate insulator, and achieved a very low threshold voltage and subthreshold swing because of improvement in

the interface quality and the a-Si:H DOS [12]. Even though Le Comber *et al.* had already suggested the use of a-SiN_X:H as the gate insulator [13], Powell's TFT showed great electrical performance, and the era for a-Si:H TFT began. Over the course of a decade, from the characterization of material by Walley, Brodsky, and LeComber to the emergence of the modern structure, a-Si:H TFT has since become the dominant technology in displays and sensors, with researchers all over the world seeking new ways to optimize its performance and broaden its application.

In order for the a-Si:H TFT technology to continue its current dominance in the AM-LCD industry, several of its drawbacks must be addressed as they can limit its potential applicability for large size displays. First of all, the a-Si:H TFT has a lower electrical performance than, say poly-silicon TFT, because the amorphous silicon film has smaller crystalline grain sizes. The distortion of the ideal tetrahedral silicon-to-silicon bond leads to the creation of the band-tail states along the conduction and valence band edges, while the unsatisfied dangling silicon bonds produce the deep-gap states [14]. Both types of states degrade the transistor's electrical performance, which in turn limits the sizes of both AM-LCDs and AM-OLEDs that use the a-Si:H TFT as the driving electronic [15, 16]. Secondly, the a-Si:H TFT can have a high leakage current, in part originating from its fabrication process. This deleterious effect can lead to AM-LCD luminance change during the driving stage of its pixel electrode circuit, due to the discharging of the storage capacitor through the channel of the switching transistor. Lastly, it is desirable to deposit the amorphous silicon films at a high deposition rate to increase the overall manufacturing throughput of the display, which in turn lowers its production cost. However, increasing the deposition rate of the a-Si:H film increases the

densities of both band-tail and deep-gap states. It is well-known that a-Si:H films with high band-tail states produces TFTs with low field-effect mobility [14], and this means that there exists a trade-off between throughput and performance. Typically, TFTs with higher electrical performance suffer even more performance degradation with increase in deposition rate. This phenomenon poses a challenge for engineers who want to maximize their displays' production throughput without compromising the integrity of the a-Si:H TFT's electrical performance.

At the time of this dissertation, there are numerous reports of high performance a-Si:H TFT's deposited at high deposition rates. Methods of a-Si:H film deposition include high frequency (HF), 13.6 MHz, plasma enhanced chemical vapor deposition (PECVD) [17], very high frequency (VHF), typically above 40 MHz, PECVD [18-20], catalytic CVD (Cat-CVD) [21, 22], and electron cyclotron resonance CVD (ECR-CVD) [23, 24]. However, only high and very high frequency PECVD systems are used for the production of the FPD panels. Although other deposition systems are capable of producing a-Si:H TFTs with high mobility values at high deposition rates, it is difficult for these tools to deposit a-Si:H over a large area. VHF PECVD systems can deposit a-Si:H over a large area, but require expensive setup to combat non-uniform deposition thickness and power loss problems caused by the standing evanescent wave at the surface of the capacitor electrodes [25]. Table 1-1 summarizes the benefits and limitations of some of the methods used for amorphous silicon film deposition.

Table 1-1: Summary of common CVD systems used for the deposition of electronic grade amorphous silicon films.

	Field-Effect Mobility ($cm^2 V^1 s^{-1}$)	Threshold Voltage (V)	Deposition Rate (nm/min)	Suitable for Large Area?	Uniformity Over Large Area?
HF PECVD [17]	1.45	1.9	50	Yes	Good
VHF PECVD [18]	1.1	1.1	60	Possible	Average
Cat-CVD [21]	0.85	4.6	114	Possible	Good
ECR-CVD [24]	15.3	3.7	120	No	Poor
PECVD in this study	0.93	1.1	102*	Yes	Good

* effective deposition rate

The mission of this dissertation is to design and fabricate a commercially viable amorphous silicon transistor structure for the future flat-panel display industry. To achieve this, we propose a novel amorphous silicon thin-film transistor multi-layer structure with a specially tailored channel region to achieve the optimum electrical performance and stability, while maintaining a short overall deposition time. This structure can be used for the commercial fabrication of large-size FPDs due to its high mobility and high potential production throughput. Next, we formulate a meticulously tuned fabrication procedure that maximizes our transistor's electrical performance. This process is fully compatible with the commercial fabrication of FPDs. Additionally, we present a novel etching method that reduces our transistor's leakage current.

1.2. Organization of Dissertation

In chapter 2, we provide the detailed fabrication steps and characterization methods used to produce and analyze the proposed multi-layer amorphous silicon thin-film transistor with the tailored channel. This chapter includes the background information regarding semiconductor processing, description of the fabrication tools and

processes, setup of the analytical systems, and engineering controls and testing techniques used during the fabrication of the proposed a-Si:H TFT. Chapter 3 describes the geometric effect of the tailored channel on the electrical performance of the proposed transistor, and evaluates the trade-off between the film deposition time and the transistor's electrical performance. We successfully fabricated a-Si:H TFTs with the tailored channel, in a PECVD system used for the commercial manufacturing of FPDs, that exhibit field-effect mobility (μ_{EFF}) of 0.93 $cm^2 V^{-1} s^{-1}$, threshold voltage (V_T) of 1V, and subthreshold swing of 0.51 V/dec.

In the following chapter, we present the effect of back channel etch (BCE) on the electrical properties of our a-Si:H TFT. We show the minimum thickness for the total amorphous silicon film deposited is ~1600 Å, and that $HBr+Cl_2$ is a promising dry etchant for the back channel etch process. Chapter 5 demonstrates a novel transistor structure with recessed source/drain contact electrodes that is specially designed to reduce the TFT's off-current. The recessed contact TFTs has off-current values of $5x10^{-15}$ and $1x10^{-11}$ A in the linear and saturation regions of operation, respectively, and shows no current crowding phenomenon. In chapter 6 we present the thermal and electrical performance and stability of the proposed a-Si:H TFT to demonstrate their applicability as the driving electronic for FPDs. Lastly, chapter 7 summarizes the work done in this dissertation and our recommendation for future research in the field of amorphous silicon thin-film transistors for display and other applications.

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Chapter 2:

Fabrication and Characterization

2.1. Thin-Film Etching

2.1.1 Mechanism and Terminology

In modern day semiconductor processing, etching has become one of the most important steps in maintaining the quality of the products. Precise etching control, including etching profile, rate, and selectivity, allows engineers and scientists to fabricate devices with high accuracy, reproducibility, and uniformity. We will assess various etching methodologies used today in the processing of hydrogenated amorphous silicon thin-film transistors. Traditionally etching is divided into wet etching and dry etching. Wet etching comprises of using solution as the primary etchant in the removing metal, semiconductor, and insulator films. On the contrary dry etching involves using a plasma to remove the desired films. Etching consists of three main steps: transport

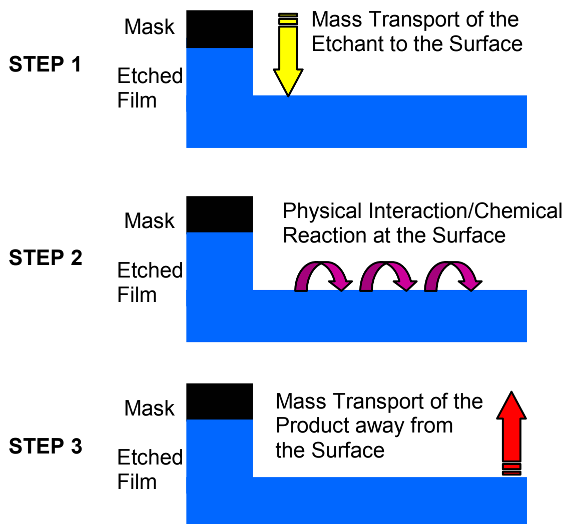

Figure 2-1: Schematic of the etching process.

of etchant to the surface of the film to be etched, physical interaction and/or chemical reaction between the etchant and the film, and transport of the etching products away from the surface (figure 2-1).

The products of the etching process are generally in the gas or liquid phase to allow the completion of the last step of etching, namely the removal of the products. Masks are commonly used to define device structures, and typically, they should either be highly resistant to the etchant, or sacrificial layers that will not be included upon the completion of the device being fabricated. There are numerous criteria used to control and judge the quality and outcome of an etching process: etch directionality, etch rate, etch uniformity, etch selectivity, undercut, and repeatability.

Etch depth (d_{ETCH}) – Amount of film removed during etching (d_{ETCH}).

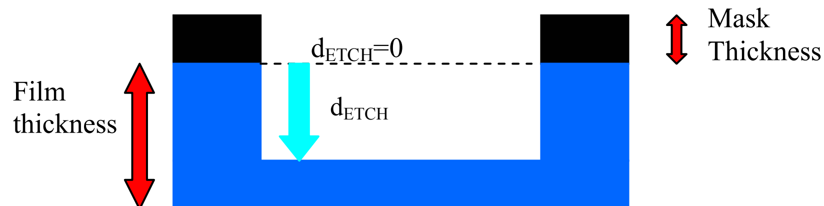

Figure 2-2: Schematic describing etching depth.

Etch rate (R_{ETCH}) – Amount of specific film etched by an etchant in a given time, typically measured in nm/min or Å/min.

Etch directionality – Measure of the relative etch rates in different directions. A special case is the measure of vertical etch rate to lateral etch rate, also know as anisotropy (A).

Etch uniformity (U) – Percent of variation in etching depths across the entire wafer, from wafer to wafer, within a lot, or from lot to lot.

$$U = \frac{R_{HIGH} - R_{LOW}}{R_{HIGH} + R_{LOW}}$$

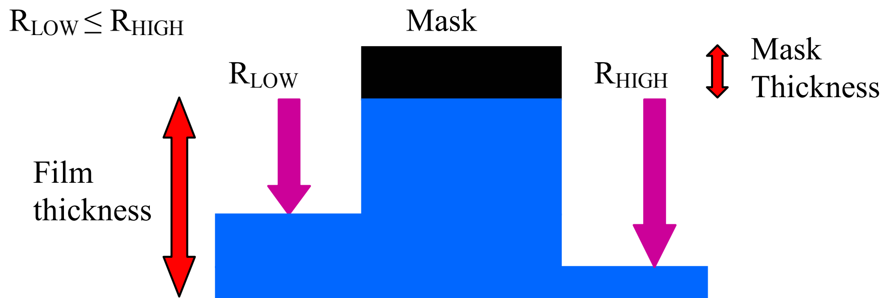

Figure 2-3: Schematic describing etching uniformity.

Etch selectivity (S) – Ratio of the etch rate of one film to the etch rate of another film for one specific etchant.

$$S = \frac{R_1}{R_2}$$

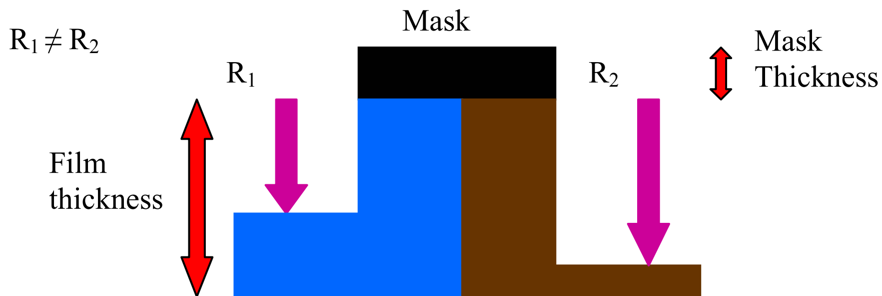

Figure 2-4: Schematic describing etching selectivity.

Undercut – Lateral etching of the target film underneath the etch mask.

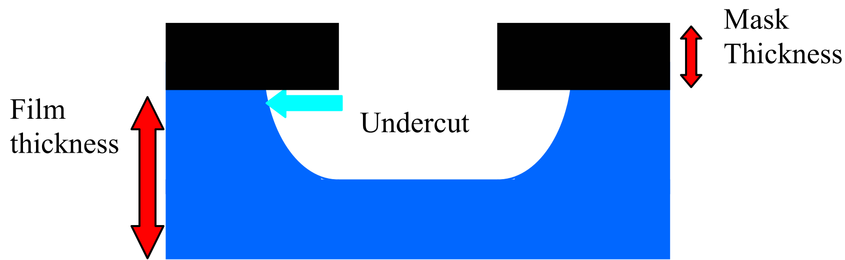

Figure 2-5: Schematic describing undercut during etching.

Anisotropy (A) – It is defined by the following relations:

$$A = 1 - \frac{R_{LATERAL}}{R_{VERTICAL}}.$$

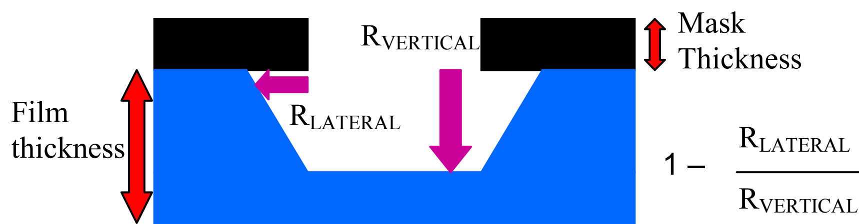

Figure 2-6: Schematic describing anisotropy.

Isotropic etch – Etching of the film in all direction at the same etch rate, or A=0.

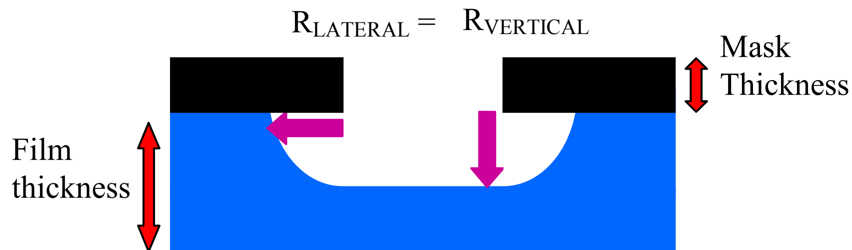

Figure 2-7: Schematic of an isotropic etch, where A=0.

Anisotropic etch – Etching of the film in different directions at different etch rates.

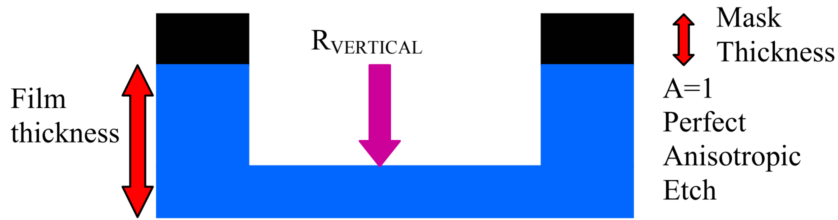

Figure 2-8: Schematic of a perfect anisotropic etch, where A=1.

Under-etch – Etching step which the actual etching depth is smaller than the target etching depth.

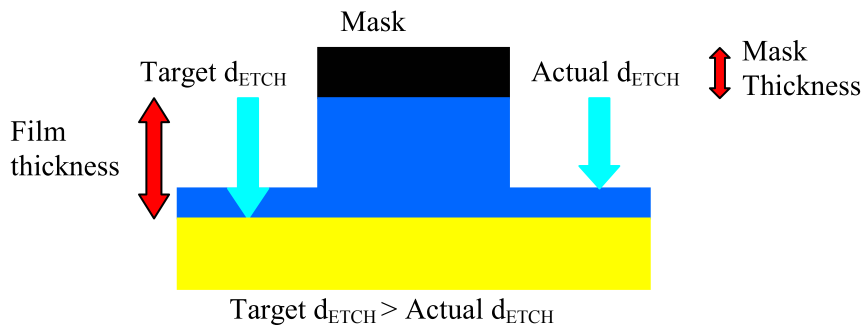

Figure 2-9: Schematic of an under-etched film.

Over-etch – Etching step which the actual etching depth is larger than the target etching depth, potentially causing some etching of the underlying film.

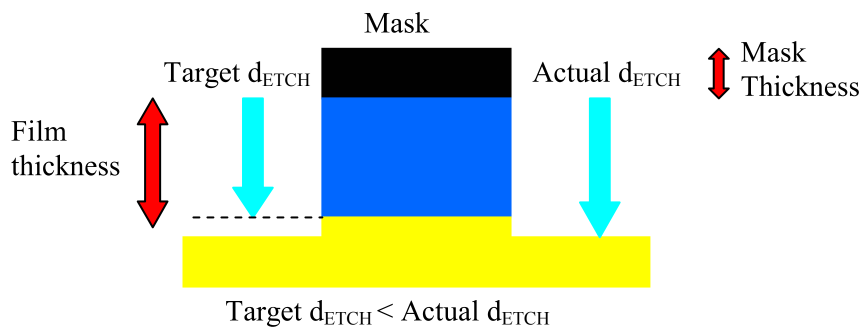

Figure 2-10: Schematic describing an over-etched film.

Loading – Decrease in etch rate caused the depletion of etchant. This is caused by excess amount of particles from the film reacting with the etchant; the extensive reaction causes the concentration of the etchant to drop, leading to a decrease in the etch rate.

2.1.2 Wet Etch

Wet etching, as the name suggests, uses liquid phase etchant to remove the target films. As the device substrate is submerged into the etchant, reactants in the solution diffuse across the stagnant layer near the surface of the film to reach the film surface. Next, chemical reaction between the reactants and the film particles take place. Lastly soluble products diffuse across the stagnant layer back into the bulk of the liquid to complete the etching process. Physical interaction, such as sandblasting, is not a significant component of the wet etching process. Typically a deionized water rinse immediately follows the chemical wet etch to stop further etching of the film by removing any solution left on the surface of the substrate. The wet etching process is highly sensitive to the etchant temperature, reactant concentration, and sometimes humidity. Since the reactant concentration near the surface decreases during the etching process as the product concentration increases, it is a common practice to stir the substrate during the wet etch to allow a more uniform distribution of reactant throughout the solution, resulting in a more consistent etch rate across the substrate during the etch. Another purpose for the stirring is to remove air bubbles that can form during the wet etch. Since the by-product of the etching process can be gaseous and liquid, air bubbles may be trapped on the surface of the substrate, especially in a viscous etchant. A trapped air bubble forms a “soft” etching mask that prevents the film underneath it to be in

contact with the liquid etchant, thus producing a non-uniform etching of the film across the entire substrate.

In the fabrication of our a-Si:H TFT, the chromium gate, hydrogenated amorphous silicon nitride encapsulation, and molybdenum source/drain contacts are etched by the following solutions: CR-14 Chromium Etchant ($C_2H_4O_2$ and $Ce\{NH_4\}_2\{NO_3\}_6$), buffered hydrofluoric acid (HF, NH_4F, and H_2O), and Aluminum Etch Type A (H_3PO_4, HNO_3, and $C_2H_4O_2$), respectively. In a few experiments, the a-Si:H and n+ a-Si:H are removed using potassium hydroxide (KOH).

Chromium Wet Etch

The reactions of the chromium etch, is shown below [1]:

$$3Ce(IV)(NH_4)_2(NO_3)_{6(AQ)} + Cr \rightarrow Cr(III)(NO_3)_{3(AQ)} + 3Ce(III)(NH_4)_2(NO_3)_{5(AQ)}. \quad (2\text{-}1)$$

Chromium etching of the gate can be quite unpredictable as the etch rate fluctuates with changes in temperature, humidity, and/or concentration of the etchant. Therefore we used test wafers before, during, and after the etching of the device wafers. Test wafers for this step were glass wafers with a sputtered chromium layer of identical thickness as the gate metal layer. Since the color of chromium is metallic gray, sputtering chromium on glass turns the wafer from transparent to opaque. During the etching of chromium-on-glass wafers in CR-14, the glass testing wafers turned from opaque to transparent, then opaque again, and finally transparent. This transition to the second transparent phase indicated a complete removal of the chromium layer. We believed that the after the first transition, there was still a thin layer of chromium or chromium oxide, which could short the gate level patterns if remained on the surface. Upon the completion of the etching, test wafers were removed from the clean room for resistivity testing. Every gate level

etching required monitoring the etch rate on the test wafers before and after the etching of the device plates for quality control.

Silicon Nitride Wet Etch

The wet etching of a-SiN_X:H in buffered hydrofluoric acid has the following chemical reaction:

$$Si_3N_4 + 12HF \rightarrow 3SiF_4 + 4NH_3. \quad (2\text{-}2)$$

The silicon nitride in the equation is deposited at high temperature (i.e. via LPCVD process), therefore the ratio between silicon and nitrogen (3:4) is well defined. For the low temperature PECVD nitride we used in our experiment, the reaction is similar, but the Si/N ratio may vary. During the BHF etch of the amorphous silicon nitride, the ammonium fluoride maintains the HF concentration, thus the pH of the solution. This buffering mechanism keeps the BHF etch rate constant, at about 500Å/min at room temperature. Figure 2-20 shows the BHF etching rate test performed on G1 and G2.

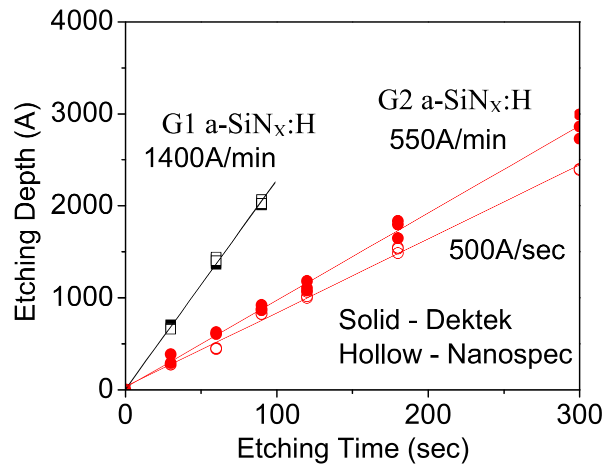

Figure 2-11: Etching rate characterization plots for G1 and G2 silicon nitride.

Amorphous Silicon Wet Etch

Selective KOH etching of silicon has the following reaction [2]:

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2 \quad (2\text{-}3)$$

At 353 K and 50 weight percent versus deionized water, the etch rate reaches above 1 μm/min [3]. Moreover, this process is highly sensitive to temperature, and the etch rate varies up to 10 %/K. In order to have better control of the etch rate, we lowered the etching temperature down to 323 K and the concentration down to 10 weight percent in deionized water. The etch rate using such formula is approximately 1200 Å/min. More details regarding silicon wet etch will be discussed in chapter 4.

2.1.3 Dry Etch

Dry etching, typically done in a plasma chamber, consists of two distinct mechanisms that occur simultaneously during the actual etching process: chemical and physical etchings. The chemical etching begins by breaking the molecules of the etchant gas into subspecies and free radicals via ionization. Typically, for a plasma generated by a specific precursor gas combination, there will be a variety of ions and particles present in the reactive ion etcher at the same time; the particle that is primarily participating in the etching process, however, is the free radical. The highly reactive free radicals chemically bond with the atoms in the layer to be etched, resulting in the formation of gaseous etching products. Table 2-1 lists some of the common precursor gases used in the etching of silicon, poly-silicon, and amorphous silicon. Since in chemical etching, the process is reaction-based, typically the selectivity is very high; the cost of this advantage is that lateral etching increases. As a result, the anisotropy decreases and we begin to observe undercut beneath the mask. To mitigate this phenomenon, the physical component of the dry etch is included. Contrary to the chemical etching by the free

radicals, physical etching begins with accelerating the ionized species in the plasma toward the substrate layer to be etched. Particles on the surface of the target film begin to depart upon impact of the collision. This sandblasting process produces side-wall deposition of non-volatile etching products, which inhibits the lateral etching by the reactive particles in the plasma. Effectively, physical etching constantly deposits sacrificial masking layers, which can be oxide-like or polymer-like, onto the side-walls during the dry etching process. Another effect of ion bombardment is that it "knocks lose" the atoms on the film's surface, making the chemical reaction occur more easily for the free radicals and the film; this lowers the activation energy of the chemical reaction between the etchant and the material of the target film.

Table 2-1: Common RIE etching recipe used for silicon transistor process.

Material	**Etchant**	**Reference**
Silicon/ Poly-Si	1. $SF_6/SF_6+C_2ClF_5$ 2. $SF_6+C_2Cl_3F_3$ 3. SF_6+O_2 4. $SF_6+H_2/He/N_2/O_2/Ar$ 5. $Cl_2:O_2$ (50:8) 6. HBr 7. $HBr:O_2$ (50:8) 8. $HCl:O_2$ (50:8) 9. $CF_4:CHF_3:Ar:CO$ (20:30:300:150) 10. $CF_4:CHF_3:Ar:C_4F_8$	1. Castan *et al*. [4] 2. Yunkin *et al*. [5] 3. Wells *et al*. and Syau *et al*. [6, 7] 4. Arora *et al*. [8] 5. Desvoivres *et al*. [9] 6. Nakamura *et al*. [10] 7. Wahlbrink *et al*. [11] 8. Wahlbrink *et al*. 9. Komeda *et al*. [12] 10. Komeda *et al*.
a-Si:H	1. $SiCl_4+Ar/CF_4/O_2$ 2. $HBr+Cl_2+He+O_2$	1. Kuo *et al*. [13] 2. Yost *et al*.[14]
n+ a-Si:H	1. CF_3Cl 2. CF_2Cl_2	1. Kuo *et al*. [15] 2. Kuo *et al*.

SF_6 Etching of Silicon

For SF_6 etching of amorphous silicon, the primary reaction is [6-8]

$$Si + 2SF_6 \rightarrow SiF_4 + 2SF_4. \quad (2\text{-}4)$$

The fluorine radicals come from the dissociation of the SF_6 molecules. Free radicals are highly reactive, and bond with the silicon atoms; both products in this reaction are volatile, and get pumped out of the plasma chamber quickly via the pump. During the plasma etch of silicon, superficial SiO_2 can also be removed by the fluoride radicals to form oxyhalides [16]. This avoids the need to perform native oxide removal prior to the island etch process as SF_6 etches both silicon dioxide as well as silicon. SF_6 dry etching is highly reaction based, which means that the lateral etch can occur. We use the SF_6 based chemistry to perform the island etch due to its high etch rate (figure 2-12). Since in our experiment a photo-resist layer was used as the mask, polymer residues may be left on the substrate after the etching. An oxygen plasma treatment, commonly known as an ashing process, can remove all the organic-based residues.

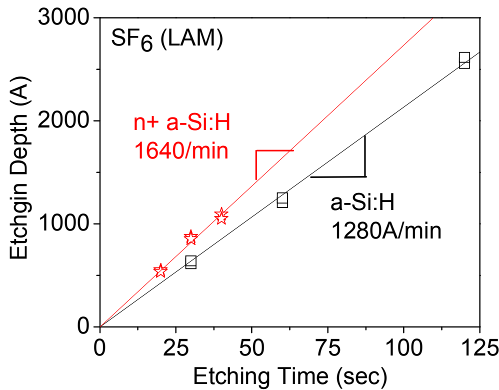

Figure 2-12: SF_6 etching rate characterization plots.

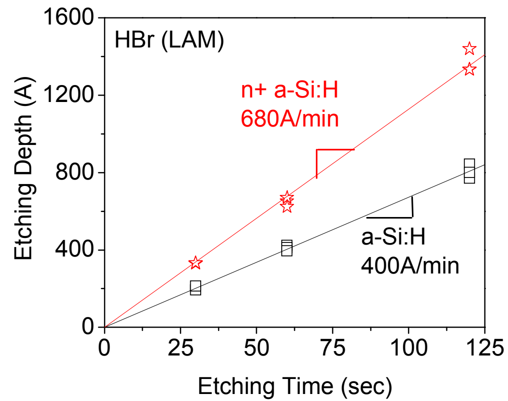

Figure 2-13: HBr etching rate characterization plots.

HBr Etching of Silicon

Similarly, the etching of amorphous silicon using HBr has the following reaction [17]:

$$Si + 4HBr \rightarrow SiBr_4 + 2H_2. \quad (2\text{-}5)$$

The atomic bromine comes from the dissociation of the HBr molecule. HBr dry etching has a more than 200:1 selectivity between silicon and oxide [18]. In this case native oxide can impede the etching of the amorphous silicon, even if an HF dip is performed right before the dry etch. A breakthrough etch using Cl_2 is necessary to remove the native oxide, and expose the amorphous silicon layer for the main HBr etching. Throughout the dry etching process, some non-volatile by-product may be deposited on the side-wall, or the surface of the film to be etched. To prevent any micro-masking by the by-product, we include Cl_2 in our HBr etching recipe (with a 1-to-1 ratio) to constantly remove the by-product. This addition also increases the overall etch rate of the amorphous silicon. Our HBr recipe etches amorphous silicon at 400 Å/min and n+ amorphous silicon at 680 Å/min (figure 2-13).

In general, wet etching tends to show higher etching rate because of the higher concentration of etchant. It does not expose semiconductor films to plasma, which have been reported to degrade the electrical properties of the transistors. However, the downside to wet etching is its lack of anisotropy, or the direction of etching. A few solution-based etching, such as KOH used on silicon, does provide some directionality as KOH etches different planes of silicon at different etch rates. But in general it is difficult to control the anisotropy of the wet etch process. Dry etching on the other hand, provides much improved anisotropy due to the side-wall inhibitor deposition and the ion

bombardment. In terms of selectivity, both wet and dry etchings have benefits and shortcomings. Many wet etchants used in semiconductor processing are acid-based. While these etchants can have very high selectivity among the insulator and semiconductor films, they will, to some degree, attack the metallic films that are ubiquitous in the fabrication of thin-film transistors. An example is, HF, which is commonly used to etch SiO_2, has a very high selectivity over silicon. However, HF also etches titanium (Ti), which is commonly used as the contact or inter-connect metal. Dry etchants, on the other hand, often etch insulator and semiconductor films at comparable rates, but rarely can etch metal effectively. It is thus important to take all these factors into consideration during the fabrication of a-Si:H TFT.

2.1.4 Dry and Wet Etching Non-Idealities

Under-etch

Under-etch occurs when the actual etching depth is smaller than the target etching depth. This leaves a layer of the target film on the surface, even though it is supposed to be removed entirely. Under-etch poses a very serious problem during the definition of the gate, n+ a-Si:H, and source/drain. Intuitively, it is obvious that the under-etching of any one of these layers leads to undesirable shorts in the amorphous silicon TFT. In the case of the chromium gate etch, residual chromium left on the substrate effectively shorts all the gates on the substrates together. An adverse outcome of under-etching the gate is that the transistors' gate level leakage is going to increase significantly. For the n+ a-Si:H layer, under-etching can lead to larger TFT off-current in both linear and saturation regimes of operation. Lastly, there is the catastrophic effect of the under-etching the

molybdenum source/drain contact. Any under-etching of the Mo layer leads to the shorting of the contacts together. A thin layer of Mo acts as a mask for the subsequent back channel etch process, which means that during the BCE, the etchant may not remove the n+ a-Si:H at all. This is especially true when we use KOH etching for the BCE of the a-Si:H TFT, because KOH does not etch molybdenum aggressively.

Over-etch

Contrary to an under-etch, an over-etch happens when the actual etching depth is larger than the target etching depth. Slight over-etch of the gate, source and drain, or the back channel will decrease gate and contact overlap because the undercut begins to diminish the area of the metal pads. One possible effect of this type of undercut is the raise in contact resistance. With a higher contact resistance the effective mobility can

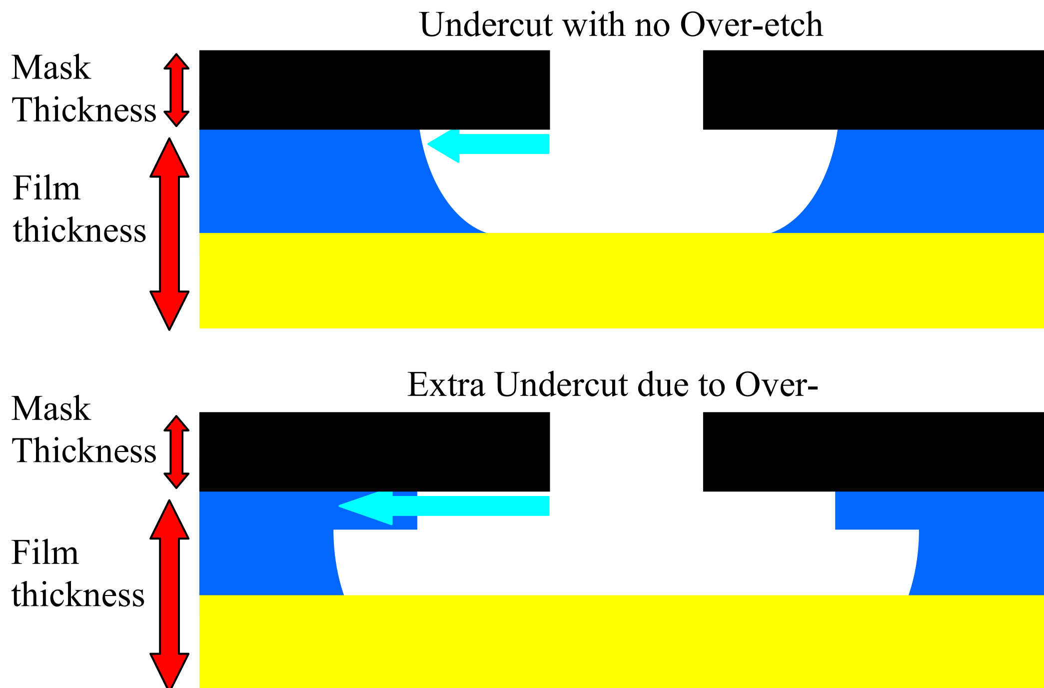

Figure 2-14: Schematic of extra undercut caused by excess over-etch.

decrease as more drain voltage is dropped across the contact. A severe case of contact resistance degradation caused by large undercut is that the source and drain contacts no longer behave as ohmic contacts. When this happens, the source and drain terminals become schottky contacts. Another over-etch problem that is exclusive to the back channel etch process is the degradation of the device characteristics. When performing the back channel etch, it is imperative to control the etching depth of the n+ a-Si:H and a-Si:H layers to prevent over-etch. The effect of over-etching of the a-Si:H film will be discussed in chapter 4.

Mask Erosion

In some cases the etchant attacks the mask used to define the features. If the etchant is not perfectly anisotropic, then it will etch laterally into the mask. An example of this is the oxygen plasma ashing the photo-resist mask during an RIE process. Mask erosion distorts the features of the device. It may produce tapered profile and/or excessive undercut. Mask erosion often takes place during dry etch, where the etching selectivity between the film and the mask tends to be lower than wet etching. If the plasma etching includes oxygen as one of the precursor gases, there certainly will be some photo-resist mask erosion. The effect of mask erosion on the film is similar to over-etching, where there is an increase in the undercut. In our process, both gate and source/drain processes use acid based solutions to etch the respective profiles. Since acid can attack photoresist, unwanted lateral etching of the metallic contacts can occur as a result of mask erosion. This may decrease the gate and source/drain overlap area, which in turn increases the contact resistance of the TFT.

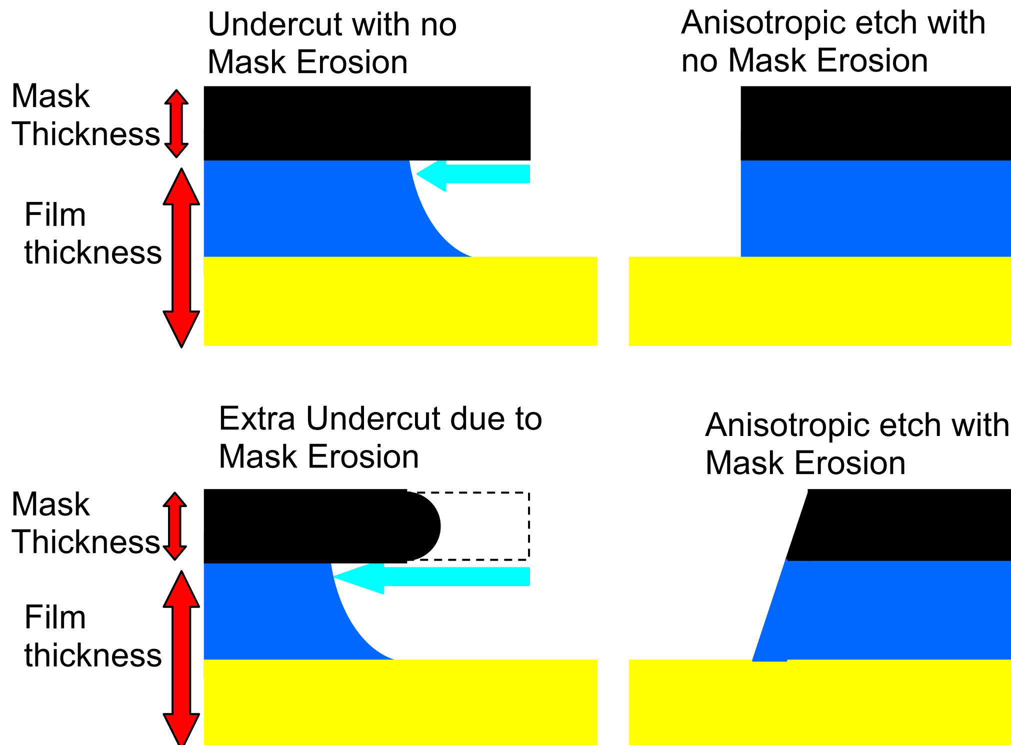

Figure 2-15: Schematic of extra undercut caused by mask erosion.

2.1.5 Etch Process Control

Even with carefully characterized etch rate, there are many factors that can lead to non-ideal etching of the device film. As mentioned before, such non-ideality can degrade device performance, or lead to device failure. To prevent such mishap from happening, we use additional ways to detect, mitigate, or even resolve the problems.

End Point Detection - RIE

Some modern reactive ion etchers are equipped with end point detection systems. Such systems detect film color change due to the thickness change, or the product gas concentration. Film color changes with thickness because of interference effect; the detail is discussed in many books regarding semiconductor processing such as Silicon

VLSI Technology by Plummer, Deal, and Griffin, and will not be reiterated here [19]. The second type of end point detection detects the concentration of product gas originated from the reaction between the etchant and the film. This technology relies on the difference in plasma etching chemistry between the film to be etched and the underlying film. Optical detectors measure the concentration of the etchant product releasing from the surface of the film during the plasma etch. Once the film is etched through, the etchant begins to react with the exposed underlying film, and the etching products change. This change in gaseous product is detected by optical detectors, and alerts users. End point detection is very useful during the island etch, because the films we try to etch are a-Si:H and n+ a-Si:H, and the underlying film is a-SiN_X:H. We observe a drastic change in output gas concentrations when we etch through the two target layers. LAM 9400 possesses end point detection based on product gas concentration.

Over-etch

The most common method to avoid problems caused by the under-etching of the film is over-etching. Typically we perform 5-10 % over-etch to ensure etching through of the film, except for the back channel etch. This over-etch reduces the possibility of under-etching caused by the loading effect, or other unexpected variations that occur before and during the etching process. During the gate and source/drain metallization, we routinely carry out a 5 % over-etch.

Use of Test Wafers

On top of all the quality control techniques mentioned above, it is still a good idea to use test wafers for all the etching processes. Test wafers have identical films compositions, lithographic patterns, and thicknesses as the device wafers; they are being etched concurrently with the device wafers. These are used to measure the depth of the etching process, without removing the etching masks on the device wafers. The assumption is that the etching depth of the test wafer is the same as the device wafer, and as long as the etching uniformity is high during the process, test wafers are very useful to detect under-etching. For every thin-film deposition, photolithography, and etching step in this dissertation, we use test wafers to improve the accuracy and reliability of the fabrication process.

2.2. TFT Fabrication Process

Our devices were fabricated on 4" oxidized silicon substrates with 10kǺ of thermally grown wet oxide. All photolithography steps were performed on a Karl Suss MA-6 Aligner using 5" chromium/quartz masks. The names of the masks are included in curly brackets for rest of this section; the critical dimension (CD) for all the masks are below 0.5µm. We used 1.5 µm of Shipley 1813 photo-resist (PR) as the etching mask for all the wet etching steps, and 3 µm of Shipley 1827 photo-resist for the dry etching steps. Prior to the deposition of a new layer of material or photo-resist, we rinsed the surface with acetone, isopropyl alcohol (IPA), and deionized water (DI), and cleaned in a spin-dryer to dry the wafers. This procedure removed dust and organic contaminants that may be present on the surface. It is especially important to perform this cleaning step before

photolithography, as any particulate on the surface creates streaks during the spin-coating of the photo-resist layer, causing non-uniform deposition of photo-resist. We developed (spinning) the photo-resist for 30 s in the metal-ion free (MIF) 319 developer using the ACS cluster tool. Emersion development could also be used, but the time should be increased. In order to prevent residual photo-resist left in the corner of any features, also known as "feet," we descummed the substrates for 30 s after each PR development. In any processing step that involves dry etching, the photo-resist layer was not hard-baked after the development to avoid cracking and reflowing of the film upon exposure to short-wave radiation and ions; for the photo-resist layer used as the mask during wet etching, we performed a hard-bake for 1 min at 388 K. This hard-bake removes extra solvent in the film in order to increase its structural stability and etching resistance. The removal of the photo-resist films after each fabrication process comprised of soaking the substrate in heated PRS-2000 solvent for 20 min, and an oxygen-plasma ashing for 5 min in the March Asher. The ashing condition is 250 mTorr, 250 W, and 17 % O_2 flow. It is absolutely essential to ash the photo-resist in addition to the PRS-2000 bath because both the radiation and dry etch by-product can leave insoluble residue on the surface of the film, making it difficult for the PRS-2000 to completely remove the photo-resist film. Throughout the entire fabrication of the device wafers, dummy wafers with identical films thicknesses and processing conditions were used in each step to ensure the quality and control of the amorphous silicon transistors. At the end of each subsection we will show the alignment marks, top-view picture, and schematic cross-section of the TFT at each step of the fabrication process.

2.2.1 Gate Metal Sputtering and Patterning

The TFT gate comprised of 2000 Å of sputtered chromium, which was deposited by an Enerjet Sputter at a rate of 270 Å/min on a rotational planetary platform (20 rpm). The deposition was done with a base pressure of at most 5 x 10^{-6} Torr, sputtering pressure of 7 mT, argon flow rate of about 40 sccm, and d.c. current of 3 A for 440 s. Subsequently, we lithographically patterned {GATE} and etched the gate metal using chromium etch (etch rate = ~1000 Å/min at 323 K). One observation worth noting is that the sputtered chromium can form a transparent conductive oxide on the surface of the substrate; a few extra seconds of etching was necessary after the apparent removal of the chromium metal to ensure proper electrical insulation among the features on the substrate. Figure 2-16 shows the first level alignment marks: the cross and the surrounding windows are used for the alignment, and the Vernier marks on the top and the left are used to determine the degree of misalignment among different levels of photolithography. Gate level patterning includes all the gates for the TFTs, as well as the bottom electrode for the storage capacitors in the pixel electrode circuit. Figure 2-17

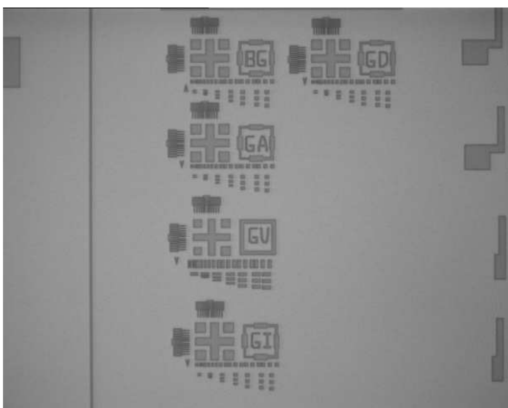

Figure 2-16: Gate level alignment and Vernier marks.

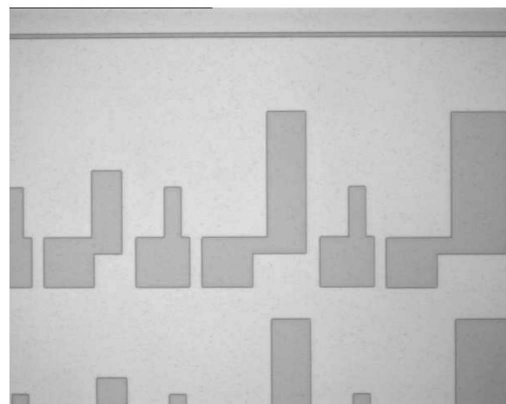
Figure 2-17: Example of TFT structures after the gate patterning.

shows the top-view of an example of thin-film transistor's gate level pattern after the completion of the chromium wet etching, and figure 2-18 shows the corresponding schematic cross-section of the TFT.

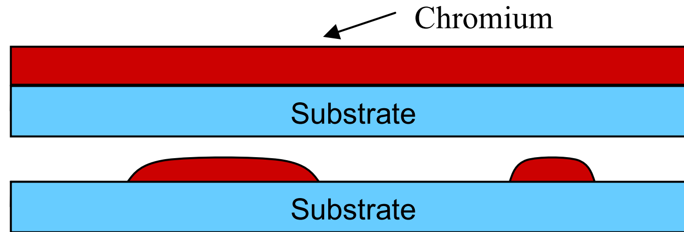

Figure 2-18: Schematic cross-section of the TFT gate metal sputtering and patterning process.

2.2.2 Plasma Enhanced Chemical Vapor Deposition

The novel amorphous silicon thin-film transistor with the tailored channel comprises of two layers of gate insulator and two layers of active material. A plasma enhanced chemical vapor deposition (PECVD) system for the commercial production of flat-panel display was used to deposit the gate insulator, amorphous silicon, and the contact layer. We deposited 3500Å of N-rich hydrogenated amorphous silicon nitride (a-SiN_X:H) at a rate of 1800 Å/min (G2) and 500Å of a-SiN_X:H at 900 Å/min (G1) as the gate insulator. Next, we deposited two layers of a-Si:H films: one at 600 Å/min (A1), and the second at 1200 Å/min (A2). A variety of plates with the following A1/A2 layer thicknesses (t_{A1}/ t_{A2}) have been fabricated: 1700/0 Å, 1600/100 Å, 1500/200 Å, 1400/300 Å, 1300/400 Å, 1200/500 Å, 1100/600 Å, and 0/1700 Å. Lastly 700 Å of 1 % phosphorous-doped amorphous silicon (n+ a-Si:H) was deposited at a uniform rate [20]. A 1000 Å of G2 encapsulation was deposited on top of the three layers to protect them

from oxygen, moisture, and organic contaminant. The film would be removed in buffered hydrofluoric acid (BHF) immediately prior to subsequent processing steps to minimize contamination (figure 2-19). The bi-layer a-SiN_X:H surface roughness (RMS value) above the gate dielectric is about 1.1 nm. Both films have slightly different film stoichiometry, but are both N-rich (N/Si > 1.3); the Si-H content in the gate dielectric deposited at lower rate is rather small (< 0.5 %). Total hydrogen content in the silicon nitride deposited at the higher rate (~36$\pm$4%) is significantly larger in comparison to the film deposited at the lower rate (~28.5$\pm$1.5%). The Tauc optical gaps for the film deposited at the higher and lower rates are about 4.6 and 5.2 eV, respectively.

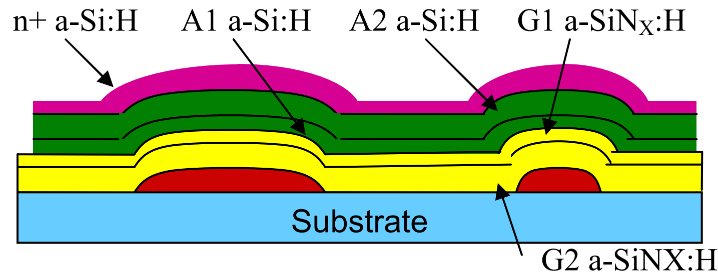

Figure 2-19: Schematic cross-section of the PECVD of G2 and G1 a-SiN_X:H, A1 and A2 a-Si:H and n+ a-Si:H films for the TFT.

2.2.3 Island Patterning

After the removal of sacrificial nitride, the island was defined {ISLAND} by photolithography, and etched with a SF_6+Cl_2+O_2+He (6:24:20:5) plasma in a LAM-9400 Transformer Coupled Plasma Reactive Ion Etcher™ (TCP-RIE). The selectivity between a-Si:H and a-SiN_X:H is approximately 21:1 for this chemistry, and with precise control of the etch time, minimal etching of the gate insulator during the definition of the amorphous silicon island can be achieved. We show the gate-to-island level alignment

mark, the top-view, and schematic cross-section view of the TFT structures after the island patterning in figures 2-20, 2-21, and 2-22, respectively.

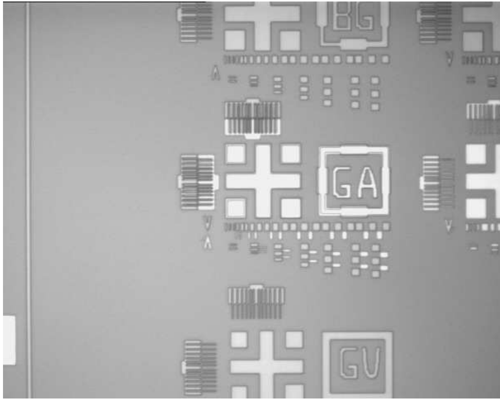

Figure 2-20: Gate-to-Island level alignment and Vernier marks.

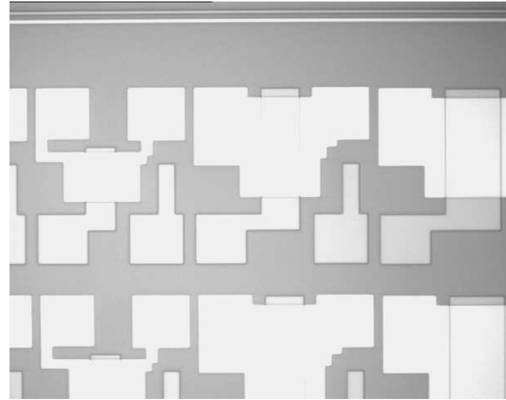

Figure 2-21: Example of TFT structures after the island patterning.

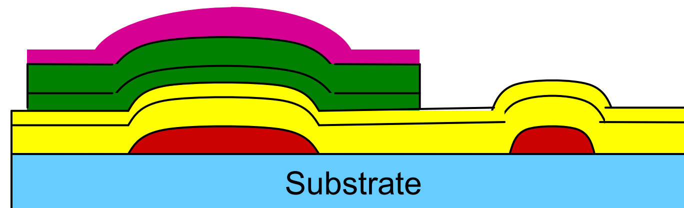

Figure 2-22: Schematic cross-section of the TFT island patterning step.

2.2.4 Gate Via Patterning

The gate via was then patterned {VIA} and etched in a PlasmaTherm Reactive Ion Etcher (PT-RIE) with a CF_4+O_2 (20:1) plasma. The etch rate is 760 Å/min and we performed a 10% over-etch to ensure that the gate via reaches all the way to the gate pad for proper electrical contact with the molybdenum to be sputtered later. However, in the middle of the etching process, wafers were rotated 180º in the reactive ion etcher to

improve the uniformity of the etching depth across the substrate. Figures 2-23 and 2-24 respectively show the gate-to-via alignment mark and the transistor structures after the gate via etch. Figure 2-25 shows the schematic cross-section of the gate via etch process.

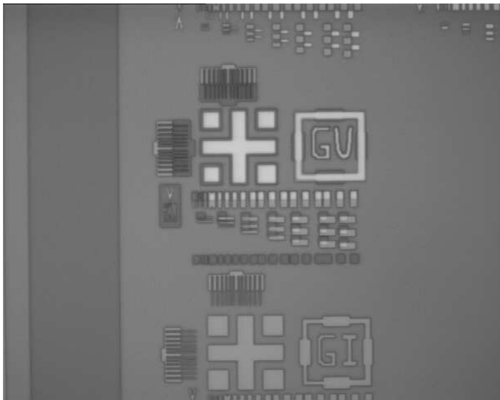

Figure 2-23: Gate-to-via level alignment and Vernier marks.

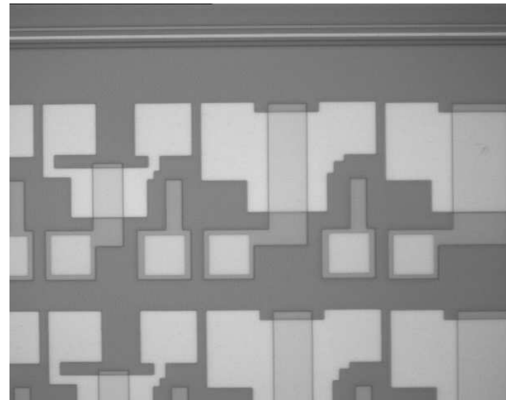
Figure 2-24: Example of TFT structures after the via patterning.

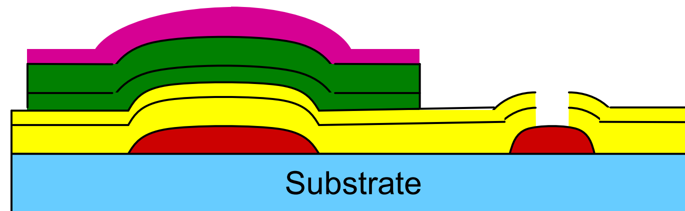

Figure 2-25: Schematic cross-section of the TFT gate via patterning process.

2.2.5 Source/Drain Metal Sputtering and Patterning

Next we perform a 100:1 H_2O:HF dip to remove any native oxide on the n+ a-Si:H; any native oxide left on the n+ layer would increase the contact resistance of the TFT. A 2000 Å thick layer of molybdenum was sputtered onto the substrates at a deposition rate of 270 Å/min; the deposition condition is similar to the sputtering of chromium described earlier for the gate metallization. This molybdenum would be used

for both source and drain contacts, as well as the gate contact pads. Afterward, we patterned and defined the source and drain of the transistor, along with their corresponding contact pads used for the electrical measurement. Molybdenum was patterned {DATA} and etched in a lukewarm (323K) Transene Type-A™ aluminum etchant made from a mixture of phosphoric (H_3PO_4), nitric (HNO_3), and acetic acid ($C_2H_4O_2$). The etch rate is about 2000Å/min. Figure 2-26 shows the cross-section schematic of the source/drain metal sputtering and etching process.

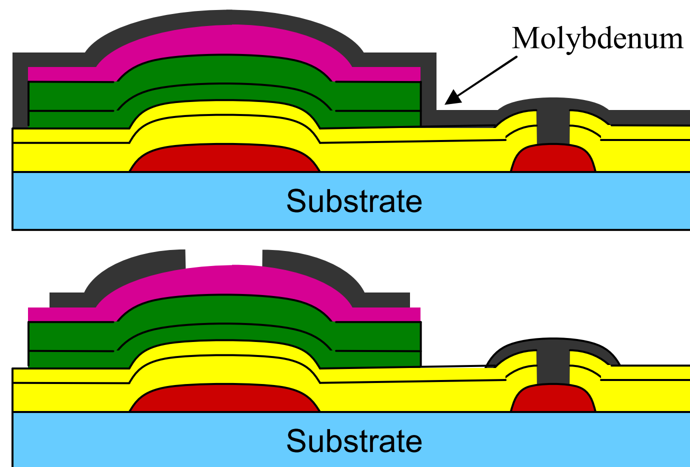

Figure 2-26: Schematic cross-section of the source/drain metal sputtering and patterning process.

2.2.6 Back Channel Etch and Thermal Annealing

Since the phosphorous atoms from the n+ layer diffuses into the amorphous silicon film in the back channel of the TFT, it is necessary to perform a back channel etch (BCE) to remove the n+ film, and a fraction of the amorphous silicon film in order to reduce the leakage current between the source and drain [21]; we dry etched, using

$HBr+Cl_2$ (1:1) as the etchant, approximately 700Å of n+ a-Si:H and 700Å of A2 in the channel region of the transistor using the LAM 9400 TCP-RIE. The n+ a-Si:H and a-Si:H dry etching will be discussed in section 4.2 in more detail. Lastly, we removed the photo-resist with heated PRS-2000, and applied an oxygen plasma treatment to the substrates to remove any organic contaminant that remained. Additionally, the amorphous silicon thin-film transistors are thermally annealed in a nitrogen oven for 1 hr at 473 K. In figures 2-27 and 2-28, we show the alignment marks for the final step of processing, and the completed structures of the a-Si:H TFT with the tailored channel. Table 2-2 summarizes the conditions and etch rates of the etching recipes used in this experiment. Figure 2-29 shows the cross-section of the final TFT structure.

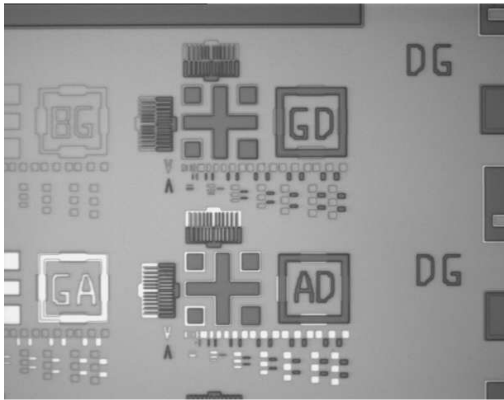

Figure 2-27: Gate-to-contact level alignment and Vernier marks.

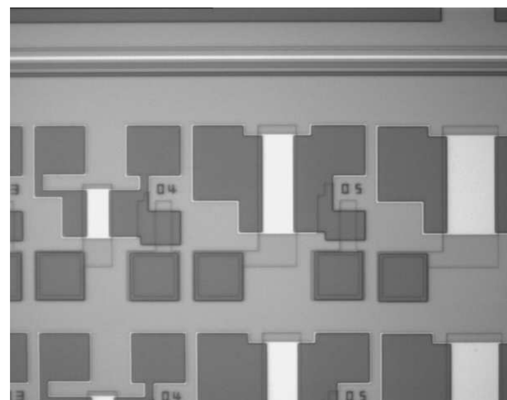

Figure 2-28: Example of TFT structures after the back channel etch.

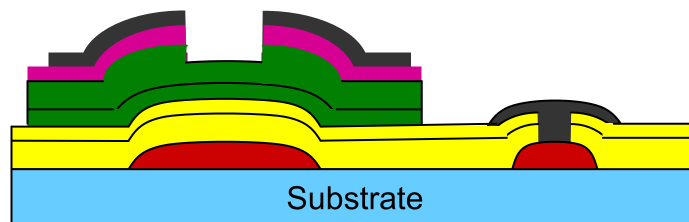

Figure 2-29: Schematic cross-section of the final TFT structure.

Table 2-2: Etching chemistry and rates used for our a-Si:H TFT fabrication process.

Material	**Etchant**	**Etch Rate**	**Comment**
Chromium	CR-14 ($C_2H_4O_2$ and $Ce\{NH_4\}_2\{NO_3\}_6$)	1000 Å/min at 323 K	Etch rate increases with temperature
a-SiN_X:H	1. BHF 2. CF_4: O_2 (20:1)	500 Å/min 760 Å/min	Requires rotation to improve etching uniformity
a-Si:H	1. SF_6:Cl_2:O_2:He (6:20:20:5) 2. CCl_2F_2:O_2 (5:1) 3. HBr:Cl_2 (3:1) 4. C_2F_6 5. KOH	1280 Å/min 150 Å/min 400 Å/min 310 Å/min ~1200 Å/min	Etch leaves organic product. Etch leaves oxide-like product. Etch rate sensitive to temperature.
n+ a-Si:H	1. SF_6:Cl_2:O_2:He (6:20:20:5) 2. CCl_2F_2:O_2 (5:1) 3. HBr:Cl_2 (3:1) 4. C_2F_6 5. KOH	1640 Å/min 300 Å/min 680 Å/min 350 Å/min ~1500 Å/min	Etch leaves organic product. Etch leaves oxide-like product. Etch rate sensitive to temperature.
Molybdenum	Al Etch 4 (H_3PO_4, HNO_3, and $C_2H_4O_2$)	2000 Å/min at 323 K	Etch rate increases with temperature

2.3 Amorphous Silicon TFT CHARACTERIZATION

2.3.1 Measurement Setup

The thin-film transistor current-voltage (I-V) characteristics measurement setup is shown in figures 2-25. All I-V characteristics were measured using Agilent 4156A and

4156C Semiconductor Parameter Analyzers. The capacitance-voltage (C-V) relations were measured using Agilent 4284A Precision LCR Meter.

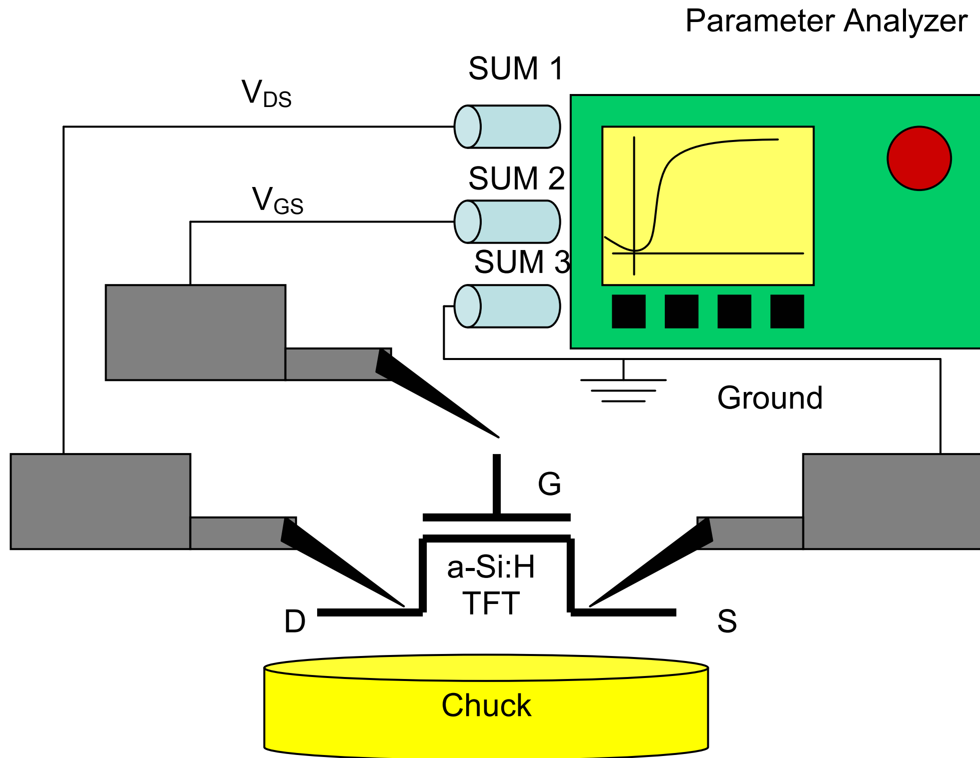

Figure 2-30: Schematic of TFT I-V measurement setup.

2.3.2 Electrical Parameter Extraction - Linear Fit

The linear and saturation region TFT characteristics are shown below:

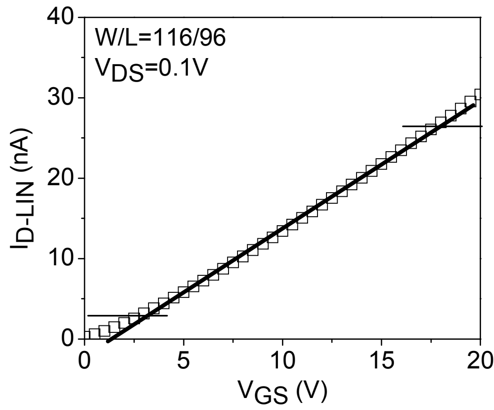

Figure 2-31: Linear region transfer characteristics of TFT: data (figure) and linear fit (line).

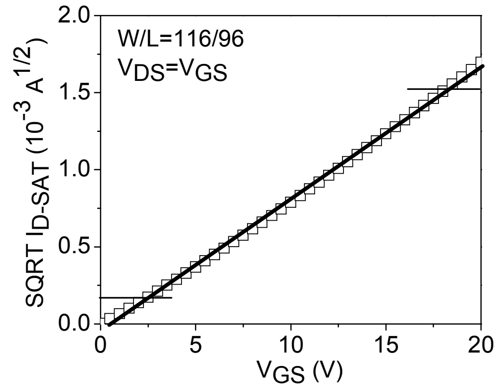

Figure 2-32: Saturation region transfer characteristics of TFT: data (figure) and linear fit (line).

We use data points within 10-90 % of the maximum drain current of the transfer characteristics to extract device parameters using the following square law equations for the linear and saturation regions of operations:

$$I_{D\text{-}LIN} = (W/L\ C_{INS}\ V_{DS})\ \mu_{EFF}\ (V_{GS}\text{-}V_T), \tag{2-6}$$

and

$$I_{D\text{-}SAT} = [W/2L\ C_{INS}]^{1/2} \mu_{EFF}^{1/2}\ (V_{GS}\text{-}V_T). \tag{2-7}$$

In the two equations shown, W, L and C_{INS} denote the transistor's channel width in μm, length in μm, and gate insulator capacitance in the unit of F/cm^2, respectively. V_{GS} and V_{DS} are the externally applied gate and drain biases with respective to the source, and μ_{EFF} and V_T are the electrical performance parameters field-effect mobility and threshold voltage measured in cm^2-V^{-1}-s^{-1} and V, respectively. The reason for choosing to fit 10-90 % of the experimental data to the square law equations shown above is that amorphous silicon transfer characteristics, in both linear and saturation regions, can deviate from the ideal linear behavior. By specifying the data range used for the linear

parameter extraction, we are able to extract the TFTs' electrical performance without being influenced by the curvatures of the transfer characteristics, which can mask the true field-effect mobility and threshold voltage values.

2.3.3 Electrical Parameter Extraction – Quadratic Fit

Another method of extracting device electrical parameters is using a quadratic equation to fit the same experimental data. As mentioned in the previous section, the TFT transfer characteristics can deviate from the ideal linear form. To compensate for this, we introduce a power fitting factor to the above square law equations. The equation used for the power fitting of the TFT characteristics in the linear region is:

$$I_{D\text{-}LIN} = (W/L\ C_{INS}\ V_{DS})\ \mu_{EFF}\ (V_{GS}-V_T)^{\gamma} = a\ (x\text{-}b)^c, \qquad (2\text{-}8)$$

where a is proportional to the field effect mobility, b is the threshold voltage, and c is the gamma factor (γ). The equation used for the power fitting of the TFT characteristics in the saturation region is:

$$I_{D\text{-}SAT} == [W/2L\ C_{INS}]^{1/2} \mu_{EFF}^{1/2}\ (V_{GS}-V_T)^{(1+\gamma)/2} = a\ (x\text{-}b)^c, \qquad (2\text{-}9)$$

where a^2 is proportional to the field effect mobility, b is the threshold voltage, and 2c-1 is the gamma factor (γ).

We can also use gamma to obtain the characteristic temperature, T_O, of amorphous silicon density of stations distribution near the Fermi level by using the equation [22],

$$\gamma = 2T_O/T - 1. \qquad (2\text{-}10)$$

The characteristics temperature reflects the slope of the conduction band-tail states: T_O increases as the width of the slope increases. In the ideal case T_O should equal to T,

indicating that γ=1, which is equivalent to the c-Si MOSFET behavior. The solid line on each plot represents the fit and the symbols represent the actual experimental data points.

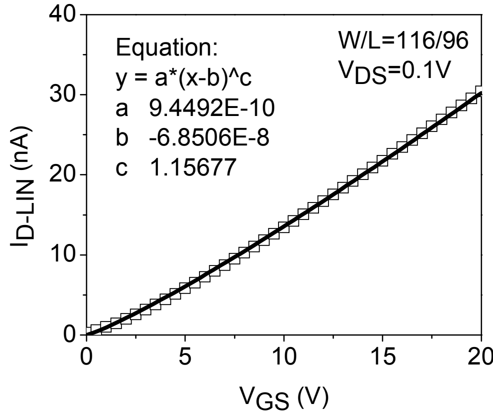

Figure 2-33: Linear region transfer characteristics of TFT: data (figure) and fit (line).

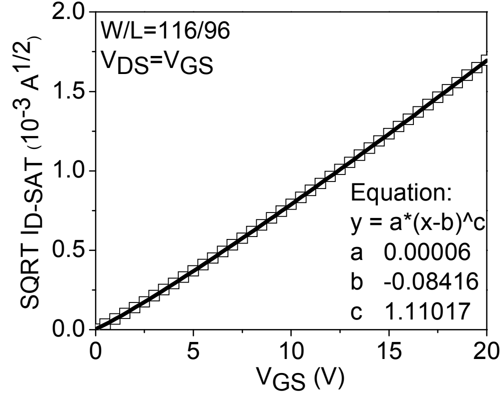

Figure 2-34: Saturation region transfer characteristics of TFT: data (figure) and fit (line).

2.3.4 Conductance Method

Even the transistors field-effect mobility and threshold voltage can be extracted quickly using the linear and the quadratic extraction methods described in sections 2.3.2 and 2.3.3, there is another method that provides a more intuitive link between the TFT transfer characteristics and its electrical parameters. This is the conductance method. Rather than fitting a line to the transfer characteristics, we take the derivative of the drain current with respect to the gate voltage [23],

$$\frac{\delta\sigma_{CH}}{\delta V_{GS}} = \frac{W}{L} C_{INS} V_{DS} \mu_{EFF}(V_{GS}) . \tag{2-11}$$

By using this method we are able to obtain the field-effect mobility values as a function of the gate biases. Since this method is used exclusively in chapter 3 of this dissertation, more details will be provided in section 3.2.

2.3.5 Subthreshold Swing and Off-Current Extraction

The subthreshold swing, S, was extracted from the transfer characteristics on a LOG-LIN scale, at a selected current value. For every transfer curve, we choose three or more data points near the dashed lines, and fit a line to those points. The line yields a slope value, and the inverse of the slope is the subthreshold swing of the device, in unit of V/dec

$$S = (\delta \log(I_D)/\delta V_{GS})^{-1}. \quad (2\text{-}12)$$

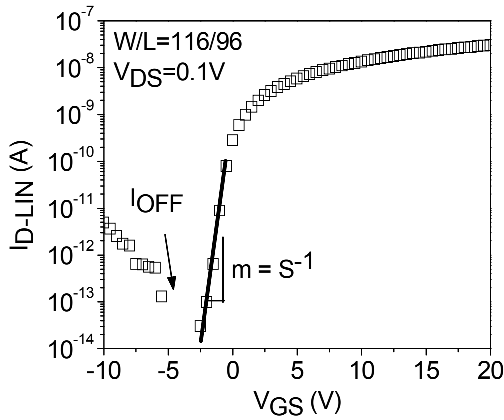

Figure 2-35: Linear region transfer characteristics of TFT on semi-log plot.

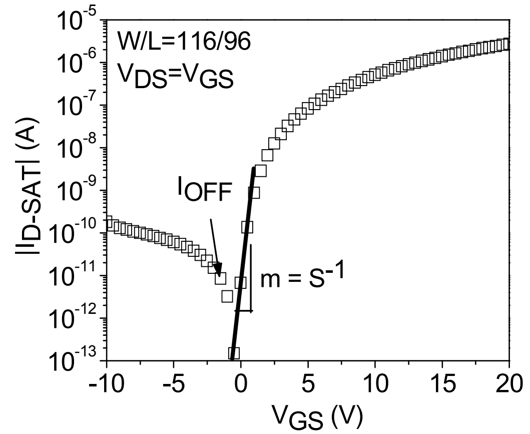

Figure 2-36: Saturation region transfer characteristics of TFT on semi-log plot.

Both linear and saturation region values can be extracted the same way. From the subthreshold swing value, we can also predict the maximum density of states

$$N_{SS}^{max} = [(S \log(e))/(kT/q)-1]\, C_{INS}/q^2, \quad (2\text{-}13)$$

where S in the subthreshold swing. Off-current, I_{OFF}, is the minimum current in the off region of the transfer characteristics.

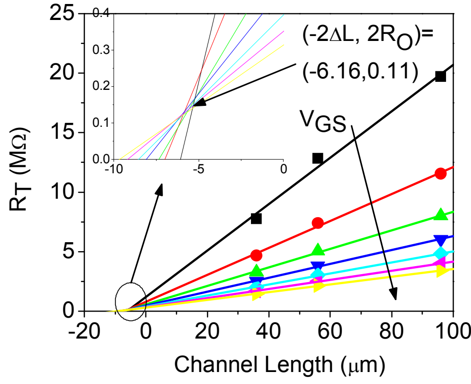

Figure 2-37: Total resistance for different TFT channel lengths.

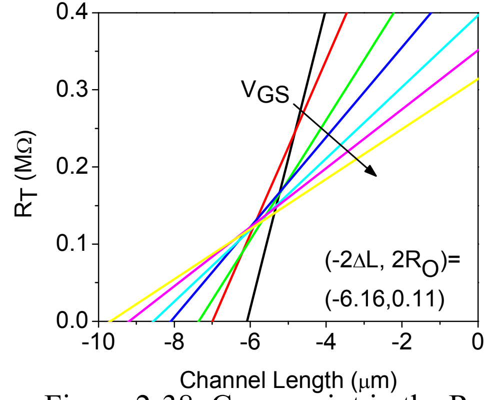

Figure 2-38: Cross-point in the R_T vs. L plot indicating ΔL and R_O.

2.3.6 Intrinsic Device Characteristic Extraction

To perform a complete analysis of the TFT contact resistance, we first plot the overall resistance R_T versus the channel length of the device on a linear-linear scale for different V_{GS} and low V_{DS} (Figure 2-37) [24].

$$R_T = V_{DS}/I_D = L/(\mu_i\, C_{INS}\, W\, (V_{GS} - V_{T\text{-}i})) = r_{ch}\, L + 2R_{S/D}. \quad (2\text{-}14)$$

This equation allows us to draw straight lines of each curve, in which the y-intercept is the total contact resistance ($R_{S/D} = R_S + R_D$) for that given voltage, and the slope is the channel resistance r_{ch} in units of $\Omega\ cm^{-1}$. If we extend the fitting lines pass the y-axis into the second quadrant, we can locate a cross-point of all the lines. This cross-point gives us ΔL, which is associated with the difference in the actual channel length and the masked channel length. For the typical a-Si:H TFT structure, drain current flows underneath the source/drain contacts before being collected. The total extension of the drain current underneath the source and the drain contacts equals to the ΔL value. Notice that the extracted ΔL for a-Si:H TFT's has a positive value. Another parameter to be extracted from the cross-point is the R_O, or the minimum source/drain contact resistance (Figure 2-

38). We can see from figures that the contact resistance is a function of gate bias and decreases with increasing gate bias.

We can further analyze the device by extracting the intrinsic threshold voltage and mobility. This can be done by plotting the channel conductance of the devices ($1/r_{ch}$) versus the gate bias:

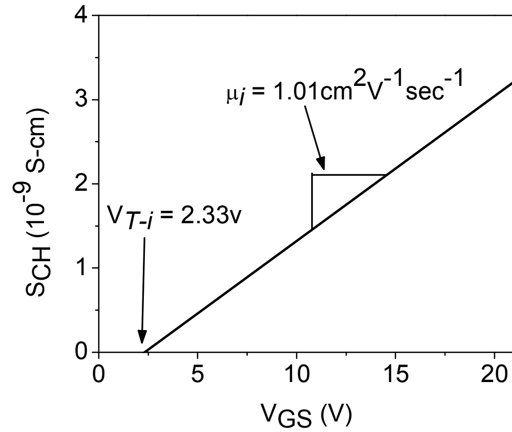

Figure 2-39: Extraction of intrinsic mobility and threshold voltage from the channel conductance.

$$r_{ch} = 1/(\mu_{FE\text{-}i}\, C_{INS}\, W\, (V_{GS} - V_{T\text{-}i}), \quad (2\text{-}15)$$

or equivalently,

$$S_{ch} = \mu_{FE\text{-}i}\, C_{INS}\, W\, (V_{GS} - V_{T\text{-}i}) \quad (2\text{-}16)$$

where S_{ch} is the inverse slope obtained from R_T versus L curve (figure 2-39). We obtain a linear fit of all the points above threshold voltage. The slope of the line is proportional to the intrinsic mobility and the x-intercept is the intrinsic threshold voltage.

Another useful TFT parameter to calculate is the transfer length L_T, which is the characteristics length of the source/drain overlap,

$$L_T = R_{S/D} / (r_{ch} \coth (d/L_T)), \quad (2\text{-}17)$$

where d is the physical source/drain overlap. This equation can be solved iteratively. Lastly we can obtain the effective contact resistance by using the equations

$$R_{Ceff} = W\, L_T^2\, r_{ch}, \quad (2\text{-}18)$$

and for the optimum effective contact resistance ($V_{GS}>>0$)

$$R_{Ceff} = W\, R_O\, |\Delta L|. \tag{2-197}$$

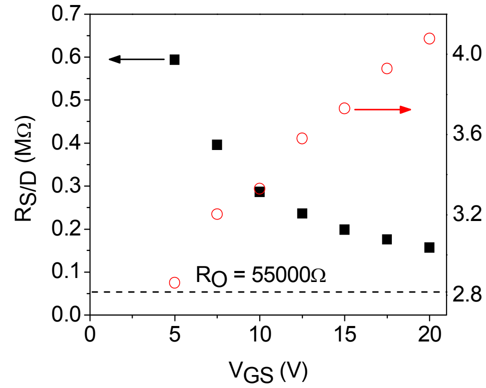

Figure 2-40: Contact resistance and effective length plot versus gate voltage.

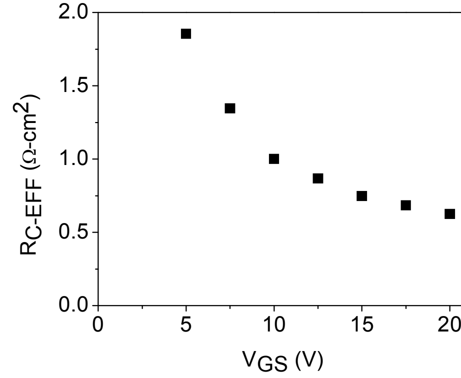

Figure 2-41: Specific contact resistance versus gate voltage plot.

From the figures and equations shown above, the following parameters can be extracted:

$V_{T\text{-}i} = 2.33$ V

$\mu_i = 1.01\ cm^2/Vs$

$R_O = 55000\ \Omega$

$R_{Ceff}\ (V_{GS} = 20V) = 0.63\ \Omega\ cm^2$.

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Chapter 3:

Channel Tailoring

3.1. Introduction

As the active-matrix liquid crystal display (AM-LCD) industry begins to introduce large-size and high-pixel-density displays, the demand for a high performance amorphous silicon thin-film transistor mounts. In order for the a-Si:H TFT to remain competitive in the flat-panel display industry, it is necessary to realize transistors with a high mobility and a low threshold voltage, while being able to be fabricated at a high rate [1]. These qualities allow the possibility of manufacturing large-size displays with low power consumption, at relatively low costs. Fabricating high performance a-Si:H TFTs requires a high electronic quality a-Si:H film, as the electrical characteristics of a TFT is intimately related the electronic quality of the a-Si:H film [2]. Even though a high electronic quality film can be achieved by lowering its deposition rate, doing so increases the overall production time. In the AM-LCD industry, the inverted staggered back-channel-etched type transistor structure is preferred over the tri-layer type transistor structure because of its reduced photolithography step and improved source/drain contact quality [3]. This structure requires the deposition of a thicker amorphous silicon film for better control of the back channel etch step [4]. However, a thicker amorphous silicon film for the TFT means a longer deposition time, which also leads to a lower production

output and higher overall costs for the AM-LCD industry [5]. Deposition time can be shortened by increasing the deposition rate of the film, but doing so degrades the mobility and threshold voltage of the transistor [6]. Similarly, the gate insulator amorphous silicon nitride should exceed 4000Å to reduce the gate leakage, but its deposition rate needs to be low in order for the a-Si:H TFT to have a high electronic quality a-SiN_X:H/a-Si:H interface for optimal threshold voltage, subthreshold swing, and electrical stability [7]. It is therefore desirable to strike a compromise between the TFT's electrical performance and the production throughput by depositing thick a-SiN_X:H and a-Si:H films in the shortest possible time without degrading the overall electrical characteristics of the a-Si:H TFT. One potential solution is depositing two amorphous silicon films as the active layer, and two silicon nitride as the gate insulator. For the a-Si:H, we deposit a thin layer of a low-deposition-rate film near the gate insulator interface in order to obtain high electronic quality a-Si:H film near the electron conduction channel, and a thick layer of high-deposition-rate film in the back channel to be used as the sacrificial layer during the etch back process. The a-SiN_X:H deposition is also separated into a two-step process: a thin layer of low deposition rate film near the high electronic quality a-Si:H film for high electrical performance and stability, and a thick layer of high deposition rate film near the gate metal to reduce the gate leakage current.

The concept of the double a-Si:H layer structure for TFT was first proposed by Takeuchi and Katoh for the purpose of reducing a-Si:H TFT photo-response [8, 9]. Characteristic of the dual amorphous silicon TFT was explored further by Kashiro *et al.,* and it was concluded that the field effect mobility is highly sensitive, and linearly proportional (up to 15nm), to the thickness of a high quality a-Si:H layer [10]. This

dependency was attributed to the effect of the low quality film's inferior electronic states, which influences the overall surface band-bending extending from the a-SiN_X:H/a-Si:H interface. Tsai *et al.* investigated the effect of the low quality film deposition rate on the overall electrical performance of the dual layer a-Si:H TFT [11], and concluded that with the increasing deposition rate the TFT's field-effect mobility decreases because of the same explanation proposed by Kashiro. From the results of the above study it is clear that dual a-Si:H layer TFT's electrical performance can suffer due to the inclusion of the low quality film away from the a-SiN_X:H/a-Si:H interface.

In this chapter we analyze in detail the a-Si:H TFT with dual a-Si:H and dual a-SiN_X:H layers. The majority of this transistor's PECVD film is deposited at very high rates to reduce its overall production time. However, two low-deposition-rate films, one a-Si:H and one a-SiN_X:H, near the conduction channel are included to tailor the front interface region of the TFT. We extract the electrical behaviors of our a-Si:H TFT with the tailored channel, and analyze the effect of high quality amorphous silicon film thickness on the overall transistor performance by evaluating its intrinsic and extrinsic characteristics [12]. Based on the result, we can quantify the effect of the high electronic quality a-Si:H thickness on the transistor's mobility, threshold voltage, subthreshold swing, and contact resistance, and identify the minimum thickness of the high electronic quality a-Si:H layer required for the TFT to exhibit promising device performance, without unnecessarily extending the deposition time.

3.2. Traditional Amorphous Silicon TFT Performance

Before we begin introducing the a-Si:H TFT with the tailored channel, we first present the electrical performance of the traditional transistors fabricated with A1 and A2 films alone. These transistors have identical gate insulator composition and thicknesses, W/L ratio, gate and top contact metals, and gate-to-drain and gate-to-source overlaps. The only difference is the active layer structure and material: TFTs made with all A1 (1700 Å) and A2 a-Si:H (1700 Å) are denoted as TA1, and TA2, respectively. As mentioned earlier, A1 amorphous silicon has a lower deposition rate than A2. We expect its electronic quality to be higher. This implies that the A1 film should have better microcrystalline order, lower band-gap, and lower densities of band-tail and deep-gap states. Logically, this advantage in its electronic quality should be highlighted by the superior electrical behavior of TA1.

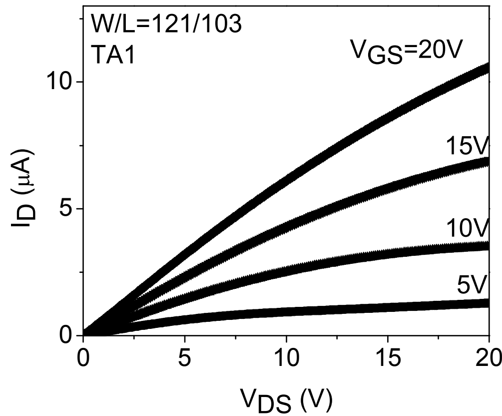

Figure 3-1: Output characteristics of TA1.

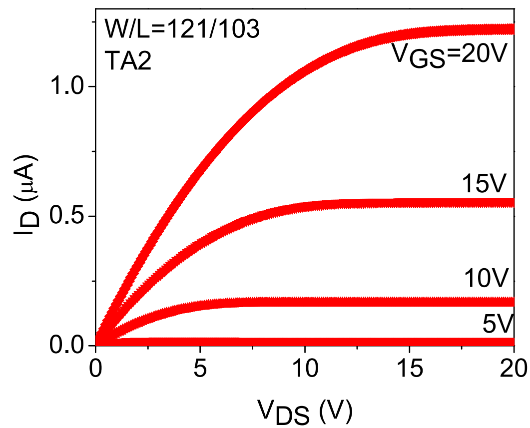

Figure 3-2: Output characteristics of TA2.

Figures 3-1 and 3-2 show the respective output characteristics of TA1 and TA2 for gate biases ranging from 5 to 20 V. We can see from the linear region transfer characteristics of TA1 and TA2 shown in figure 3-3 that the active material has a significant effect on the electrical performance of the TFT. TA1 has noticeably superior electrical performance than TA2. Its field effect mobility, threshold voltage, and subthreshold swing values are 0.94 cm^2 V^{-1} s^{-1}, 1.18 V, and 0.49 V/dec, respectively. TA2 has much inferior electrical parameters: μ_{EFF} of 0.65 cm^2 V^{-1} s^{-1}, V_T of 4.78 V, and S of 0.71 V/dec.

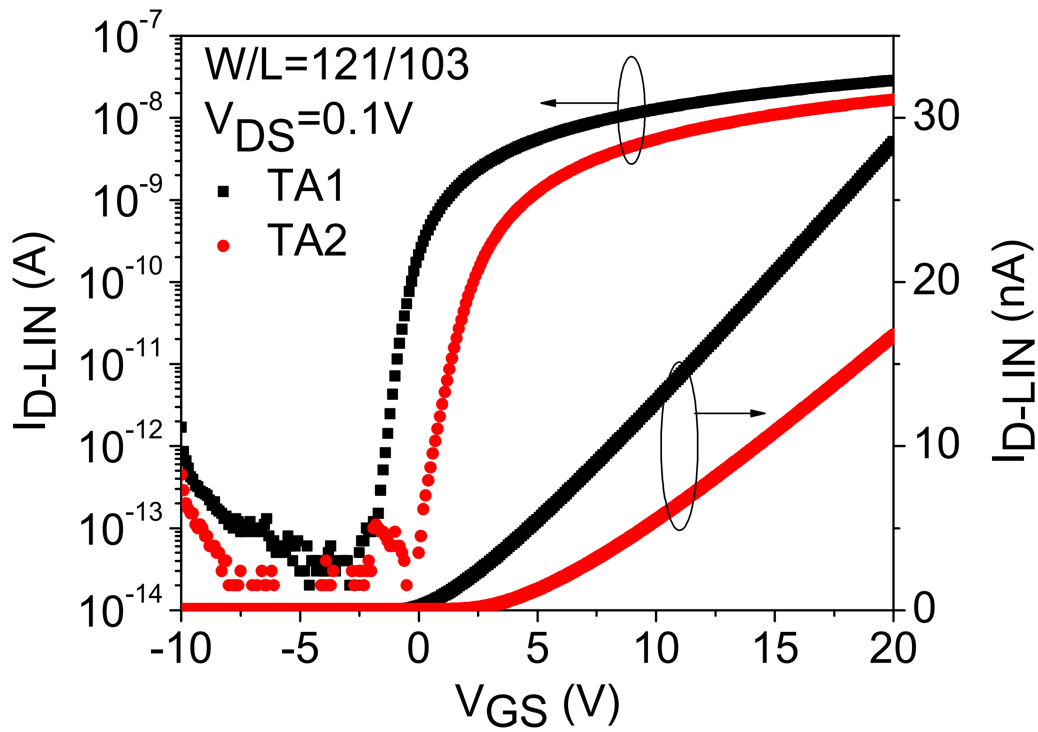

Figure 3-3: Linear region transfer characteristics of traditional transistors fabricated with only low-deposition-rate (TA1) and high-deposition-rate (TA2) amorphous silicon films.

3.3. TFT Parameter Extraction Methodology

Since the goal of this study focuses on the change in a-Si:H TFT performance with respect to t_{A1}, it is imperative that we first develop accurate parameter extraction techniques that represent the true TFT electrical behaviors. Changes observed, if any, should be solely due to differences caused by electrical properties change originating from varying t_{A1}, not artificial effects contributed by the parameter extraction method. In addition to the linear method mentioned in the previous chapter, we are introducing the conductance method for the TFT electrical characteristics extraction [13-15]. When extracting a-Si:H TFT parameter via the linear method, as explained earlier, a line fits the experimental data points of the I_D-V_{GS}, or transfer, characteristic in the linear region (figure 3-4) or $[I_D\text{-}V_{GS}]^{1/2}$ characteristic in the saturation region (figure 3-5); the data range selected is between 10-90% of the maximum drain current. The fitting line represents MOSFET square law equations:

$$I_{D-LIN} = \frac{W}{L} C_{INS} \mu_{FE1-LIN} \left[V_{GS} - V_{T1-LIN}\right] V_{DS-LIN} \tag{3-1}$$

$$I_{D-SAT}^{1/2} = \left[\frac{W}{2L} C_{INS} \mu_{FE1-SAT}\right]^{1/2} \left[V_{GS} - V_{T1-SAT}\right] \tag{3-2}$$

where W, L, and C_{INS} symbolize the a-Si:H TFT channel width, length, and gate insulator capacitance, respectively. Field-effect mobility values in the linear and saturation regions of operation are denoted as $\mu_{FE1-LIN}$ and $\mu_{FE1-SAT}$; similarly the threshold voltage values in each region of operation are represented by V_{T1-LIN} and V_{T1-SAT}. The symbols V_{GS} and V_{DS-LIN} are the gate and drain biases with respect to the source terminal of the TFT.

From the equations above it is clear that from the slope of the fitting line to the transfer

characteristic, we can extract the field-effect mobility values, and the x-intercept yields the threshold voltage.

The second method of parameter extraction is based on the conductance of the a-Si:H TFT. We begin by defining the linear region channel conductance (σ_{CH-LIN}) of the device from the square law current equation:

$$I_{D-LIN} = \frac{W}{L} C_{INS} \mu_{FE2-LIN} \left[V_{GS} - V_{T2-LIN} \right] V_{DS-LIN} \quad (3\text{-}3)$$

$$\sigma_{CH-LIN} \equiv \frac{\delta I_{D-LIN}}{\delta V_{DS-LIN}} = \frac{W}{L} C_{INS} \mu_{FE2-LIN} \left[V_{GS} - V_{T2-LIN} \right] \quad (3\text{-}4)$$

where $\mu_{FE2-LIN}$ is the linear region field-effect mobility. To obtain the field-effect mobility we take the derivative of the channel conductance with respect to the gate bias (figure 3-4):

$$\frac{\delta \sigma_{CH-LIN}}{\delta V_{GS}} = \frac{W}{L} C_{INS} \mu_{FE2-LIN} . \quad (3\text{-}5)$$

It should be clarified that the two separate field effect mobility notations are used for the same square law equation to distinguish the difference in extraction method: $\mu_{FE1-LIN}$ in (3-1) is a constant value with respect to V_{GS} and $\mu_{FE2-LIN}$ from (3-5) varies with the gate bias. The threshold voltage extraction from the conductance method (V_{T2-LIN}) is done by taking the derivative of (3-5) with respect to V_{GS}, and defining the maximum value as the threshold voltage. This choice is based on the fact that the channel conductance changes with the gate bias, as shown in figure 3-4. By defining threshold voltage as the maximum value on the $\frac{\delta \sigma^2_{CH-LIN}}{\delta V^2_{GS}}$ plot, we incorporate a physical origin to the threshold voltage parameter as the specific point where the maximum change in channel conductance with the gate bias occurs.

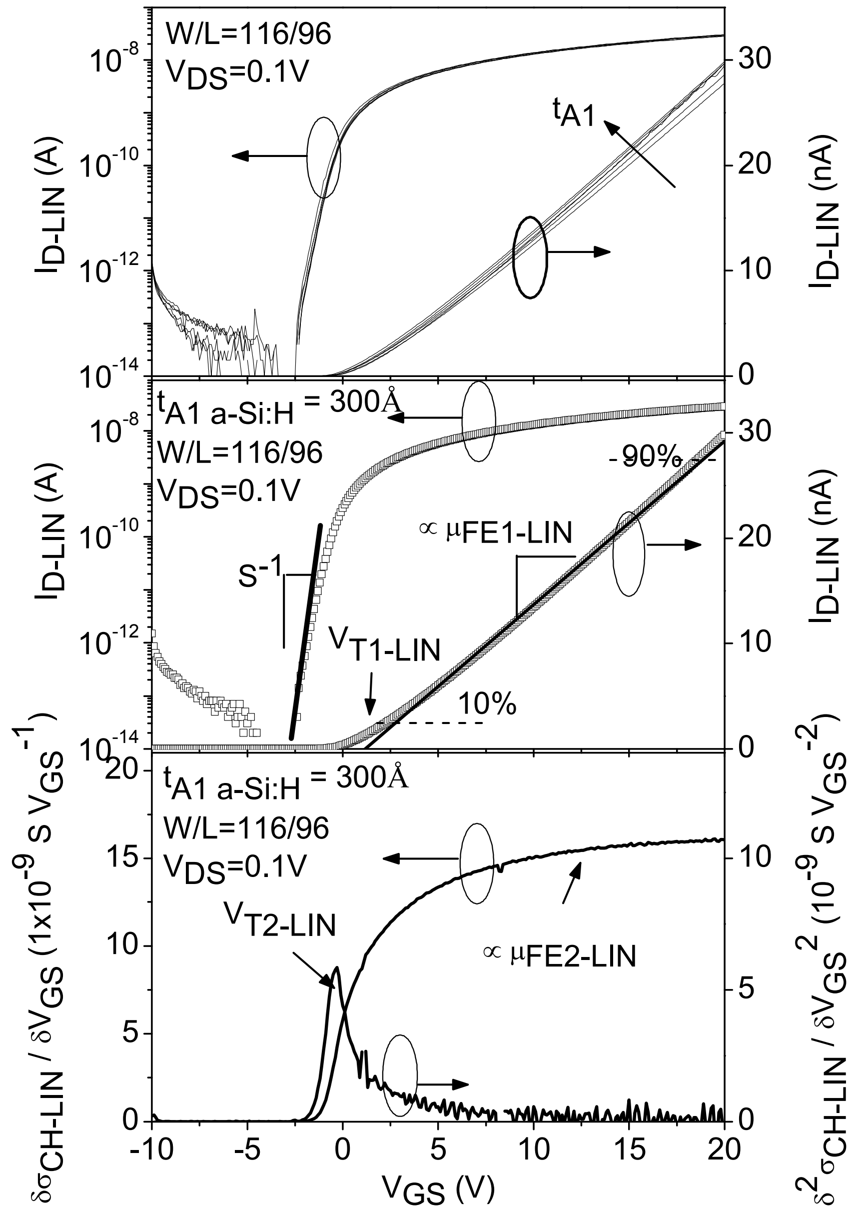

Figure 3-4: Linear region transfer characteristics of a-Si:H TFT with different A1 and A2 a-Si:H thicknesses (top). Experimental data points are intentionally displayed as thin lines to show the variations among different transistors. Demonstration of parameter extraction using the linear method for a TFT with t_{A1} of 300Å is also included: figures represent data points collected and lines represent fitting equations. Demonstration of parameter extraction using the conductance method: calculated $\delta\sigma_{CH-LIN}/\delta V_{GS}$ and $\delta^2\sigma_{CH-LIN}/\delta V^2_{GS}$ curves for a TFT (bottom) used in this experiment.

Field-effect mobility extraction in the saturation region ($\mu_{FE2-SAT}$) also begins with the square law current equation:

$$I_{D-SAT} = \frac{W}{2L} C_{INS} \mu_{FE2-SAT} [V_{GS} - V_{T2-SAT}]^2 . \tag{3-6}$$

Since $V_{DS-SAT} = V_{GS} - V_{T2-SAT}$ and $dV_{DS-SAT} = dV_{GS}$, the channel conductance in the saturation region is

$$\sigma_{CH-SAT} \equiv \frac{\delta I_{D-SAT}}{\delta V_{DS-SAT}} = \frac{W}{L} C_{INS} \mu_{FE2-SAT} [V_{GS} - V_{T2-SAT}], \tag{3-7}$$

and the change in channel conductance with respect to the gate bias is

$$\frac{\delta \sigma_{CH-SAT}}{\delta V_{GS}} = \frac{W}{L} C_{INS} \mu_{FE2-SAT} . \tag{3-8}$$

Figure 3-5 shows the extractions of field-effect mobility from the $\frac{\delta \sigma_{CH-SAT}}{\delta V_{GS}}$ plot and threshold voltage (V_{T2-SAT}) from the $\frac{\delta \sigma^2_{CH-SAT}}{\delta V^2_{GS}}$ plot. Both $\mu_{FE2-LIN}$ and $\mu_{FE2-SAT}$ values are extracted from the conductance curves at the maximum conductance value; in both cases maximum values occur at V_{GS}=20V. It should be noted that the conductance method is only used in this chapter to compliment the linear method. Subthreshold swings for linear and saturation regimes of operation are defined as the inverse values of the steepest slopes of the respective I_D-V_{GS} semi-log plots.

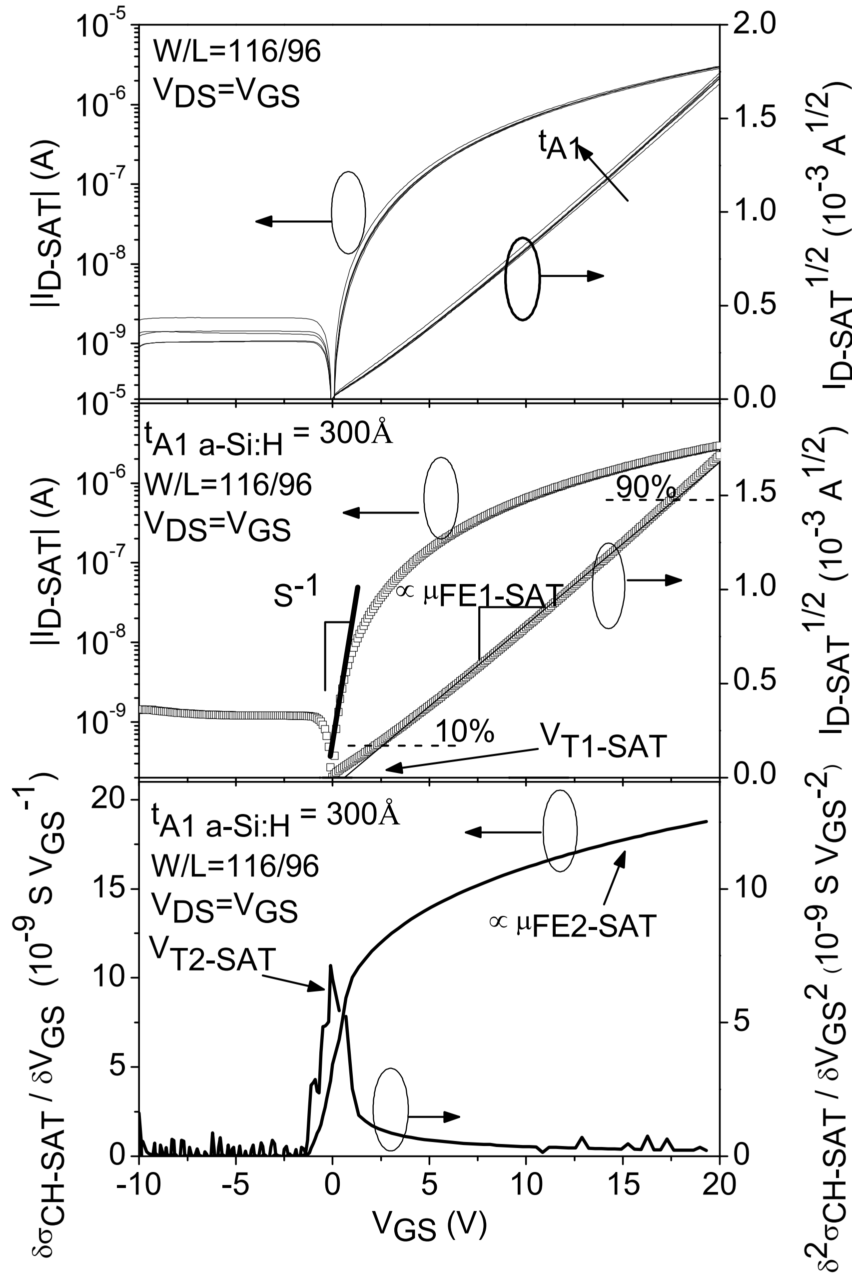

Figure 3-5: Saturation region transfer characteristics of a-Si:H TFT with different A1 and A2 a-Si:H thicknesses (top). Experimental data points are intentionally displayed as thin lines to show the variations among different transistors. Demonstration of parameter extraction using the linear method for a TFT with t_{A1} of 300Å: figures represent data points collected and lines represent fitting equations. Demonstration of parameter extraction using the conductance method: calculated $\delta\sigma_{CH\text{-}SAT}/\delta V_{GS}$ and $\delta^2\sigma_{CH\text{-}SAT}/\delta V^2_{GS}$ curves for a TFT (bottom) used in this experiment.

For the intrinsic parameter extraction, we use the transmission line method (TLM). Detail description of the method has been described in chapter 2 of this dissertation. We show examples of the data obtained by utilizing TLM in figures 3-6 and 3-7, plus the equation for total resistance (R_T) of a-Si:H TFT during the linear region of operation [16]:

$$R_T = \frac{V_{DS}}{I_D} = r_{CH}(V_{GS})L + 2R_C(V_{GS}) = \frac{L}{W\mu_i C_{INS}(V_{GS} - V_{T-i})} + 2R_C(V_{GS}). \quad (3\text{-}9)$$

In (9) $r_{CH}(V_{GS})$, $R_C(V_{GS})$, μ_i, and V_{T-i} represent the channel resistivity, total contact resistance, intrinsic mobility, and intrinsic threshold voltage, respectively.

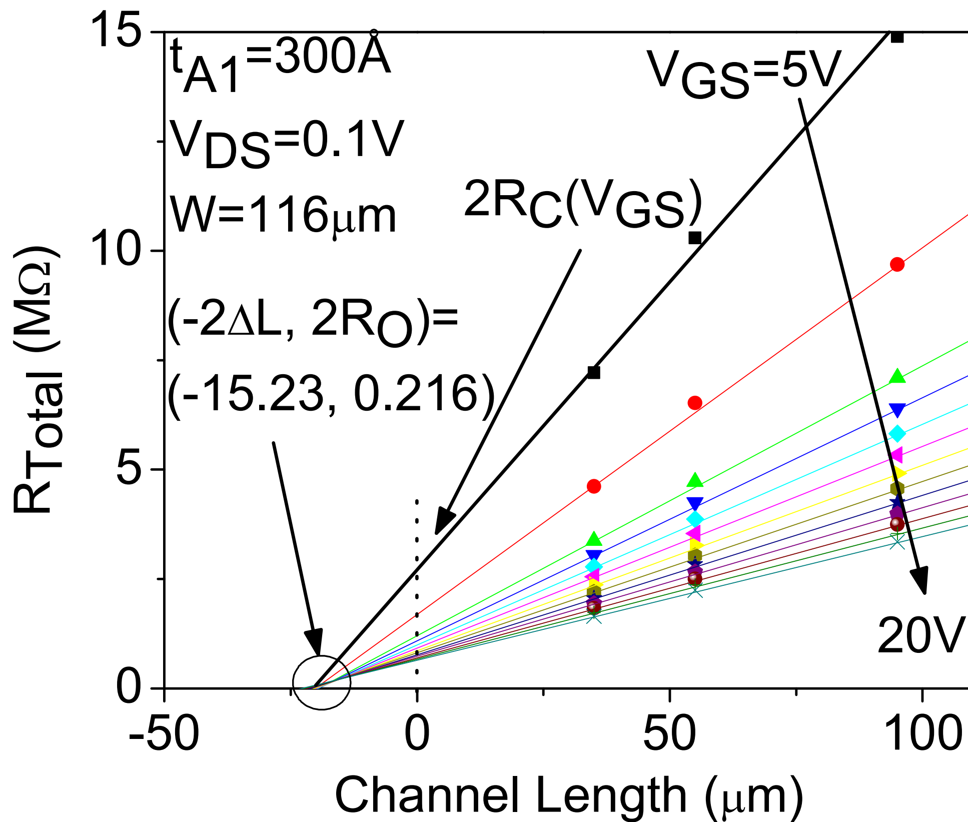

Figure 3-6. Example of R_{TOTAL}, r_{CH}, $R_C(V_{GS})$, R_O, and ΔL value extraction using TLM.

From figure 3-6, we can obtain the values of $r_{CH}(V_{GS})$ and $R_C(V_{GS})$ for a given gate voltage from the slope and the y-intercept, respectively, of a fitted line for the total resistance values of transistors with different channel lengths. The minimum contact resistance (R_O) and the effective channel length change (ΔL) are extracted from the intersection of all the R_T fitted lines. Channel conductivity, $S_{CH}(V_{GS})$, is equal to the inverse value of the channel resistivity. One point worth noting is that due to the geometry of the TFT near its source and drain contacts, the actual transistor channel length is not the masked channel length L, but L+ΔL. From plotting the channel conductance values with respect to gate bias, and performing a linear fit to the data points, we can extract the intrinsic mobility and threshold voltage values respectively from the slope and the x-intercept of the best-fit line (figure 3-7).

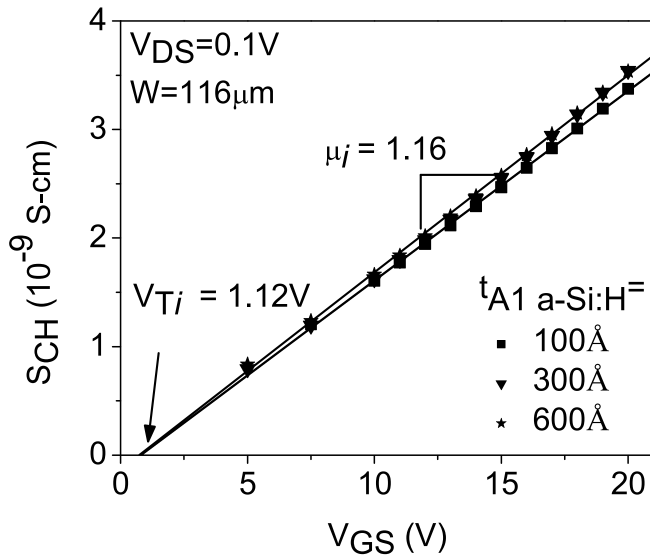

Figure 3-7. Extraction of an a-Si:H TFT's (t_{A1}=100, 300, 600Å) intrinsic mobility and threshold voltage by using channel conductivity versus gate voltage plot: symbols and lines represent experimental data and the best-fit line, respectively. Values of intrinsic mobility and threshold voltage shown belong to TFT with t_{A1} of 600Å.

3.4. Results and Discussion

From the linear region transfer characteristics of the a-Si:H TFTs shown in figure 3-4 (top), there is a slight increase in the drain current with t_{A1}. The same trend can be seen from the saturation region transfer characteristics in figure 3-5 (top). Changes in extrinsic threshold voltage and the subthreshold swing, however, are inconspicuous from observing the I-V characteristics. Figure 3-6 shows the values of $R_C(V_{GS})$, R_O, $S_{CH}(V_{GS})$, and ΔL of two a-Si:H TFTs: examples shown here are for transistors with t_{A1} of 100 (top) and 300 Å (bottom). Both channel resistivity and contact resistance values decrease as V_{GS} increases. Figure 3-7 shows the conductance plots and the values of the intrinsic mobility and threshold voltage for the TFTs shown in figure 3-6. Summary of the results for the TFT extrinsic and intrinsic extractions are shown in figure 3-8.

We observe five important facts regarding the influence of the low-deposition-rate amorphous silicon thickness on the performance of the TFT: 1) both linear and saturation region field-effect mobility values increase linearly by 5-9%, depending on the extraction method, from t_{A1} of 100 to 300 Å, and remain the same beyond that thickness, 2) the a-Si:H thickness has different effect on the threshold voltage, which depends on the extraction method, 3) the subthreshold swing decreases with increasing t_{A1}, 4) the contact resistance does change with t_{A1}, but such change depends on the applied gate bias, and 5) the ΔL increases from 6.5 to 10 µm with increasing t_{A1}.

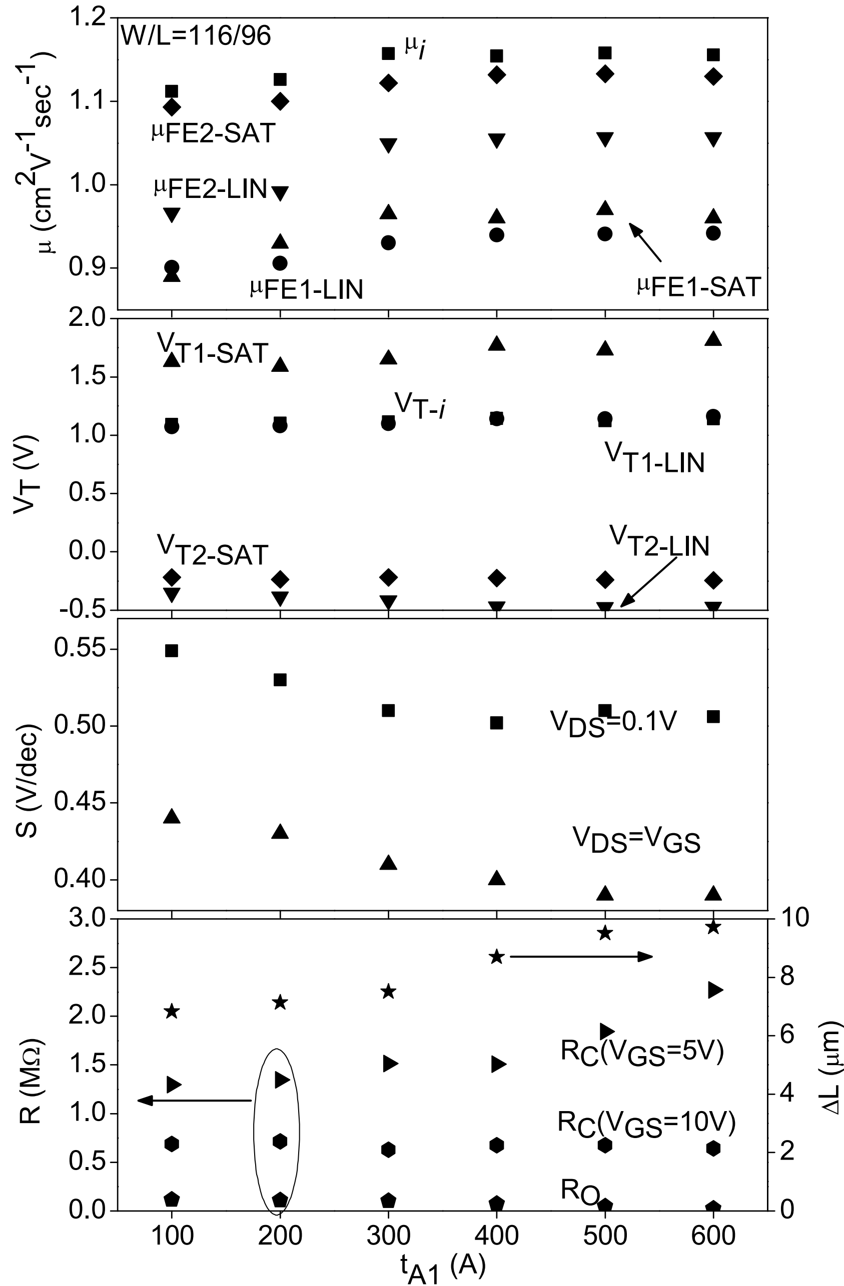

Figure 3-8. Intrinsic mobility and threshold voltage, and linear and saturation regions field-effect mobility, threshold voltage, subthreshold swing, contact resistances, and channel length deviation values for a-Si:H TFT's with different A1 thicknesses investigated in this work.

The increase in intrinsic and field-effect mobility values is observed repeatedly and falls within the standard deviation value of our measurement (2%). This means that as t_{A1} increases from 100 to 600Å, the crystalline order of the amorphous silicon film increases, and the width of the band-tail states along the electron conduction channel of the transistor decreases [3]. The effect of this trend has been studied in the single layer amorphous silicon thin-film transistors; there is a lowering in field-effect mobility with increasing film deposition rate caused by the increasing formation of the Si-$H_{2,3}$ bonds versus the ideal Si-Si tetrahedral bonds [17]. Non-ideal bondings, such as the Si-H_2 and Si-H_3 bonds, distort the microcrystalline structure of the amorphous silicon lattice, thus leading to a lower field-effect mobility. We expect our A1 film to have a higher ratio of Si-Si versus Si-$H_{2,3}$ bonds than the A2 film since it has a lower deposition rate. This explains the improvement in field-effect mobility that is associated with the increasing t_{A1}. Moreover, the increase saturates at about 300Å, which suggests that the electron conduction is confined within this thickness, because further increase in t_{A1} does not lead to a higher mobility.

The values and trend of threshold voltage change with respect to t_{A1} varies with different extraction methods. Using the linear method, the extrinsic threshold voltage increases by 0.08 V as t_{A1} increase from 100 to 600Å; same percentage of increase can be observed in the intrinsic voltage extraction. However, when using conductance method, there is a decrease in threshold voltage by 0.12 V. More importantly these slight changes are close to the standard deviation value (0.1 V) of three measurements. Therefore based on our observation we conclude that the threshold voltage remains the same as t_{A1} changes.

Subthreshold swing values, in both regions of operation, decrease by 10% with increasing t_{A1}; the decrease, however, saturates between 300 to 500Å. Since S is a function of both a-Si:H bulk states and a-SiN_X:H/a-Si:H interface states, and we assume that TFTs with all different t_{A1} have identical interface states density (N_{SS}), the lowering of S with increasing t_{A1} originates from the decrease in the neutrally charged deep-gap state density (N_{bs}) in the amorphous silicon bulk [18]. From the subthreshold equation derived by Rolland *et al.* [19],

$$S = \frac{kT_{MEAS}}{q\log(e)}\left[1+\frac{qx_i}{\varepsilon_i}\left(\sqrt{\varepsilon_s N_{bs}}+qN_{ss}\right)\right], \qquad (3\text{-}10)$$

and assuming a constant interface state density for all of our a-Si:H TFTs, we can calculate the decrease in effective bulk state density from the decrease in the subthreshold swing values with t_{A1}. Based on the measured S values in the linear region for TFTs with different t_{A1}, for N_{ss} of $1\text{x}10^{11}$ cm^{-2} eV^{-1}, the effective N_{bs} changes from 9.5 to 7.7 $\text{x}10^{18}$ cm^{-3} eV^{-1}, while using the saturation region S values, N_{bs} decreases from 5.7 to 4.3 $\text{x}10^{18}$ cm^{-3} eV^{-1}. For N_{ss} of $1\text{x}10^{12}$ cm^{-2} eV^{-1}, the N_{bs} changes from 9.3 to 7.5 x 10^{18} cm^{-3} eV^{-1} for the linear region and 5.6 to 4.2 $\text{x}10^{18}$ cm^{-3} eV^{-1} for the saturation region S values.

At a low gate voltage (V_{GS}=5 V), the contact resistance increases with t_{A1}. As V_{GS} increases to 10 V, the contact resistance is invariant to t_{A1} and maintains a mean value of 0.67 MΩ. However, the minimum contact resistance R_O decreases with t_{A1} from 0.11 to 0.02 MΩ. To analyze the above observations we will discuss the change in $R_C(V_{GS})$ based on the a-Si:H bulk and junction resistances of the TFT. The contact resistance is the sum of the a-Si:H bulk resistance and the a-Si:H/n+ a-Si:H/Mo junction resistance. It is well known that the amorphous silicon film deposited at a higher rate, therefore containing a lower hydrogen content, has a higher dark conductivity than an a-

Si:H film deposited at a lower rate [20]. This indicates that film A1 has higher bulk resistivity than A2 due to its lower deposition rate. All of the TFTs fabricated in this study have the same overall a-Si:H thickness of 1700Å; transistors made on plate with the thinnest t_{A1} (100Å) has the thickest t_{A2} (1600Å), and vice versa. As t_{A1} increases from 100 to 600Å, the thickness of the high resistivity film increases while the thickness of the low resistivity film decreases, resulting an increase in the overall contact resistance. The increase in $R_C(V_{GS}=5V)$ with increasing t_{A1} suggests that the bulk resistivity of the amorphous silicon film dominates at lower gate voltages ($V_{GS}<5V$). As the gate bias increases ($V_{GS}\geq 10V$), the contribution from the a-Si:H bulk resistivity diminishes and the junction resistivity begins to dominate, and $R_C(V_{GS})$ becomes invariant to the thickness of t_{A1} or t_{A2}. Lastly the ΔL of the our transistor increases with A1 a-Si:H film thickness. This increase is a response to the contact resistance increase: since the bulk resistivity of the film goes up with t_{A1} at gate biases below 10V, the cross-sectional area (W x ΔL) for the current flow has to increase to compensate for this change.

3.5. Conclusion

We have fabricated and characterized the intrinsic and extrinsic electrical properties of the a-Si:H TFT with the tailored channel. Based on our investigation, the film thickness of the high electronic quality a-Si:H should be about 300 Å for the TFTs to exhibit promising characteristics without requiring extensive deposition time. At t_{A1} of 300Å, our TFT has a linear regime field-effect mobility of 0.93 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage of 1 V, subthreshold swing of 0.51 V/dec, and $R_{S/D}(5V)$ of 1.5 MΩ. For t_{A1} thinner than 300 Å we observe an increase in S, while having thicker t_{A1} does not

improve the transistor's mobility, threshold voltage or subthreshold swing significantly. It is worth noting that this a-Si:H TFT, with t_{A1} of 300 Å, has very similar device performance values as the TFT with t_{A1} of 1700 Å.

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Chapter 4:

Back Channel Etch Chemistry

4.1. Introduction

Since the electrical performance of the hydrogenated amorphous silicon thin-film transistor technology impacts the performance of a variety of electronic applications, ranging from the flat panel displays [1-4] to sensors [5-8], it is crucial to develop processing steps and chemistry that optimize its device electrical characteristics. A transistor's electrical performance is intimately related to its fabrication processes, especially during dry etching steps where the device is exposed to high energy radiation and ions [9, 10]. For the a-Si:H TFT with inverted staggered back channel etch (BCE) type structure, an etching of the channel region amorphous silicon film after the source and drain definition is required to reduce its off-current (I_{OFF}) [11]. This BCE process is a critical step, because the plasma generated during the reactive ion etching (RIE) of the back channel of the TFT can degrade its field-effect mobility (μ_{EFF}) by up to 15 % compared to the same TFT etched with wet etchant [12]. Even though the a-Si:H TFT can be fabricated completely using wet etch only [13], dry etch is still the preferred method for critical etching steps due to its superior selectivity versus metal and photoresist (PR), high anisotropy, and reduced residue formation [14]. Thus it would be

desirable to search for a dry etchant that encompasses the benefits mentioned above regarding dry etching without degrading the electrical properties of the transistor.

Numerous dry and wet etchants have been reported in the etching of silicon for various applications [15, 16]. Fluorocarbon compounds, such as C_2F_6 and CF_4, have been used as RIE gas species to etch the n+ (phosphorous-doped) amorphous silicon [17]. Alternatively, chlorofluorocarbon compounds like CCl_2F_2 and CF_3Cl have also been utilized to dry etch the n+ a-Si:H due of its high selectivity versus intrinsic a-Si:H, and that they do not to leave organic etching byproduct common in fluorocarbon dry etching [18, 19]. Hydrogen bromide (HBr) has often been used to dry etch silicon-based devices because of its high selectivity versus oxide, and high aspect ratio of the profile [20]. For plasma-free etching of the silicon film, potassium hydroxide (KOH) and tetramethyl ammonium hydroxide (TMAH) have been employed [21, 22]. With such a diverse range of BCE etchants, a comprehensive study of their impacts on the electrical performance of the a-Si:H TFT is needed in order to select, if any, an attractive dry etchant chemistry for the back channel etch fabrication process.

Choe and Kim evaluated the effect of dry etchants on the off-current of the amorphous silicon thin-film transistor transistors, and related the increase in off-current to the increase in contaminant ($MoCl_X$ and MoF_X) concentrations in the TFT's back channel [23]. GadelRab *et. al* compared the difference in TFT electrical performance between tri-layer transistors etched with SF_4:O_2 plasma, and KOH [9], and concluded that the wet etched device shows higher electrical performance. Additionally, Ando *et. al* presented an in-depth analysis regarding the effect of back channel etching depth and etchants (i.e. fluorine-based gas and hydrazine monohydrate) on the TFT electrical

characteristics, and concluded that dry etching degrades μ_{EFF} of a-Si:H TFT [12]. With our best effort, however, we cannot find a study that assesses the influence of a wide array of back channel etchants, with distinct etching chemistries and mechanisms, on the advanced multi-layer a-Si:H TFT's electrical performance [24]. In this study we compare the impact of different BCE etchants on the characteristics of the inverted staggered advanced a-Si:H TFT, and identify a promising dry etchant that is capable of producing transistors with comparable electrical performance as the device etched by a wet etchant.

4.2. a-Si:H TFT Fabrication

The fabrication process up to the source/drain electrode etching has been described in detail in the previous chapter, and will not be repeated here (figure 4-1a). After the etching of the molybdenum electrodes, the positive tone photoresist layer (Shipley 1813) remains on the molybdenum source and drain as the mask for the back channel dry etch process (figure 4-1b). This PR layer is necessary to shield the molybdenum film from direct ion bombardment during the RIE in order to prevent top layer molybdenum consumption and the contamination of the TFT back channel due to metallic residue (e.g. MoF_X and/or $MoCl_X$) formation [23]. Four different etching chemistries, three dry and one wet, are used for the back channel etch (BCE) process of the advanced a-Si:H TFT. Two of the dry-etch experiments, $HBr+Cl_2$ (1:1) and C_2F_6, are done in the LAM 9400 Transformer-Coupled Plasma Reactive Ion Etcher (TCP-RIE), and the third, $CCl_2F_2+O_2$ (5:1), in a capacitive-coupled reactive ion etcher (Table 4-1). The wet etching of the amorphous silicon active layer is done in a 50 ˚C solution

comprised of 400 g of potassium hydroxide (KOH) pellets dissolved in 4000 mL of deionized water; only molybdenum is used as the mask for the KOH etching because the alkali-based solution attacks positive tone PR (figure 4-1c). After the BCE and the removal of the photoresist, the TFTs are annealed in nitrogen for 1 hr at 200 ˚C to remove plasma-induced radiation damages in the a-SiN:H and a-Si:H films [25]. Figure 4-1 shows the complete fabrication schematic of the advanced a-Si:H TFT used in this study. The fabricated devices were not passivated with any passivation layer. It should be mentioned here that we perform a 10% over-etch, by intentionally extending the etch time, during the gate and S/D metals etching steps, and the island etching step, to avoid unwanted electrical shorts between the device features. The TFT's electrical characteristics are measured and extracted using methods described in the pervious publication [24]. Table 4-1 shows the detailed etching recipes and etch rates of the four BCE etchants used for the etching of the a-Si:H and n+ a-Si:H films.

To investigate the effect of BCE etchants on the transistor performance, we first need to identify the best BCE etching depth of the a-Si:H TFT for each etchant. Wafers with identical films and patterns, up to source/drain electrode wet etch undergo BCE using a specific etchant for a set duration. For TFTs etched with $HBr+Cl_2$, the final a-Si:H thicknesses ($d_{a\text{-}Si:H}$) in the TFT's channel region to range from 1190 to 800 Å and no over-etch time is included. Similar experiments are conducted using other etchants for the back channel etch process. The electrical characteristics of the best transistor for each etchant will be used as the basis of comparison regarding the impact of BCE etchant chemistry and mechanism.

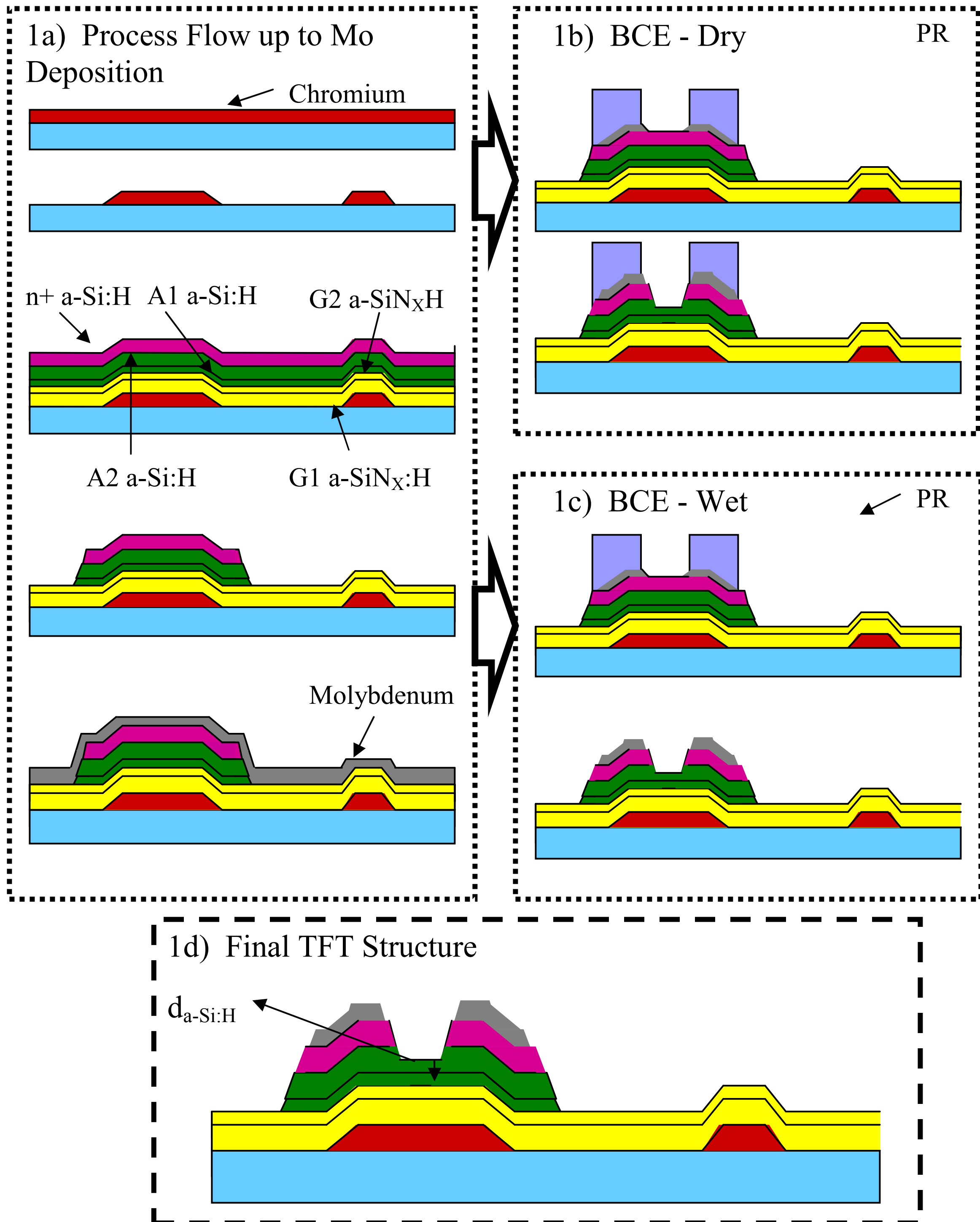

Figure 4-1: Complete fabrication schematic of a-Si:H transistor. Figure 4-1a) represents the fabrication process up to the source/drain molybdenum deposition. Figure 4-1b) shows the dry BCE process, with photoresist left on the source/drain as the etching mask. Figure 4-1c) shows the wet BCE process, which removes the PR during the back channel etch of the amorphous silicon film. Figure 4-1d) is the schematic of the final a-Si:H structure.

Table 4-1: Etching chemistry and conditions for back-channel etch process used in this chapter, and their respective etch rates for PECVD a-Si:H and n+ a-Si:H films.

Etchant	TCP-RF (W)	Bias RF (W)	Pressure (mTorr)	a-Si:H/n+ a-Si:H Etch Rate (Å/min)
$HBr:Cl_2$ (1:1)	100	30	12	400/680
C_2F_6	200	80	12	310/350
$CCl_2F_2:O_2$ (5:1)	-	100	100	150/300
KOH	-	-	-	1200/1500
$SF_6:Cl_2:O_2:He$ (6:20:20:5)	100	30	12	1280/1640

4.3. Result and Discussion

4.3.1. Impact of the Gate and Source/Drain Metal Wet Etch

We show in figure 4-2 the scanning electron microscope images of the source/drain region of the inverted staggered a-Si:H TFT fabricated for this work. Wet etchant was used for the S/D electrodes fabrication, and we notice that the molybdenum electrode is over-etched by about 1000 Å, which is much larger than the initially targeted 10% over-etch, or 200 Å for the metal film. It is possible that the lateral etch is faster than the vertical etch due to the stress of the film. Among the three etched layers (gate, S/D, and n+ a-Si:H/a-Si:H), only the molybdenum S/D shows tapered profile, with a tapered angle of about 32˚ as measured from the surface of the film. Such low tapered angle for the film is achieved by using wet etchant that is highly isotropic (i.e. significant lateral etching underneath the photoresist mask occurs). This high lateral etch rate can also explain the excessive molybdenum S/D over-etch mentioned above.

A low tapered angle is a very desirable property since it can improve the overall active-matrix liquid crystal displays (AM-LCD) production yield. During the fabrication of AM-LCD panels, there are multiple levels of film deposition and etching steps that are

required to produce fully functional products [26]. Each thin-film's contour and conformity is influenced by the surface morphology of the underlying layers [27]. In the case of the a-Si:H TFT presented in this work, the gate metal and n+ a-Si:H etchings produce sharp corners (i.e. large tapered angle) near their respective edges; the sharp corners can reduce the step coverage of the films deposited afterward (e.g. molybdenum). Such contact profile near the electrode corner can be highly strained, and lead to the delamination and/or buckling of the subsequent film. If a strain-induced fissure is created in a metallic film, it can potentially create unwanted open circuits, leading to a failure in the electronic operation. For the traditional AM-LCD fabrication process [26], the films deposited after the molybdenum (data) lines are the passivation amorphous silicon nitride, and the ITO pixel electrode. Tapered data lines reduce the chance of unwanted open circuit connection between the data lines and the pixel electrodes, and increase the overall production yield. To further improve our a-Si:H TFT fabrication process, the etchants for the gate and n+ a-Si:H/a-Si:H should both be highly isotropic, so the data lines and the pixel electrodes can have better step coverage.

4.3.2. Impact of the a-Si:H Film Etching Depth

Figures 4-3 (top) and 4-4 (top) show the linear and saturation region electrical characteristics for the a-Si:H TFTs etched with the HBr recipe during the BCE process. Transistors with different $d_{a\text{-}Si:H}$ values are seen here. We extracted their electrical parameters, and summarized the average of three measurements in figure 4-5 by plotting them against $d_{a\text{-}Si:H}$. The a-Si:H TFT's off-current and subthreshold swing (S) both decrease with decreasing $d_{a\text{-}Si:H}$. The transistors' field-effect mobility trend shows a 9%

decrease as $d_{a\text{-}Si:H}$ changes from 1190 to 1070 Å, and remains constant as the $d_{a\text{-}Si:H}$ decreases down to 800 Å; the threshold voltage values appear to increase as $d_{a\text{-}Si:H}$ decreases. However, since μ_{EFF} and V_T error bars are about ± 0.07 $cm^2V^{-1}s^{-1}$ and ± 0.23 V, respectively, the changes are accounted as a statistical fluctuation, which means both parameters remain unchanged with $d_{a\text{-}Si:H}$. Since all of the a-Si:H TFTs have identical

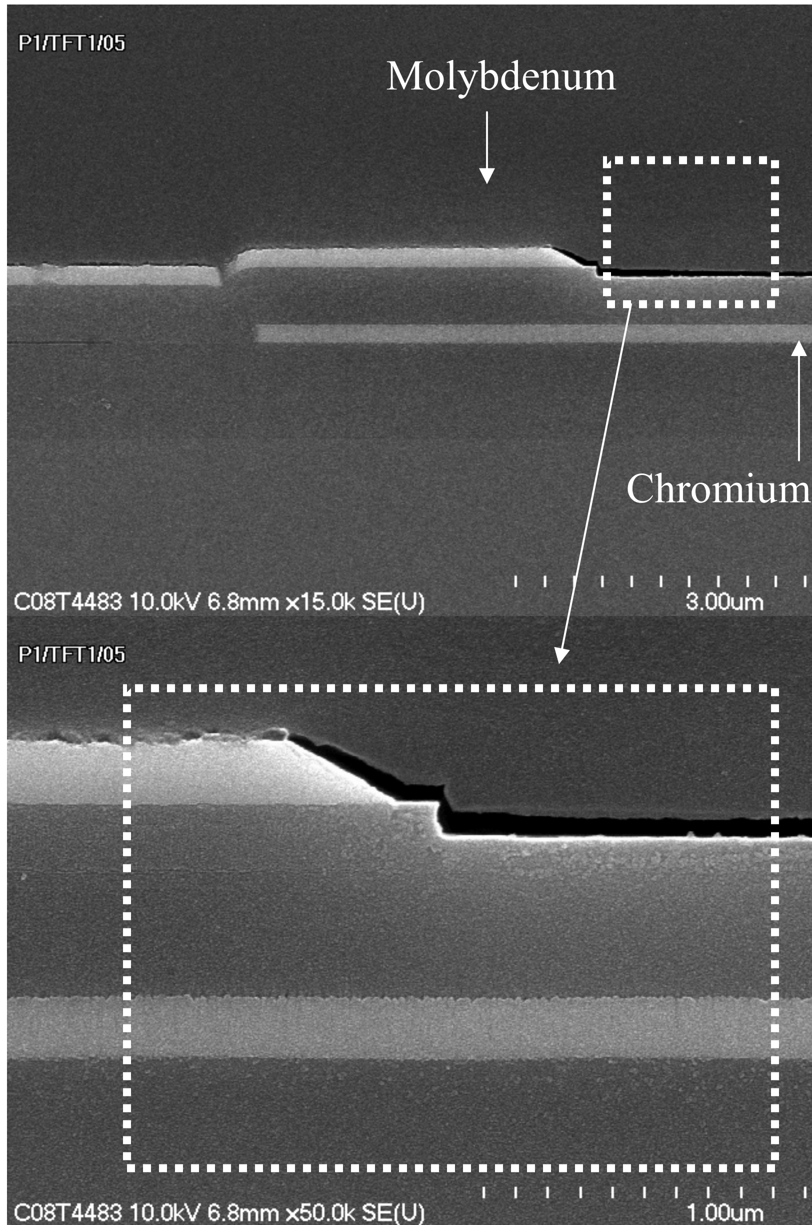

Figure 4-2: SEM images of the etching profile near the source terminal of the a-Si:H TFT. The molybdenum is etched with Al Etchant Type A, and the n+ a-Si:H with $HBr+Cl_2$.

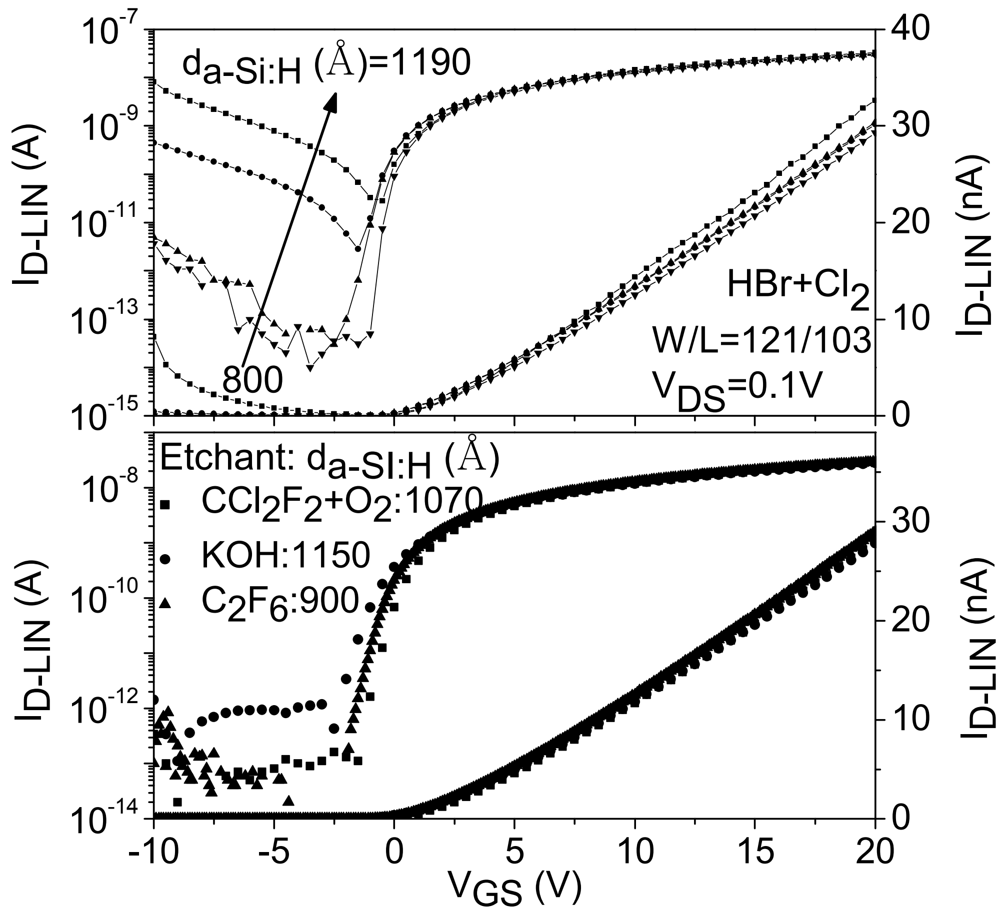

Figure 4-3: Linear region (V_{DS}=0.1V) transfer characteristics of a-Si:H TFT's etched with $HBr+Cl_2$ (top) for different $d_{a\text{-}Si:H}$, and $CCl_2F_2+O_2$, C_2F_6, and KOH (bottom).

initial a-Si:H film thickness values (prior to the BCE), and the device structure is an inverted staggered TFT, we do not expect any difference in the electronic qualities of the a-Si:H film, front interface qualities, nor the transistors' source/drain contact resistances before the back channel etch process. Both TFTs' μ_{EFF} and V_T values remain constant, within statistical range, as $d_{a\text{-}Si:H}$ decreases from 1190 to 800 Å. This observation, together with the fact that all transistors have similar electrical and geometric parameters

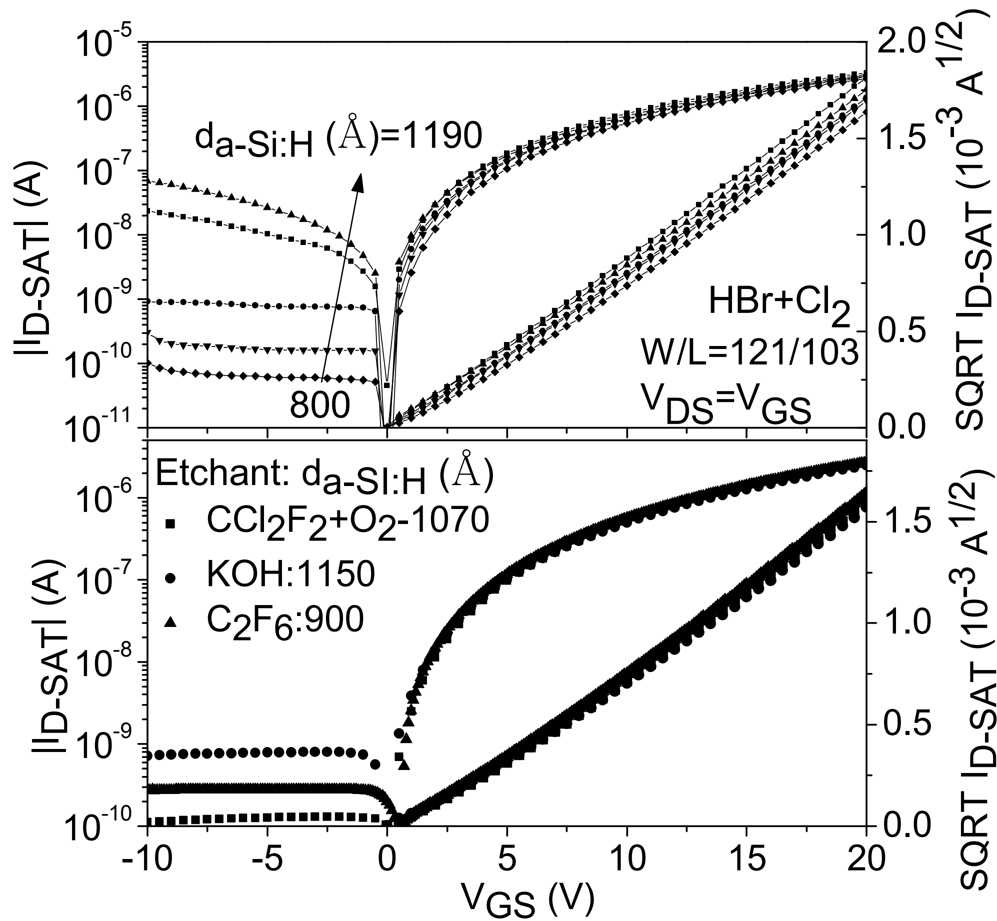

Figure 4-4: Saturation region (V_{DS}=V_{GS}) transfer characteristics of a-Si:H TFT's etched with HBr+Cl_2 (top) for different $d_{a\text{-}Si:H}$, and CCl_2F_2+O_2, C_2F_6, and KOH (bottom).

other than $d_{a\text{-}Si:H}$, leads us to conclude that the channel region a-Si:H film thickness after BCE does not impact the TFT's field-effect mobility and threshold voltage.

The drastic reduction (~10^4) in a-Si:H TFT I_{OFF} with the thinning $d_{a\text{-}Si:H}$ can be explained by the removal of the phosphorous doped a-Si:H film in the back channel (a-Si:H/atmosphere interface), which causes a leakage path between the source and the drain of the a-Si:H TFT [12]. During the sequential PECVD deposition of the a-SiN_X:H, a-Si:H, and n+ a-Si:H, phosphorous atoms in the n+ a-Si:H layer diffuse in the neighboring

a-Si:H film for an additional few 100's Å. The activation of these dopants in the a-Si:H leads to the increasing conductivity of the film due to higher electron concentration. Since the Fermi-level in the back interface of a-Si:H is much closer to the conduction band then in the a-Si:H bulk, negative voltage applied to the gate of the transistor is insufficient to "turn-off" the electrical current conduction path in the back channel. Thus electrons can conduct between the source and drain of the TFT along the phosphorous-rich a-Si:H film near the back channel when $d_{a\text{-}Si:H}$ is thick. As the back channel of the a-Si:H film is gradually etched away, the highly conductive section of the film disappears and the off-current is reduced.

The most puzzling trend is observed for the subthreshold swing: S decreases with decreasing $d_{a\text{-}Si:H}$. It is well known that the generation of deep-gap and interface states causes S to increase [24, 28]. As $d_{a\text{-}Si:H}$ decreases, it is unlikely that the densities of states (DOS) of the bulk amorphous silicon film, and the front (a-SiN_X:H/a-Si:H) and back interfaces improve. Moreover, it has been shown that there is a linear correlation between S and V_T [29], which we do not observe. We believe that the observed higher S values of TFT's with thicker $d_{a\text{-}Si:H}$ (i.e. 1190 and 1070Å) is related to the high I_{OFF} originating from the back channel conduction. In these devices a significant portion of the electrical conduction occurs in the back channel of the a-Si:H TFT. These electrons flow in the a-Si:H film (A2) with a higher bulk deep-gap state density than the a-Si:H film (A1) in the front channel [25]. Furthermore, I_{OFF} also flows near the back interface, which has higher surface deep-gap state density then the front interface due to less ideal deposition condition [25]. Higher deep-gap state densities at both locations lead to the higher S values, because the Fermi level near the back interface gets pinned in those

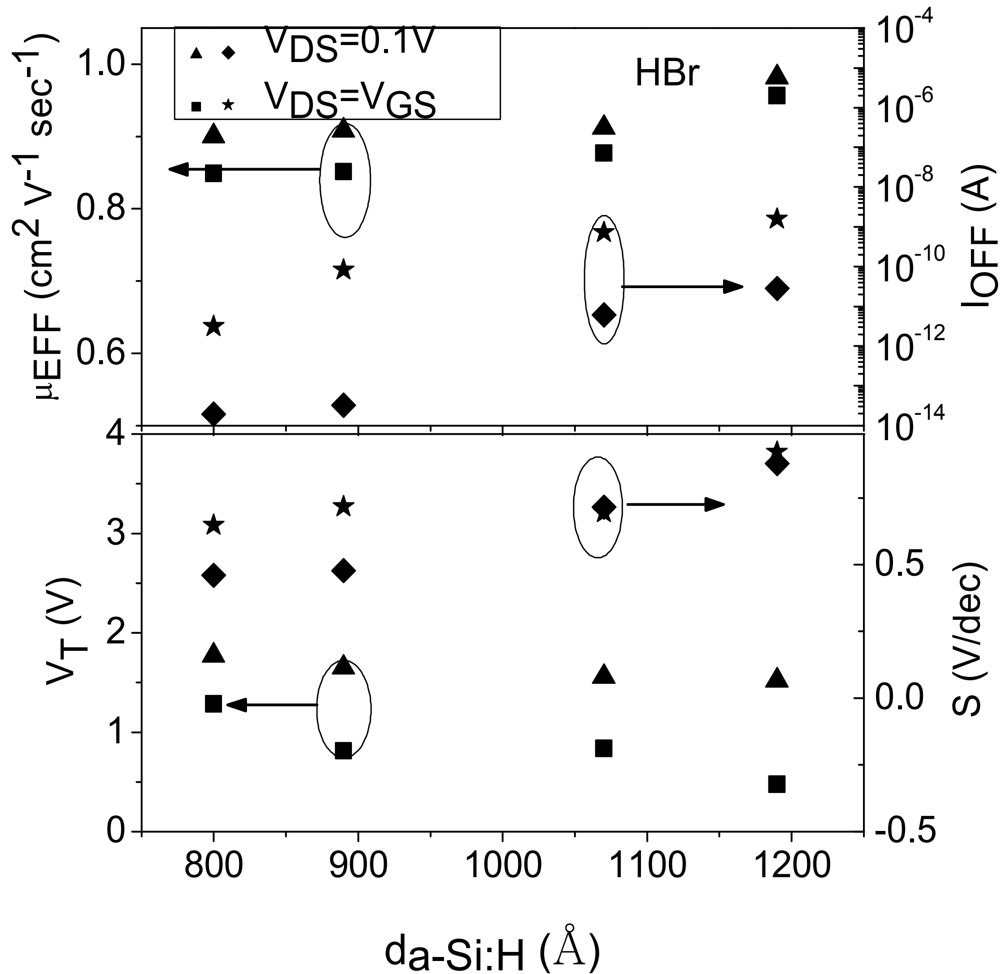

Figure 4-5: Amorphous silicon TFTs' field effect mobility, threshold voltage, subthreshold swing, and off-current values change with $d_{a\text{-}Si:H}$. All transistors are etched using $HBr+Cl_2$.

transistors [10]. This explains why transistors with thicker $d_{a\text{-}Si:H}$ shows higher S. These higher subthreshold swings we extracted are the S values that account for both the front and back channel conduction behaviors. Once $d_{a\text{-}Si:H}$ becomes thinner (i.e. 890 and 800 Å), I_{OFF} decreases due to the reduced phosphorous concentration in the back channel, and consequently, the subthreshold swing values decreases. For such device, a large number of electrons begin to flow in A1 a-Si:H with lower DOS. This trend does not imply that

the front channel a-Si:H bulk and interface DOS improves with the progressive etching of $d_{a\text{-}Si:H}$, but rather the contribution of the back channel decreases with the reduction of $d_{a\text{-}Si:H}$. but rather the contribution from the back channel DOS decreases as the conductive back channel in the amorphous silicon film gradually disappears.

In summary, about 800 Å of amorphous silicon film was etched away during the BCE process to achieve an acceptably low I_{OFF} (~10^{-14} A in the linear region of operation) for our a-Si:H TFT. While other literatures have reported that the over-etching during the BCE step led to the degradation in the transistor's electrical characteristics [10], we do not observe any degradation in μ_{EFF}, V_T, and S as $d_{a\text{-}Si:H}$ decreases from 1190 to 800 Å. For the fabrication of inverted staggered BCE type multi-layer a-Si:H TFT with the tailored channel, we recommend the a-Si:H film deposition thickness to be at least 1600 Å to realize transistors with reasonably low I_{OFF} without any deterioration in their electrical performance.

4.3.3. Impact of the Back Channel Etchant Chemistry

Our next experiment evaluates the impact of the BCE etchants on the electrical performance of the multi-layer a-Si:H TFTs with the tailored channel. Three of the four etchants expose transistors to ions and radiations in the plasma, with KOH being the only one that relies purely on the chemical reaction to etch the n+ and a-Si:H films [30]. Although the three dry etch recipes are all carried out in plasma chambers, their silicon etching mechanisms are quite different. CCl_2F_2 molecule contains both fluorine and chlorine atoms, yet the primary species involved in the etching of amorphous silicon is the chlorine [31]. The reason for this is that the C-F bond is stronger then the C-Cl bond,

and in CCl_2F_2 there is a higher probability to remove the chlorine atoms from the molecule [31]. Gerlach-Meyer *et. al* have demonstrated that the chlorine atoms require ion bombardment to chemically react with silicon atoms, and that the volatile etching product formed is $SiCl_4$ [32]. Other etching products can also be formed following the chemical reaction between chlorine and silicon: SiCl, $SiCl_2$, and $SiCl_4$ [33]. For the $HBr+Cl_2$ chemistry, both bromine and chlorine ions participate in the etching of silicon. Similar to the chlorine etching of silicon, the bromine etching of the amorphous silicon requires ion bombardment to overcome the activation energy necessary to trigger the chemical reaction between the bromine and the silicon atoms. As a result, using $HBr+Cl_2$ chemistry as the back channel etchant should lead to highly anistropic n+ profile, which can be seen in the SEM images in figure 4-2. The volatile product formed is $SiBr_4$ [34]. Other non-volatile etching by-product ($SiBr_X$) can also be formed and deposited on the side-wall [35]. The C_2F_6 etching of the amorphous silicon film involves the chemical interaction between the fluorine and the silicon atoms. Since the activation energy required is quite low (0.1eV), fluorine-based dry etching of silicon can be triggered with little or no ion bombardment [33].

Figures 4-3 (bottom) and 4-4 (bottom) show the transfer characteristics of our a-Si:H TFTs fabricated with 4 different BCE etchant chemistries. The summary of their electrical parameters in the linear region of operation is shown in figure 4-6; the saturation region parameters are similar in values and trends and will not be shown here. These data represent the electrical characteristics of the a-Si:H TFTs with optimized $d_{a\text{-}Si:H}$ (Å): $HBr+Cl_2$ (800), $CCl_2F_2+O_2$ (1070), C_2F_6 (900), and KOH (1150). The TFTs' field-effect mobility, threshold voltage, and subthreshold swing values show no change

when different etchants were used. This consistency among the extracted electrical parameters suggests that the density of states in the amorphous silicon film and the front channel interface do not change with the back channel etchant. I_{OFF} values for the dry-etched a-Si:H TFTs have similar values, but the KOH etched TFT has approximately 1 order of magnitude higher off-current value. This is due to a layer of conductive residue left in the back channel of the TFT during the KOH etching of the amorphous silicon film [19]. According to our experiment, the presence of plasma does not significantly or permanently degrade the electrical performance of the a-Si:H TFT since their μ_{EFF}, V_T, and S have very similar values. $HBr+Cl_2$ chemistry can be used for the BCE step

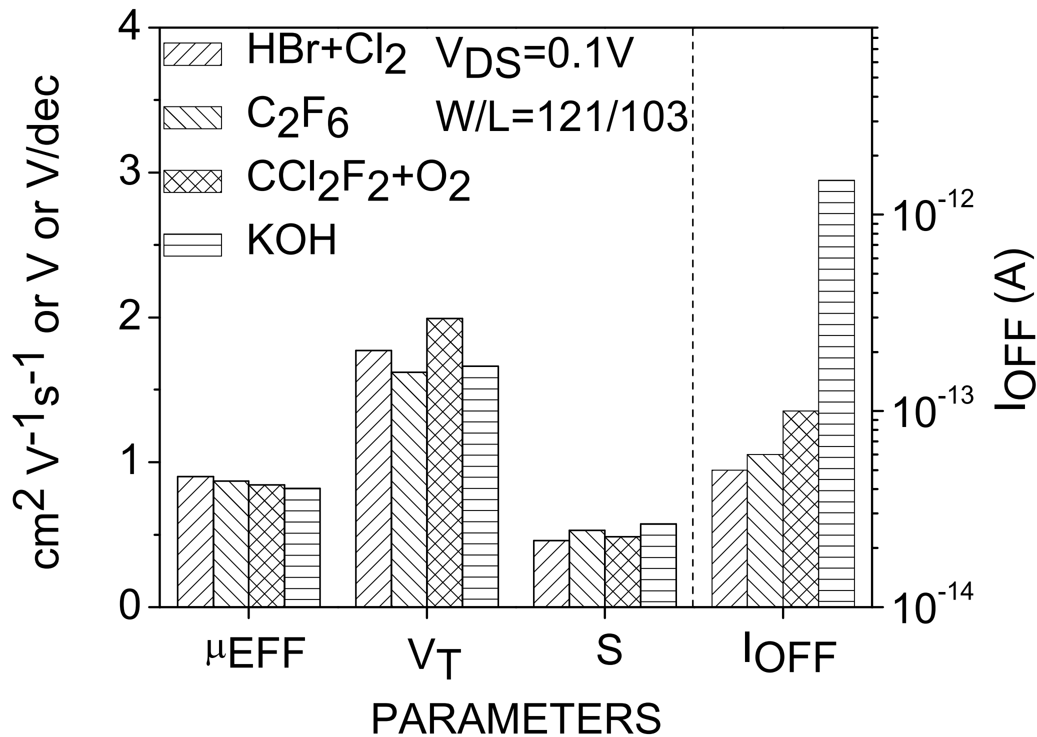

Figure 4-6: Optimum a-Si:H TFTs' field effect mobility, threshold voltage, subthreshold swing, and off-current values comparison.

because we observe no electrical degradation caused by plasma and radiation, and it offers excellent selectivity over a-SiN_X:H (>200:1).

4.4. Conclusion

Based on our experimental results, the deposition thickness of a-Si:H film for advanced a-Si:H TFT should be at least 1600 Å. This allows the etching of the back channel a-Si:H film (~800Å) for the purpose of reducing I_{OFF} without degrading, caused by an overetching of the a-Si:H, the electrical properties of the transistor. We have shown that by utilizing RIE for the BCE process, we can obtain transistors with similar electrical characteristics as those etched with KOH. There seems to be no significant correlation between the dry etch chemistry and the transistors' device performance for the investigated etching chemistries in this work. We recommend using HBr+Cl_2 as the etching chemistry for the BCE process because it has reasonably high n+ a-Si:H etch rate (680 Å/min) and acceptable a-Si:H/n+ a-Si:H selectivity (1:1.7), and shows no negative impact on the electrical properties of the a-Si:H TFT with the tailored channel.

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Chapter 5:

Recess Etch

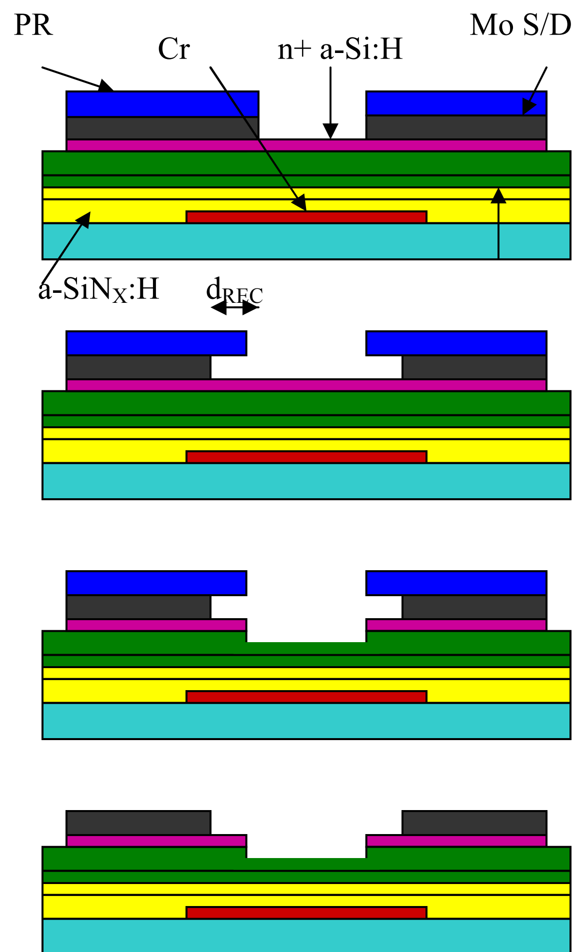
5.1. Introduction

Active-matrix liquid crystal display (AM-LCD) and active-matrix organic light emitting display (AM-OLED) are two of the most prevalent applications that require the extensive use of hydrogenated amorphous silicon thin-film transistors (a-Si:H TFT) as the driving electronic for individual display pixels [1-3]. One important criterion for the a-Si:H TFT is to have a low off-current to minimize the discharging of storage capacitors in the pixel electrode circuit during its driving stage, which would result in the degradation of the image quality over the frame time [1-6]. It is well known that the amorphous silicon film back surface conduction contributes to the increase in off-current [5, 6]. Among the four common transistor structures, the inverted back channel etch type TFT is especially susceptible to high rear surface conduction, because the amorphous silicon active layer is exposed during the plasma etching of the back channel [7-9]. Yet this structure is still being used due to its fabrication simplicity, high yield, and acceptable electrical characteristics [3, 10]. Various methods, ranging from passivation deposition to plasma treatment, have been proposed to reduce the effect of back surface conduction [3, 11, 12]. Since one of the factors that contributes to the generation of surface state arises from the metallic contamination during the reactive ion etch (RIE) of

the back channel [7], we propose a novel intentional over-etching technique to fabricate a novel a-Si:H TFT structure with recess source/drain electrodes that is designed to decrease the off-current of the a-Si:H TFT by reducing the metallic contamination of the back channel RIE step.

5.2. Fabrication of the TFT with Recess Source/Drain Contacts

We fabricated back channel etched type inverted staggered a-Si:H transistors with the tailored channel, based on the processing steps described in chapter 2 of this thesis, up to the molybdenum etching step of the source and drain (S/D) electrodes. After the metallization of the S/D contact, we perform an intentional over-etch process to recede the S/D contact electrodes,. This over-etch process undercuts the photoresist film by laterally etching the molybdenum film. We fabricated 3 sets of transistors with different S/D recess depths (d_{REC}): 0 (Conv. TFT), 2.5 (R-TFT1), and 10 (R-TFT2) kÅ. To recede the



S/D contact electrodes, we perform an intentional over-etch process. To achieve d_{REC} of 0, 2.5, and 10 kÅ, the over-etch times were 0, 40, and 160 s, respectively. This over-etch process undercuts the photoresist (PR) film by laterally etching the molybdenum film. Lastly, we dry-etched ($HBr:Cl_2$ in 1:1 ratio) the n+ a-Si:H film, and 700 Å of A2 in the channel region of the transistor using the LAM 9400 TCP-RIE with the PR film still on top of the molybdenum S/D electrodes. All patterning steps were performed using contact photolithography via a MA-6 mask aligner. The electrical characteristics of the conventional transistor, with d_{REC}=0 kÅ, is used as the basis of comparison against the performance of the recess contact transistors R-TFT1 and R-TFT2 in order to quantify the effect of the S/D over-etch.

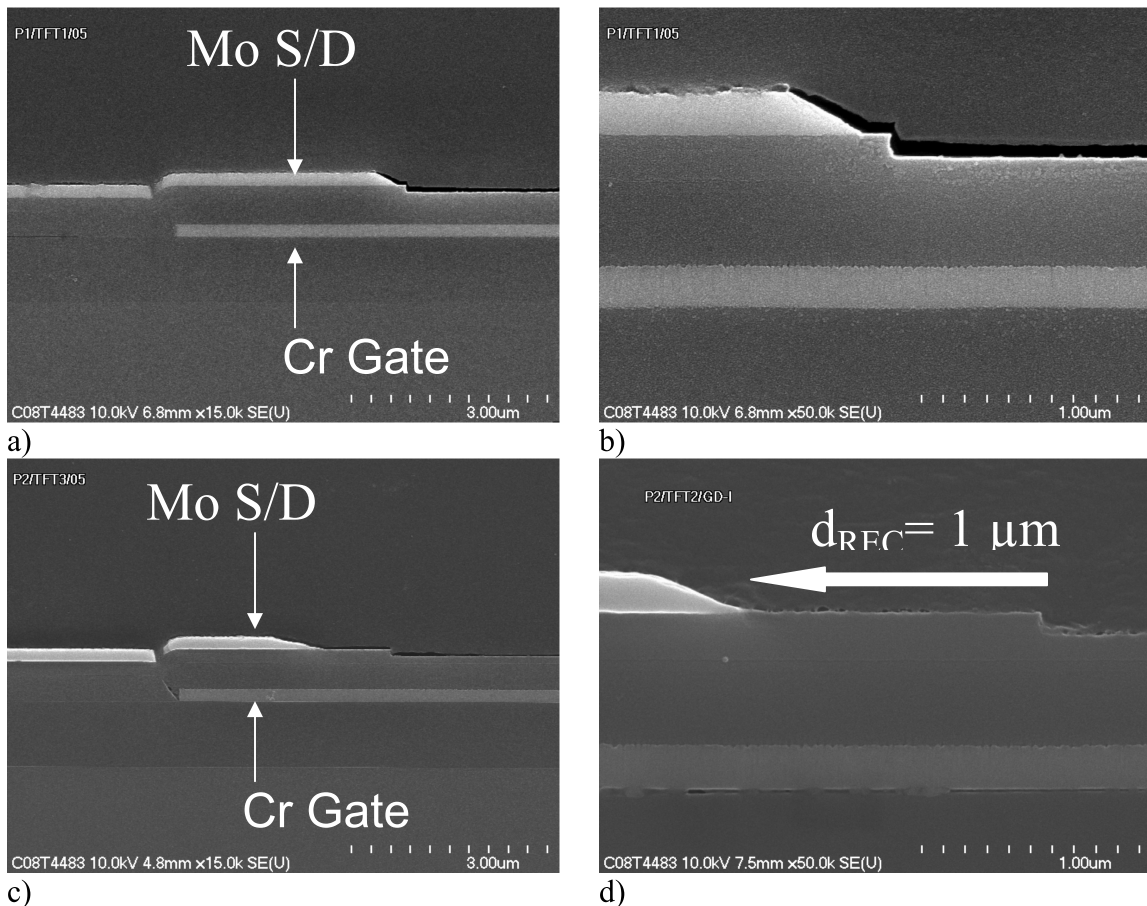


Figure 5-2: Scanning electron microscope image of the a-Si:H TFT with normal S/D profile (a and b), and recess S/D profile (c and d).

In figure 5-2, we present the cross-section scanning electron microscope (SEM) images of the a-Si:H TFTs with conventional S/D contact profile (a and b), and recess S/D contacts profile (c and d). In figure 5-2 a), we see the Mo contact and Cr gate of the TFT, as well as their overlap (3 μm). Figure 5-2 b) shows the S/D contact structure of the conventional TFT. Figures 5-2 c) and d) show the transistor after receding 1 μm of the Mo contact, and we can see that the overlap between the gate and the S/D have been reduced down to 2 μm.

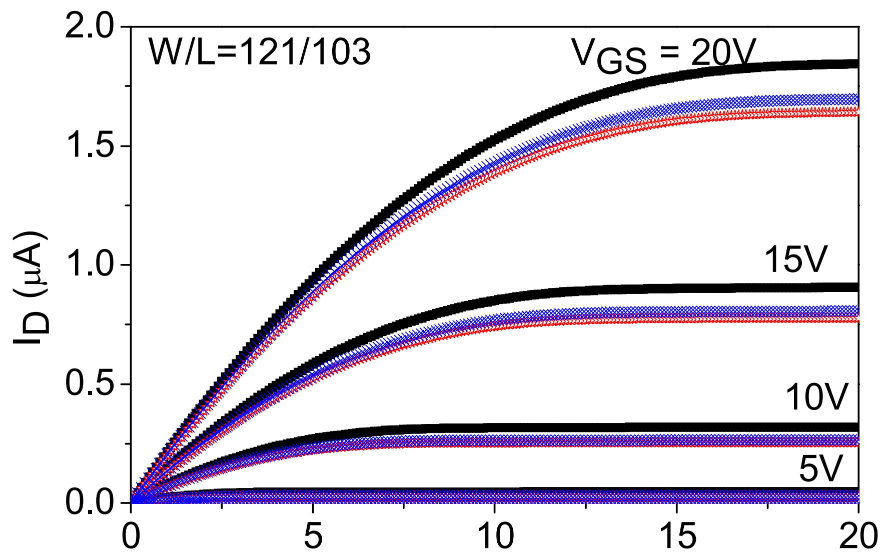


Figure 5-3: The output characteristics of the transistors are shown in this figure.

5.3. Result and Discussion

5.3.1. On- and Subthreshold Regions Electrical Characteristics

From the TFTs' output characteristics shown in Figure 5-3, we see that the transistors with different S/D contact profiles show similar on- region current levels for V_{GS} = 5 to 20 V. There is no visible current crowding at low V_{DS} values, which indicates that the S/D contact resistances ($R_{S/D}$) do not severely degrade the electrical performance of all three a-Si:H TFTs [15]. Next we examine in more detail the impact of the recess S/D profile on the electrical performance of the a-Si:H TFT. Based on the transfer characteristics of the TFTs (figure 5-4), we can extract their electrical performance (figure 5-5) and contact resistance values (figure 5-6), and [13]. Figures 5-4 (bottom) and 5-6 (top) demonstrate examples of the parameter extractions. Given that the three TFTs discussed in this work have identical gate insulators and active materials, we expect their field-effect mobility, threshold voltage, and subthreshold swing values to be nearly identical. This assumption has been experimentally verified, as seen in figure 5-5. The only question remains is the change, if any, in the transistors' contact resistance and I_{OFF}. It is well-known that the gate and source/drain overlap of a TFT influences its contact resistance [16]. Since the overlapping area between the molybdenum S/D and the chromium gate decreases linearly with increasing d_{REC}, it would be reasonable to assume that R-TFT1 and R-TFT2 will have higher contact resistance values than Conv. TFT. However, we see from figure 5-6 that all three transistors have similar $R_{S/D}$ values, for V_{GS} ranging from 2 to 20 V. This indicates that the recess contact TFTs shown in this work do not suffer any electrical performance degradation caused by the devices' contact resistance, and the contact resistance is mainly controlled by the n+ a-Si:H/a-Si:H

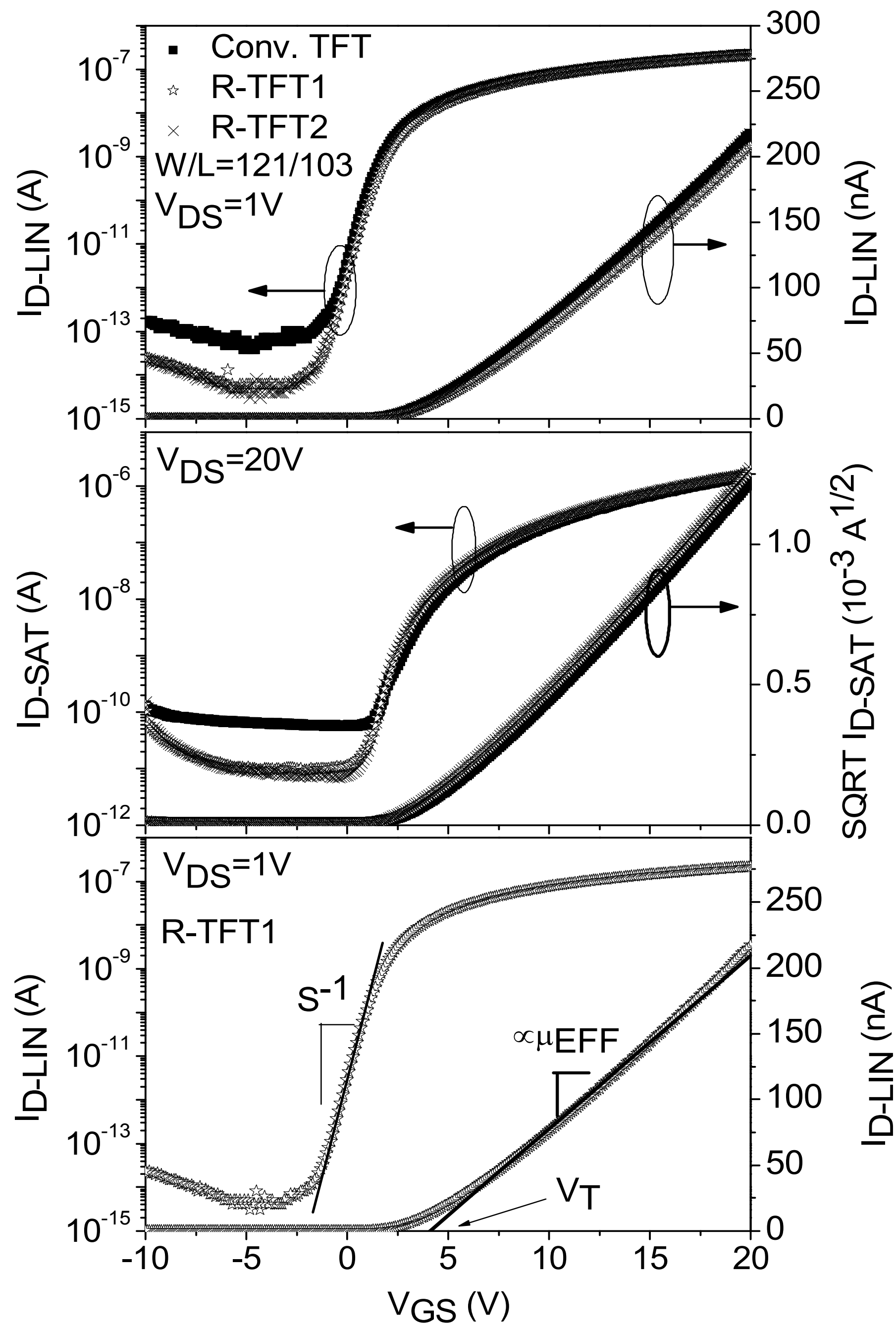


Figure 5-4: Linear (top) and saturation (middle) regions transfer characteristics of the three types of a-Si:H TFT structures presented in this work. The bottom plot shows an example of the parameter extraction.

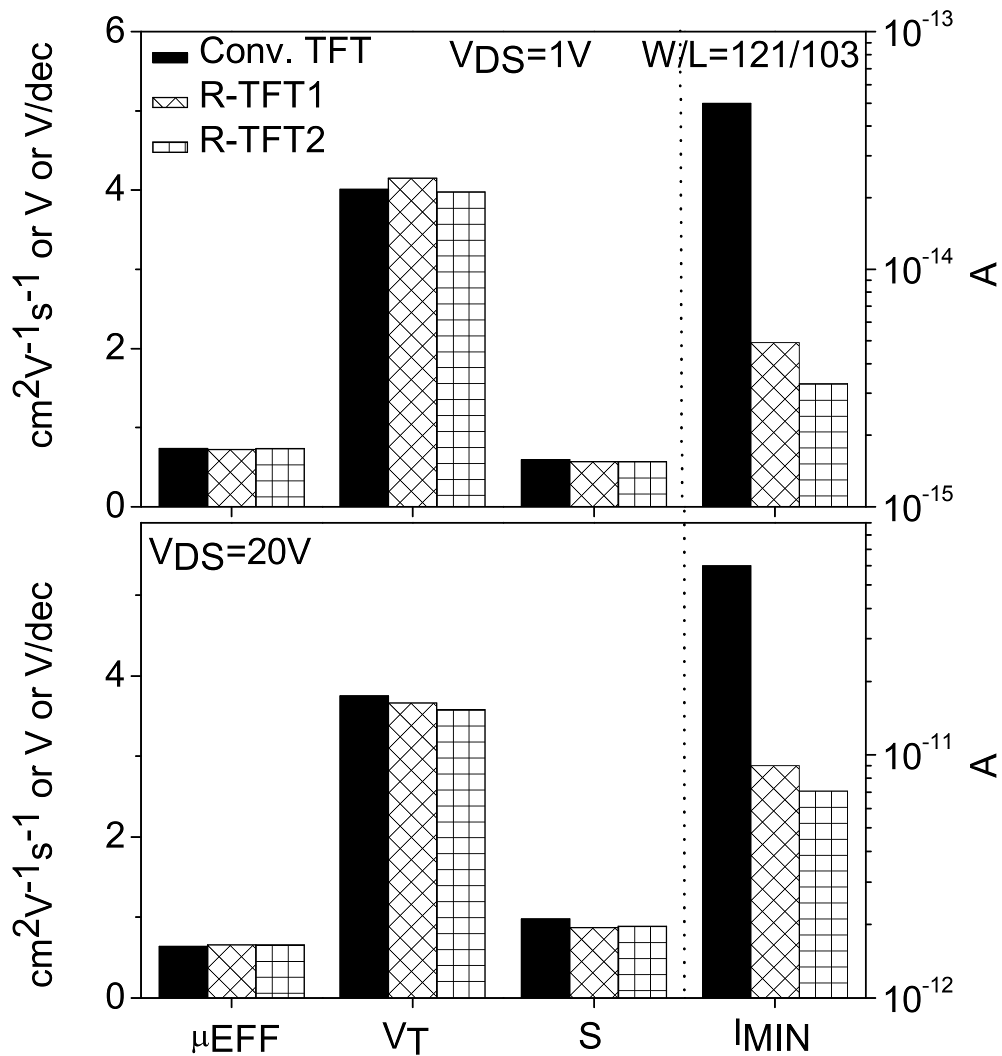


Figure 5-5: Summaries of the extrinsic electrical performance of the a-Si:H TFT's fabricated using the conventional processing steps (Conv. TFT), and with the inclusion of the recess etches (R-TFT1 and R-TFT2).

interface and the thickness of the a-Si:H layer. The minimum contact resistance is 130 MΩ and ΔL is 3μm for the conventional TFT and the recess S/D TFT. These values indicate that there is no significant deterioration to the contact quality for the novel TFT.

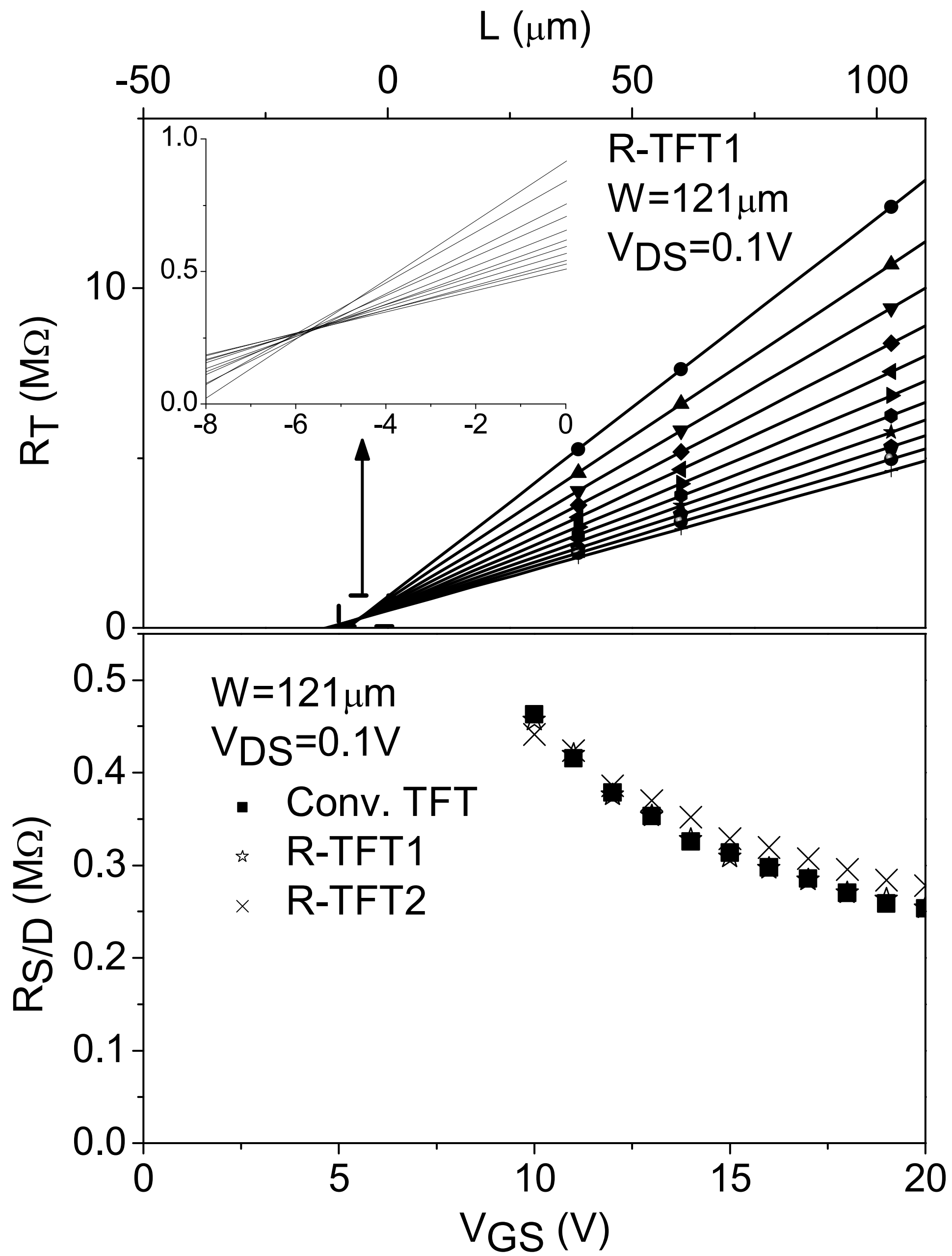


Figure 5-6: The extraction of $R_{S/D}$ for R-TFT1 is shown in the top figure. The bottom figure shows the source/drain contact resistance values for all three transistors structures at different gate biases.

5.3.2. Off Region Electrical Characteristics

In the transistors' off region of operation, the drain currents for TFT with d_{REC} of 2.5 and 10 kÅ decrease by ~1 order of magnitude as compared to the Conv. TFT (d_{REC}=0 Å), as seen in figure 5-5. This reduction is believed to be related to the decrease in the molybdenum complexes (e.g. $MoCl_X$) in the TFT channel [7]. Choe and Kim have shown that the presence of molybdenum in the channel region, as a result of the ion bombardment in the RIE during the back channel etch, increases the off-current drastically. Complete exposure of the molybdenum S/D can cause I_{OFF} to reach as high as 10^{-9} A. On the contrary, by masking the top surface of the molybdenum with a layer of photo-resist, I_{OFF} becomes as low as 10^{-13} A [7]. We believe that the I_{OFF} decrease observed in the present study occurs because by performing the recess etch step to the S/D molybdenum pads, the metallic layer is concealed from the plasma during the back channel etch process, thus reducing the possibilities of depositing Mo complex on the back channel of the amorphous silicon TFT. Additionally, only 2.5 kÅ of over-etching is needed to reduce the TFT off-current values.

5.3.3. Possible Advantage of this Structure

While this study focuses on the d. c. analysis of the recess S/D contact transistor, the reduction between the gate and source/drain overlap could also improve its a. c. characteristics by decreasing the parasitic capacitance. The reduction in gate-to-S/D capacitance is necessary for high-resolution flat-panel displays as it minimizes image distortion [17-20]. During the end of the programming stage of an AM-LCD pixel electrode circuit, an unwanted voltage drop (feed-through voltage) on the storage

capacitor can occur due to the capacitive coupling between the scan line and the gate of the driving TFT via a parasitic capacitor [21]. This parasitic capacitor exists because the gate and the source electrodes of the switching TFT overlap, and creates a small MIS capacitor. The overlapping area is directly proportional to the parasitic capacitance, and therefore the feed-through voltage value. Our novel recess S/D TFT has a reduced overlap between the source/drain and the gate metal electrodes because of the intentional over-etch process of the molybdenum contacts. Therefore, we believe that on top of its lower leakage current characteristics, its gate-to-source parasitic capacitance value will also be reduced, which is a very desirable characteristics for high-resolution, large-size AM-LCD.

5.4. Conclusion

By introducing an intentional over-etch (2.5 kÅ) of the molybdenum source and drain contacts of the a-Si:H TFT, we were able to reduce the off region current by one order of magnitude by diminishing the introduction of metal contaminants over the back channel during the RIE process. This over-etch step minimizes the molybdenum contaminants in the back channel of the transistor. Under moderate gate bias ($V_{GS} < 20$ V), which is common for most flat-panel display applications, the transistor suffers no electrical performance degradation. It is also expected that the I_{OFF} value will be more uniform across a large area for such device. Moreover, the fabrication process of this recess source/drain contact TFT requires no additional photolithography step, and can be performed by simply extending the etching time of the source and drain contacts. This over-etch step should be performed after the S/D definition, and before the back channel

etch process to conceal the molybdenum metal from the plasma in the RIE. The alternative solution could b to perform the over-etch step after the back channel definition. Additionally, this new TFT structure is expected to have faster a. c. response and lower feed-through voltages.

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Chapter 6:

High Temperature Electrical Performance and Stability

6.1. Introduction

It is well known that the traditional a-Si:H TFTs suffer from electrical degradation, namely the positive-direction threshold voltage shift (ΔV_T). This degradation causes non-uniformity in the transistors' performance across the FPD [1-5]. This inconsistency directly impacts the luminance of the organic light-emitting diode (OLED) in each pixel of the AM-OLED [6-10]. The a-Si:H TFT with the tailored channel is not immune from these deleterious effects [11], thus necessitating a thorough study of the mechanics of these device stability issues.

Positive threshold voltage shift is due to the trapping of electrons in the hydrogenated amorphous silicon nitride gate insulator (a-SiN_X:H) [12, 13] and near the a-SiN_X:H/a-Si:H interface [14, 15], the creation of meta-stable states in the amorphous silicon [16, 17], or a combination of both mechanisms [18, 19]. Threshold voltage shift appears to be larger at elevated temperatures, because the trapping of electrons and states creation are both thermally activated processes [14]. Incidentally in AM-OLED, joule heating from the organic light-emitting diodes can reach up to 86ºC during its operation [20], which means the temperature inside an AM-OLED can reach a comparable level. Thus transistors in AM-OLEDs may operate under elevated temperature, where the

threshold voltage degradation mechanisms mentioned above are accelerated. An increase in the threshold voltage leads to the decrease in the drain current if both gate and drain voltages remain the same on a given transistor. Positive threshold voltage shift of the driving transistors in a pixel-electrode circuit of AM-OLED can lower the OLED's luminance, [21-23] since it is proportional to the current provided by the a-Si:H driving transistor [24]. This degradation negatively impacts the viewing quality of the AM-OLED.

In this study we examine our a-Si:H TFT's electrical characteristics, as well as its threshold voltage stability under extended application of current and voltage stresses at an elevated temperature. We combine the experimental results from our TFT stability measurements with a computational simulation to quantify the effect of TFT threshold voltage shift on the overall performance of an AM-OLED pixel electrode circuit.

6.2. Experimental

All electrical measurements were carried out in a Karl Suss probe station. The device temperature was regulated by means of a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Electrical characteristics were measured using an HP 4156A Parameter Analyzer via the Metrics Interactive Control Software on a computer. We measured both the linear ($V_{DS}<V_{GS}-V_T$) and saturation ($V_{D-SAT}>V_{GS}-V_T$) region transfer characteristics of our a-Si:H TFT at measurement temperatures (T_{MEAS}) ranging from 293 to 353 K; V_{DS}, V_{D-SAT}, V_{GS}, and V_T denote the drain, saturation drain, gate, and threshold voltages, respectively. Prior to the measurement, all TFTs were annealed at 473 K for 1 hr in a nitrogen oven. The chuck was first heated to the desired

T_{MEAS} before the a-Si:H TFTs with the tailored channel were placed on top of it. We allowed a 10 min stabilization time before the electrical measurement to avoid recording artifacts from thermal shock. For the electrical measurement of the TFT's transfer characteristics operating in the linear region, the parameter analyzer internally grounded the source terminal, applied a constant voltage of 0.1 V on the drain terminal, and swept the voltage on the gate terminal from -10V to 20V with a 0.1 V interval. For the saturation region transfer characteristics, the setup was identical to that of the linear region, except the analyzer internally synchronized the drain and gate terminals to the same bias instead of applying a constant bias on the drain terminal. The currents flowing into the drain, gate, and sources were collected by the parameter analyzer, with currents flowing into the terminals denoted as the positive direction. Throughout the measurement of the electrical characteristics, the TFTs remained at a specific T_{MEAS}, with fluctuation less than 0.1 K. Each transistor was measured only once at T_{MEAS} to avoid electrical and thermal stresses.

We also study the effects of prolonged application of bias stresses at an elevated temperature of 353 K (T_{STR}). During the bias temperature stress (BTS) experiments, constant biases were applied continuously to the gate, drain, and/or source of the TFTs. At specified intervals, the biases were suspended for less than 10 s to measure the saturation transfer characteristics of the transistors without changing the temperature of the transistor substrates, or T_{MEAS}=T_{STR}. The duration of the electrical stress applied to the TFT is denoted as the stressing time (t_{STR}). We acknowledge that there will be some unwanted errors from this style of measurement. First, the interruption of the bias stress to measure the transfer characteristics allows the restoration of charges, and second, the

application of voltages when taking the drain current versus gate-to-source voltage (I_D-V_{GS}) characteristics can add additional stress to the a-Si:H TFT. However, the contributions from both factors should not skew the degradation behavior significantly over a long period of time, as both the interruptions and the measurements last only a few seconds. Four BTS experiments were carried out with the following biasing conditions: a) V_{GS}=V_{DS}= 40 V, b) V_{GS}=40 V and V_{DS}=0 V, c) V_{GS}=40 V and the drain was floating, and d) V_{GD}=40 V and the source was floating (figure 6-1).

Current temperature stress (CTS) measurements were also performed. During the CTS experiment, a constant electrical current (I_{STR}) was applied to the drain of our a-Si:H TFT at T_{STR}=353 K. There were two different TFT biasing schemes for the CTS experiments: CTS 1 and CTS 2. For CTS 1, the gate was biased at 20 V while the I_{STR} was applied to the drain of the TFT. For CTS 2, the gate and the drain terminals were externally shorted together ($V_{DS}(t)$=$V_{GS}(t)$) during the CTS experiments, which meant the

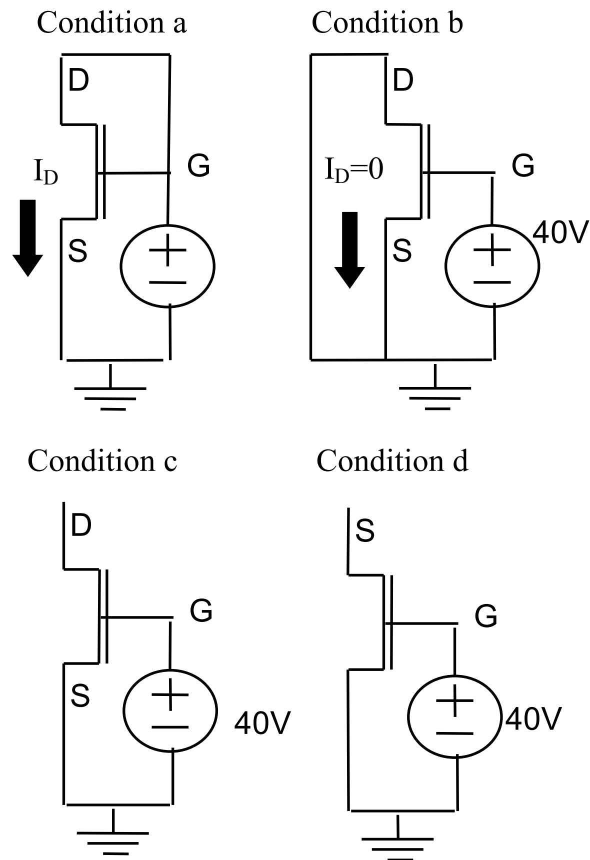

Figure 6-1: BTS experimental setups for four a-Si:H TFT stressing conditions described in the text.

I_{STR} going into the drain also set up the bias on the gate (figure 6-2). CTS 1 is equivalent to operating the TFT in the linear region, and CTS 2 operates in the saturation region. The measurement technique, stress duration, and measurement time intervals were the same as the BTS experiments. Stress current ranges from 10 nA to 5.5 μA to reflect the current levels required to drive an OLED pixel of a XGA display [25].

It is important to emphasize that BTS and CTS apply electrical stresses to transistors differently over a long period of time. In BTS the biases at the gate, drain, and source are biased at constant voltages throughout the stressing experiment; this means that the band bending in the amorphous silicon reduces over time because the electrons trapped near the a-Si:H/a-SiN_X:H interface shield the mobile electrons in the channel. On the contrary, the gate and/or drain voltages in the CTS experiment increases over time to maintain the stressing current that would otherwise decrease due to electrical stress induced degradation (shift towards more positive V_{GS}) of the a-Si:H TFT's. The increase in biasing voltages keeps the band bending in the a-Si:H constant. In the BTS experiment, the current decreases and the bias remains constant, while in the CTS experiment the bias increases and the current remains the same. These discrepancies lead to difficulties when comparing results collected

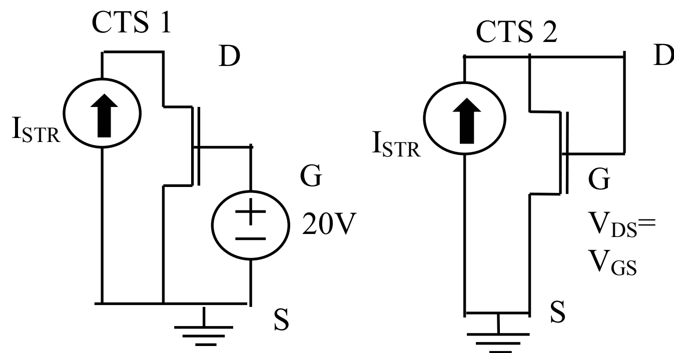

Figure 6-2: CTS experimental setups used in this work: CTS 1 (V_{GS}=20 V) and CTS 2 (V_{GS}=V_{DS}). The stress current (I_{STR}) levels are 10 nA, 500 nA, and 5.5 μA.

from BTS and CTS experiments. Lastly, the actual temperature inside the amorphous silicon bulk may exceed T_{STR} by almost 50 K due to joule heating from the electrical current. However, since this study focuses on the operation of TFTs at higher external temperature, we present the cumulative effect of external and internal heating on the thermal degradation mechanism for the TFTs.

6.3. Results and Discussion

6.3.1. Temperature Effect on the a-Si:H TFT

From the transfer characteristics of the a-Si:H TFT with the tailored channel (figure 6-3), we extracted the field-effect mobility (μ_{EFF}), threshold voltage (V_T), and subthreshold swing (S) of the transistors at different measurement temperatures (figure 6-4). Experimental data were fitted to the transistor square law equations based on the gradual channel approximation for linear and saturation regions of operation to obtain the μ_{EFF} and V_T [26]:

$$I_{D-LIN} = \frac{W}{L}\mu_{EFF}C_{INS}(V_{GS} - V_T - \frac{V_{DS}^2}{2})V_{DS}\,, \tag{6-1}$$

$$(I_{D-SAT})^{1/2} = (\frac{W}{2L}\mu_{EFF}C_{INS})^{1/2}(V_{GS} - V_T)\,. \tag{6-2}$$

Even though the amorphous silicon transfer characteristics can deviate from ideal with non-linear transfer characteristics (i.e. exponent of V_{GS}-V_T term is not 1), we use data range from 10-90 % of $I_D(V_{GS}=20\ V)$ in order to compare different μ_{EFF} values [27]. If the exponent of V_{GS}-V_T changes with the temperature, μ_{EFF} will have different units ($cm^2\ V^{-exp}\ s^{-1}$ instead of $cm^2\ V^{-1}\ s^{-}1$) and can no longer be evaluated fairly. Our choice of using 10-90% data range is justified by the consistency of both the linear and saturation

region transfer characteristic curvatures within this range: the mean exponents based on the non-linear [27] fit are 1.061 with a standard deviation of 0.0007 in the linear region, and 1.068 with a standard deviation of 0.001 in the saturation region, respectively, for T_{MEAS} ranging from 293 to 353 K. The S values were extracted by selecting a set current

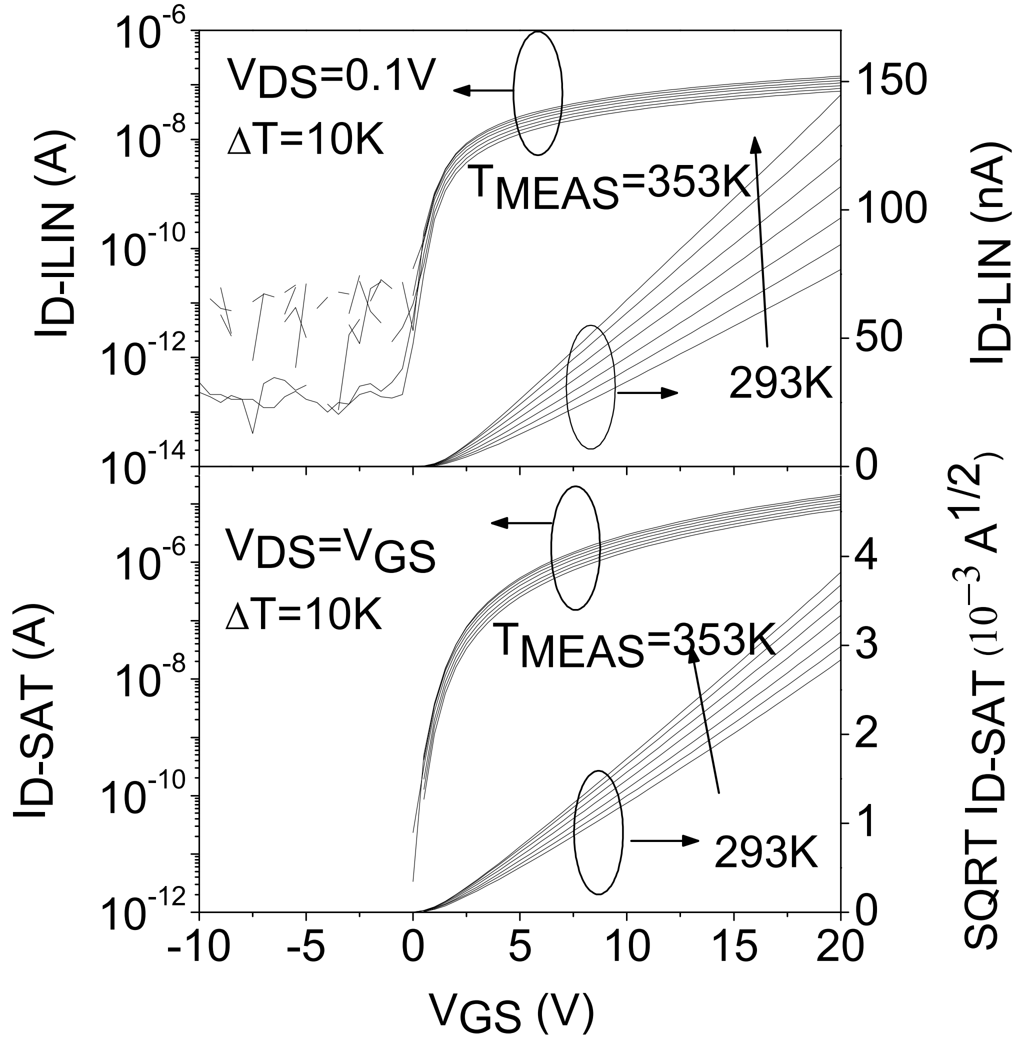

Figure 6-3: Linear and saturation transfer characteristics of a-Si:H measured from (T_{MEAS}) = 293 to 353K.

value for each region of operation, 0.1 nA for the linear and 1 nA for the saturation, as the center value, and fitting a straight line to three data points near the center (center value, plus one point above and below it). The inverse of the slope of the straight line is defined as the subthreshold swing value. This method defines S at a given current density level, which allows an unbiased comparison of the TFT characteristics at

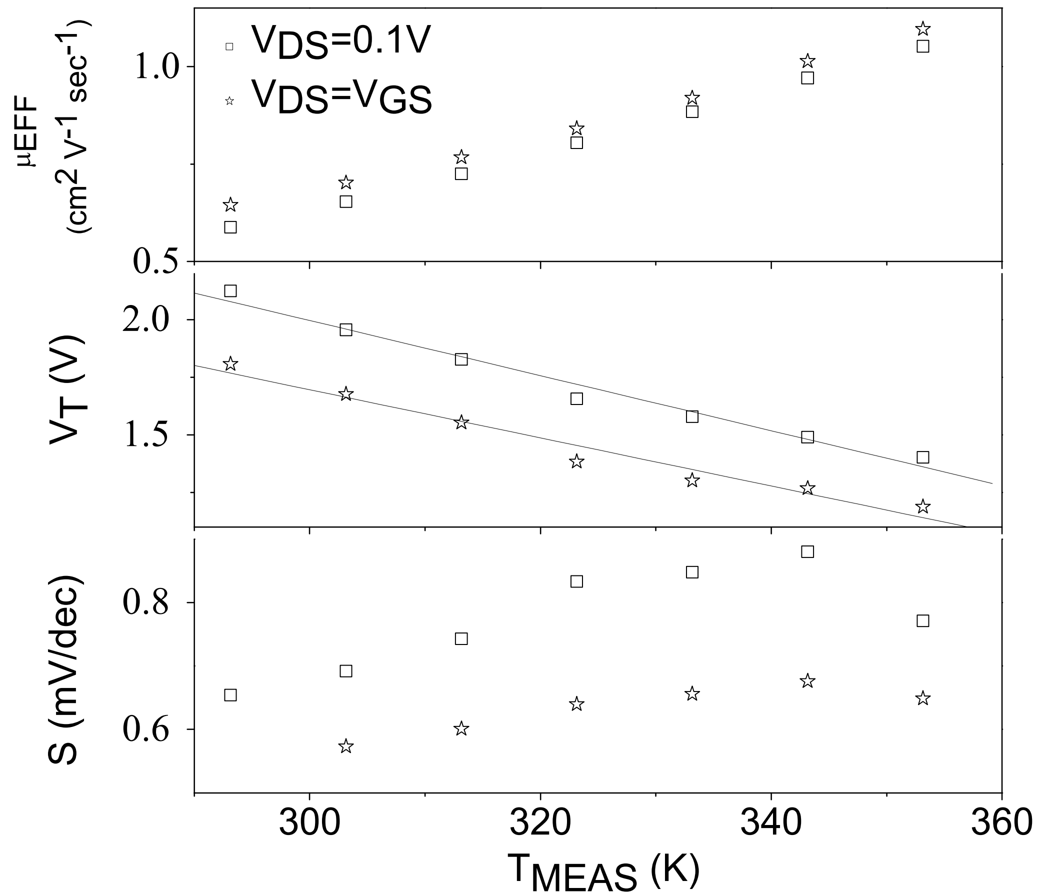

Figure 6-4: Field effect mobility, threshold voltage, and subthreshold swing change with the measurement temperature. Symbols represent experimental data and lines are numerical fit.

different T_{MEAS} [28]. Both μ_{EFF} and S increase with temperature, while V_T decreases with increasing temperature. Details of the physics dictating these behaviors have been addressed by numerous groups [17, 18, 29, 30]. Larger mobility values at higher

temperatures suggests that the transport of carriers obey the multiple trapping model described by LeComber and Spear [31] as well as Tiedje *et al.* [32]. In the multiple trapping model, electrons at high temperature (>240 K) moves through amorphous silicon by alternating between drifting along the extended states of the conduction band, and residing in localized deep gap states. The transition between the two modes is due to the trap and thermal release of carriers, which causes the increase in the mobility at a higher temperature as electrons escape from the deep traps more frequently. The relation between the mobility and temperature in the multiple trapping model is exponential in nature and can be described by [29-32]:

$$\mu = \mu_O \exp(-\frac{E_D}{kT_{MEAS}}) . \quad (6\text{-}3)$$

In (6-3), μ_O is the mobility prefactor and E_D is the electron mobility activation energy; our TFT has E_D of 87.5meV and μ_O of 18.67 $cm^2\ V^{-1}\ s^{-1}$ in the linear region and 81.1meV and 15.70 $cm^2\ V^{-1}\ s^{-1}$ in the saturation region (figure 6-5).

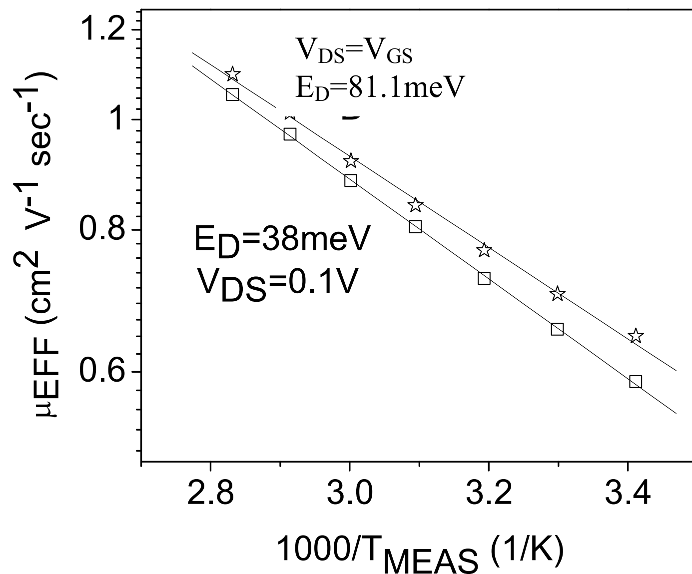

Figure 6-5: Field-effect mobility variation as function of $1/T_{MEAS}$ for a-Si:H TFT used in this work.

The activation energy signifies the energy difference between the edge of

conduction band (E_C) and the Fermi level (E_F); it equates to the average energy required for the electrons trapped in the localized states to gain in order to jump into the extended states [32, 33]. One note we need to emphasize is that the temperature has the same effect on both field-effect mobility and drift mobility [34], which means that the temperature effect is intrinsic to the amorphous silicon, not dependent on the device geometry or operation.

Lustig *et al.* also attributed it to a decrease in contact resistance at an elevated temperature. Based on a simulation of the a-Si:H TFT with different source/drain contact resistance values, field-effect mobility increases from 0.6 to 1.1 $cm^2 V^{-1} sec^{-1}$ when specific contact resistance decreases from 0.9 to 0.2 Ω-cm^2 [35]. Based on a simulation of the a-Si:H TFT with different source/drain contact resistance values, field-effect mobility increases from 0.6 to 1.1 $cm^2 V^{-1} s^{-1}$ when the specific contact resistance decreases from 0.9 to 0.2 Ω-cm^2 [35]. However, it is unlikely for the specific contact resistance to decrease by a factor of 4 with a temperature increase of 60 K. This leads us to conclude that even though the contact resistance may decrease with the increasing temperature, the primary cause for the observed mobility increase comes from the thermal activation of the electron transport within the device channel.

The threshold voltage decreases with the increasing temperature because a lower surface potential is needed to release the trapped electrons in the bulk amorphous silicon from the localized states into the extended states at an elevated temperature [36]. Moreover, the surface state ionization at the a-SiN_X:H/a-Si:H interface also contributes to this decrease [37]. As free electrons from both ionization processes accumulate near the interface, the surface band bending increases, and the Fermi level at the interface moves

closer toward the conduction band. A linear equation is used to describe the threshold voltage dependence on the transistor operating temperature [29]:

$$V_T(T_{MEAS}) = V_T(T_O) - \alpha(T_{MEAS} - T_O)\,. \qquad (6\text{-}4)$$

T_O is the room temperature in Kelvin and α is an empirical parameter extracted from experiment: for our devices we obtain α values of 0.012 for the linear region and 0.01 for the saturation region, and $V_T(T_O)$ values of 2.15 V for the linear region and 1.78 V for the saturation region, respectively. The ionization of both bulk and interface states is also responsible for the increase in subthreshold swing with the temperature. More available states in both the deep and shallow states at a higher temperature leads to larger S value because the Fermi level sweeps at a slower rate due to the pinning of unoccupied states. By using an equation for maximum bulk (N_{bs}) and surface (N_{ss}) state densities calculation [38]:

$$S = \frac{kT_{MEAS}}{q\log(e)}\left[1 + \frac{qx_i}{\varepsilon_i}\left(\sqrt{\varepsilon_s N_{bs}} + qN_{ss}\right)\right], \qquad (6\text{-}5)$$

we found that for T_{MEAS} of 293.15 to 343.15 K, N_{bs} changes from $1.4\text{x}10^{17}$ to $1.9\text{x}10^{17}$ $cm^{-3}\ eV^{-1}$ for the linear region and from $9.8\text{x}10^{16}$ to $1.07\text{x}10^{17}$ $cm^{-3}\ eV^{-1}$ in the saturation region when N_{ss} is assumed to be 0. Similarly N_{ss} in the same T_{MEAS} range changes from $9.63\text{x}10^{11}$ to $1.12\text{x}10^{12}$ $cm^{-2}\ eV^{-1}$ for the linear region and from $8.01\text{x}10^{11}$ to $8.38\text{x}10^{11}$ $cm^{-2}\ eV^{-1}$ in the saturation region when N_{bs} is assumed to be 0. In this equation, ε_i and ε_s are the a-SiN_X:H and a-Si:H dielectric constants, respectively. Even though this calculation does not separate the bulk and surface states when calculating the subthreshold swing value, we see that both can increase with the operating temperature of the transistor.

We extracted the drain current activation energy (E_{AC}) at different gate biases following method described by Lustig and Chen [30, 39, 40], and the resulting activation energies for different V_{GS} values are shown in figure 6-6. The drain current activation energy decreases from 112 to 90 meV in the linear region, and 120 to 75 meV in the saturation region when V_{GS} increases from 2 to 20 V. This trend is consistent with results reported by Lustig and Chen, but the range is lower: their drain current activation energy values decrease from about 500 to 50meV as V_{GS} increases from 2 to 20V for both linear and saturation regions. This activation energy represents the average energy required for the electrons to escape from the less mobile deep trap states into the more mobile band tail states [37]. Naturally as band bending increases, as a result of the application of gate voltage, this energy decreases because the Fermi level moves closer to the edge of the conduction band tail states. More importantly, the range of E_{AC} value is indicative of the electronic quality of the amorphous silicon. For a steep conduction band tail slope, the Fermi level lies closer to the conduction band edge due to less pinning effect, which results in a smaller E_{AC}. On the contrary, a lower electronic quality amorphous silicon will have a higher range of values of activation energy. Chen computed the a-Si:H TFT drain current activation energy values for the gate voltage ranging from 0 to 20V with different conduction band tail slope values [35]. Based on his simulation results [35], our amorphous silicon has a conduction band tail slope around 28±3 meV.

The dual a-Si:H and a-SiN_X:H layers TFT shows promising linear region electrical performance with a field-effect mobility of 0.6 $cm^2 V^{-1} s^{-1}$, threshold voltage of 2.1 V, and subthreshold swing of 0.65 V/dec at room temperature, and a field-effect mobility of 1.1 $cm^2 V^{-1} s^{-1}$, threshold voltage of 1.4 V, and subthreshold swing of 0.77 V/dec at 353 K. The drain current activation energy decreases from 120 to 90 meV as V_{GS} increases from 2 to 20V. The conduction band-tail slope is around 28 meV. Compared to the state-of-the-art a-Si:H TFT with the active and gate insulator layers deposited using the conventional single-step processes, the a-Si:H TFT with the tailored channel shows promising electrical performance while having the advantage of a shorter overall deposition time.

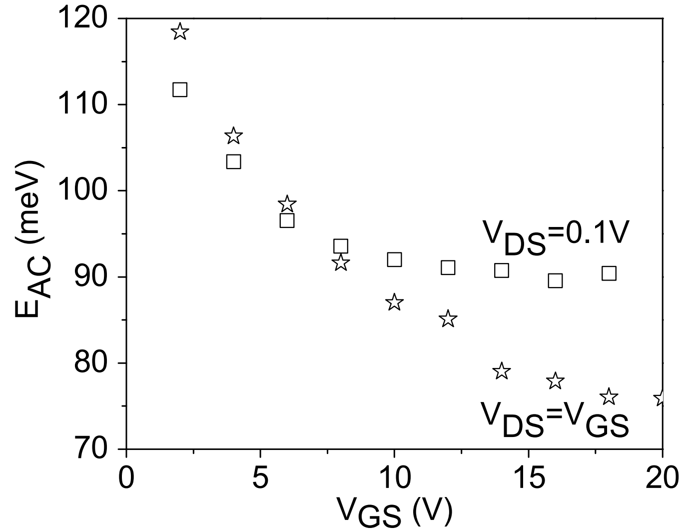

Figure 6-6: Drain current activation energy value versus gate voltage for linear (V_{DS}=0.1V) and saturation (V_{DS}=V_{GS}) regions of device operation.

6.3.2. Bias Instability of a-Si:H TFT

Figure 6-7 (top) shows the evolution of the saturation transfer characteristics with the stress time (t_{STR}) for BTS condition (a) in linear scale. The device degradation is defined as the change in threshold voltage (ΔV_T)

$$\Delta V_T = V_T(t = t_{STR}) - V_T(t = 0)\,. \tag{6-6}$$

Threshold voltage is extracted from the saturation region transfer characteristic and the method of extraction is described in the previous section. Each transfer curve in figure 6-8 signifies the electrical performance of the a-Si:H TFT at a given t_{STR}. As stressing time progresses, the curves shift to the right while the slope remains the same. When using the linear fit extraction method described earlier, the field-effect mobility remains the same with increasing t_{STR}; we only need to address the increase in the threshold voltage.

Figure 6-8 shows the variations of the ΔV_T for the four BTS conditions described above (a, b, c, d), in both log and linear scales. The largest degradation (b) occurs when a high electric field (1MV/cm) is setup across the entire gate insulator, assuming the entire

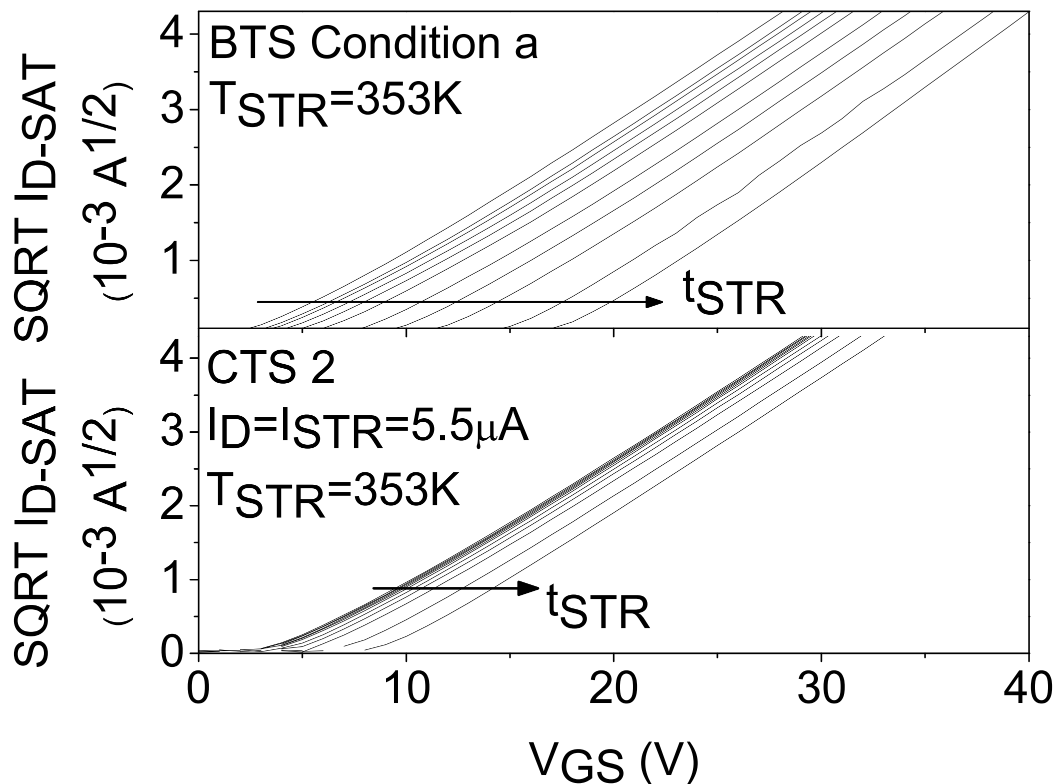

Figure 6-7: Example of $I_{D\text{-}SAT}^{1/2}$ vs. V_{GS} in the saturation region of operation during BTS (top) and CTS (bottom).

channel area is grounded by the source and drain terminals. TFTs stressed under conditions (c) and (d) have similar ΔV_T compared to condition (b). Even though either the source or drain terminal is floating, the potential at the floating terminal should be similar to the grounded terminal because the current flow between the two terminals is negligible. This suggests that the electric field profile across the gate insulator for conditions (c) and (d) is similar to that of condition (b), resulting in similar ΔV_T. The lowest shift occurs in condition (a), even though it is the only one with a current flow during the electrical stressing. Our BTS experiments confirms observation made by other groups that a high drain current alone does not necessarily lead to a high threshold voltage shift in an a-Si:H TFT [19, 41]. This agrees with observation made by Powell *et a.l*, where they suggest a strong field dependence of the trapping mechanism in the a-SiN_X:H and near the a-SiN_X:H/a-Si:H interface [19]. One theory that explains such observation is that the electron hopping at the Fermi level is proportional to the gate-induced electric field [42]. In BTS condition (a), only the source region experiences high gate electric field, so the majority of electron trapping occurs near the source. In BTS conditions (b), (c), and (d), however, the entire channel region of the TFT experiences a high electric field. Thus the TFT stressed under these BTS conditions show larger threshold voltage shifts because electrons accumulated in the entire channel can hop along the Fermi level into the amorphous silicon nitride gate dielectric. This result indicates that the most stable operational region for the a-Si:H TFT with the tailored channel is when the gate and drain electrical potentials are identical because the gate-induced electric field near the drain region is minimized. Under such biasing condition,

only the source region experiences a high gate-induced electric field. Such region of operation is the saturation region of operation, where $V_{GS}<V_{DS}-V_T$.

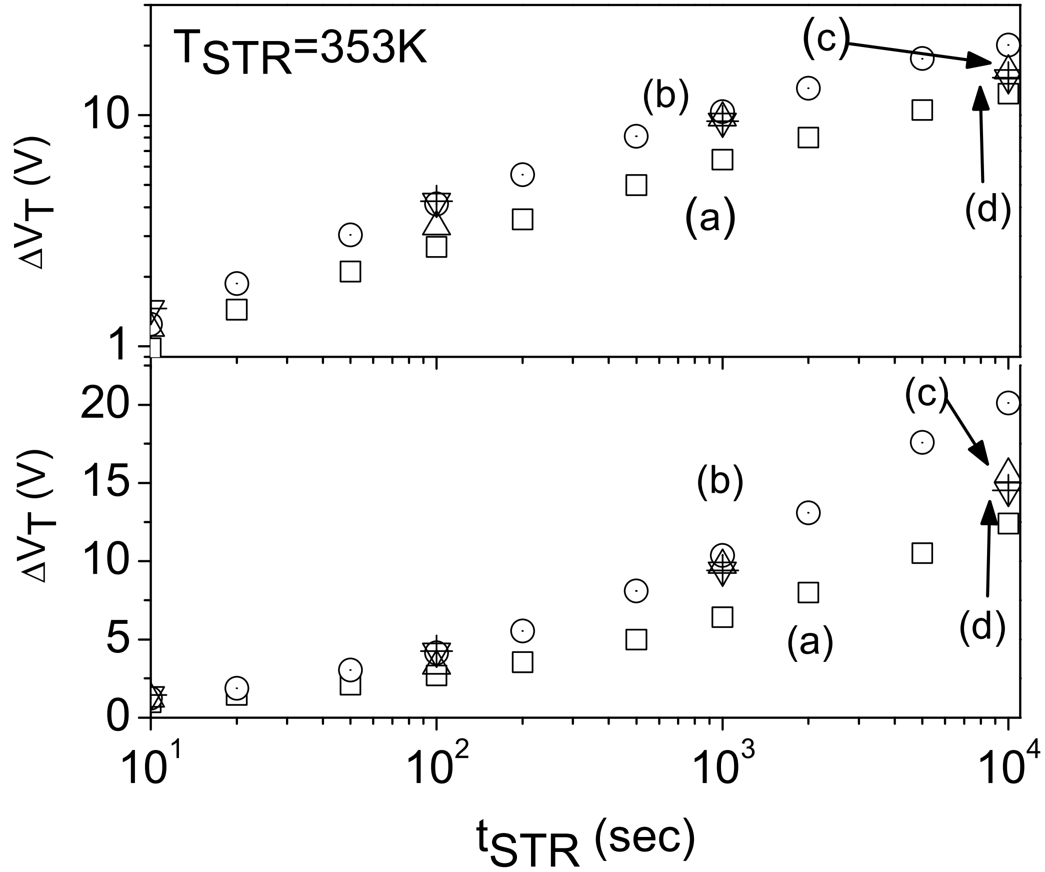

Figure 6-8: Variation of ΔV_T with the stress time on both log (top) and linear (bottom) scales, at T_{STR}=353 K, for the following BTS conditions: a) $V_{GS}=V_{DS}$=40 V, b) V_{GS}=40 V and V_{DS}=0 V, c) V_{GS}=40 V and the drain is floating, and d) V_{GD}=40V and the source is floating.

6.3.3. Current Instability of a-Si:H TFT

The extraction of device degradation for the CTS experiment is the same as for the BTS experiment: using the threshold voltage shift of the saturation transfer characteristics as the parameter to quantify electrical instability. The TFT transfer characteristics for different t_{STR} are shown in figure 6-7 (bottom). The ΔV_T plot versus

t_{STR} of the a-Si:H TFTs under CTS is shown in figure 6-9 (symbols). The top portion represents the CTS experiments conducted under linear region of operation (CTS 1) and the bottom portion represents the saturation region of operation (CTS 2). The TFTs undergoing current temperature stress suffer larger device degradation when they operate in the linear region than the saturation region. For example, with 500 nA of stress current, the transistor biased in CTS 1 condition has a ΔV_T of almost 6 V after 10,000 s, where the TFT biased in CTS 2 only experienced a ΔV_T of less than 1 V for the same T_{STR} and t_{STR}. The transistors' high temperature electrical stability improves up to a factor of five when changing the biasing condition from CTS 1 to CTS 2. Under the more stable CTS biasing condition, namely CTS 2, the highest threshold voltage shift is less than 4 V when I_{STR}=5.5 μA, t_{STR}=10,000s, and T_{STR}=353 K. This trend is consistent with the observation made in the BTS experiments. Changing biasing condition on a transistor extends its operational lifetime: under CTS 1, an a-Si:H TFT with the tailored channel stressed with 5.5 μA of current at 353 K has a threshold voltage shift of 2 V after only 31 s, where as the TFT experiencing the same thermal (T_{STR}=353 K) and electrical (I_{STR}=5.5 μA) stress biased in CTS 2 condition reaches the same level of shift after 2600 s.

Based on the CTS experiments, we can see that the biasing conditions of the gate and drain are critical for minimizing the threshold voltage shift of our a-Si:H TFT. Two identical TFTs can suffer different threshold voltage shifts while driving the same current, if the gate-to-drain electric fields are different. In the case of CTS 1 biasing, a large fraction of the gate insulator experiences a high electric field, up to 0.5 MV/cm near the source region and 0.35 MV/cm near the drain region for I_{STR}=5.5 μA. The large gate

field accelerates electrons into the insulator and causes the formation of trapped charges near the a-Si:H/a-SiN_X:H interface. On the contrary, the same TFT undergoing CTS with the gate and drain shorted together (CTS 2) experiences much less electrical degradation, even if the stress current and temperature are identical. This is due to a reduction of the electric field across the gate insulator by biasing the gate and drain at the same potential: for I_{STR}=5.5 μA, the highest value of the gate-induced electric field (0.32 MV/cm) occurs at the source, and no vertical electric exists at the drain. The calculation of electric field is done by dividing the gate voltage by the total gate insulator thickness; this calculation assumes that all the applied voltages are dropped across the gate insulator. Under this condition, only electrons close to the source get accelerated and injected into the gate insulator as trapped charges that contribute to a positive direction threshold voltage shift. Electrons near the drain region only experience a lateral electric field. Since the electron hopping via E_F is gate-field dependent, CTS 2 results in smaller threshold voltage shift than CTS 1 because: (i) field induced trapping only occurs near the source region instead of the entire channel, and (ii) the vertical electric field near the source is reduced by 40 %, from 0.5 to 0.32 MV/cm. Under CTS 2 stressing condition, the maximum threshold voltage shift we observe is less than 4V when I_{STR}=5.5 μ, T_{STR}=353 K, and t_{STR}=10,000s.

We demonstrated that transistors operating in the saturation region suffer less electrical characteristic degradation during the electrical stress due to a reduction of gate-induced electric field. We would like to emphasize that this reduction physically can translate to decreases in charge trapping, creation of meta-stable states, or a combination of both mechanisms that contribute to the threshold voltage instability. This concept is

fully applicable to a current-driven AM-OLED circuit: driving TFTs in AM-OLED should ideally operate in the saturation region, because it makes the drain current invariant to the drain voltage, and is only controlled by the gate voltage [43].

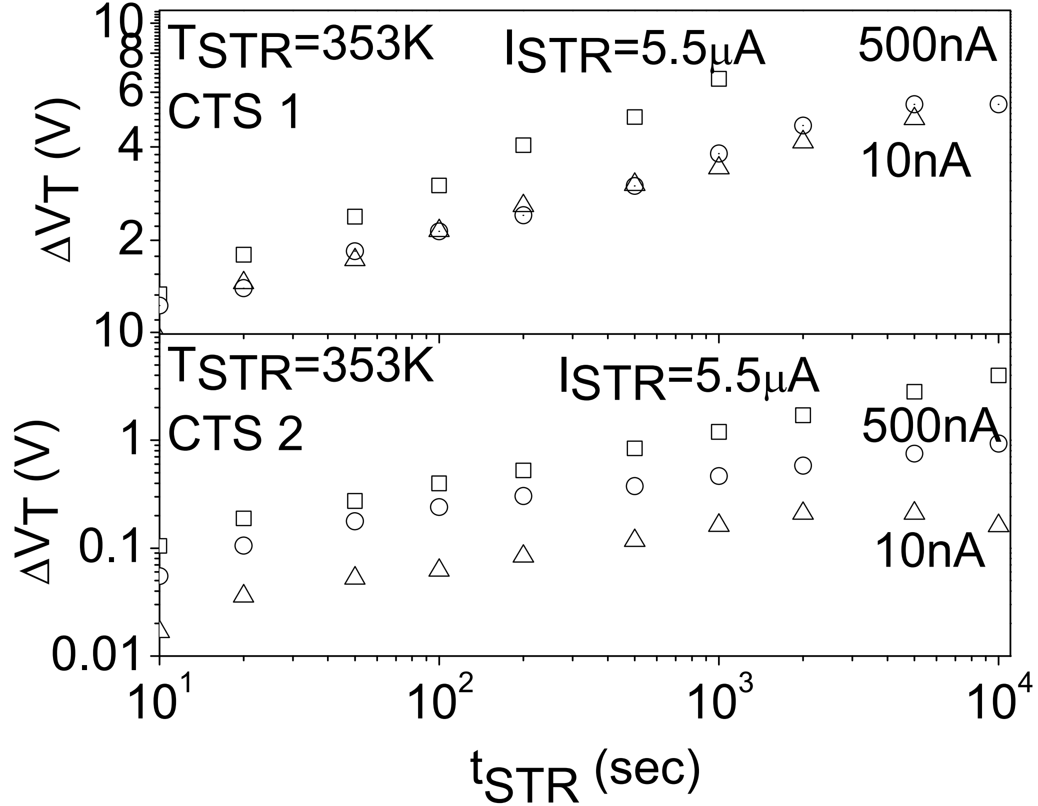

Figure 6-9: CTS induced ΔV_T extracted from figures with stress temperature at T_{STR}=353 K for V_{GS}=20 V (top) and $V_{GS}(t)= V_{DS}(t)$ (bottom).

6.4. Impact of the Threshold Voltage Shift on AM-OLED

In this section, we evaluate the impact of the threshold voltage degradation on the electrical performance of a pixel electrode circuit for AM-OLED proposed by Lin *et al.* [21, 44]. During the on-state of the pixel electrode circuit proposed by *Lin et al* (figure 6-

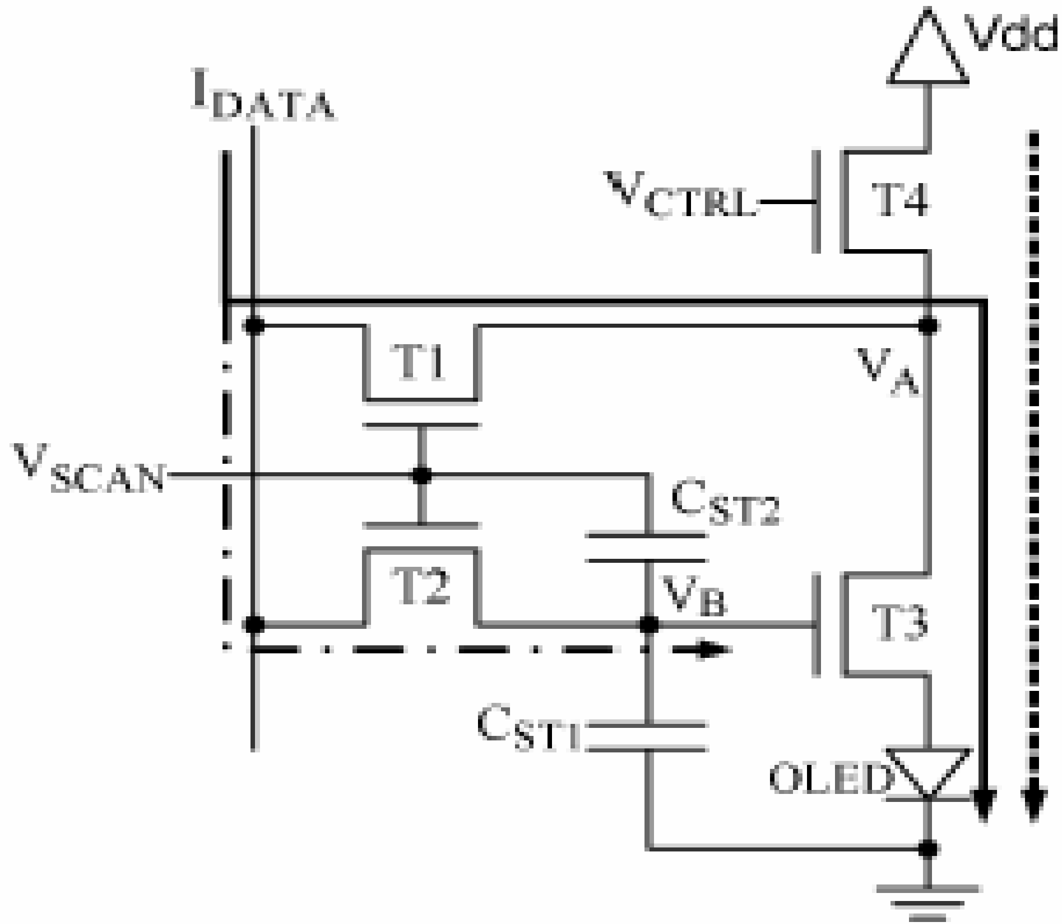

Figure 6-10: Schematic diagram of current-driven AM-OLED pixel electrode circuit proposed by Lin *et al* [21].

10) [21], V_{SCAN} turns on switching transistors T1 and T2 to allow the data current (I_{DATA}) to charge the storage capacitors C_{ST1} and $C_{ST2.}$ As the pixel electrode circuit switches from the on-state to the off-state, V_{SCAN} turns T1 and T2 off while V_{CTRL} turns T4 on. Charges stored in C_{ST1} and C_{ST2} during the on-state remain as T2 is turned off, however $V_{B\text{-}ON}$ changes from its on-state value, as determined by I_{DATA}, to its off-state value ($V_{B\text{-}OFF}$) because of the change in the V_{SCAN} value [21]:

$$V_{B-OFF} = V_{B-ON} - \Delta V_{SCAN} \cdot \frac{C_{ST2} // C_{OV-T2}}{C_{ST1} + C_{ST2} // C_{OV-T2}} = V_{B-ON} - V_{SCALING} . \qquad (6\text{-}7)$$

With $V_{B\text{-}OFF}$ holding its off-state value, it determines the amount of OLED current (I_{OLED}) flowing through T4, T3, and the OLED during the off-state of operation. Figure 6-11 shows the timing diagram of the pixel electrode circuit.

The threshold voltage shift compensation takes place because $V_{B\text{-}ON}$ is determined by I_{DATA}, μ_{EFF}, C_{INS}, V_T, W, and L of T3; it will automatically adjust with the changing threshold voltage of T3 to allow I_{DATA} to flow through. The following equation is modified from (6-2), and replaced with the variables discussed in this section to show the change in $V_{B\text{-}ON}$ with the threshold voltage [21],

$$\left[\frac{I_{DATA}}{\frac{W_3}{2L_3}\mu_{EFF}C_{INS}}\right]^{1/2} + \left(V_T + \Delta V_T\right) = V_{B-ON}\,. \tag{6-8}$$

The symbols V_T and ΔV_T stand for the initial threshold voltage value and the change in the threshold voltage, respectively. The value in the parenthesis represents the total threshold voltage of T3. It is clear that even though $V_{B\text{-}ON}$ is set by I_{DATA}, it increases linearly with ΔV_T to achieve the compensation effect to the threshold voltage instability. Therefore, ideally any threshold voltage shift of T3 will be fully compensated through I_{DATA} by increasing the voltage at V_B and V_A nodes, and the off-state OLED current will not be affected by the threshold voltage shift of T3, as demonstrated by the following equations [21]:

$$I_{OLED} = \frac{W_3}{2L_3}\mu_{EFF}C_{INS}(V_{B-OFF} - (V_T + \Delta V_T))^2, \tag{6-9}$$

$$I_{OLED} = \frac{W_3}{2L_3}\mu_{EFF}C_{INS}(V_{B-ON} - V_{SCALING} - (V_T + \Delta V_T))^2, \tag{6-10}$$

$$I_{OLED} = \frac{W_3}{2L_3}\mu_{EFF}C_{INS}(\left(\frac{I_{DATA}}{\frac{W_3}{2L_3}\mu_{EFF}C_{INS}}\right)^{1/2} + (V_T + \Delta V_T) - V_{SCALING} - (V_T + \Delta V_T))^2, \quad (6\text{-}11)$$

$$I_{OLED} = \frac{W_3}{2L_3}\mu_{EFF}C_{INS}(\left(\frac{I_{DATA}}{\frac{W_3}{2L_3}\mu_{EFF}C_{INS}}\right)^{1/2} - V_{SCALING})^2. \quad (6\text{-}12)$$

We can see from the above OLED current equation that the threshold voltage shift has no effect on the OLED current in the ideal case. However, another factor could influence I_{OLED}: threshold voltage shift of T4 along with the channel length modulation effect of T3. Our analysis will focus on the ΔV_T of T4 during the off-state, with the assumption that T3's ΔV_T can be fully compensated. Even though T4 is defined as a switching transistor, it experiences the same amount of current flow as the driving transistor (T3) throughout the off-state. During the on-state of the circuit, T4 provides the data current to the OLED, and a positive threshold voltage shift of T4 results in a decrease in the OLED current during the off-state. This is caused by the effective increase in the channel resistance associated with the threshold voltage degradation of T4, and the channel length modulation of T3 [21]. As T4's channel resistance increases, a larger voltage drops across its source and drain, which leads to a smaller voltage drop across the source and drain of T3. This causes the T3 drain current to decrease because of the channel length modulation factor, along with the OLED luminance. Quantitatively this decrease in OLED current can be computed by solving the OLED current equations flowing through T3 and T4 simultaneously. We developed the following equations to describe the

relation between ΔV_T and ΔI_{OLED} caused by T4's electrical instability (ΔV_{T4}) and T3's channel length modulation factor (λ):

$$I_{OLED} = \frac{W_3}{2L_3}\mu_{EFF}C_{INS}(V_{B-OFF}'-V_T)^2(1+\lambda V_A'), \quad (6\text{-}13)$$

$$I_{OLED} = \frac{W_4}{2L_4}\mu_{EFF}C_{INS}((V_{CTRL}'-V_A')-(V_T+\Delta V_{T4}))^2. \quad (6\text{-}14)$$

We simplified the mathematics by setting the voltage across the OLED (V_{OLED}) as the reference: $V_{CTRL}' = V_{CTRL}-V_{OLED}$, $V_A' = V_A-V_{OLED}$, and $V_{B-OFF}' = V_{B-OFF}-V_{OLED}$. The channel length modulation factor is set at 0.05 V^{-1}, and we assume that T3 and T4 have identical transistor geometric and electrical parameters. By setting the two OLED equations equal to each other, we can solve the value of V_A' using the quadratic formula

$$V_A'^2-V_A'\left[2(V_{CTRL}'-(V_T+\Delta V_{T4}))+\lambda(V_{B-OFF}'-V_T)^2\right]+\left[(V_{CTRL}'-(V_T+\Delta V_{T4}))^2-(V_{B-OFF}'-V_T)^2\right]=0, \quad (6\text{-}15)$$

and

$$V_A' = \frac{-B\pm\sqrt{B^2-4AC}}{2A}, \quad (6\text{-}16)$$

where A = 1, $B = [2(V_{SCAN}'-(V_T+\Delta V_{T4}))+\lambda(V_{B-OFF}'-V_T)^2]$, and $C = [(V_{SCAN}'-(V_T+\Delta V_{T4}))^2-(V_{B-OFF}'-V_T)^2]$. It is important to clarify that we only account for the channel length modulation of T3, not T4. Moreover we assume the ideal case where charges stored on C_{ST1}, C_{ST2}, and the gate of T3 remain constant throughout the off-state, with negligible dielectric leakage and charge injection from T2. Based on (13, 14), we plot the simulated result for the OLED current decrease (ΔI_{OLED}), as defined by equation 5 in [21], with respect to the threshold voltage shift of T4 for the I_{OLED} values ranging

from 0.1 to 4 μA (figure 6-12). This range is selected to reflect current values necessary

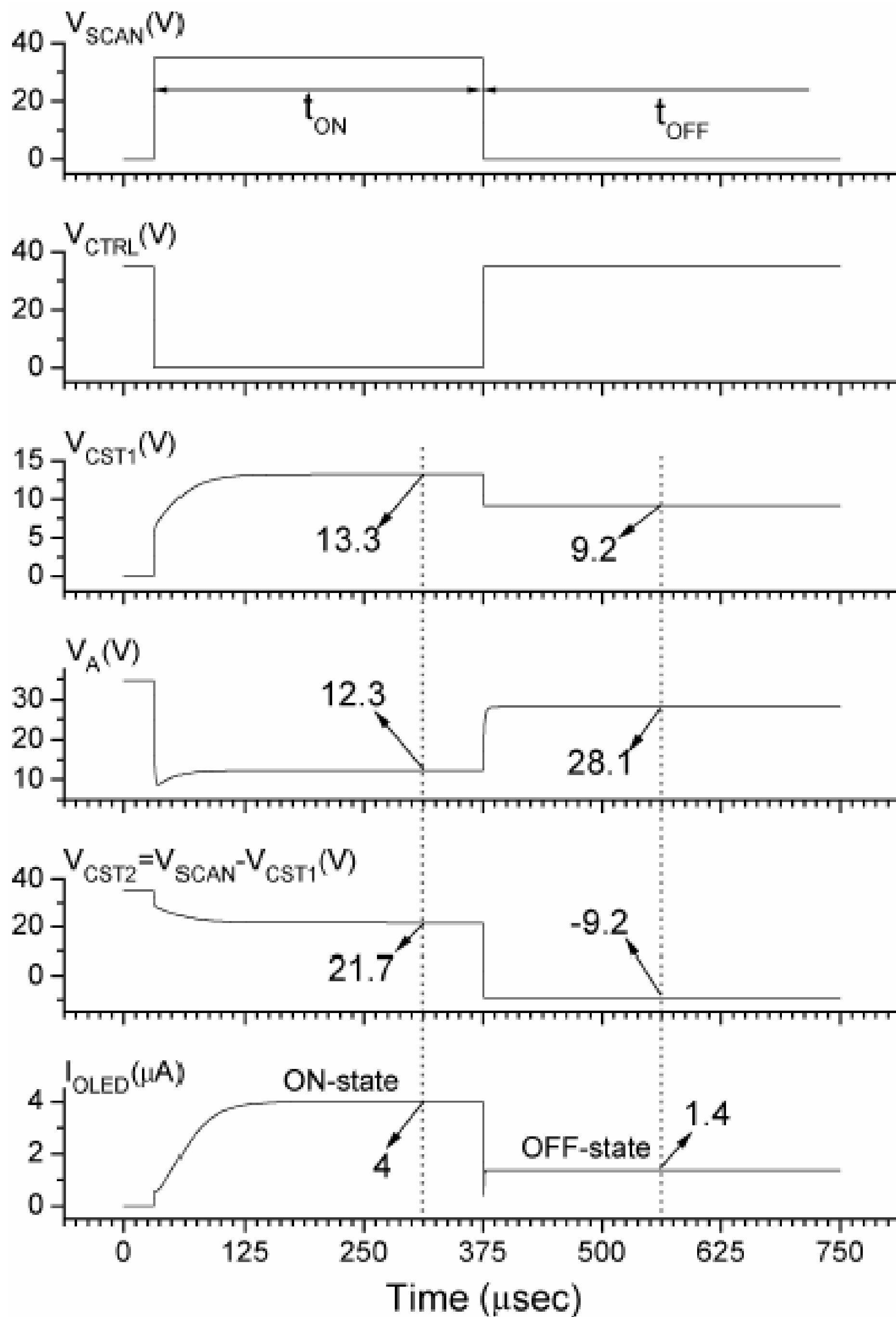

Figure 6-11: Timing diagram of current-driven AM-OLED pixel electrode circuit proposed by Lin *et al* [21].

to drive an OLED in XGA displays at various gray scales [21]. At a given I_{OLED}, there is a linear dependence between the OLED current decrease and T4's threshold voltage

increase: a ΔV_T increase from 1 to 7 V causes ΔI_{OLED} to increase from 2.5 to 17.1 % for I_{OLED}=4 μA. Moreover, for a constant ΔV_{T4}, the ΔI_{OLED} increases with I_{OLED} as seen in the inset of figure 6-12, where we plot the ΔI_{OLED} versus I_{OLED} for ΔV_T ranging from 1 to 4 V. OLED current degradation occurs in the presence of ΔV_T regardless of the magnitude of the actual OLED current level. Based on our CTS experimental result, we see that after applying I_{STR} of 5.5 μA for 1000 s at 353 K, if T4 is biased in CTS 2 mode, the ΔI_{OLED} will be 2.9 % when driving an I_{OLED} of 4 μA. This OLED degradation

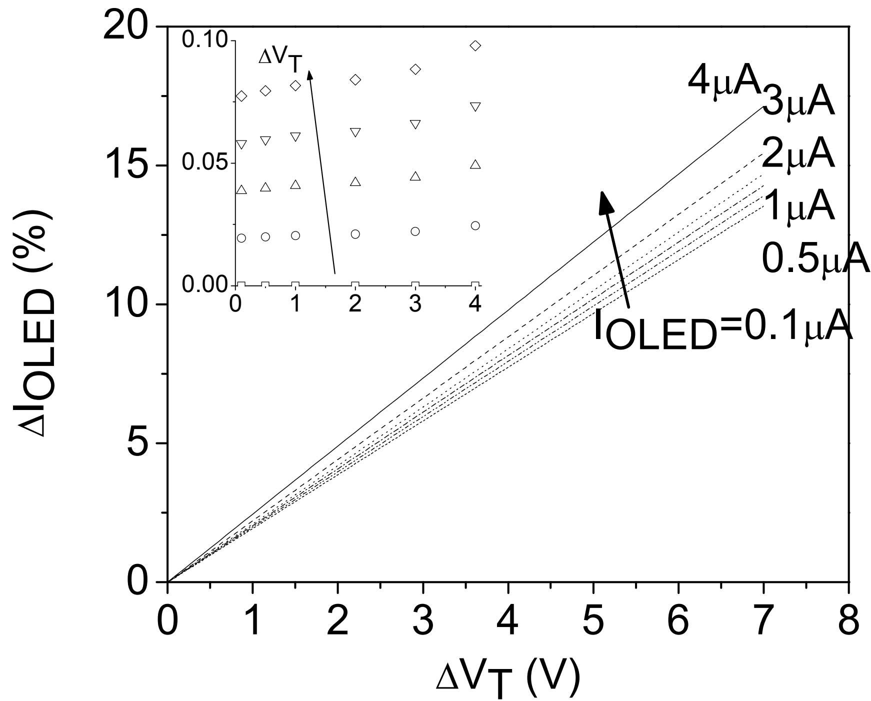

Figure 6-12: Simulated OLED current decrease with T4 threshold voltage shift and T3 channel length modulation factor of 0.05. The inset shows ΔI_{OLED} with I_{OLED} ranging from 0.1 to 4μA for ΔV_T of 0 to 4V.

increases to 16.2 % if the biasing scheme for T4 is CTS 1. This drastic change suggests that all transistors in pixel electrode circuit should be biased in CTS 2 scheme to prolong the operation of the entire display panel.

6.5. Conclusion

We have shown that the amorphous silicon thin-film transistors deposited at a high rate have a promising electrical performance, with an acceptable field-effect mobility and a low drain current activation energy. Our a-Si:H TFT, which has a relatively small W/L ratio, can withstand up to 5.5 μA of current stress for 10,000 s at 353 K and still suffers a ΔV_T of less than 4 V, which shows comparable electrical stability properties compared to the TFTs fabricated using the conventional deposition method. The transistors operating in the saturation region undergo less threshold voltage shift during the electrical stressing than the same transistors operating in the linear region. This trend was observed in both CTS and BTS experiments. For the AM-OLED pixel electrode circuit studied in this thesis, the application of 5.5 μA of continuous stress current for 1000 s at 353 K causes a threshold voltage shift of 1.2 V, which translates to a 2.9% decrease for the OLED current of 4 μA. Changing the operating condition of a-Si:H from the linear to the saturation region in a pixel electrode circuit alone can achieve a factor of five improvement in the circuit electrical stability. This technique can improve the stability of TFT regardless of its electrical performance and quality because it does not require making any fundamental changes to the TFT.

For engineers designing circuit for AM-OLED, we recommend that all driving transistors to be maintained in CTS 2 condition at all time to minimize electrical

degradation. Also it is recommended that the a-Si:H TFT's ΔV_T to be less than 3 V during the operation of the AM-OLED's. Such ΔV_T is expected to produce ΔI_{OLED} of 5.8 % for I_{OLED}=0.1 μA to 7.3 % for I_{OLED}=4 μA, which is acceptable for many display applications. In order for the AM-OLED to be fully commercialized, much work is needed to optimize its packaging, circuit design, and OLED performance. It is unclear when this technology will, if possible, replace AM-LCD as the dominant FPD. However, we have shown that the multi-layer a-Si:H TFT technology presented in this work is capable, both in terms of electrical performance and stability, of being used as the driving electronic for such display.

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Chapter 7

Summary and Recommendation for Future Work

7.1. Summary

In this dissertation, we introduce the a-Si:H TFT with the advanced multi-layer structure. This transistor consists of a specially tailored channel region that was designed specifically to meet the needs of the commercial production of flat-panel displays. Through a series of thorough investigation we have shown that our a-Si:H TFT exhibits a comparable electrical performance as those deposited at lower rates, and can be fabricated in short amount of time because of the rapid deposition of the PECVD films. A detailed fabrication procedure for this TFT has been presented. For the tailoring of the amorphous silicon and silicon nitride films along the channel of the transistor, we show that the low-deposition-rate amorphous silicon film can be as thin as 300 Å for the TFT to exhibit a field-effect mobility of 0.93 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage of 1 V, and subthreshold swing of 0.51 V/dec. Reducing this film below 300 Å degrades the field-effect mobility and subthreshold swing, while increasing it beyond this thickness raises the transistor contact resistance without improving its electrical properties. This demonstrates the fact that the fabrication of high performance a-Si:H TFTs can be achieved without compromising the display production throughput. Only the PECVD films near the a-Si:H/a-SiN_X:H interface need to possess high electronic quality for the

TFT to exhibit high field-effect mobility and low threshold voltage. By using the multi-layer structure, we can fabricate transistors with comparable electrical performance as those made with single layer structure, yet decreasing the PECVD deposition time by 40%.

We have studied the effects of the back channel etching depth and etchant on the electrical performance of our a-Si:H TFT. It is necessary to etch approximately 800 Å of the a-Si:H film in the back channel to reduce the off-current to an acceptable value. The remaining a-Si:H film in the channel region can be as thin as 800 Å without the TFT suffering any electrical degradation. Dry etchant such as $HBr+Cl_2$ should be used for the back channel etch process, because it shows a high selectivity over the gate insulator, a high anisotropy, acceptable selectivity between n+ a-Si:H and a-Si:H (~1.7:1), and most importantly, does not degrade the electrical performance of the TFT. Another novel transistor structure, the recess contact TFT, has been introduced. The recess contact TFT has an order of magnitude lower off-current than the conventional TFT, while maintaining similar electrical performance in the on-region of operation. By replacing the conventional TFTs in a pixel electrode circuit of a flat-panel display with the recess contact TFTs, the switching transistor's off current will be decreased, while the driving transistor's on current will be unaffected. Additionally, the reduction in gate and S/D overlap could also reduce the TFT's parasitic capacitance, thus minimizing the error voltage of a high-resolution display.

Lastly, we present the high temperature electrical performance and stability mechanisms of the a-Si:H TFT with the advanced multi-layer structure. The mobility activation energy values in the linear and saturation regions of operation are 81.1 and

87.5 meV, respectively. The drain current activation energy decreases from 120 to 75 meV as the gate bias increases from 0 to 20 V. These values are comparable to the traditional transistor's activation energy values, which means that the electronic qualities of our a-Si:H TFT is similar to those deposited using the single step process. Based on our investigation of the TFT's high-temperature electrical stability, we have established that the main cause of threshold voltage degradation for this transistor structure is the presence of high electric field across the gate insulator. Under a continuous current stress of 5.5 μA for 10,000 s at 353 K, the a-Si:H TFT (W/L=24/6) with the tailored channel suffers less than 4 V of threshold voltage shift. This work demonstrates that the multi-layer TFT presented in this work is stable enough to be used in the pixel electrode circuit of future AM-OLEDs.

7.2. Recommendation for Future Work

In order to further improve the proposed transistor structure, the thickness of the low-deposition-rate amorphous silicon nitride film can be varied to study its impact on the TFT electrical performance and stability. We have fabricated devices with 500 Å of the aforementioned a-SiN_X:H film for this work, yet it is possible that other thicknesses can produce transistors with better electrical characteristics and/or faster production throughput. For the present work, amorphous silicon has been the material of choice for the fabrication of TFT. To further improve the transistor's performance, future researchers can consider using silicon-germanium alloys just for the active material in the channel region of the TFT, or throughout the entire thin-film. For crystalline MOSFET, it has been shown that the addition of germanium to silicon can improve the transistor's

mobility. Amorphous silicon-germanium technology has already been included in the fabrication of photo-detector to improve its performance, and we expect that the TFT made with such alloy can have superior electrical performance than the pure amorphous silicon TFT.

It would be interesting to investigate the dynamic electrical behavior of the a-Si:H TFT with recess contacts. Presumably, the reduction of gate-to-drain and gate-to-source overlap caused by the recess etch process should reduce the parasitic capacitance during the dynamic operation of the amorphous silicon transistor. Such reduction decreases the distortion voltage of high-resolution FPDs. Lastly, we recommend future researchers to investigate the impact of the a-Si:H and a-SiN_X:H film thicknesses on the TFT's electrical stability.