HIGH FREQUENCY MIS-BASED III-NITRIDE TRANSISTOR AND INTEGRATED BIO-SENSOR TECHNOLOGY

by

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To my daughter, Yeonjung

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CHAPTER 1
Introduction

1.1 Motivation

This thesis focuses on microwave semiconductor technology based on group III-Nitride compound semiconductor materials and integrated bio-sensor components. Microwave integrated device technology has been regarded as a key technology due to largely expanded applications and rapid progress in microwave device fabrication techniques. There are two fast growing applications of the microwave integrated technology; communication and sensor applications. III – Nitride technology is highly beneficial to both applications, due to its inherent material characteristics. III-Nitrides and their alloys such as GaN, AlN, AlGaN and InGaN are wide-bandgap semiconductor materials permitting the realization of high power and high frequency components, which are attractive for developing future microwave and millimeterwave systems for communications. Furthermore, III-Nitride materials have a number of specific properties not commonly found in conventional semiconductor materials such as silicon, GaAs and InP. They are high mechanical, thermal and chemical stability, the possibility of high temperature operation, and almost complete optical transparency in the infrared and visible spectral range [1-1]. These highly beneficial characteristics are suitable for chemical and bio-sensor applications.

This work addresses III-Nitride semiconductor with emphasis on Metal-Insulator-

Semiconductor (MIS) structures and in particular the AlN/GaN heterojunction system, as well as, integrated sensor technology for permittivity characterization of liquids and cell suspensions in microwave frequencies. The final aim of the work is the integration of microwave semiconductors and sensors based on III-Nitride technology. III-Nitrides materials are ideally suited for biological studies due to their biocompatibility and chemical inertness, their high sensitivity in charge sensing, as well as, the possibility of integration of light sources necessary for monitoring biological processes. Thus studies of thus type could lead in the development of new generations of lab on the chip components.

1.2 III-Nitride Compound Semiconductor Technology

Since the early 1970s, research of Gallium Nitride (GaN) based materials and semiconductor devices have been intensively pursued, because GaN's inherent advantageous characteristics are attractive in the area of high power, high frequency applications. The major GaN's features are high breakdown voltage, high saturation and peak carrier velocity, good thermal conductivity, low dielectric constant, high melting point and direct bandgap. These physical properties permit the use of GaN for high power and frequency applications, as well as use in applications requiring high temperature tolerance. Other applications include blue and green light emission. Therefore, the GaN material system has a very wide range of electronic and optoelectronic application examples of which are depicted in Fig. 1.1.

In terms of wireless communication applications like 3G or future 4G mobile network infrastructure, there are growing demands for improvements in microwave

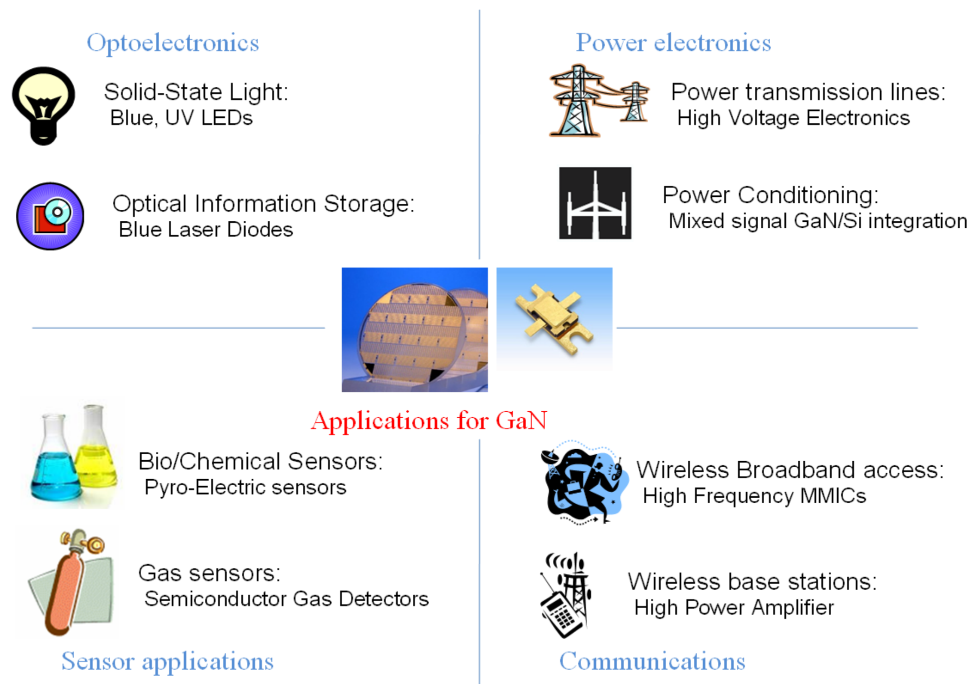


Figure 1-1: Examples of applications for GaN

power amplifier performance. Voice and non-voice communication like video telephone requires high data rate and therefore high performance base station power amplifiers are one of the key components. There are four major demands for base station power amplifiers; high power, which defines base station coverage, high efficiency, which defines operating cost, high robustness, which defines maintenance cost and lastly high linearity which defines network capacity. Current silicon-based Lateral Double-diffused MOSFET (LDMOS) power device technology has a limitation of output power handling due to the device's breakdown voltage and frequency limit due to inherent Si material properties. Even though high power LDMOS arrowed operation up to 3.5 GHz for WiMAX applications, a major breakthrough is still required leading a regime of higher frequency and higher power applications [1-2].

Material	**Bandgap (eV)**	**Electron Mobility (cm^2/Vs)**	**Hole Mobility (cm^2/Vs)**	**Drift Velocity ($\times 10^7$ cm/s)**	**Breakdown Field (MV/cm)**	**Dielectric constant (ε_0)**
AlN	6.2	135	14	1.4	4 - 12	8.5
GaN	3.44	300 – 1000	< 200	2.5	5.0	10.4 (∥) 9.5 (⊥)
InN	0.8-0.9	1000 - 1900		2.5	5.0	15.3
6H SiC	3.03	400	50	2.0	3 – 5	10.3 (∥) 9.66 (⊥)
4H SiC	3.23	900	100	2.0	3 – 5	10.3(∥) 9.66 (⊥)
Si	1.12	1500	450	1.0	0.3	11.8
GaAs	1.42	8500	400	1.0	0.4	13.1

Table 1-1: Electronic Properties of III-Nitride material with Si, GaAs and SiC material [1-3] ∥: longitudinal, ⊥ transverse

As a strong counterpart in compound semiconductor technology, GaN is a material suitable for developing 4H (High power, High efficiency, High robustness and High Linearity) base station power amplifiers due to its superior electronic properties. Table 1.1 lists the electronic properties of III-Nitrides and compares them with other semiconductor materials.

GaN is referred to as wide bandgap semiconductor material, since it has a large 3.44 eV band gap and one order of magnitude higher breakdown field than GaAs or Si. Bulk GaN has a relatively low electron and hole mobility compared to Si or GaAs. However, GaN heterostructure formed based on it i.e. AlGaN/GaN demonstrates higher electron mobility (~ 1600 cm^2/Vs) due to the presence of a Two-Dimensional Electron Gas (2DEG) channel. Moreover, the piezoelectric and spontaneous polarization effects result in a high density 2DEG at the AlGaN/GaN heterointerface. Electron sheet concentration

of the order of 1.3×10^{13} cm^{-3} (more than 3 times higher than the sheet concentrations are usually obtained in AlGaAs/GaAs or AlInAs/InGaAs heterostructures) are easily formed with such heterostructures. Therefore GaN-based heterostructure systems like AlGaN/GaN or AlN/GaN permit device realization with high current capacity. By combing the high voltage capability from the high breakdown field and high current density from the high 2DEG electron density, GaN-based heterostructure semiconductors permit one to obtain higher power density than conventional semiconductor devices. GaN allows in fact obtaining the highest power density reported up to now among semiconductor materials. The state of the art GaN-based Heterostructure Field Effect Transistors (HFETs) shows more than 6 times higher power density than same size transistors i.e. LDMOS [1-1].

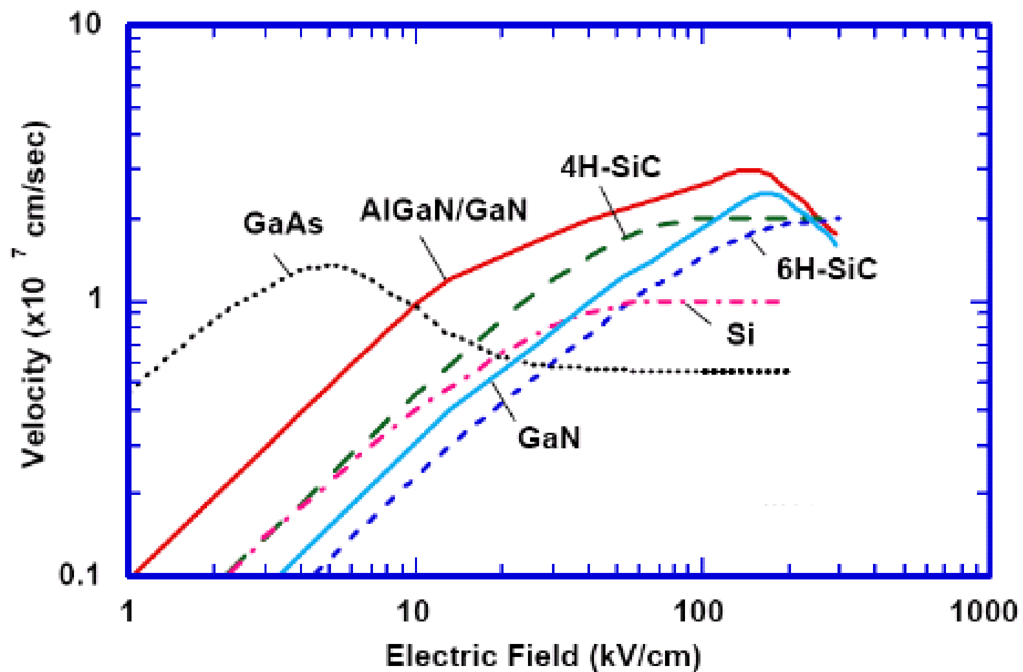


Figure 1-2: Electron velocity versus electric field characteristics for various semiconductor materials [1-4]

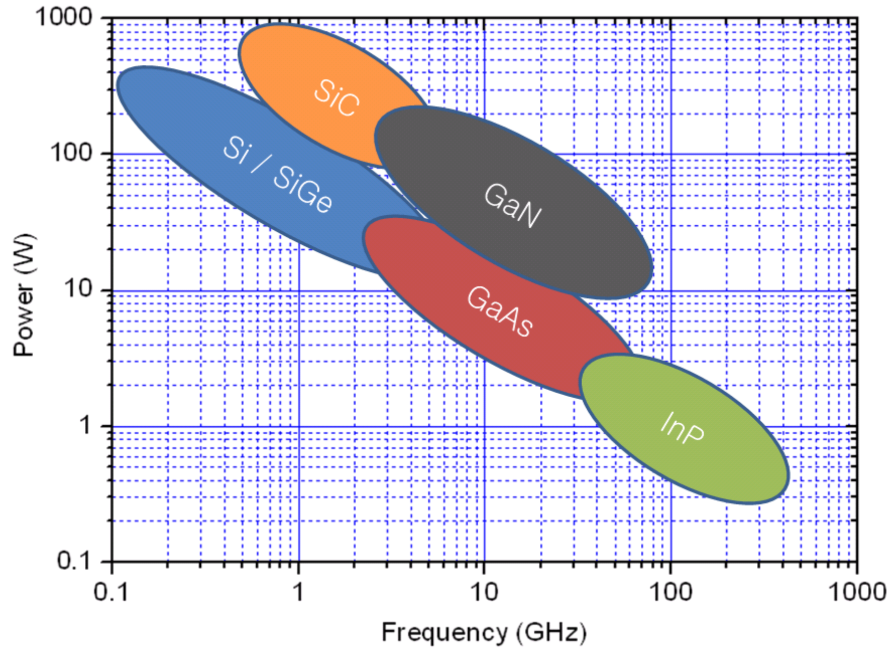


Figure 1-3: Power and frequency regions for GaN and other materials for electronic devices

For high frequency operation of microwave devices, saturated drift velocity (ν_{SAT}) is an important property because the velocity of carriers in the high electric field region is governed by ν_{SAT}. The ν_{SAT} of bulk GaN from recently published experimental results has a value of 1.4×10^7 cm/s [1-5], which is higher than that of Si (1×10^7 cm/s) and two times as high as for bulk GaAs (0.74×10^7 cm/s) [1-6]. As can be seen in Fig. 1.2, AlGaN/GaN heterostructures have even higher saturation velocity (about 3×10^7 cm/s) because of the higher 2DEG electron velocity.

Overall, GaN covers a wide region in the power versus frequency diagram of Fig. 1.3 and it can be used in the 1~ 100 GHz range of frequencies allowing one to obtain 10 ~ 100 Watt power. Though recent SiGe based electronics overcome the frequency barrier which has been believed to be a limit of Silicon, GaN has principal advantages in terms of high power in the same range of frequencies.

Nevertheless, GaN technology is not fully matured in terms of material growth, device fabrication and circuit implementation, since it is relatively new compared with other semiconductor technologies. No bulk substrates of GaN have, for example, been produced so far in commercially viable size (diameter > 25 mm) and with reasonable cost. Therefore, GaN crystals have to be epitaxially grown as a thin film on foreign substrate materials such as Sapphire, SiC and Silicon by Metal Organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxy (MBE) growth techniques. As a result, the physical properties of the GaN crystal structure and device characteristics are limited by mismatch between GaN and the substrate material. Sapphire has been the major choice for GaN growth because of its high crystal quality, high melting point and relatively low cost. However, the high lattice mismatch of GaN based materials with respect to it, and the low thermal conductivity limit the device performance as can be seen in Table 1.2. Lattice mismatch induces high defect densities possibly reducing breakdown voltage as well as, limiting power and heat dissipation through the sapphire substrate due to its low thermal conductivity.

On the contrary, SiC substrate acts as a good heat sink and GaN grown on SiC has lower defect density. However, it is less cost effective and its size is limited to diameter of 50 mm. In terms of cost, Si substrates are the best option because large substrate size at very low price is available. At the same time Si substrates permit easy integration of GaN technology with commercially matured Si based technology. However the lattice and thermal mismatch of Si substrate are more severe than those of sapphire and SiC. Based on growth techniques such as the use of superlattice and multi-temperature buffer layer, companies like Nitronex were able to produce advanced GaN on Silicon wafers. Recently

Substrate	Lattice constant (Å)	Thermal conductivity (W/cm K)	Thermal expansion coefficient	Lattice mismatch (%)
GaN	3.189	1.3	5.59	0
AlN	3.112	3.0	4.2	2.4
6H-SiC	3.080	4.9	4.2	3.4
Sapphire	2.747	0.5	7.5	13.9
Si	5.430	1.5	-3.6	-70.3
GaAs	5.653	0.5	6.0	-74.4

Table 1-2: Physical Properties of GaN Material Growth Substrate [1-8]

reported 35 mm GaN on Si HFET devices produced 368W at 60 V with 70 % drain efficiency at the frequency of 2.14 GHz [1-7].

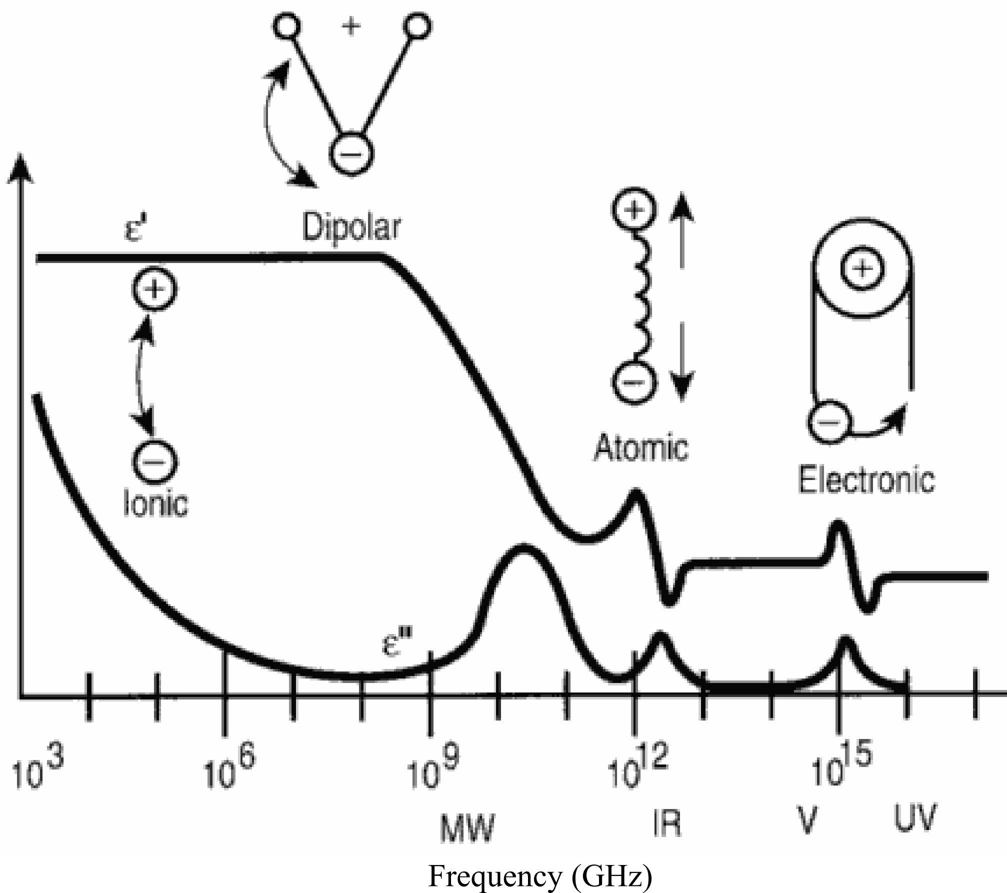
In this work, most of the GaN layers were grown on sapphire substrate since it is appropriate for research purposes and allows easy evaluation of new device structure designs due to its wide availability and low cost. After evaluation of sapphire based technologies, this approach can be easily transferred to higher performance SiC substrates.

1.3 CPW Sensors for Permittivity Measurements

Dielectric spectroscopy is a powerful tool to characterize liquids or biological samples in electro-magnetic (EM) fields. The response of a dielectric material in EM fields can be described by the complex permittivity and it is as follows.

$$\varepsilon = \varepsilon' + j\varepsilon'' \tag{1.1}$$

where ε is the complex permittivity, ε' is the real part of the complex permittivity and ε'' is the imaginary part of the relative complex permittivity. The permittivity is a physical quantity that describes how an electric field affects and is affected by a dielectric medium. It is determined by the ability of a material to polarize in response to the EM-field, and therefore reduce the total electric field inside the material. Thus, permittivity relates to a material's ability to transmit an electric field [1-9], [1-10].



Frequency (GHz)

Figure 1-4: A dielectric permittivity spectrum over a wide range of frequencies [1-10]

As can be seen in Fig. 1-4, the complex permittivity are related with various polarization processes; ionic and dipolar relaxation, and atomic and electronic resonances at higher energies [1-10]. In the frequency range of interest (1 ~ 40 GHz), the major dielectric effect is dipolar relaxation. In the application of biological samples such as cells or tissues, the frequency dependent dielectric permittivity can provide valuable information on bio-molecular properties including cell structure, orientation of molecular dipoles, surface conductance, and membrane processes [1-11].

Of many available measurement techniques, the open-ended coaxial probe approach is most commonly used for complex permittivity measurements in biological applications due to its ease of use and non-destructive nature [1-12]. However, this method requires relatively large sample volumes and often yields inaccurate measurement results when the specimen is heterogeneous, which is often the case for biomaterials [1-13]. As an alternative, planar-type sensors utilizing microstrip lines or coplanar waveguides (CPW) were proposed for permittivity measurements of biomaterials at microwave frequencies. A planar geometry permits integration of the sensor with micro-fabricated fluidic wells or with microfluidic networks to drastically reduce volume requirements for what are often expensive and/or low-abundance samples. Moreover, these planar devices can be fabricated using standard photolithography, deposition and etching techniques that enable precise control of sensor geometry at low cost [1-14], [1-15]. Finally, the extended nature of these waveguide sensors inherently average out any inhomogeneity in the sample, which is often the case for biomaterials [1-13].

Coplanar waveguides (CPWs) are a good choice for a planar device intended for high-frequency spectroscopic measurements since the lack of a backside ground-plane

minimizes fabrication complexity and maximizes interaction of the waveguide mode with the test media. CPW-based microwave permittivity sensors were firstly proposed by Stuchly *et al.* [1-16]. Facer *et al.* [1-17] measured several biological samples including a cell suspension using CPW sensors bonded to a polydimethylsiloxane microfluidic network over the frequency range of 40 Hz to 26.2 GHz. However, only transmission spectra, without any complex permittivity calculations, were presented at frequencies beyond 45 MHz. Raj *et al* [1-13] proposed a transmission matrix (ABCD matrix) based de-embedding method for calculating liquid permittivity from measured S-parameters, and presented accurate permittivity measurements of reference liquids up to 4.5 GHz. Recently, J. Mateu *et al.* [1-18] used a CPW sensor integrated with a microfluidic network to extract the complex permittivity of an aqueous suspension of polystyrene latex beads up to 40 GHz.

While significant progress has been made using CPW sensors to extract the frequency-dependent dielectric permittivity of liquids and bio-substances there is no report on the measurement and extraction of the complex permittivity at microwave frequencies of biological specimens such as cell suspensions using coplanar sensors. In Chapter 9, the fabrication of coplanar sensors with an SU-8 container and a rapid de-embedding method is described. The performance of the fabricated coplanar sensor is verified by reference liquid measurements, and subsequently the complex permittivity of a cell suspension is reported together with a study of the impact of a known cytotoxic chemical on the cell suspension permittivity over the time.

1.4 Overview of Dissertation

In the following chapters, high frequency III-Nitride Metal Insulator Semiconductor

Field Effect Transistors (MISFETs) are designed, simulated, fabricated and measured. The focuses are on AlN/GaN MISFETs and *in-situ* Si_3N_4/AlN/GaN MISFETs. The work on AlGaN/GaN HEMTs technologies are referenced and compared, since AlGaN/GaN HEMT technology is matured and is the basis of developing III-Nitride MISFET technology.

In chapter 2, basic properties of the III-Nitride MISFETs and AlGaN/GaN HEMTs are reviewed. The intrinsic properties of AlN/GaN heterostructure; spontaneous and piezoelectric polarization are investigated. The potential and challenges of AlN/GaN MISFETs are addressed and the *in-situ* deposition of Si_3N_4 for improving AlN/GaN MISFETs is discussed. Chapter 3 discusses the results obtained from simulation of GaN HEMTs. Using the MEDICI and ISE TCAD programs, drift diffusion-based simulations were performed that account for the physical properties of devices such as III-Nitride based HEMTs, double heterostructure HEMTs and MISFETs. The results were then used to optimize the device design. Chapter 4 explains the technologies developed for fabricating the III-Nitride MISFETs and HEMTs of this work. The challenges and process optimization of ohmic contacts for AlN/GaN MISFETs are fully examined. The fabricated III-Nitride MISFETs are characterized using several measurement techniques such as DC, pulsed IV, S-parameter and large signal. The measurement results and discussions are given in chapter 5. Based on the small and large signal measurement data, small and large-signal models were developed for AlN/GaN MISFETs and the data obtained were used for extracting the device physical parameter. Chapter 6 discusses small and large signal modeling of AlN/GaN MISFETs using non-linear optimization techniques. A wideband balanced low noise amplifier with AlGaN/GaN HEMTs is

described in chapter 7 as possible circuit application of the developed technology. Other applications include diodes using III-Nitride heterostructures, AlGaN/GaN superlattice diodes were designed, fabricated and characterized for this purpose and reported in chapter 8. Chapter 9 addresses another possibility for integrated technology involving a Coplanar Waveguide (CPW) line fabricated in the bottom of an SU-8 based liquid container. Complex permittivity measurements of liquids and living cell suspensions were performed based on this approach and are presented in this chapter. Finally, chapter 10 summarizes the accomplishments of this work and presents suggestions for future work.

CHAPTER 2
Theory of III-Nitride HFETs

In this chapter, the basic properties and design issues of AlN/GaN MISFETs and AlGaN/GaN HEMTs are reviewed. The basic concept and design of III-Nitride MISFETs and HEMTs are exactly same except for the gate insulating layer; HEMTs use AlGaN and MISFETs use AlN. Ideally AlN/GaN MISFETs should have better performance in terms of power and frequency due to their higher 2DEG density resulting from the higher polarization field, better carrier confinement associated with the higher conduction band discontinuity and higher transconductance due to the thin barrier layer. However, because of the growth and fabrication technology difficulties, AlN/GaN MISFETs have not fully utilized the advantages of inherent AlN/GaN heterostructure properties. However, with the help of *in-situ* deposited Si_3N_4 in the same growth chamber which was used for AlN/GaN growth, The performance of AlN/GaN MISFETs can be drastically improved and the fabrication process for high quality ohmic contact becomes simpler. In the following sections, the operation principles of III-Nitrides MISFETs and HEMTs are investigated and 2DEG, induced by spontaneous and piezoelectric polarization effects, are reviewed. Then, *in-situ* Si_3N_4 on III-Nitride MISFETs is discussed.

2.1 III-Nitride HFET Characteristics

Most of the reported state of the art results of GaN-based semiconductor devices are

from AlGaN/GaN High Electron Mobility Transistors (HEMTs). These are also often referred to as Modulation Doped Field Effect Transistors (MODFETs). The unique feature of HEMT is its heterostructure in which a wider energy bandgap material (i.e. doped or undoped AlGaAs or AlGaN) is grown on top of an undoped narrower bandgap material (i.e. GaAs or GaN) allowing carriers to diffuse and form a channel. Also due to this modulation doping, carriers in the undoped heterointerface are spatially separated from the doped region and have extremely high mobility since impurity scattering is absent. The carriers in the heterointerface form a two dimensional electron gas (2DEG) since they are confined two-dimensionally and are quantized as sheet carrier density. The idea of modulation doping was simultaneously proposed at Thomson-CSF, Bell Laboratories and Fujitsu in the late 1970s [2-1].

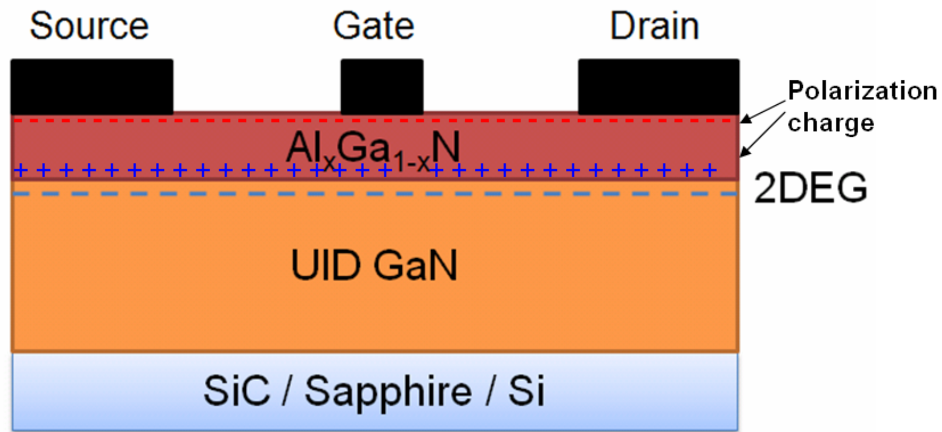
Although the fundamentals of GaN based HEMTs are not different from the conventional III-V based HEMTs, GaN based HEMTs have distinct properties such as the origin of 2DEG: spontaneous and piezoelectric polarization induced 2DEG [2-2]. In fact, due to the piezoelectric and spontaneous polarization, AlGaN/GaN HEMTs are able to achieve a 2DEG with sheet carrier concentrations of up to ~ 2×10^{13} cm^{-2} close to the interface, which exceeds that observed in other III-V material systems. These high sheet carrier concentrations can be obtained even without intentionally doping the barrier [2-3]. This effect is much more pronounced in GaN based heterostructures when grown on the c-plane than in the case of conventional III-V materials. Practically, in AlGaN-based transistors, the piezoelectric polarization of the top layer is more than five times larger than in analogous AlGaAs structures. Furthermore, according to Bernaldini et al. [2-4], a very large spontaneous polarization charge also exists which must be taken into account

in the calculations of the sheet carrier concentration and carefully considered in device design and analysis.

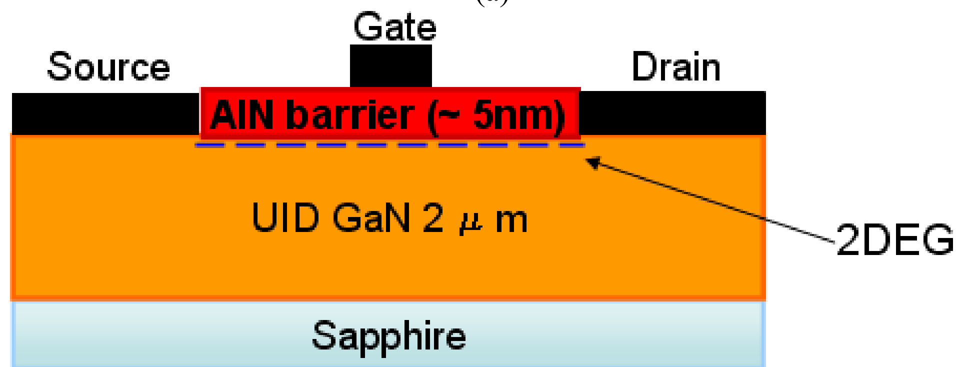
2.1.1 Spontaneous and piezoelectric polarizations

The origin of the 2DEG is spontaneous and piezoelectric polarization in the case of the AlGaN/GaN heterostructure. Because of the two distinct polarization mechanisms, 2DEG sheet carrier concentrations of 10^{13} cm^{-2} or higher can be achieved even without intentional doping. Spontaneous polarization is polarization on heterojunction interface at zero strain, which results from net charge of the growth front. Piezoelectric polarization results from the difference between lattice constants at the heterostructure, and thus increases as the strain at the interface increases.

These two polarization effects are quite important in nitride-based HFETs. Fig. 2.1 shows device structure of the AlGaN/GaN HEMTs and the AlN/GaN MISFETs with the locations of 2DEG and polarization charge. The energy band profiles for the HEMTs are depicted in Fig. 2.2. The difference in piezoelectric and spontaneous polarization between AlGaN and GaN layer determines a fixed 2-D charge density at the interface between the two materials. Polarization difference induces a positive charge at the interface and electrons are attracted by this positive charge. The electrons accumulate at the interface and form a conductive channel. The high electric field induced by the interface charge help to form a large channel carrier density and a strong channel confinement. Moreover, the strong electric field compensates the space charge contribution coming from the ionized donors.

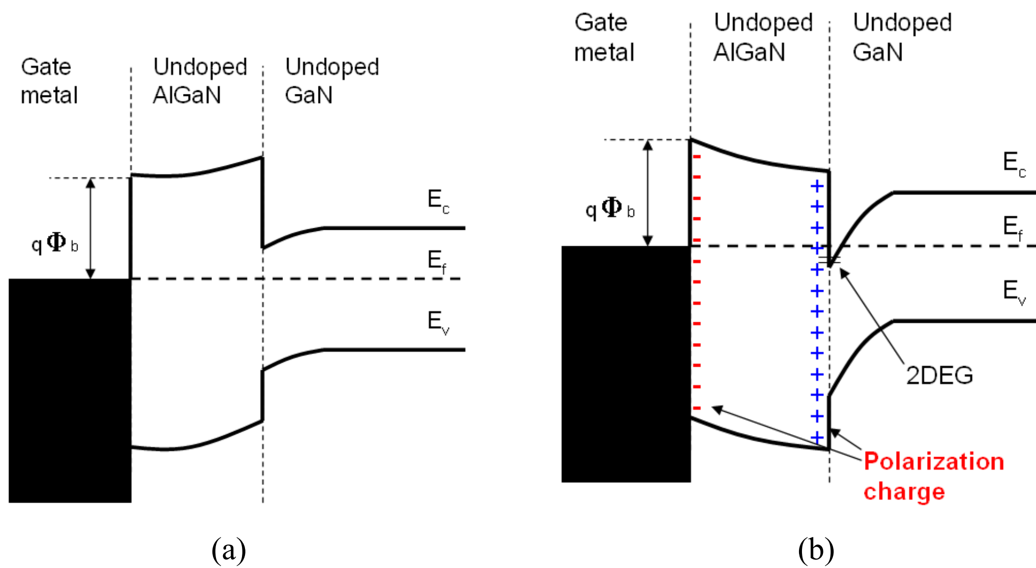


(a)



(b)

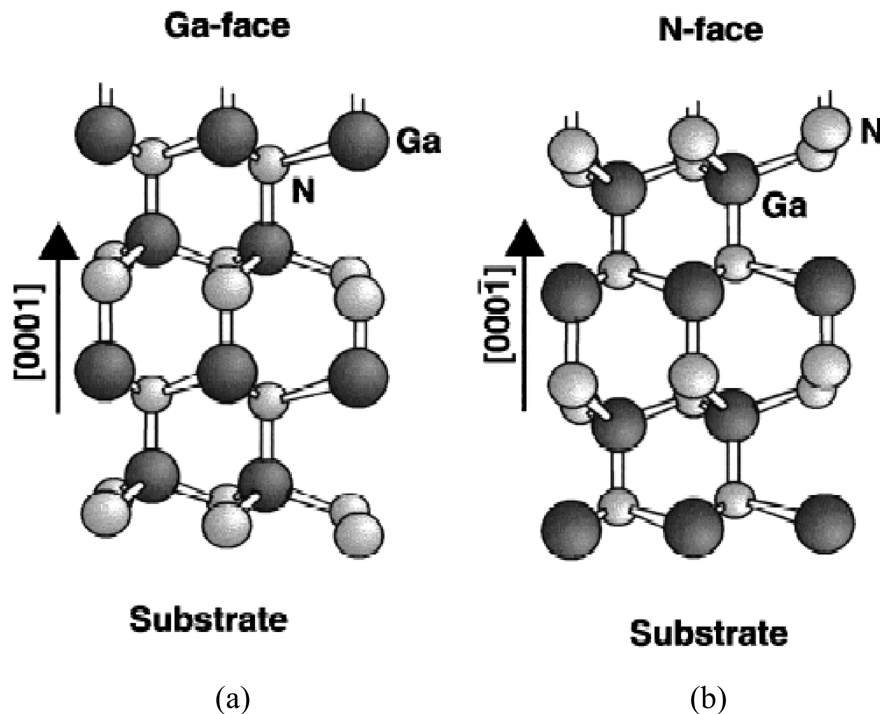
Figure 2-1: Layer structure of (a) AlGaN/GaN HEMTs and (b) AlN/GaN MISFETs



(a) (b)

Figure 2-2: Conduction and valence band profile of AlGaN/GaN HEMTs (a) without polarization charge and (b) with polarization charge

The device characteristics are to a great extent decided by the surface termination of the heterostructure. GaN grown on sapphire forms a hexagonal wurtzite structure. Along the common growth direction of [0001] or [000-1], atoms are arranged in bilayers. These bilayers are comprised of two closely spaced hexagonal layers, one formed by cations (Ga atoms) and the other formed by anions (N atoms). If the surface has [0001] polarity, the top position of the {0001} has only Ga atoms and is referred to as Ga-face. In contrast, [000-1] polarity has only N at the surface and is referred to as N-face. Ga-face and N-face surfaces of GaN are nonequivalent and different chemically and physically. [2-5]. AlGaN/GaN grown on sapphire by MOCVD is always Ga-faced, but material grown by MBE can have either Ga- or N-faced surface depending on the existence of a AIN nucleation layer.



(a) (b)

Figure 2-3: Schematic drawing of the crystal structure of (a) wurtzite Ga-face and (b) N-face GaN [2-5]

As mentioned earlier, the total macroscopic polarization of GaN or AlGaN layer is the summation of the spontaneous polarization and the piezoelectric polarization. Therefore, if the polarizations are in opposite direction, polarization effect can be reduced. In case of Ga-face, the spontaneous polarization is pointing towards the substrate. In contrast, the spontaneous polarization of N-faced AlGaN/GaN heterostructure points to opposite direction. The piezoelectric polarization changes direction depending on the strain; negative for tensile and positive for compressive strained barriers. In order to get high confinement of carrier at the 2DEG, two polarization directions should be same. Thus, compressive strain, GaN layer is above AlGaN layer, is not adequate for the HEMT operation. In case of the Ga-face, compressive strain; GaN deposited over AlGaN, results in minus sheet charge which attract holes at the interface, and the tensile strain; AlGaN grown over GaN, induces positive sheet charge which attracts electrons. In order to form large sheet carrier concentration 2DEG at the interface, the tensile strain is need to the Ga-face, and compressed strain is required to the N-face. Normally, Ga-faced and AlGaN deposited over GaN AlGaN/GaN HEMTs are favorable in AlGaN/GaN HEMTs

2.1.2 Properties of AlN/GaN MISFETs

The first demonstration of AlGaN/GaN HEMT was made in 1993 by Khan et al.[2-6]. After more than 10 years of intensive GaN device developments, recent GaN HEMTs demonstrated a very high cut off frequency (f_T = 181 GHz) [2-7], as well as very high power density of 30 W/mm at 4 GHz [2-8] and 10W/mm at 40 GHz [2-9]. These power results showed more than 3 times higher power density than that of the state of the art AlGaAs/GaAs HEMTs. In spite of these achievements, there is still room for improving

the high frequency performance. Decreasing only the gate length for higher frequency operation does not present any significant advantage below 100 nm because of the low aspect ratio of the gate length and barrier thickness. Therefore, the gate length and the barrier thickness should be decreased at the same time. However, decreasing the barrier thickness of AlGaN/GaN HEMTs results in a decrease of two dimensional electron gas (2DEG) density due to effects such as proximity of the heterointerface to the negatively charged surface and/or defects [2-10]. In order to solve this problem, a thin AlGaN barrier layer with higher Al composition or even an AlN barrier layer can be used. The higher polarization effect resulting from the Al rich barrier layer can compensate the decrease of 2DEG density caused by barrier thinning. Moreover, the presence of a wide bandgap (6.2 eV) AlN layer will contribute in reducing the gate leakage. Furthermore, the AlN barrier layer allows transport without alloy scattering and can enhance the transconductance (g_m), as well as, decrease the short-channel effects. Therefore AlN/GaN Metal Insulator Semiconductor FETs (MISFETs) can be an ideal device approach for high frequency GaN based HFETs.

Fig. 2.4 shows the theoretically calculated spontaneous, piezoelectric, total polarization at the lower interface of a Ga-face AlGaN/GaN heterostructure as a function of the alloy composition of the barrier. It is evident that increasing the Al composition improves the sheet carrier density of the 2DEG. However an increase of Al composition results in the reduction of the carrier mobility because of several effects; intersubband scattering, increasing alloy disordering in AlGaN, increasing density of interface charges, and larger potential fluctuation due to the surface interface [2-4].

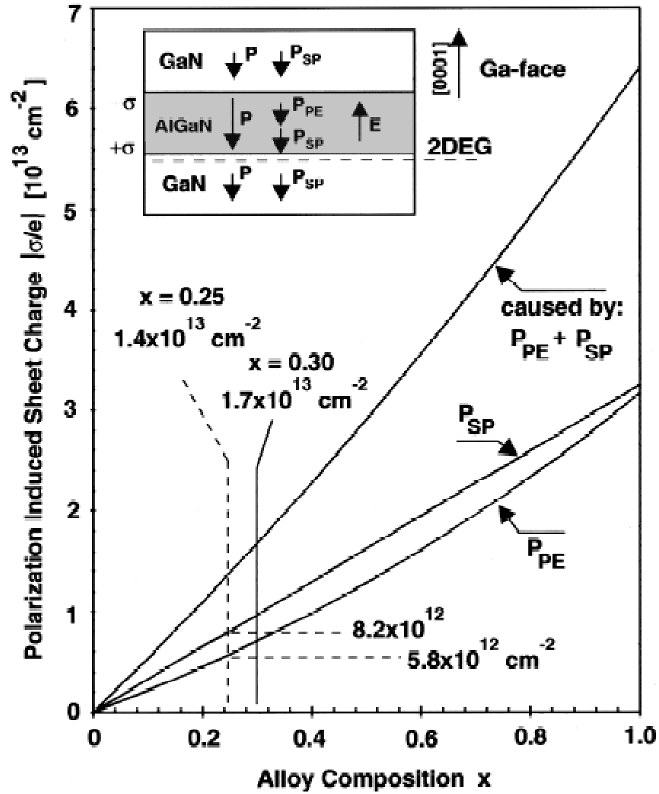


Figure 2-4: Calculated sheet charge density caused by spontaneous and piezoelectric polarization at the lower interface of Ga-face GaN/AlGaN/GaN heterostructure vs. alloy composition of the barrier [2-4]

Since the first fabrication of AlN/GaN MISFET [2-11], few results were reported [2-12]-[2-14] because of the difficulty in producing high quality AlN layers and AlN/GaN heterointerface, as necessary for such devices. An additional difficulty is imposed by the realization of good ohmic contacts in the presence of the AlN barrier layer. Due to the large lattice constant difference between AlN and GaN layers, it is difficult to obtain a high quality AlN layer on top of the GaN layer and if the thickness of the AlN layer exceeds 9 ~ 10 nm, cracks and defects are often observed on the AlN layer. Therefore great care must be taken in growth of AlN. From the technology point of view, it is extremely difficult to make a good ohmic contact on AlN layer because of AlN surface

oxidation. Therefore AlN should be removed for ohmic contact formation and this makes the process more complicated. Despite this difficulty, AlN/GaN MISFETs have high potential in terms of high power and high frequency applications and growth control. As fabrication processes progress by optimization, they are expected to lead in breakthrough in III-Nitride based FET technology. This thesis addresses the promising family of AlN/GaN MISFET devices by presenting a comprehensive study, which includes physical simulation, growth of high quality AlN/GaN device structures, processing and experimental demonstration of DC, power and high-frequency characteristics.

2.1.3 *In-situ* MOCVD deposited Si_3N_4/AlN/GaN MISFETs

As explained in the section 2.1.2, AlN/GaN Metal Insulator Semiconductor Field Effect Transistors (MISFETs) are attractive for high frequency and high power GaN-based HFETs applications. This is due to their wide bandgap and large polarization charge of the AlN/GaN heterostructure, which result in high carrier density even for very thin (3 ~ 5 nm) barrier. Although promising results were recently reported on AlN/GaN MISFETs [2-15],[2-16], there is still room for improvement of their characteristics. Studies of their large-signal properties as those reported in the thesis are also needed. In this work, the improvement of AlN/GaN MISFETs' DC and high frequency characteristics could be achieved with *in-situ* deposited Si_3N_4 by the same MOCVD system as the one used for growth of the MISFET epitaxial layers. Surface passivation plays an important role in AlN/GaN MISFETs, since the AlN layer can be rapidly oxidized and surface states can easily deplete the 2DEG due to the presence of the rather thin AlN layer. *In-situ* MOCVD deposition of Si_3N_4 passivation layer prevents surface

oxidation and/or contamination by air exposure and subsequent fabrication processes. The AlN surface is protected in this case right upon growth and is not therefore directly exposed to the atmosphere. Thus the formation of surface states can be drastically reduced leading in improvement of device characteristics. The layer structure of *in-situ* Si_3N_4/AlN/GaN MISFETs is shown in Fig. 2.5.

AlGaN/GaN HEMTs generally suffer from DC-to-RF dispersion, which results from the surface states or defects mentioned earlier. The traps induced by surface states or defects on the semiconductor surface have slow response time for trapping and de-trapping of the electrons. As a result, the high-frequency characteristics of the AlGaN/GaN HEMTs are not as good as those predicted by DC performance and the so called DC-to-RF dispersion is observed. The dispersion can be significantly reduced by passivating the surface with plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 [2-17]. Normally the PECVD Si_3N_4 deposition is done after ohmic formation or gate deposition. As a result, dispersion depends on the Si_3N_4 deposition conditions and surface

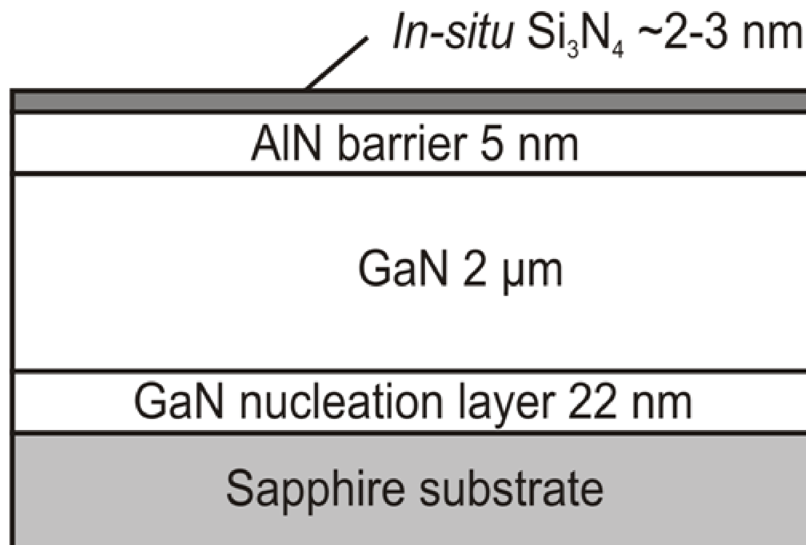


Figure 2-5: Layer structures of *in-situ* Si_3N_4/AlN/GaN MISFETs

preparation before passivation [2-18]. Therefore, *in-situ* deposition of Si_3N_4 in the growth chamber right after the AlGaN growth is very advantageous, since the AlGaN surface is never exposed to the air environment and is protected throughout the fabrication process. *In-situ* Si_3N_4 on AlGaN/GaN HEMTs with MOCVD [2-19] and MBE [2-18] were reported and improvements of device characteristics were shown.

In case of AlN/GaN MISFETs as those studied here, the effect of *in-situ* Si_3N_4 is more promising than in case of AlGaN/GaN HEMTs. *In-situ* Si_3N_4 on AlN/GaN MISFETs reduces as in the case of AlGaN/GaN HEMTs the surface states or defects, as well as, surface contamination. Moreover, *in-situ* Si_3N_4 protects the AlN from surface oxidation, which leads in degradation of ohmic contact quality in AlN/GaN MISFETs. Using *in-situ* Si_3N_4 deposition techniques, the problem of AlN oxidation can be totally alleviated, since the AlN surface is never exposed to the air. Therefore etching of AlN is no longer necessary. Ohmic contact formation is possible directly on the top of Si_3N_4 layer, since the ohmic metal can easily penetrate through the thin (2 nm) Si_3N_4 and can form a high quality ohmic contact. Additionally, silane (SiH_4) used for Si_3N_4 growth provides silicon as a dopant to the AlN during *in-situ* Si_3N_4 growth [2-19]. The resulting silicon doping may also help to improve the ohmic contact quality on AlN. Detailed ohmic data with and without *in-situ* Si_3N_4 will be shown in chapter 4.

2.2 Summary

In this chapter, an overview of GaN-based HEMTs and MISFETs was presented with the basic properties of device operation. The origin of high 2DEG sheet carrier density in AlGaN/GaN and AlN/GaN heterostructures was shown to be related to

spontaneous and piezoelectric polarizations. Even without doping in the barrier layer, electrons can be accumulated with a high density at the heterointerface as a result of the positive sheet charge which is induced by the polarization effects. Key features of AlN/GaN heterostructure devices are higher carrier concentration, better control of the 2DEG channel and less gate leakage than conventional AlGaN/GaN HEMTs. On the contrary, AlN/GaN MISFETs demand highly controlled growth and optimization as well as more complex process. In the final section, the advantages of *in-situ* deposition of Si_3N_4 for protecting AlN surface were discussed.

CHAPTER 3
Drift-Diffusion Simulations of III-Nitride HFETs

3.1 Introduction

In order to develop advanced GaN-based semiconductor devices, a thorough study based on device physics is necessary to allow a better understanding of device operation. Simulation studies are necessary at device level for exploring new device designs and concepts. Device fabrication process and characterization need long time and can be rather costly in evaluating new concepts and optimizing performance. Device simulation offers an effective alternative method. It reduces significant time and effort in device optimization and therefore actual device fabrication runs can be minimized. In addition, the sensitivity of device characteristics to process variations can also be studied too.

There are several physical simulation tools available for semiconductor device simulation. In this study, two simulation tools were used; MEDICI and ISE TCAD. MEDICI was used for simulating AlGaN/GaN HEMTs and InGaN-based double-heterostructure HEMTs. ISE-TCAD was mainly used for simulating AlN/GaN MISFETs. Both simulators support electrical, thermal, and optical behavior of semiconductor devices. ISE TCAD supported more accurately III-Nitride material characteristics, which were not available in MEDICI at the time this work was performed. However for the device study performed in this thesis, the physics-based approach of MEDICI combined with our own developed database for GaN properties allowed one to obtain reliable data

All simulations were based on drift-diffusion modeling of the transport characteristics. The model assumes full-ionization, non-degenerate, steady-state and constant temperature. Comparing with the hydrodynamic model, which considers self-heating effects and ballistic transport of the carriers, it is much simpler and faster. Therefore, it is possible to achieve simple and clear identification of key device processes of the semiconductor device. Hydrodynamic simulation is necessary when the gate length is 100 nm or less. Drift-diffusion simulation provides highly reliable simulation results when the gate length is around 1 μm, which is the case for this study.

In section 3.2, MEDICI was used for simulating AlGaN/GaN HEMTs. A δ-doping polarization model for generating polarization charges in AlGaN/GaN HEMTs is described and the impact of gate-recess on device performance is also discussed. Finally, InGaN-based double-heterojunction HEMTs (DHEMTs) were simulated in order to find an optimum device design with better carrier confinement.

In section 3.3, ISE TCAD simulations of AlGaN/GaN HEMTs and AlN/GaN MISFETs are described. The impact of device parameters such as trap density, contact resistance and interface charge on device performance is also described. Simulated DC and AC characteristics of AlGaN/GaN HEMTs and AlN/GaN MISFETs are presented. Finally, simulation results of field-plated gate of AlGaN/GaN HEMTs are discussed.

3.2 Device Simulation for III-Nitride based HEMTs using MEDICI

III-Nitride HEMTs were designed and simulated with the MEDICI simulation program. In designing III-Nitride HEMTs, the most important considerations to be made are the presence of piezoelectric and spontaneous polarization effects, which lead in high

2DEG sheet carrier concentration density in the order of $10^{13}cm^{-2}$. Since MEDICI does not support polarization effects directly, these are modeled by inserting a δ-doped layer of high concentration near the heterojunction of the AlGaN side. This model cannot, however, fully implement the polarization effects of GaN-based HEMTs. Moreover, it does not consider the piezoelectric coefficients of the materials. In order to obtain results consistent with the experimentally reported performance of AlGaN/GaN HEMTs, the carrier density of the 2DEG was fitted in the range of 10^{13} cm^{-2} by adjusting the depth, width and concentration of δ-doping. Therefore, the profile of the δ-doping model (concentration, doping depth and width) is a key factor in correctly determining the device characteristics. In order to limit the high current flow due to the high carrier concentration at the δ-doping layer, the electron mobility of that layer was modified to much smaller values than those of other regions. As mentioned earlier, the spontaneous and piezoelectric polarizations are dependent on the surface face (Ga-faced or N-faced GaN semiconductor) and strain type (compressive or tensile). Thus, for each design, the location of 2DEG was first defined by considering the direction of polarization, and then the δ-doping layer was inserted in the AlGaN barrier layer near the 2DEG to allow consideration of the impact of the polarization effects on the carrier concentration of the 2DEG.

In section 3.2.1, the δ-doping polarization model was adjusted to obtain a carrier concentration corresponding to the experimental AlGaN/GaN HEMT data. Another consideration in the model adjustments was the conduction band profile, which should be intercepted by the Fermi level. Thus a triangular potential well should be formed at the channel region. The impact of the δ-doping concentration on device characteristics was

studied in section 3.2.2. Then in section 3.2.3, the ohmic contact properties were then adjusted in order to reproduce the experimental device characteristics. In section 3.2.4, design variations on the HEMT structure such as the use of a double-heterostructure and InGaN channel were simulated based on extracted physical parameters in order to optimize the GaN-based HEMT design.

3.2.1 Recessed gate single-heterojunction HEMTs

A Single-heterostructure High Electron Mobility Transistor (SHEMT) with recessed gate was simulated and the simulation results are presented in this section. The material parameters were the same as in [3-4]. However, because of difficulty in accurately accounting for all polarization effects, some of the parameters were modified to ensure that the predicted characteristics correspond well to those expected for III-Nitride HEMTs. Table 3.1 shows the thickness, doping level and material composition of the SHEMT. The gate length was 0.2 μm and the separation between source and drain was 0.6 μm. The Al mole fraction x in the $Al_xGa_{1-x}N$ layer was 0.15 instead of the original design value of 0.26 specified in the thesis. As mentioned earlier, in order to achieve a high density 2DEG, the Al mole fraction should be higher. However, because of convergence difficulties in the MEDICI numerical simulation, the x value was reduced to 0.15.

The device considered was assumed to be Ga-faced. Drain and source ohmic contacts were formed with Ti/Al and gate metal (Ni/Au) was deposited on the recessed area. The metal work functions were set to be 4.28 eV for the drain and source and 5.125 eV for the gate as suggested in [3-4]. The δ-doping carrier concentration was set to be $2\times10^{19}cm^{-3}$. As can be seen in the Fig. 3.1, the current flows mainly through the 2DEG at

Layer	Material	Thickness(nm)	Doping (cm^{-3})
1 (Ohmic)	n^+-GaN	20	10^{19}
2 (Barrier)	$Al_{0.15}Ga_{0.85}N$	20	10^{18}
3 (Spacer)	$Al_{0.13}Ga_{0.87}N$	5	10^2
4 (Channel)	UID-GaN	5	10^2
5 (Nucleation)	n-GaN	50	5×10^4

Table 3-1: Device design specification of the recessed gate AlGaN/GaN SHEMT

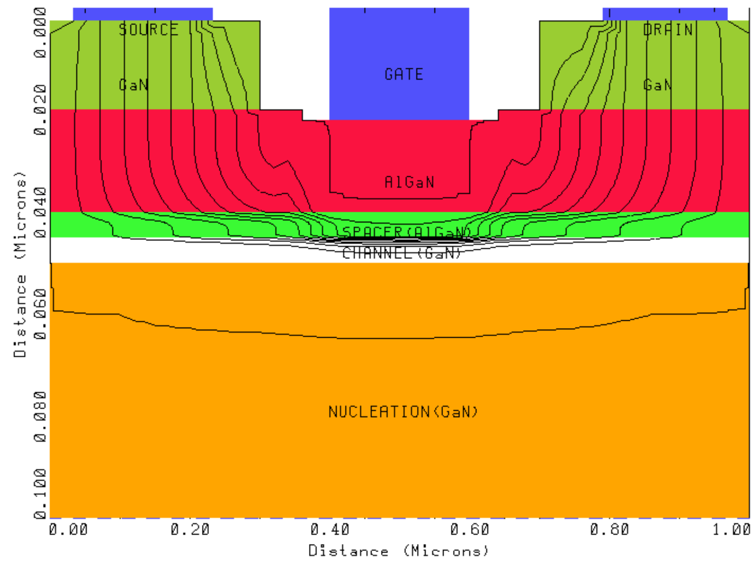
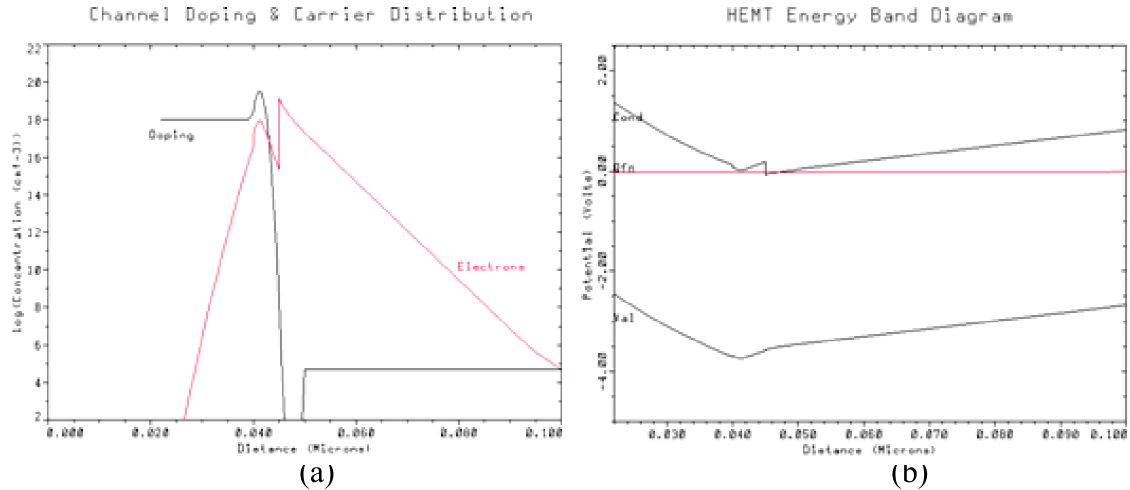


Figure 3-1: Device structure and current flow of the recessed gate AlGaN/GaN SHEMT

the heterostructure interface of the GaN layer. Fig. 3.2 shows that the carriers are confined and form a 2DEG. Finally the conduction band profile was intercepted by the Fermi level and a triangular potential well was formed at the channel region.

The high δ-doping polarization model induces a dip in the conduction band, as well as, high carrier (electron) concentration at the spacer. As previously mentioned, the high delta doping carrier concentration does not contribute adequately to the expected current



(a) (b)

Figure 3-2: (a) Channel doping and carrier distribution and (b) energy band diagram of the recessed gate AlGaN/GaN SHEMT

flow, and the electron mobility of that layer had therefore to be adjusted to a lower than originally set value. The δ-doping should ideally correspond to a very thin layer and have a very high peak concentration in order to describe the polarization effect reasonably.

However, a high peak concentration will result in a deep dip in the conduction band, which will either pin the Fermi level or shift below it. In this case, the residual carrier concentration at the δ-doping layer will allow current flow in spite of the low mobility and the threshold voltage will increase considerably. Therefore, a compromise needs to be made by adjusting the device parameters in order to obtain a reasonable value of threshold voltage.

Fig. 3.3 shows the I-V curve and gate characteristics respectively. From the I-V curve one sees that breakdown occurs at Vg = 35 V. This is a much smaller value than expected, considering the high breakdown field of GaN material; expected breakdown voltage values for GaN HEMT are around 100 V. The reason for this discrepancy is the high δ-doping considered in the model which initiates impact ionization at the gate edge

of drain side. The threshold voltage was -1 V which is a smaller value than the expected

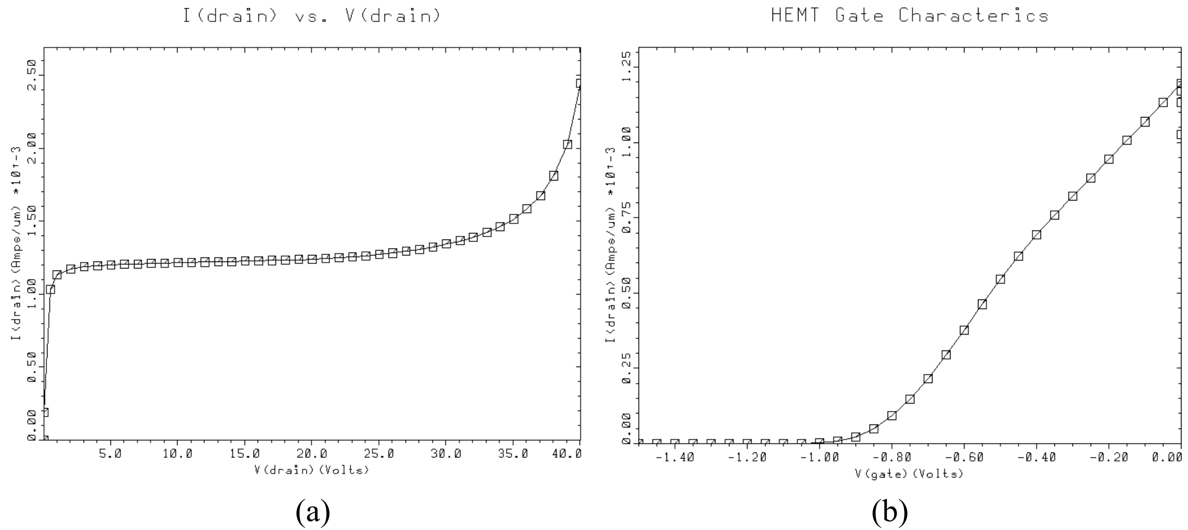


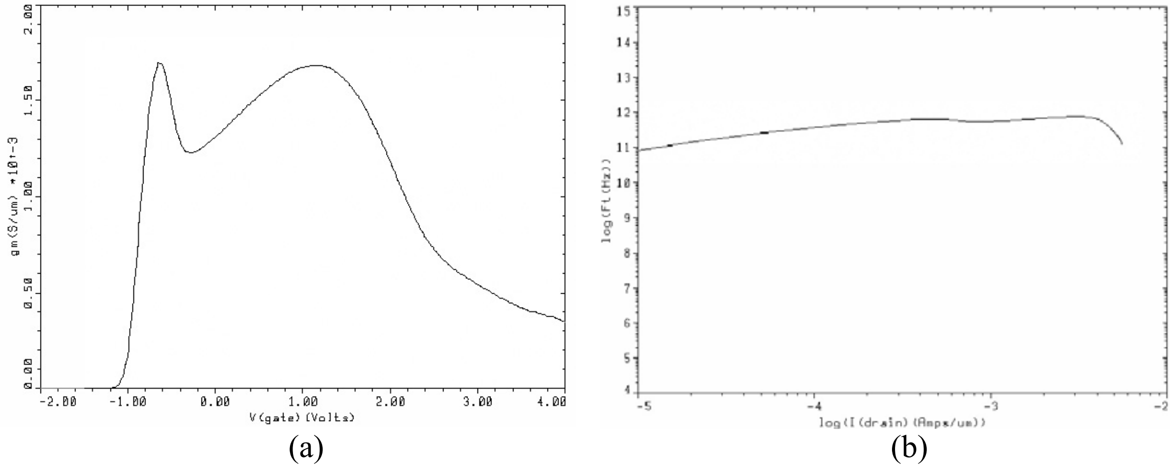
Figure 3-3: Output characteristics of the recessed gate SHEMT; a) I_{DS}-V_{DS} curve at V_{GS}=0, b) Gate characteristics (I_{DS}-V_{GS} curve)

value of -5 V. As mentioned earlier, the threshold voltage is mainly dependent on the doping and thickness of δ-doping layer. If V_{th} is fitted to the experimentally obtained values, the δ-doping should be increased and this would induce degeneracy in the spacer layer and the current flowing through the δ-doping layer.

Based on the above, the threshold voltage should be kept to a small value to ensure proper device operation. In addition, the drain current was also found to be higher than the reported values (100~400 mA/mm or $1\sim4\times10^{-4}$ A/μm). This could, however, be accounted for by adjusting the contact resistance as discussed later in section 3.2.3.

Fig. 3.4 shows the gate transconductance g_m vs. gate bias and cutoff frequency f_T vs. drain bias. The gate transconductance value is an order of magnitude higher than the reported value in [3-4]. This is due to the consideration of an ideal device design neglecting defects and non-idealities in the device such as contact resistance. With regard to the obtained high frequency characteristics, the cutoff frequency f_T was found to be

about 315 GHz which is also one order higher than the reported value (32.3 GHz). Since f_T can be expressed as a function of g_m, this result is reasonable considering the high value of g_m predicted by the model.

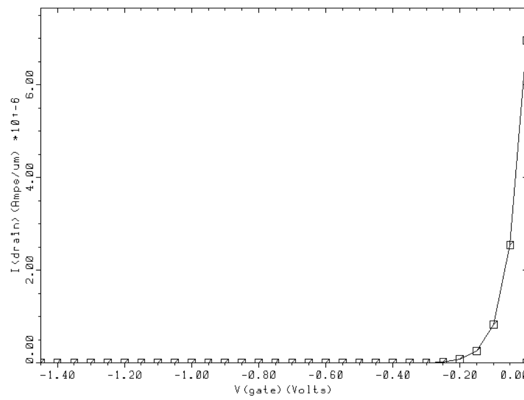


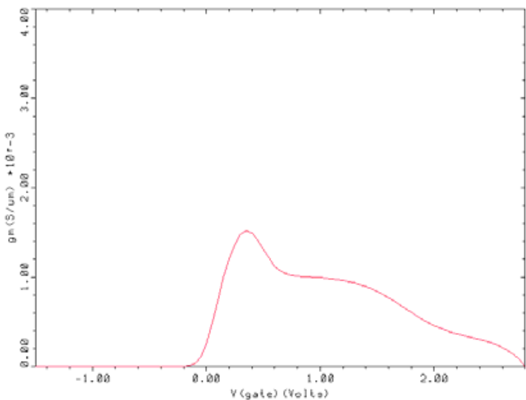
(a) (b)

Figure 3-4: (a) transconductance g_m (S/μm) vs. gate voltage and (b) cutoff frequency f_T vs. drain bias for the recessed gate AlGaN/GaN SHEMT

3.2.2 Impact of the δ-doping polarization model on the simulated HEMT characteristics

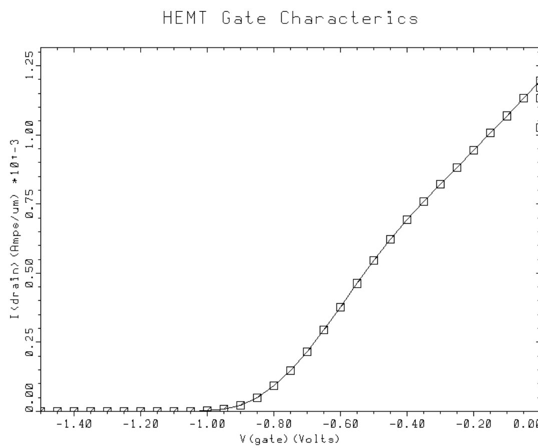
The difference between the simulated and reported values of threshold voltage, transconductance g_m and cut off frequency f_T described in section 3.2.1 are due to the δ-doping polarization model and the ohmic contact resistance which was considered to be ideal. The thickness and concentration of δ-doping were determined by adjusting the model parameters to obtain a 10^{13} cm^{-2} sheet carrier density at the heterojunction and ensure that the peak of the triangular shape conduction band is below the Fermi level. However, this simulation did not consider the drain and source metal contact resistance, which also affect the device characteristics. Therefore, by considering realistic contact

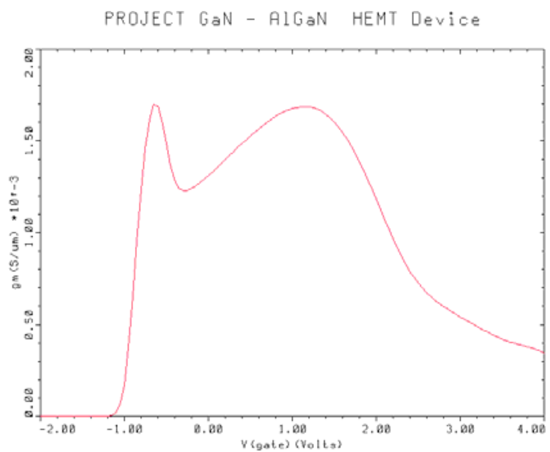




(a) (b)

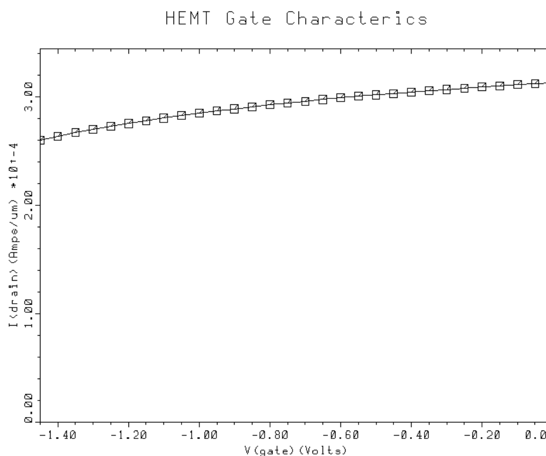
Figure 3-5: (a) I_{DS}-V_{GS} curve (b) g_m for the δ-doping concentration of 1×10^{19}cm^{-3}

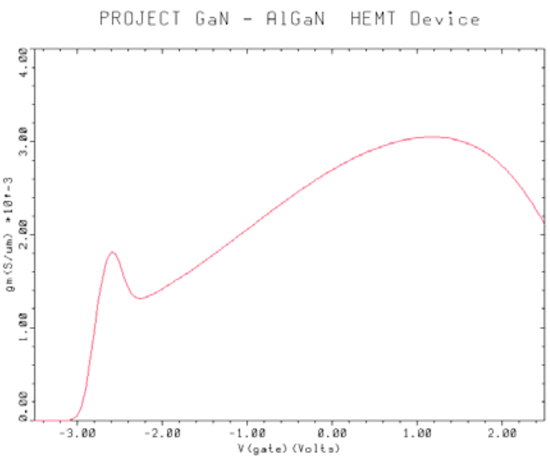




(a) (b)

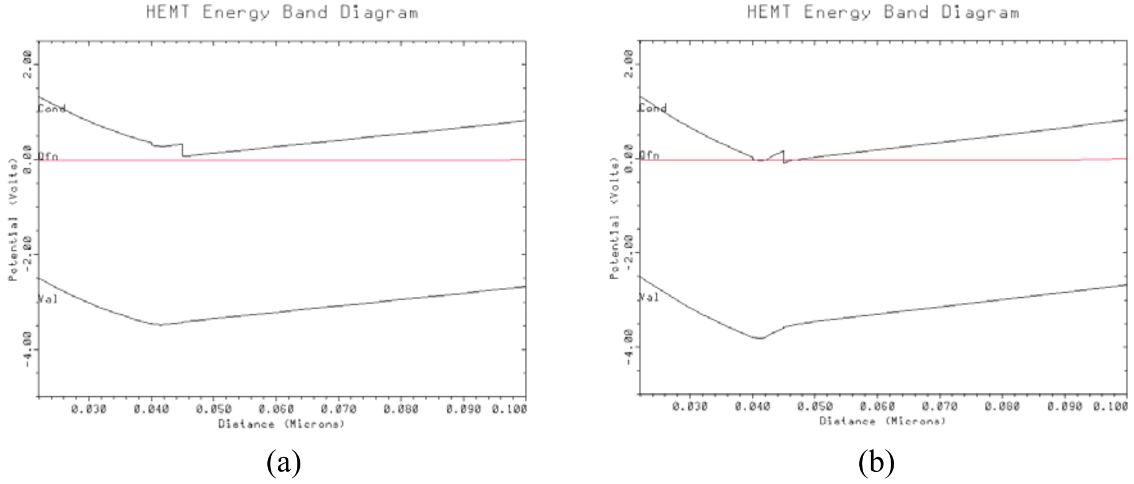
Figure 3-6: (a) I_{DS}-V_{GS} curve (b) g_m for δ-doping concentration 2×10^{19}cm^{-3} from section 3.2.1. (Same figure as in Fig. 3.3 (b) and Fig. 3.4 (a))





(a) (b)

Figure 3-7: (a) I_{DS}-V_{GS} curve (b) g_m for δ-doping concentration of 4×10^{19}cm^{-3}



(a) (b)

Figure 3-8: Energy band diagram for δ-doping concentration of (a) $1\times10^{19}cm^{-3}$ and (b) $4\times10^{19}cm^{-3}$

resistance values, the simulated performance can correspond better to the experimentally observed g_m and f_T values.

In order to investigate the impact of the δ-doping model on device characteristics, the threshold voltage and transconductance were simulated by adjusting the δ-doping concentration. Fig. 3.5 shows the I_{DS}-V_{GS} and transconductance characteristics for the case of up to 50% smaller doping concentration ($1\times10^{19}cm^{-3}$), while Fig. 3.6 corresponds to the case of the originally simulated results described in section 3.2.1 (δ-doping concentration of $2\times10^{19}cm^{-3}$). Fig. 3.7 corresponds to for the case of double δ-doping concentration ($4\times10^{19}cm^{-3}$).

As the δ-doping concentration decreases from $4\times10^{19}cm^{-3}$ to $1\times10^{19}cm^{-3}$. V_{TH} and g_m also decrease. From the energy band diagram at Fig 3.8 (a), there is no 2DEG formed at the heterostructure at zero gate voltage, because the impact of polarization effects is then too small. Also the drain current decreases to half of the drain current for δ-doping concentration of $2\times10^{19}cm^{-3}$. In case of increased concentration, the conduction band is

shifted below the Fermi level at the position of δ-doping and thus current flows through this layer even though low carrier mobility is considered. V_{TH} is also decreased from -1 V to -3.2 V and the maximum g_m is reduced from 1.7×10^{-3} S/μm (1700 mS/mm) to 3.1×10^{-3} S/μm (3100 mS/mm). The saturation current is finally increased to more than 10mA.

An important consideration factor for proper device simulation is the contact resistance, which was ignored in the previous simulation. In the following section, the contact resistance is taken into account in an attempt to obtain realistic values of device characteristics.

3.2.3 Non-recessed vs. recessed gate SHEMT: consideration of ohmic contact resistance

In order to optimize the HEMT performance, it is very important not only to enhance the 2DEG properties but also to reduce the presence of parasitic resistances. However, the high Al composition in the AlGaN barrier, which induces the presence of high carrier concentration of carrier at the heterostructure, results in poor ohmic contact. From the measured HEMT performance values [3-4], a contact resistivity of 8×10^{-6} Ωcm^2 was found in case of n-GaN (doping concentration: $1\times10^{19}cm^{-3}$). This increased to 7×10^{-5} Ωcm^2 in case of lower n-AlGaN doping concentration ($1\times10^{18}cm^{-3}$). In a recessed gate structure, ohmic contacts of low resistivity can be formed if a high doping density is ensured for the n-GaN layer grown on the top of the AlGaN barrier layer. Consideration of variable contact resistance values can be made for both the source and drain metals through the input statement CON.RESIS in MEDICI. To investigate the advantages of recessed gate design, a non recessed gate SHEMT was designed with same doping and

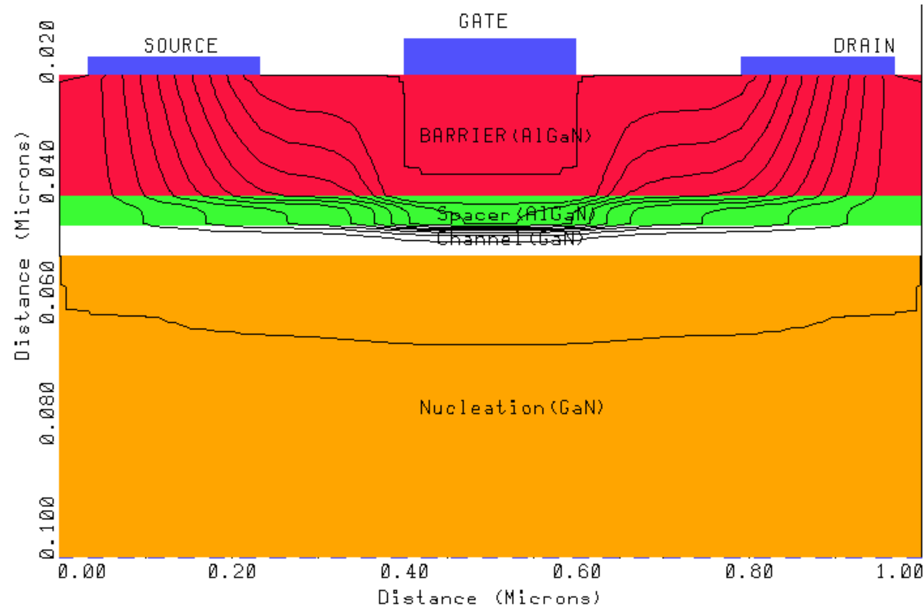
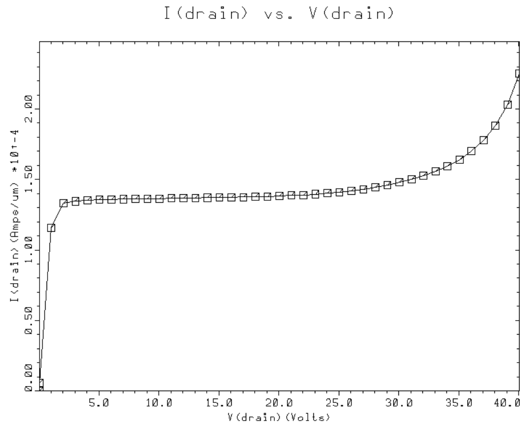


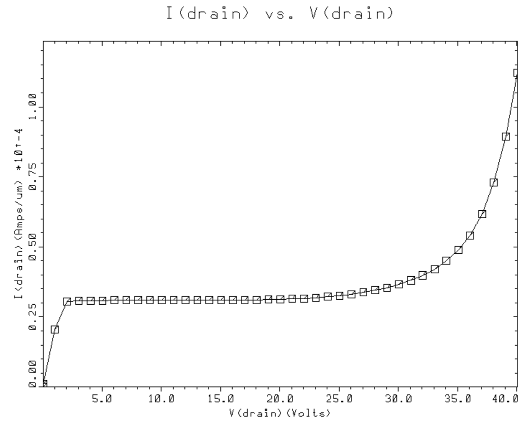
Figure 3-9: non-recessed gate SHEMT device structure and current flow

thickness for each layer, but without a GaN cap layer. Fig. 3.9 shows the device structure and current flow.

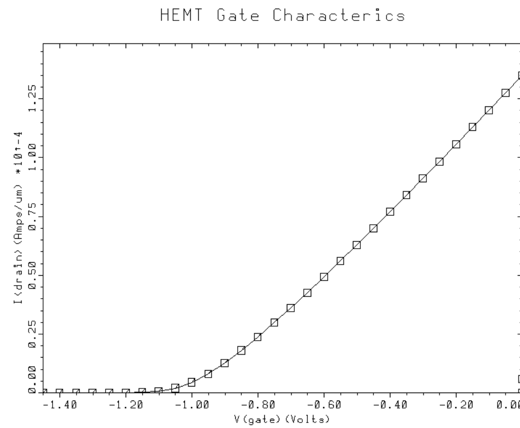
As in the case of the recessed gate SHEMT, the impact of δ-doping polarization model on the device characteristics is very significant. In order to compare the two designs, the concentration and thickness of δ-doping were set to be the same for both designs. The contact resistance for the AlGaN barrier layer was adjusted to 4.8×10^{-5} Ωcm^2. Since the contact resistance of the recessed gate HEMT simulated in sections 3.2.1 and 3.2.2, was not considered all device characteristics were simulated again with proper contact resistance value. The carrier distribution and 2DEG density was not affected by the contact resistance but the drain current was decreased due to the contact resistance. However, the device characteristics such as threshold voltage, which are mainly dependent on the δ-doping did not change. Fig. 3.10 shows the output and transfer characteristics of recessed gate and non-recesses gate HEMTs.



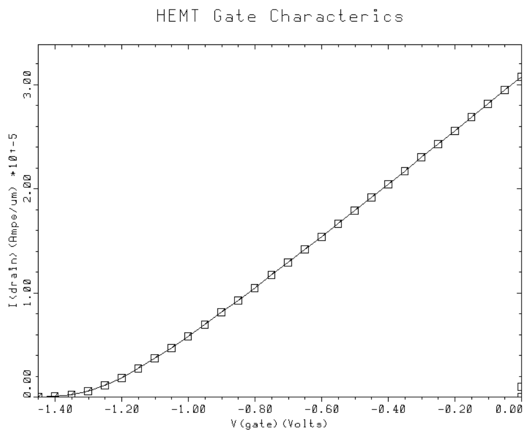
(a)



(b)



(c)



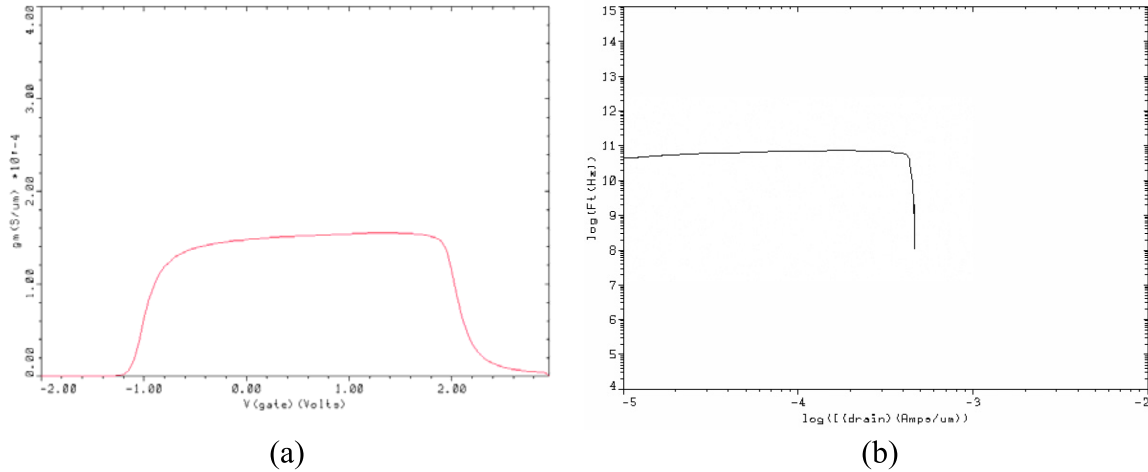
(d)

Figure 3-10: I_{DS} vs. V_{DS} curve at zero gate voltage for a) recessed gate b) non-recessed gate and I_{DS} vs. V_{GS} curve for c) recessed gate b) non-recessed gate

The saturation current for the recessed gate HEMT was 1.35×10^{-4}A/μm (135mA/mm) which corresponds to the reported values. In case of non-recessed gate SHEMTs, the saturation current was 0.32×10^{-4}A/μm (32mA/mm) corresponding therefore to 24% of the I_{DSsat} value of the recessed gate design. In case of the threshold voltage, the non-recessed gate showed an increase to -1.3 V due to the different distance assumed between the gate and channel; in the recessed gate design, the gate is closer to the channel by 2 nm due to barrier layer etching. This supports the fact that the threshold

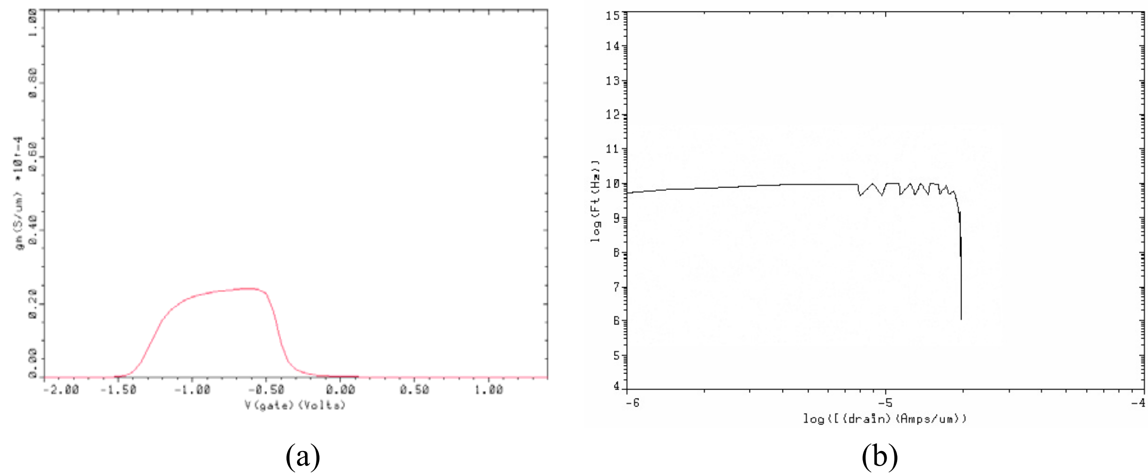
voltage can be adjusted through the control of the gate to channel distance. Fig. 3.11 and Fig. 3.12 show the g_m and f_T results for both designs. When a zero contact resistance is considered, the transconductance value for the recessed gate design is an order of magnitude higher than the reported value. Moreover the g_m characteristics indicate the presence of a hump. After introduction of a finite contact resistance value in the simulation, the shape of g_m plot became more realistic and g_m equals 1.58×10^{-4} S/μm (158 mS/mm). The cut off frequency f_T was also found to be reduced to 50 GHz from the originally simulated value of 315 GHz. As a result, the recessed gate SHEMT allowed good reproduction of the experimentally observed HEMT characteristics. A degradation of g_m and f_T device performance in case of the non-recessed gate design could also be found. The transconductance was 22 mS/mm (degraded by 86%), and cutoff frequency was only about 12 GHz (degraded by 76%).

In conclusion, the AlGaN/GaN HEMT with recessed gate was found to manifest higher saturation current, as well as, better frequency performance than without recess due to the fact that the GaN ohmic layer under the source and drain had smaller contact resistance. However, recessed gate HEMTs are more demanding in terms of processing, requiring careful gate etching.



(a) (b)

Figure 3-11: (a) g_m vs. V_{GS} and (b) f_T vs. I_{DS} for the recessed gate SHEMT.



(a) (b)

Figure 3-12: (a) g_m vs. V_{GS} and (b) f_T vs. I_{DS} for the non-recessed gate SHEMT

3.2.4 Double-heterojunction HEMT with InGaN layers

In spite of the impressive results obtained in terms of predicted performance for recessed gate SHEMTs, the single-heterojunction HEMT design presents certain limitations [3-5]. First, carriers in the 2DEG can easily spill over into the buffer GaN or the barrier AlGaN layers. This spillover decreases transconductance and increases the low frequency noise [3-6]. In addition; the spilled-over carriers may be trapped and thus give

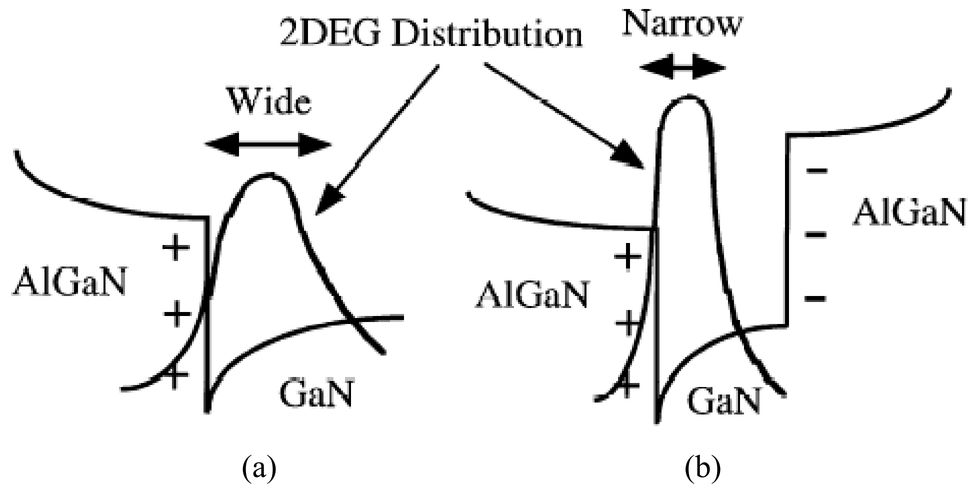


Figure 3-13: Conduction band profile and 2DEG distribution of (a) SHEMT and (b) DHEMT (from [3-5])

rise to slow transient processes and RF-current collapse. There are two possible solutions for impeding carrier spillover: i) using a bottom AlGaN layer between the channel and nucleation GaN layer and ii) using InGaN instead of GaN for the channel.

Fig. 3.13 shows the potential profile and carrier distribution of single heterojunction and double heterojunction device designs. As can be seen, in case of double heterojunctions, the AlGaN layer forms a potential barrier under the channel which impedes carrier spilling. Furthermore, the presence of lattice strain at the GaN/AlGaN heterostructure is combined with the presence of negative piezoelectric charges at the AlGaN barrier under the channel. These charges push electrons to the barrier side of the heterointerface and as a result the carrier confinement in the 2DEG increases. In case of the second design option where an InGaN channel is used, the conduction band discontinuity increases due to the fact that the bandgap of InGaN is smaller than that of GaN. Since the Bohr radius and lattice constant of InN are larger than those of GaN, the tensile stain of the AlGaN barrier layer is increased. Therefore the piezoelectric

polarization effect (i.e., piezoelectric charges), which is responsible for attracting electrons at the heterostructure, is more significant in case of the InGaN channel design.

Increased carrier confinement, induced by the double heterojunction and InGaN channel, not only prevent carrier spillover but also increase the 2DEG mobility [3-7]. This differs from the case of 2DEG mobility in GaAs HEMTs where no such an enhancement is observed when using double heterostructures. Therefore, the mobility enhancement in DHEMTs is a unique phenomenon specific to III-Nitride HEMTs. The 2DEG mobility increase is explained by two mechanisms: i) the enhanced screening effect against the ionized impurity scattering both in the channel and from the barrier layer, and ii) the enhanced screening effect against the piezoelectric scattering in the channel. As can be seen in Fig. 3.13 carriers are better confined in the 2DEG due to the presence of the double heterostructure. Therefore, the probability of carriers to interact with the ionized impurity or piezoelectric charge is reduced. However, the use of a bottom AlGaN layer leads to two problems. The heterointerface morphology of GaN on AlGaN is not as good as AlGaN on GaN. Moreover, an additional parasitic second 2D channel is created at the interface between the bottom AlGaN layer and the GaN nucleation layer, resulting in degradation of the device characteristics. The AlGaN/InGaN/GaN DHEMT design is therefore preferable since it eliminates the parasitic second channel, improves the structural morphology and simplifies the growth procedure.

In the following section, three designs of DHEMTs; AlGaN/GaN/AlGaN, AlGaN/InGaN/AlGaN, and AlGaN/InGaN/GaN DHEMT are simulated. Table 3.2 shows the design specifications of the three DHEMTs.

1. AlGaN/GaN/AlGaN			3. AlGaN/InGaN/AlGaN			3. AlGaN/InGaN/GaN		
Material	Thick. (nm)	Dop. (cm^{-3})	Material	Thick (nm)	Dop. (cm^{-3})	Material	Thick (nm)	Dop. (cm^{-3})
n^+-GaN	20	10^{19}	n^+-GaN	20	10^{19}	n^+-GaN	20	10^{19}
$Al_{0.15}Ga_{0.85}N$	20	10^{18}	$Al_{0.15}Ga_{0.85}N$	20	10^{18}	$Al_{0.15}Ga_{0.85}N$	20	10^{18}
$Al_{0.13}Ga_{0.87}N$	5	10^2	$Al_{0.13}Ga_{0.87}N$	5	10^2	$Al_{0.13}Ga_{0.87}N$	5	10^2
UID-GaN	5	10^2	$In_{0.10}Ga_{0.90}N$	5	10^2	$In_{0.15}Ga_{085}N$	5	10^2
$Al_{0.13}Ga_{0.87}N$	40		$Al_{0.25}Ga_{0.75}N$	40	5×10^4			
n-GaN	10	5×10^4	n-GaN	10	5×10^4	n-GaN	50	5×10^4

Table 3-2: Design specifications of the three double-heterostructure HEMTs (DHEMTs)

Most of the design parameters used in the simulation were the same as for the recessed gate SHEMT design parameters except for the InGaN channel and bottom AlGaN layer. Fig. 3.14 shows the device structures and corresponding current flows. For design 1 (AlGaN/GaN/AlGaN) and design 2 (AlGaN/InGaN/AlGaN), the bottom barrier layer was inserted above the nucleation layer. The thickness of the AlGaN barrier layers was 40 nm which is larger than that mentioned in the reference papers [3-5],[3-7]. This permits to avoid consideration of the additional parasitic 2DEG at the heterostructure between the bottom barrier layer (AlGaN) and nucleation layer (GaN). For more accurate results, the parasitic 2DEG should be modeled by the δ-doping model. This was not, however, considered necessary since the assumption of increased thickness was found to be adequate for simulating the carrier confinement effect. Design 3

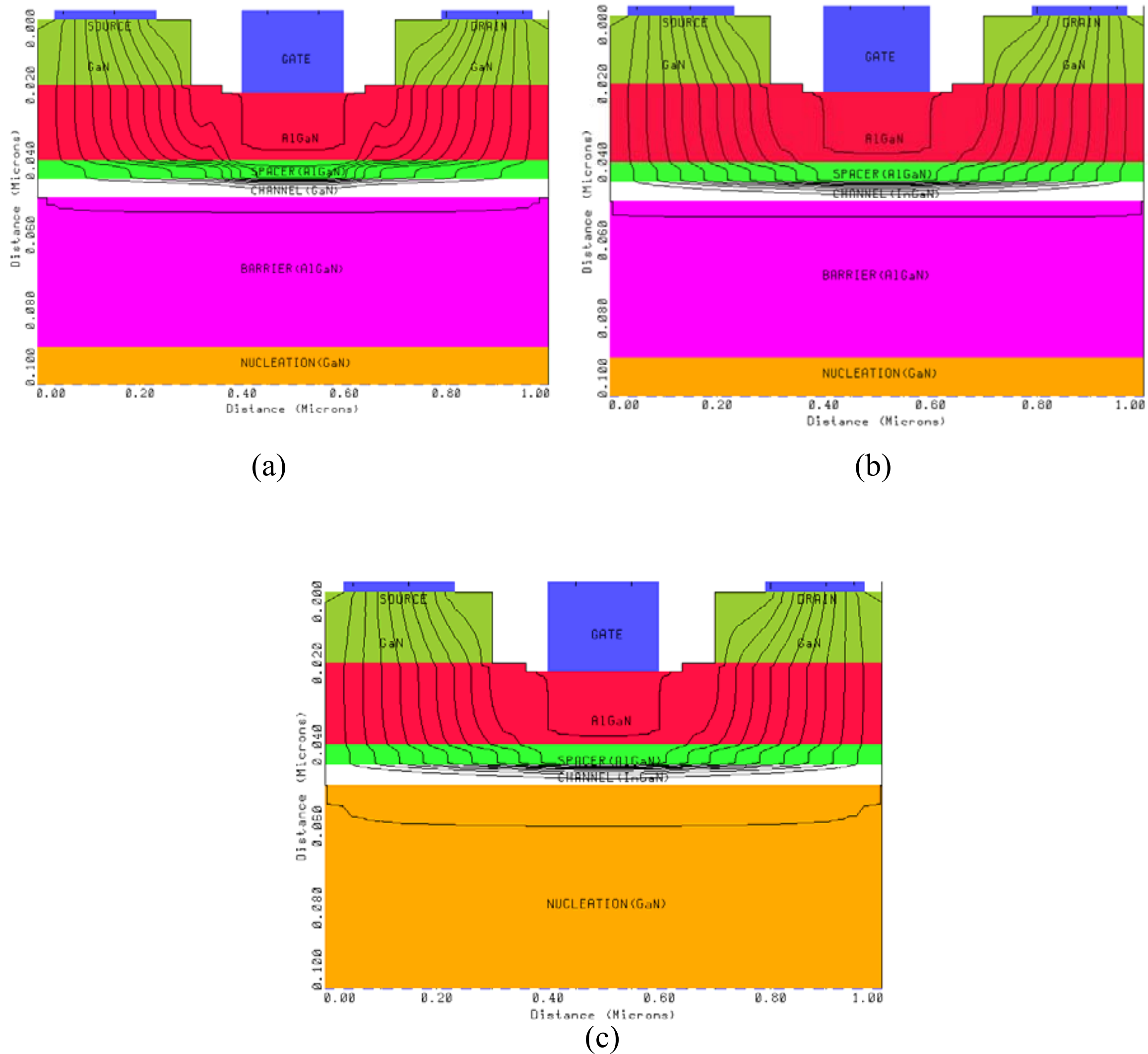


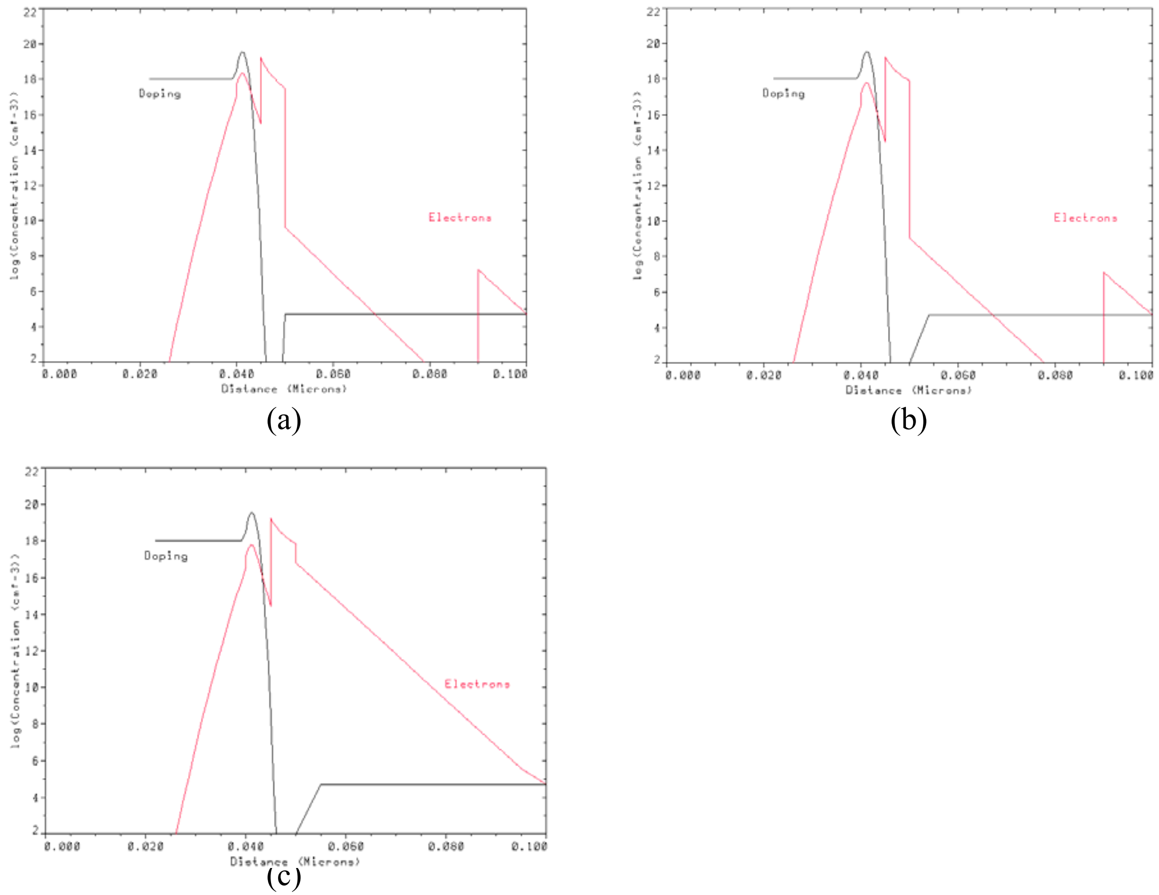
Figure 3-14: Device structures and current flows for the three DHEMTs; (a) design 1 (AlGaN / GaN / AlGaN) (b) design 2 (AlGaN / InGaN / AlGaN) and (c) design 3 (AlGaN / InGaN / GaN)

(AlGaN/InGaN/GaN) is the same design as that of the recessed gate SHEMT except for the GaN channel which was substituted in this case by InGaN. Fig. 3.14 shows that current flows are mainly through the 2DEG at the heterointerface.

The device characteristics of each design can be easily examined by considering the carrier distributions as shown in Fig. 3.15 and energy band diagrams in Fig. 3-.16. In case of the design 1 and 2, the bottom AlGaN barrier layers lead in conduction band barriers at

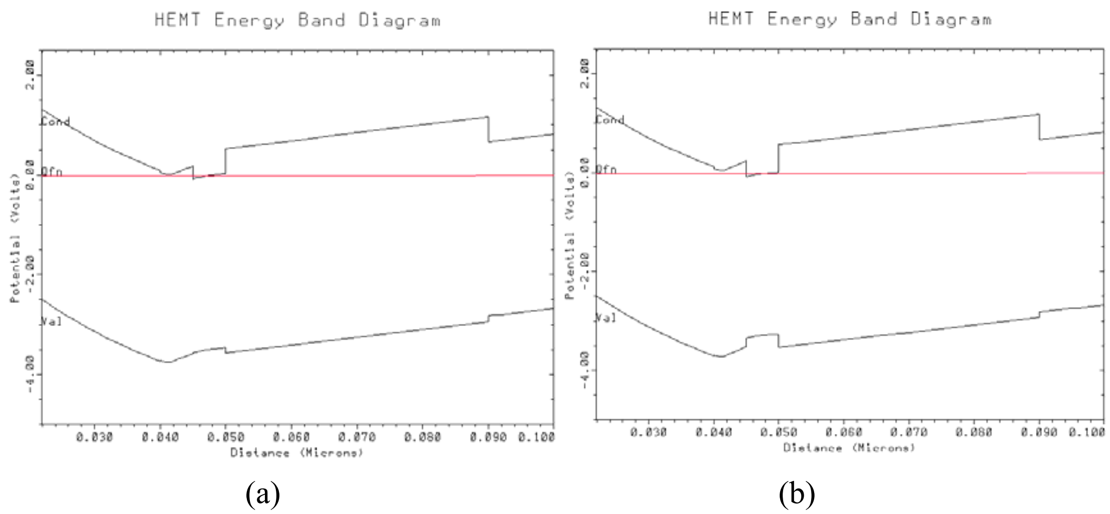
the bottom side of the channel as seen in the Fig. 3.16 (a) and (b). Therefore, carriers are more confined at the channel and hardly spill over the bottom layer. Hence the carrier distributions do not have a long tail over the barrier and nucleation layers in Fig. 3.15 (a) and (b). The improvement of device characteristics by carrier confinement can be verified by the saturation current at V_{GS} = 0V. I_{DSSAT} of the non-recessed gate SHEMT, which was 135 mA/mm, increases to 168 mA/mm (25% improvement) by using a double heterostructure with GaN channel (design 1) and to 195 mA/mm (45 % improvement) with InGaN channel (design 2). It should be noted that in the simulation performed, the negative polarization charge in the bottom AlGaN barrier, which pushes carriers to the 2DEG, is not considered. Thus the carrier confinement effect is smaller than that present in the real device. Interestingly enough, the breakdown voltage V_{br} for InGaN channel shown in Fig. 3.17 is about 5V less than that of GaN channel. This is most likely due to the smaller band gap of InN (2.01 eV at 300K).

In the case of design 3, the saturation current increases (188 mA/mm, 40% improvement) compared with the GaN channel SHEMT operated under the same conditions. According to [3-5], design 3 should show similar or even better performance than design 2, but I_{DSSAT} for design 3 is only 188 mA/mm which is 7 mA/mm less than that of design 2. This is due to the fact that there is no consideration of parasitic 2DEG effects between InGaN/AlGaN in the performed simulation. However, this result suggests that design 3 is more attractive. The improvement of I_{DSsat} is not significantly different (only 7mA/mm) between design 2 and design 3 but design 3 is better due to its simpler structure and easier growth of InGaN on GaN than InGaN on AlGaN.



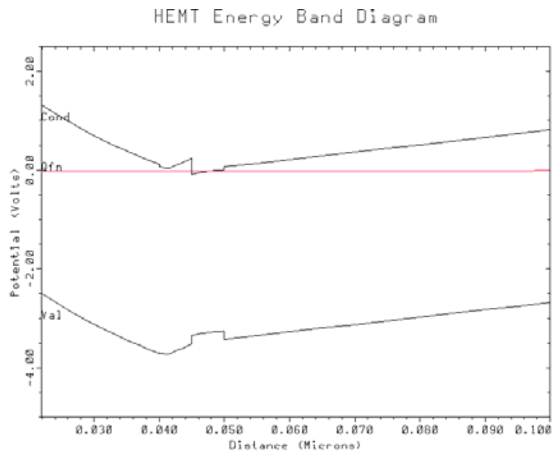
(a) (b) (c)

Figure 3-15: Doping density and carrier concentrations of (a) design 1 (AlGaN/GaN/ AlGaN) (b) design 2 (AlGaN/InGaN/AlGaN) and (c) design 3 (AlGaN/InGaN/GaN)



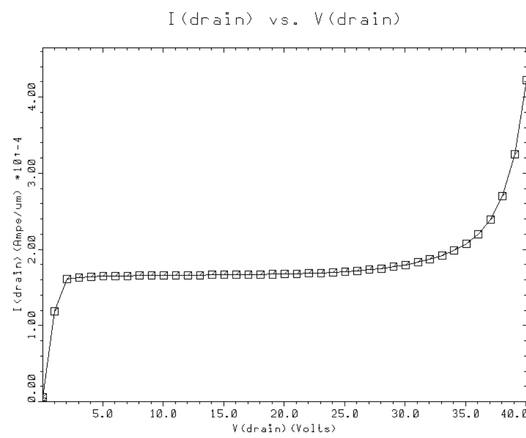
(a) (b)

Figure 3-16: Energy band profile of design 1 (AlGaN/GaN/ AlGaN) (b) design 2 (AlGaN/InGaN/AlGaN) and (c) design 3 (AlGaN/InGaN/GaN)

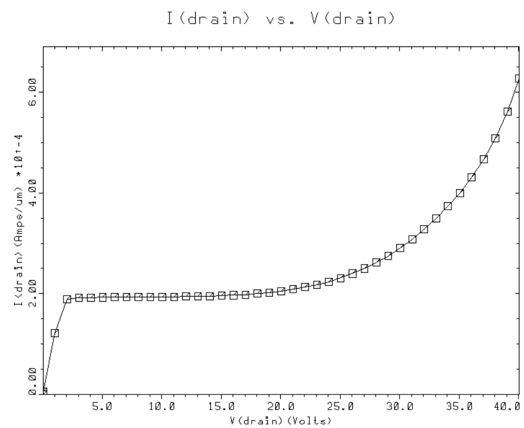


(c)

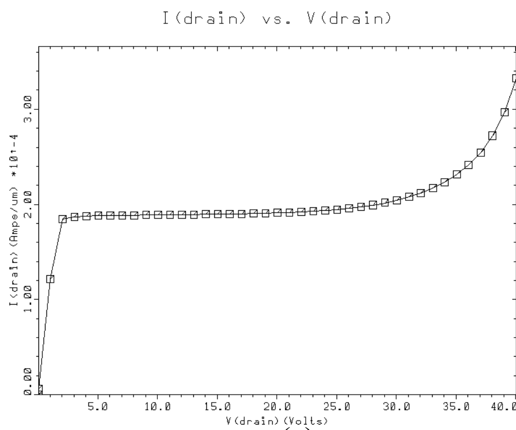
Figure 3-16 (continued) Energy band profile of (a) design 1 (AlGaN/GaN/AlGaN) (b) design 2 (AlGaN/InGaN/AlGaN) and (c) design 3 (AlGaN/InGaN/GaN)



(a)



(b)



(c)

Figure 3-17: I_{DS}-V_{DS} curves with V_{br} of (a) design 1 (AlGaN/GaN/AlGaN) (b) design 2 (AlGaN/InGaN/AlGaN) and (c) design 3 (AlGaN/InGaN/GaN)

The simple model for polarization effect used in this simulation does not appear to be adequate for accounting for the difference of transconductance and cutoff frequency of the three designs. In the designs considered here, the piezoelectric constant of GaN and InGaN are in reality different, and the strain in the heterostructure, which induces piezoelectric polarization, is different for AlGaN/GaN and AlGaN/InGaN heterostructures. However in the performed simulation, the δ-doping model used is the same in order to verify the effect of carrier confinement by the use of InGaN channel and double heterostructure. Without fixing the profile of δ-doping, it is not possible to see the device performance differences, which is a weakness of the polarization model used in the simulation. However, based on the drain current variation, one can investigate the impact of carrier confinement on device characteristics in case of double heterostructure designs.

In theory, an InGaN channel is superior to a channel made of GaN. However, it is difficult to obtain a high quality InGaN layer, because of the low InN decomposition temperature which is about 500˚C and therefore much lower than that used for GaN growth (1050˚C). Moreover, the growth rate of InGaN is much slower than that of GaN. In order to make use of the advantages of the InGaN channel, one should therefore overcome the growth difficulties involved in realizing such structures.

In conclusion, using MEDICI-based simulations, non-recessed gate and recessed gate AlGaN/GaN single-heterostructure HEMTs were designed in conjunction with a simplified δ-doping model for the piezoelectric and spontaneous polarization effects. In spite of the imperfect polarization model used in our simulations, the advantages of recessed gate over non-recessed gate structures were clearly shown. By introducing

realistic contact resistance values to non-recessed designs, the simulated results can be matched well to experimentally obtained device characteristics. In addition, the superiority of DHEMT on SHEMT and the advantages of using InGaN rather than GaN channels were examined and simulated based on a comparative study of three DHEMT designs (AlGaN/GaN/AlGaN, AlGaN/InGaN/AlGaN, and AlGaN/InGaN/GaN DHEMT). Because of the imperfection of the polarization model, and in particular the significant dependence of transconductance, cutoff frequency, and threshold voltage on the δ-doping profile, the device characteristics were only compared based on drain current considerations. The results of this study agree well with theoretically predicted expectations of better carrier confinement in the 2DEG and higher current density in case of DHEMTs.

Overall, AlGaN/GaN HEMTs present unique advantages over other power devices and therefore significant effort is still needed in order to optimize their performance. InGaN/GaN structures appear to be very attractive for high frequency applications due to their higher mobility and better carrier confinement.

3.3 Device Simulation for AlN/GaN MISFETs using ISE-TCAD

Physical simulation models of AlN/GaN MISFETS and AlGaN/GaN HEMT are needed to better understand the factors influencing the operation of the devices fabricated. The operation and properties of III-nitride devices have not been understood completely, and there are various aspects of growth and fabrication that cannot be precisely controlled or reproduced. Examples of their difficulties are the AlN/AlGaN/GaN interface quality achievable in different reactors under different growth conditions as well as the experimentally obtained source and drain ohmic contact quality [3-8],[3-9]. Other

important characteristics such as Schottky barrier height at the gate contact can only be roughly estimated. Internal conditions such as electric field strength in the gate-drain region, levels of unintentional doping (UID) and possible impact of bulk and interface traps can be studied theoretically since they are not easily measurable.

An appropriate simulation model allows variation of these parameters and matching of resulting I-V curves to those of fabricated devices. This permits estimation of the Schottky barrier height and evaluation of surface depletion effects, effective interface charge density and UID and their impact on device operation. For design purposes, physical aspects of the device such as barrier layer thickness, dimensions, effect of passivation, etc. can also be evaluated with the help of physical simulation. One can for example evaluate in this way the dependence of AC performance on barrier layer thickness by simulation. Simulations are also a useful method to compare the relative performance of other types of devices to fabricated ones, such as MISFETs and HEMTs, when all device types are not available foe measurements.

The device physical simulator used in this work is DESSIS from ISE-TCAD (now available as Synopsys). Since the gate length of the devices under simulation is around 1μm, basic drift-diffusion mobility models are used. Hydrodynamic models are needed only when the gate length begins to approach 100nm.

3.3.1 ISE-TCAD simulator

ISE-TCAD is composed of several sub programs or tools for drawing, meshing, simulating, and graphing. The following is brief description of each program and special setup used for the AlGaN/GaN HEMTs or AlN/GaN MISFET simulations.

GENESIS : This is the simulation framework which makes it possible for a tool chain to be created with different tools for device creation, simulation and viewing the results.

DEVISE : To create the simulation, the tool DEVISE is used to set geometries, define doped areas and setup the mesh. To emulate UID, n-type doping in the range of $10^{15} \sim 10^{16}$ cm^{-3} is defined for the entire area. Regions like the source and drain contacts are given a high n-doping concentration of 10^{19} cm^{-3} to duplicate ohmic conditions. The contacts for a device such as source, drain and gate are defined in this step. Fig. 3.18 shows the example meshing of gate-source region in AlN/GaN MISFETs.

DESSIS : The DESSIS tool controls which terminals are subjected to voltage. Various types of analysis can be specified such as AC and transient types. The physics of the device and material properties can be set. Significant simulation inputs that are specified here include the ohmic contact resistance at the source and drain, Schottky barrier height, polarization charge and trap density at the hetero-interface and bulk trap levels and density. Apart from the voltages and currents a large list of data can be compiled with information about the device.

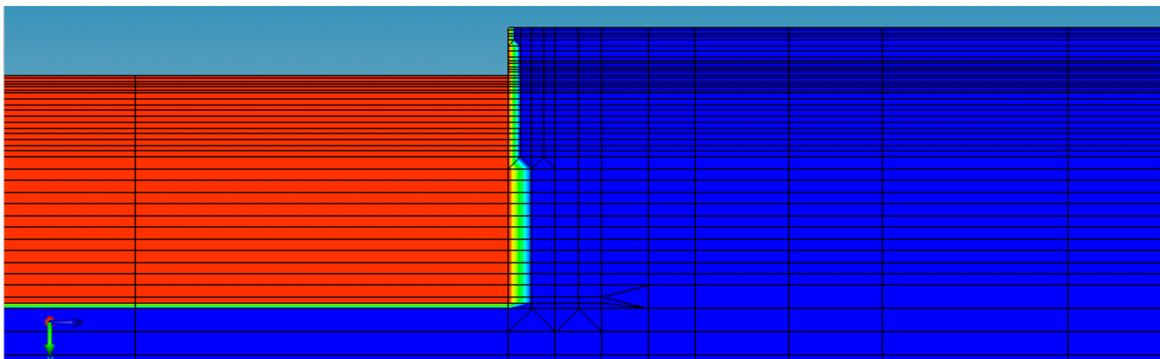
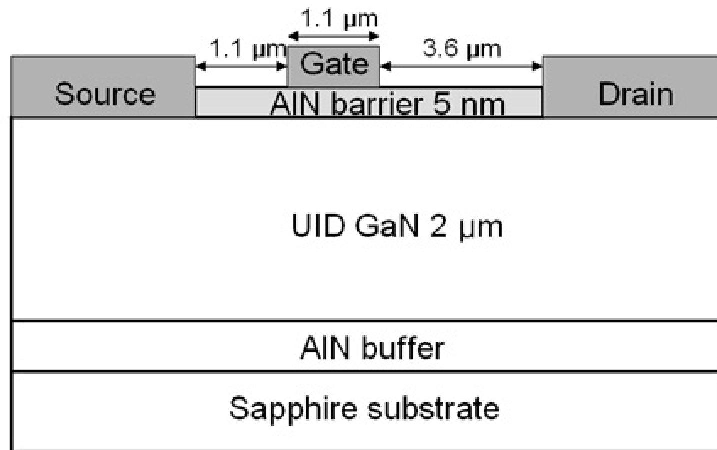


Figure 3-18: Mesh and doping profiles created using DEVISE for a AlN/GaN MISFET. Gate-Source access region is shown.

TECPLOT, INSPECT : These tools are used to view the results produced by DESSIS. INSPECT can be used to plot I-V curves and TECPLOT can be used to map data such as electric field or trapped charges in the entire device or selectively view certain device regions.

3.3.2 AlN/GaN MISFETs simulation conditions

Drift diffusion simulations were performed for 1 μm gate length AlN/GaN MISFET devices with self-heating effects ignored, since the aim of the study was to obtain a first understanding of the device physics while allowing one to make comparisons to other device designs. The initial simulation is performed with theoretically estimated values of the hetero-interface charge, Schottky barrier height and assuming a low ohmic contact resistance. Then in successive iterations these parameters were varied and their effect on the I-V curves was compared with experimental values. The obtained AlN/GaN MISFET model was used to match experimental characteristics of fabricated devices. An AlGaN/GaN HEMT model was used for the purpose of comparison. The device schematics for the two devices are depicted in Fig. 3.19. The followings are main physical parameters of the devices considered for simulations.



(a)

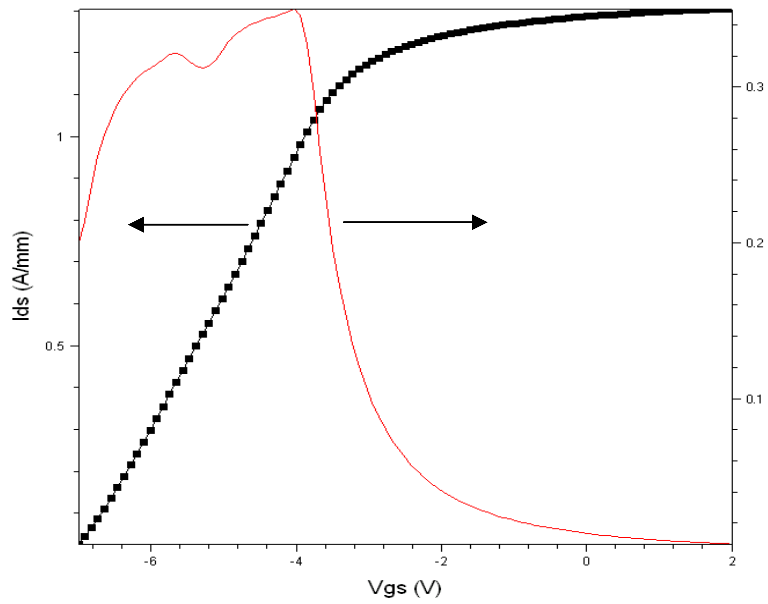
(b)

Figure 3-19: (a) Schematic of AlN/GaN MISFET and (b) Schematic of AlGaN/GaN HEMT for DESSIS simulations

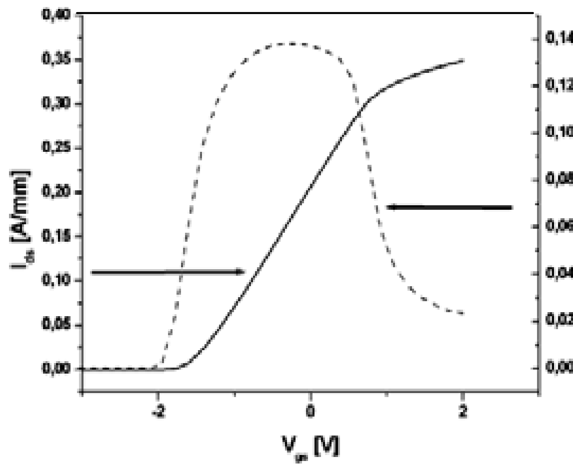
Contact resistance: Contact resistance can be specified in the simulation for the source and drain ohmic contact region. The effect of the contact resistance to the DC simulation is most pronounced, and has a major impact on the maximum drain current value. Based on actual TLM measurement results, a value of 1.75 Ω·mm has been used

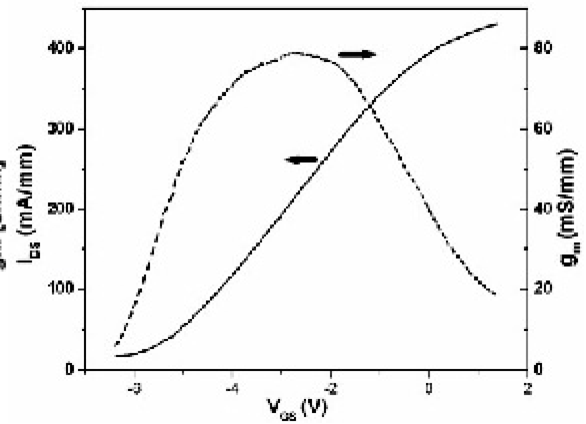
for the MISFET simulations.

Interface charge: Simulations carried out with the theoretically predicted polarization sheet charge density due to piezoelectric and spontaneous polarization charges of 6×10^{13} cm^{-3} predicted a higher current than observed experimentally [3-9]. However, Hall measurements performed on AlN/GaN structures showed sheet carrier densities of only 0.98×10^{13} cm^{-2}. The presence of a very thin unpassivated AlN layer can contribute to a reduction in 2DEG density due to a high surface barrier height [3-10]. The significant lattice mismatch between AlN and GaN might lead to formation of a large number of interface electron traps which result in reduction of the effective polarization charge. Therefore, a further parameter introduced is the interface trap density, which is adjusted to 0.43×10^{13} cm^{-2} to reproduce the experimentally observed values. Since there is considerable variation in growth for III-nitride materials, the quality of the interface cannot be guaranteed. The adjustment required for matching the simulation results to experimental characteristics provides an indication of the actual properties of the material used in fabrication.



(a)





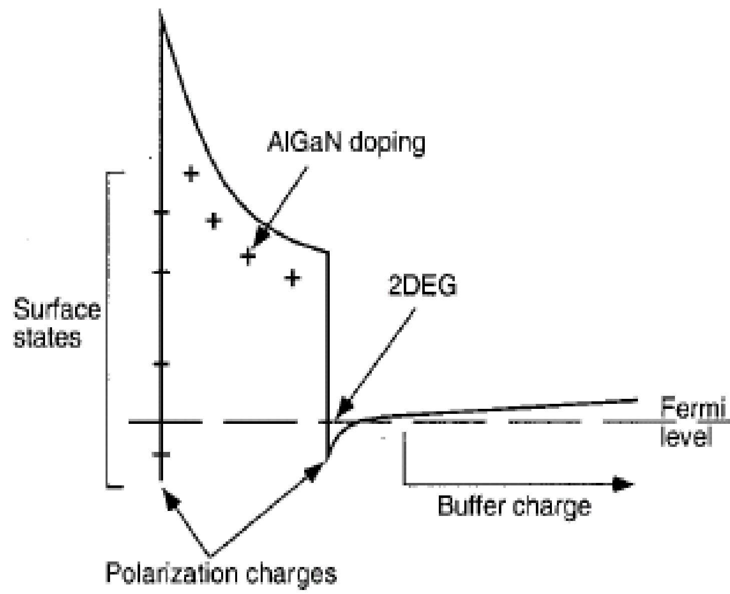
(b) (c)

Figure 3-20: (a) I_{DS}-V_{GS} and g_m curves with an interface charge of 6×10^{13} cm^{-3} in AlN/GaN MISFETs (b) maximum I_{DS} closer to the experimentally measured curve in (c) due to reducing the interface charge and introducing interface traps.

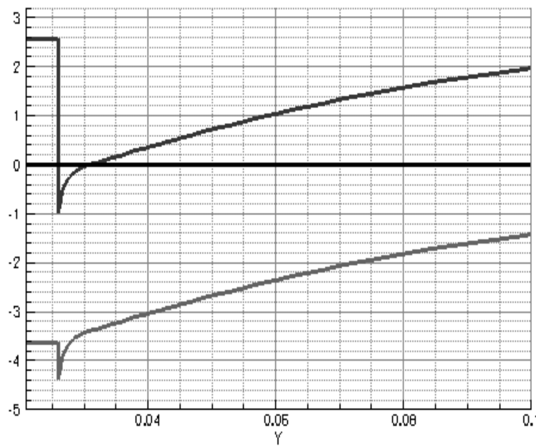
Bulk traps: In Figure 3.20 (c) it is observed that the experimental device pinches off only at a gate voltage of -6 V and that pinch off is not complete. By varying the UID concentration in bulk GaN one can simulate the presence of pinch-off features. Gradual pinching can be explained by the presence of defects in the bulk material whose impact is controlled by the UID. The drain current decreases if the level of traps is set closer to the conduction band or the concentration of traps is increased.

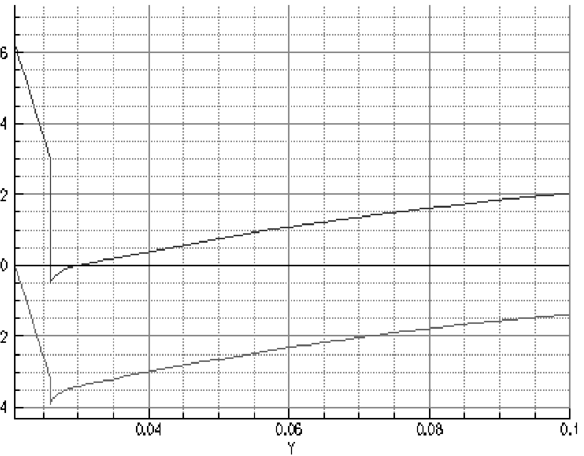
Schottky barrier height: this determines the pinch-off voltage and also the rate at which the device pinches off. For the MISFET simulations a barrier of 2.65 eV was a good fit to the slope of the experimental I_{DS}-V_{GS} curves

Surface States: Unless a positive interface charge is specified, DESSIS cannot generate the correct band diagram at the AlN/GaN interface. For the system to be charge neutral a mirror negative charge is specified at the AlN surface. Since the AlN barrier is undoped, it acts as a source of electrons for the 2DEG from donor like states on the surface [3-10]. The surface states effect on the band diagram is shown by comparison with theoretical band diagrams in Fig. 3.21. With passivation, the effect of surface states is mitigated and the 2DEG density increases as seen in Hall measurements.



(a)





(b) (c)

Figure 3-21: (a) theoretical band diagram of the barrier layer and interface for III-Nitride HEMTs, (b) band diagram without any charge at the surface and (c) the change when a negative charge is defined at the AlN surface for AlN/GaN MISFETs

3.3.3 AlN/GaN MISFETs simulation results

A 5 nm AlN barrier layer thickness MISFET and a HEMT of the same dimensions, with a 24 nm $Al_{0.32}Ga_{0.68}N$ barrier layer were simulated. From Hall measurements, a

charge of 0.98×10^{13} cm^{-2} was used to simulate the MISFET, with a mirror negative charge placed at the unpassivated AlN surface. Hall measurements performed on the AlN/GaN structures showed sheet carrier densities of 0.98×10^{13} cm^{-2}, which was used to simulate the MISFET. The lower than expected electron density may be due to the very thin unpassivated AlN layer which contributes to a reduction in 2DEG density due to a high surface barrier height [3-12]. The significant lattice mismatch between AlN and GaN might lead to formation of a large number of interface electron traps which results in a reduction of the effective polarization charge. A negative polarization charge of the same magnitude was placed at the unpassivated AlN surface for modeling the surface potential. From test simulations, a Schottky barrier height of 2.65 eV for AlN was found to be the closest approximation for the experimentally obtained DC results for the devices reported in this work.

A HEMT of the same dimensions, with a 24nm $Al_{0.32}Ga_{0.68}N$ barrier layer was also simulated. Based on Hall measurements, a charge of 1.09×10^{13} cm^{-2} was introduced at the AlGaN/GaN interface and a negative charge of the same magnitude was placed at the AlGaN surface. The Schottky barrier height of the AlGaN/GaN HEMT gate was estimated to be 1.59 eV based on observations that the barrier height increases by approximately 0.02 eV from that of a metal/GaN contact for a 1% increase in the Al mole fraction [3-13]. The effect of interface traps and other non-idealities were not considered. Fig. 3.22 shows the simulated conduction and valance band profile and sheet carrier density for AlN/GaN MISFETs and AlGaN/GaN HEMTs.

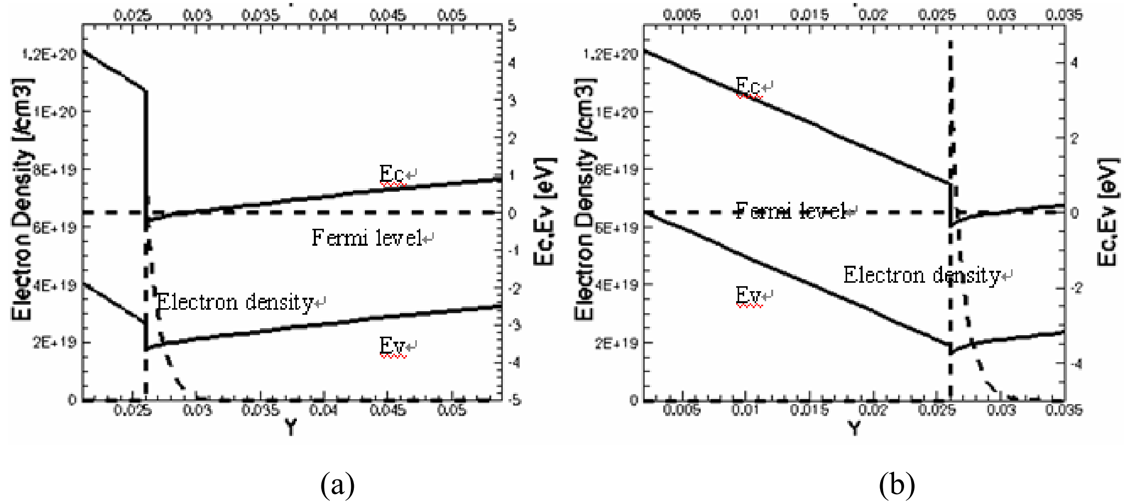
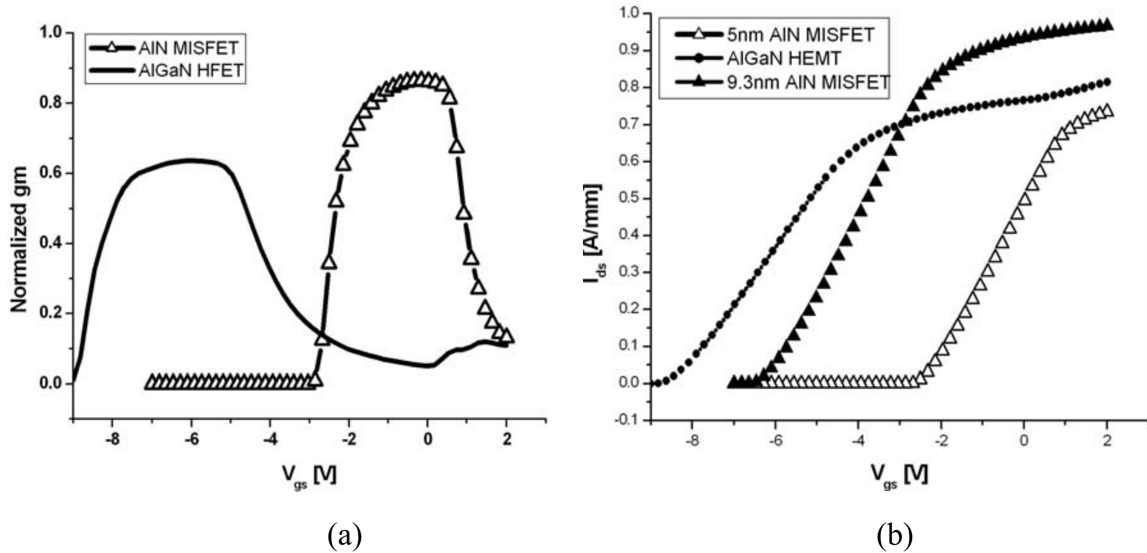


Figure 3-22: Simulated conduction and valence band profile and sheet carrier density of (a) AlN/GaN MISFET and (b) AlGaN/GaN HFET at zero-bias

Fig. 3.23 shows simulated normalized transconductance for the 5 nm AlN MISFET and the 24 nm $Al_{0.32}Ga_{0.68}N$ HEMT. The depletion of the barrier layer at zero bias is larger in the case of AlN since its higher bandgap results in a larger effective Schottky voltage at the gate. Along with the stronger 2DEG modulation due to its thinner barrier layer, the MISFET shows a 30% higher transconductance and consequently better high-frequency performance. As can be seen in Fig. 3.24, simulation of I_{GS}-V_{GS} characteristics shows that the higher Schottky voltage of the MISFET also provides for several orders lower gate leakage current. This is in favor of the AlN/GaN MISFET design for high-power applications. Since non-idealities were not taken into account, the I_{GS}-V_{GS} curves obtained from simulation show a much lower reverse gate leakage than that measured experimentally. However, based on the overall trends observed, AlN/GaN MISFET have significantly better characteristics than AlGaN HEMTs in terms of lower leakage and higher gate breakdown.



(a) (b)

Figure 3-23: (a) Simulated normalized transconductance of the 5 nm AlN layer MISFET and 24 nm $Al_{0.32}Ga_{0.68}N$ HEMT and (b) Simulated I_{DS}-V_{DS} curves of 5 nm AlN layer MISFET, 24 nm layer $Al_{0.32}Ga_{0.68}N$ HEMT and 9.3 nm AlN layer MISFET at V_{DS} 5V

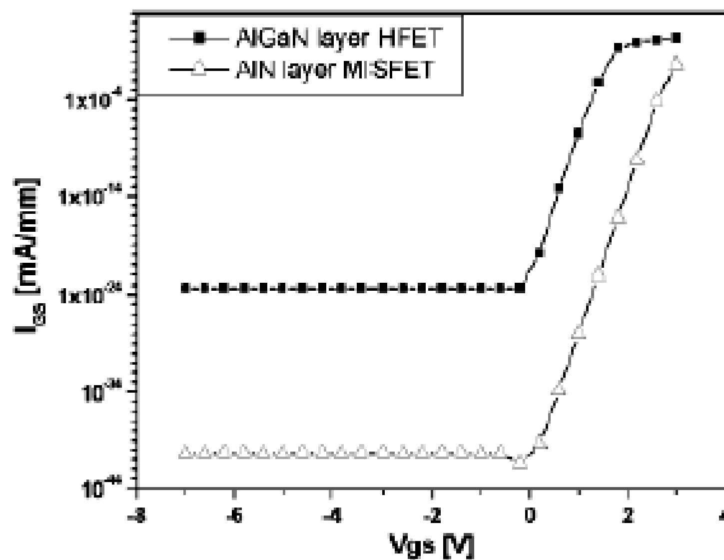


Figure 3-24: Simulated gate diode characteristics of MISFET and HEMT

The simulated peak I_{DS} for the 5 nm AlN/GaN MISFET is seen to be lower compared to the HEMT due to the 2DEG proximity to the device surface and resulting depletion effects. Hall measurements on a passivated 5 nm AlN/GaN MISFET sample

showed an increase in the sheet carrier density. The effect of surface states is also mitigated for a thicker AlN barrier layer resulting in a higher drain current. Fig. 3.23 (b) shows the simulation result for a MISFET of the same dimensions with 9.3 nm thick AlN layer. From Hall measurements, a charge of 1.58×10^{13} cm^{-2} was placed at the AlGaN/GaN interface with a corresponding charge at the surface. The peak I_{DS} is observed to be higher compared to the 24 nm $Al_{0.32}Ga_{0.68}N$/GaN HEMT.

3.4 Summary

Using commercial device simulation tools, MEDICI and ISE-TCAD, GaN-based HFETs were simulated based on the drift-diffusion model. Drift diffusion simulations are adequate for gate lengths down to 100 nanometer. DC and high frequency performance of non-recessed and recessed gate AlGaN/GaN HEMTs were first investigated using a simplified polarization model in MEDICI. Three types of Double-heterojunction HEMTs using InGaN channel were also designed and simulated.

AlN/GaN MISFETs and AlGaN/GaN HEMTs were simulated using the ISE-TCAD simulator. The parameters used and the simulation conditions applied were shown. Measured data such as ohmic contact properties and sheet carrier density are essential for simulating the device under realistic conditions. 5 nm barrier layer thickness AlN/GaN MISFETs and 24 nm $Al_{0.32}Ga_{0.68}N$/GaN HEMTs were simulated and compared using drift diffusion simulation. The advantages of AlN/GaN MISFET were shown by simulation in terms of DC characteristics.

CHAPTER 4

III-Nitride HFETs Fabrication Technology

4.1 Introduction

In this chapter, the fabrication process of III-Nitride based MISFETs and HEMTs is described. Process optimization is necessary to fully utilize the high potential of the III-Nitride based HFETs. AlGaN/GaN HEMTs and AlN/GaN MISFETs basically necessitate the same device processing technology. This includes MESA (active area of the device) etching for device isolation, lithography and metal deposition, metal contact annealing for ohmic contact formation, device passivation with dielectrics such as Si_3N_4 and an airbridge process. In general, the device process steps are quite similar to the traditional semiconductor processes of GaAs technology. However, due to the intrinsic material hardness of GaN, the etching process is more challenging and the annealing temperature is normally over 800 ºC which is much higher than the temperature used for GaAs ohmic contact annealing (~ 400 ºC). Handling of the device is easier than GaAs based heterostructure devices because GaN is normally grown on mechanically strong substrates such as SiC or sapphire.

In the following sections, the challenges and optimization of the process technology for GaN based HFETs are described.

Process	Description
Dicing & Wafer cleaning	2 inch wafer is diced into pieces of the multi-reticle chip size. Solvent cleaning with xyline, methanol, acetone and isopropanol is followed. Then acid cleaning is performed by mixture of phosphoric acid and sulfuric acid.
MESA etching	MESA area is patterned with photolithography and the photoresist is hard baked for improving hardness for withstanding dry etching. Cl_2 based chemical reaction based dry etching or Ar based mechanical dry etching is followed. Etching depth is around 200~350 nm for HEMTs and MISFETs.
Ohmic contact	Ohmic patterns are defined with photolithography or electron beam lithography. Ti/Al/Ti/Au metallization using e-beam evaporator is followed. After lift-off process, The sample is annealed at 850 ºC for 30 sec with Rapid Thermal Annealing (RTA) for ohmic formation.
Schottky contact	Schottky gates are patterned by optical lithography for 1 µm gate or by e-beam lithography for submicron gate. Ni/Au or Ni/Ti/Au metallization is followed by lift off.
Interconnect layer	The interconnect layer necessary for microwave probe measurements is defined by optical lithography. Thick Ti/Al/Ti/Au layer deposition is done by electron beam evaporator.
Airbridge formation	Two step optical lithography is used for defining the pillar and airbridge areas. Ti/Au/Ti seed layer is deposited and Au electro plating is followed. Airbridge release is the last step.

Table 4-1: Brief descriptions of III-Nitride FET processes

4.2 III-Nitride based HFETs Process

III-Nitride HFET processes of the group of Professor Pavlidis were developed in the mid 1990's and optimized in this thesis work. Table 4.1 shows the related process flow. The following sections describe detailed description of each process.

4.2.1 MESA isolation with dry etching

Dry etching process is required for device isolation. The active area remaining after dry etching is called MESA. For isolating individual AlGaN/GaN HEMTs and AlN/GaN MISFETs from the other devices on the same wafer, the etched area should be deeper than the 2DEG channel where conductivity is very high. Normally more than 200 nm of the active layer are etched in order to increase the resistance between the active areas of the neighboring devices for better isolation. However if etching depth (also referred to as MESA height) is more than 350 nm, gate leakage increases due to poor gate metal step coverage at the edge of the MESA area existing between the gate pad and the gate metal deposited on the active area (on the MESA). Therefore precise control of the dry etching depth is crucial for device isolation and gate leakage reduction.

GaN and AlN have very strong banding energy between atoms which is 8.9 eV and 11.5 eV respectively [4-1]. Therefore Nitride-based materials are not easily etched by chemicals, but UV-assisted chemical etching is often used. However this technique is complex and requires additional steps of processing. Reactive Ion Etching (RIE) is mostly used for etching process or GaN and is primarily Cl_2 based plasma etching such as CCl_2F_2/Ar or Cl_2/Ar plasma. Ar-based mechanical plasma etching is also used in GaN process.

The etching process starts with cleaning; the wafer is cleaned with hot xyline for 3 minutes, and is followed by normal methanol cleaning for 1 minute, hot acetone cleaning for 3 minutes and 1 minute isopropanol cleaning. After this, acid cleaning with H_2SO_4:H_3PO_4:H_2O and HCl:H_2O is followed. The substrates are then spin coated by Photoresist AZ1518 or AZ4533 and soft bake follows for 1 minute on 90 ºC hotplate. Using a MESA mask and photolithography, the photoresist is patterned after exposure and development. Hard baking of photoresist is required for higher photoresist's hardness during ion etching process and shaping of the photoresist edge so that a smooth transition and better step coverage can be obtained. The thickness of photoresist after hardbaking should be more than twice of the etching depth target. After etching, the etching depth should be checked. Etching process is continued until the target etching thickness is achieved.

4.2.2 Ohmic process

Good ohmic contact formation is necessary to utilize the full potential of AlGaN/GaN HEMTs and AlN/GaN MISFETs, since it ensures a good interface of the intrinsic device to the outside world. Ohmic contact formation on GaN is more difficult than on conventional semiconductor materials like GaAs or Si because of GaN's wide bandgap and low diffusivity [4-2]. The ohmic contact quality can be characterized by the Transmission Line Measurement (TLM) method which provides information on contact resistance (R_c), sheet resistance (R_s) and specific contact resistivity (R_{sc}). R_c is dependent on metallization type and process used such as annealing. R_s is a more material dependent resistance parameter, which is not highly affected by contact quality. R_{sc} is a normalized

contact resistance per unit area. All three values should be as small as possible but there are limitations due to the metallization scheme used, process optimization and epitaxial layer quality. In this work, the ohmic contact value considered characteristic of good ohmic contacts on GaN is defined by $R_c < 1\ \Omega\cdot mm$, $R_s < 1000\ \Omega/square$ and $R_{sc} < 1\times10^{-5}\ \Omega\cdot cm^2$.

For ohmic contact metallization, a Ti/Al/Ti/Au stack of metals is used. As can be seen in Table 4.2, Ti has a low metal work function which is required for good ohmic contact with high probability of tunneling. Also Ti can be melted and diffused into GaN by high temperature annealing around 800 ºC and forms an inter-metallic compound TiN_x which creates a high doping level within a thin layer below the metal contact [4.3]. Ti has good adhesion properties on semiconductor materials and was therefore chosen as the first layer of the metallization.

As a second layer, Al is used since it forms an Al_3Ti interlayer, which has better conductivity and is less reactive to air. A relatively thick Au layer is used on top of the metallization since it protects the metal layer below. Between Au and Al, a Ti layer is inserted in order to block the Au layer to be diffused into the Al layer or even down to the Ti layer. Ni, Pt, or Mo can be also used as intermediate layer.

The ohmic metallization process starts also with cleaning of the sample because the hard baked photoresist used in MESA etching process can leave residuals on the substrate. A photolithography process including photoresist spinning, softbaking, UV exposure and development defines the ohmic contact area. Just before metal evaporation, the surface of GaN layers is chemically processed using buffered HF in order to remove thin oxidized layers like Ga_xO_y. Using an electron beam evaporator, a Ti/Al/Ti/Au metallization is

deposited. After lifting off the metal with acetone soaking, the sample is subjected to be annealed by Rapid Thermal Annealing (RTA). A two step temperature annealing is used in this process which involves 550 ºC annealing for stabilization followed by annealing at 850 ºC. Resistances usually achieved with this process are R_c = 0.5 Ω·mm, R_s = 600 Ω/square and $R_{sc} = 0.5\times10^{-5}$ Ω·cm^2.

Metal	Metal work function	Contact behavior
Aluminum (Al)	4.28	Ohmic
Titanium (Ti)	4.30	Ohmic
Chromium (Cr)	4.50	Slight rectifying
Tungsten (W)	4.55	Slight rectifying
Molybdenum (Mo)	4.60	Slight rectifying
Silver (Ag)	4.26	Schottky
Gold (Au)	5.10	Schottky
Nickel (Ni)	5.15	Schottky
Platinum (Pt)	5.65	Schottky

Table 4-2: Metal work function and characteristics of contact with n-GaN [4-4]

4.2.3 Gate process; optical lithography

For AlN/GaN MISFETs and AlGaN/GaN HEMTs, the Schottky gate process by optical contact lithography is most challenging and important, due to the wavelength of the UV light used and light diffraction. A minimum 1 μm opening of the photoresist

could be obtained. This opening was found to be the same as the gate length,. Sub micron gates of ~ 100 nm length can only be achieved by electron beam lithography. In our process, Ni is used as a Schottky contact metal. As can be seen in Table 4.2, Pt is also a good candidate for Schottky contacts, but stable and repeatable contact formation was difficult to obtain due to the high melting point of Pt comparing with Ni.

As a first demonstration of the device, optical lithography is preferred since the process is not demanding in equipment such as e-beam lithography machine. AZ1512HS (HS: High Sensitive) photoresist was used for this purpose since it provides around 1 μm thickness of photoresist after spinning and soft baking. For better lift off, which is more challenging for small photoresist openings, chlorobenzol soak is performed. Chlorobenzol soak changes the chemical hardness of the surface of photoresist so that the surface is slowly developed compared with photoresist near the semiconductor surface. Therefore an overhang of the photoresist is achieved and the lift off process becomes easier. However chlorobenzol is not a recommended chemical to use and therefore extreme care is required in handling it. A 1 μm gate process with stable and repeatable characteristics could be obtained following several tests and optimizations. Fig. 4.1 shows the 1 μm gate lithography results on AlGaN/GaN HEMT wafers and Fig 4.2 show the SEM picture of the processed gate.

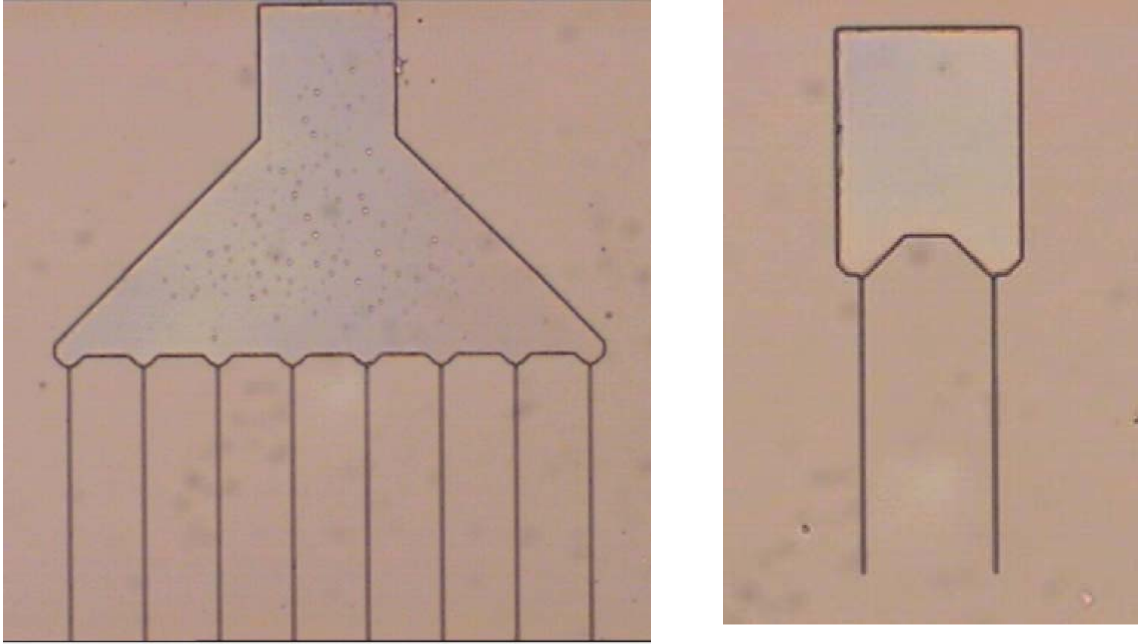


Figure 4-1: Photograph of developed optical 1 μm gate opening.

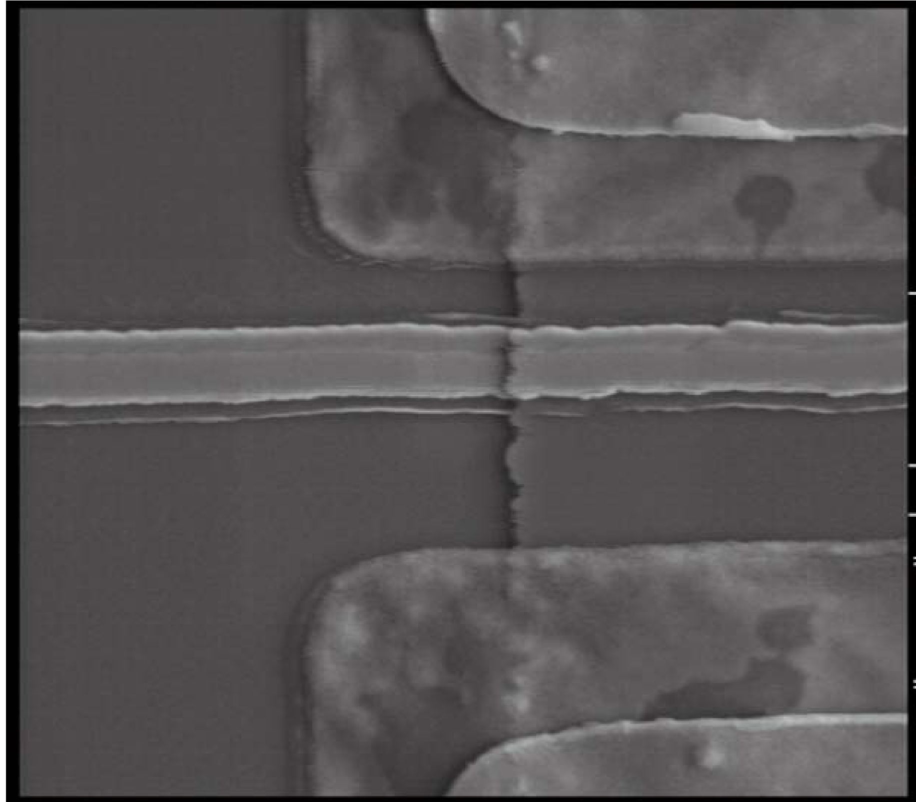


Figure 4-2: SEM image of optical gate with 1 μm gate length.

4.2.4 Gate process; electron beam lithography

The optical lithography has a limit of gate length around 1 μm due to the light diffraction and relatively large wavelength of UV light. In order to achieve sub-micron gate lengths in the range of 100 nm to 200 nm, electron beam (e-beam) lithography, where an electron beam permits patterning of a photoresist layer, is necessary. This process is maskless and very small structures of 50 nm can be achieved. The e-beam process of GaN-based HFETs described here was performed at the Institute of Electronics, Microelectronics and Nanotechnology (IEMN), Lille, France. The e-beam system used was an EBPG 5000 Plus from Leica, which has an electron acceleration voltage of 50 KeV.

Fig. 4.3 shows the two-layer resist process used in submicron T-gate process of the AlN/GaN MISFETs and AlGaN/GaN HEMTs. Further details for the processing steps are given in Table 4.3. The actual gate length was equal to the size of the gate footprint, which is defined by the high resolution and low sensitive resist (PMMA 950K). In order to reduce gate resistance, a gate head region is defined by the low resolution and high sensitive resist (PMMA-MAA). Two separate doses were used for gate foot and gate head definition.

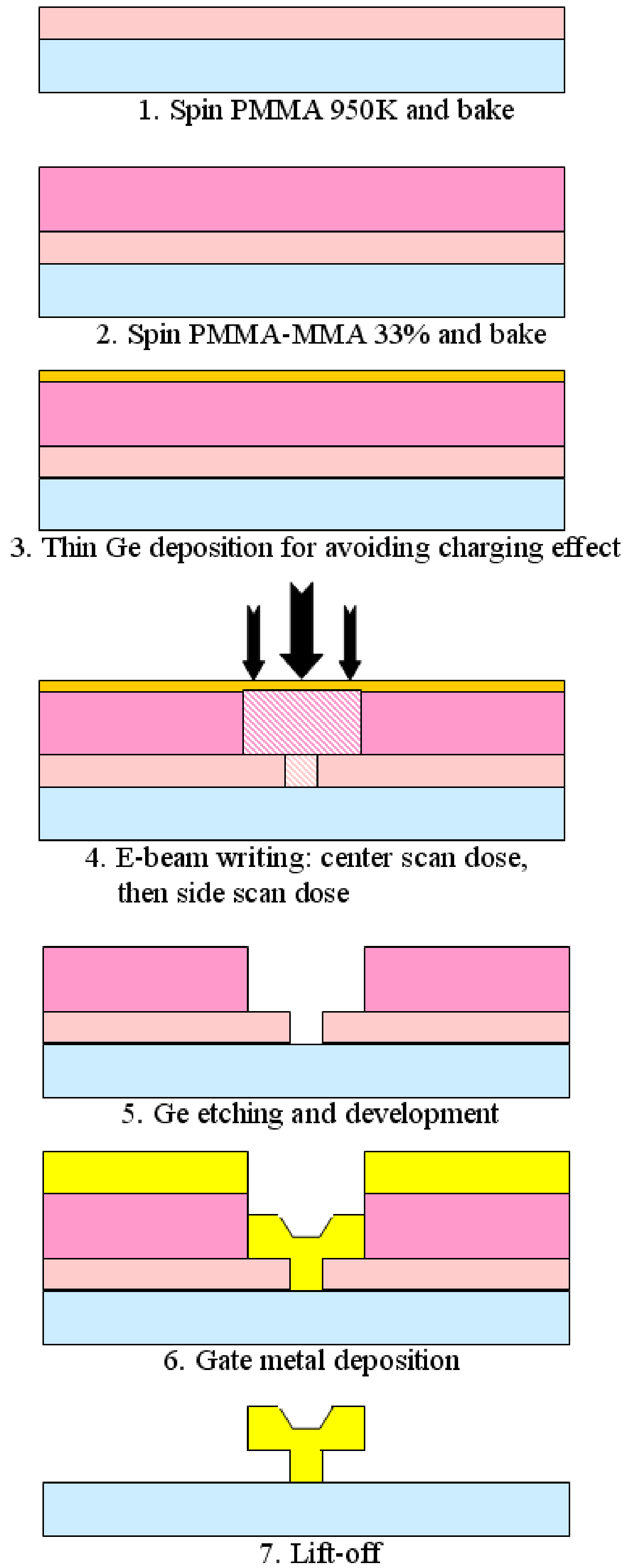


Figure 4-3: Two layer (PMMA/PMMA-MMA) resist process for sub micron T-gate

Process steps	Step description	Comments
1. PMMA 950K	-spin at high speed > 3000 rpm: 100 ~ 200 nm - Two step bake on hot plate and oven	- for gate footprint
2. PMMA-MAA	-spin at low speed < 3000 rpm - Two step bake on hot plate and oven	- for gate head
3. Ge deposition	- very thin conductive layer deposition	for avoiding electron charging effect on sapphire substrate
4. E-beam writing	- Two dose step process with a higher dose for gate footprint compared with gate head	Two separate doses for size control of gate foot and gate head.
5. Development	- Conductive layer etching - MIBK:IPA soak for development then IPA rinse	Develop both resist at the same time
6. Metal evaporation	- Ni/Ti/Au metal deposition by e-beam evaporator	
7. Lift-off	- PMMA remover soak - Rinse with acetone and IPA	

Table 4-3: Bi-layer PMMA resist process for sub-micron T-gate process

Before e-beam exposure, a thin conductive layer was deposited in order to avoid electron charging effects in the sapphire substrate, which is non-conductive. After e-beam writing, this layer was first etched away and then the sample was soaked in MIBK:IPA solution for development. Fig. 4.4 shows the SEM image of developed resist.

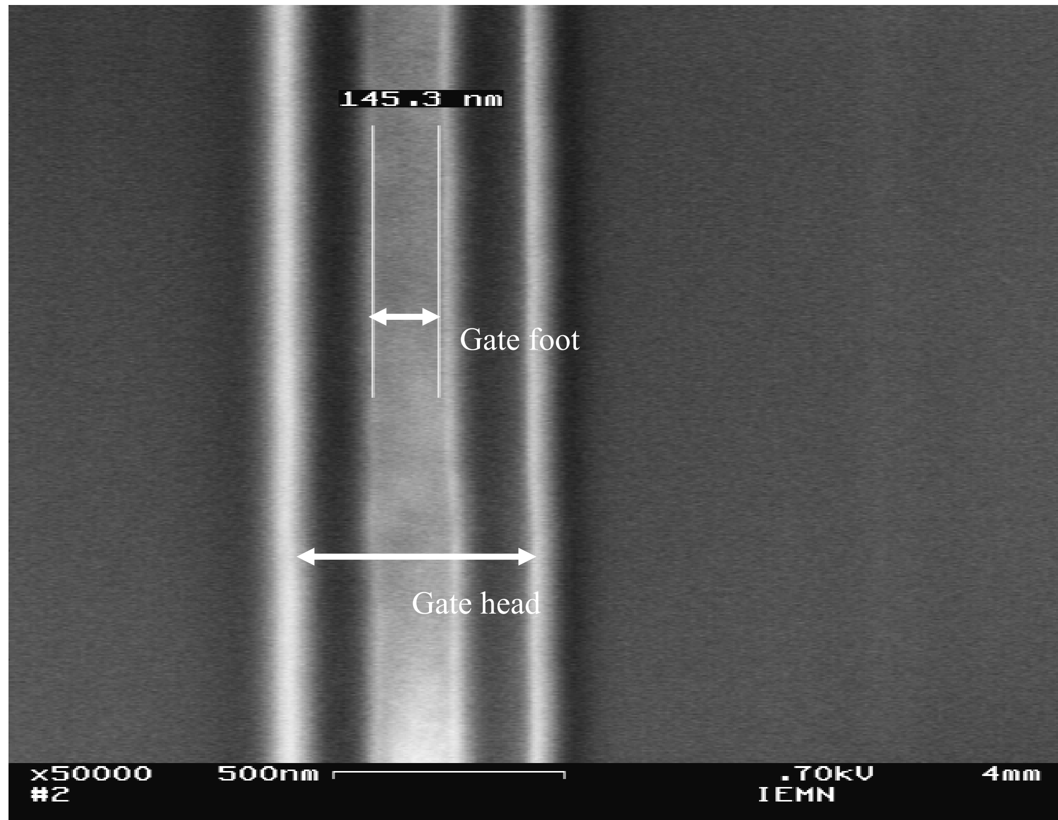


Figure 4-4: SEM image of the developed resist for 150 nm T-gate (Courtesy of IEMN).

After development, a Ni/Ti/Au gate metal was deposited by e-beam evaporation. Lift-off with was then followed. Fig. 4-5 and 4-6 show the SEM image of the processed sub-micron T-gate on GaN-based HFETs with 150 nm and 250 nm gate length respectively..

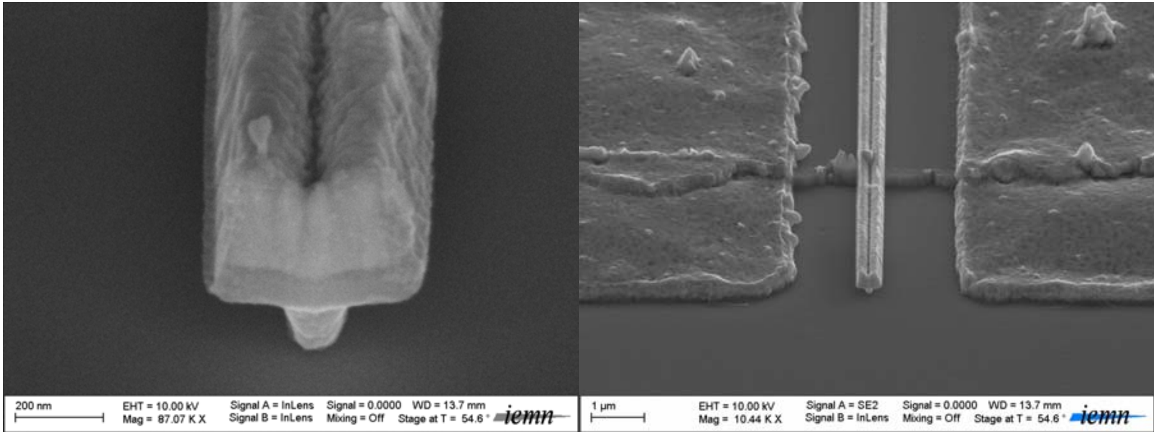


Figure 4-5: SEM images of the 150 nm T-gate on GaN-based HFETs (Courtesy of IEMN)

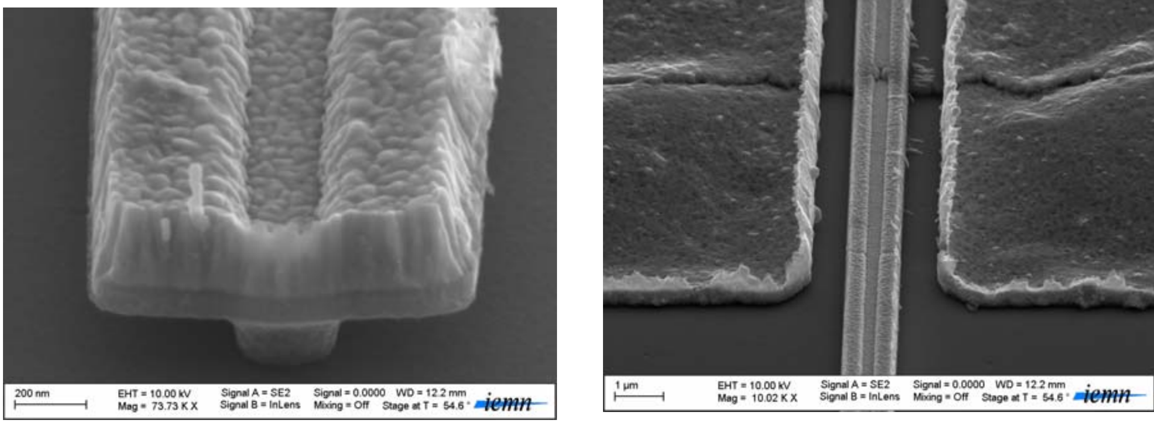


Figure 4-6: SEM images of the 250 nm T-gate on GaN-based HFETs (Courtesy of IEMN)

4.2.5 Airbridge process

In order to obtain higher output current i.e. higher power, the device size should be increased. For microwave devices when the gate width becomes larger, the gate periphery may approach the wavelength of the high frequency signal under which the device is excited. Individual gate widths of the order of 300 μm are not therefore appropriate for X-band or higher frequency operation. Therefore, multiple gate designs such as 4- or 6-fingers or even more are needed. With the multi-finger gate approach, the gate width can be increased by increasing the number of gate fingers. The inner source pads between

gates should in this case be connected to the outside source and this can be achieved with the help of airbridges having a 'pillar' contacting the source, while the 'airbridge' itself connects the pillars to other device parts or circuit transmission lines. The airbridge process starts with photolithography of the pillar area. A seed layer of Ti/Au/Ti metallization is then deposited by e-beam evaporation and a photolithography step is used for defining the airbridge area. The top Ti layer of the seed layer is etched by BHF just before gold plating. A gold bath is used for electroplating and achieving 4~5 μm thick airbridges. At last, the airbridge is released by removing the photoresist seed layers. An example of a typical airbridge realized in this way is shown in the SEM photograph of Fig. 4.7.

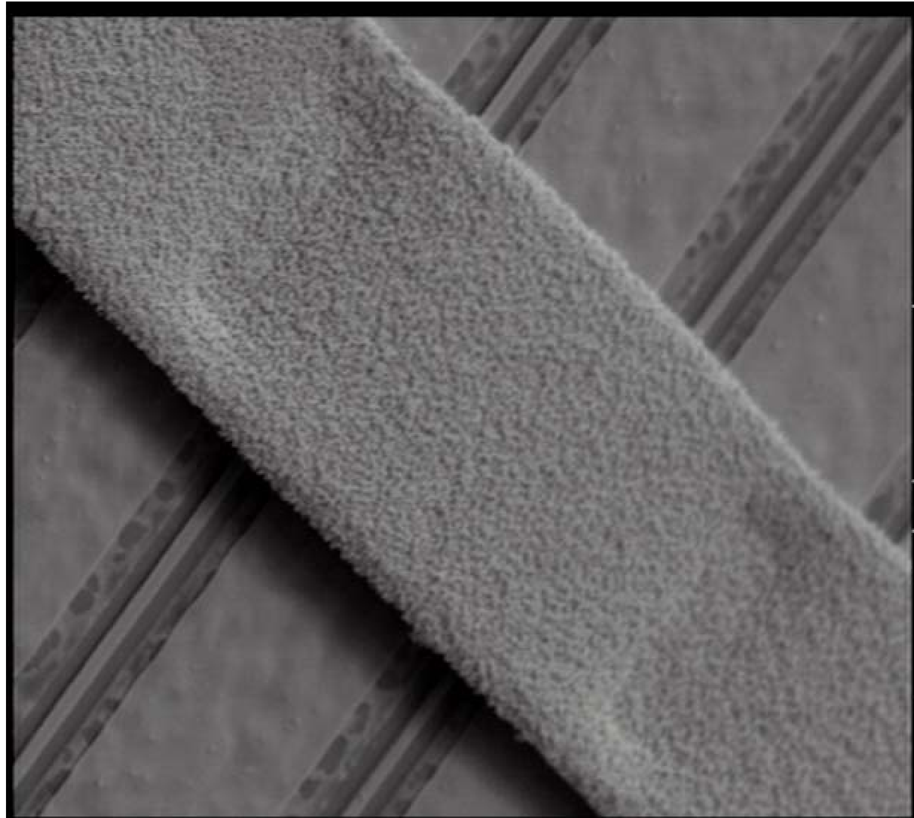


Figure 4-7: SEM image of the fabricated Airbridge of AlGaN/GaN HEMT

4.3 Advanced Process Technology for AlN/GaN MISFETs

AlN/GaN MISFETs have special technology needs for ohmic contact formation. Because of the very wide bandgap of AlN (AlN: 6.2 eV and GaN: 3.4 eV) and native oxide of AlN surface, it is extremely difficult to obtain a good ohmic contact on AlN directly and special process optimization is required. In this section, the technology development needed for AlN/GaN MISFET ohmic contact formation is described.

4.3.1 AlN wet etching

The AlN/GaN MISFET structure was grown on Sapphire (Al_2O_3) substrate by in house Metal Organic Chemical Vapor Deposition (MOCVD). The epi-layers consisted of an AlN buffer, 2 μm unintentionally doped (UID) GaN layer and 5 nm UID AlN barrier layer. The growth temperature of AlN layer was 1050 °C and the reactor pressure was 50 Torr. The flow rate of TMAl and NH_3 for AlN layer was 5 and 150 sccm respectively. The growth rate of AlN layer was 1.1 nm/min. In case of ohmic contacts formed directly on the AlN barrier layer of the AlN/GaN MISFET, the electrical characteristics are severely influenced by the resulting high contact resistance. To circumvent this problem in the devices of this work, the AlN layer was selectively etched in the region of ohmic contacts. Ideally it is preferred to leave a 1 ~ 2 nm AlN barrier layer in the ohmic region in order to maintain a 2DEG under the ohmic contact electrode. Then, electrons can tunnel though thin AlN layer and be introduced in the high carrier concentration 2DEG channel. However it is difficult to control the AlN chemical etching since the etching rate is highly dependent on the AlN layer quality, chemical etchant solution and temperature. Measuring precisely the AlN layer thickness in nanometer scale is also challenging. In works by other groups, H. Kawai et. al. [4-5] etched 4 nm thick AlN barrier layer with an

alkaline solution. The wafer was then reloaded in the reactor and 0.5 μm thick GaN layer was regrown selectively. However, this regrowth technique could induce thermal stress in the materials due to the high regrowth temperature. T. Ide et. al. [4-6] used hot phosphoric acid wet chemical etching of the AlN barrier layer to selectively remove from GaN. For phosphoric acid, temperature is between 170 and 210°C, only the AlN layer can be selectively etched. Using this method, it was possible to obtain relatively good contact resistance of 0.72 Ω mm and the contact resistivity of 8.25×10^{-6} Ω cm^2. This work showed that it is possible to obtain good ohmic contact after entirely removing the AlN layer on ohmic contact area.

Wet etching of AlN is preferred because Reactive Ion Etching can damage the GaN surface while it is difficult to etch AlN selectively film without etching GaN. Instead of hot phosphoric acid, a KOH solution [4-7] and an AZ400K developer [4-8] were investigated for AlN crystal film etching. From their study, AZ400K developer etches AlN films grown on sapphire substrate with an etching rate of ~ 6 nm / min at around 60°C. Therefore, Instead of the commonly employed hot phosphoric acid for etching the AlN layer, a 65°C AZ400K developer diluted in DI water was used due to process simplicity and safety considerations.

4.3.2 Hall test for AlN etching

The AlN/GaN MISFET structure has a 2DEG channel of high mobility (μ) and carrier concentration (N_s) just below the AlN layer. The μ, N_s parameters can be evaluated directly by Hall measurements. If the AlN layer is etched totally, the 2DEG will disappear and mobility will be drastically decreased. Therefore, with increasing time of etching, one can estimate the etching of the AlN layer. 2 inch MOCVD grown wafers with 5 nm thick

Condition	Mobility (cm^2/Vs)	Carrier conc. (cm^{-2})
No treatment	901	0.98×10^{13}
30 sec BHF soak	711.3	1.14×10^{13}
+ 1 min BHF soak	824.3	1.05×10^{13}
+ 5 min AZ400K 20°C soak	558	1.31×10^{13}
+ 5 min AZ400K 65°C soak	747	0.90×10^{13}
+ 15 min AZ400K 65°C soak	252	-

Table 4-4: Hall measurement results on 5 nm AlN layer MISFET sample

AlN layer were diced in 5 mm × 5 mm square samples. Indium contacts were made on the four edges and then annealed at 250 °C for 10 minutes for ohmic contact formation. Hall measurements were done before etching and after etch etching steps. First, in order to make sure that AlN layers are not etched by buffered HF (BHF), the sample was immersed in to BHF for 30 second followed by 1 minute and then Hall measurement was performed. Table 4.4 shows the results.

As can be seen, mobility and carrier concentration was not changed much with 1.5 min BHF soaking. This ensures that AlN layer is not etched at all during Si_3N_4 etching by BHF for etch mask patterning. Additionally AZ400K developer at room temperature for 5 minutes did not show drastic changes. However, after total 20 minutes AZ400K 65°C soak, the mobility decreased to 252 cm^2/Vs. The results show the 5 nm AlN layer was totally etched by between 10 minutes and 25 minutes,. Instead of using pure AZ400K for etching AlN, it is better to use AZ400K solution (AZ400K and D.I water mixture). This reduces the etching rate and it is therefore easier to control etching of AlN layer. In order

to evaluate the etching rate of AlN by the developer solution, the same 5 nm AlN sample was immersed in 65°C AZ400K developer solution repeatedly at various time intervals. Hall measurements were performed after every immersion. As can be seen in Fig. 4.8, after 25 minutes of etching, the Hall mobility drastically decreases to ~ 300 cm^2/Vs, which is the corresponding bulk GaN mobility. The AlN barrier layer was in this case totally etched and the 2DEG disappeared. The 2DEG density also decreased with increasing etching time and this can be explained by the increased effect of surface charge due to the decrease of AlN barrier thickness.

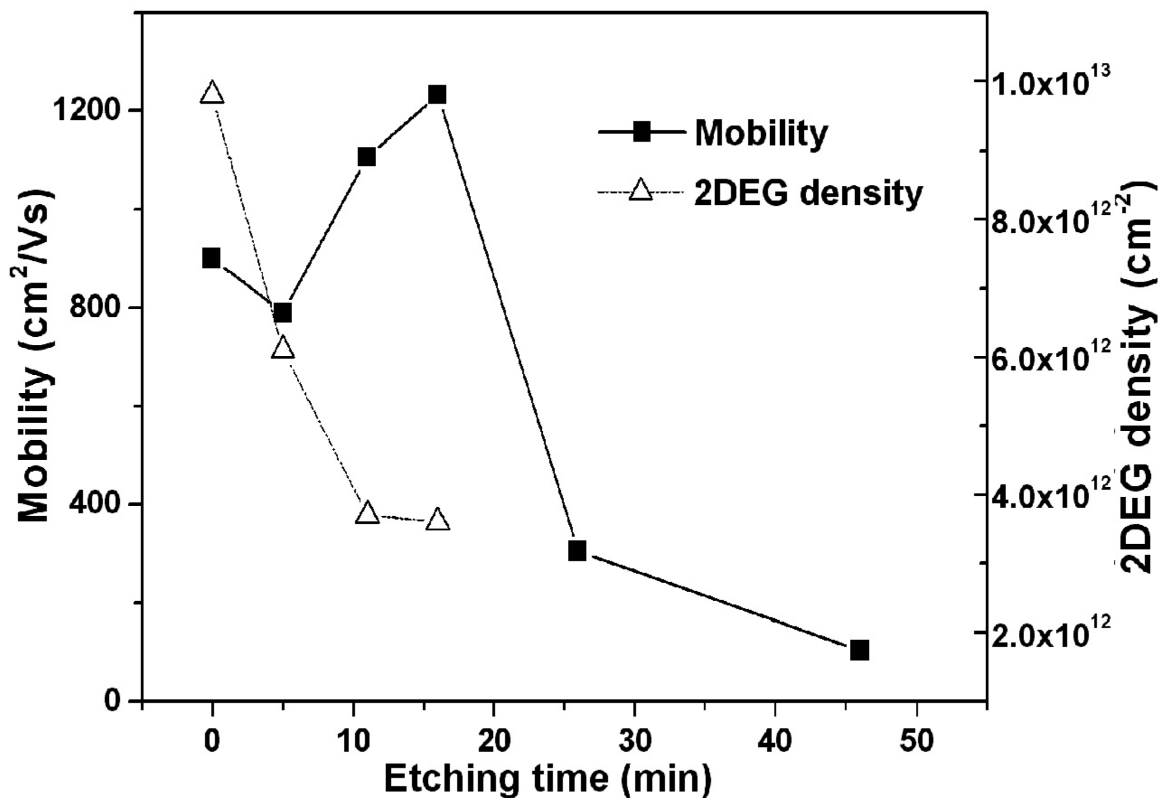


Figure 4-8: Experimentally determined mobility and 2DEG density changes due to the AlN etching of a AlN/GaN MISFET (5 nm AlN layer) structure in 65°C AZ400K solution with DI water (1:4)

4.3.3 AlN etching process flow

As mentioned earlier, photoresist is not adequate to be used as etch mask since it is developed or etched with a KOH-based solution like AZ400K solution or phosphoric acid. Therefore, Plasma Enhanced Chemical Vapor Deposition (PECVD) system deposited Si_3N_4 was used as etch mask since Si_3N_4 can not be easily etched by a KOH-based solution and can be patterned using BHF etching. Fig. 4.9 shows the processing steps of AlN etching and ohmic contact formation. Two different thickness of Si_3N_4 layers (500 Å and 1000 Å) were deposited on 2 inch silicon wafer for testing and AlN/GaN MISFET samples. From the thickness measurements, the etching rate of Si_3N_4 was found to be higher than 3 Å per minute. This type of dielectric layers was therefore found to be stable for AZ400K soaking up to 2 hours.

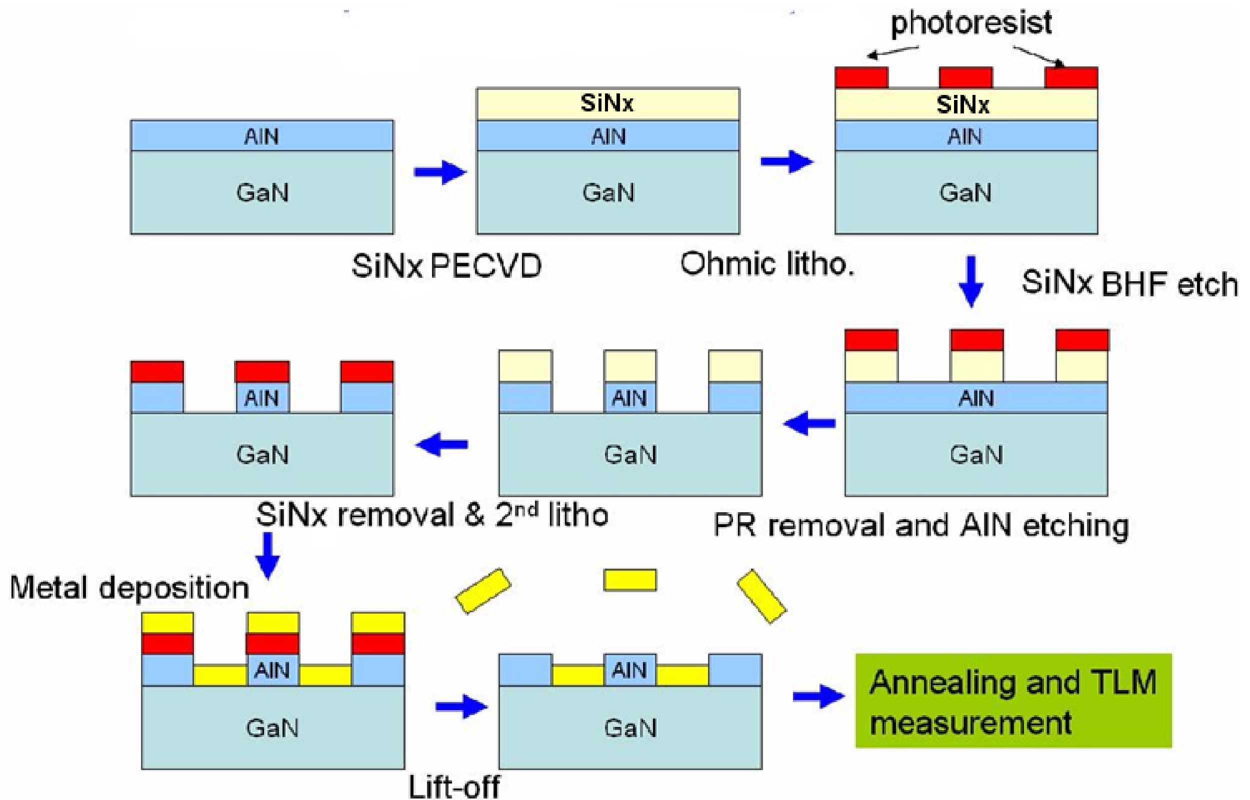


Figure 4-9**:** AlN etching process steps

Based on the above results of silicon wafer, AlN/GaN MISFET samples with 500 Å and 1000 Å Si_3N_4 were patterned with photoresist for ohmic contact formation. BHF etching of Si_3N_4 layer was done over 40 seconds for the 500 Å sample and 140 seconds for 1000 Å. Etching time for 1000 Å was increased from 90 seconds to 140 seconds.

PECVD deposited Si_3N_4 was found to be suitable as an etch mask for AlN etching in a 65°C AZ400K solution. Based on the results obtained from the etching study, AlN/GaN MISFETs were fabricated. MESA formation was done using Reactive Ion Etching for device isolation. Then, a 50 nm thick Si_3N_4 dielectric layer was deposited using PECVD and the dielectric layer was patterned by means of a photolithography and wet etching step in order to obtain a suitable etch mask. The AlN barrier layer in the source and drain ohmic contact areas was etched by AZ400K solution (1:4 DI water) at 65 °C. After removing the remaining dielectric layers, ohmic contact metals Ti/Al/Ti/Au (30/120/30/300 nm) were deposited by electron beam evaporation, followed by lift off and rapid thermal annealing at 850 °C for 30 seconds in N_2 environment. TLM measurements showed that the ohmic contact quality had a contact resistance R_C of 1.75 Ω·mm, a specific contact resistivity ρ_c of 1.14×10^{-4} Ω·cm^2 and a sheet resistance R_s of 569 Ω/□. The specific contact resistivity was about one order higher than that of conventional AlGaN/GaN HEMTs and this may be partly due to the etching of AlN in ohmic contact areas which resulted in removing the 2DEG below. Then Ni/Ti/Au (75/25/250 nm) gate metal was deposited by electron beam evaporation. Fig. 4.10 shows the photograph of a processed AlN/GaN MISFET.

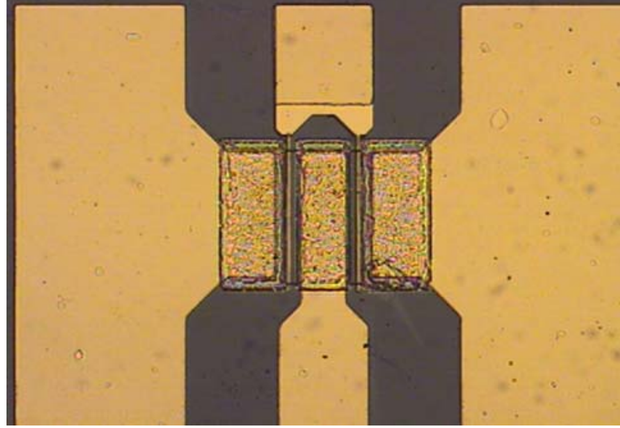


Figure 4-10: Microscopic image of the fabricated AlN/GaN MISFETs

4.3.4 *In-situ* Si_3N_4 deposition for high quality ohmic contact on AlN/GaN MISFETs

As mentioned in chapter 2, *in-situ* Si_3N_4 on AlN/GaN MISFETs has several advantages due to the surface protection from oxidation and process damages. Oxidized AlN is a main obstacle for obtaining high quality ohmic contacts. In the originally developed AlN/GaN MISFET process, the AlN layers were totally etched away at the time of the wet etching process step leading in inferior ohmic contact quality compared with AlGaN/GaN HEMTs. The main reason of relatively poor ohmic contact quality is (see Fig. 4.11 (a)), the lack of direct connection between ohmic metal and the 2DEG channel since the AlN/GaN heterostructure is no longer present due to the AlN etching under the ohmic contact. This is an inherent drawback of AlN/GaN MISFETs, which limits the demonstration of their full potential.

To address this problem, *in-situ* Si_3N_4/AlN/GaN MISFETs were studied where AlN oxidation is well prevented, since there is no air-exposure of the AlN layer. As can be seen in Fig. 4.11 (b), the ohmic contact directly the 2DEG and therefore the overall ohmic contact quality is improved. An additional effect present in this technology is the

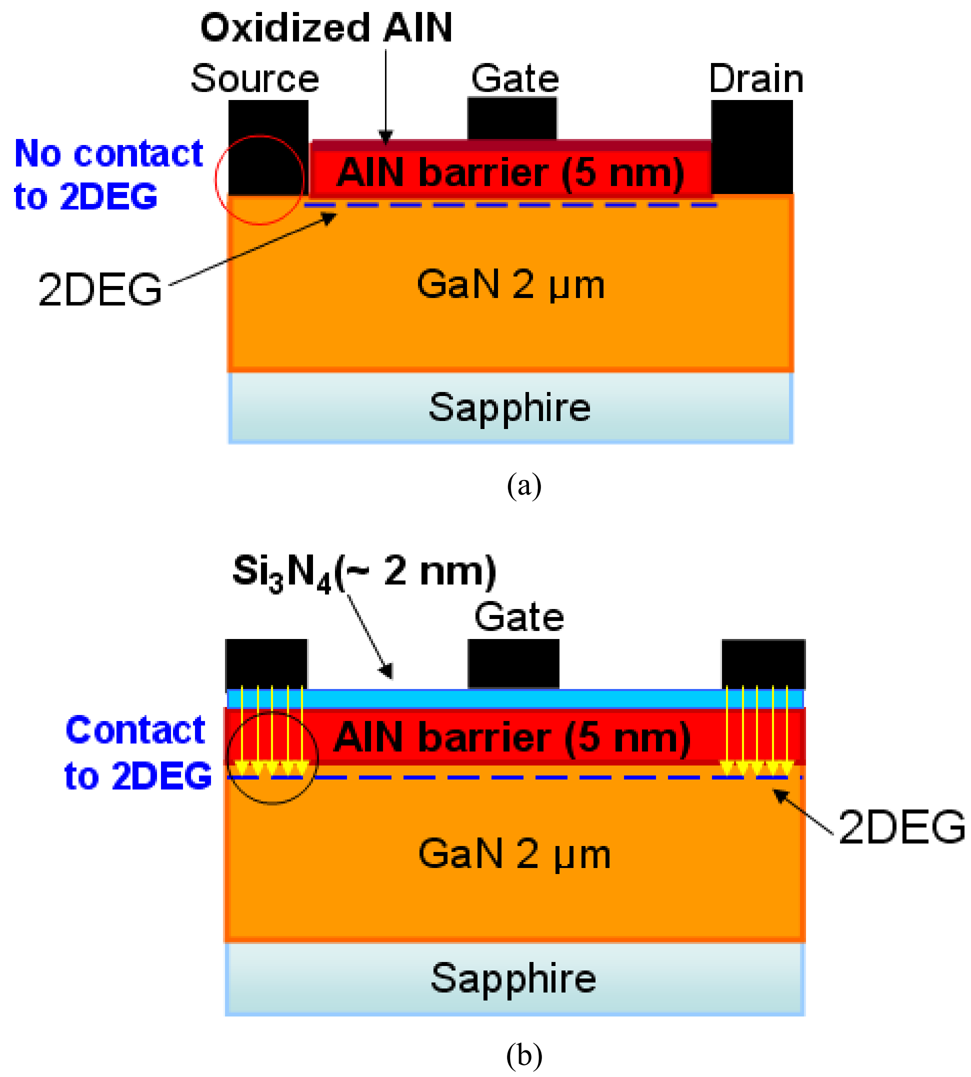


Figure 4-11: Schematics of (a) AlN/GaN MISFETs and (b) *in-situ* Si_3N_4/AlN/GaN MISFETs.

	Contact resistance R_c (Ω mm)	Contact resistivity ρ_{sc} (Ω cm^2)
AlN/GaN MISFETs	1.75	1.14×10^{-4}
in-situ Si_3N_4/AlN/GaN MISFETs	0.55	1.36×10^{-5}

Table 4-5: Ohmic quality of AlN/GaN MISFETs and *in-situ* Si_3N_4/AlN/GaN MISFETs

light AlN layer doping by silicon during *in-situ* Si_3N_4 deposition which helps improving the ohmic quality.

For the ohmic process of *in-situ* Si_3N_4/AlN/GaN MISFETs, Ti/Al/Ti/Au (30/120/30/300 nm) was deposited by electron beam evaporation, and followed by lift off and rapid thermal annealing at 850 °C for 30 seconds in N_2 environments; this is the same ohmic process used for AlN/GaN MISFETs without AlN etching. TLM measurements showed that the ohmic contact quality had a contact resistance R_C of 0.55 Ω·mm, a specific contact resistivity ρ_c of 1.36×10^{-5} $\Omega \cdot cm^2$ and a sheet resistance R_s of 445 Ω/□. The ohmic contact results obtained for AlN/GaN MISFETs are compared in Table 4.5. For *in-situ* Si_3N_4/AlN/GaN MISFETs, the contact resistance was found to decrease by about one third and the contact resistivity decreased by almost one order of the magnitude comparing with the contact resistivity of AlN/GaN MISFETs.

4.4 Summary

In this chapter, the fabrication process developed for III-Nitride FETs was described. MESA isolation, ohmic contact formation, Schottky gate metallization and airbridge processes were reviewed in detail. Due to the inherent material characteristics of GaN, mesa etching process for device isolation and ohmic contact formation in the source and drain region are complicated and difficult. Dry etching process with Cl_2 based plasma ion etching is generally used for stable and repeatable GaN MESA etching. For ohmic contact formation, Ti/Al/Ti/Au metallization was used due to the low metal work function and good diffusivity of Ti. 1 μm gate process using optical contact lithography was established. Sub-micron gate process with bi-layer resist process permitted the fabrication

of reliable T-shaped submicron gate down to 150 nm. The airbridge process was described in section 4.2.5. In section 4.3, the special technology needs of AlN/GaN MISFET process were explained especially with emphasis on ohmic contact optimization. Tests of Si_3N_4 dielectric layer as an etching mask for AlN etching were described. AlN etching by KOH solution at 65ºC and ohmic contact formation on the etched area enabled to achieve a specific contact resistance of 1.14×10^{-4} Ωcm^2. This contact value is still high comparing with ohmic contact results on AlGaN/GaN HEMT and requires further optimization of ohmic metal composition and/or annealing temperature. *In-situ* grown Si_3N_4 AlN/GaN MISFETs showed improved ohmic contact quality over AlN/GaN MISFETs with AlN etching. This was possible due to the inherent advantage of i*n-situ* Si_3N_4 deposition on AlN; absence of AlN oxidation and AlN doping with silicon.

The developed processes were used for fabricating III-Nitride MISFETs successfully. The measurement results of the fabricated devices are described in chapter 5.

CHAPTER 5
Experimental Results of III-Nitride MISFETs

5.1 Introduction

There are several characterization techniques for microwave semiconductor devices. Each technique has its own purpose and different characteristics of the device can be measured and analyzed. For III-Nitride MISFETs, there are several characterization methods including DC, Capacitance-Voltage (CV), pulsed I-V measurement, noise measurement, S-parameter measurement, load pull measurement and etc. In this chapter, key measurement techniques for high power and high frequency applications were performed on in-house fabricated III-Nitride MISFETs; they are DC, pulsed, S-parameter and large signal measurements. DC measurements are the most basic measurement technique which provides information on I_{DS}-V_{DS}, transfer characteristics, transconductance, gate leakage and breakdown voltage. Using pulse measurement techniques, self-heating effect can be removed due to isothermal characteristics of the pulsed signal. Also, a trap related study is useful since the pulse time width can be shorter than pulse trapping and de-trapping response time and therefore trapping effects can be removed. S-parameter measurements are essential for characterizing high frequency properties of the device and provide data for small signal modeling. Load pull measurements allow evaluation of power characteristics of the device such as maximum output power, power gain and Power Added Efficiency (PAE). With two tone (two

different frequency input power signal) load pull measurements, the linearity of the device can be characterized.

In the following sections, DC, pulsed, S-parameter, and large signal measurements on III-Nitride MISFETs are described.

5.2 DC Characteristics of III-Nitride MISFETs

DC measurements were performed on AlN/GaN MISFETs using an Agilent 4145B semiconductor analyzer and a Keithley 2602 source meter. The Agilent 4145B has a current compliance of 100 mA and its use was therefore limited to small size devices. In contrast, Keithley 2602 has a current compliance up to 3 A [5-1] and was used for larger gate periphery devices. Devices were tested with a wafer probe station and contacted with Ground Signal Ground (GSG) microwave probes. All measurements were performed at room temperature.

5.2.1 DC characteristics of AlN/GaN MISFET

DC measurements were performed on in house fabricated AlN/GaN MISFETs which are designed as shown in Fig. 5.1. The ohmic contact characteristics were evaluated and further processing of the wafers to the gate interconnect and airbridge levels was continued depending on ohmic contact quality. As can be seen in Table 5.1, the processed MISFET devices have relatively good ohmic quality with contact resistivity values in the range of 10^{-4} Ωcm^2. In house fabricated AlGaN/GaN HEMTs have contact resistivity in the range of 10^{-5} Ωcm^2; this value is close to that reported in case of state of the art AlGaN/GaN HEMT devices. Ohmic quality improvement was achieved by *in-situ* Si_3N_4 deposition on AlN layer as explained in chapter 4. 1 µm optical gates with Ni/Ti/Au

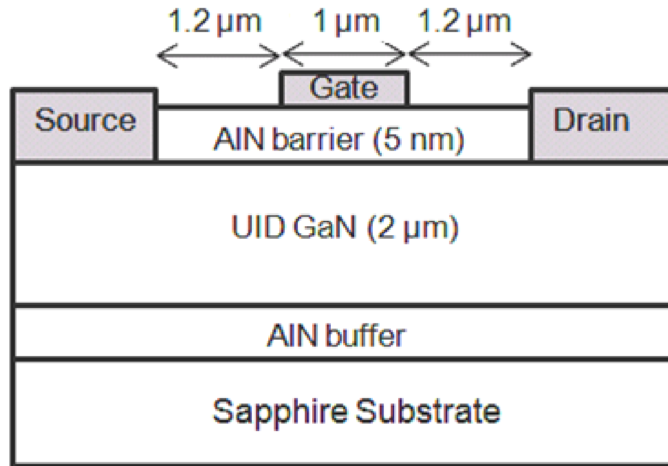
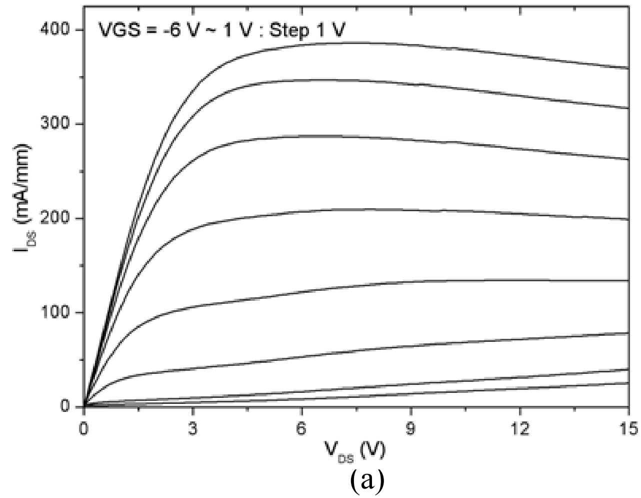


Figure 5-1: Schematic cross section of AlN/GaN MISFETs

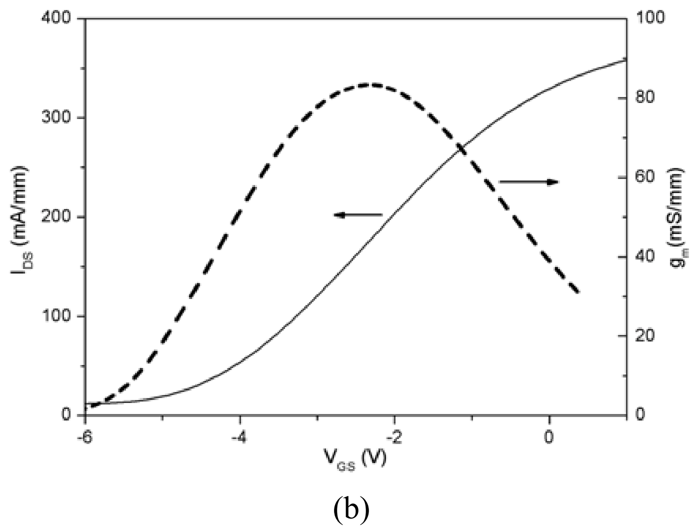
Contact resistance R_c	Sheet Resistance R_s	Specific R_{sc}	I_{max} at 25 V
1.75 Ω mm	569 Ω/sq	$1.14 \times 10^{-4} \Omega cm^2$	43 mA

Table 5-1: TLM measurement results for 5 nm AlN/GaN MISFET

metallization were then defined and DC measurements were performed under room temperature conditions with a Keithley 2602 source meter. Fig. 5.2 shows DC characteristics of a 2 finger Pi-shaped gate MISFET with 100 µm gate width and 3× offset; the distance between the gate and drain edge was in this case three times larger than the gate to source distance. The I_{DS}-V_{DS} curves of Fig. 5.2 (a) allowed evaluation of MISFET characteristics such as knee voltage (transition between the linear and saturation region), on-resistance, maximum current and self-heating. The transconductance g_m shown in Fig. 5.2 (b) is a figure of merit for MISFETs; the higher $g_{m,}$ the larger will be the gain that the transistor can achieve. It is calculated from the derivative of I_{DS}-V_{GS} curves at fixed V_{DS} and is expressed in Siemens. In addition, the threshold voltage (V_{th}) can be measured with the help of I_{DS}-V_{GS} curves and was estimated from Fig. 5.2 to be -6.2 V.



(a)



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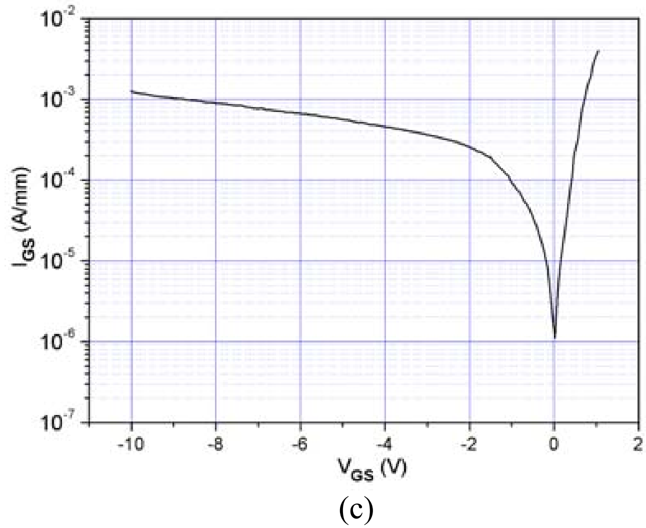


(c)

Figure 5-2: DC characteristics of AlN/GaN MISFET; (a) I_{DS} vs. V_{DS}, (b) I_{DS} & transconductance (g_m) vs. V_{GS} at V_{DS} = 5V and (c) I_{GS} vs. V_{GS}

The DC data described above are generally normalized to the gate width and the corresponding values are given in A/mm, S/mm. The gate leakage current I_{GS}-V_{GS} curve in Fig. 5.2 (c) was measured with floating drain bias. High gate leakage current values increase the static power consumption and therefore reduce the efficiency of the device. The Power Added Efficiency (PAE) of the AlN/GaN MISFETs was found to be rather low (~ 25 %) as will be shown in section 5.5. Normally AlGaN/GaN HEMTs with low gate leakage have a PAE of more than 40%. Therefore, the AlN/GaN MISFETs has relatively high gate leakage. However, the high gate leakage was reduced by *in-situ* Si_3N_4 deposition technique and the reduced gate leakage will be shown in section 5.2.2

As can be seen in Fig. 5.2 (a), for I_{DS}-V_{DS} characteristics, the gate and drain voltage varied from -6 V to 1 V and from 0 V to 15 V respectively. The device exhibited a peak current density of ~ 380 mA/mm at V_{GS} = 1 V. The AlN/GaN MISFET did not pinch-off completely due to the modest resistivity GaN buffer or the presence of high density states at the AlN/GaN interface, which restrict the current flow even in the depleted gate region. In Fig. 5.2 (b), the threshold voltage V_{TH} is about -6 V and the peak extrinsic transconductance was ~ 85 mS/mm. This is lower than the expected value due to the presence of high contact resistance; the intrinsic transconductance was found to be 120 mS/mm. The gate leakage current (I_{GS}) was measured versus V_{GS} and was found to be in the order of 10^{-4} A/mm at reverse V_{GS} of -10 V and 10^{-3} A/mm at V_{GS} = 1 V as shown in Fig. 5.2 (c).

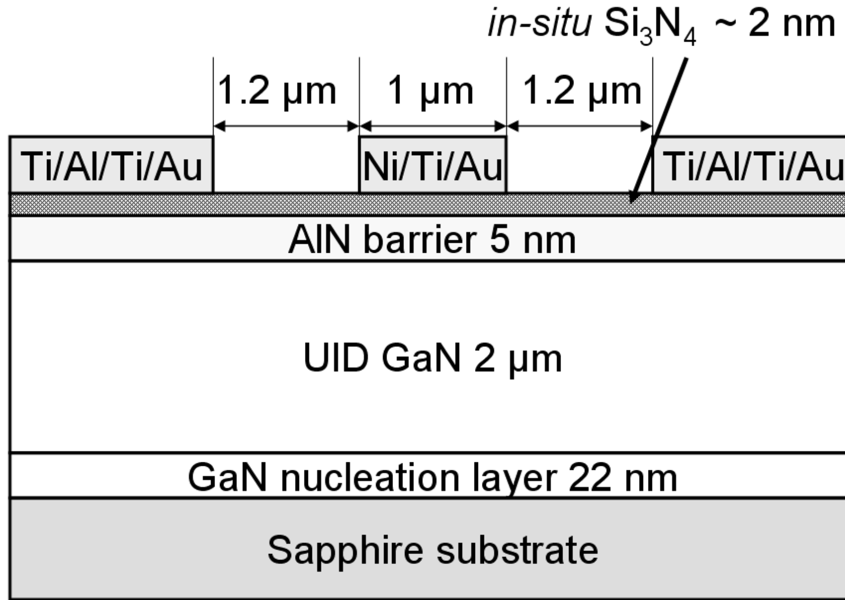
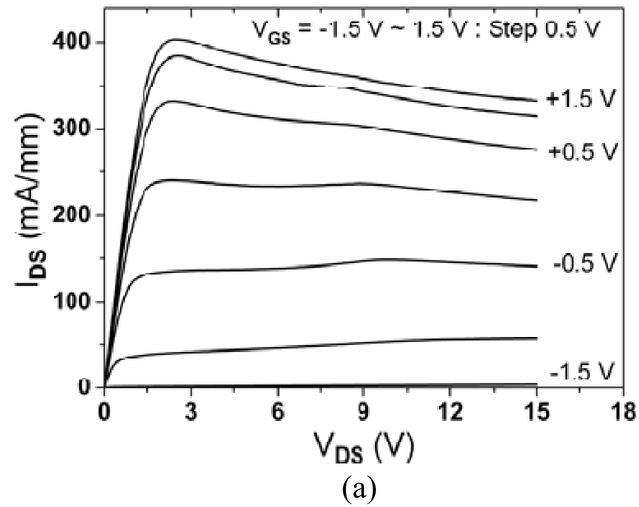


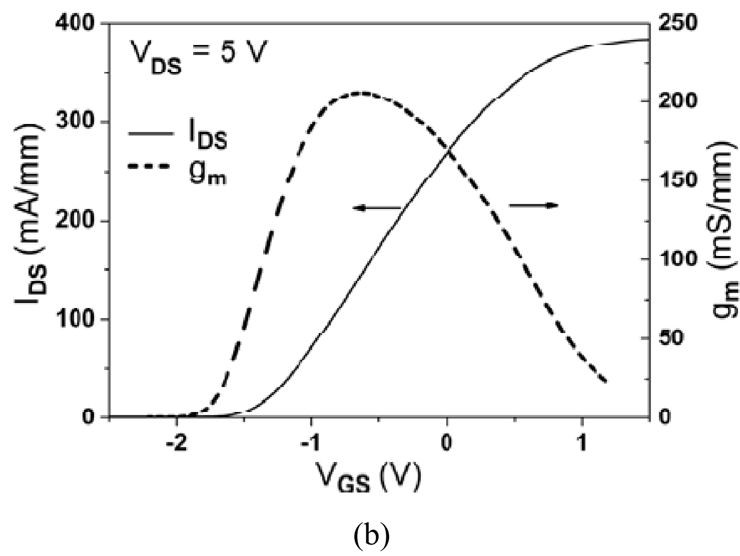
Figure 5-3: Schematic cross-section of AlN/GaN MISFETs with in-situ deposited Si_3N_4

5.2.2 DC characteristics of *in-situ* Si_3N_4/AlN/GaN MISFET

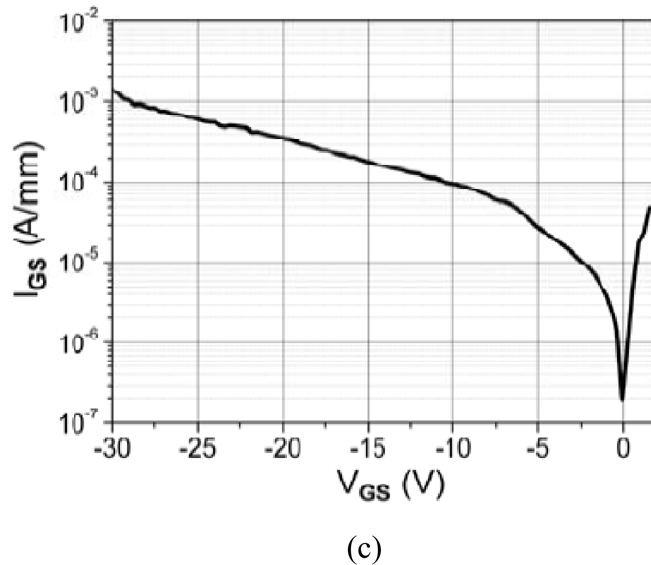
DC characteristics of *in-situ* Si_3N_4/AlN/GaN MISFETs were measured at room temperature. The schematic of the fabricated and measured *in-situ* Si_3N_4/AlN/GaN MISFET is shown in Fig. 5.3. The device designs such as gate length and source to drain distance are exactly the same as for the conventional AlN/GaN MISFETs studied in this work. The device exhibited a peak current density of 403 mA/mm at V_{GS} = 1.5V and the threshold voltage V_{TH} was about -1.5 V as can be seen in Fig. 5.4 (a). The peak extrinsic transconductance g_m was 206 mS/mm at V_{GS} = -0.6 V and V_{DS} = 5 V as can be seen in Fig. 5.4 (b). Gate leakage current density was around 10^{-3} A/mm at reverse V_{GS} of -30 V as can be seen in Fig. 5.4 (c). Overall, AlN/GaN MISFETs with *in-situ* MOCVD deposited Si_3N_4 exhibited greatly improved DC characteristics; increase of g_m by almost a factor of 3 (85 mS/mm to 206 mS/mm), one order of magnitude lower gate leakage current (from ~10^{-2} A/mm to ~10^{-3}A/mm for V_{GS} = -30V)



(a)



(b)



(c)

Figure 5-4: DC characteristics of *in-situ* Si_3N_4/AlN/GaN MISFET; (a) I_{DS} vs. V_{DS}, (b) I_{DS} & transconductance (g_m) vs. V_{GS} at V_{DS} = 5V and (c) I_{GS} vs. V_{GS}

5.3 Pulsed I-V Characteristics of AlN/GaN MISFETs

AlN/GaN MISFETs present strong self heating effects due to their high current density (> 300 mA/mm) independent of gate length and width. These effects are enhanced in case of devices made on sapphire substrate due to the substrate's low thermal conductivity and therefore limitation of heat dissipation. Self-heating may result in negative conductance behavior characteristics as observed under high V_{DS} region in Fig. 5.5. This effect can be minimized by using pulsed I-V biasing, which allows one to ensure isothermal conditions under short pulse conditions.

For the pulsed measurement, the gate and drain were first biased at 0 V and then to a higher value with the help of two synchronized pulses. The two pulses were adjusted through oscilloscope monitoring in order to ensure that the gate and drain pulses are applied to the device exactly at the same time. DC to RF dispersion effects related to material defects and/or surface/interface states can be studied by pulsed IV measurements

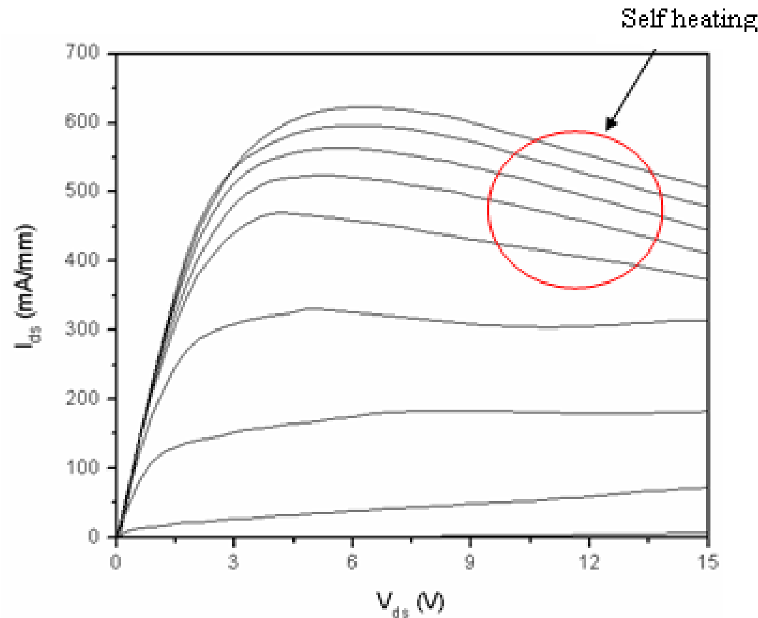


Figure 5-5: Typical DC characteristics of AlN/GaN MISFETs with strong self heating effect

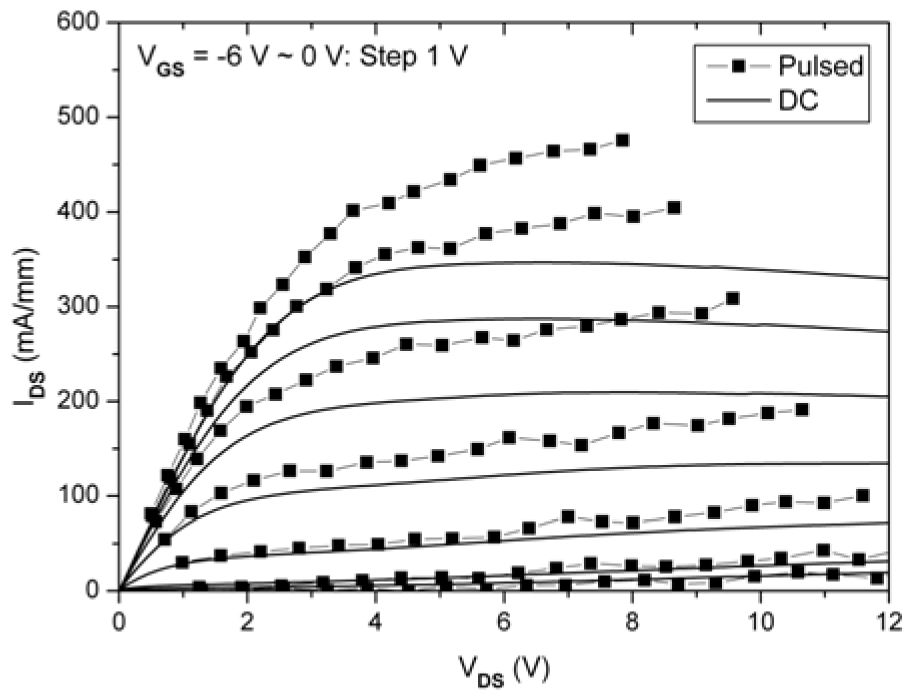


Figure 5-6: Pulsed and DC IV characteristics of 2 × 100 μm AlN/GaN MISFET (quiescent bias point: V_{DS} = 0V, V_{GS} = 0V)

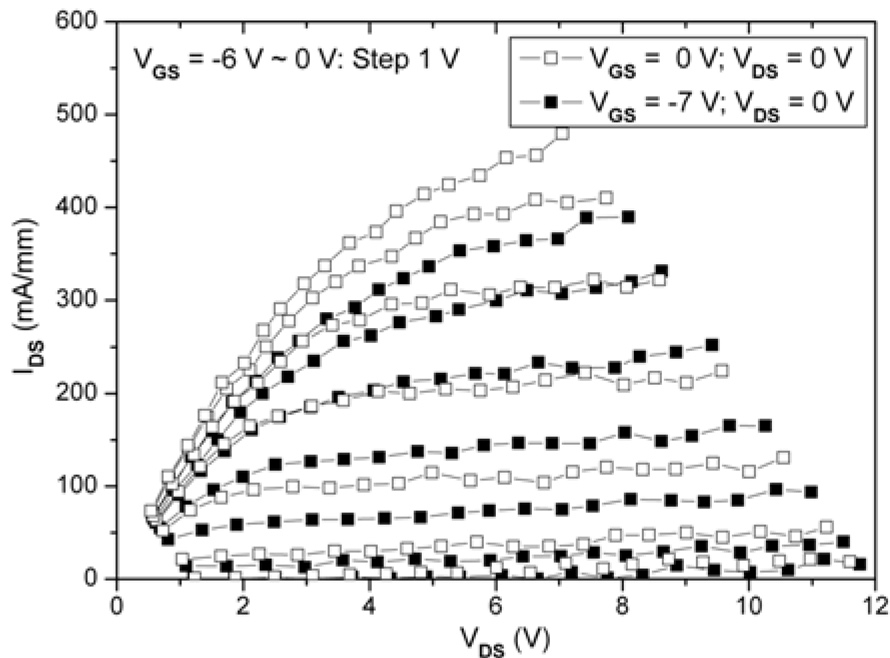


Figure 5-7: Pulsed IV characteristics of 2 × 100 μm AlN/GaN MISFET with 3× gate offset (quiescent bias point: V_{DS} = 0V, V_{GS} = 0V and V_{DS} = 0V, V_{GS} = -7 V) for gate lag measurement.

[5-2]. Moreover, the nature of the trapping effect can be studied by controlling the pulse width to be shorter than the time constant of trapping and de-trapping in surface/interface states and defects.

Pulsed measurements with 500 ns wide pulses were performed on 2 × 100 μm width AlN/GaN MISFETs. Fig. 5.6 shows DC and pulsed I-V characteristics at the quiescent bias point of V_{GS} = 0 V and V_{DS} = 0 V. A current discrepancy of more than 20% was observed between DC and pulsed current implying that there is considerable self-heating due to the low thermal conductivity of the sapphire substrate. Pulsed I-V measurements at different gate bias voltages were also performed on AlN/GaN MISFET with 2 × 100 μm width. As can be seen in Fig. 5.11, current slump up to 20 % was observed due to gate lag. This is associated with the ionized donor states located on the AlN surface between gate and drain [5-3]. The relatively high gate lag effect may be due to the unpassivated surface of gate-drain region and it is expected to be reduced by surface passivation with Si_3N_4 as discussed next.

For comparison, in house fabricated $Al_{0.25}Ga_{0.75}N$ HEMTs with Si_3N_4 passivation were evaluated by pulsed IV measurements to investigate gate lag effect. Fig. 5.8 shows the I_{DS}-V_{DS} characteristics under DC and pulsed IV condition. As can be seen in the Fig. 5.8, drain current collapse was observed due to the self heating and the maximum current was drastically increased. Fig. 5.9 shows pulsed IV measurement characteristics at different gate bias points. Here, the gate is DC biased at a fixed value and the desired voltage pulse is subsequently applied. V_{GS} = 0 V and -3 V were used as bias point and the results are shown in the Fig. 5.9. When the gate is biased at V_{GS} = -3 V, the electrons under the gate are forced into the surface states and trapped. Therefore the trapped

electrons behave as a virtual gate which depletes the 2DEG in the channel below. However, since the devices were passivated with Si_3N_4, most of the surface traps were suppressed. Although the difference between the two conditions is not apparent at V_{GS} = -1 V and 0 V. Current collapse can be observed at V_{GS} = 1 V and 2 V and a knee voltage increases. This indicates that some traps remain present after pulse biasing or bulk defect related traps exist even after surface passivation.

The conventional AlN/GaN MISFETs investigated in this work were not surface passivated and therefore gate lag effects are more severe in our devices than in case of the passivated AlGaN/GaN HEMTs.

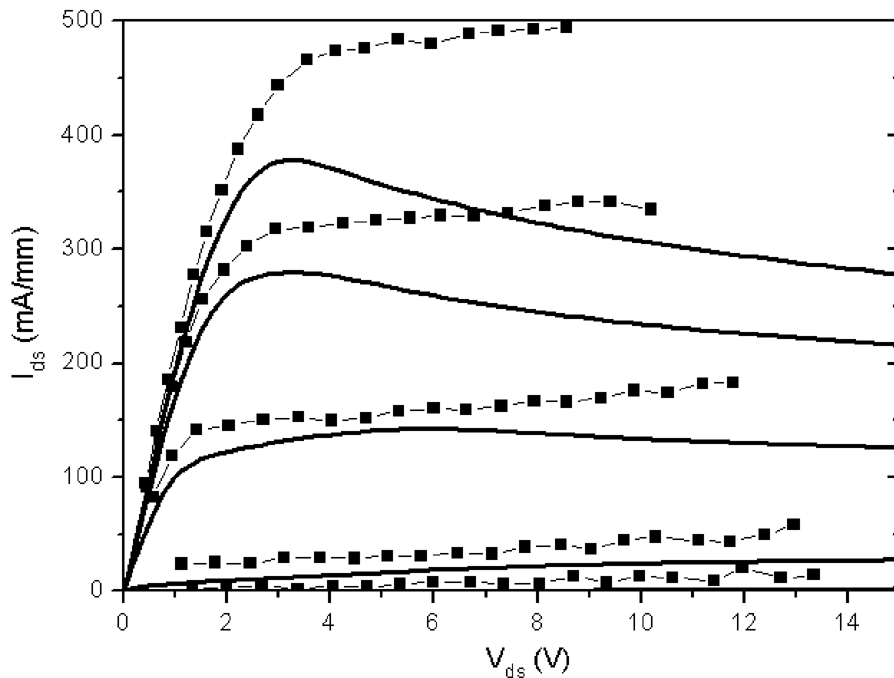


Figure 5-8: DC and pulsed IV characteristics of $Al_{0.25}Ga_{0.75}N$ HEMTs (solid line : DC, square : pulsed IV at V_{GS} = 0V bias), at V_{GS} = -2 ~ 2V (1 V step)

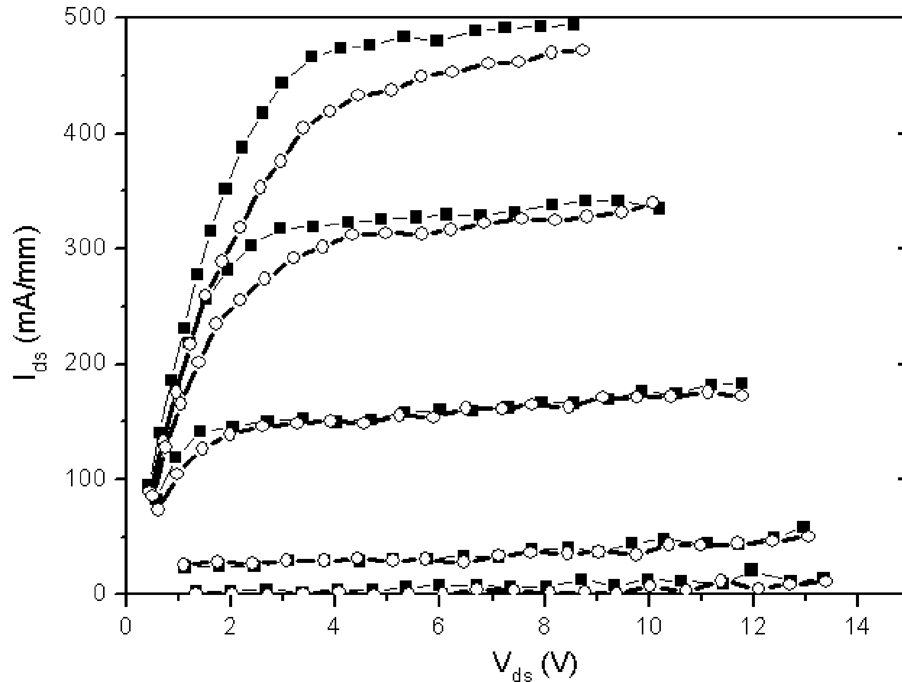


Figure 5-9: Pulsed IV characteristics of $Al_{0.25}Ga_{0.75}N$ HEMTs with different pulse bias conditions (black square: V_{GS} = 0 V, white circle: V_{GS} = -3 V), at V_{GS} = -2 ~ 2 V (1 V step)

5.4 High Frequency Performance of III-Nitride MISFETs

The high frequency performance of microwave devices can be evaluated through S-parameter measurements. Measurements of this type are referred to as small signal due to the relatively small input signal level used for characterization. In this work, an Anritsu 37397C Vector Network Analyzer was used for S-parameter measurements. This VNA has a measurement frequency range of 0.045 GHz ~ 65 GHz and can be extended to 110 GHz using a special module. The devices could be externally biased by means of computer controlled external voltage sources and bias tees and the bias dependence of S-parameters could be measured in this way. There are several useful pieces of information that can be extracted about the device characteristics from S-parameter measurements. Cut off frequency f_T and maximum oscillation frequency f_{max} are two of them

representing important figures of merit concerning the frequency limits of the device.

f_T is defined as the frequency where forward current gain (h_{21}) from hybrid parameters becomes unity and f_{max} is defined as the frequency where unilateral gain (U_g) or maximum stable gain (MSG) becomes unity. H_{21}, U_g and MSG were extracted directly from measured S-parameters by the following equations.

$$H_{21} = \left| \frac{-2S_{21}}{(1-S_{11})\times(2-S_{22})-S_{12}\times S_{21}} \right| \tag{5.1}$$

$$U_g = \frac{|S_{21}|^2}{(1-|S_{11}|^2)\times(1-|S_{22}|^2)} \tag{5.2}$$

$$MSG = \left| \frac{S_{21}}{S_{12}} \right| \times (K \pm \sqrt{K^2-1}) \tag{5.3}$$

where

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2\times|S_{12}|\times|S_{21}|} \tag{5.4}$$

f_T and f_{max} can be also expressed as analytical equations as in (5-5) and (5-6) [5-4]. All terms are small signal equivalent circuit parameters which will be explained in Chapter 6.

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs}+C_{gd}+(R_s+R_d)[g_{ds}(C_{gs}+C_{gd})+g_m C_{gd}]} \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{5-5}$$

$$f_{max} = \frac{f_T}{\sqrt{4g_{ds}(R_{in}+\frac{R_s+R_g}{1+g_m R_s})+\frac{4C_{gd}}{5C_{gs}}(1+\frac{2.5C_{gd}}{C_{gs}})(1+g_m R_s)^2}} \approx f_T\sqrt{\frac{R_{ds}}{4R_{in}}} \tag{5-6}$$

5.4.1 High frequency performance of AlN/GaN MISFETs

AlN/GaN MISFETs were characterized in the small signal regime. Fig. 5.10 shows the typical measured S-parameters of the devices at the bias point V_{GS} = -2 V and V_{DS} = 15 V of 2 finger 2×100 μm AlN/GaN MISFET. The measurement frequency range was from 0.1 GHz to 20.1 GHz. Using the S-parameter measurement data and equations (5-1, 5-2, 5-3, 5-4) the current gain H_{21}, unilateral gain U_g and Maximum Stable Gain (MSG) could be calculated as a function of frequency and are shown in Fig. 5. 11.

Fig. 5.11 shows the small signal characteristics of the same AlN/GaN MISFET device with a bias voltage V_{GS} = -2 V and V_{DS} = 12 V. The f_T and f_{max} can be determined based on this graph; f_T is the frequency value where h_{21} becomes 0 dB and f_{max} is the frequency where U_g or MSG becomes 0 dB. f_T and f_{max} were determined to be 5.83 GHz and 10.58 GHz respectively. The gate bias dependence at fixed drain voltage of 12 V is shown in Fig. 5.12.

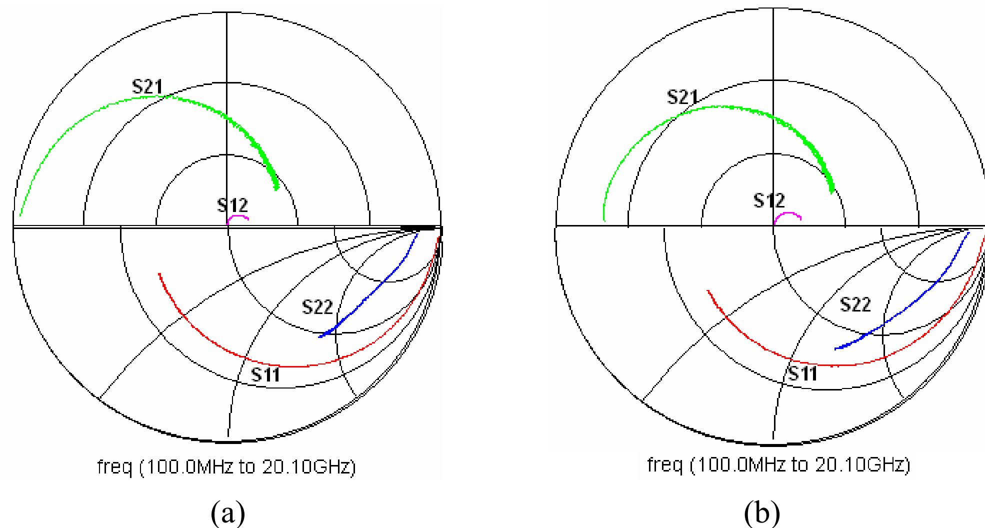


Figure 5-10: S-parameter data for AlN/GaN MISFET from 100 MHz to 20.1 GHz; (a) 2 finger × 100 μm no offset device with high output power (850 mW/mm) (b) 4 finger × 50 μm device with (420 mW/mm); Both at the bias point of V_{GS} = -2 V and V_{DS} = 10 V

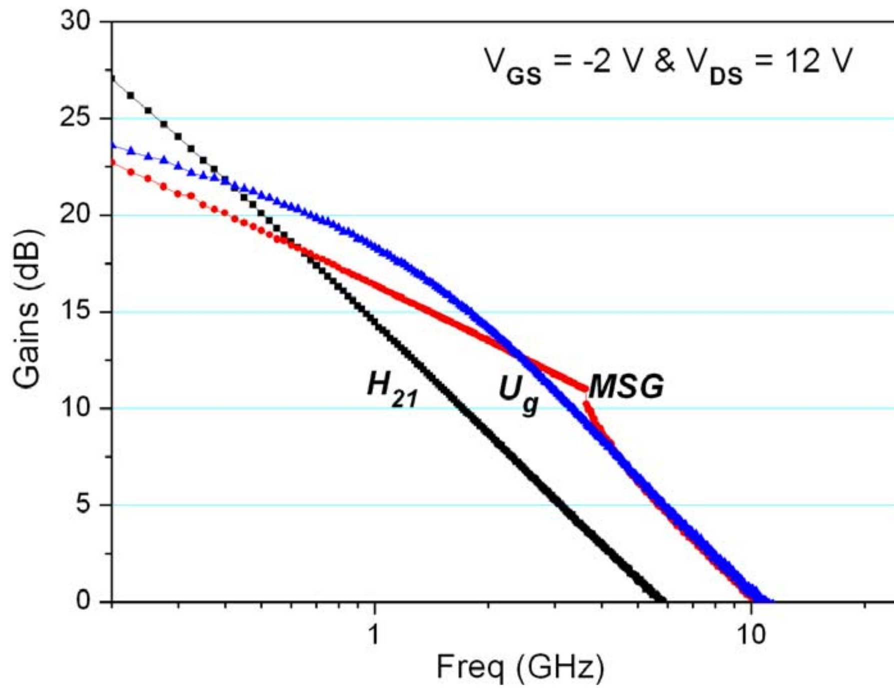


Figure 5-11: Current gain (H21), Maximum available gain (Ug) and Maximum stable gain (MSG) over frequency for AlN/GaN MISFETs at V_{GS} = -2V and V_{DS} = 12V

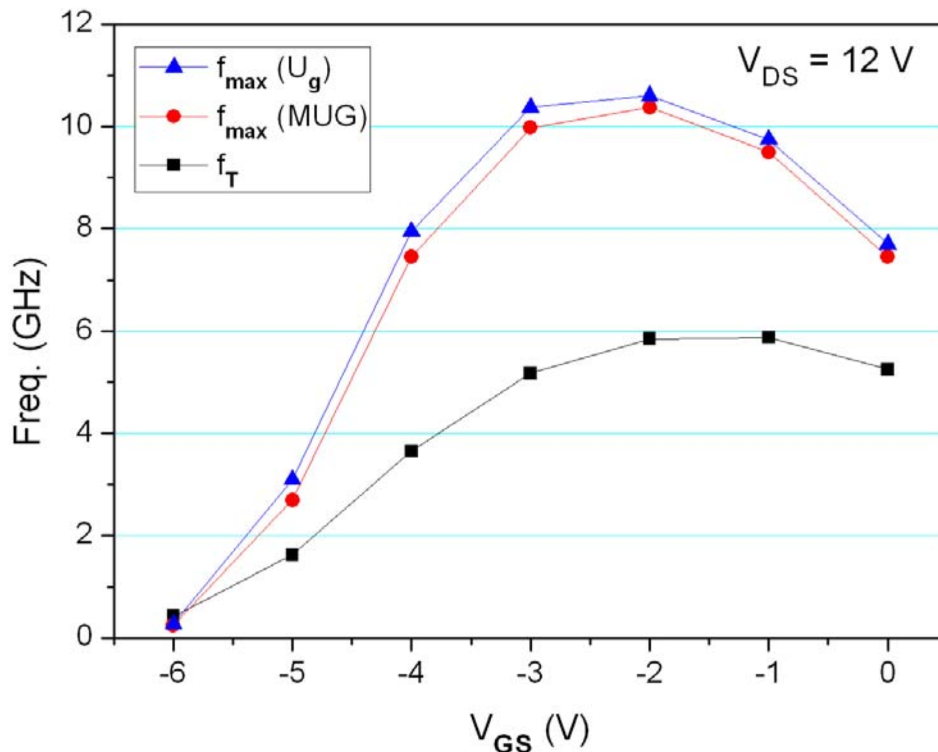


Figure 5-12: Gate bias dependence of current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of the 1μm gate length and 200μm width AlN/GaN MISFET

The peak f_T is 5.88 GHz at V_{GS} = -1 V and the peak f_{max} is 10.6 GHz at V_{GS} = -2 V. The f_T and f_{max} values are mostly below 10 GHz since the gate length is relatively large (1 μm).

The measured S-parameters are essential for modeling the small signal and large signal characteristics. These models are necessary for designing circuits made as MMICs. Information on both small signal and large signal modeling processes are provided in chapter 6. Using the small signal data, certain physical device parameters can also be extracted. An important parameter is electron saturation velocity (V_{sat}) which provides information on material quality and process technology. In order to estimate the electron saturation velocity, small signal modeling was done. Good agreement was observed between measurement and simulation results. These will be shown in chapter 6. The electron saturation velocity could be estimated from the S-parameter data and equivalent circuit parameters using the following equations [5-5].

$$\tau_{RC} = (R_G + R_S)(C_{gs} + C_{gd} + C_{pg}) \quad (5\text{-}7)$$

$$\tau_g = \frac{L_{geff}}{v_{sat}}, \tau_{gd} = \frac{L_{gd} + L_{tr}}{2v_{sat}} \quad (5\text{-}8)$$

$$\tau_{total} = \frac{1}{2\pi f_T} = \tau_{RC} + \tau_g + \tau_{gd} \quad (5\text{-}9)$$

where τ_{total} is total time delay for electron, τ_{RC} is the RC time constant for charging gate capacitances, τ_g is transit time under the gate, τ_{gd} is the transit time from gate edge to drain, and L_{geff}, L_{gd} and L_{tr} are the effective gate length, the gate-drain spacing and the ohmic contact transfer length respectively. Using the equivalent circuit elements and physical data of the device, the estimated saturation velocity υ_{sat} was found to be 1.36 ×

10^7 cm/s. This value is less than half of the predicted value obtained from Monte Carlo simulation of the $Al_{0.3}Ga_{0.7}N$/GaN heterostructure [5-6], suggesting that there is room for improvement in terms of the electron velocity by optimizing the process technology and the AlN/GaN heterointerface growth.

5.4.2 High frequency performance of *in-situ* Si_3N_4/AlN/GaN MISFETs

In-situ Si_3N_4/AlN/GaN MISFETs were also characterized in the small signal regime. Small signal, on wafer S-parameter measurements were performed using the Anritsu 37397C Vector Network Analyzer too. The f_T and f_{MAX} were found to be 10.2 GHz and 32.3 GHz respectively at a bias of V_{GS} = -1 V and V_{DS} = 8 V as can be seen in Fig. 5.13. . The gate bias dependence at fixed drain voltage of 8 V is shown in Fig. 5.14.

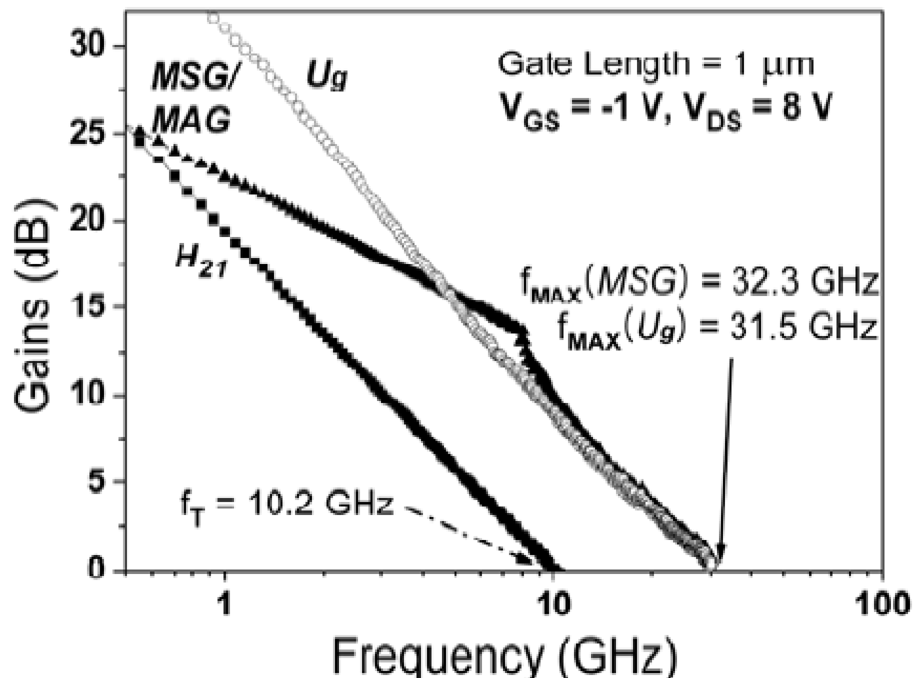


Figure 5-13: Current gain (H21), unilateral gain (Ug) and maximum stable gain (MSG) over frequency for 1 μm long gate *in-situ* Si_3N_4/AlN/GaN MISFETs at V_{GS} = -1V and V_{DS} = 8V

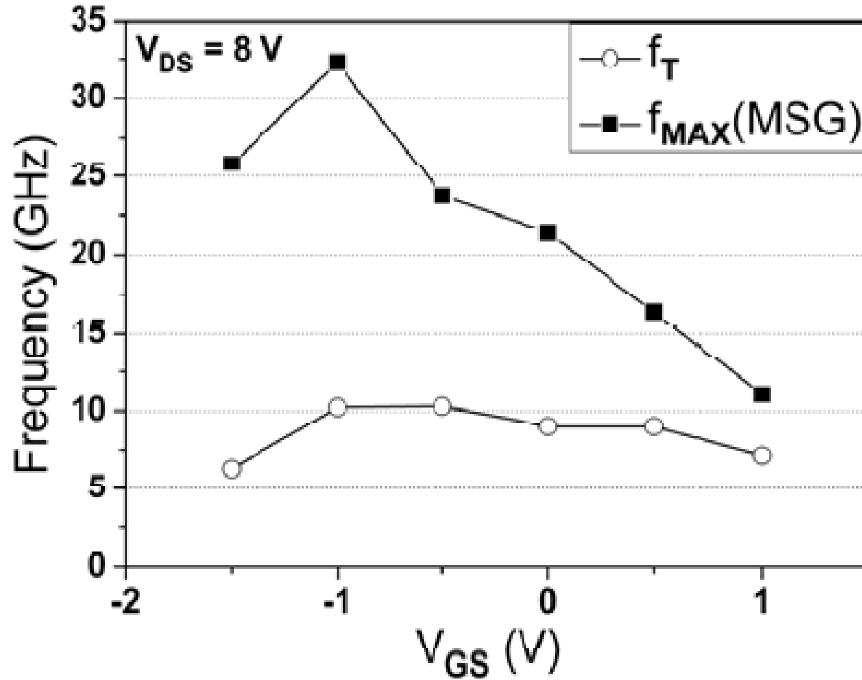


Figure 5-14: Cut off frequency f_T and maximum oscillation frequency f_{MAX} (MSG) dependence on V_{GS} at V_{DS} = 8V for 1 μm long gate *in-situ* Si_3N_4/AlN/GaN MISFETs shows the f_T and f_{MAX} dependence on gate voltage V_{GS} at V_{DS} = 8V.

Comparing with AlN/GaN MISFETs without Si_3N_4 passivation, which were fabricated using the same growth and fabrication technology, AlN/GaN MISFETs with *in-situ* MOCVD deposited Si_3N_4 exhibited greatly improved RF characteristics; a factor of 2 to 3 improvement for f_T and f_{MAX} respectively (f_T: 5.8 GHz to 10.2 GHz and f_{MAX}: 10.47 GHz to 32.3 GHz).

5.4.3 High frequency performance of sub-micron *in-situ* Si_3N_4/AlN/GaN MISFETs

Sub-micron T-gates were fabricated on *in-situ* Si_3N_4/AlN/GaN MISFETs as explained in section 4.2.4 and characterized by VNA at room temperature. Fig. 5.15 shows the current gain, unilateral gain and maximum stable gain over frequency for *in-*

situ Si_3N_4/AlN/GaN MISFETs with 150 nm gate length and 200 µm gate width at V_{GS} = -0.5 V and V_{DS} = 10 V. The f_T and f_{MAX} were found to be 49.9 GHz and 102.3 GHz respectively. Sub-micron AlN/GaN MISFETs fabricated on MBE layers and reported by other groups. [5-7] showed f_T of 107 GHz and f_{MAX} of 171 GHz with 40 nm gate length. f_T of 52 GHz and f_{MAX} of 60 GHz with 250 nm gate length were also shown by [5-8]. The fabricated *in-situ* Si_3N_4/AlN/GaN MISFETs show therefore comparable or even better small signal characteristics considering their gate length. However, there is still room for improvement in terms of their small signal characteristics by reducing parasitic elements such as parasitic capacitance and improving carrier concentration by growth optimization.

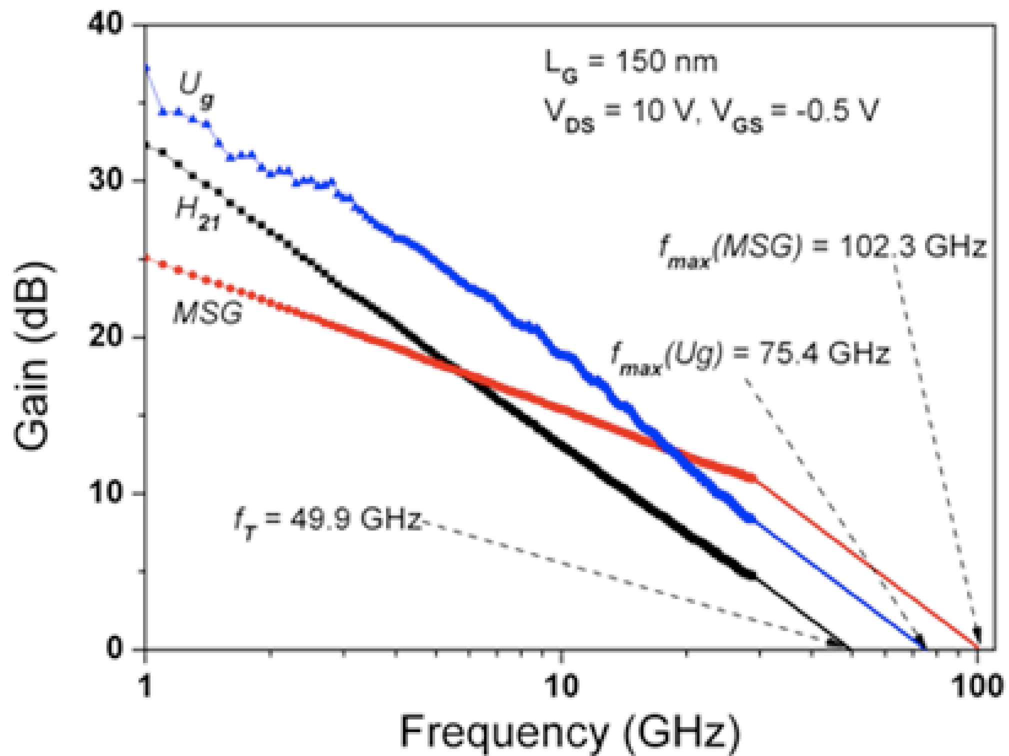


Figure 5-15: Current gain (H21), unilateral gain (Ug) and maximum stable gain (MSG) over frequency for 150 nm long T-gate gate *in-situ* Si_3N_4/AlN/GaN MISFETs at V_{GS} = -0.5V and V_{DS} = 10V

5.5 Power Performance of AlN/GaN MISFETs

Power performance of the fabricated AlN/GaN MISFETs without Si_3N_4 were characterized at 2 GHz using an active load pull system. Single tone power measurements were performed several AlN/GaN MISFETs. Fig. 5.16 shows the typical output power and Power Added Efficiency (PAE) results of the devices. The active load pull system estimated first the maximum output power and PAE load matching point. Several load matching points were then measured in order to find the optimum matching load corresponding to maximum output power or maximum PAE. For the investigated AlN/GaN MISFETs, these two points were found to be very close together. Therefore, a single load matching point is expected to allow one to obtain simultaneously reasonably high output power and high PAE values.

For each of the evaluated optimum output matching point, the input power of the device was swept from the linear to the non-linear region where PAE reaches maximum

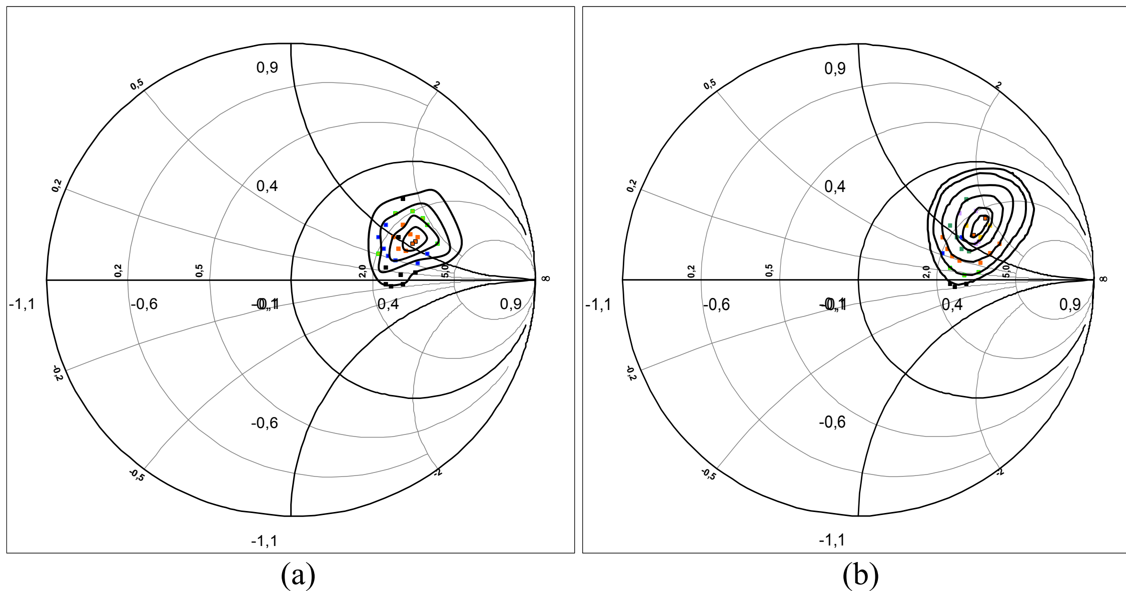


Figure 5-16: Typical output power (a) and PAE (b) contours of AlN/GaN MISFET

value. Fig. 5.17 shows the measured output characteristics for 2 finger 100 μm AlN/GaN MISFET.

Normally, a higher V_{DS} bias leads to higher output power and V_{GS} bias defines the class of amplifier. If the V_{GS} bias is such that it corresponds to half of the maximum I_{DS}, the class of operation is referred to as A and corresponds to higher power and gain but relatively low efficiency. When the V_{GS} bias equals pinch off, one operates under class B, which is associated with higher PAE but lower output power and gain. If V_{GS} is biased between class A and class B, it is referred to as class AB and compromises the gain, power and PAE. Table 5.2 lists the power characteristics of the measured AlN/GaN MISFET on various bias conditions. Based on I-V characteristics of AlN/GaN MISFETs in Fig. 5.2 (a), biasing at V_{GS} equal to -2 V and -3 V can be classified as class A and AB operation.

At the bias of V_{GS} = -3 V & V_{DS} = 10 V (class AB), a linear gain of 11.9 dB, maximum output power of 20.26 dBm (531.44 mW/mm) and maximum PAE of 26.43 % were measured. With higher V_{GS} = -2V and V_{DS} = 10V (class A), higher linear gain of 13.11 dB, higher maximum output power of 22.3 dBm (849.73 mW/mm) and lower maximum PAE of 23.77 % were achieved. At V_{GS} = -3V, the maximum output power increased (from 531 mW/mm to 754 mW/mm) with increased V_{DS} (from 10V to 15V), which is the same in case for V_{GS} = -2V biasing.

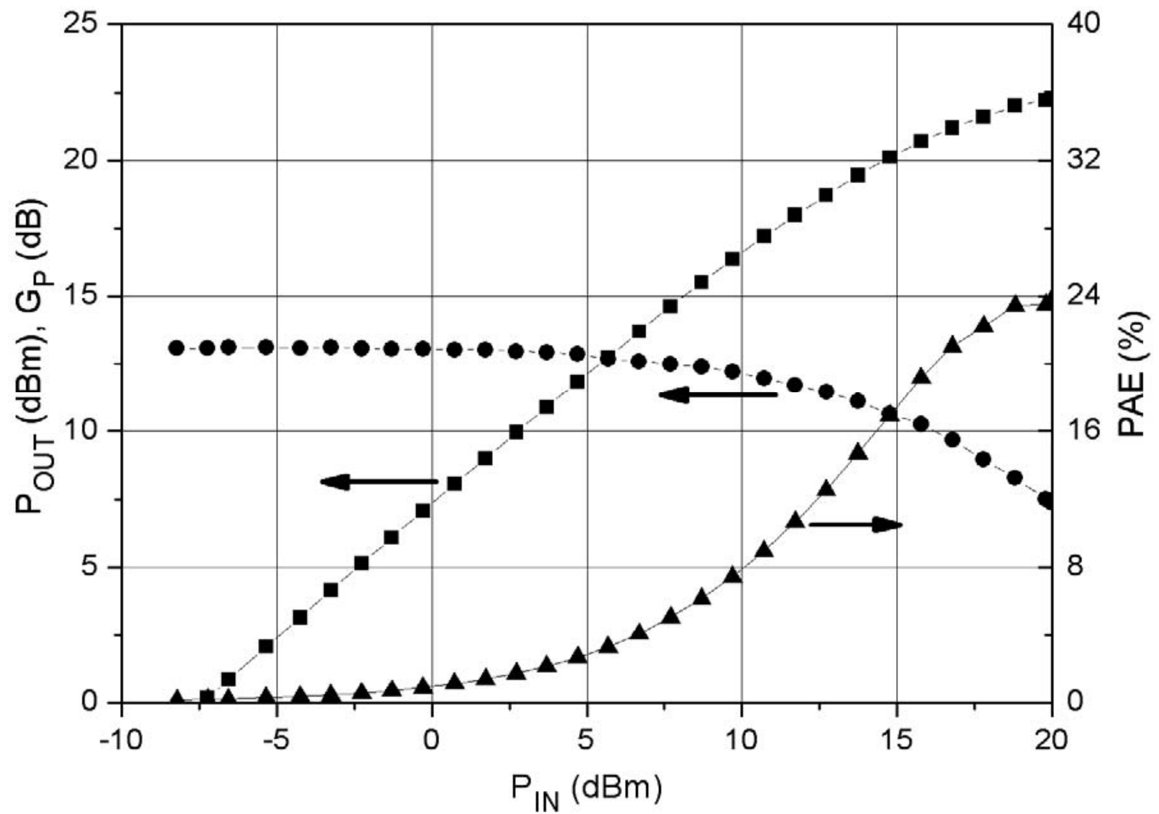


Figure 5-17: Active load pull measurement results for 2 finger × 100 μm no offset AlN/GaN MISFET device at V_{GS} = -2V, V_{DS} = 15V.

V_{GS} Bias	V_{DS} Bias	P_{OUT} density (mW/mm)	max PAE (%)	Linear gain (dB)
-2 V	10 V	577	23.6	12.7
-2 V	15 V	850	23.8	13.1
-3 V	10 V	531	26.5	11.9
-3 V	15 V	754	26.4	12.2

Table 5-2: Power characteristics under various bias conditions

5.6 Summary

In this chapter, several measurement techniques such as DC, pulsed, small signal S-parameters and large signal power, PAE characterization were employed to evaluate the properties of AlN/GaN MISFETs. From DC measurements, the drain characteristics (I_{DS}-V_{DS}), transfer characteristics (I_{DS}-V_{DS}) and gate leakage (I_{GS}-V_{GS}) could be studied. These characteristics provide preliminary information on the power and frequency characteristics of the device. From the drain characteristics, one can estimate the power available from the devices based on the product of maximum current and maximum voltage range. Transfer characteristics allow one to estimate the maximum operation frequency of the device since the maximum cut off frequency f_T is directly proportional to the transconductance g_m.

5 nm thick AlN barrier layer AlN/GaN MISFETs exhibited a peak current density of ~ 380 mA/mm at V_{GS} = 1 V. This threshold voltage V_{th} was about -5 V and the peak extrinsic transconductance was ~ 85 mS/mm. Gate leakage current (I_{DS}) was in the order of 10^{-4} A/mm under reverse V_{GS} and 10^{-3} A/mm under forward V_{GS}. *In-situ* Si_3N_4/AlN/GaN MISFETs exhibited greatly improved DC characteristics; increase of g_m by almost a factor of 3 (85 mS/mm to 206 mS/mm), one order of magnitude lower gate leakage current (from ~10^{-2}A/mm to ~10^{-3}A/mm for V_{GS} = -30V).

Pulsed measurements were used to characterize self-heating, gate lag effects. Small signal measurement i.e. S-parameter measurement were also performed on AlN/GaN MISFETs and AlGaN/GaN HEMTs.

Measured S-parameters provided information on the frequency operation of the devices and will be used in small- and large-signal modeling in chapter 6. AlN/GaN

MISFET showed a maximum cutoff frequency f_T of 5.88 GHz and a maximum oscillation frequency f_{max} of 10.6 GHz. Small signal parameters were extracted from the measured S-parameters and the saturation velocity of the device V_{sat} was calculated as 1.36×10^7 cm/s. *In-situ* Si_3N_4/AlN/GaN MISFETs exhibited highly improved RF characteristics; a factor of 2 to 3 improvement for f_T and f_{MAX} respectively (f_T: 5.8 GHz to 10.2 GHz and f_{MAX}: 10.47 GHz to 32.3 GHz). Sub-micron (150 nm) long gate *in-situ* Si_3N_4/AlN/GaN MISFET at V_{GS} = -0.5V and V_{DS} = 10V showed f_T of 49.9 GHz and f_{MAX} were found to be 49.9 GHz and 102.3 GHz respectively.

An active load pull system was used to characterize the large signal characteristics of AlN/GaN MISFETs. The maximum power and PAE load points were found using load pull contours and at these points the input power was swept with power gain, output power and PAE. For AlN/GaN MISFETs under V_{GS} = -2V and V_{DS} =10V, a linear gain was 13.11 dB, a maximum output power of 22.3 dBm (849.73 mW/mm) and a maximum PAE of 23.77 % were achieved.

CHAPTER 6

Equivalent Circuit Modeling of III-Nitride MISFETs

6.1 Introduction

In order to design and simulate circuits and systems, it is necessary to have a precise device model. GaN-based Monolithic Microwave Integrated Circuits (MMICs) require accurate small and large signal modeling of the III-Nitride HFETs too. Without such models, implementation of MMICs with the developed GaN-based semiconductor device is not possibilbe.

There are two main approaches in device modeling; physical device modeling and empirical equations based modeling. Physical device modeling is based on the physical processes related to device operation such as carrier transport, device geometry and material properties. The equivalent circuit elements such as resistors, capacitors, inductors, current and voltage sources express the physical characteristics and the device itself. The empirical modeling is based on the mathematical representations or tables of the measured input/output characteristics of the devices. It is also often referred to as 'black box' modeling since it relies only on the measurement data without considering the physical processes of the device [6-1]. Both modeling methods have pros and cons. Empirical modeling has advantages like computational efficiency, possibility of modeling out of measurement range and high accuracy, but this model does not provide any physical insight of the device. In contrast, physical modeling provides a good insight to

the device, which can be used directly for device design and/or fabrication optimization. However, due to the assumptions used and the estimations made for the values of the physical parameters its accuracy may, however, be limited. Furthermore, nonlinear characteristics such as dispersion and self-heating effects are difficult to be described by discrete components.

In physical modeling, each discrete circuit elements is defined based on the FET's physical structures and characteristics. Fig. 6.1 shows how these are related together. There are 14 discrete elements and they are categorized into two types of parameters based on their physical characteristics; intrinsic and extrinsic parameters. Intrinsic elements are bias dependent and therefore have different value, depending on gate-source voltage and drain-source voltage. Extrinsic elements are parasitic elements of the device and are therefore not bias-dependent. The six intrinsic parameters include; transconductance of device (g_m), gate to drain feedback capacitance (C_{GD}), gate to source capacitance (C_{GS}), drain to source capacitance (C_{DS}), drain to source resistance (R_{DS}), gate to source channel resistance (R_i). In addition, one more variable of time constant is included corresponding to the voltage controlled current source and providing g_m (τ). The eight extrinsic parameters are parasitic inductances and contact resistances for gate, source and drain (L_G, R_G, L_S, R_S, L_D and R_D) and contact pad capacitances between gate and source (C_{PGS}) and drain to source (C_{PDS}).

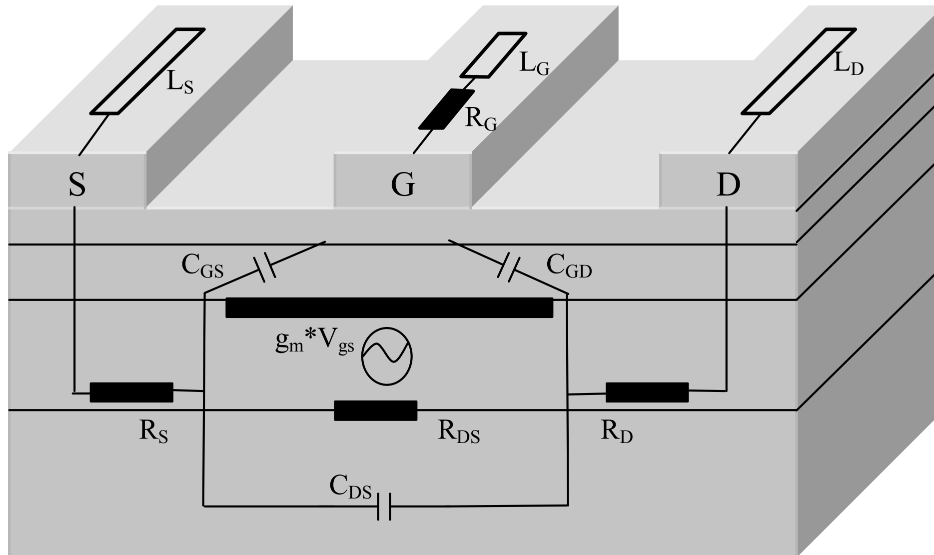


Figure 6-1: Equivalent circuit elements to be related to the physical device geometry and characteristics for HFETs

In this work, physical modeling was developed and utilized to model AlN/GaN MISFETs in view of obtaining a good insight of the physical parameters of the device for device design/fabrication optimization. In order to obtain high modeling accuracy, non-linear optimization techniques for parameter fitting were developed and described. This physical model can be called small signal model since this can be used only up to relatively small signal power level. For large signal modeling, the Agilent EEHEMT1 model was used because of its ability to model accurately the self heating and dispersion effects which are pronounced in AlN/GaN MISFETs. The EEHEMT1 model is an equation based semi-empirical model which also includes physical fitting parameters. Analogous small and large signal modeling methods can be applied to AlGaN/GaN HEMTs and AlN/GaN MISFETs, because their physical characteristics are quite similar except for differences in barrier layer materials; AlGaN or AlN. Therefore same method of small and large signal modeling was described on both types of HFETs. In section 6.2,

a brief review of physical modeling of FETs is presented. Small signal modeling with extraction of external and internal parameters is described in section 6.3. Finally the large signal modeling method which describes DC, S-parameters and power characteristics are presented in section 6.4.

6.2 Small Signal Modeling of AlN/GaN MISFETs

Based on the physical models which were described in the section 6.2, small signal models were developed and evaluated for AlN/GaN MISFETs. The small signal model has only linear elements and therefore it can only be used for small signal circuit designs and not for nonlinear circuits such as power amplifiers. In addition, a small-signal model is valid at a fixed bias point where the intrinsic parameters were extracted. However, most of the parameters extracted through small signal modeling are used again for AC parameter extraction of large signal modeling. Thus, accurate small signal modeling is the first step to large signal modeling for MMIC design. In addition, the small signal parameters such as parasitic elements provide an insight of device optimization. The small signal models and modeling methods are based on the well-known de-embedding technique by [6-2], [6-3]. Fig. 6.2 shows the small signal equivalent circuit used in this work.

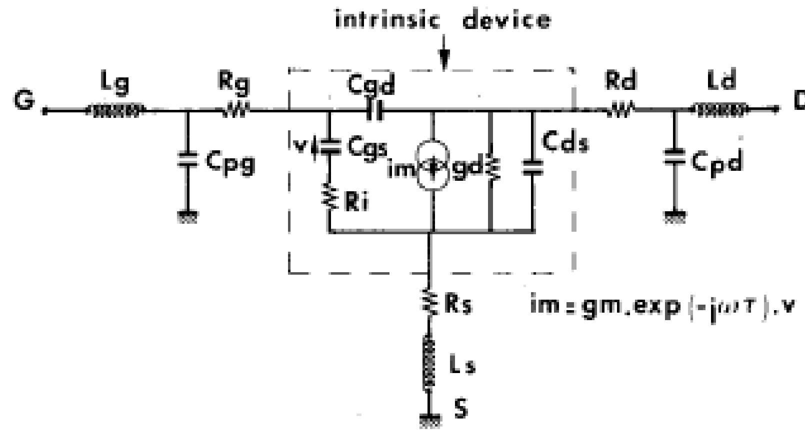


Figure 6-2: Small-signal equivalent circuit for AlN/GaN MISFET [6-2].

The extraction of equivalent circuit elements are in two steps; first the extrinsic elements are extracted by the so called two step cold FET modeling [6-2, 6-3] and the intrinsic elements are extracted by de-embedding the parasitic elements using a 2-port matrix transformation. The following sections describe the parameter extraction techniques in detail.

6.2.1 Extrinsic parasitic parameter extraction

As a first step, the so called ColdFET technique was applied [6-3] and extrinsic parameters could be extracted. At the bias condition of V_{DS} = 0 V and $V_{GS} < V_{pinchoff}$, only the capacitive elements of the equivalent circuit in Fig. 6.2 are dominant and are depicted in Fig. 6.3. S-parameters measured on that bias condition were transformed to Y-parameters and the Y-parameter values can be used in the following equations for extracting capacitance values.

$$\mathrm{Im}(Y_{11}) = \omega(C_{pg} + C_{gd0} + C_{gs0}) \tag{6.1}$$

$$\mathrm{Im}(Y_{12}) = -\omega C_{gd0} \tag{6.2}$$

$$\mathrm{Im}(Y_{22}) = \omega(C_{pd} + C_{gd0}) \tag{6.3}$$

where ω is angular frequency. Assuming a symmetrical structure with equal residual coupling capacitances (C_{gd0} = C_{gs0}), the gate and drain pad capacitances (C_{pg}, C_{pd}) can be extracted.

As a second step, S-parameters were obtained under V_{DS} = 0 V and V_{GS} bias condition which correspond to high I_{GS} (around 100 mA/mm). At this bias point, the HFET gate behaves like a Schottky diode and the high current flows from gate to the source and drain terminal. Thus capacitive elements can be negligible and only resistive and inductive elements remains to be considered.

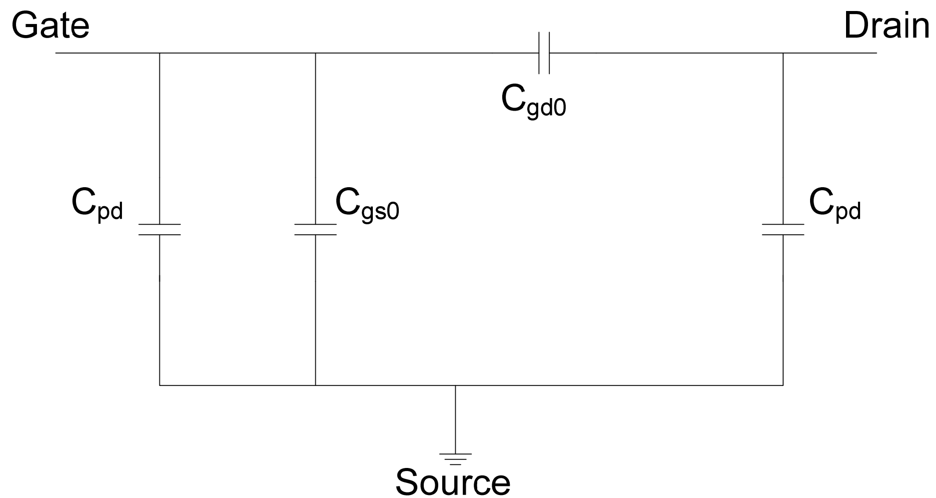
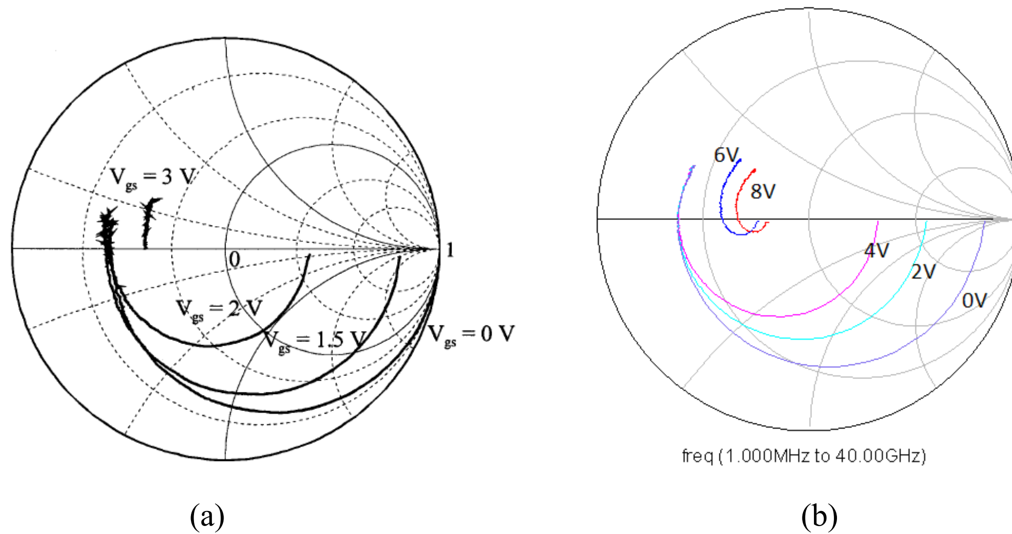


Figure 6-3: Simplified small signal equivalent circuit at V_{DS} = 0 and $V_{GS} < V_{pinchoff}$



(a) (b)

Figure 6-4: S_{11} variation due to change of V_{GS} voltage (a) for $Al_{0.3}Ga_{0.7}N$ HEMT (30 nm barrier thickness) with 1 µm gate length and 120 µm width from ref. [6-4] (b) for 2 finger 200 µm AlN/GaN MISFET with 3× offset. (0.1 GHz ~ 40.1 GHz)

Fig. 6.4 (a) shows typical S_{11} variations over the 45 MHz to 40 GHz frequency range due to forward Gate bias voltages changes [6-4]. At V_{GS} = 3V, S_{11} shows pure inductive behavior. This bias voltage is significantly higher than used in conventional AlGaAs/GaAs HEMTs because of the higher conduction band discontinuity [6-5]. In case of AlN/GaN MISFETs, a capacitive type of nature can be seen at very high forward bias voltage at the gate (V_{GS} = 8 V). A higher then 8 V forward bias could not be applied to avoid gate breakdown. However, as can be seen in the following sections, the S-parameter values for V_{GS} = 8 V can be used for parameter extraction since the optimization step with ADS for the parasitic value extraction is followed for error reduction. The measured S-parameters at the bias of inductive behavior were converted to Z-parameters and then the following equations can be applied [6-3].

$$Z_{11} = R_s + R_g + \frac{1}{3}R_{ch} + j\omega(L_s + L_g) \quad (6.4)$$

$$Z_{12} = Z_{21} = R_s + \frac{1}{2}R_{ch} + j\omega L_s \quad (6.5)$$

$$Z_{22} = R_s + R_d + R_{ch} + j\omega(L_s + L_d) \quad (6.6)$$

To determine the four resistance parameters from these three equations one more equation is required. The channel resistance R_{ch} can extracted from linear interpolation of the real part of Z_{22} versus $1/(V_{gs}-V_{th})$. Fig. 6.5 shows the graphs.

$$\mathrm{Re}(Z_{22}) = R_s + R_d + R_{ch} \quad \text{with} \quad R_{ch} \propto \frac{1}{V_{gs} - V_{th}} \quad (6.7)$$

The intersection of the extrapolated line fitted for low gate voltages and y-axis yields the sum of R_s and R_d as can be seen in Fig. 6.5.

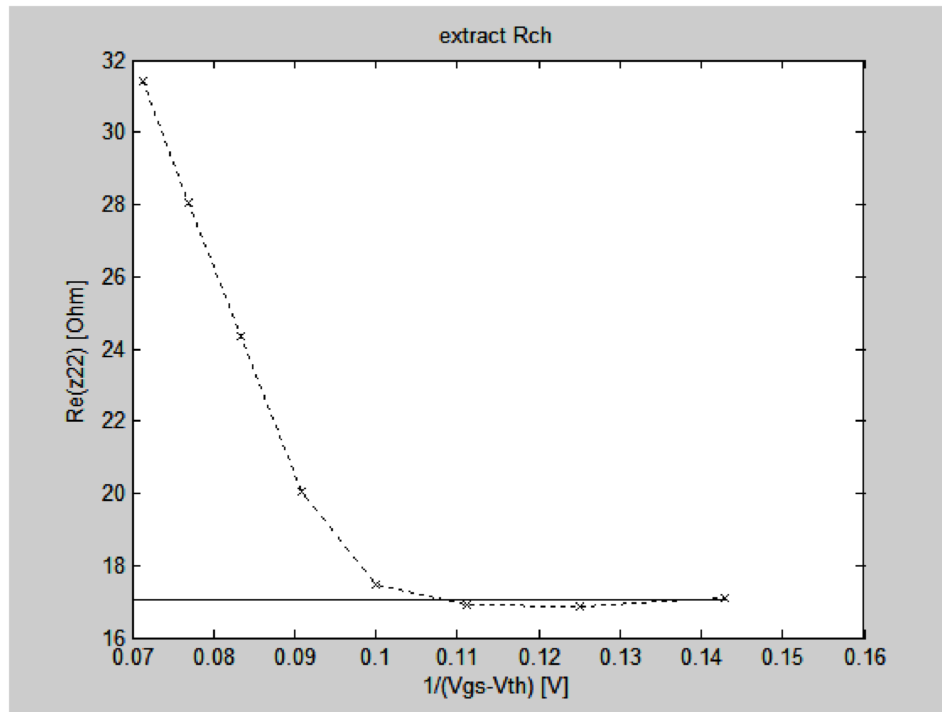


Figure 6-5: Determination of the channel resistance (V_{DS} = 0). Dashed line is real part of Z_{22} and the line is extrapolated line.

From the above equations one can now extract the parasitic elements as follows [6-3].

$$R_{ch} = \mathrm{Re}(Z_{22}) - R_s - R_d \quad (6.8)$$

$$R_s = \mathrm{Re}(Z_{12}) - \frac{1}{2} R_{ch} \quad (6.9)$$

$$R_d = R_s + R_d - R_s \quad (6.10)$$

$$R_g = \mathrm{Re}(Z_{11}) - R_s - \frac{1}{3} R_{ch} \quad (6.11)$$

$$L_s = \frac{\mathrm{Im}(Z_{12})}{\omega} \quad (6.12)$$

$$L_d = \frac{\mathrm{Im}(Z_{22})}{\omega} - L_s \quad (6.13)$$

$$L_g = \frac{\mathrm{Im}(Z_{11})}{\omega} - L_s \quad (6.14)$$

Best results were obtained when calculating an average value over a frequency range, where the parasitic values are almost constant. At higher frequency range (normally over 10 GHz), the values of the parasitic parameters are more accurate. In AlN/GaN MISFET modeling, C_{pg} and C_{pd} were averaged over 10 ~ 15 GHz, whereas the R and L values were averaged over 20-25 GHz.

It should be mentioned that the extracted values for the parasitic (extrinsic elements) using the coldFET method as described above have some errors, because even at high gate voltages the device still shows inductive behavior. The errors can be resolved by applying optimization techniques in ADS as described in the later section.

6.2.2 Intrinsic equivalent circuit parameter extraction

Using the obtained extrinsic elements, intrinsic elements can be obtained by 2-port matrix transformations from measured S-parameters to Y-parameters. The measured S-parameters contain whole intrinsic and extrinsic parameters as can be seen in Fig. 6.5. By

transformation of the S-parameters to Z-parameters, extrinsic inductances of L_g and L_d can be subtracted. Then the Z-matrix is transformed to Y-matrix and extrinsic capacitances of C_{pg} and C_{pd} can be subtracted. The subtracted Y-matrix is transformed to Z matrix again and the remaining extrinsic parameters (R_s, R_g, R_d and L_s) can be subtracted. Finally, the obtained Z-matrix is transformed to Y-matrix which has only the intrinsic parameters. Fig. 6.6 describes the above transformation and subtraction process for deembedding extrinsic elements.

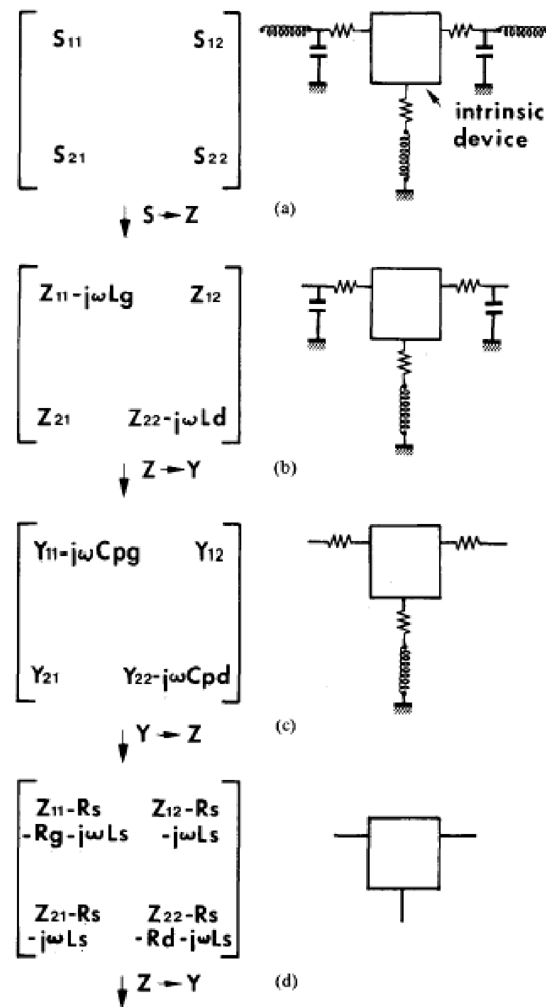


Figure 6-6: Method for extracting the device intrinsic Y-Matrix [6-2]

From intrinsic Y-Parameters, the intrinsic elements can be calculated by the following equations [6-3].

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{6.15}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{(\mathrm{Re}(Y_{11}))^2}{(\mathrm{Im}(Y_{11}) - \omega C_{gd})^2}\right) \tag{6.16}$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{(\mathrm{Im}(Y_{11}) - \omega C_{gd})^2 + (\mathrm{Re}(Y_{11}))^2} \tag{6.17}$$

$$g_m = \sqrt{((\mathrm{Re}(Y_{21}))^2 + (\mathrm{Im}(Y_{21}) + \omega C_{gd})^2)(1 + \omega^2 C_{gs}{}^2 R_i{}^2)} \tag{6.18}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - \mathrm{Im}(Y_{21}) - \omega C_{gs} R_i \,\mathrm{Re}(Y_{21})}{g_m}\right) \tag{6.19}$$

$$g_{ds} = \mathrm{Re}(Y_{22}) \tag{6.20}$$

The above equations are valid over the entire frequency range. Best results can be obtained when averaging the values over the frequency range of interest for MMIC design. In this work, the averaging frequency range was chosen to be from 5 to 15 GHz.

C_{pd}	35 fF	L_s	0 pF
C_{pg}	62 fF	C_{gd}	69 fF
R_s	12 ohms	C_{gs}	579 fF
R_g	3 ohms	R_i	19 ohms
R_d	22 ohms	g_m	0.0328 S
L_g	4 pH	Tau	0.25 ps
L_d	10 pH	R_{ds}	233 ohms

Table 6-1: Extracted extrinsic and intrinsic equivalent circuit parameters for 2 finger 200 µm AlN/GaN MISFETs with 3× gate offset at bias point of V_{GS} = -2.5 V & V_{DS} = 8 V

Table 6.1 shows the extracted values for 2 finger 200 µm wide gate AlN/GaN MISFET device with 3× gate offset.

The extracted intrinsic element values include small errors, since they rely on values extracted for the extrinsic elements, which are also not exact. Nevertheless, they can be employed as good starting values for a nonlinear optimization process which allows further error reduction. The optimization was carried out using Agilent ADS [6-6] software package as described in the following section.

The process of extracting extrinsic and intrinsic element values as programmed with MATLAB [6-7]. The MATLAB Graphic User Interface (GUI) shown in Fig. 6.7 was developed to perform parameter extraction technique in an automated way.

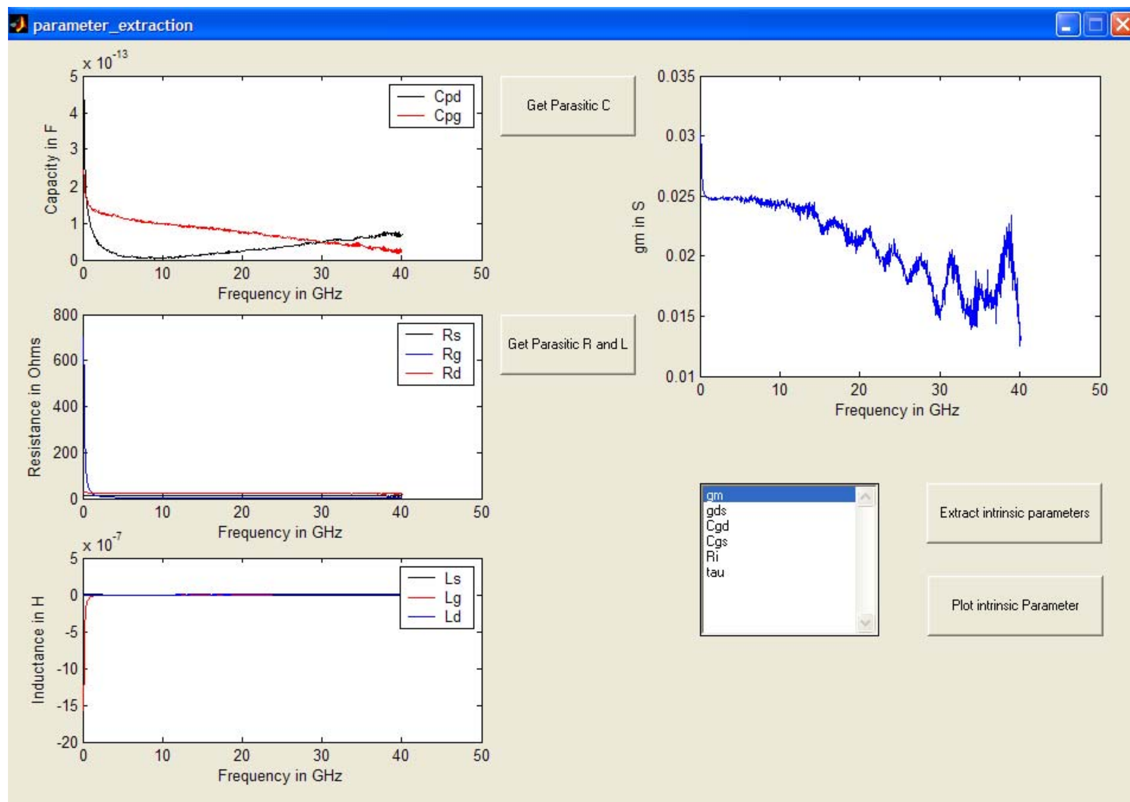


Figure 6-7: Developed MATLAB GUI for parameter extraction

6.2.3 Non-linear optimization of parameter fitting

As mentioned earlier, the extraction technique is sensitive to the S-parameters measured under ColdFET conditions. This is especially critical for AlN/GaN MISFETs, where it was not possible to measure fully inductive S-parameters lying in the inductive parts of the Smith chart even at the very high V_{GS} bias voltage which is close to breakdown. Therefore, the extracted parameters include errors, which can be eliminated by a gradient-based nonlinear optimization approach in Agilent ADS software was employed for this purpose in small signal modeling of AlN/GaN MISFET. Fig. 6.8 shows the corresponding optimization setup in ADS.

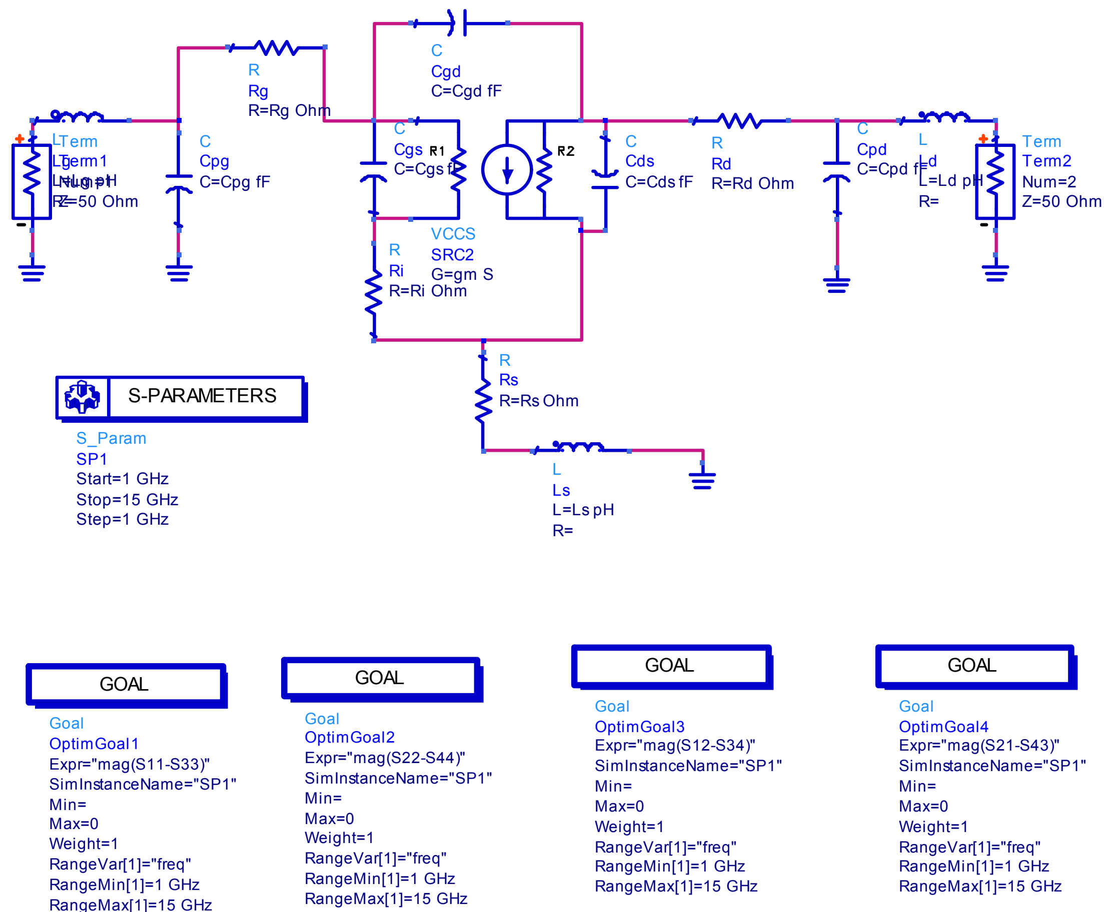


Figure 6-8: Nonlinear optimization setup in Agilent ADS for small signal modeling optimization.

The extracted equivalent circuit parameters by coldFET modeling were used as initial values for the optimization. The optimization goals were satisfied when the difference between the measured and modeled S-parameters equaled zero.

Table 6.2 lists the optimized equivalent circuit parameters an obtained by coldFET modeling approach with non-linear optimization. Fig. 6.9 shows a Smith chart with the

Parameters	Before optimization	After optimization
C_{pd}	35 fF	34.831 fF
C_{pg}	62 fF	0.0218936 fF
R_s	12 ohms	14.4225 ohms
R_g	3 ohms	7.8739 ohms
R_d	22 ohms	12.99 ohms
L_g	4 pH	26.5316 pH
L_d	10 pH	116.063 pH
L_s	0 pH	41.666 pH
C_{gd}	69 fF	56.0617 fF
C_{gs}	579 fF	539.619 fF
R_i	19 ohms	1.14514 ohms
g_m	0.0328 S	0.0237371 S
tau	0.25 ps	1.91488 ps
R_{ds}	233 ohms	247.164 ohms

Table 6-2**:** Equivalent circuit parameters of 2 finger 200 µm AlN/GaN MISFET before and after the non-linear optimization

modeled and measured S-parameters before and after optimization. After optimization, the matching between modeled and measured S-parameters was significantly improved.

The optimized values were obtained by searching for a minimum in the error function. Because the error function is highly nonlinear, it is unsure that the minimum determined by the gradient search method is a local or an absolute minimum. If the starting values for the gradient search method were close enough to the actual physical parameters of the device, the search method converged to the absolute minimum, which represents the real parameter values. Also if the small signal model's S-parameters are well matched with the measured S-parameters, it can be stated that the values for the parasitic parameters determined by the optimizer correspond to their real values.

The parameter extraction was performed again by the technique described in the previous sections using the values that the optimizer has determined for the parasitic.

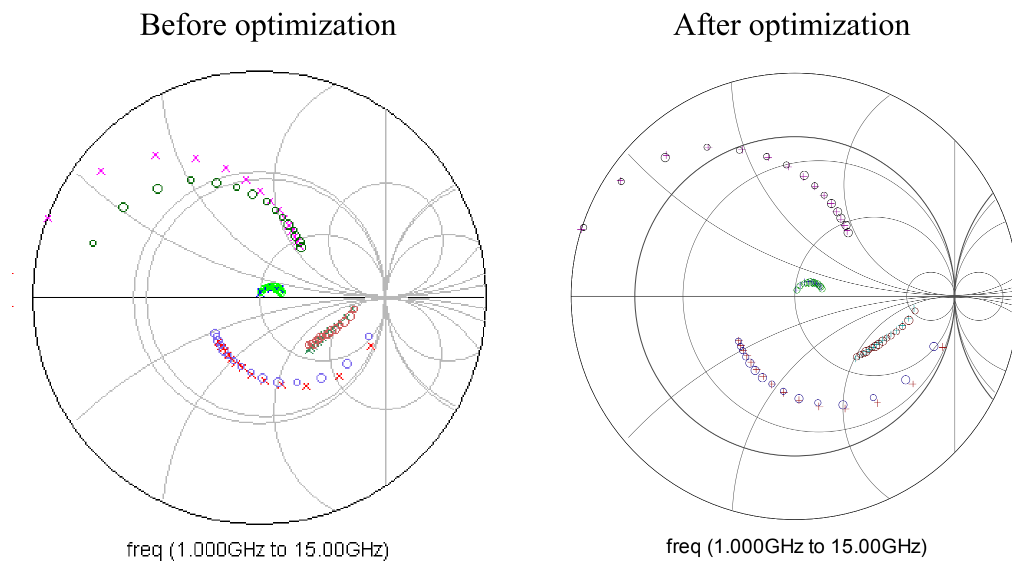


Figure 6-9: Measured (circle) and simulated (cross) S-parameters of AlN/GaN MISFET at the frequency range from 1 GHz to 15 GHz. (bias at V_{GS} = -2.5V & V_{DS} = 8V)

The results produced for the intrinsic values should correspond to the values determined by the optimizer as given in Table 6.2. Table 6.3 shows the intrinsic values determined by the optimizer and those determined by the extraction technique described in the previous sections.

As can be observed in Table 6.3, the values from the optimizer and those from the extraction technique are almost identical. This is a good indication that the optimizer has found a global minimum and the values for the parasitic that were determined by the optimizer are accurate.

The same procedure of small signal modeling was applied on in house fabricated AlGaN/GaN HEMTs with 25% Al composition and 30 nm barrier layer thickness. As stated before, there is no fundamental difference between modeling of AlN/GaN MISFETs and AlGaN/GaN HEMTs. Therefore, good small signal modeling was achieved for AlGaN/GaN HEMTs. Table 6.4 shows the intrinsic and extrinsic parameters of 2 finger 250 μm wide AlGaN/GaN HEMTs. The measured and small signal modeled S-

Intrinsic Parameters:	Values from Optimizer:	Values from Extraction Technique:
C_{gd}	56.0617 fF	53.175 fF
C_{gs}	539.619 fF	547.30 fF
R_i	1.14514 ohms	1.1446 ohms
g_m	0.0237371 S	0.0242 S
Tau	1.91488 ps	1.9267 ps
R_{ds}	247.164 ohms	238.0952 ohms

Table 6-3: Comparison of intrinsic parameters from the optimizer and from the extraction technique.

parameters were reasonably well matched. Therefore, the small signal modeling method, which utilizes non-linear optimization, can be successfully applied on AlN/GaN MISFETs and AlGaN/GaN HEMTs.

C_{pd}	35.9 fF	L_s	10.5 pH
C_{pg}	54.1 fF	R_s	8.37 Ω
L_g	38.8 pH	R_d	7.50 Ω
L_d	53.9 pH	R_g	3.22 Ω
C_{gd}	40.7 fF	R_i	15.3 Ω
C_{gs}	824.6 fF	g_m	20.4 mS
R_{ds}	221 Ω	tau	4.20 psec

Table 6-4: Equivalent circuit parameters of 2×125 μm 3× offset $Al_{0.25}Ga_{0.75}N$/GaN HEMT at bias of V_{GS} = 0 V and V_{DS} = 10 V

6.3 Large Signal Modeling of AlN/GaN MISFETs

The developed small signal models are valid only for specific bias point and it is therefore not possible to use them under large signal conditions where the load line includes a wide range of DC biasing points. Therefore a large signal model which contains bias dependent parameters is necessary to be developed for use in non-linear MMIC design.

6.3.1 Agilent EEHEMT1 large signal model

In large signal modeling, DC, small-signal and large-signal characteristics of the device should be fitted well with measurement data at the same time. It is only under

such conditions that the performance of a circuit can be predicted correctly. In this work, the Agilent EEHEMT1 model [6-6] was used because of the main advantages it offers to GaN-based heterostructure device modeling namely consideration of parameters for self-heating effects and DC-RF dispersion. AlGaN/GaN HEMTs and AlN/GaN MISFETs on sapphire substrate are normally experiencing strong self heating effect due to the low thermal conductivity of substrate. Moreover, dispersion effects are pronounced for GaN-based materials due to surface and interface deep-level traps investigated in chapter 5.

Fig. 6.10 shows the equivalent circuit model of EEHEMT1 and Fig. 6.11 shows the Agilent ADS device schematic of EEHEMT1 with external parasitic elements. Though the model is an equation based semi-analytical model, all the parameters had some physical significance and could be extracted and easily estimated (visually) from measured data such as g_m-V_{GS} plots [6-6]. Comparing with other popular large signal models like the Curtice model, EEHEMT1 has more parameters to be fitted but this can be compensated by the better accuracy of the model. In the following sections, the procedure used for large signal modeling of AlGaN/GaN HEMTs and AlN/GaN MISFETs is shown.

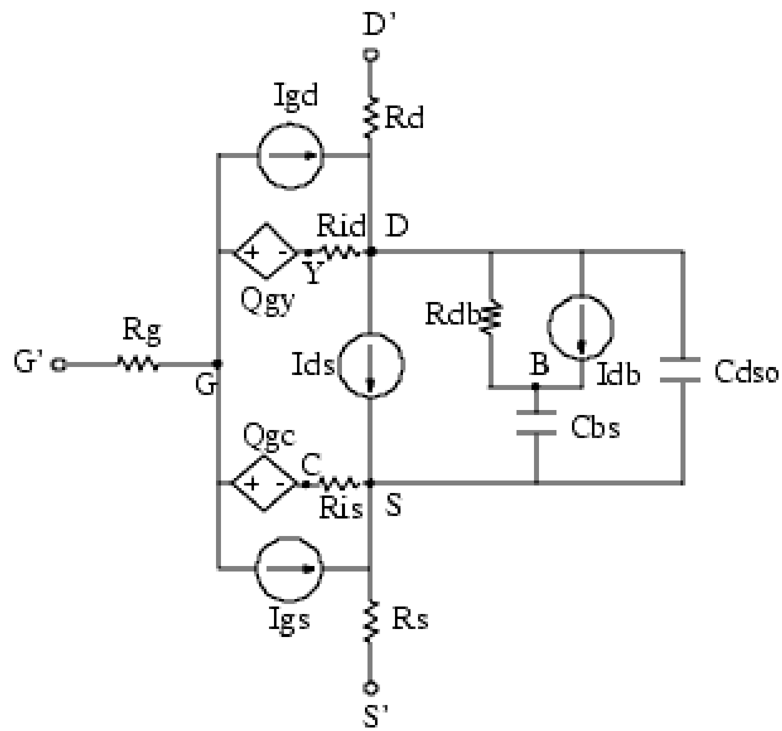


Figure 6-10: Equivalent circuit model of Agilent EEHEMT1 large signal model [6-6]

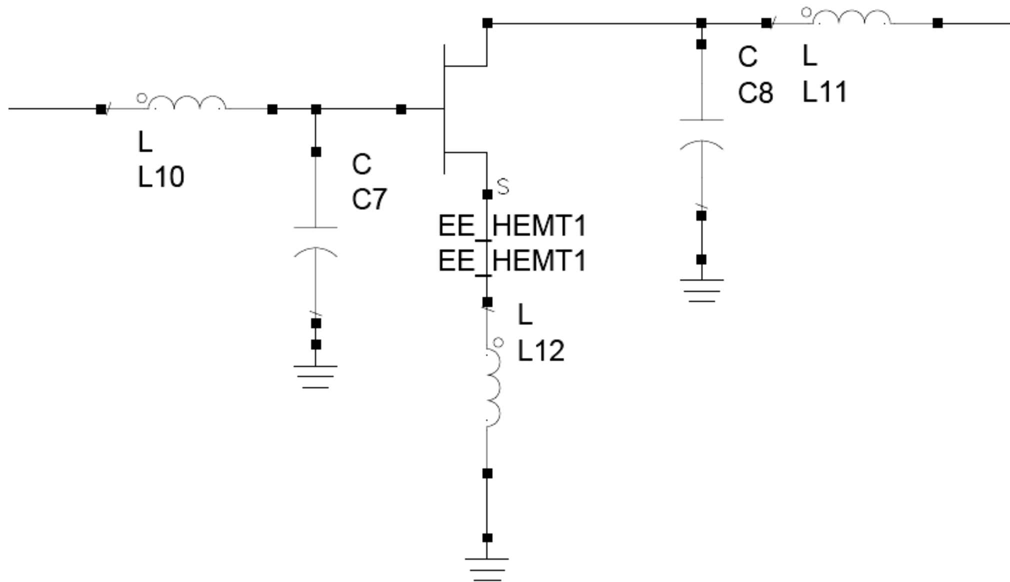


Figure 6-11: EEHEMT1 model with external parasitic elements

6.3.2 Verification of DC parameters of large signal model

As a first step toward the large signal modeling, DC parameters were extracted by fitting the I-V characterization. In order to match the simulated I-V curves of the model to the measured data, parameters that influence the DC behavior of the device were determined. Firstly initial DC parameters were determined from g_m-V_{GS} curves. Fig. 6.12 shows the initial DC parameters associated with the g_m-V_{GS} curve. When $V_{DS} = V_{DS0}$ (V_{DS0} = Knee voltage, in AlN/GaN MISFET V_{DS0} = 5V) and P_{eff} is set large (to disable the self-heating model), the DC parameters of V_{to}, V_{go}, Gmmax, V_{co}, V_{ba}, V_{bc}, Deltgm, and Alpha can be easily extracted from a plot of g_m-V_{GS} [6-6]. Table 6.5 shows an example of extracted DC parameters from the g_m-V_{GS} curve for AlN/GaN MISFETs.

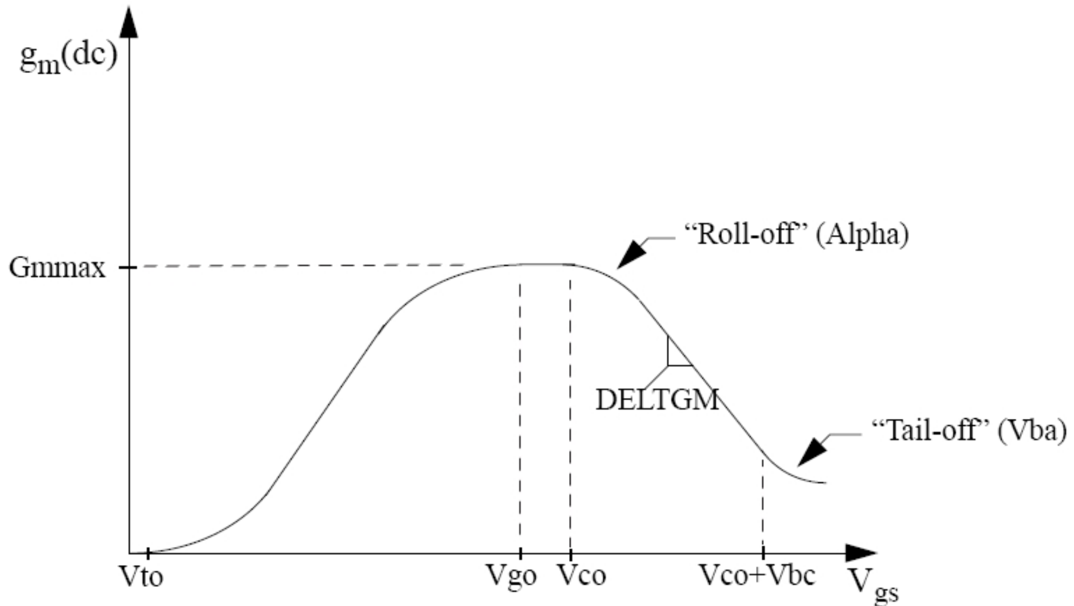


Figure 6-12: EEHEMT1 DC parameters on g_m-V_{gs} curve [6-6]

Name	Value	Unit	Name	Value	Unit
Vdso	5	V	Peff	e.g. 999999	W
Vto	-6.5	V	Deltgm	0.007	S
Vgo	-2.52	V	Alpha	1.2	
Vco	-2.2	V	Vbc	2.2	V
Gmmax	0.0167	S			

Table 6-5: Extracted initial DC parameters from g_m-V_{gs} curve

Following the determination of the initial values, the gradient optimization method was used for parameter optimization. The procedure of DC curve fitting involved first I_{DS}-V_{DS} curve fitting in the linear and then the saturated region. If the fitting of I_{DS}-V_{DS} curves is good, the fitting of I_{DS}-V_{GS} and g_m-V_{GS} curves can be achieved easily. For I_{GS}-V_{GS} curve (gate leakage current), the parameters of I_S and N should be defined additionally. These two parameters describe the gate forward conduction. Forward conduction in the gate junction is modeled using a standard 2-parameter diode expression. The current for this gate-source current is defined by the following equation.

$$I_{gs}(V_{gs}) = Is \cdot \left[e^{\frac{qVgs}{nkT}} - 1 \right] \tag{6.21}$$

where q is the charge on an electron, k is Boltzmann's constant, and T is the junction temperature [6-6]. For this purpose, a MATLAB program was developed as can be seen at Fig. 6.13. From the graphical user interface the user can import the measured data of I_{GS}-V_{GS} and fitting can adjust the parameters by adjusting two scrollbars.

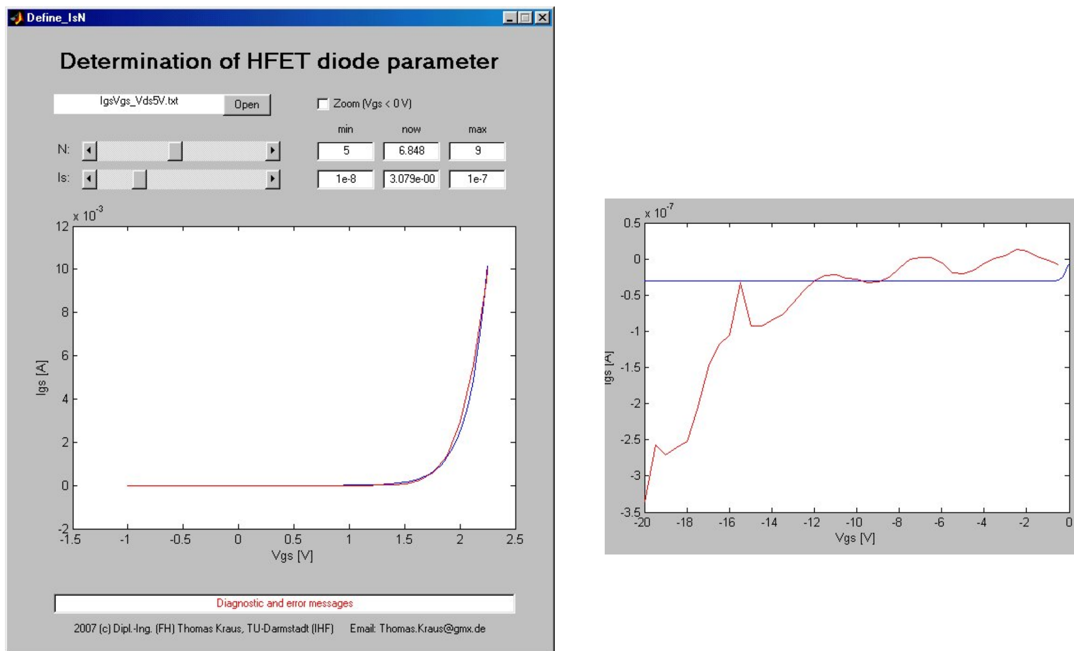
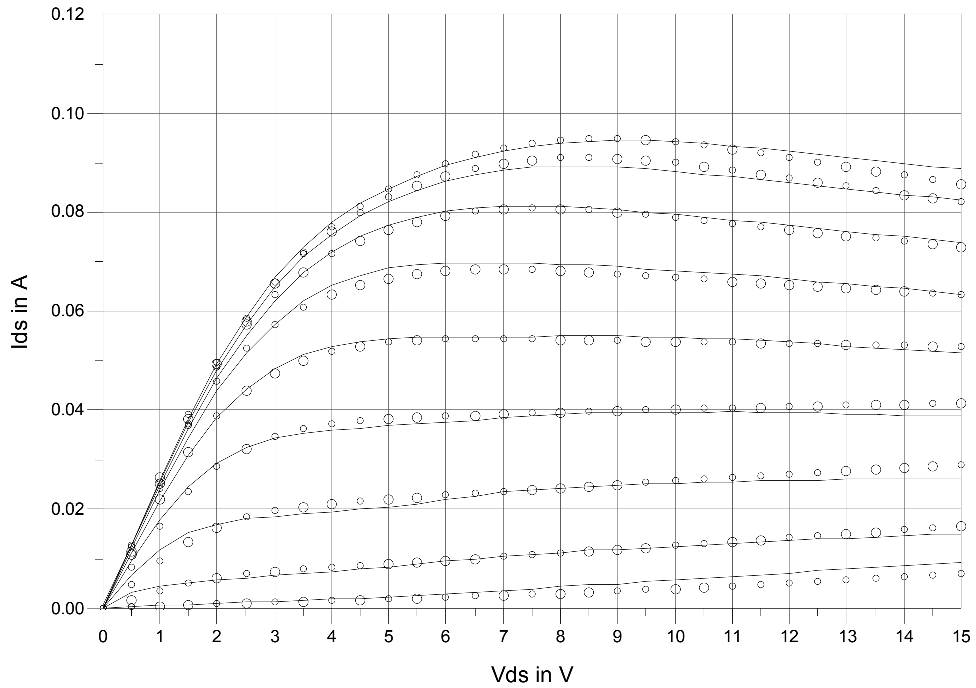


Figure 6-13: left: MATLAB program for extracting parameters from HFET diode characteristics b) zoomed negative V_{GS} region ($V_{GS} < 0V$)

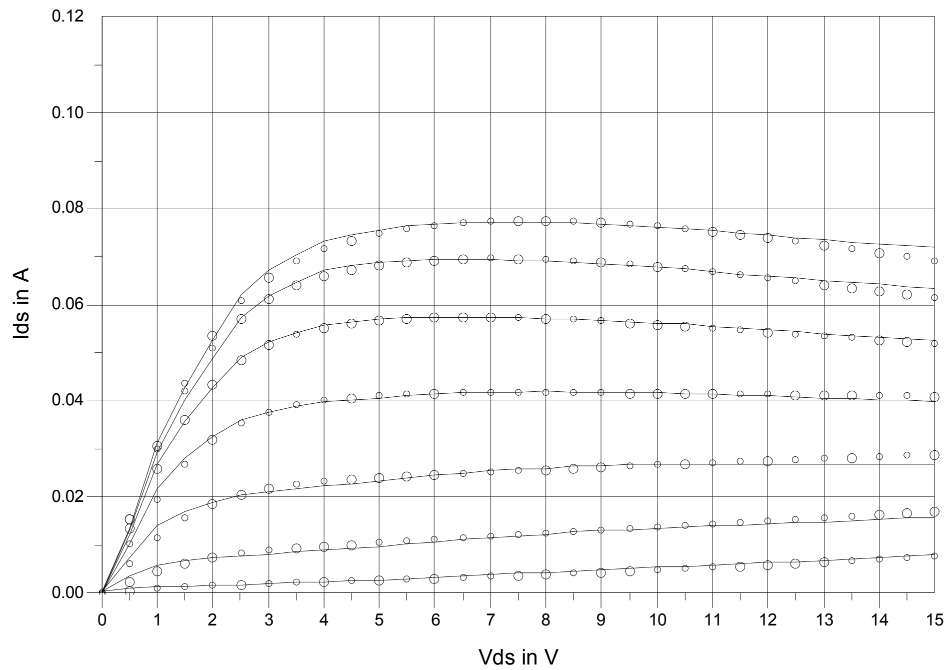
The large signal modeling method was applied on 2 finger 2×100 µm AlN/GaN MISFET with 3× offset and non offset configuration (I_{DS} to V_{DS}) for several bias points (V_{GS} values from +2 V to -6 V in 1V steps for offset device and 0 V to -6 V for non offset device) and the measured g_m values for V_{DS} = 6V (offset device) and V_{DS} = 5V for non offset device at the same time. The optimized DC parameters of EEHEMT1 model are listed in Table 6.6. All of the DC fitting results is shown in Fig. 6.14, Fig. 6.15 and Fig. 6.16.

Name	Value	Unit	Name	Value	Unit
Gamma	0.0140301	1/V	Rs	0.0495878	Ω
Vdso	5	V	Rg	0.270149	Ω
Vch	0.314944	V	Rd	4.32774	Ω
Gmmax	0.022393	S	Vtso	-19.4496	V
Vsat	4.58057	V	Idsoc	5.03981	A
Peff	2.80543	W	Vto	-6.59285	V
Kappa	3.92222e-5	1/V	Vgo	-1.43443	V
Mu	-0.336381		Vco	-3.12332	V
Deltgm	0.00701939	S/V	Vbc	5.84336	V
Alpha	2.67874	V	Is	356e-6	A
Vba	0.498741	V	N	30	

Table 6-6: Optimized DC-parameters of EEHEMT1 model for AlN/GaN MISFET

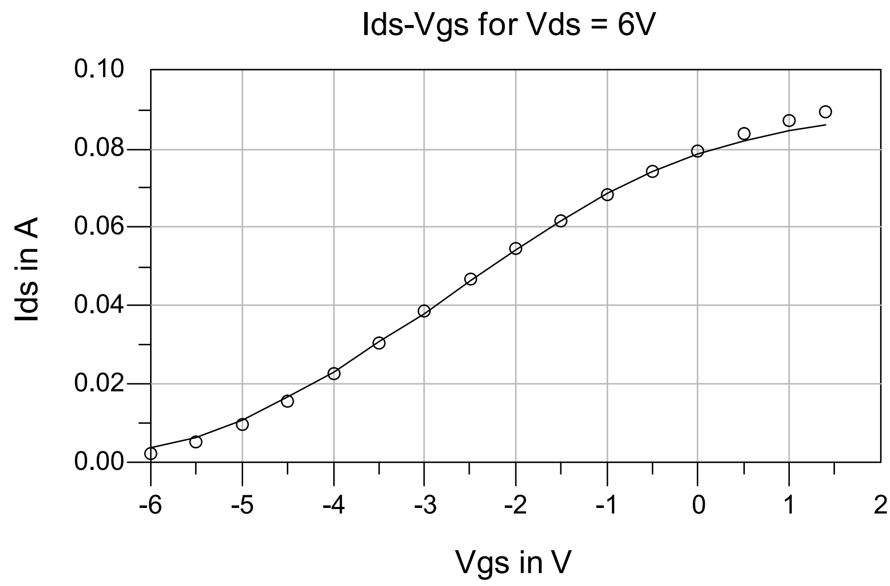


(a)

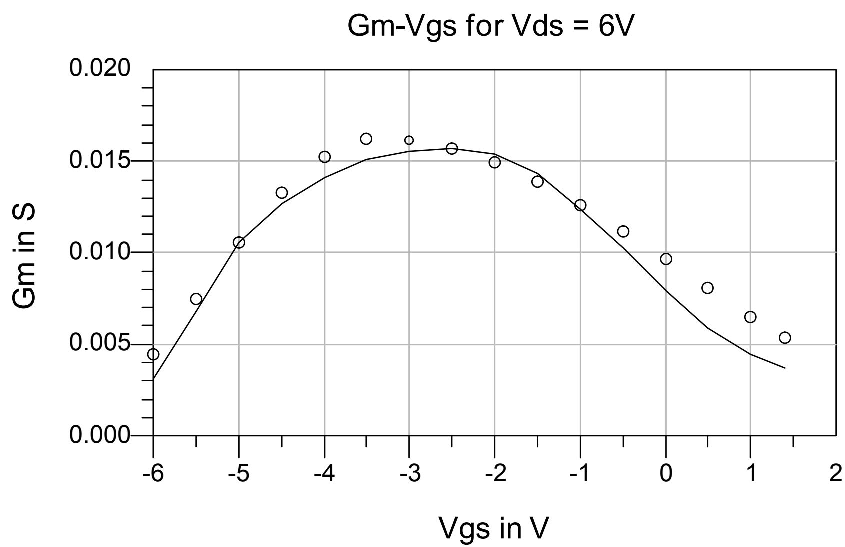


(b)

Figure 6-14: I_{DS}-V_{DS} curve fitting (a) of 2 finger 2×100 μm 3× offset MISFET and of (b) non offset MISFET; solid line: measurement, circle: simulated

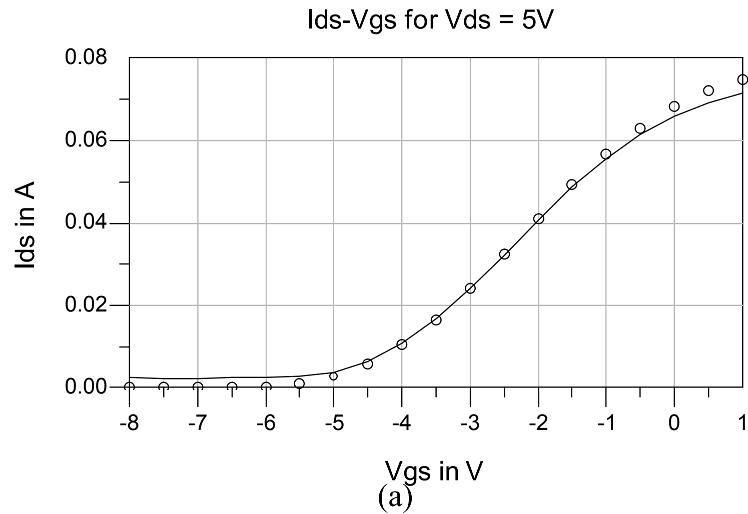


(a)

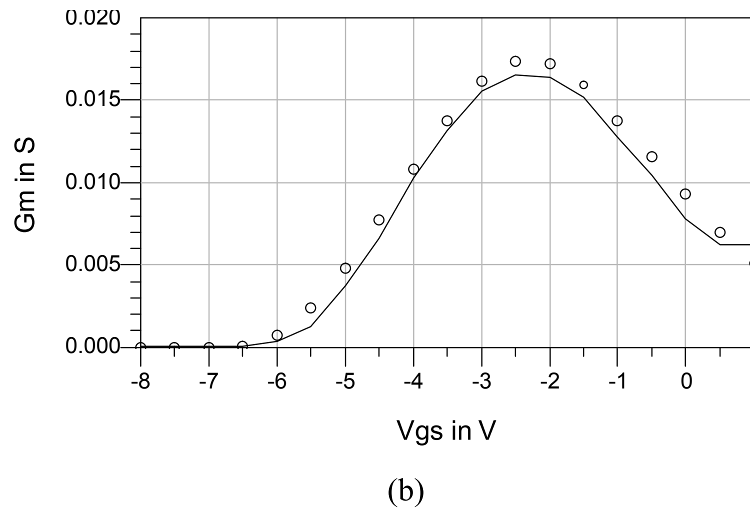


(b)

Figure 6-15: (a) I_{DS}-V_{GS} curve fitting and (b)g_m-V_{GS} curve fitting at V_{DS} = 6V for 2 finger 2×100 μm 3× offset MISFET (solid line : measurement, circle : simulated)



(a)



(b)

Figure 6-16: (a) I_{DS}-V_{GS} curve fitting and (b) g_m-V_{GS} curve at V_{DS} = 6V for 2 finger 2×100 μm non-offset MISFET (solid line: measurement, circle: simulated)

As can be seen in the above figures, DC fitting corresponds to almost perfect data matching. There are small discrepancies in the pinch off and full saturation regions. However, the model represents well the self heating effect and dispersion effect of the AlN/GaN MISFET device well.

The same modeling procedure was applied to $Al_{0.25}Ga_{0.75}N$/GaN HEMTs. Figure 6.17 shows simulated and measured I_{DS}-V_{DS} curves presenting good agreement. The I_{DS}-V_{GS} and g_m-V_{GS} curves at V_{DS} = 5V are shown in Fig. 6.18.

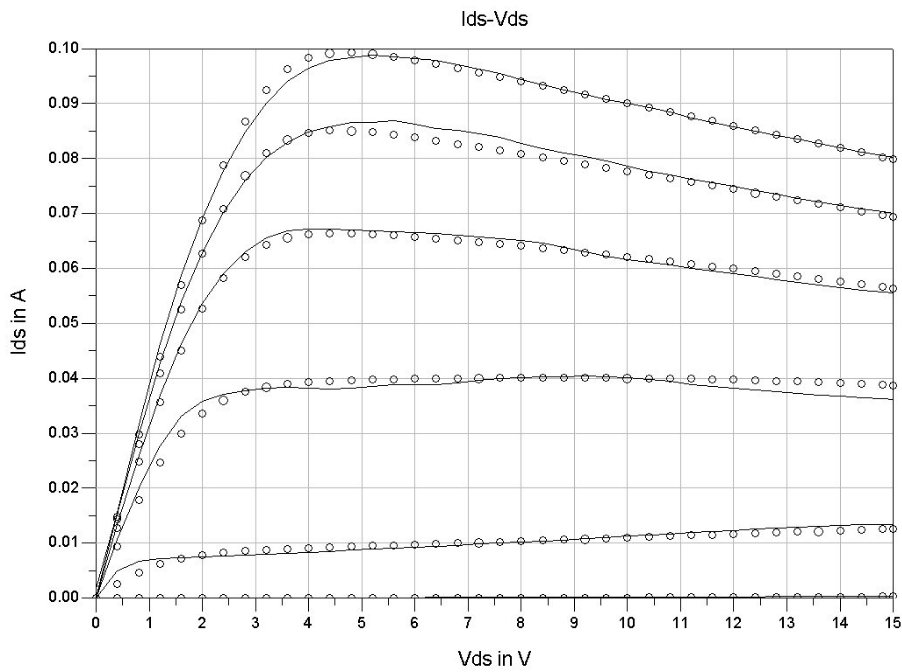


Figure 6-17: Simulated and measured I_{DS}-V_{DS} curve of $Al_{0.25}Ga_{0.75}N$/GaN HEMT with 2 finger 2×125μm 3× offset device [V_{GS} = (2 / 1 / 0 / -1 / -2 / -2.5 / -2.75) V]; dot: simulated & line: measured

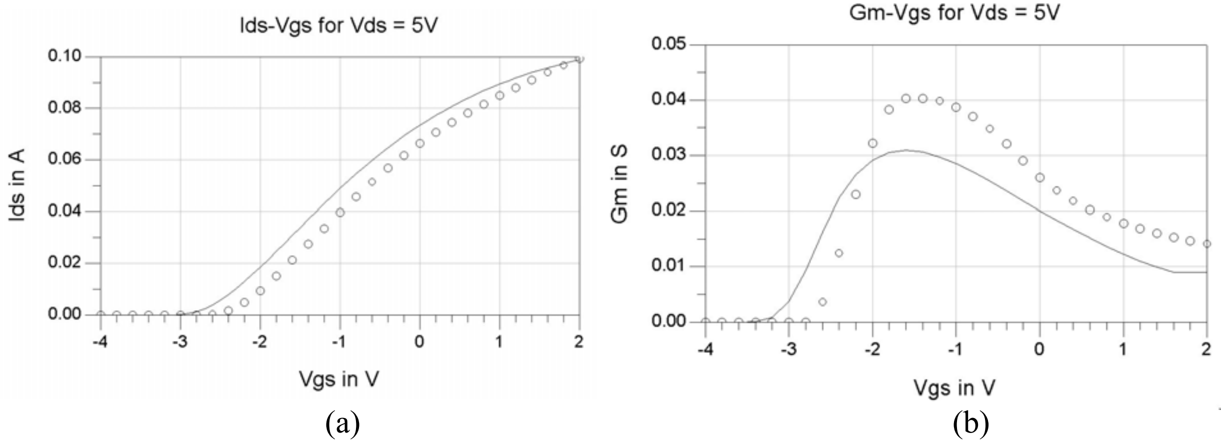


Figure 6-18: (a) I_{DS}-V_{GS} and (b) g_m curve of $Al_{0.25}Ga_{0.75}N$/GaN HEMT with 2 finger 2×125μm 3× offset device; dot: simulated & line: measured

6.3.3 Verification of small signal characteristics of large signal model

In order to build an accurate large signal model, the model should present a good fit of measured S-parameter data at different bias points. The small signal model in section 6.2 is valid only for one bias point because the intrinsic parameters are bias dependent. Large signal models should fit the S-parameters at multiple bias points. Fitting of multiple bias points can be tedious work but non-linear optimization can be helpful in this respect by enabling a good fit and saving time and effort.

Similarly with DC fitting, AC fitting should have good initial AC parameters for non-linear fitting. From the C_{11}-V_{GS} curve which represents gate-charge characteristics, initial values for six AC-parameters (C_{11o}, C_{11th}, Deltgs, Deltds, V_{inf} and Lambda) can be extracted. The C_{11} capacitance is defined as following equation [6-6].

$$C_{11} = \frac{im[y_{11}]}{\omega} = \frac{\partial q_g}{\partial v_{gs}} \tag{6.22}$$

where y_{11} is a y-parameter which is transformed from s-parameter, ω is angular frequency and q_g is gate charge. Fig. 6.19 shows a C_{11}-V_{GS} curve together with the related AC-parameters. The parameter Deltds models the gate capacitance transition from the linear region of the device into saturation. Lambda models the slope of the C_{11}-V_{DS} characteristic in saturation [6-6].

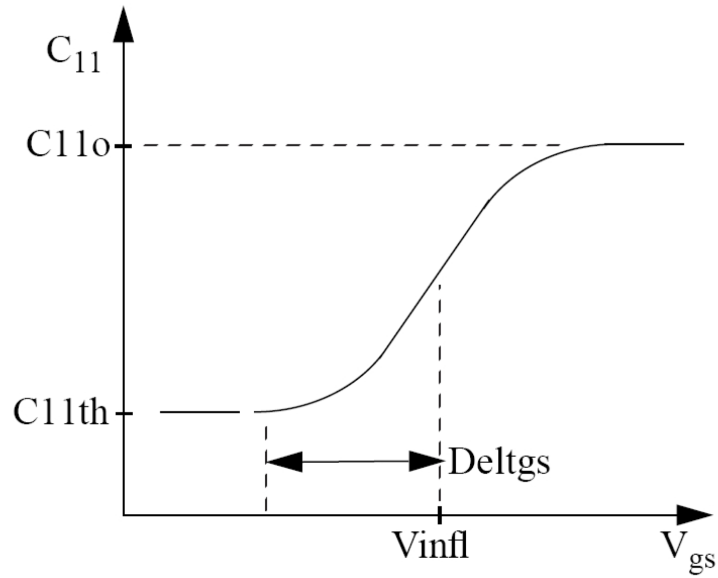


Figure 6-19: C_{11}-V_{GS} curve for AC parameter extraction [6-6]

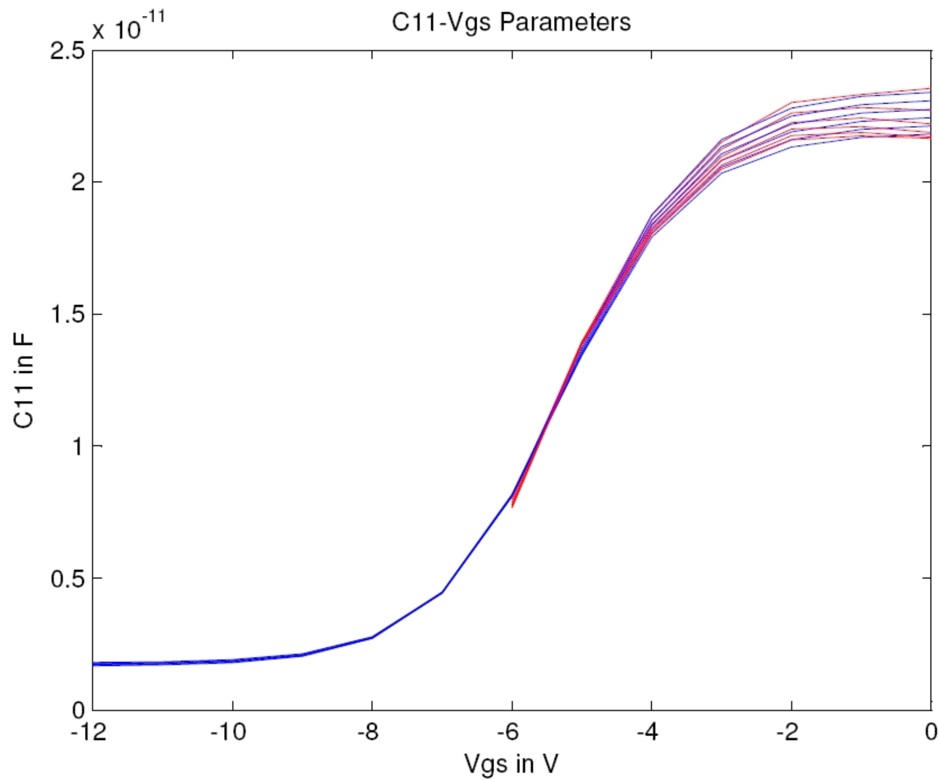


Figure 6-20: C_{11}-V_{GS} curves of measured and models for AlN/GaN MISFETs (blue: model, red: measurement)

Name	Value	Unit	Name	Value	Unit
C11o	2.10e-11	F	Deltds	3.0	V
C11th	0.16e-11	F	Vinfl	-5.0	V
Deltgs	5.56	V	Lambda	0.016	S

Table 6-7: Extracted initial AC parameters for AlN/GaN MISFETs

A MATLAB program was also developed for this purpose in order to allow extraction of the initial AC parameters. Fig. 6.20 shows the measured and model's C_{11}-V_{GS} curve for AlN/GaN MISFET and Table 6.7 lists the extracted initial AC parameters from the curve.

Gradient optimization was performed using the obtained initial AC parameter and external parasitic values. The purpose of the optimization was to achieve very good correspondence of measured and simulated S-parameters at almost all the bias points. Measured S-parameters on different bias points are imported into ADS using a data tool and were directly compared with the simulated S-parameters for optimization. Due to the high DC to RF dispersion effect in AlN/GaN MISFET and AlGaN/GaN HEMTs, fitting of S_{22} is normally difficult. In EEHEMT1 model there are dispersion parameters which enable S_{22} fitting and dispersion effect consideration inside the model. These are Gdbm, Cbs, Rdb, Vdsm, and Kbk. Optimization iteration on these parameters is very effective for fitting the S_{22} parameters. S-parameter fittings on 2 finger 2×100 μm AlN/GaN MISFET 3× offset device at different bias points are shown in Fig 6. 21.

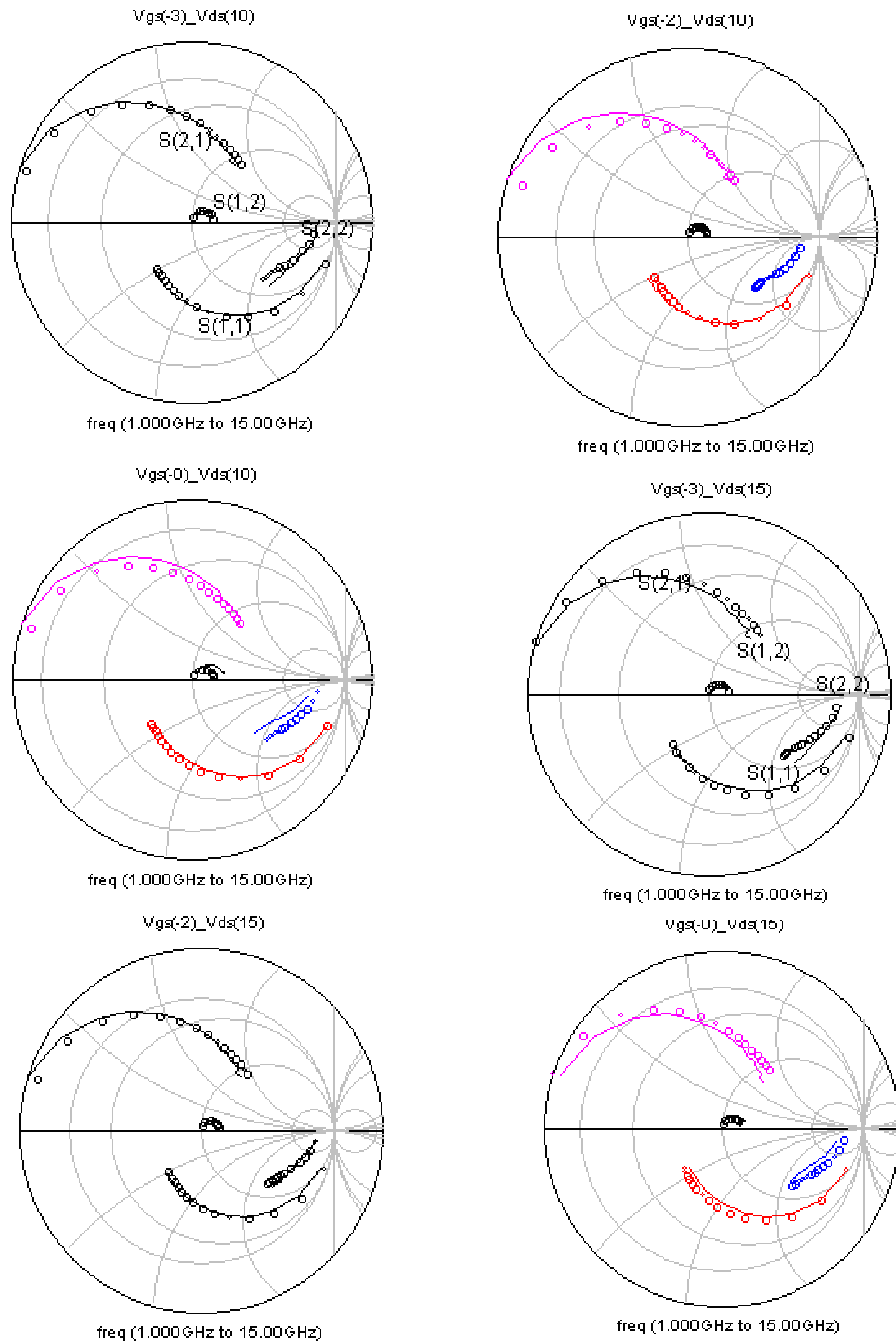


Figure 6-21: Measured and simulated S-parameters of 2 finger 2×100 μm AlN/GaN MISFETs on various bias points (V_{GS} = 0V, -1V, -2V & V_{DS} = 10V, 15V) in the frequency range of 1 GHz ~ 15 GHz. (Solid line : measurement, circle : simulation)

6.3.4 Verification of power characteristics of large signal model

The experimentally obtained power characteristics were compared to those obtained from the model to evaluate the model's validity. The measured power characteristics of the AlN/GaN MISFET were imported into ADS. The DC and small signal modeled EEHEMT1 model was simulated with the harmonic balance test bench in ADS as can be seen in Fig. 6.22.

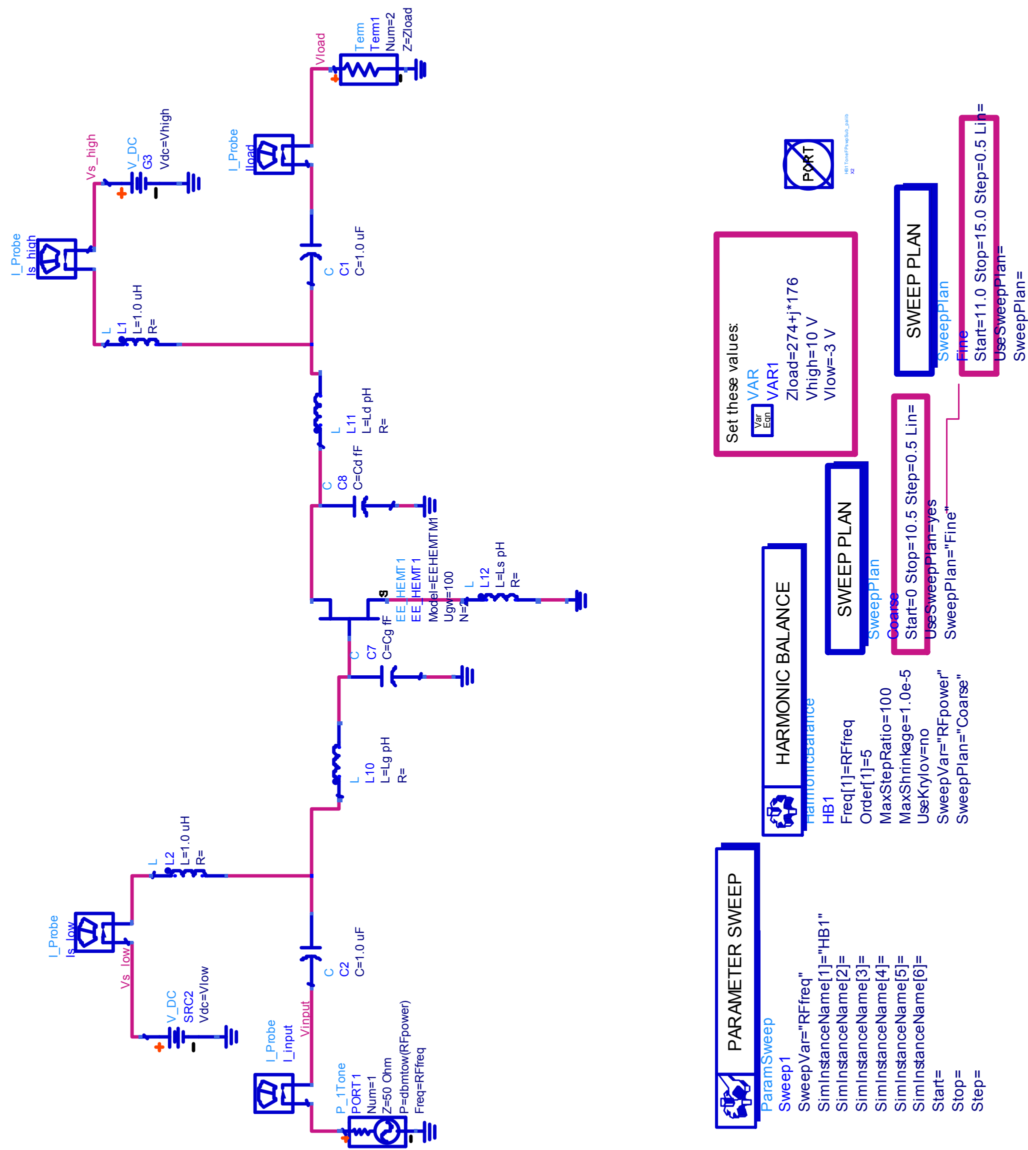


Figure 6-22**:** Harmonic balance test bench in ADS for simulation of power characteristics

Both the measurements and simulation were done at 2 GHz at various bias points. In both cases, the output load was matched for maximum power matching point. Figs. 6.23, 6.24, 6.25 and 6.26 show the measured and simulated power characteristics of 2 finger 2×100 μm 3× offset AlN/GaN MISFET with different bias points, which are V_{GS} = -2 V & V_{DS} = 10 V, V_{GS} = -3 V & V_{DS} = 10 V, V_{GS} = -2 V & V_{DS} = 15 V and V_{GS} = -3 V & V_{DS} = 15 V respectively. For all four bias points, the simulated power characteristics were well matched with the measured ones. From these results, it can be stated that the large signal modeling method based on the Agilent EEHEMT1 model works well for GaN-based HFETs

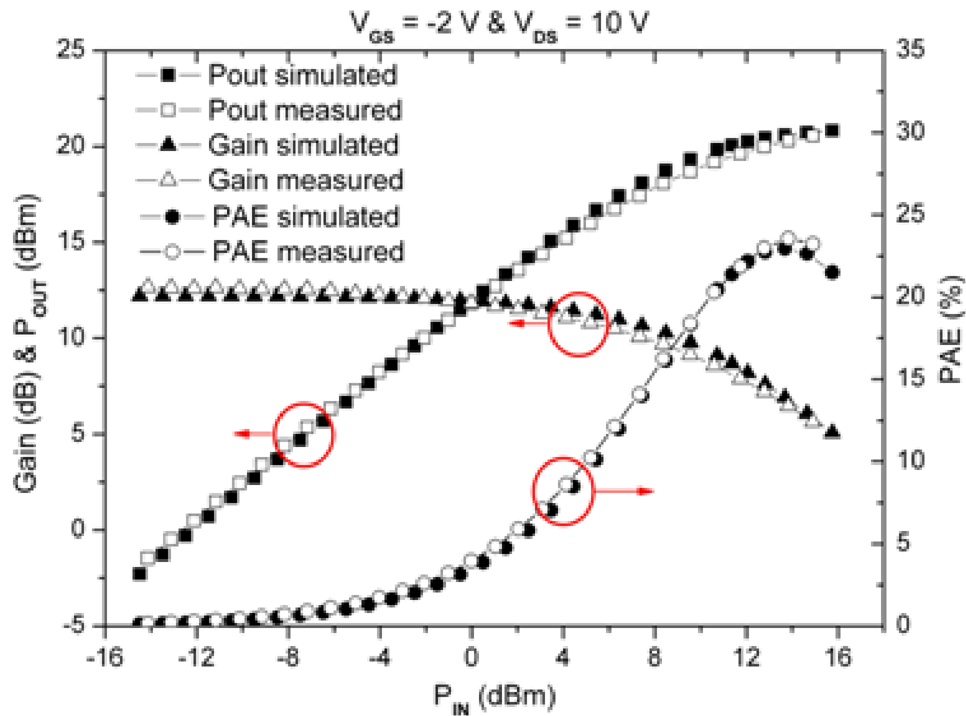


Figure 6-23: Power characteristics of AlN/GaN MISFETs (V_{GS} = -2V & V_{DS} = 10 V)

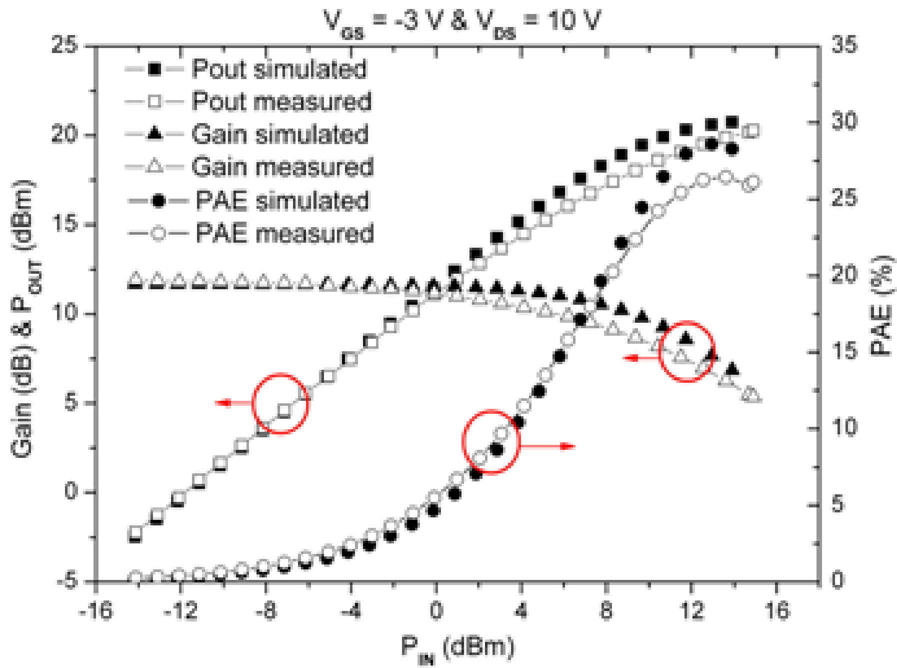


Figure 6-24: Power characteristics of AlN/GaN MISFETs (V_{GS} = -3 V & V_{DS} = 10 V)

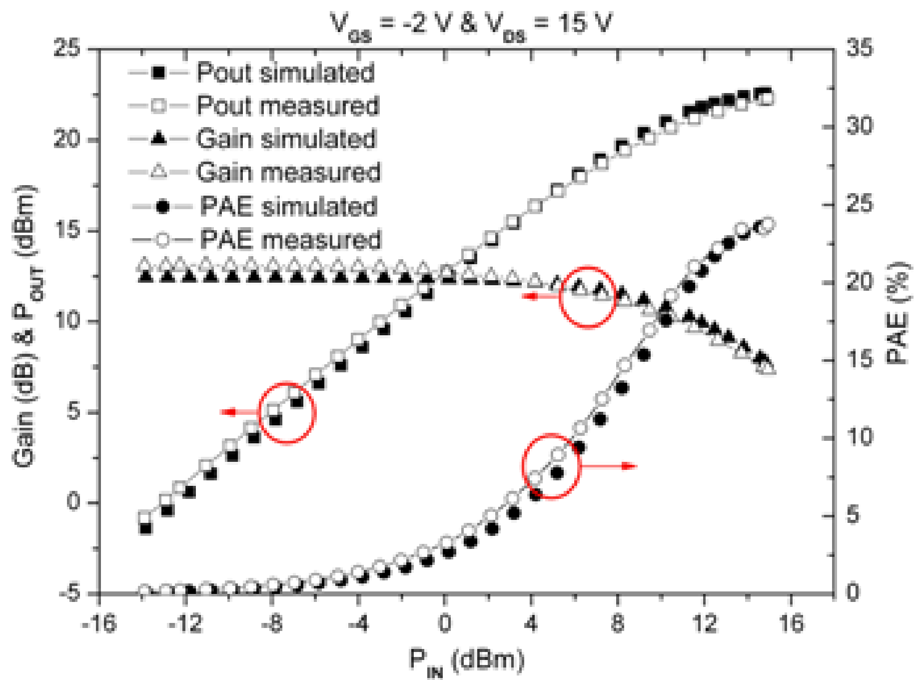


Figure 6-25: Power characteristics of AlN/GaN MISFETs (V_{GS} = -2V, V_{DS} = 15V)

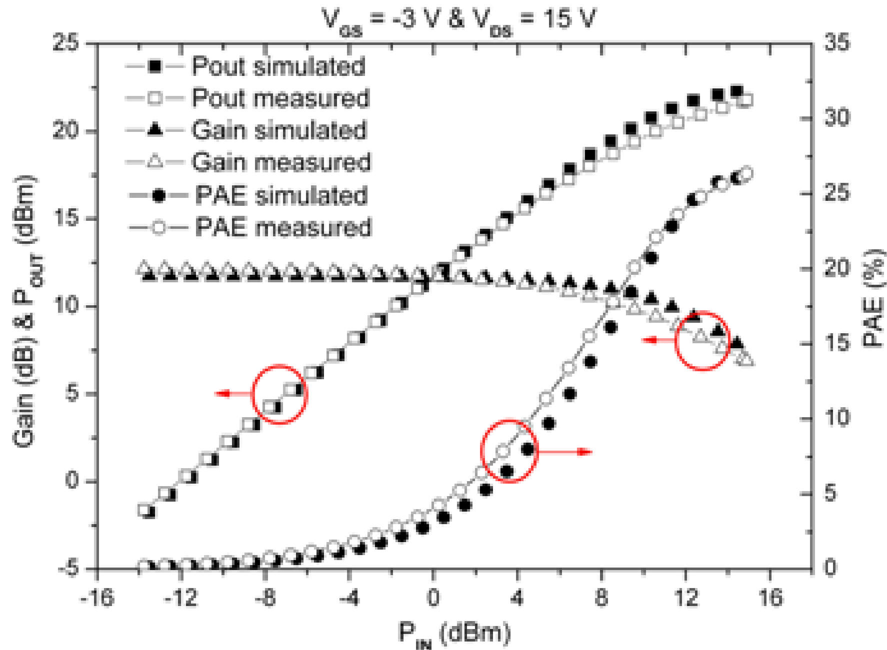


Figure 6-26: Power characteristics of AlN/GaN MISFETs (V_{GS} = -3V, V_{DS} = 15V)

6.4 Summary

In this chapter, small and large signal modeling methods of AlN/GaN MISFET have been presented. Both for small and large signal modeling, an ADS-based non-linear optimization technique was used to obtain accurate matching and save time and effort. For small signal modeling, a physical equivalent circuit model was used with 14 intrinsic and extrinsic elements. Extraction of equivalent circuit elements was performed in two steps. First the extracting extrinsic elements were extracted by two step cold FET modeling, and then the intrinsic elements were extracted by de-embedding the parasitic elements with the help of a 2-port matrix transformation. The extracted elements were evaluated with the help of a non-linear optimization tool and very accurate fitting with measured s-parameters was achieved at different bias point.

The Agilent EEHEMT1 semi-analytical model was utilized for large signal

modeling of AlN/GaN MISFETs, since this model contains several parameters which account for self heating and dispersion effects. Using a non-linear optimization technique, accurate fitting of the large signal model to measured data was achieved. Self heating and dispersion effects in AlN/GaN MISFET could be modeled well using the above discussed approaches. The DC and small signal fitted EEHEMT1 model was verified by comparison with actual measurement data of the power characteristics. The developed model could predict the power characteristics of AlN/GaN MISFETs well in terms of Power Added Efficiency (PAE), output power and power gain. Overall, small and large signal modeling of the AlN/GaN MISFET has been successfully developed and investigated. The ADS-based non-linear optimization technique allowed the entire modeling process to be simpler and more accurate.

CHAPTER 7
Development of III-Nitride HFET MMICs

7.1 Introduction

In this chapter, the design, simulation, fabrication and measurement of AlGaN/GaN HEMTs based wideband balanced low noise amplifier MMICs are described. AlGaN/GaN HEMTs are promising devices for low noise applications, because they combine low noise figure performance with high breakdown voltage characteristics [7-1]. As a result, AlGaN/GaN HEMT devices can be a preferred choice in LNA front-ends due to the benefits obtained by the absence of RF limiting circuitry, which often degrades the noise performance of communication systems [7-2]. This chapter presents first the design, fabrication, characterization and modeling of passive components for MMIC design. The design procedure, fabrication, and characterization of a wideband AlGaN/GaN HEMT MMIC LNA are presented next in case of a balanced amplifier configuration utilizing 4-finger CPW Lange couplers.

7.2 Development of the Passive Components for GaN-based MMIC technology

In this section, the design, fabrication, characterization and modeling of the passive components used in MMICs are described. Passive components are necessary in MMICs for matching, DC blocking and biasing.

Passive MMIC components can be in lumped or distributed form. The choice of

lumped or distributed elements is dependent on the design frequency, chip size and corresponding parasitics. At frequencies below 20 GHz, lumped elements are the preferred choice since they occupy much smaller space (their dimensions are $\leq \lambda/4$) than distributed elements which are λ/4 or longer. For higher frequencies, the distributed elements are preferred due to their small size and relatively modest parasitics compared with lumped components. Most of the GaN-based MMIC designs are reported so far in X- and Ku-band (7~18 GHz) or below. Therefore, lumped elements are the preferred choice for such MMICs.

The most commonly used lumped elements are the interdigital capacitor, the MIM (Metal-Insulator-Metal) capacitor, the spiral inductor, the spiral transformer and the thin film resistor. In the following sections, the realization of MIM capacitors and spiral inductors will be discussed.

7.2.1 Spiral inductors

Spiral inductors are normally used for matching and biasing purposes in MMIC design. The fabricated spiral inductors had values in the range of 0.84 nH to 8.11 nH, which are appropriate for designing matching networks. Figure 7.1 shows the photograph of a fabricated spiral inductor with an inductance value of L = 0.84 nH. The width and spacing of the lines were 7 μm while the number of turns was 10. The resonance frequency of this inductor is higher than 40 GHz. There are three design parameters for the spiral inductor; width of the lines, spacing (or gap) between them and number of turns. For smaller dependence of the fabrication on processing, the width and gap of the lines were set to have the same value and were 5 μm, 6 μm and 7 μm. The number of turns was

i n

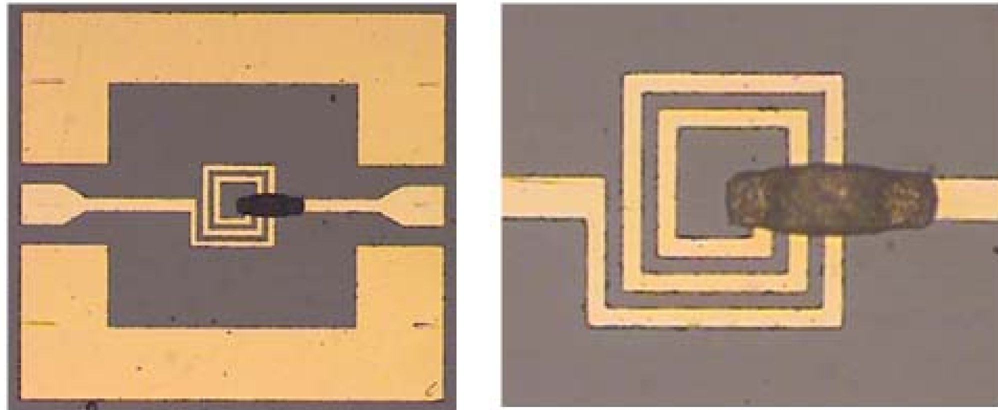


Figure 7-1: Spiral inductor with 10 turns and a line and space width of 7 µm

the range of 10 to 30 with a step size of 4 turns. The interconnection between the center of the inductor and the other circuit components was achieved by airbridge.

The measured inductance values are shown in Figure 7.2 and were found to be proportional to the square of the number of turns. ($L \sim turns^2$) The proportionality factor

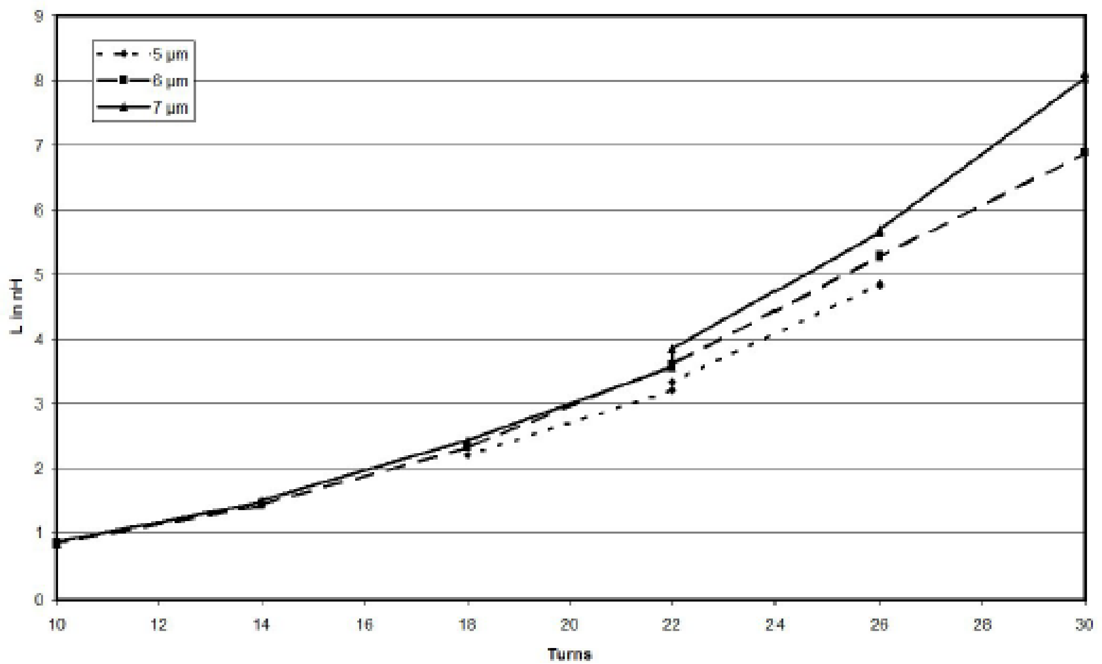
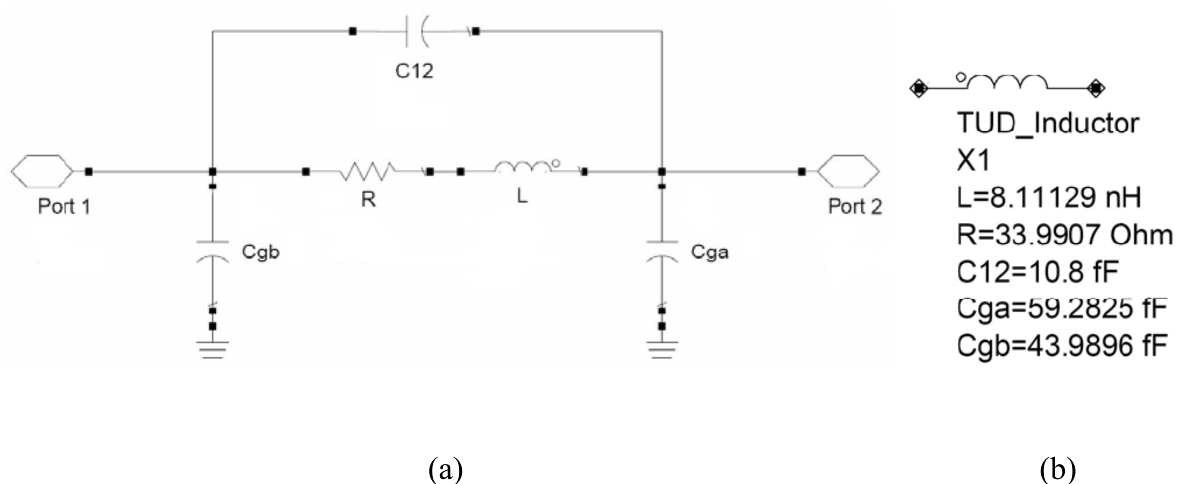


Figure 7-2: Measured inductance value L with the function of the number of turns for 5, 6

and 7 µm width & gap spiral inductors

extracted from the measurements was found to be 7 pH/turns^2, 7.5 pH/turns^2 and 8 pH/turns^2 for the 5 µm, 6 µm and 7 µm inductors, respectively. The 6 µm and 7 µm structures were preferred in the circuit design considering their relaxed photolithography needs.

The fabricated spiral inductors can be modeled using five equivalent circuit elements as shown in Figure 7.3 (a). The circuit element values for a 7 µm spiral inductor (7 µm line width and gap between lines) with 30 turns are shown in Fig. 7.3 (b). By using the optimization routine of Agilent ADS for fitting the measured S-parameters and simulated S-parameters of an inductor of this geometry one can find its inductance and parasitic components. The results of S-parameter measurements and simulations for a 7 µm size 10 turn spiral inductor are shown in Figure 7.4. Very good agreement is shown between the measured inductance values and those predicted by simulation.



(a) (b)

Figure 7-3: (a) Equivalent circuit model for spiral inductors and (b) example equivalent circuit element values for 7 µm size 30 turn spiral inductor

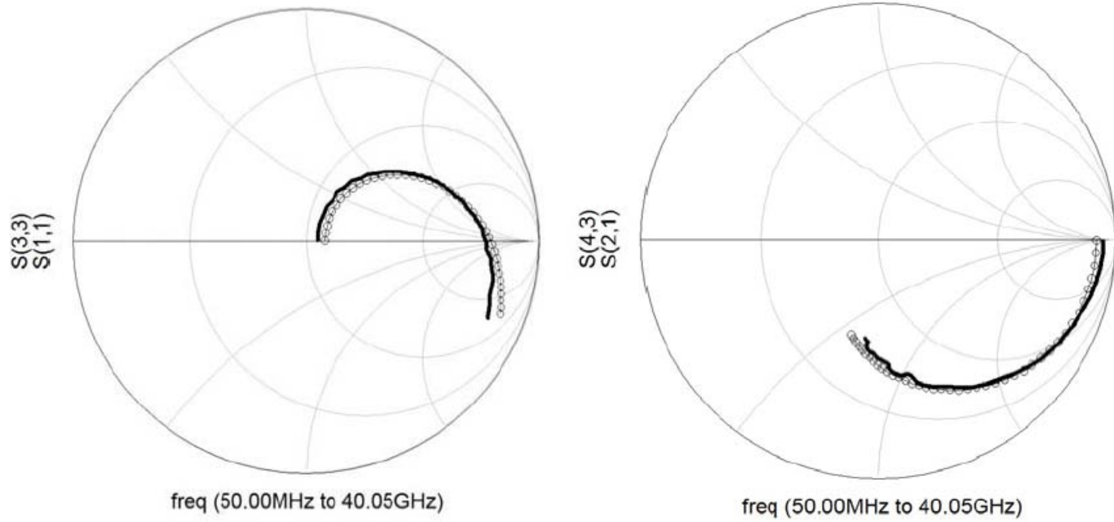


Figure 7-4: Simulated from model and measured S-parameters for the spiral inductor with 7 µm size 10 turns.

An essential criterion for the applicability of coplanar spiral inductors in circuit design is the value of the quality (Q) factor of the component [7-3]. The Q-factor is defined as follows.

$$Q = \frac{\mathrm{Re}(Z_{11})}{\mathrm{Im}(Z_{11})} \tag{7.1}$$

where Z_{11} is a Z-parameter of the spiral inductor which can be found by transformation from the measured S-parameters. The Q-factor for the 7 µm size inductor with 0.84 nH inductance (10 turns) was found to be 7 at 15 GHz, while the Q-factor for the 7 µm size inductor with 8.1 nH inductance (30 turns) was 3 at 3 GHz. When the inductance is increased, the Q-factor is decreased in agreement with the theoretically predicted trends [7-4].

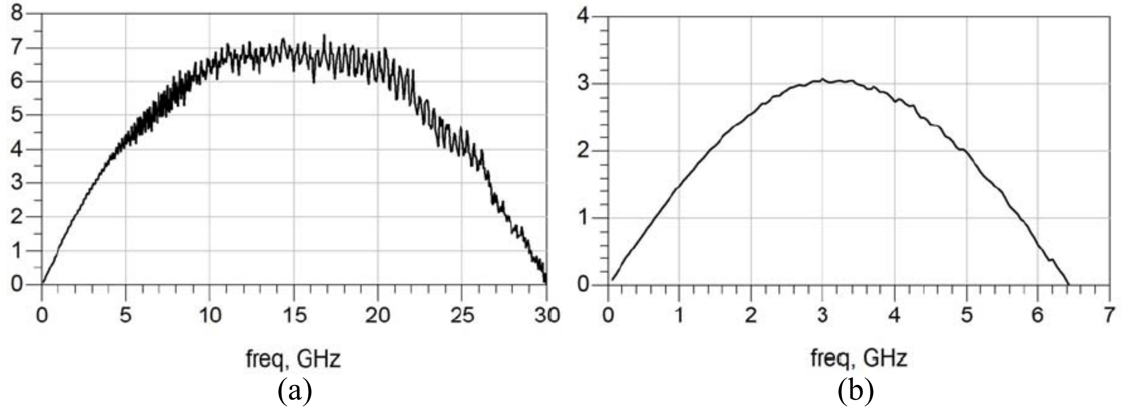


Figure 7-5: Measured Q-factor of 7 μm size spiral inductors with (a) 10 turns and (b) 30 turns

The resonance of the spiral inductors occurs when the reactance of its parasitic capacitance balances out the reactance of the inductance. The resonance frequency is defined as

$$f_{resonant} = \frac{1}{2\pi\sqrt{LC_{parasitic}}} \tag{7.2}$$

where L is the inductance and $C_{parasitic}$ is the parasitic capacitance of the spiral inductor.

At frequencies larger than the resonant frequency, the parasitic capacitance becomes dominant and the spiral inductor is not anymore inductive. The resonant frequency decreases as the number of turns increases or equivalently speaking, the inductance increases as can be seen in Fig. 7.6.

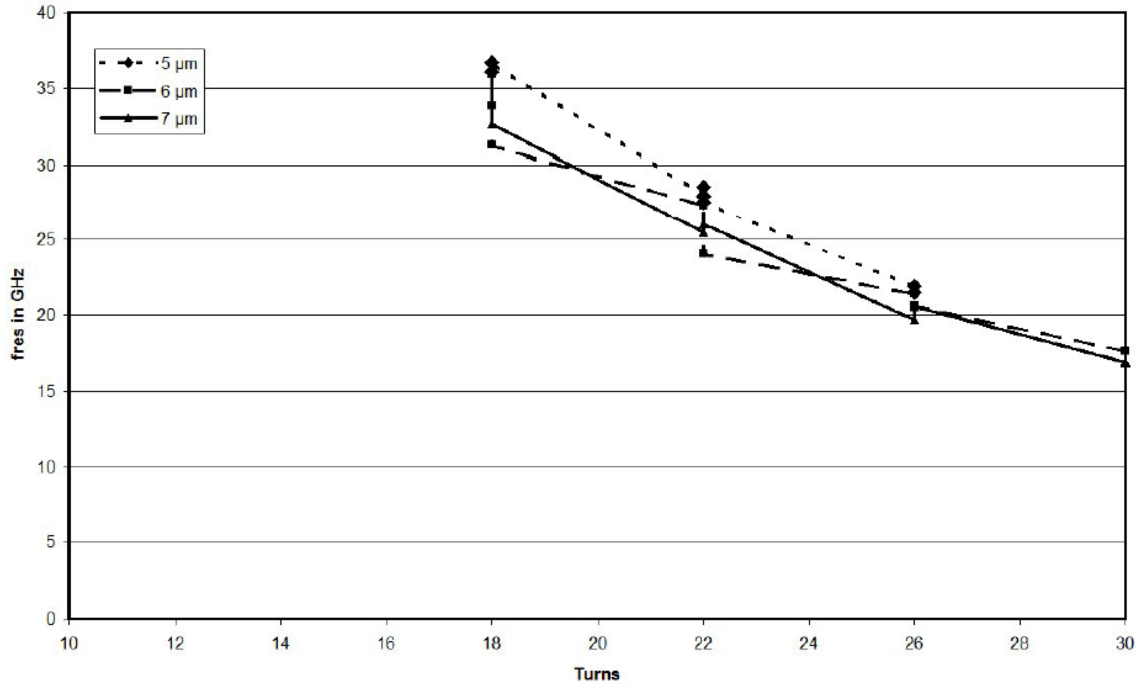


Figure 7-6: Measured resonant frequency of the spiral inductors vs. number of turns

7.2.2 MIM capacitors

Metal-insulator-metal (MIM) capacitors have an insulator between two metal layers for achieving the desired capacitance. Si_3N_4 and SiO_2 are normally used as an insulator. MIM capacitors are commonly used in MMIC technology, since they permit obtaining a wide range of capacitance values. MIM capacitors are however complex to fabricate, since they require deposition of two metal layers as well as realization of an insulator layer together with air-bridge processing. The fabricated MIM capacitors in this work have values in the range of 457 fF to 8.46 pF. Fig. 7.7 shows the microscopic images of different size fabricated MIM capacitors. The thicknesses of the bottom and top metal layers are 622 nm and 421 nm, respectively. 222 nm thick Si_3N_4 was used as an insulator. The capacitance value depends on the permittivity and thickness of the Si_3N_4

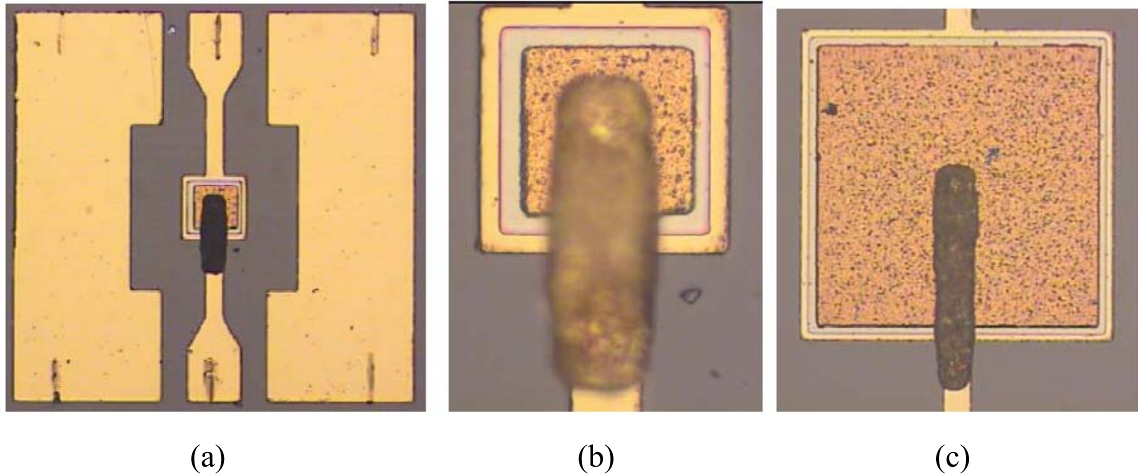


Figure 7-7: Microscopic images of the fabricated MIM capacitors with a size of (a) & (b) 40×40 μm² (C = 457 fF) and (c) with a size of 180×180 μm² (C = 8.46 pF)

dielectric, as well as the size of the top metal plate.

In this work, different size MIM capacitors (40 μm × 40 μm to 180 μm × 180 μm) were fabricated and characterized. The measured capacitance of the MIM capacitors is

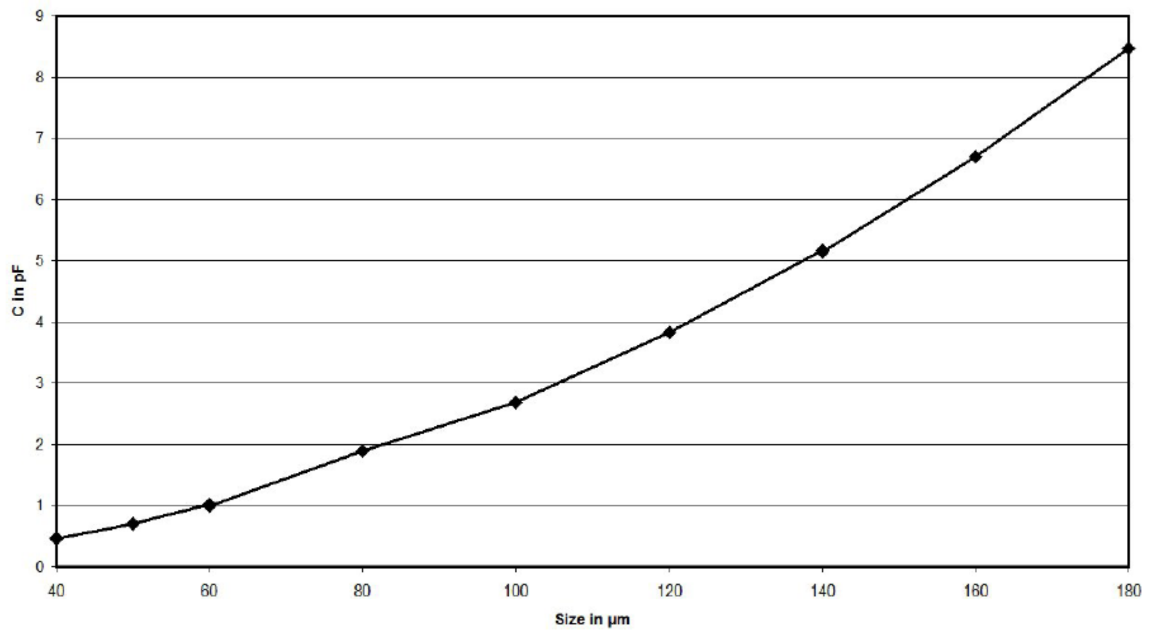
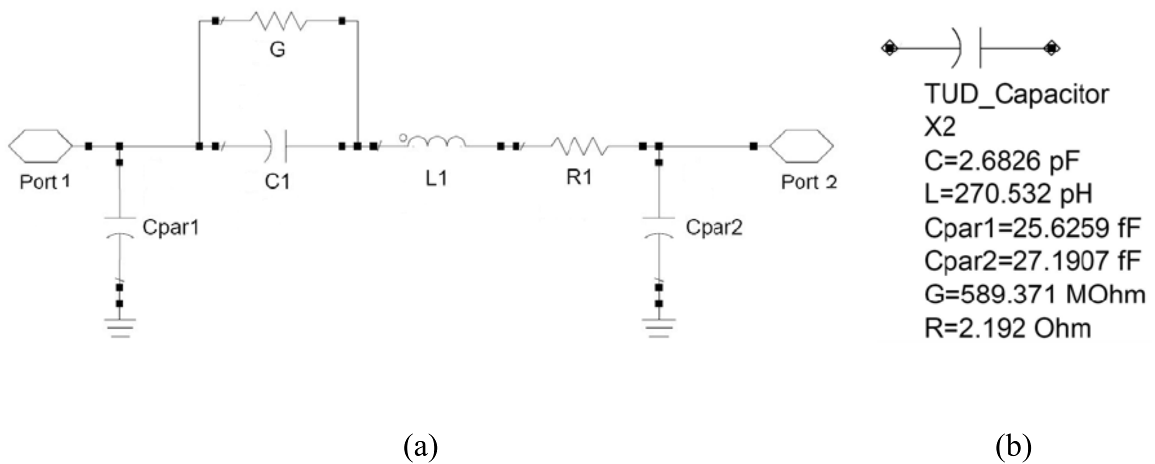


Figure 7-8: Measured capacitance of the various sizes of the MIM capacitor.



(a) (b)

Figure 7-9: (a) Equivalent circuit model for MIM capacitors and (b) example equivalent circuit element values for 100 μm ×100 μm MIM capacitor.

shown in Fig. 7.8. As can be seen, the capacitance is proportional to the area of the MIM capacitor. (*C*~*area*) The proportionality factor extracted from the graph is 263 fF/μm².

MIM capacitors can be modeled with six equivalent circuit elements as can be seen in Fig. 7.9 (a). Example circuit element values for a 100 μm × 100 μm MIM capacitor are shown in Fig. 7.9 (b). Fitting of the measured and simulated S-parameters was achieved

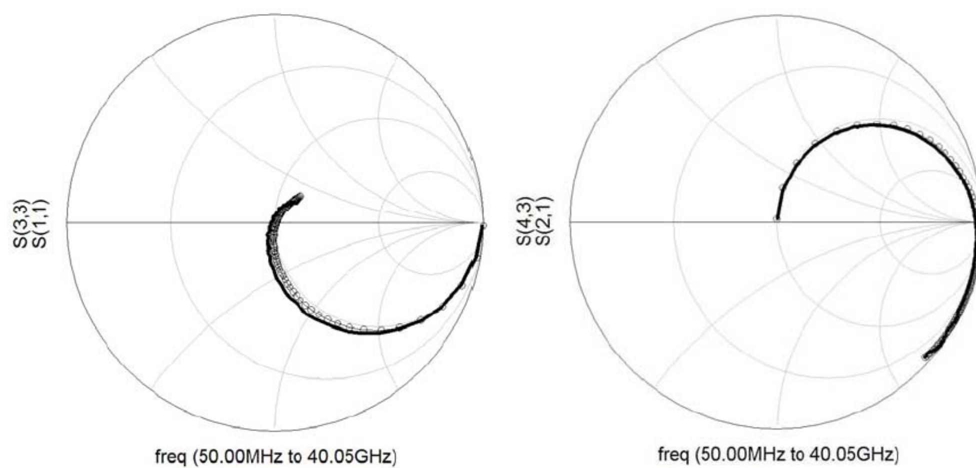


Figure 7-10: Simulated from model and measured S-parameters for the MIM capacitor with 40 μm× 40 μm size.

using the optimizer of Agilent ADS and allowed characterization of the capacitance C and parasitic component values. The measured and simulated S-parameter values of 40 μm× 40 μm MIM capacitors are shown in Figure 7.10. The results show very good agreement between the measured and predicted by simulation capacitance values.

The resonant frequency of the MIM capacitors can be defined same as spiral inductors (7.2). Fig. 7.11 shows the resonant frequency versus the size of the MIM capacitor. The resonance frequency for the smallest capacitor (40 μm× 40 μm) was 26 GHz. As the size of the capacitor increases, its resonant frequency decreases.

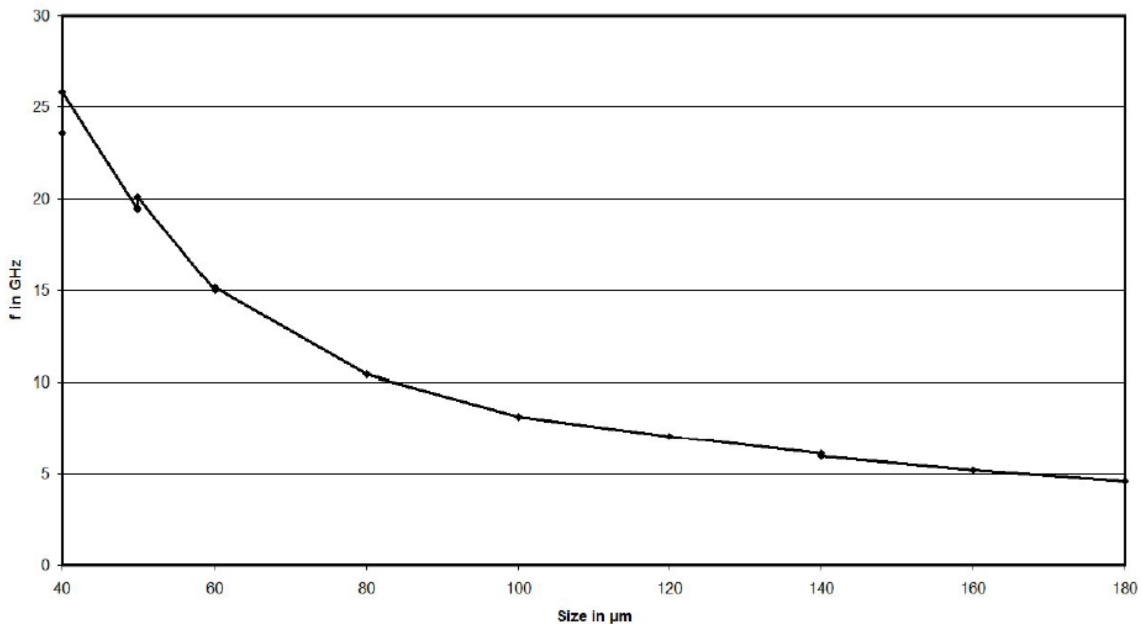


Figure 7-11: Measured resonant frequency of the MIM capacitors with various sizes.

7.3 Wideband Balanced AlGaN/GaN HEMT Low Noise Amplifier MMIC

AlGaN/GaN HEMT-based Monolithic Microwave Integrated Circuit (MMIC) LNAs have been reported with operating frequency at X-band and below [7-5]-[7-9], as well as with wideband frequency characteristics (3-18 GHz) [7-10]. AlGaN/GaN HEMT devices

are the preferred choice in LNA front-ends due to the benefits obtained by the absence of RF limiting circuitry, which often degrades the noise performance of communication systems [7-5]. In addition, the balanced amplifier configuration is usually preferred in LNA applications such as base-station transceiver front-ends because it presents several advantages over single-ended amplifiers: (1) improvement of 1 dB compression point by 3 dB, (2) inherent 50 Ω input/output matching due to the coupler presence, and (3) redundancy i.e. if one of amplifiers fails, the balanced amplifier unit will still operate with reduced power gain. This section presents the design procedure, fabrication, and characterization results of a wideband AlGaN/GaN HEMT MMIC LNA with balanced amplifier configuration utilizing 4-finger CPW Lange couplers.

7.3.1 AlGaN/GaN HEMTs for MMIC design

$Al_{0.3}GaN_{0.7}$/GaN HEMT layers used in the balanced amplifier were grown by RF-assisted nitrogen plasma Molecular Beam Epitaxy (MBE) on semi-insulating (0001) 4H-SiC substrates in HRL. TLM measurements of ohmic contacts (evaporated Ti/Al) showed contact resistance of 0.7 Ω-mm and sheet resistance of around 350 Ω. Ni/Al T-gate HEMTs with 0.15 μm length and a 1.2 μm source to drain spacing were fabricated by electron beam lithography. The photographs of the fabricated devices with different size are shown in Fig. 7.12. The 4-finger 75 μm gate width device, used in the first stage of the LNA, showed a minimum noise figure (F_{min}) of 0.97 dB at 10 GHz and F_{min} less than 1.4 dB across the 3 – 21 GHz frequency range. The 6×100 μm gate finger device used for the second stage had F_{min} of 1.57 dB with an associated gain of 5.66 dB and F_{min} less than 1.93 dB over the same frequency range [7-11] as can be seen in Fig. 7.13. A coplanar

waveguide design was used for the amplifier transmission lines since it offers simplicity by avoiding the difficulty involved in via-hole processing on SiC substrates. CPW lines for signal and biasing paths had 5 μm-thick metal lines for low RF losses and high current density capability.

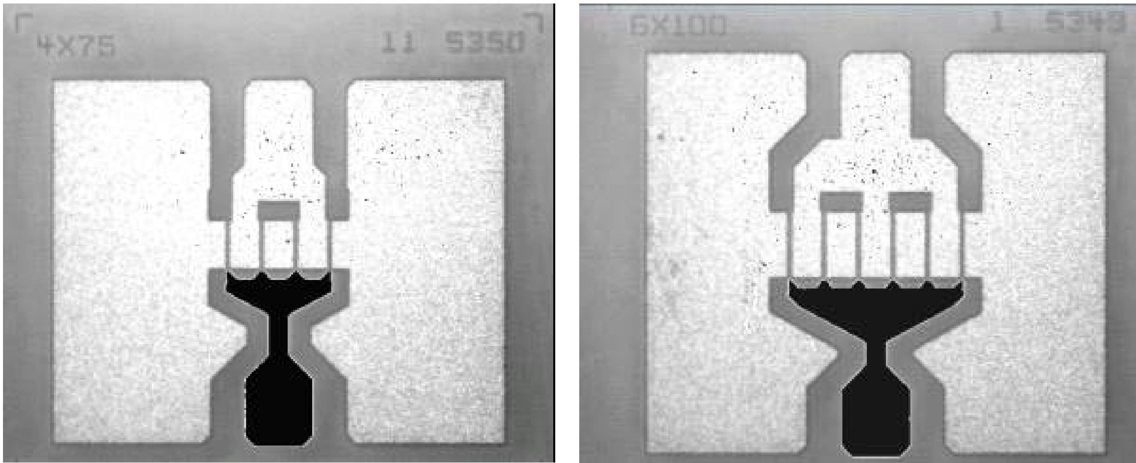


Figure 7-12: Photographs of $Al_{0.3}Ga_{0.7}N$ HEMTs with 4 finger 75 μm device and 6 finger 100 μm device.

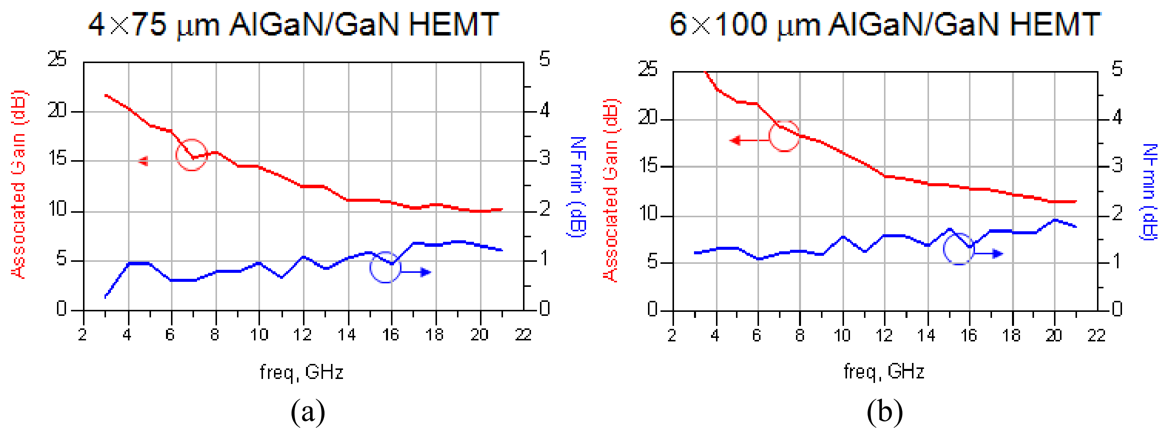
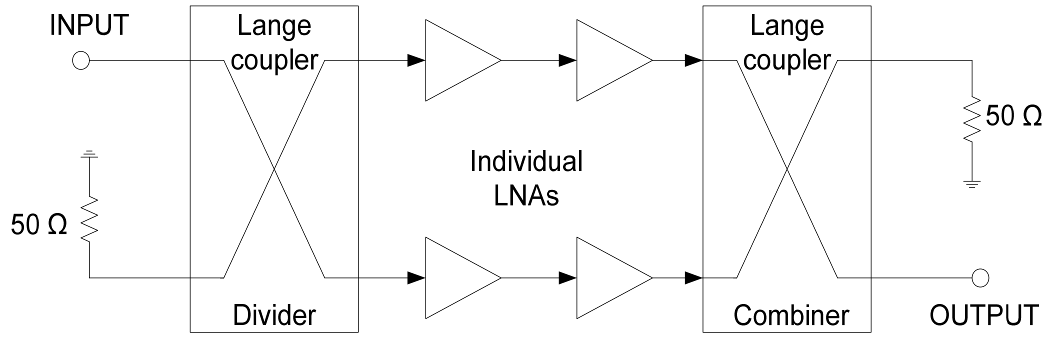


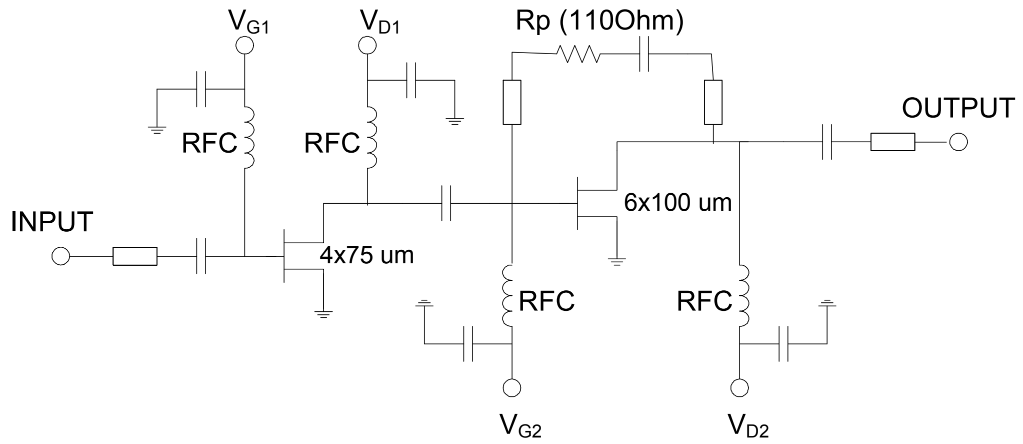
Figure 7-13: Associated gain and minimum noise figure of 4×75 μm AlGaN/GaN HEMT (a) and 6×100 μm AlGaN/GaN HEMT (b)

7.3.2 LNA design and simulation: individual LNA design

As can be seen in Fig. 7.14, the wideband amplifier design is based on the use of individual low noise amplifiers consisting of 2-stages; the first stage used a 4 × 75 μm gate AlGaN/GaN HEMT for low noise and high gain while the second stage used a 6 × 100 μm gate device for higher gain and linearity. The circuit design was based on measured S-parameters and noise parameters for the first and second stage devices under biasing conditions, corresponding to V_{DS} = 5 V with I_{DS} = 67 mA and V_{DS} = 10 V with I_{DS} = 240 mA respectively. Parallel feedback with an 110 Ω on-chip resistor and capacitor was used in the second stage for improving gain flatness and bandwidth. The EM electrical characteristics of all lumped elements including spiral inductors and metal-insulator-metal (MIM) capacitors were simulated with Agilent MOMENTUM. Agilent ADS was used for simulating the individual LNAs and the simulation results of the individual LNAs are shown in Fig. 7.15 and Fig 7.16. Matching of individual LNA stages was optimized for low noise and flat gain characteristic rather than input and output voltage standing wave ratio (VSWR), which turned out to be high. Since the VSWR characteristic of the balanced amplifier is dependent on the coupler, this should not be a handicap for the circuit. The simulated gain was found to be around 20 dB and had only 4.3 dB fluctuation over the 4-20 GHz frequency range. The noise figure was less than 2.6 dB at the same frequency range. As explained earlier, the input and output VSWR (see Fig. 7-16) were high due to the fact that prime emphasis was placed on noise matching of the balanced amplifier. However, the overall VSWR was much smaller (< 2.4) while maintaining the same gain and noise characteristics.



(a)



(b)

Figure 7-14: Circuit schematics of balanced (a) and individual two-stage low noise amplifier design (b)

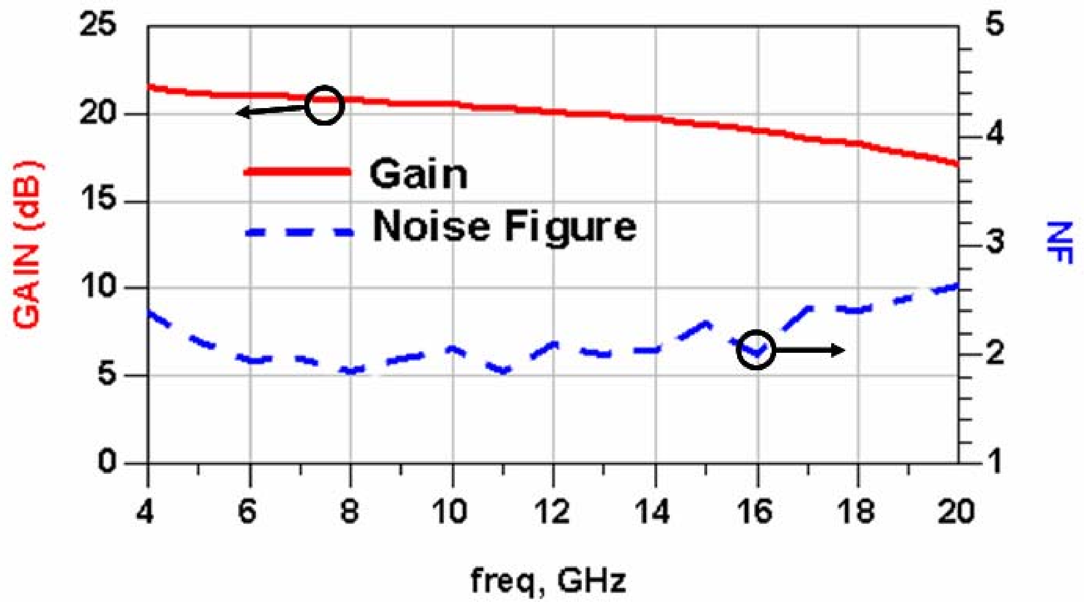


Figure 7-15: Simulated gain and noise figure of individual LNAs

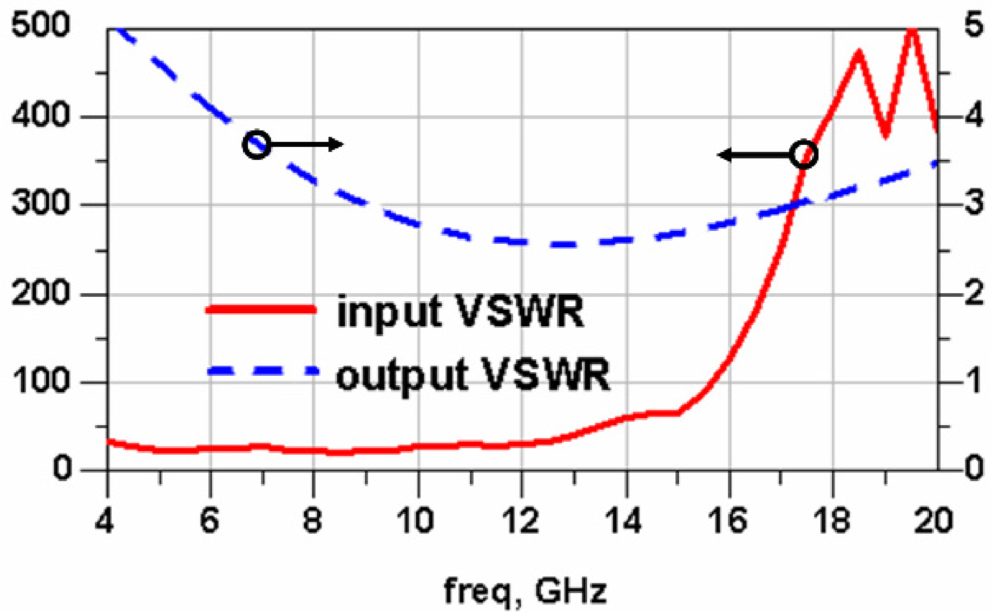


Figure 7-16: Simulated input and output VSWR of individual LNAs

7.3.3 CPW-based Lange couplers

The Lange coupler [7-12] can be made of four or six coupled lines with interconnections and could provide strong 3 dB coupling. Its design tends to compensate the differences in even- and odd-mode phase velocities and as a result, bandwidth can be very high. Lange couplers on CPW were recently implemented based on classical strip line design methods [7-3],[7-14]. In this work, a traditional microstrip design method with airbridge interconnection between lines was used. As can be seen in Fig. 7.17, the critical dimensions of the coplanar Lange coupler are the coupled line length (L), coupled line width (W), gap between lines (S), and distance (D) from coupled lines to ground plane. The L, W, and S values were calculated based on computed values of the even- and odd-mode impedances and effective dielectric constants using the assumption of coupled microstrip lines. These values were then adjusted for CPW configuration using optimized values of the distance D obtained with Agilent MOMENTUM. Transmission line loss was considered and the height of the air-bridge was assumed to be 10 μm in the simulations. The optimum coupler values are listed in Table 1. In Fig. 7.18, the simulation results are shown for all four ports of the coupler. The coupling bandwidth covered 6.5 - 18.5 GHz and was centered at 13 GHz with amplitude of -3.3 ± 0.8 dB.

Dimension	L	D	W	S
Values	2.5 mm	15 μm	30 μm	10 μm

Table 7-1: Dimensions of the CPW Lange Coupler

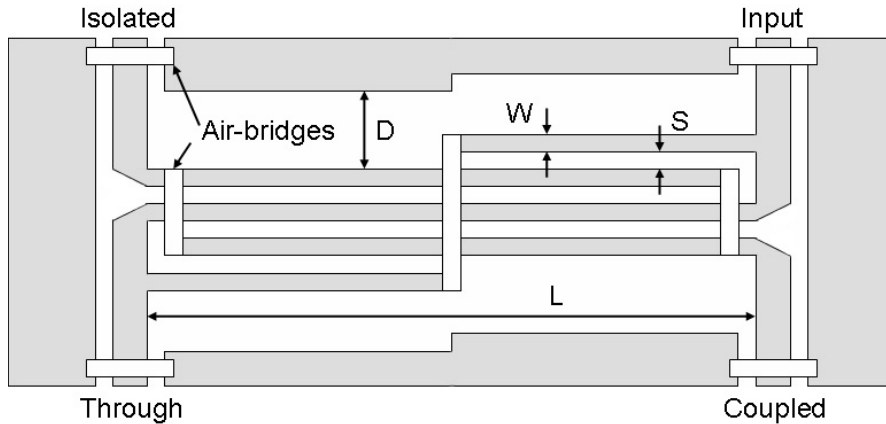


Figure 7-17: Schematic of a four-finger CPW Lange coupler

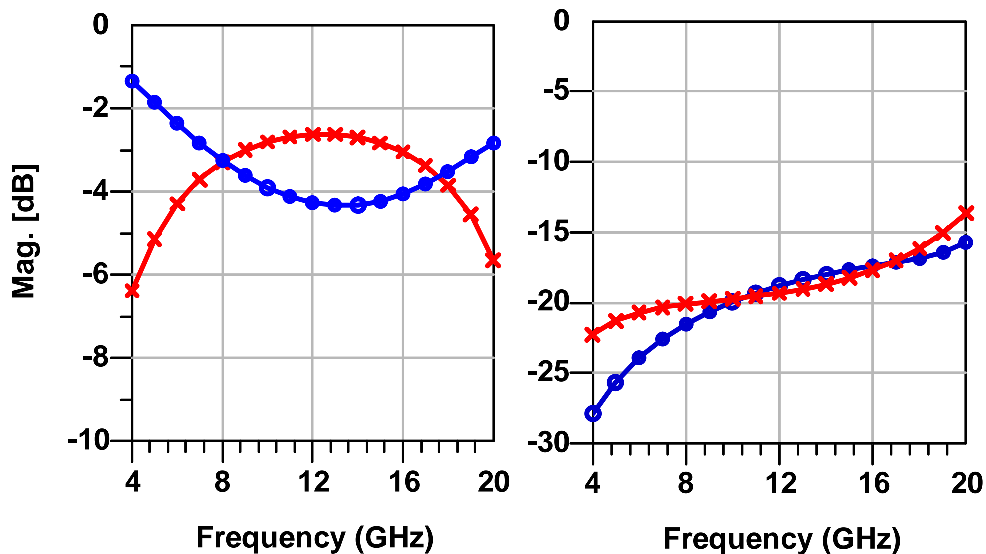


Figure 7-18 (left) Simulated through (o) and coupled (x), (right) Simulated return loss (o) and isolated (x) port of the CPW Lange coupler.

7.3.4 Wideband balanced LNA MMIC

The wideband amplifier was designed based of the 2.5D simulation results of the CPW Lange coupler and employed two identical individual LNAs connected to the coupler input and output as can be seen in Fig. 7.19. The isolated ports of the Lange coupler were terminated by on-chip thin-film 50 Ω resistors. Figs. 7.20 and 7.21 show the

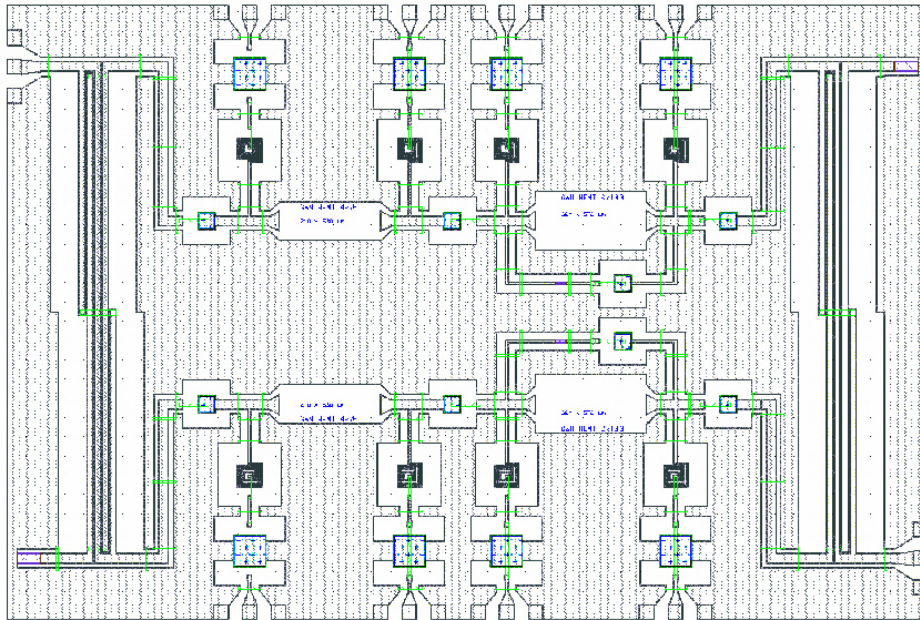


Figure 7-19: Layout of the AlGaN/GaN HEMT balanced LNA MMIC

simulated associated gain together with the noise figure and input and output VSWR of the balanced LNA. Compared with the individual LNA simulation results, gain flatness was improved but noise figure was slightly increased due to the use of the Lange coupler. Noticeable performance improvement was observed for the input and output VSWR which were found to be less than 2.4 over the frequency range of 4-20 GHz. This was due to the fact that the VSWR of the balanced amplifier is dictated by the coupler characteristics.

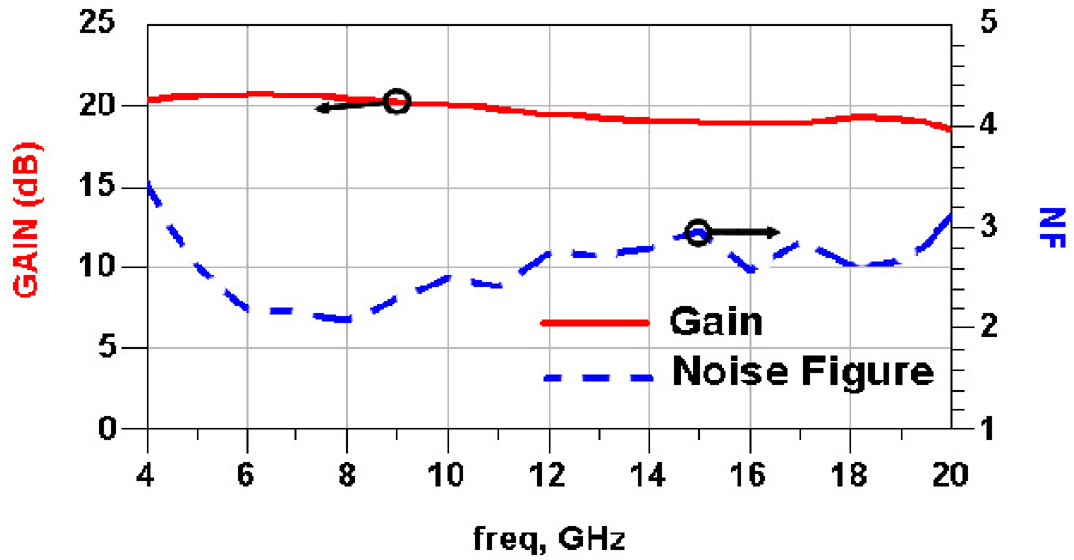


Figure 7-20: Simulated gain and noise figure of Balanced LNA

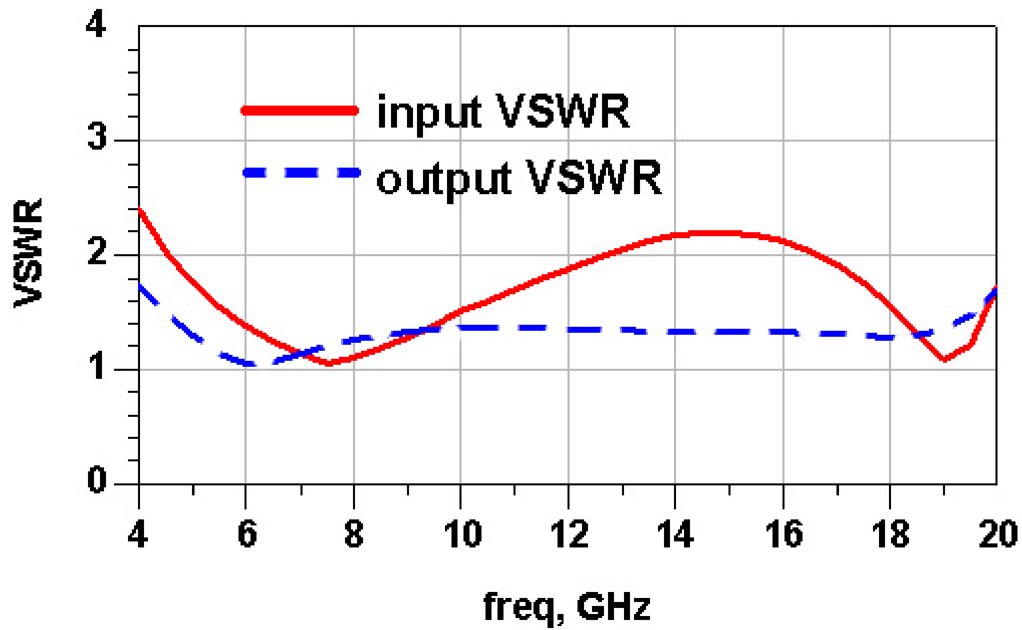


Figure 7-21: Simulated input and output VSWR of Balanced LNA

7.3.5 High frequency and noise characteristics of wideband LAN MMICs

A photograph of the fabricated chip is shown in Fig. 7.22. The amplifier chip size is 3187 μm × 4800 μm. The measured small-signal gain (S21) is shown in Fig. 7.23 for different amplifier bias points. The blue curve (squares) was measured with V_{DS} = 5 V

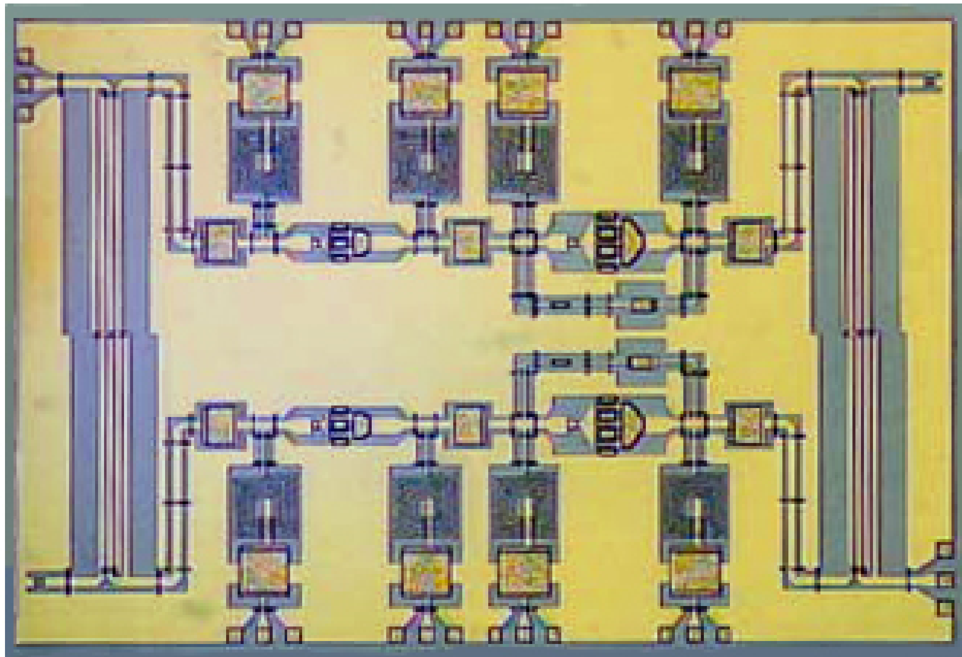


Figure 7-22: Photograph of the wideband HEMT LNA Chip (size: 3187 μm × 4800 μm)

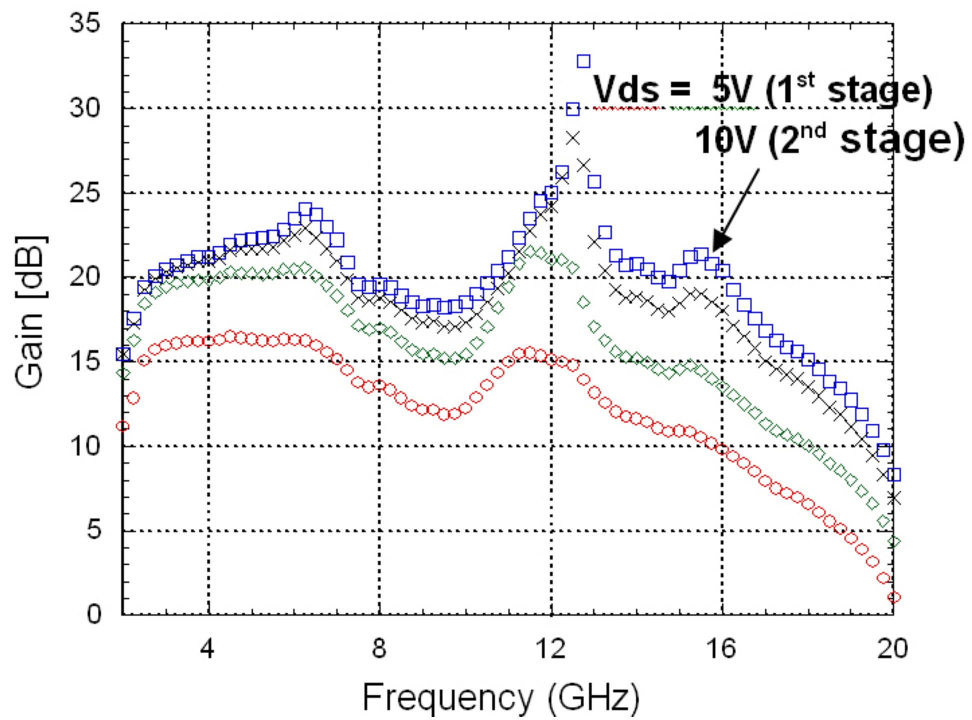


Figure 7-23: Measured Gain Characteristics of the Wideband Amplifier with various bias conditions.

for the 1st stage and V_{DS} = 10 V for the 2nd stage. The measured gain was about 20 dB with gain flatness of +/−3 dB over a wide bandwidth of 3 - 16 GHz.

The noise performance and associated gain of the amplifier are shown in Fig. 7.24. The data were taken with V_{DS} (1st stage) = 5 V and V_{DS} (2nd stage) = 10 V. The minimum Noise Figure was ~ 4 dB with an associated gain of 20 dB and the Noise Figure was less then 7.5 dB over the 4~20 GHz range. The measured noise was found to be 2 ~ 4 dB higher than the simulated values and the associated gain decreased drastically above 16 GHz, which was not expected by the simulation.

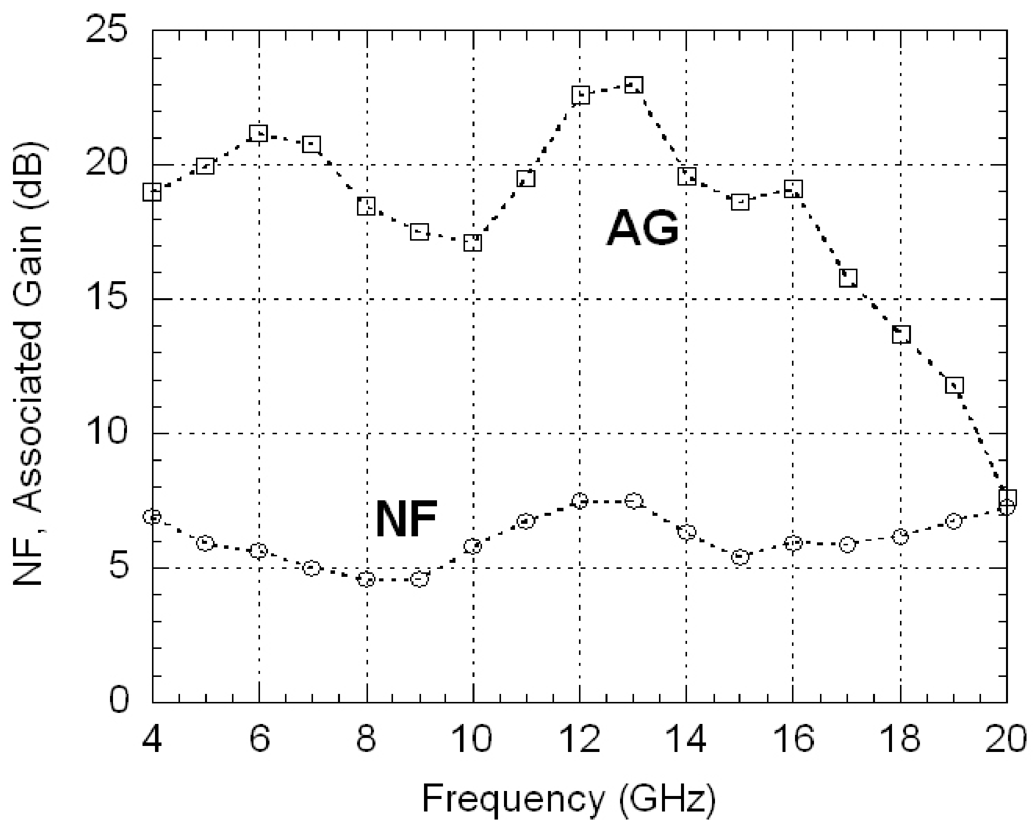


Figure 7-24: Noise performance and associated gain of the amplifier at V_{DS} (1st stage) = 5 V and V_{DS} (2nd stage) = 10 V.

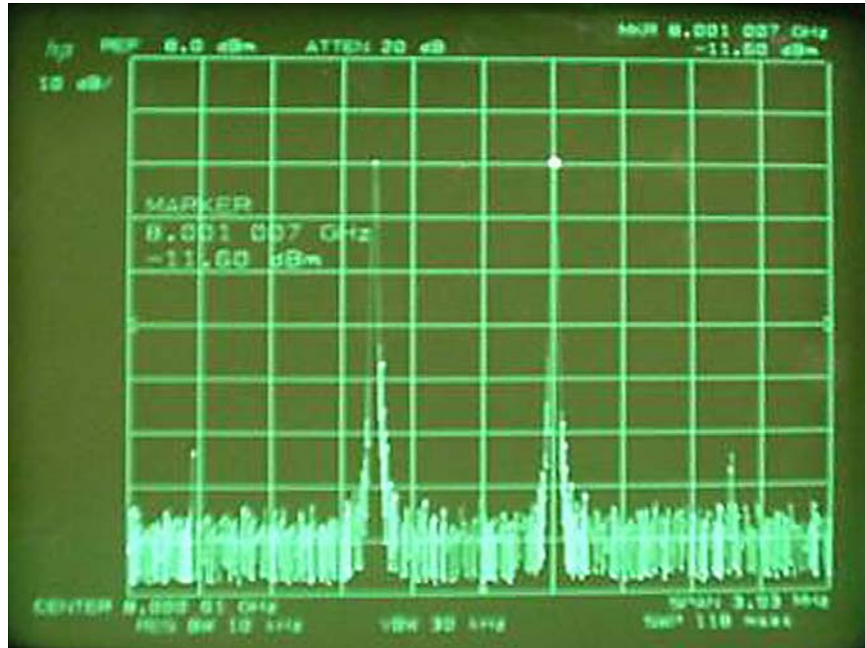


Figure 7-25: Spectra of two-tone signal at 8 GHz with tone spacing of 1 MHz offset.

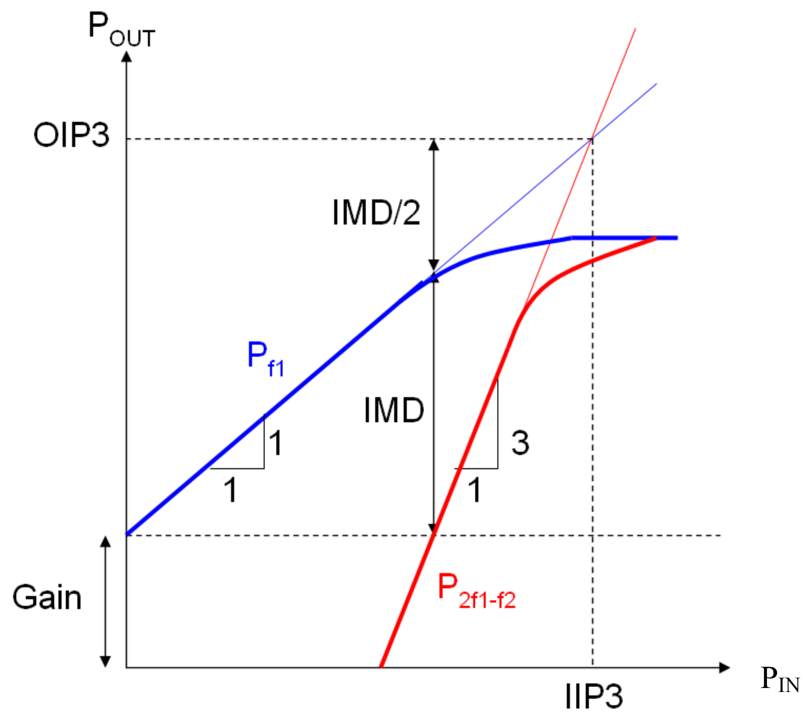


Figure 7-26: General two tone output power characteristics with IIP3, OIP3 and IMD definition

The main reason for the discrepancies between simulation and measured results was assumed to be the imperfect on-chip thin-film resistors used for 50 Ω terminations and the 100 Ω feedback resistors used in individual LNAs. These reduced the coupling bandwidth of the Lange couplers and gain flatness at frequencies over 16 GHz. Fig. 7.24 shows the spectrums of two-tone fundamental signals with a tone spacing of 1 MHz offset at 8 GHz and 3rd order intermodulations (IM3) at the Input power of -10 dBm. Intermodulation Distortion (IMD), which is the power difference between the fundamental signal and IM3 signal as can be seen in Fig. 7.26, was measured to be 59 dBc. Therefore, the output 3rd order intercept point (OIP3) can be calculated in the following way:

$$P_{out} = -11.5 \text{ dBm} + 20 \text{ dB (attenuation)} = 8.5 \text{ dBm} \quad (7.3)$$

$$\text{OIP3 (38 dBm)} = \text{Pout (8.5 dBm)} + \text{IMD/2 (59 dBc/2)} \quad (7.4)$$

The OIP3 value calculated using Eq. 7.4 was found to be equal to 38 dBm.

	Gain	Bandwidth	min NF	OIP3
This work	20 ± 3 dB	3 -16 GHz (13 GHz)	4 dB	38 dBm
G. A. Ellis et. al, IMS 2004 [7-10]	20 ± 2.5 dB	3 -18 GHz (15 GHz)	2.4 dB	37.8 dBm
D. Krausse et. Al, GAAS 2004 [7-7]	17 ± 2 dB	7.5 – 11 GHz (3.5 GHz)	1.81 dB	> 26 dBm
H. Xu et. al, MWCL 2004 [7-6]	10 ± 3 dB	4 - 8 GHz (4 GHz)	1.6 dB	24 dBm
S. Cha et. al, IMS 2004 [7-8]	16 ± 3 dB	0.5 – 5.5 GHz (5 GHz)	< 2.0 dB	43 dBm
R Schwindt et. Al, CSIC 2004 [7-9]	6.5 ± 2 dB	7 – 12 GHz (5 GHz)	2.5 dB	-

Table 7-2: Gain, bandwidth, noise and linearity characteristics of AlGaN/GaN HEMT based LNAs

Table 7-2 summarizes the gain, bandwidth, noise and linearity characteristics of the fabricated balanced LNA together with those of other reported AlGaN/GaN HEMT based LNAs. Comparing with other AlGaN/GaN HEMT-based LNAs, good wideband, linearity and low-noise performance was demonstrated by the developed AlGaN/GaN HEMT LNA. Furthermore, the LNA of this work is based on a balanced configuration which presents several advantages such as redundancy, low VSWR and easiness to cascade. All other MMICs listed in Table 7-2 correspond to a non-balanced configuration. The developed MMIC is the first balanced MMIC amplifier ever developed with GaN-based HFETs.

7.4 Summary

A balanced AlGaN/GaN HEMT MMIC LNA was demonstrated with broad bandwidth of 3-16 GHz and high gain of ~ 20dB for the first time at the moment of publication [7-15],[7-16], using a coplanar waveguide (CPW) Lange coupler. The MMIC LNA shows a minimum noise figure of 4 dB with an associated gain of 20 dB. 38 dBm of OIP3 was demonstrated at the frequency of 8 GHz. The results suggest that the balanced GaN HEMT LNA is a promising candidate for robust LNA applications such as transceiver front-ends.

CHAPTER 8

Design, Fabrication and Characterization of AlGaN/GaN Superlattice Diodes

8.1 Introduction

Semiconductor superlattices (SLs) proposed by Esaki-Tsu [8-1] have been shown to exhibit negative differential conductance (NDC) due to the Bragg reflection of miniband electrons. The NDC of SL induces traveling dipole domains and self-sustained current oscillation. Recently, high frequency oscillators were reported using GaAs-based SLs. Microwave radiation up to 103 GHz was observed from GaAs/AlAs SLs [8-2],[8-3] and InGaAs/InAlAs superlattice oscillators generated a microwave signal at 55 GHz [8-4] and 74 GHz [8-5]. III-Nitrides are also a suitable material system for millimeter wave generation due to the benefits expected from them, such as high power, high breakdown voltage etc. Therefore, one can expect that $Al_xGa_{1-x}N$/GaN SLs can offer an advantage for generating high power mm-waves. $Al_xGa_{1-x}N$/GaN SLs have in fact been predicted theoretically to have the potential for generating THz-range signals [8-3]. This chapter presents a DC and capacitance study of experimentally investigated MOCVD grown GaN-based SLs and reports NDC and negative capacitance effects.

8.2 Theoretical Investigation and Superlattice Growth

Short-period AlGaN/GaN superlattices should provide harmonic electron oscillations at multiples of the fundamental Bloch frequency. Theoretical investigations

performed by our group and suggest that the traveling dipole domain oscillation frequency should be in the THz range. These conclusions agree with reported results such as shown in Fig. 8.1 [8-6]. The oscillation condition was satisfied with an aluminum composition x between 18% and 40% and a value for the sum of the barrier and quantum well thickness d of less than 50 Å [8-7]. Based on the above mentioned theoretical expectations, $Al_xG_{1-x}N$/GaN SL layers complying with the oscillation conditions were designed and grown by our in-house MOCVD on sapphire substrates. Three different designs were explored and are presented in this chapter. The superlattices consisted of 50 periods of AlGaN/GaN layers with a 15 Å thick AlGaN barrier layer of 34% Al composition and a 15 Å thick GaN well layer for design A. Design B had a thinner AlGaN barrier layer of 10 Å and a thicker GaN layer of 30 Å with lower Al composition

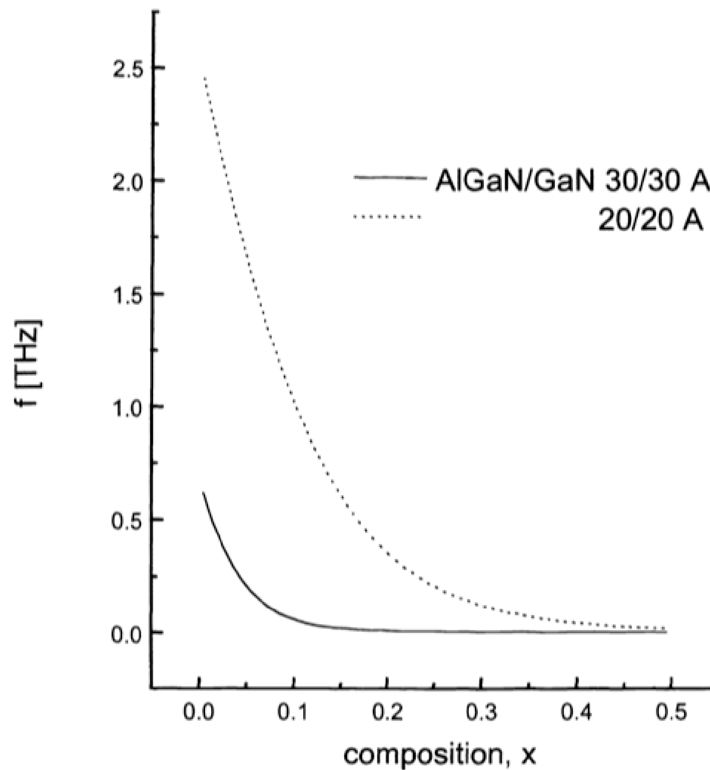


Figure 8-1: Calculated oscillation frequency in AlGaN/GaN SL diodes [8-6]

of 28%. Design C had the same thickness of AlGaN and GaN layer as design A with higher aluminum composition of 36%.The superlattice was embedded between GaN buffer layers with a Si-doping of 4×10^{18} cm^{-3} which served for obtaining good quality ohmic contacts. The layer structure used for the study is shown in Fig. 8.2. There were several challenges faced in the growth of the superlattice. Layer thickness control was the main difficulty due to GaN and AlGaN decomposition during growth, as well as, change of growth rate from run to run due to reactor coating. The AlGaN/GaN interface roughness control was an additional challenge since the superlattice design requires that it should not exceed 5 Å. High doping (~ 10^{19} cm^{-3}) GaN layers with smooth surface were not easy to obtain since the Si-doping degrades the surface quality. Growth of SL layers was optimized in terms of interface roughness and layer thickness control and optimum condition was used for the layers employed in this work.

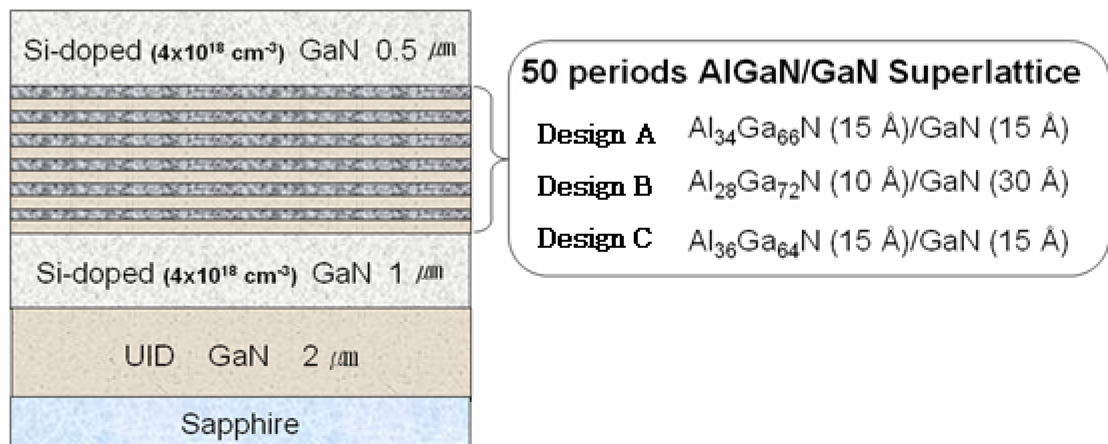
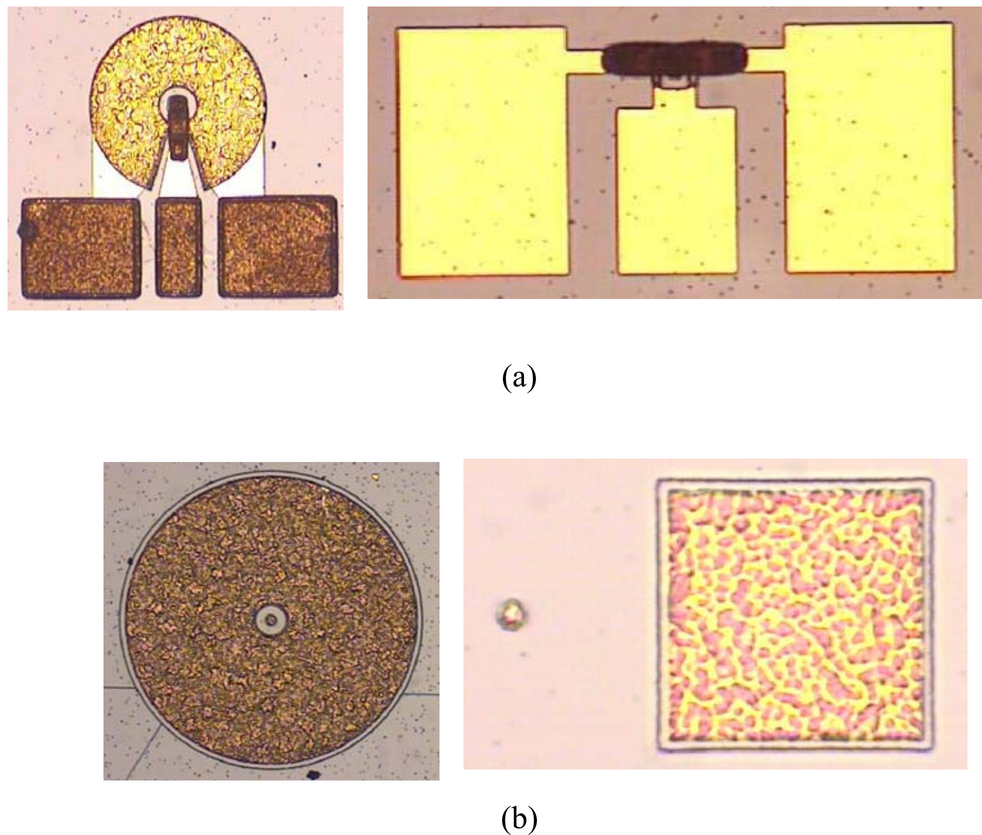


Figure 8-2: Layer structures for MOCVD grown superlattice structures

8.3 Superlattice Diode Design and Fabrication

An airbridge and a non airbridge design were employed in this work. The non-airbridge design involved relatively simple fabrication steps due to no need for airbridge fabrication. In case of diodes with small size MESA geometry, this design did not permit good contacts when using DC needles or microwave probes. The SL diode design with airbridges involved a more complicated fabrication process. Contacting for measurements was, however, much easier since it was achieved through contact pads. The airbridge connects, in this case, an inner MESA of small diameter (> 8 μm) to an outer contact which is in its turn connected to a microwave probe of ground-signal-ground



(a)

(b)

Figure 8-3: Microscopic images of the fabricated diodes; (a) with and (b) without airbridge

configuration; direct contact with microwave probes to the small MESA was not easy to have and proven to be non-reliable. The microscopic images of the fabricated diodes with and without airbridges are shown in Fig. 8.3. The mask set designed for this work contained diodes with inner MESA varying from 8 μm to 15 μm. The two ohmic contact designs were composed of a small and a large MESA as can be seen in the right picture of Fig. 8.3 (b). Small MESA designs were explored with both square and circular shape. The distance between the two MESAs was 100 μm in order to permit direct contact with a 100 μm pitch microwave probe. A non airbridge design of 'doughnut' type was also fabricated. It consisted of two ohmic contacts (an inner smaller contact surrounded by an outer larger contact) and is shown in the left picture of Fig. 8.3 (b).

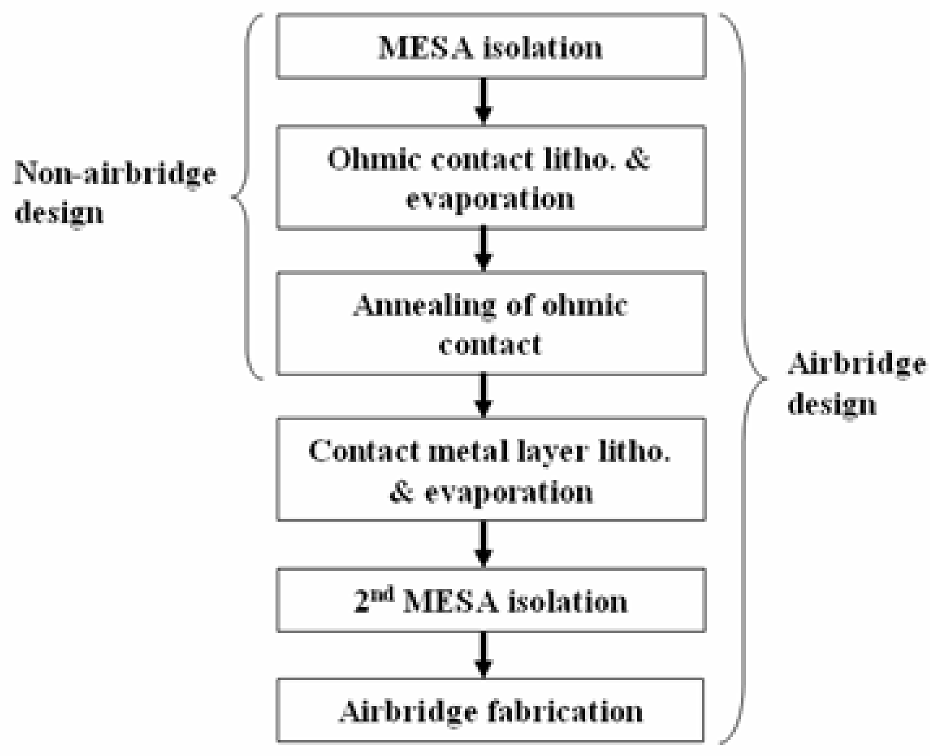


Figure 8-4: Fabrication steps for AlGaN/GaN superlattice diode with and without airbridge

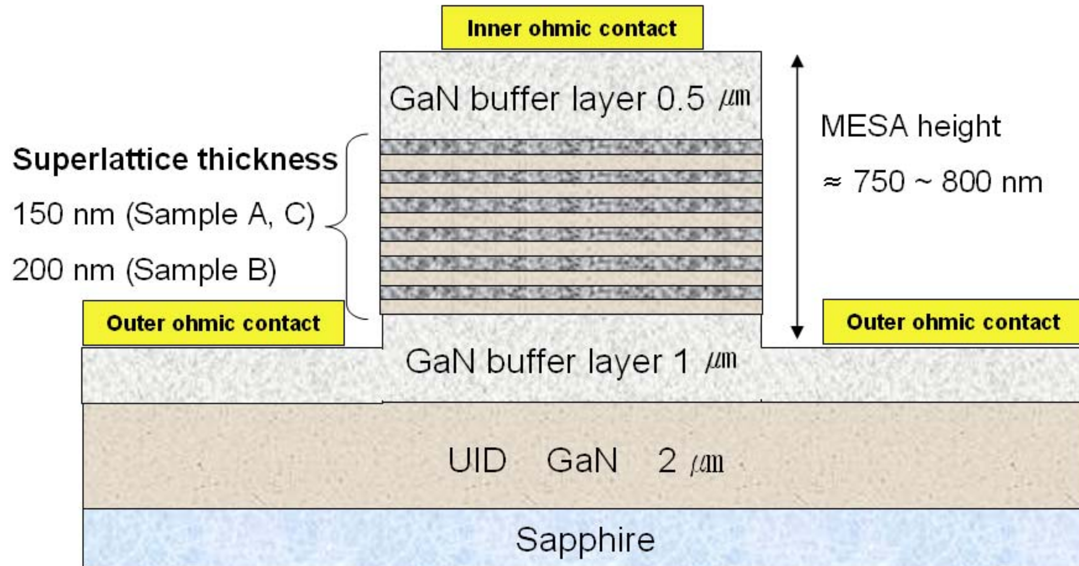


Figure 8-5: Schematic of the superlattice diode without airbridge ('doughnut' design)

Two designs were explored; one with an outer contact at the same hight as the inner contact and another with an outer contact on the bottom Si-doped GaN layer below the superlattice layers. The fabrication steps of superlattice diodes are similar to the fabrication steps of AlGaN/GaN HEMT and AlN/GaN MISFET technology. The key steps of the diode fabrication process are shown in Fig. 8.4. The diode schematic for non-airbridge 'doughnut' design is depicted in Fig. 8.5.

8.4 DC and Capacitance Characterization of the Superlattice Diode

The current-voltage characteristics of the superlattice diodes were measured using a high precision DC measurement instrument (Keithley 2602 source meter) at room temperature [8-8]. All three designs (A, B & C) of superlattice were characterized but the following results are referred only to design A, since it presented the most profound negative differential resistance effects. The voltage was swept from -5 V to 5 V with 50 mV voltage step in the continuous mode. The anode and cathode ohmic contacts were

contacted with a tip of 10 μm diameter DC probe. Fig. 8.6 shows the measurement results for the 30 μm diameter diode. Measurements IV#1 ~ #7 were done consecutively with an 1 min lapse of time. A negative differential resistance region was observed from 3 V to around 3.9 V and the negative differential resistance current decreased during consecutive measurements. The current-voltage measurement results suggest room temperature negative differential resistance presence with a peak-to-valley ratio of 1.3 and a relative broad voltage range, which could be of interest for practical implementations.

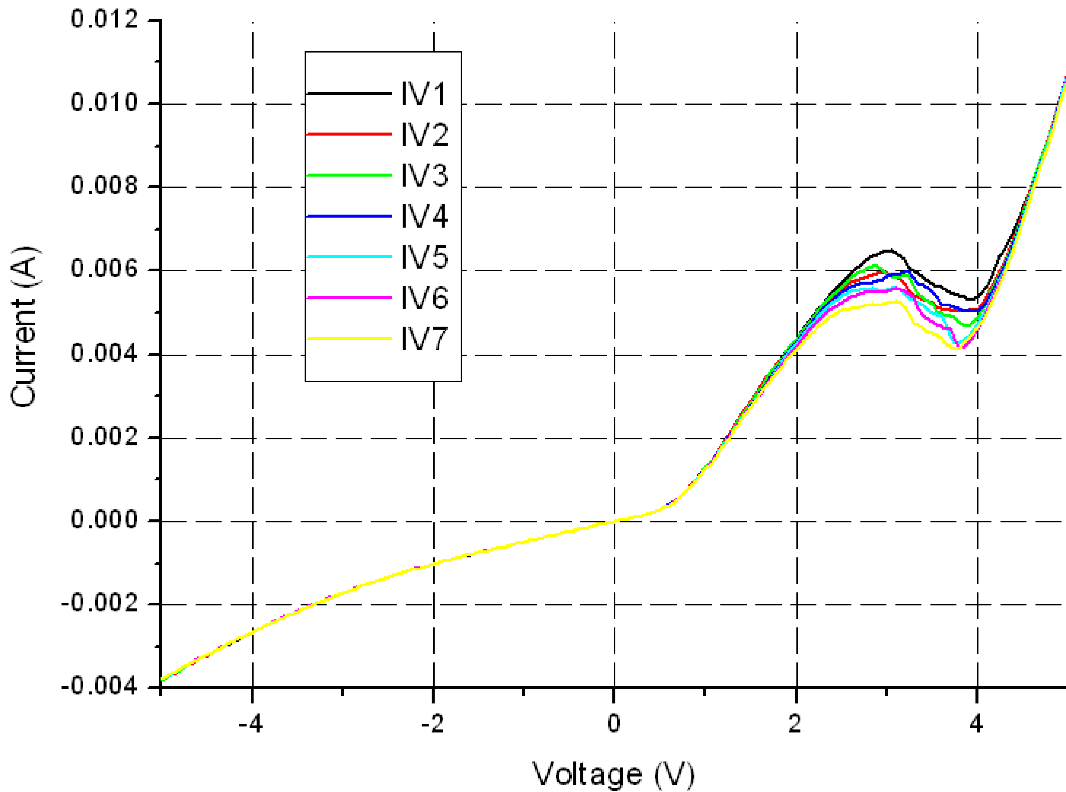


Figure 8-6: Current-Voltage characteristics of a 30μm diameter superlattice diode upon consecutive measurements

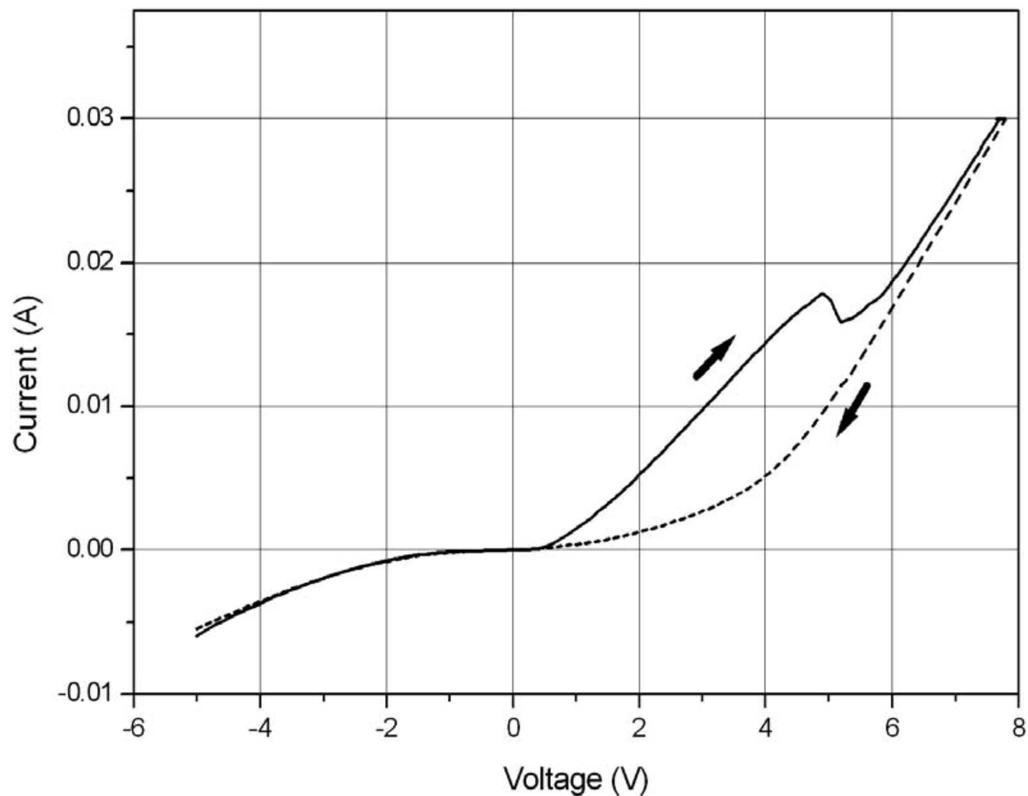


Figure 8-7: Current-Voltage characteristics of a 20㎛ diameter SL diode with up sweep (solid line) and down sweep (dashed line)

DC measurements were also done for 20 ㎛ diameter superlattice diodes with opposite sweep polarity as shown in Fig. 8.7. However, in this case, no negative differential resistance was observed. A similar complex behavior was also observed in GaN/AlN resonant tunneling diodes [8-9],[8-10]. The behavior of the peaks in the I-V characteristics depend on the previous charge state of the device produced by electrical bias. They suggested that the effects of polarization fields in wurtzite nitride structures and the presence of defects existing in the GaN well and the AlGaN/GaN interface induce the observed complex current behavior. It was shown by measuring the capacitance as a function of frequency, that the electron trapping and de-trapping effects by traps located

in the AlN/GaN interfaces are responsible for the observed behavior. A similar explanation may be applied to the AlGaN/GaN superlattice structures of this work which include traps at the interface.

In order to verify the presence of the above described trapping effect in defects, capacitance-voltage measurements were performed on the same device with an HP 4289A 1 MHz C-V meter [8-11]. As can be seen in Fig. 8.8, the SL diode displayed asymmetric C-V characteristics with negative capacitance features. The capacitance varied from about -22 pF at -5V to slightly 0 pF as the voltage increased to 0V and then decreased slowly to -5 pF when the device was biased with increased positive voltage. Negative capacitance effects have been shown in various semiconductor devices, such as

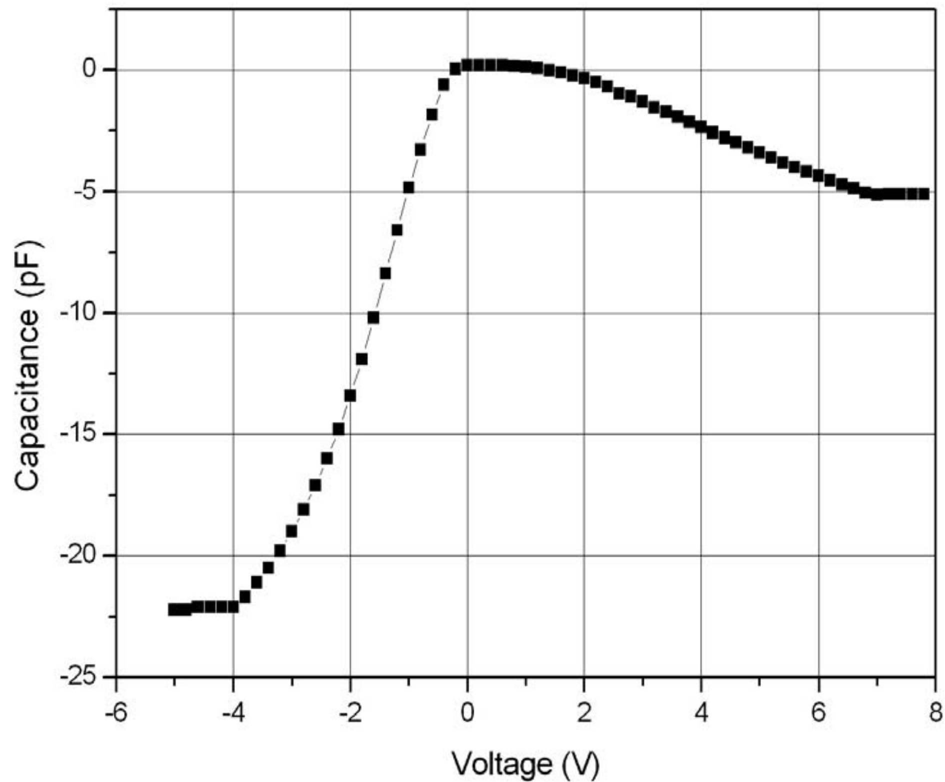


Figure 8-8: CV characteristics (at 1 MHz) at room temperature of a 20μm diameter superlattice diode

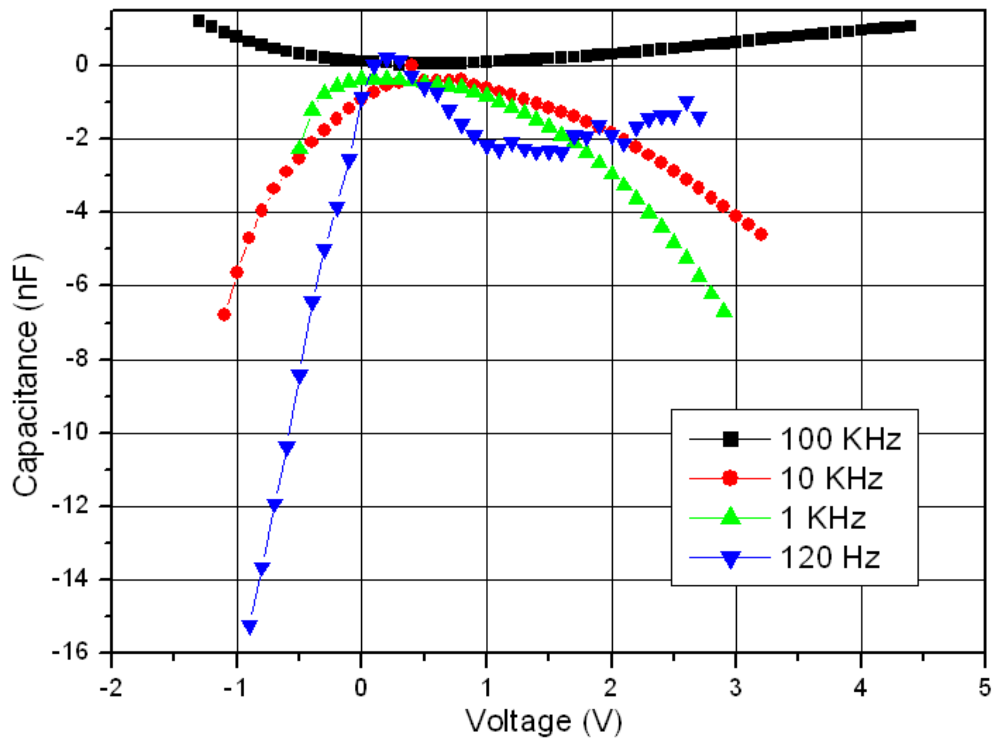


Figure 8-9: CV characteristics at room temperature of a 20μm diameter superlattice diode with variable frequency of measurement

p-n junctions, Schottky diode, and GaAs/AlGaAs quantum well infrared photodetectors [8-12]. In general, the negative capacitance effect is due to the non-radiative recombination of injected carriers into trap levels [8-13]-[8-15], or due to the capture-emission of injected carriers between multilevels [8-12].[8-16]

For further study of the observed negative capacitance effect, another 20 μm diameter SL diode was tested using the HP 4274A Frequency variable LCR Meter and the results are shown in Fig. 8.9. A frequency dependence was observed, which tends to disappear (flattening of the curves) when the frequency is increased. It appears that the observed effects are related to time dependent parameters that occur at low frequencies and as the frequency moves from Hz to kHz and MHz they tend to disappear since they

can no longer respond to the input signal. Temperature dependent tests may help in gaining additional information about the observed features since they could provide information on trap time constants and cross sections. Si_3N_4 passivation is required for future fabrication of SL diodes in order to cover the sidewall of the mesa exposed to plasma etching. Due to the damage from RIE etching, the sidewall might include surface traps and defects which may degrade device performance. Since the thickness of the mesa is over 800 nm, the thickness of PECVD deposited Si_3N_4 should be about the same as the mesa in order to adequately cover the sidewall. Another improvement in terms of processing can be the change of ohmic material from the currently used Ti/Al/Au to Ti/Al/Mo/Au metal stack that was reported to sustain high power and high temperature and manifest less migration effects under high power operation [8-17].

8.5 Summary

In this chapter, superlattice $Al_xGa_{1-x}N$/GaN diodes were designed, fabricated and measured. Theoretical investigation of the SL diode operation predicted terahertz generation of traveling dipole domains. SL layers were grown and optimized by MOCVD and diodes were processed. Room temperature DC measurements showed an NDC region around 1 V range with 1.3 peak to valley ratio. However, the NDC I-V characteristics were found to depend on the charge state of the device as determined by the bias voltage. C-V measurements were also performed and showed negative capacitance effects, which are possibly caused by carrier trapping and emission effects in the well and the heterostructure interface. Low temperature measurements are necessary for further studying the trapping and de-trapping effects.

CHAPTER 9

Complex Permittivity Measurements of Liquids and Cell Suspensions at Microwave Frequency

9.1 Introduction

The frequency dependent complex permittivity of biological samples such as cells or tissues can provide valuable information on bio-molecular properties including cell structure, orientation of molecular dipoles, surface conductance, and membrane processes [9-1]. These properties endow a unique “dielectric signature” to a given biological sample and can, for example, enable discrimination between living and dead cells, and between benign and cancerous tissues [9-2]-[9-5]. This ability to measure dielectric properties of biological media at microwave frequencies and to relate these measurements to physical properties of the biological system under test may enable powerful new methods for both *in vivo* and *in vitro* diagnostics.

Among the many available measurement techniques for measuring complex permittivity at microwave frequencies, the open-ended coaxial probe approach is most commonly used in biological applications due to its ease of use and non-destructive nature [9-6]-[9-8]. However, coaxial probes require expensive machining steps in order to obtain small aperture diameters. Furthermore, while coaxial probes are promising for *in vivo* dielectric spectroscopy, they inherently require large sample volumes for *in vitro* measurements due to their non-planar shape.

As an alternative, coplanar waveguide (CPW) sensors, where the substance under

test (SUT) is placed on top of the CPW and enclosed by the container, have been proposed for non-destructive permittivity measurements [9-9]. The advantages of this technique include the use of extremely small sample volumes (several μL) and the ability to average out any inhomogeneity in the sample.

The final goal of this work is to develop bio-semiconductor hybrid devices, which utilize both GaN-based semiconductor devices and CPW passive elements as bio-sensors. GaN-based material systems are very attractive for use as bio-semiconductor hybrid sensors due to their unique properties, such as chemical inertness, optical transparency and low signal to noise ratio [9-10]; the latter is due to the AlGaN/GaN heterostructure's low noise performance with high breakdown voltage characteristics [9-11] and could possibly enhance the measurement accuracy. Recent reports on chemical and/or biological sensors support the interest in AlGaN/GaN heterostructures [9-11]-[9-15]. The pH change of chemicals or bio-chemical processes are monitored in this case by measuring I_{DS} versus V_{DS}. I_{DS} is dependent on the change of 2DEG density which is modulated by changes of surface potential of the HEMT. The gate area of the HEMT is open (without gate-metallization) and the non-gated HEMT surface potential is changed by the charged particles and molecules absorbed onto the exposed gate area [9-16] as can be seen in Fig. 9.1.

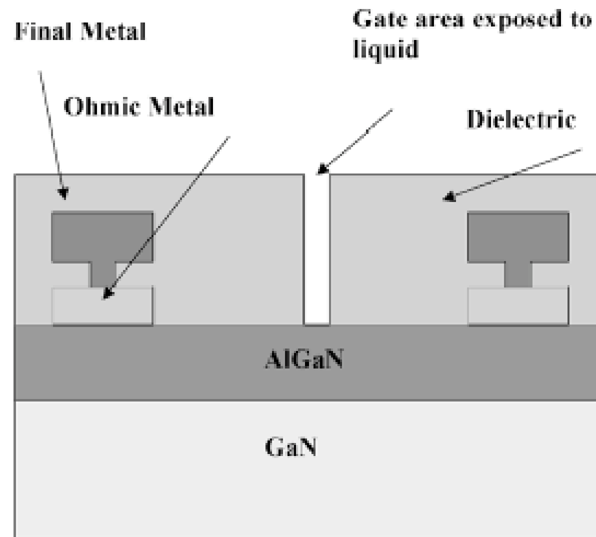


Figure 9-1: Schematic of gateless AlGaN/GaN HEMT for chemical or biological sensor [9-12]

The change of I_{DS} due to the chemical composition on the gateless surface is limited from few μA [9-12] to few mA [9-15] depending on chemicals on the surface and this can be considered as a drawback for this type of sensor. Furthermore, once the particles or molecules are absorbed onto the AlGaN surface, it may be difficult to remove them for the subsequent test cycle, due to the fact that the surface potential may be fixed to a value determined by them. AlGaN/GaN heterostructures have a strong surface potential due to the polarization charge as shown in Fig. 2.1. Therefore, charged particles can be stuck on the surface by charge attraction. The particle's potential and that of the surface get in this case in equilibrium and no further action is possible in terms of attracting other particles in the subsequent test.

As an alternative method, a hybrid approach based on an active and passive bio-sensor concept is proposed here. Both passive and active devices are in this case fabricated on the same substrate. The passive CPW-based sensor is used as a sensing

element and the active HEMT device is used for amplifying the sensed signal for better detection and/or for generating a high frequency signal as appropriate for the measurement under question as can be seen in Fig. 9.2. Generally, CPW is used as transmission line for interconnects or matching element in GaN-based MMICs as for example, shown in Chapter 7. Therefore the CPW sensor discussed in this chapter is very appropriate for being integrated together with GaN-based MMICs.

As can be seen in Fig. 9.3, the signal generator-based hybrid concept employs an oscillator circuit together with a CPW sensor used as a resonator in the same circuit; the CPW is not used in this case directly as a sensor but as a resonator for an oscillator circuit employing AlGaN/GaN HEMTs. In this case, the bio-chemical processes taking place on the CPW line will affect the CPW characteristics and this will in its turn change the resonating characteristics of the CPW. Finally this will modulate the oscillation frequency of the circuit, which can then be monitored easily.

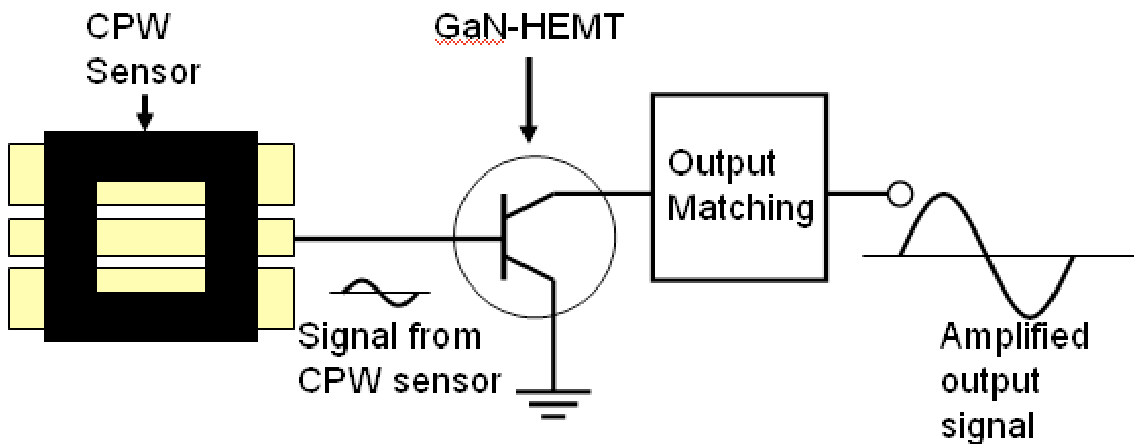


Figure 9-2: Schematic of a hybrid sensor approach based on an active and passive bio-sensor concept.

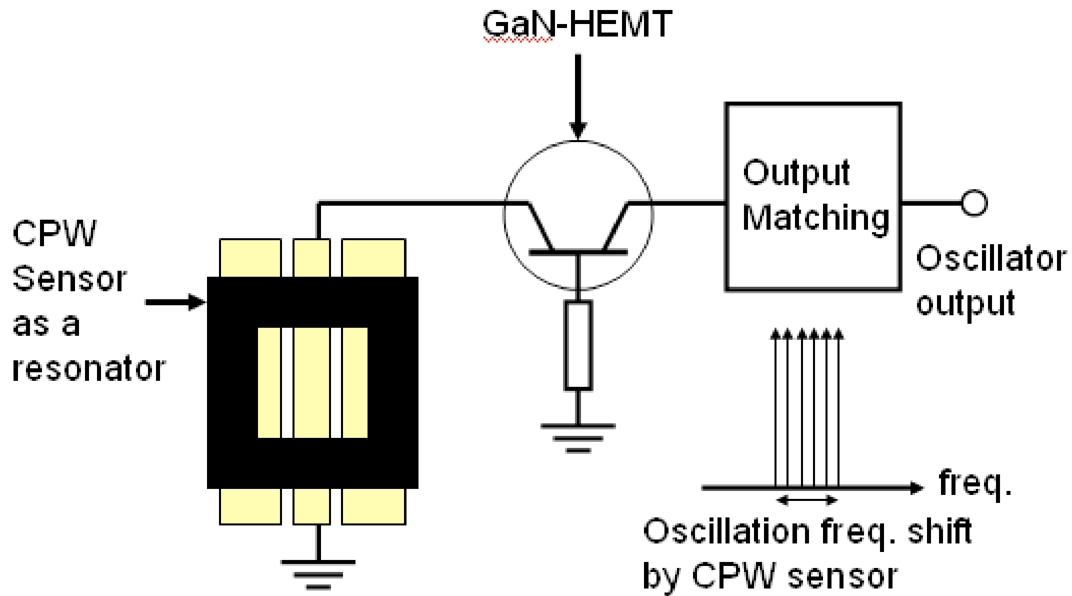


Figure 9-3: Schematic of the signal generator-based hybrid concept employing an oscillator circuit together with a CPW sensor used as a resonator

The work reported in this thesis investigates separately the CPW sensor and the AlGaN/GaN HEMTs, AlN/GaN MISFETs. Both types of components can, however, be easily combined with passive sensors for future active-passive hybrid bio-sensing applications. This work opens consequently a way for developing future GaN-based hybrid biosensors.

In this Chapter, the complex permittivity measurements of liquids, cell media and living cell suspensions with CPWs in an SU-8 container are described. The CPW sensor design and fabrication steps are presented in Section 9.2, together with a description of the measurement setup. A simple and rapid de-embedding method for extracting the relative permittivity of the liquid was developed based on the inverse method as described in [9-17] and is presented in Section 9.3. In Section 9.4, the substrates of CPW sensors (Corning Pyrex 7740 glass wafers and Schott Lithosil glass wafers) are evaluated

in terms of permittivity and loss measurements. Moreover, the SU-8 polymer used for fabrication of the liquid container was evaluated in the same frequency range.

The CPW sensor and the de-embedding method were verified by reference liquid measurements. Methanol, isopropanol and 0.9 % saline were used as the reference liquids since they have known Cole-Cole parameters, allowing verification of the permittivity values extracted from the measurements. Using the same method, commonly used cell culture media in the absence of cells were characterized in terms of complex permittivity from 1 GHz to the upper frequency of operation of the test device (~32 GHz). Finally we report the complex permittivity of a cell suspension as well as a study of the impact of a known cytotoxic chemical (dimethyl sulfoxide) on the cell suspension permittivity as a function of time.

9.2 Design and Fabrication of the CPW Sensor

A schematic and image of the fabricated CPW sensor are shown in Fig. 9.4 and Fig. 9.5 and the dimensions of the devices used in this study are shown in Table I. Using commercial software (Linecalc in ADS), the dimension of three different CPW line designs (W, S, W_g) were defined for a characteristic impedance of 50 ohms. Consideration was also made for the microwave probe contact dimensions with 150 μm pitch. Propagation was considered to take place in the quasi-TEM mode and low dispersion was assumed such that simplified equations could be used for the propagation constant and characteristic impedance as derived from the conformal mapping approach. This condition was satisfied under the assumption that the substrate height h is larger than $W + 2S$ [9-18].

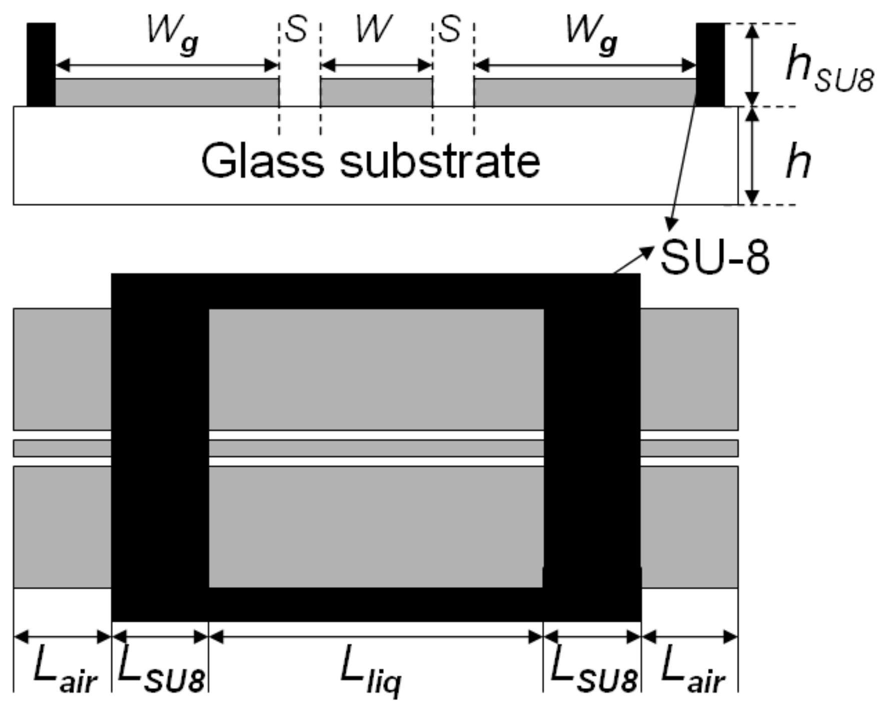


Figure 9-4: Schematic of the CPW sensor with SU-8 container

Figure 9-5: photograph and microscopic image of the fabricated CPW sensor chip

Param.	Value			Specification
	Type I	Type II	Type III	
W	96 μm	136 μm	178 μm	Center conductor width
S	14 μm	19 μm	24 μm	Gap
W_g	486 μm	672 μm	672 μm	Ground conductor width
h	700 μm			Substrate thickness
h_{SU8}	300 μm			SU8 thickness
L_{air}	200 μm			Air exposed CPW length
L_{SU8}	300 μm			SU-8 covered CPW length
L_{liq}	2, 3, 5, 7, 9 mm			Liquid exposed CPW length

Table 9-1: Dimensions of CPW sensors

The length of the SU-8 exposed CPW area (L_{SU8}) and that of the air exposed CPW area (L_{air}) were chosen in order to prevent lifting off of the SU-8 container by the interface strain appearing between the container and the CPW metal. Additionally, the distances between each CPW sensor were kept at more than 1 mm in order to avoid contacting the 300 μm high SU-8 container of adjacent CPW sensors by the microwave probe. There were two choices of the glass wafers; Pyrex 7740 and fused silica Lithosil™ glass wafers (Schott AG, Germany, 700 μm thickness). Lithosil wafers were chosen for the substrate because of their low relative permittivity and loss tangent (ε_r ~ 3.8 vs. 4.6 and tan δ ~ 0.0014 vs. 0.004 at 1 MHz for Lithosil and Pyrex respectively). The lower permittivity and loss tangent of the substrate provide higher sensitivity in measuring the liquid permittivity.

The CPW was fabricated using photolithography and electroplating. A Cr/Au seed layer was evaporated and patterned by photolithography followed by Au electroplating. The total thickness of the CPW line was 3 μm. SU-8 polymer was used for fabricating the container. The choice for this polymer was made based on its mechanical and biocompatible properties, as well as its ability to form high aspect ratio (> 20:1) structures [9-20]. In order to achieve a high aspect ratio structure with good adhesion to the metal line and glass wafer, the SU-8 process was optimized as follows. First, SU-8 2100 was spun on the fabricated CPW lines at 1000 rpm and maintained unprocessed for several hours for planarization. The devices were then softbaked on a hotplate with a temperature ramping from 65°C up to 95°C at 2°C/min. The samples were maintained at 95°C for 3 hours, cooled to room temperature, and then left overnight in order to limit material stress. Using an MJB-3 mask aligner, the SU-8 container layer was exposed for 110 sec at a power density of 12.5 mW/cm^2. A post exposure bake was performed by ramping the hotplate at 2°C/min from 55°C to 95°C, where the samples were maintained for 1 h. After cooling to room temperature and sitting for 3 additional hours, the SU-8 could be developed by immersing in MR-Dev 600 developer for 10 min. Cleaning with IPA completed the process.

Two-port S-parameter measurements were performed on the fabricated test structure using microwave probes and an Anritsu 37397C vector network analyzer (VNA). Ground-signal-ground microwave probes with 150 μm pitch were used to contact the CPW sensors. Short-open-load-through (SOLT) standards on a GGB CS-5 calibration substrate were used for calibration. The multiline thru-reflect-line (TRL) calibration [8-16] offers higher accuracy and the possibility of de-embedding discontinuities in the

CPW line at the calibration step [9-22]. However, on-wafer TRL calibration requires a set of long lines for wideband measurements, which takes up a large area on the wafer. Additionally, for different types of CPW sensors, as listed in table I, separate calibrations are necessary for de-embedding different size of SU-8 containers. At the frequency range of interest, SOLT calibration provides reasonable accuracy without requiring large test structures on the wafer [9-23]. The temperature of the CPW sensors was maintained at 25°C by a temperature controlled probe chuck and ambient temperature was kept at 23°C during measurement. After microwave probe contact was established, the SU-8 container was filled with the liquid using a micro-pipette. The liquid volume was on the order of a few micro-liters.

9.3 Theory of Deembedding and Permittivity Extraction

The reference plane used for S-parameter measurements was set to be the contact point of the microwave probes. This required de-embedding in order to account for the SU-8 covered CPW region and the air exposed CPW between the SU-8 wall and the contact reference plane. This was done using simple ABCD matrix inversion [9-17]. Based on network analysis theory [9-24], the ABCD matrix of the complete structure (T_{tot}) can be written as

$$T_{tot} = T_{air} \times T_{SU8} \times T_{liq} \times T_{SU8} \times T_{air} \tag{9.1}$$

where T_{air}, T_{SU8} and T_{liq} are ABCD matrices for regions consisting of air exposed CPW, SU-8 covered CPW and the liquid regions, respectively as depicted in Fig. 9.4.

Two-port transitions between T_{air} and T_{SU8} and T_{SU8} and T_{liq} were ignored. The de-embedding method was verified with 3D full-wave simulation and ignoring transitions is okay. Using (9.1), de-embedding can be performed as follows.

$$T_{liq} = T_{SU8}^{-1} \times T_{air}^{-1} \times T_{tot} \times T_{air}^{-1} \times T_{SU8}^{-1}. \tag{9.2}$$

Direct conversion of measured S-parameters to ABCD matrices can be obtained based on well known relations [9-24]. To construct the T_{air} and T_{SU8} matrices, the following equation can be utilized based on a quasi-TEM mode assumption.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma \cdot L) & Z_c \sinh(\gamma \cdot L) \\ \frac{1}{Z_c}\sinh(\gamma \cdot L) & \cosh(\gamma \cdot L) \end{bmatrix} \tag{9.3}$$

If the characteristic impedance Z_c, propagation constant γ and length of the CPW region L are given, the ABCD matrices of the SU-8 and air sections can be calculated. For this purpose, all CPW lines were measured before SU-8 container fabrication and tests were complemented by fabrication and measurement of an SU-8 covered CPW line on the same wafer.

9.3.1 T_{air} calculation

Before SU-8 processing, each line was characterized with the VNA. The measured S-parameters were then converted into an ABCD matrix. The eigenvalues of the ABCD matrix are related to the propagation constant as follows [9-25].

$$\gamma = \frac{1}{L} \cdot \ln\left[\frac{(A+D) \pm \sqrt{(A+D)^2 - 4}}{2}\right] \tag{9.4}$$

The characteristic impedance and effective permittivity can be calculated as given in [9-26].

$$Z_c = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \cdot \frac{K(k)}{K(k')} \tag{9.5}$$

$$\varepsilon_{eff} = \left(\frac{c_0 \cdot \gamma}{2\pi f}\right)^2 \tag{9.6}$$

where $k = \frac{c}{b}\sqrt{\frac{b^2 - a^2}{c^2 - a^2}}$, $k' = \sqrt{1 - k^2}$, $a = W/2$, $b = a + S$, $c = b + W_g$,

and c_0 is the speed of light in vacuum, f is the frequency and *K( )* is complete elliptical integral of the first kind. The exact length of the air exposed CPW (L_{air}) was determined by optical microscopy. Using the parameters calculated with (9.4)-(9.6), the ABCD matrix for the air exposed CPW line can be determined.

9.3.2 T_{SU8} calculation

In order to generate the transmission matrix for an SU-8 loaded CPW line, an SU-8 calibration CPW line was fabricated on the same substrate and the S-parameters were

measured. Using network analysis theory, the ABCD matrix of the fully loaded SU-8 region can be written as

$$T_{SU8} = T_{air2}^{-1} \times T_{tot2} \times T_{air2}^{-1} \quad (9.7)$$

where T_{tot2} and T_{air2} are ABCD matrices for the complete SU-8 CPW test line and the air exposed CPW used for contact, respectively. Using the T_{tot2} values calculated from the measured S-parameters of the SU-8 calibration line and equations (9.4)-(9.6), γ and Z_c of the SU-8 loaded line were obtained in the same manner as T_{air}. The length of the SU-8 loaded section in the CPW sensor (L_{SU8}) was measured and T_{SU8} was then obtained.

9.3.3 Complex permittivity calculation

The above approach allowed obtaining T_{liq} values after calculating (9.2). The propagation constant γ of the liquid loaded line only then could be obtained using T_{liq} and (9.4). The attenuation constant α contains information on dielectric, conductor and radiation losses. In order to properly extract properties of the liquid while accounting for other loss mechanisms, the dielectric attenuation constant must first be determined by

$$\alpha_d = \alpha - \alpha_c - \alpha_r \quad (9.8)$$

where α_d, α, α_c and α_r are attenuation constants for dielectric, calculated, conductor and radiation loss respectively. α_c and α_r can be determined using equations available in the literature [9-17]. The propagation constant of the liquid loaded line considering only

dielectric loss is as follows

$$\gamma' = \alpha_d + j \cdot \beta \tag{9.9}$$

ε_{eff} of the liquid loaded CPW can be obtained with (9.6) using γ'. Finally the complex permittivity of the liquid can be calculated using the following relations of the conformal mapping approach [9-26].

$$\varepsilon_{eff} = 1 + \frac{1}{2}(\varepsilon_{r1} - 1) \cdot q_1 + \frac{1}{2}(\varepsilon_{r2} - 1) \cdot q_2 \tag{9.10}$$

$$q_i = \frac{K(k) \cdot K(k_i')}{K(k') \cdot K(k_i)} \tag{9.11}$$

where

$$k_i = \frac{\sinh(\pi c / 2h_i)}{\sinh(\pi b / 2h_i)} \sqrt{\frac{\sinh^2(\pi b / 2h_i) - \sinh^2(\pi a / 2h_i)}{\sinh^2(\pi c / 2h_i) - \sinh^2(\pi a / 2h_i)}}$$

and i = 1 is the glass substrate and i = 2 represents the liquid. hi is thickness of the liquid and substrate. From (9.9), the complex permittivity of the liquid ε_{liq} can be calculated as follows

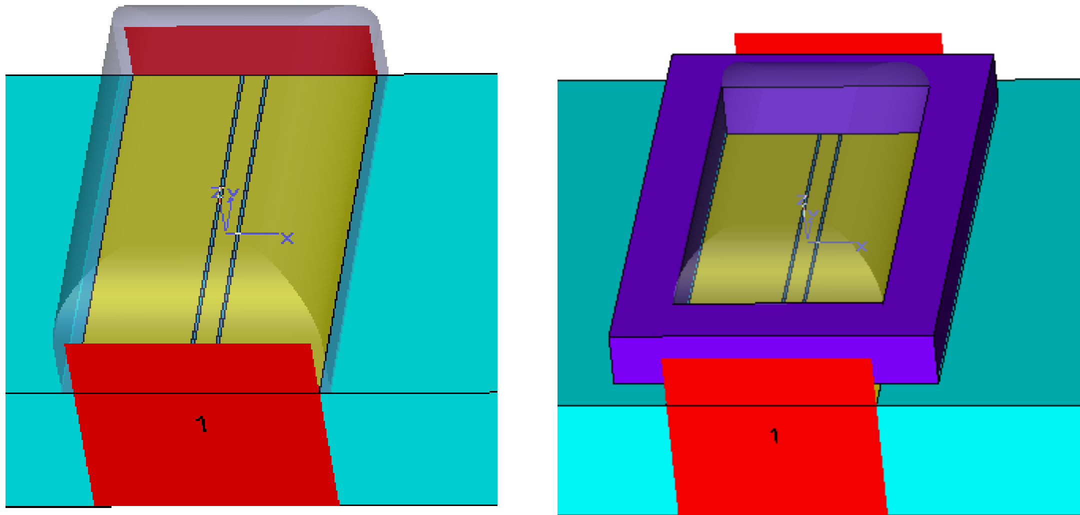
$$\varepsilon_{liq} (= \varepsilon_{r2}) = 1 + \frac{2}{q_2}(\varepsilon_{eff} - 1) - \frac{q_1}{q_2}(\varepsilon_{r1} - 1) \tag{9.12}$$

9.3.4 De-embedding method verification

In order to validate the de-embedding method, 3D full-wave simulation was performed on the CPW sensor using the CST Microwave Studio. CPW lines with and without SU-8 containers on the Lithosil wafer were simulated as can be seen in Fig. 9.6. All the physical dimensions of the CPW sensors were the same as in Table 9.1 and permittivity of the Lithosil wafer and test liquid were referenced from theoretical values.

Isopropanol was filled into the SU-8 container for simulation. The CPW line without a container was totally covered with isopropanol up to the end of the two ports and therefore there were no discontinuities to be de-embedded in the test structure. Complex permittivity of isopropanol was extracted from de-embedded S-parameters of the CPW sensor. Then it was compared with extracted permittivity of isopropanol on the CPW line without the SU-8 container and the results are shown in Fig. 9.7. The two results are in good agreement and therefore the de-embedding method is valid over the simulated frequency range.

Full wave 3-D simulation was performed on the effect of side wall. CPW sensors with different side wall distances were simulated for the case of an isopropanol filled SU-8 container. Three different side wall distances were simulated and the schematic and simulation results are shown in the next figures.



(a) (b)

Figure 9-6: 3-D simulation schematics; (a) CPW line without SU-8 container covered with isopropanol and (b) normal CPW sensor with SU-8 container filled with isopropanol

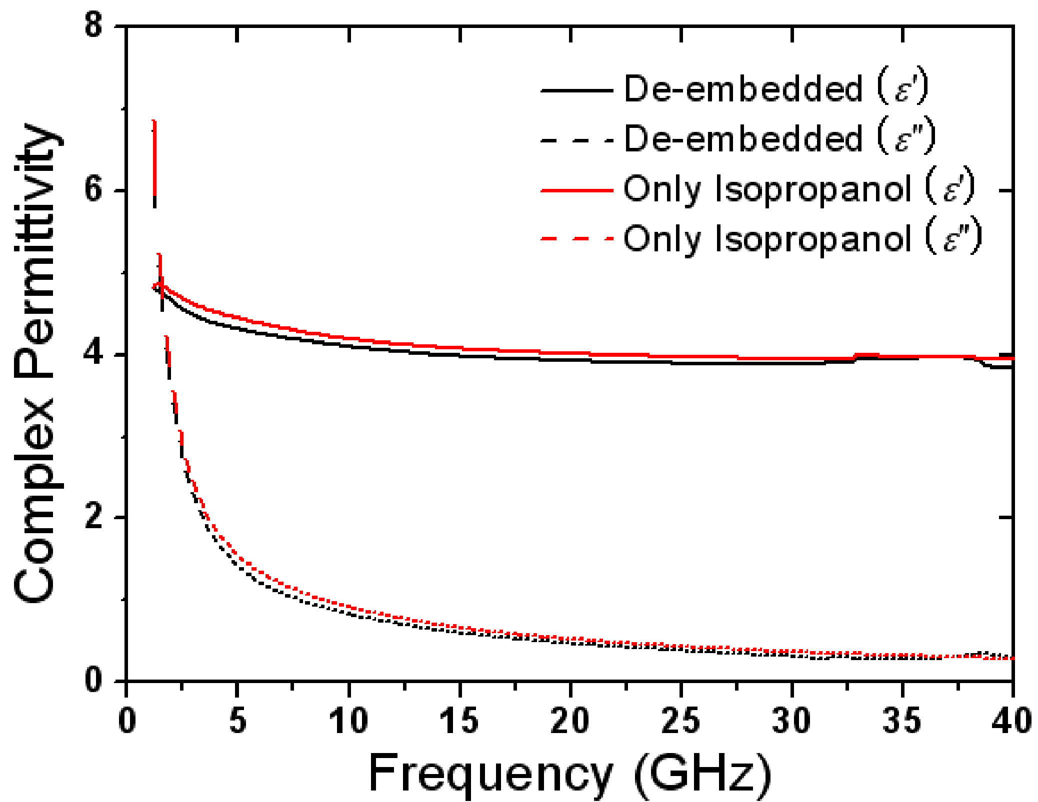


Figure 9-7: Simulated complex permittivity of isopropanol in the CPW sensor; (de-embedded) with SU-8 container and (only isopropanol) without SU-8 container.

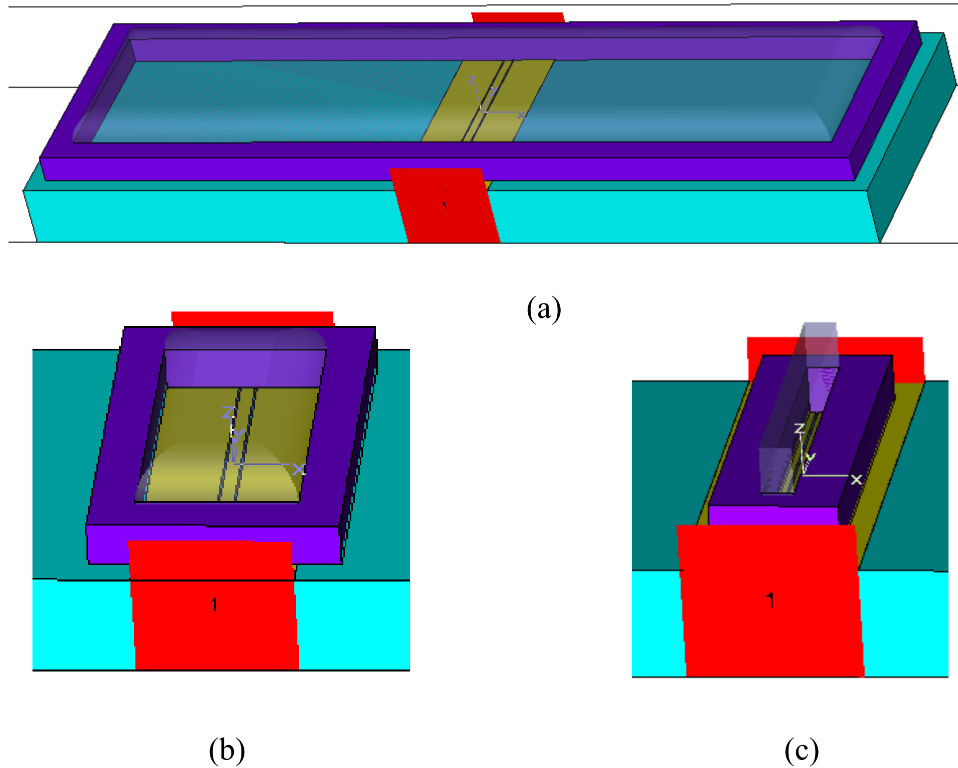


Figure 9-8: 3-D simulation schematics; (a) IPA in CPW container with side wall distance of 9 mm (b) normal CPW sensor with side wall distance of 1.1 mm (c) 0.2 mm.

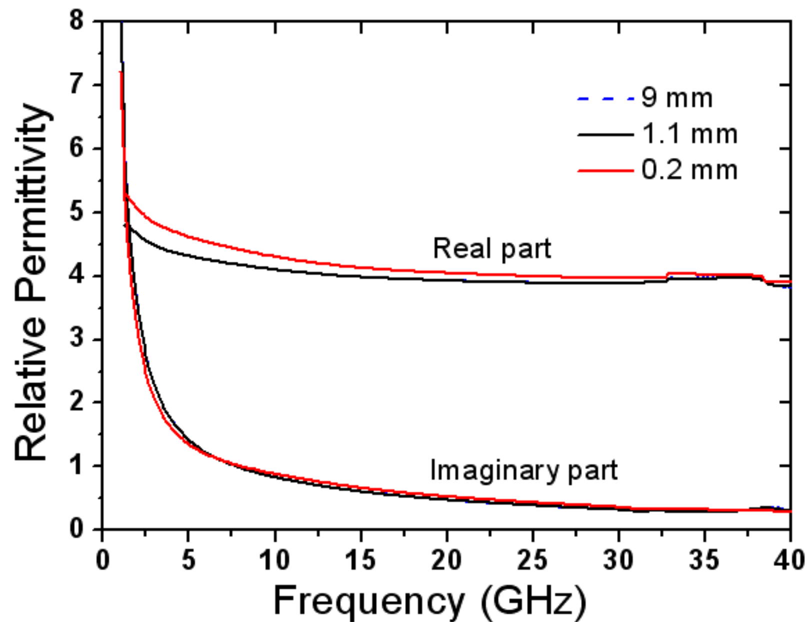


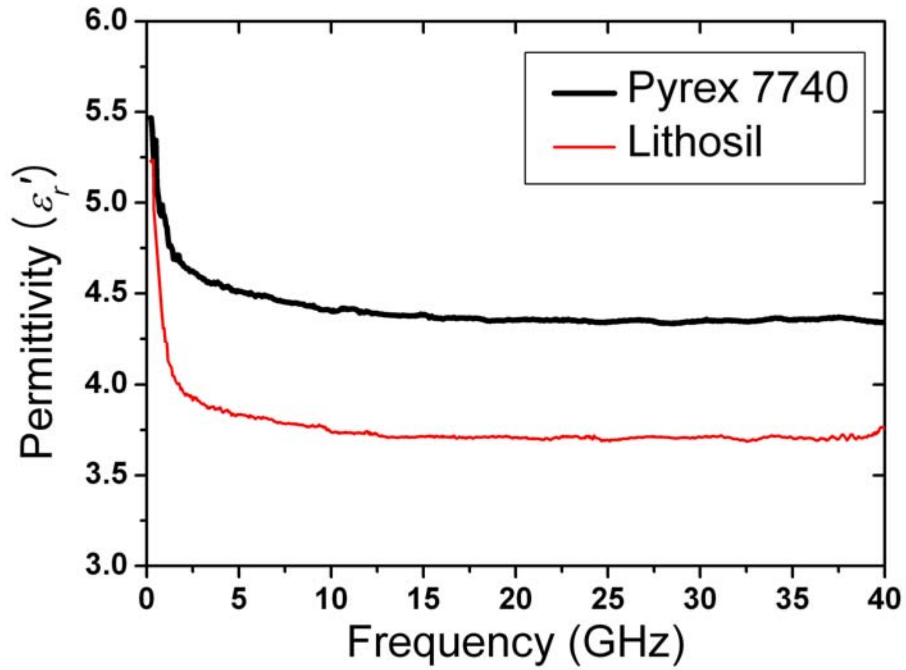
Figure 9-9: Complex permittivity of IPA on structure with side wall distances of 9 mm, 1.1 mm and 0.2 mm. (9 mm and 1.1 mm results are almost identical. Therefore the difference is not appear in the graph)

As can be seen in the IPA permittivity, there is almost no difference between 9 mm and 1.1 mm results. This means the side wall effect were negligible for our structure. The side wall effect appears in case of 0.2 mm, which is an extreme case.

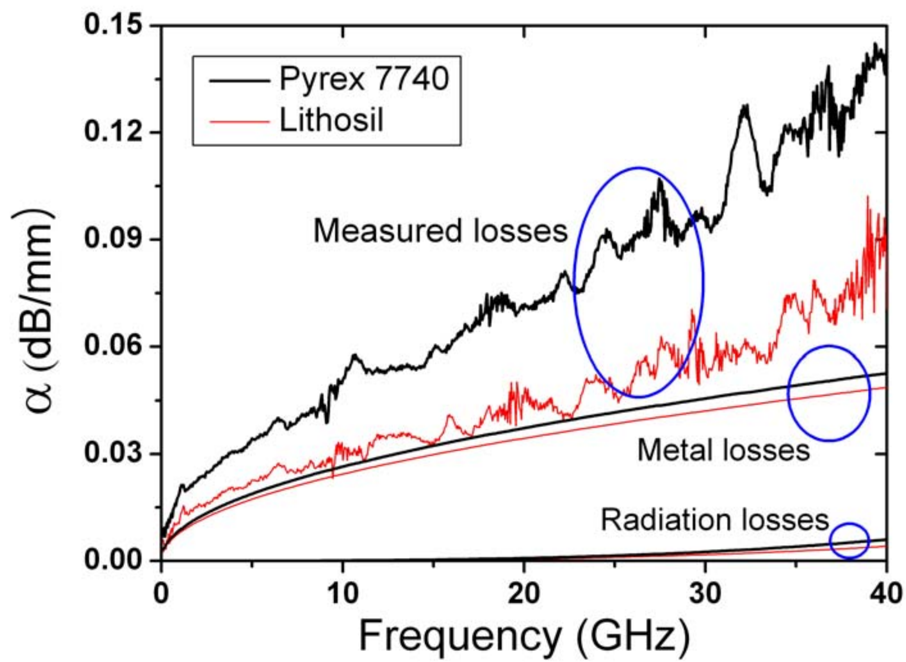
9.4 Measurement Results

9.4.1 Glass substrate and SU-8 container evaluation

To reduce errors in the de-embedding process explained in Section 9.3, it is necessary to evaluate separately the glass substrates and SU-8 container characteristics. Using the S-parameter measurement results of CPW lines before commencing the SU-8 process, one can calculate the permittivity and dielectric attenuation constants using equations (9.4) and (9.12). No de-embedding is necessary in this case and the results are shown in Fig. 9.10. The permittivity of Pyrex 7740 and Lithosil glass substrates were measured to be 4.35 and 3.7 respectively at 30 GHz.



(a)



(b)

Figure 9-10: (a) Measured relative permittivity (ε_r') and (b) measured total loss and simulated metal and radiation losses of Pyrex 7740 and Lithosil glass substrates for 9 mm line with type III

The measured total attenuation is depicted together with the attenuation constants for the metal loss and radiation loss in Fig. 9.10 (b). Based on equation (9.8), the dielectric loss equals the difference between total losses and metal loss (radiation loss is negligible at the frequency range of interest). Overall, Lithosil substrates showed better electrical characteristics with lower permittivity and dielectric loss. Loss of the CPW lines can be drawn in terms of loss tangent. The loss tangent is defined as

$$\tan\delta = \frac{\varepsilon_r''}{\varepsilon_r'} = \frac{imag(1+\frac{2}{q}(\varepsilon_{eff}-1))}{real(1+\frac{2}{q}(\varepsilon_{eff}-1))} \tag{9.13}$$

and $\varepsilon_{eff} = \left(\frac{c_0 \cdot \gamma}{2\pi f}\right)^2$, $\gamma = \alpha + j\beta$

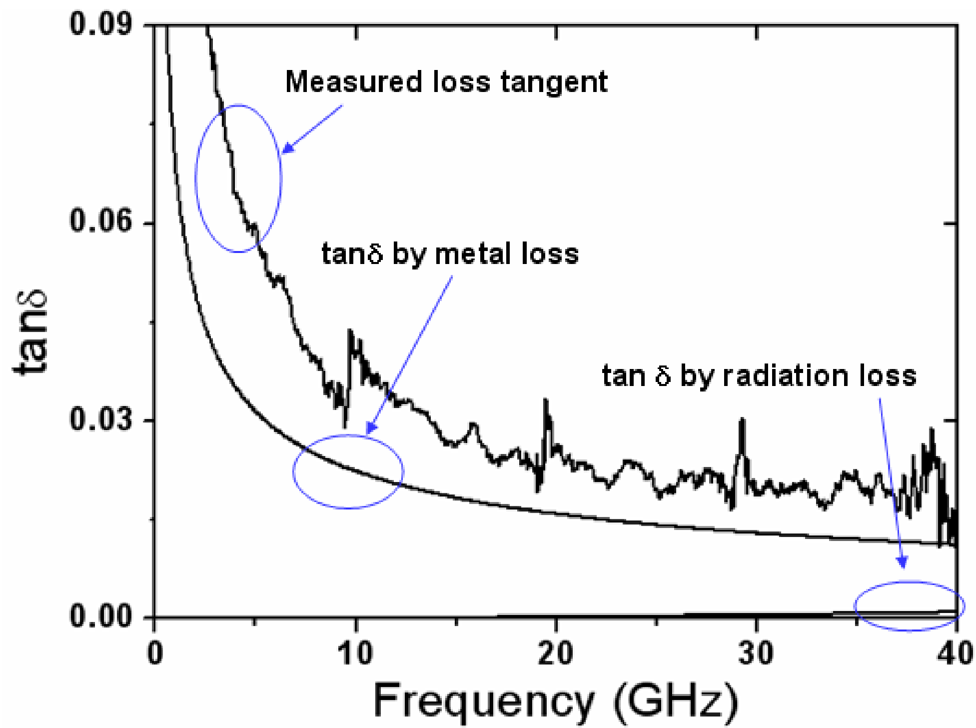


Figure 9-11: Loss tangents of Lithosil wafer calculated by (9.13)

Therefore we can calculate the loss tangent from measured α and β. Fig. 9.11 presents the loss tangents for Lithosil wafer. The method can resolve the low loss tangent. However alpha (Fig. 9.10 (b)) is preferred instead of loss tangent, since alpha directly shows loss characteristics of the wafers and does not include phase error from β, which also appeared in the loss tangent graph at low frequencies.

The abrupt change in permittivity observed at low frequencies may come from the effect of systematic phase error. The phase error is due to the inability of the relatively short CPW lines to accurately detect the phase below 2 GHz [9-20]. Measurement uncertainty increases dramatically as the frequency nears 0 GHz. Stuchly *et al* [9-27] proposed an empirical expression for the normalized transmission line length L/λ which gives minimum experimental uncertainty.

$$\frac{L}{\lambda} = \frac{1}{4}\left|\varepsilon(j\omega)\right|^{-0.5} \tag{9.14}$$

where L, λ, and $\varepsilon(j\omega)$ are the optimum line length, the wavelength and the imaginary part of effective permittivity, respectively. L was calculated for a 3 mm CPW line on a Lithosil wafer and it is shown in Fig. 9.12. At the frequency range below 2 GHz, L is more than 6 mm and increases drastically as frequency decreases. Therefore at low frequencies, experimental uncertainty is greatly increased and results in the error at low frequencies.

Another reason for the observed permittivity increase at low frequencies is the assumption of negligible conductor loss in CPW used for deriving equations (5) and (6). As pointed out by [9-28], the assumption of negligible conductor loss is not valid at low

frequencies, where conductor losses need to be considered. Although this assumption introduced errors in the permittivity extracted at low frequencies, it was used in the work presented in this thesis, since it allowed consideration of finite dielectric (shunt) losses. Losses of this type are often neglected in theories where conductor losses are taken into account since their main objective is to predict “open-air” transmission line characteristics. This is not, however, the case in this thesis, where high-dielectric loss liquids such as cell suspensions are addressed. The extraction of permittivity in such media makes the consideration of dielectric losses of prime importance. The results presented in this work provide the possibility of reliable analysis of the electrical properties of liquids but should be treated with caution at low frequencies.

The SU-8 polymer was also evaluated based on permittivity calculations as shown in Fig. 9.9. The real and imaginary parts of the permittivity were measured to be 3.2 and 0.1 respectively at 30 GHz, which agree with published results [9-20].

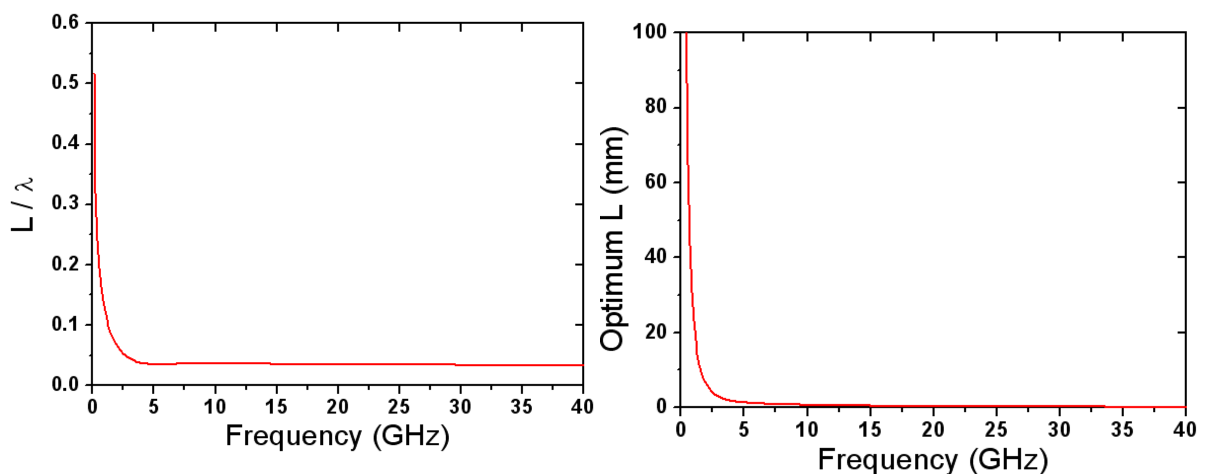


Figure 9-12 (left) Normalized line length (L/λ) for the CPW line on Lithosil wafer & (right) optimum line length L for permittivity extraction.

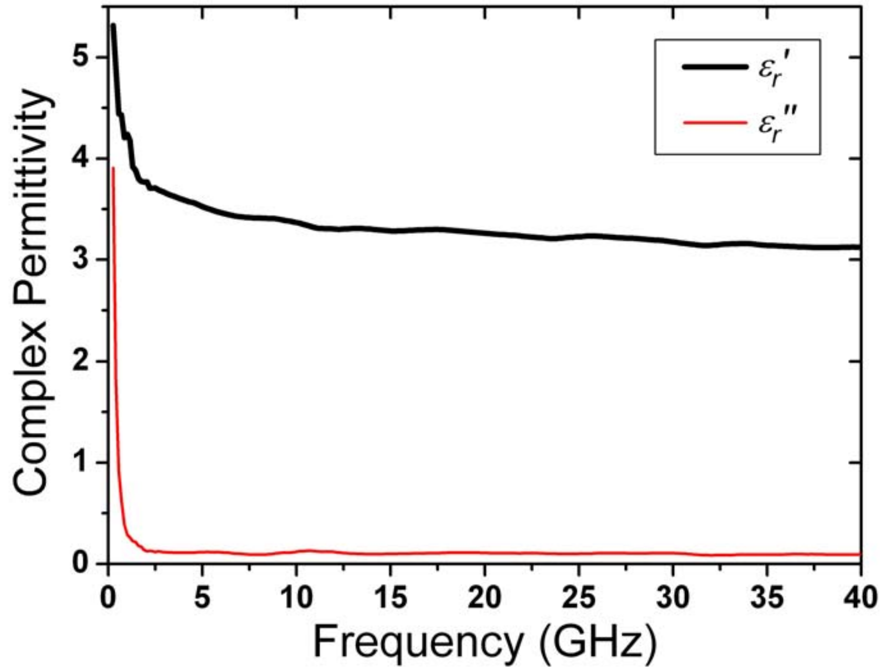


Figure 9-13: Measured complex permittivity of SU-8 polymer

9.4.2 Reference liquid measurements

In order to verify the de-embedding method and evaluate the CPW test structure, the permittivity of reference liquids was measured. Cole-Cole equation and parameters were used to evaluate measured permittivity, which are given in [9-29]-[9-31]. The Cole-Cole equation is as follows.

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + (j\omega\tau)^{1-\alpha}} - j\frac{\sigma}{\omega\varepsilon_0} \tag{9.15}$$

Cole-Cole parameters for the measured reference liquids are listed in Table II. In order to compensate for measurement errors, measurements were repeated on different

line types and lengths and then all data were averaged. Fig. 9.14 and Fig. 9.15 show the measured complex permittivity of methanol and isopropanol respectively. The expected values obtained using the Cole-Cole equation were shown together. The measurement data agree well with the Cole-Cole equation in the frequency range of 1 to 40 GHz.

Reference liquids	Cole-Cole Parameter				
	ε_s	ε_∞	τ (ps)	α	σ
0.9% Saline	75.3	4.5	8.1	0.02	1.55
Methanol	33.7	4.5	49.64	0.043	0
2-Propanol	20.8	3.8	254	n/a	0

Table 9-2: Cole-Cole parameters of the reference liquids at 25 °C

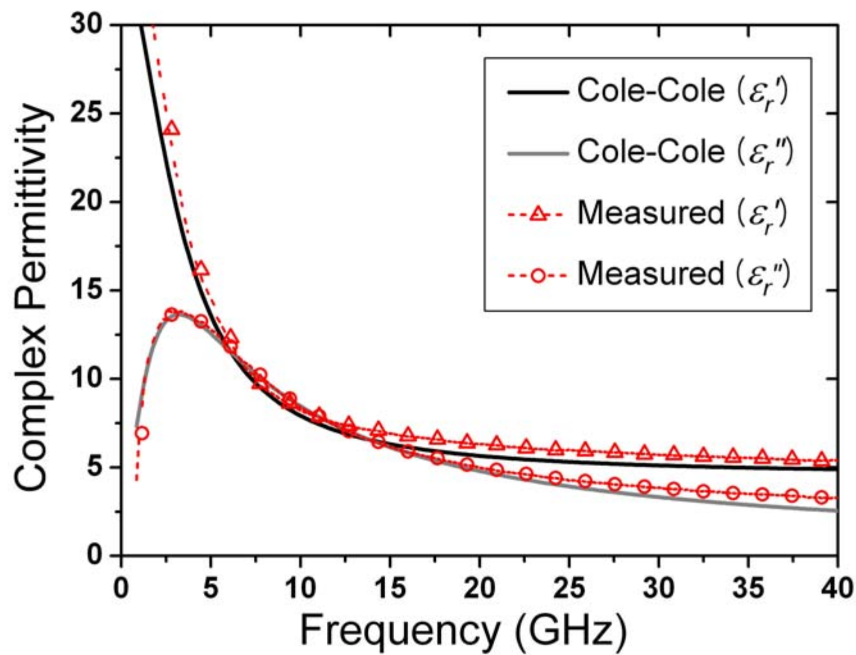


Figure 9-14: Measured complex permittivity of methanol with theoretical values

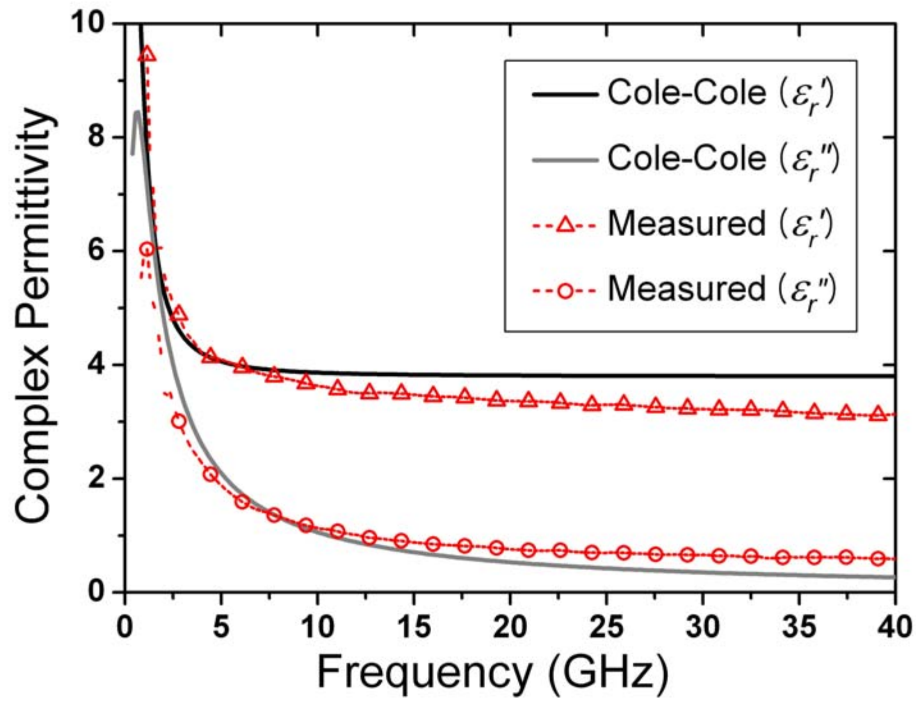


Figure 9-15: Measured complex permittivity of isopropanol with theoretical values

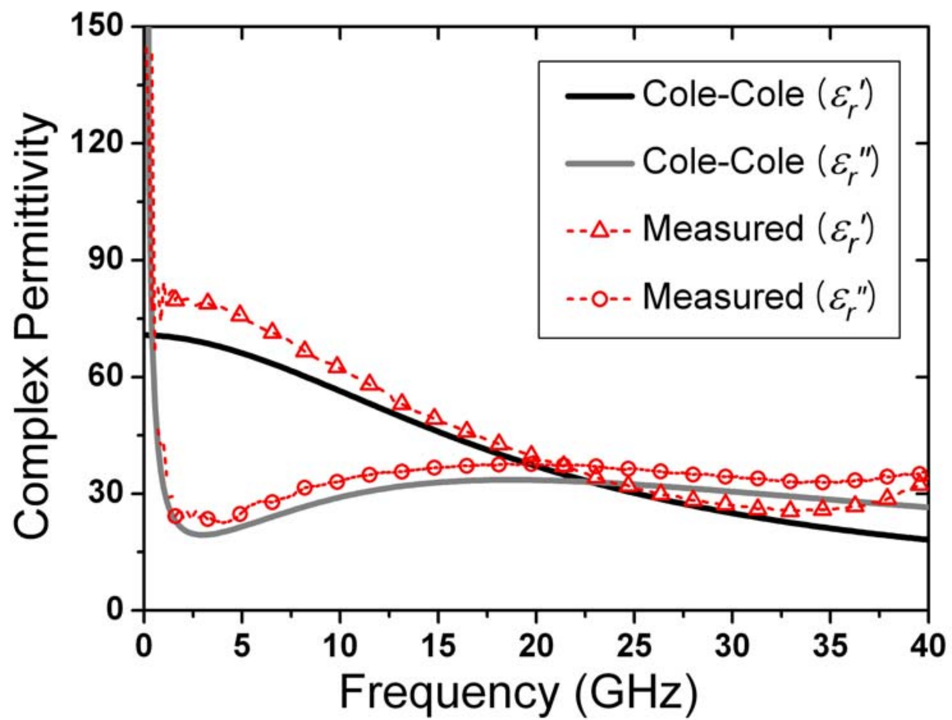
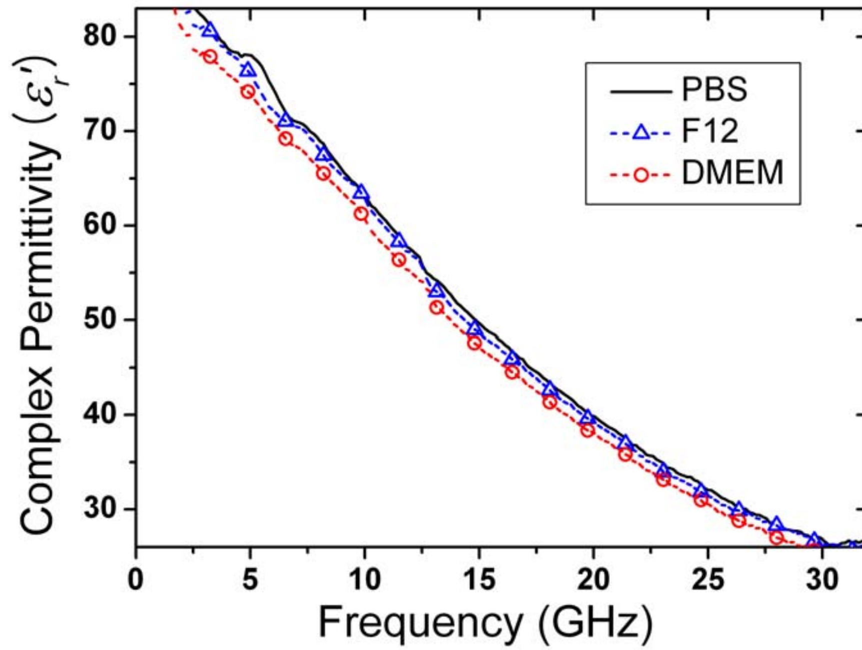


Figure 9-16: Measured complex permittivity of 0.9% saline with theoretical values

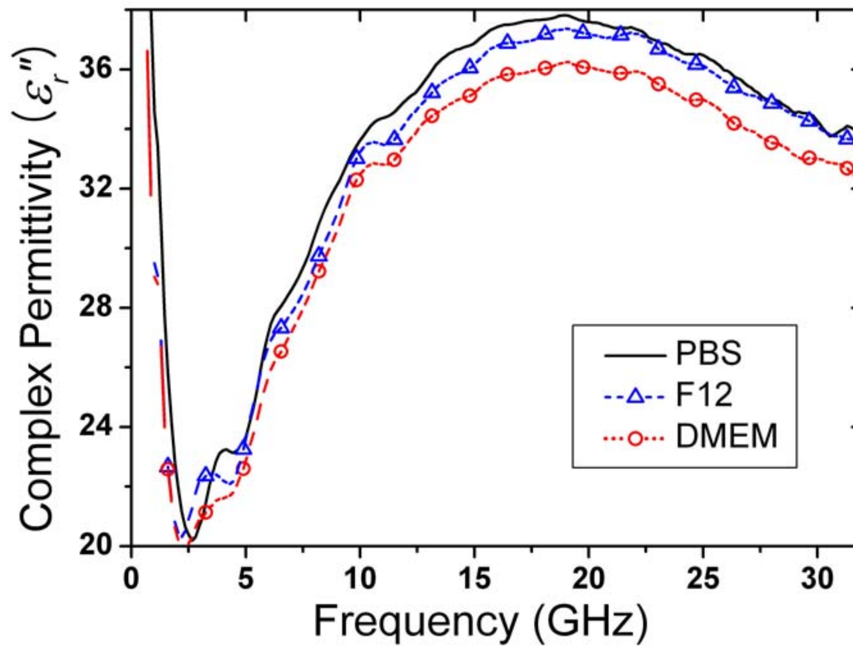
Fig. 9.16 shows the frequency dependence of the complex permittivity of 0.9 % saline. At frequencies larger than ~ 32 GHz, the real part of the permittivity (ε_r') deviates from the Cole-Cole prediction. For high loss materials such as saline, the CPW line becomes strongly dispersive at high frequencies and equation (9.4) cannot be used. Based on the above observation and considering the fact that cell culture media and cell suspensions have similar characteristics as 0.9% saline, it was decided to only measure cell culture media only up to 32 GHz.

9.4.3 Cell culture media measurements

Using the fabricated CPW sensors, various cell culture media were characterized. Most of media are similar to 0.9% saline but with additional components such as amino acids, inorganic salts and vitamins. Three different media are measured in this study; Dulbecco's modified eagle medium, phosphate buffered saline and Ham's F12 media. A number of measurements were performed on different 2 mm lines with the same ambient and calibration conditions. Fig. 9.17 shows the average complex permittivity of the three cell culture media. Phosphate buffered saline has the highest real and imaginary permittivity and Dulbecco's modified eagle medium has the lowest. The difference in permittivity between these two media is 3 ~ 4. This disparity can be attributed to the fact that Dulbecco's modified eagle medium contains additional components for the purpose of promoting cell growth.



(a)



(b)

Figure 9-17: Measured complex permittivity of Phosphate Buffered Saline (PBS) and cell culture media; Ham's F12 and Dulbecco's modified eagle medium (DMEM) (a) real (ε_r') and (b) imaginary part (ε_r'')

9.4.4 Cell suspension measurements

Cells of the human embryonic kidney cell-line (HEK-293) of an early passage were cultured in a humidified atmosphere with 5% CO_2 at 37 °C as a monolayer in 25 cm^2 flasks. They were grown in Dulbecco's modified eagle medium containing 10% foetal calf serum, 1% L-glutamine (Gibco, Eggenstein), 0.1% penicillin/streptomycin and 0.01 % gentamycin. Cells were harvested at confluency with trypsin/ethylene diamine tetraacetic acid (Gibco) for the purpose of measurement. After 5 minutes of trypsination in the incubator, enzymatic dissociation was subsequently stopped by adding ice-cold Ham's F12 medium supplemented with 10% foetal calf serum. Cells were washed two times and kept in 0.9 % saline. Cell density was measured with a hemocytometer.

In order to characterize CPW sensor response to cell viability, cell suspensions were treated with the cytotoxic chemical dimethyl sulfoxide and characterized as a function of time. Dimethyl sulfoxide is a hygroscopic fluid that acts as an organic solvent and especially affects the cell membranes. In concentrations of > 10%, it is absolutely cytotoxic. The cell membrane is a double phospholipid membrane which restrains the cell from its environment, while at the same time it is the structure by which the cell interacts with its environment via transmembrane and membrane coupled proteins and the cytoskeleton. Dimethyl sulfoxide is able to disturb those connections to induce transient defects (water pores) in the membranes and to promote a subsequent diffusive pore-mediated transport of salt ions [9-32]. Before permittivity measurements, a trypan blue staining test was performed on dimethyl sulfoxide treated cell suspensions using the same conditions as for the permittivity measurements. Dimethyl sulfoxide treated cell suspensions with a concentration of 2×10^6 cells/cm^3 were stained with trypan blue, a

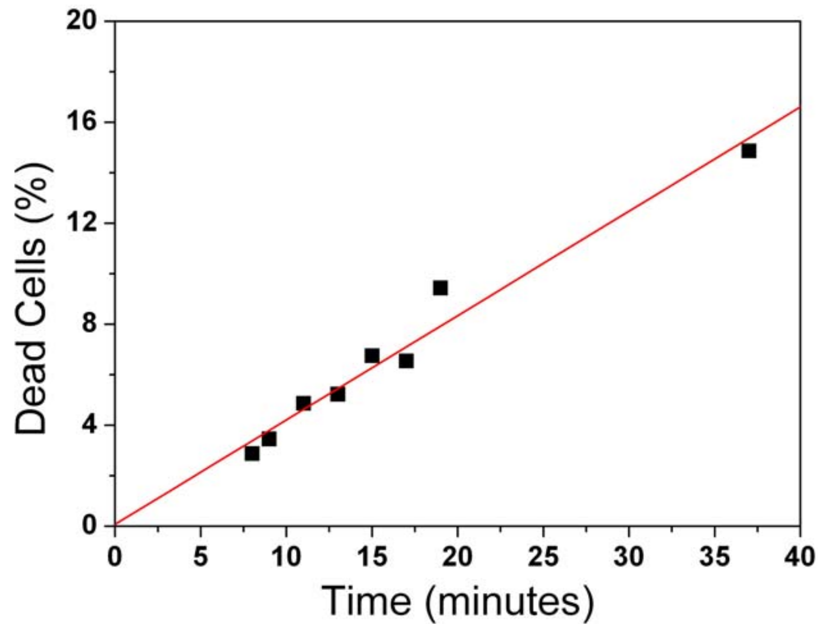
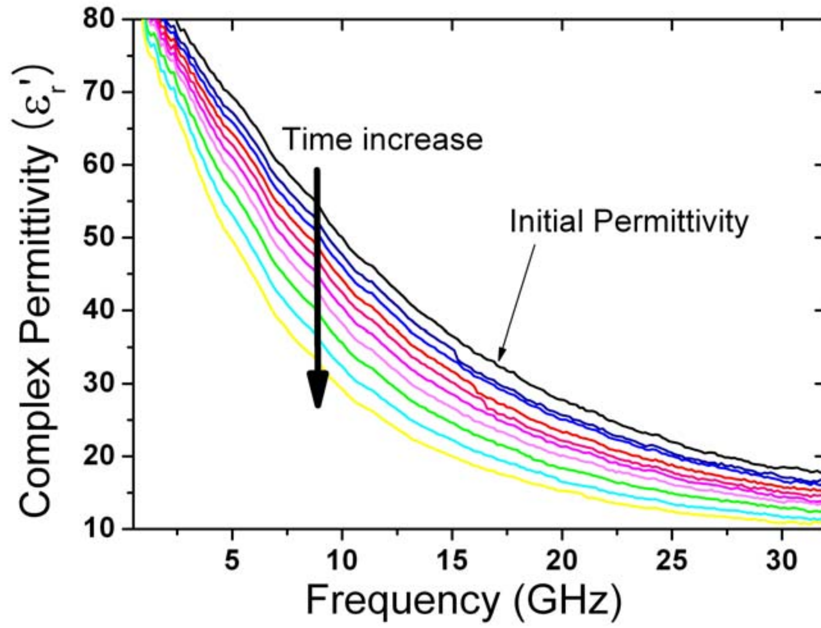


Figure 9-18: Percentage of dead cells over time due to 10 % dimethyl sulfoxide treatments measured by the trypan blue test.

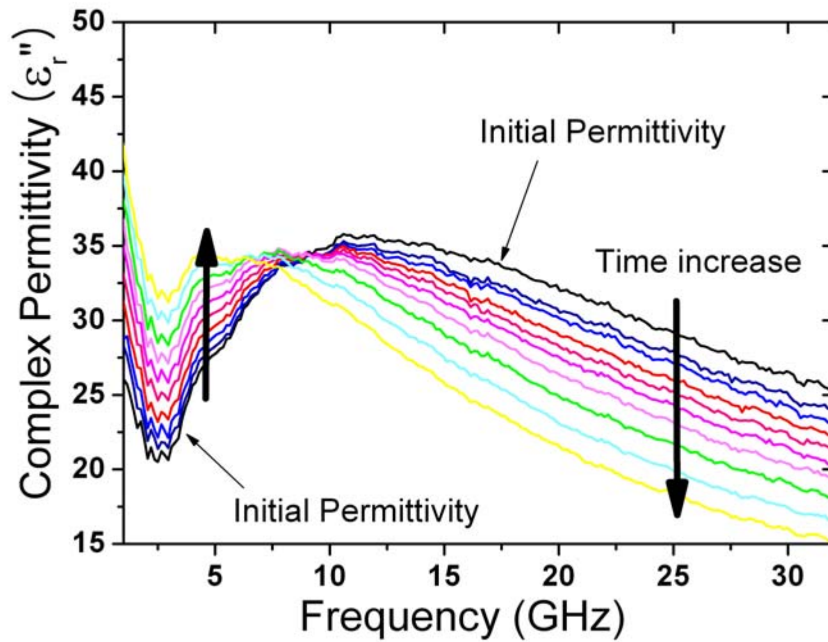
diazo dye used to selectively color dead cells. The stained cells were then counted in a hemocytometer. Fig. 9.18 shows the percentage of dead cells over time. For permittivity measurements, cell suspensions were treated with 10 % dimethyl sulfoxide in the same way and then immediately transferred to the CPW sensor for permittivity measurement.

Cell suspension measurements were performed using only 2 mm long lines. This was possible since the fabricated glass wafer contained several 2 mm lines on it and therefore multiple measurements were possible without cleaning the glass wafer. These are reported below. As listed in Table I, there are three different CPW types with various gap widths; 16 μm, 19 μm and 24 μm. It was found that the cell measurement results were not dependent on the gap width. This may be due to the size of the measured HEK-293 cell whose diameter was about 10~15 μm while the CPW gap size was enough to keep cells inside the gap where the EM-field maximum exists.

Fig. 9.19 shows the measured complex permittivity of dimethyl sulfoxide treated cell suspensions (HEK-293 cell in 0.9 % saline) at 2 min intervals for 20 min, and Fig. 9.20 shows the measured permittivity of cell suspensions without dimethyl sulfoxide treatment. Both the real and imaginary parts of ε_r decrease at high frequency as the time increases. The slight permittivity decrease in non-dimethyl sulfoxide treated cell suspensions is due to the slow evaporation of water during measurements. However, in the case of dimethyl sulfoxide treated cell suspensions, the decrease of both the real and imaginary parts of the permittivity are apparent at high frequencies. Fig. 9.21 shows the measured complex permittivity of dimethyl sulfoxide treated 0.9 % saline only (without cells). Fig. 9.19 and Fig. 9.21 show the same trends in permittivity change over time, but the degree of change is higher for permittivity of cell suspensions (with cells, Fig. 9.19) than for permittivity of 0.9 % saline (without cells, Fig. 9.21). Decreases in the real part of permittivity at 10 GHz are 20.8 and 13.7 with and without cells respectively. In the case of the imaginary part of the permittivity, decreases at 30 GHz are 10.5 and 6.8 with and without cells respectively.

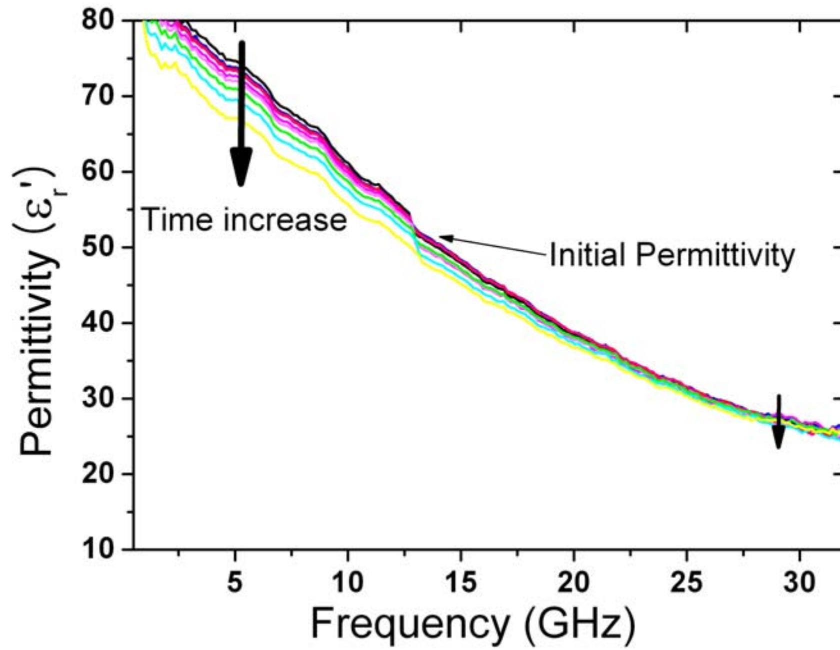


(a)

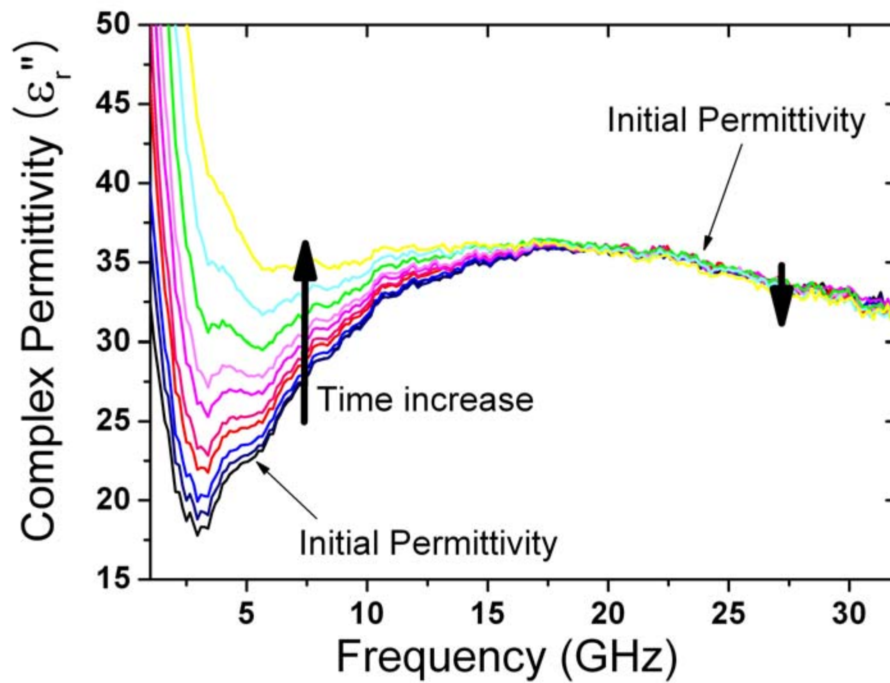


(b)

Figure 9-19: Measured complex permittivity of 10 % dimethyl sulfoxide treated HEK-293 cell suspensions (cells in 0.9 % saline) with concentration of 2×10^6 cells/cm^3 with 2 min intervals up to 20 min (a) real part (ε_r') and (b) imaginary part (ε_r'')

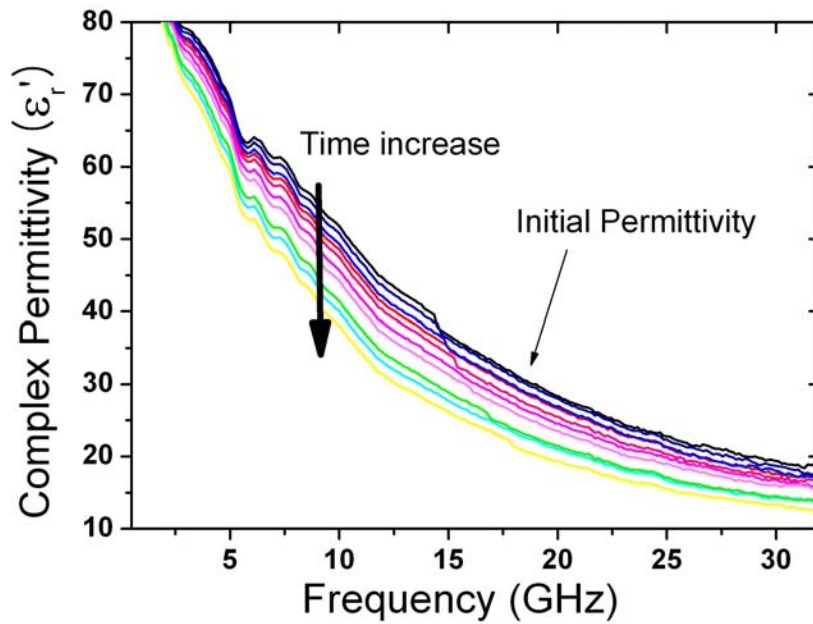


(a)

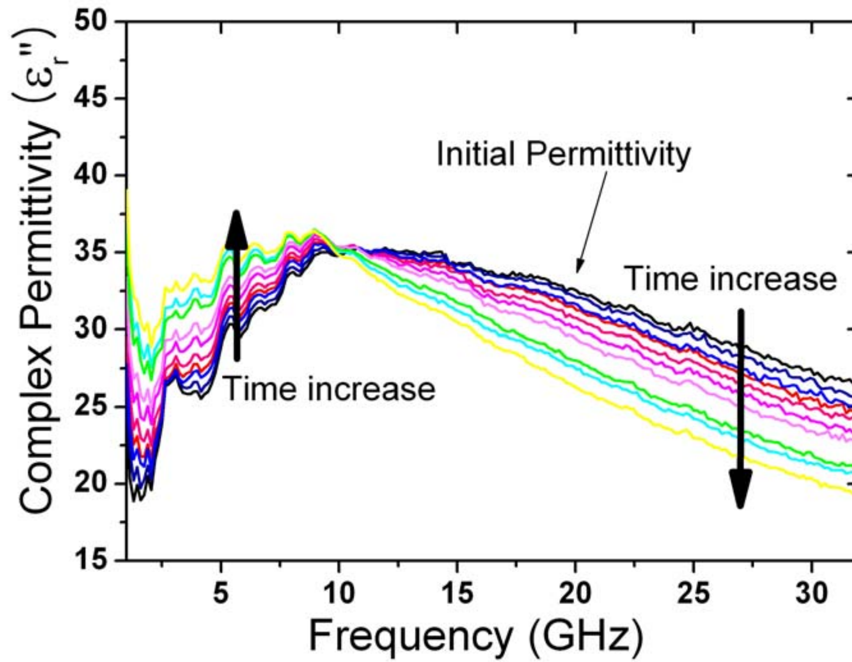


(b)

Figure 9-20: Measured complex permittivity of HEK-293 cell suspensions with concentration of 2×10^6 cells/cm^3 without dimethyl sulfoxide treatment with 2 min intervals up to 20 min (a) real part (ε_r') and (b) imaginary part (ε_r'')



(a)



(b)

Figure 9-21: Measured complex permittivity of 10 % dimethyl sulfoxide treated 0.9 % saline (no cells) with 2 min intervals up to 20 min (a) real part (ε_r') and (b) imaginary part (ε_r'') . (There are calibration errors at low frequencies)

The permittivity variation at fixed frequency is shown in Fig. 9.22. The permittivity changes of cell suspensions with cells were subtracted by the permittivity changes of 0.9 % saline without cells in order to present permittivity change of cells only. Both real and imaginary parts of permittivity changes are in linear behavior and they are corresponding to the cell death over time tested by the trypan blue staining test in Fig. 9.18. We suspect the reduced permittivity and hence polarizability of the cell solution is a result of the compromised cell membrane due to dimethyl sulfoxide. It is also possible that cellular components released upon death further affect the cell solution permittivity

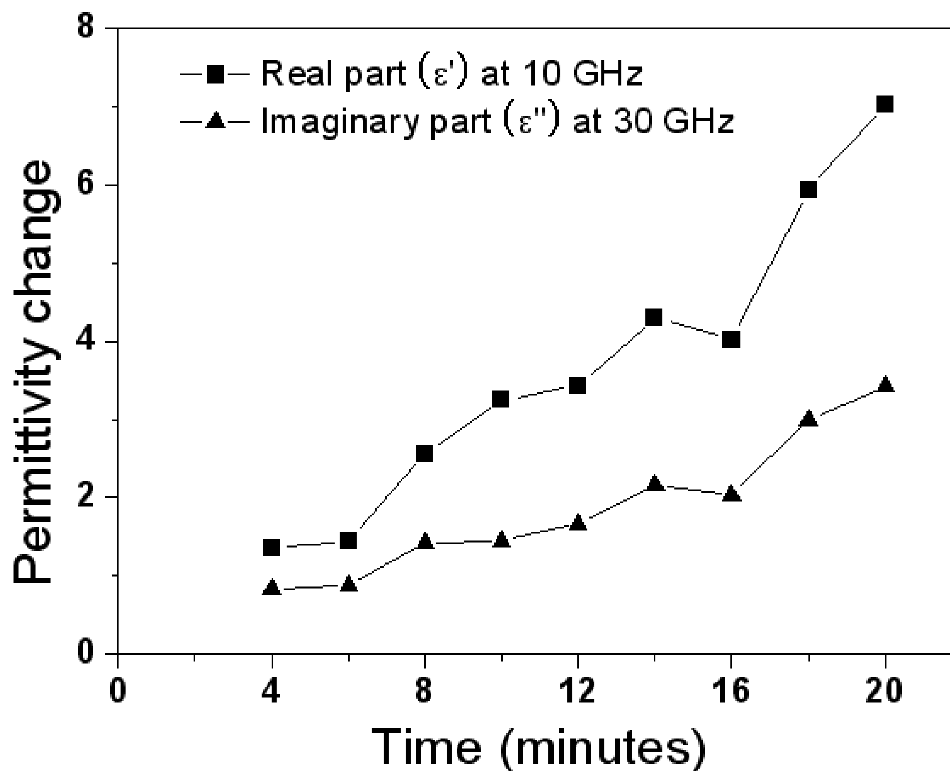


Figure 9-22: Real and imaginary parts of permittivity change over time for HEK-235 cells. (real part data at 10 GHz and imaginary part data at 30 GHz) The data are normalized to reference dimethyl sulfoxide treated cell media (0.9% saline without cells).

9.5 Summary

Wideband complex permittivity measurements of liquids and cell suspensions by CPW sensors using SU-8 containers were presented. A simple de-embedding methodology using ABCD matrices, quasi-TEM analysis and conformal mapping was described. Reference liquid measurements of methanol, isopropanol and 0.9 % saline allowed verification of the CPW sensing principle and the de-embedding method used for data extraction. Three kinds of cell media without cells were characterized in terms of complex permittivity and they showed permittivity difference due to the components of the cell media. Cell suspensions of Human embryonic kidney cells (HEK-293) were characterized over the frequency range of 1 to 32 GHz and their complex permittivity was found to vary over time due to disruption of the cell membrane by dimethyl sulfoxide. These results may open the way to a promising evaluation approach of biological systems based on high frequency dielectric constant characterization.

CHAPTER 10

Conclusions and Future Work

Gallium Nitride (GaN) based semiconductor devices have been intensively investigated over the last ten years due to their inherent material properties; high breakdown voltage, high saturation and peak carrier velocity, good thermal conductivity, low dielectric constant, high melting point and direct bandgap. These physical properties enable GaN-based Heterostructure Field Effect Transistors (HFETs) to be most suitable for high power & frequency applications. In this dissertation, III-Nitride Metal Insulator Semiconductor (MIS) based FETs (AlN/GaN Metal Insulator Semiconductor FETs (MISFETs)) have been investigated through theoretical studies, simulations of device operation, process optimization, characterization and modeling. Novel *in-situ* Si_3N_4/AlN/GaN MISFETs were developed for the first time and allowed substantial improvement of the AlN/GaN MISFETs' DC and RF characteristics presented in this work. As a circuit application of GaN-based HFETs, a wideband balanced low noise amplifier using low noise AlGaN/GaN HEMTs was designed, simulated, and characterized to demonstrate the use of such devices in Microwave Monolithic Integrated Circuits (MMICs). A diode application of III-Nitride materials was also explored, AlGaN/GaN-based superlattice diodes were designed, fabricated and characterized for this purpose as possible candidates for presenting Negative Differential Resistance (NDR) and thus acting as signal sources at millimeter or sub-millimeter waves. Current-

voltage measurements showed the presence of NDR at room temperature. This is the first observation of NDR in an III-Nitride based superlattice diode. Using the developed integrated device fabrication technology, an integrated CPW-based bio sensor was developed and utilized for complex permittivity characterization of liquids and cell suspensions at microwave frequencies. This opens the way to the integration of microwave semiconductors and sensors based on III-Nitride technology. III-Nitrides materials are ideally suited for biological studies due to their biocompatibility and chemical inertness, their high sensitivity in charge sensing, as well as, the possibility of integration of light sources necessary for monitoring biological processes. Thus studies of thus type could consequently lead to the development of new generations of lab on the chip components. The thesis covers various aspects of III-N technology spanning form device technology development to device simulation and MMIC applications, as well as, development of integrated bio sensors. Future work will be necessary to allow further improvement of the reported device and MMIC characteristics, as well as bio-sensors.

The sections below describe the key results obtained in the course of this Ph. D work. Future work is also proposed together for each of the discussed topics.

Device simulation on GaN-based HFETs

Simulation studies are essential for understanding many aspects of semiconductor device and MMIC operation. A comprehensive simulation study can reduce time, effort and cost for the realization of novel device design schemes, establishment of growth conditions and optimization of MMIC operation.

Using the MEDICI device simulator, various types of III-Nitride based HFETs were studied. Non-recessed gate and recessed gate AlGaN/GaN Single-heterostructure HEMTs

(SHEMTs) were designed based on a simplified δ-doping model for the piezoelectric and spontaneous polarization effects. This model, although not perfect, allowed the evaluation of the advantages of recessed gate over non-recessed gate structures. Good matching to experimental characteristics could be obtained by making use of the measured contact resistance value in the simulation of non-recessed devices. Various types of Double-heterostructure HEMTs (DHEMTs) were designed and simulated using AlGaN/GaN, AlGaN/InGaN and InGaN/GaN heterojunctions. The superiority of DHEMT on SHEMT and the advantages of using InGaN instead of GaN channel were examined and simulated based on three DHEMT designs (AlGaN/GaN/AlGaN, AlGaN/InGaN/AlGaN, and AlGaN/InGaN/GaN DHEMT). The simulation showed that AlGaN/InGaN/GaN is the preferred choice for III-N based DHEMTs due to improved carrier confinement at the 2DEG channel and mobility increase thanks to the InGaN channel layer.

At a next step of the simulation study, MIS-based device analysis was performed using the drift-diffusion simulation approach of ISE-TCAD. AlN/GaN MISFETs and AlGaN/GaN HEMTs with 1 micron gate length were simulated for this purpose. ISE-TCAD fully supports GaN-based material parameters, which was not the case of the MEDICI program where our own developed data base of III-N material characteristics was employed. The simulation results showed that AlN/GaN MISFETs had 30 % higher transconductance and several orders of magnitude lower gate leakage than conventional AlGaN/GaN HEMTs.

There are several aspects to be further studied in III-N device simulations. First, hydrodynamic simulations should be performed for submicron gate MISFETs and HEMTs; submicron gates of 100 nm or less are necessary for high frequency operation of

III-Nitride FETs. Another interesting aspect is thermal simulation. In the simulation scheme used in this study, the isothermal condition is applied throughout the calculations. However, as shown in Chapter 5, thermal effects are pronounced in the fabricated MISFETs due to the low thermal conductivity of the sapphire substrate. Using the hydrothermal simulation, the heat generation in each part of the device can be simulated and can be accounted for in the design of the device later on. Moreover, InGaN/GaN heterostructures should be further studied using a better simulation scheme that includes the latest III-N material parameters for InGaN as the understanding of this material system improved considerably over the last few years

Fabrication technology of III-Nitride based FETs

Fabrication processes were described for GaN-based semiconductor devices. These were well controlled after intensive optimization. Although this is particularly true for standard AlGaN/GaN HEMTs processing, there is room for AlN/GaN MISFET optimization where there are still many challenges to overcome. Ohmic contact optimization was one of the targets of the work. Specific contact resistance values in the range of 10^{-4} Ωcm^2 have been achieved by simple KOH-based wet etching. However, the chemical etching of AlN was not always reproducible due to its strong temperature and concentration dependence. The etching process was well established for 5 nm thin AlN layers. For better MISFET operation, further improvement of ohmic contact quality was necessary. This was achieved by depositing an *in-situ* Si_3N_4 layer on the AlN surface. Specific contact resistance values in the range of 10^{-5} Ωcm^2 have been achieved and are close to the specific contact resistance value of AlGaN/GaN HEMTs.

For AlN/GaN MISFETs, submicron gate technology based on 250 nm, 200 nm and

150 nm gate length processes havef been developed. The final target of AlN/GaN MISFET is high power and high frequency operation with gate length smaller than 100 nm, so that reduced short channel effects can be ensured by using ultra thin AlN as barrier layer. In addition, for higher power applications, a field-plate gate process for submicron gates should be developed. This would require a two step electron beam process; one for Si_3N_4 etching for gate foot process and another for field plate writing.

Characterization of III-Nitride based FETs

In this work, the processed devices were evaluated using several measurement techniques such as DC, pulsed IV, S-parameter measurement and load pull measurements. In house grown and fabricated AlN/GaN MISFETs and *in-situ* Si_3N_4/AlN/GaN MISFETs were fully characterized with these measurement techniques. The AlN/GaN MISFETs showed a maximum drain current density (I_{DSmax}) of 380 mA/mm and a peak extrinsic transconductance (g_{mo}) of 85 mS/mm. Power characteristics were evaluated for the first time and showed an output power density of 850 mW/mm with 23.8% PAE and 13.1 dB linear gain at 2 GHz. Current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) were measured to be 5.85 GHz and 10.57 GHz respectively. Improvements of AlN/GaN MISFETs' DC and RF characteristics were achieved with *in-situ* deposited Si_3N_4. The fabricated *in-situ* Si_3N_4/AlN/GaN MISFET showed I_{DSmax} of 403 mA/mm and g_{mo} of 206 mS/mm. f_T and f_{MAX} were found to be 10.2 GHz and 32.3 GHz respectively, which correspond to a factor of 2 to 3 improvement of DC and RF characteristics over non-passivated devices. An 150 nm long gate device on *in-situ* Si_3N_4/AlN/GaN MISFETs exhibited promising high frequency characteristics; f_T = 50 GHz and f_{MAX} = 110 GHz.

In order to further characterize the fabricated devices, pulsed IV measurements were performed and gate lag effects were characterized under various pulsed bias points. Due to the limit imposed by the measurement setup, the initial V_{DS} bias could only be set to 0V. With modification of the pulsed setup, a higher V_{DS} bias such as V_{DS} = 15V should be possible. The drain lag effect for AlN/GaN MISFETs could then be further investigated. Furthermore, pulsed IV measurements should be performed for *in-situ* Si_3N_4/AlN/GaN MISFETs in order to evaluate the expected low DC-RF dispersion effects resulting through surface passivation.

Small and large signal modeling of III-Nitride based FETs

Small signal modeling based on a 14 element equivalent circuit was performed. A non linear optimization technique was employed to reduce fitting time and increase model accuracy. Extrinsic element extraction techniques were also performed using a MATLAB graphical user interface developed for this purpose. A fast and iterative method of large signal modeling was successfully developed using the Agilent EEHEMT1 model. The model was found to work well for AlN/GaN MISFETs in terms of DC characteristics, S-parameters and power matching. Modeling results of this type are reported for the first time for AlN/GaN MISFETs. Accurate modeling of the device is the first step for accurate MMIC design. Therefore, accurate large signal modeling is necessary for future studies of power amplifiers with AlN/GaN MISFETs. Small and large signal modeling of *in-situ* Si_3N_4/AlN/GaN MISFET should also be investigated in the future.

Wideband balanced AlGaN/GaN HEMT MMIC LNA

The design, simulation, fabrication and characterization of a wideband balanced low

noise amplifier were described. The developed balanced AlGaN/GaN HEMT MMIC LNA demonstrated for the first time broad bandwidth of 3-16 GHz and high gain of ~ 20 dB using a coplanar waveguide (CPW) Lange coupler. The MMIC LNA shows a minimum noise figure of 4 dB with an associated gain of 20dB. A 38 dBm output third order intercept point (OIP3) was demonstrated at the frequency of 8 GHz. This is the first report of balanced MMICs with AlGaN/GaN HEMTs. The results suggested that the balanced GaN HEMT LNA is a promising candidate for robust LNA applications such as transceiver front-ends.

As a next step, other types of MMICs taking advantage of the high frequency properties of AlN/GaN MISFETs should be developed. This includes MMIC oscillators with AlGaN/GaN HEMTs and AlN/GaN MISFETs; there has been no report on AlN/GaN MISFET based MMICs so far. Therefore, developing such new types of MMICs is highly attractive, especially for extending MMIC III-Nitride based MMIC technology to millimeter-wave frequencies.

AlGaN/GaN superlattice diode

$Al_xGa_{1-x}N$/GaN based superlattice diodes were designed, fabricated and measured. The materials necessary for SL diode designs were determined based on theoretical studies and were grown and optimized by MOCVD. Diodes of this type were processed. Room temperature DC measurement showed a stable Negative Differential Resistance (NDR) around 1 V with 1.3 peak to valley ratio. However, the NDR I-V characteristics were found to depend on the charge state of the device as determined by the bias voltage applied. This is the first report of NDR in III-Nitride based superlattice diode. C-V measurements were also performed and showed the presence of negative capacitance

characteristics, which are possibly caused by carrier trapping and emission effects in the well and the heterostructure interface.

In spite of these first promising results, III-Nitride based superlattice diodes require significant improvement in terms of growth. As indicated by the capacitance measurements, trapping and de-trapping effects are presently pronounced in superlattice diodes and may hinder signal generation. Therefore, further investigation of these effects is required such as low temperature measurements allowing better understanding of the trapping and de-trapping features. Overall, further effort is necessary for obtaining high quality AlGaN/GaN heterostructures and achieving high frequency signal generation using this technology.

Integrated CPW bio sensors for complex permittivity measurements

Coplanar waveguide (CPW)-based sensors, with integrated SU-8 liquid containers, were developed and used for wideband complex permittivity measurements of liquids, cell media and living cell suspensions. Complex permittivity measurements of methanol, isopropanol and 0.9 % saline showed good agreement with theoretical values over the frequency range of 1 ~ 40 GHz. Commonly used cell media in the absence of cells were characterized over the frequency range of 1 ~ 32 GHz for the first time. Finally, results for live human embryonic kidney cell suspensions measured over the same frequency range were described. Dimethyl sulfoxide toxicity tests on cell suspensions showed time dependent permittivity changes due to cell disintegration and diffusion process. Changes of the real and imaginary part of permittivity over 20 minutes showed 13% and 11% decrease at 10 GHz and 30 GHz respectively. . These results are expected to open the

way to a promising evaluation approach of biological systems based on high frequency characterization.

As a future work, different types of toxic chemicals on cell suspensions should be studied with the same method. Biological and chemical interaction between cells and dimethyl sulfoxide and its effect on complex permittivity has not been clearly understood yet. Therefore, other toxic chemical affects on cell suspensions should be studied and the mechanism behind them should be understood. Additionally, micro fluidic channels could be explored in conjunction with CPW lines for characterizing even smaller volumes of cell suspensions. Single cells may be evaluated with this approach and differentiation of cell types may be possible.

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