

WAFER-LEVEL PACKAGING FOR ENVIRONMENT-RESISTANT MICROINSTRUMENTS

by

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To my family: Your love and dedication made this possible

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Abstract

WAFER-LEVEL PACKAGING FOR ENVIRONMENT-RESISTANT MICROINSTRUMENTS

by

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A generic wafer-level packaging technology for high-performance MEMS devices, operating under harsh external conditions is developed. This technology not only provides physical protection from the surroundings, but also provides thermal and mechanical isolation to enhance device performance. The wafer-level encapsulation and generic assembly approach accommodate a wide range of MEMS devices with minimal process lead-time and manufacturing cost. To realize this environment-resistant package, thermal isolation, mechanical isolation, generic device transfer/integration, wafer-level vacuum packaging, and feedthroughs have been developed.

The environment-resistant package consists of two substrates: a platform substrate providing thermal and mechanical isolation, and a package cap wafer providing vacuum encapsulation. Thermal stabilization is provided by oven-controlling the device at a temperature higher than the maximum environment temperature utilizing a heater and a temperature sensor located on the platform or the MEMS device. The heated structure is thermally isolated from the environment by isolation suspensions, anti-radiation shield, and vacuum encapsulation to minimize heat loss. The isolation suspensions are designed with high thermal resistance for minimal heat loss, sufficient stiffness for mechanical support, and flexibility for rejecting environmental vibrations. The package cap seals the MEMS device in vacuum. Vertical feedthroughs for a signal delivery are formed on the platform substrate or the cap wafer. These vertical feedthroughs save area and allow direct attachment to circuit boards. Shock absorption layers, and a getter layer for achieving and maintaining high vacuum are deposited on the inside wall of the package.

Performance is evaluated by packaging Pirani gauges and mode-matched tuning fork gyroscopes. The package size is $1.2 \times 1.2 \times 0.17 \text{ mm}^3$, and the packaged device size is $4.5 \times 4.5 \times 0.5 \text{ mm}^3$. The package has maintained vacuum pressure of $\sim 6 \text{ mTorr}$ for ~ 1 year. A packaged gyroscope shows a high-Q mode-matched operation ($Q \sim 65,000$) at a constant temperature of $-5 \text{ }^\circ\text{C}$. Allan variance analysis displays an estimated angle random walk (ARW) of $0.012 \text{ }^\circ/\sqrt{\text{hr}}$ and a bias instability value of $0.55 \text{ }^\circ/\text{hr}$ at a constant $-5 \text{ }^\circ\text{C}$. Drive frequency stability of $0.22 \text{ ppm}/^\circ\text{C}$ is obtained using a compensated oven-control approach. Low power consumption of 33 mW for oven-control at $80 \text{ }^\circ\text{C}$ is demonstrated when the environment temperature is $-30 \text{ }^\circ\text{C}$. The temperature control accuracy is $\pm 0.2 \text{ }^\circ\text{C}$.

Chapter 1

Introduction

MEMS (Micro-Electro Mechanical System) devices such as micromachined sensors, actuators, and microinstruments have made significant progress since the first commercial products (i.e. pressure sensor) were demonstrated in the 1980's [1]. In recent years, the MEMS business has grown significantly. It is expected to reach almost \$8 Billion by the end of 2008, and double that amount by 2012 with strong growth in the consumer, automotive, medical and industrial sectors (Figure 1.1) [2].

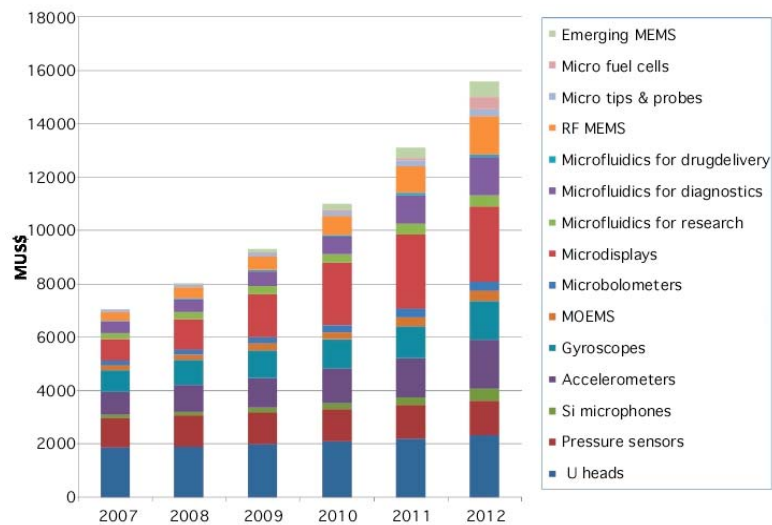


Figure 1.1 MEMS market forecast 2007-2012 in value (dollar) [2].

As the MEMS industry grows, demand for high-performance MEMS devices has also increased. These precision instruments are needed for gas and chemical analysis, environmental and health monitoring, all of which are critical elements of many emerging applications. They often require specific environmental conditions including controlled surrounding atmosphere (i.e. vacuum/hermetic), temperature isolation, and mechanical isolation.

Environmental conditions have a profound impact on the performance of precision micromachined instruments (Table 1.1). External conditions such as temperature, humidity, vibration, and shock can easily corrupt the output of an instrument, and can induce undesirable long-term effects that are not correctable using electronics. The need for protection against environmental conditions becomes more pronounced as the performance levels are increased. Therefore, to realize the potential of high-performance MEMS, it is critical that the environment surrounding the instrument be protected or controlled.

Table 1.1 Environmental factors impacting MEMS devices [3].

Mechanical	Chemical	Physical
Stress	Gases	Temperature
Vibration	Humidity	Pressure
Shock	Corrosion	Acceleration

Typically, the environmental protections of precision MEMS devices have been provided by a package, which has been and will continue to be a significant challenge in the MEMS area. Although the electronics manufacturing industry has a robust and viable infrastructure, direct application of electronics packaging techniques to most MEMS parts is not feasible due to the complexities of their operational structure and domain. Unlike ICs, most MEMS devices interact with the environment or other components

directly or indirectly through electrical, mechanical, thermal, chemical or optical interfaces [4]. For that reason, the MEMS package needs to comply with the requirements of traditional protections as well as provide application-specific elements such as gas access holes in pressure sensors or optical windows in MOEMS devices [5].

Because of the inherent difficulties in packaging MEMS devices, MEMS developers face many challenges in yield, size, standardization, process lead-time and cost. To accommodate the application specific elements in packaging, specially designed packages have typically been employed for housing MEMS devices. These customized packages often require chip-scale handling and assembly processes that are not desirable in mass production. This chip-scale process increases the probability of damage and loss of the device, and the size of the external package is sometimes too large to assemble into small system level products.

Unlike the IC industry, standardization of the packaging technology is not widely available in the MEMS industry. This absence of standard results from the diversity of MEMS applications and operational requirements. Most customized packaging solutions cannot be translated from one specific application to another. This causes long lead-time in developing MEMS, and cost increase.

The cost of single-chip packaging processes, utilizing customized packages, is usually too high to meet the market's needs [6]. Like the IC industry, MEMS developers also have tried to shrink the size of the bare MEMS device to reduce the manufacturing cost. However, this effort alone is not sufficient to maximize the return on investment, because the packaging of small devices increases costs and effort. This size reduction

approach also cannot be applied in some applications such as high-performance inertial sensors due to their inherent physical and operational limitation.

Recently most MEMS development efforts have been focused on reducing size and cost through utilizing wafer-level packaging [7]. A typical wafer-level packaging approach encapsulates the MEMS device before it is singulated from its host wafer. This approach reduces cost as well as protects the device during back-end processes, including dicing and die handling. By encapsulating the device, one can also provide hermetic or vacuum environments, which is often required in stable operation of many sensors, including resonant sensors and infrared detectors.

Furthermore, the MEMS package not only provides the traditional benefits such as simple protections and selective environmental interfaces, but also can be an integral part for improving the performance of the product itself. In other words, in addition to the MEMS specific packaging elements, the package can provide additional functions. For example, by adding thermal and vibration isolation, the packaged MEMS device can be more effectively protected from the environment, and provide higher performance. Typically, these additional functions have been implemented using specially designed large-scale enclosures or board-level system assemblies. This traditional approach requires die-level or chip-scale handling which is not an effective manufacturing approach. It is desirable to integrate these functions during the wafer-level packaging processes before die separation.

Developing a standard, or generic, packaging technology is a desirable feature of future microsystems packaging. This means that different devices with different applications or fabrication processes can be packaged without developing a completely

new set of packaging technology. To realize this approach, the packaging technology needs to be compatible with a variety of device types, and amenable to re-use and re-configuration.

In summary, a desirable goal in developing MEMS packaging technology is to develop a cost-effective generic wafer-level packaging approach that can preserve and enhance device performance. To fulfill this goal, several key technological challenges in device encapsulation/protection, interconnections/feedthroughs, and device integration/assembly are required to be resolved [8]. The MEMS package should protect the enclosed MEMS device with selective access to the external environment. The package also needs to provide long-term stable, small, and low parasitic feedthroughs. It is also desirable to have a standard, modular assembly technology that can be applied to a wide range of MEMS applications.

The goal of this thesis is to offer generic wafer-level MEMS packaging technologies that provide environmental-resistance functions including thermal and mechanical isolation. In order to fulfill these objectives, a new environmentally isolated wafer-level package technology and a generic device transfer/assembly method for the integration of monolithic and hybrid MEMS into the package have been developed. To evaluate this packaging technology, high-performance gyroscopes, Pirani gauges and test chips have been packaged.

The rest of this chapter introduces typical MEMS packaging processes and requirements. Then, a wafer-level environment-resistant package concept for packaging high-performance MEMS devices will be presented. To close the chapter, the contributions and organization of the thesis are outlined.

1.1 MEMS Packaging

1.1.1 Role of MEMS Packaging

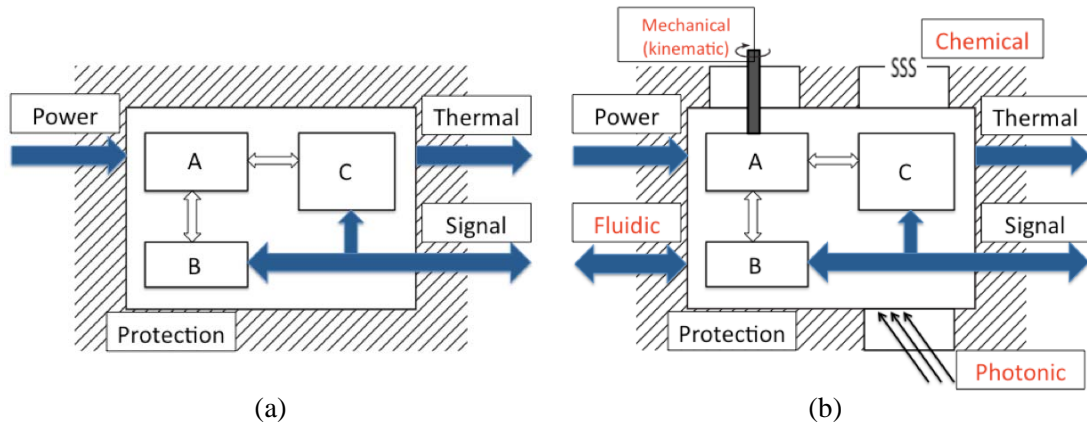


Figure 1.2 Functions of packaging: (a) traditional: IC, (b) MEMS packaging [9].

In general, packaging provides four key functions including power delivery, signal mapping/redistribution, thermal management, and environmental protection, as illustrated in Figure 1.2 (a) [9]. Power delivery and signal transport are necessary for the operation of electronics or devices within the package. However, in MEMS packaging, additional interfaces/functions need to be involved (Figure 1.2 (b)).

Table 1.2 MEMS applications and their specific interface requirements.

Application	Interface Requirement
Pressure sensor	Physical access hole
Inertial sensor	Vacuum/hermetic environment Room for moving parts
IR sensor	IR access window
Actuator	Room for moving part
Bio MEMS	Fluid access hole
Gas sensor	Gas access hole

These interfaces are, directly or indirectly, related to the application, and MEMS has a large number of diverse applications. As a result, a variety of functional interfaces

such as optical, RF, thermal (radiation, conduction, and convection), fluidic (liquids or gases), mechanical (body or surface loadings) and others (Table 1.2), are needed.

Figure 1.3 shows typical MEMS packages of a pressure sensor and inertial sensors. These packages provide not only physical protection but also allow for operational interfaces (Figure 1.3 (a)), hybrid integration with circuitry (Figure 1.3 (b)), or subsystems (Figure 1.3 (c)).

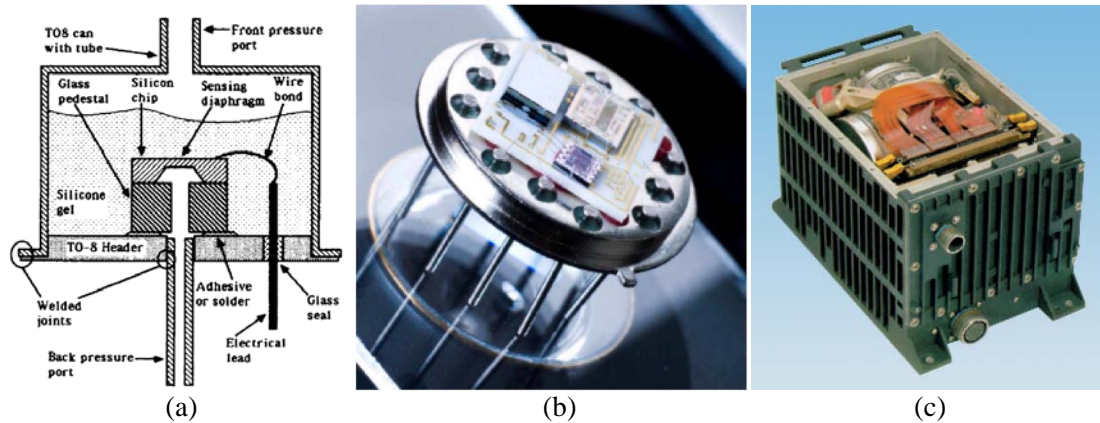


Figure 1.3 Examples of higher level MEMS packages: (a) Conceptual drawing of a typical TO-8 (Transistor Outline-8) pressure sensor package for differential pressure [10], (b) Accelerometer assembled on a hybrid substrate and packaged in a TO can [11], (c) GPS-Inertial navigation system for launch and reentry vehicles [12].

1.1.2 MEMS Packaging Procedures

As mentioned before, the packaging of MEMS devices is application dependent, and typically imposes a number of additional requirements compared to standard IC packaging. Packaging can be categorized under five hierarchical levels (Table 1.3) [13]. MEMS devices usually consist of delicate moving structures, and require free space with special environments or selective access holes. Once the moving structure is released, it is susceptible to physical disturbances. Therefore, 0-level packaging or protection is an important step on the path to 1-level packaging.

Table 1.3 IC and MEMS packaging hierarchy [13].

Level		IC	MEMS
0	Element	Transistor within IC	MEMS structure
	Interconnected /Encapsulated by	IC metallization	Conductive feedthroughs Thin film / shell (temporary or permanent)
1 “Chip-to-Package”	Element	ICs, discrete components	Discrete MEMS die
	Interconnected by	Package leadframes (single-chip) or multichip module interconnection system	Package leadframes 3D multichip module system Direct flip-chip interconnection
2 “Package-to-Package”	Element	Single- and multi-chip packages	
	Interconnected by	Printed wiring boards	
3 “Board-to-Board”	Element	Printed wiring boards	
	Interconnected by	Connectors / backplanes (busses)	
4 “System”	Element	Chassis or box	
	Interconnected by	Connectors / cable harnesses	

After finishing wafer-level fabrication of the MEMS structures, the MEMS dies are singulated with proper 0-level protection. Typically, these dies are separated by a dicing saw tool with a diamond blade while passing a coolant stream over the device wafer. This dicing procedure can damage released MEMS structures unless they are properly protected. The cooling water stream can break and cause stiction of the released structures. Debris or particles generated during this process can prevent operation.

Various approaches have been used to protect the device during the separation process [14] and they can be categorized under four techniques (Figure 1.4). The first approach uses partial dicing and separation. One such approach was developed by Texas Instruments (TI) for its Digital Micromirror Device (DMD) [15]. In this case, the device wafer is partially diced, and then the structures are released at the wafer-level. After cleaning and release, the wafer is ground from the backside down for complete separation of the dies utilizing a specially designed wafer fixture. Instead of the backside grinding, the wafer can be cleaved through the partially diced lines.

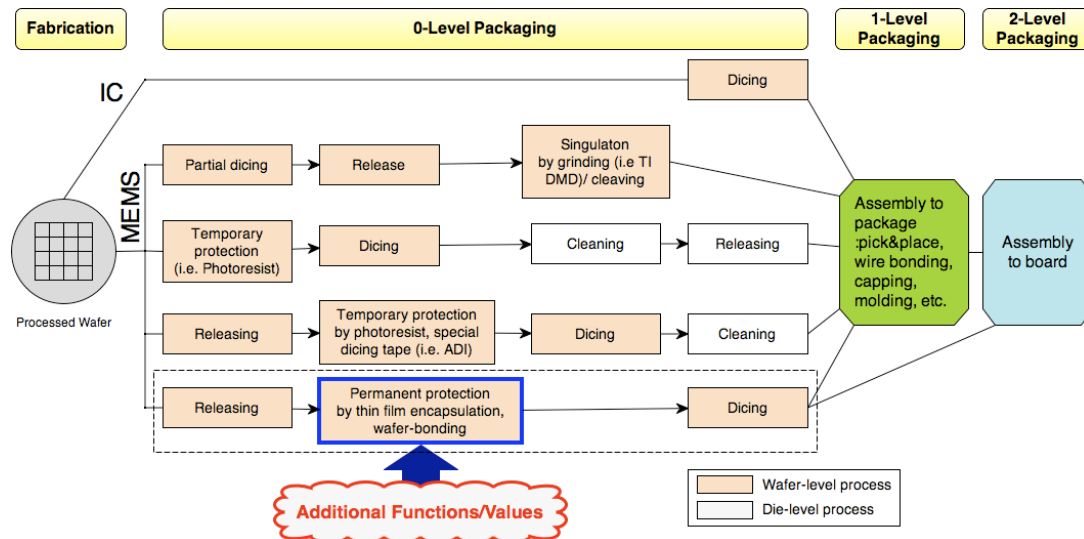


Figure 1.4 Typical packaging processes: 0-, 1-, and 2-level packaging.

The second approach uses a temporary protection before releasing the structures. The protected wafer is diced, cleaned, and then released. In this case, the cleaning and releasing processes are done at the die-level, which is not preferable in mass production due to its high cost.

The third approach uses temporary protection after releasing the structures. After the wafer-level releasing process, the released structures are covered by removable materials such as photoresist. After dicing the wafer, these protection materials are removed at the die-level. This approach also requires undesirable die-level processing. An alternative to protecting the released MEMS device during dicing is that developed by Analog Devices [16]. A specially designed adhesive film with cavities in the region of the released structures is placed on the front of the wafer. This wafer is then diced from the backside to separate the die. The adhesive film protects the die from the coolant stream and particles.

The fourth approach uses a permanent protection or encapsulation after releasing and before dicing. In most cases, “wafer-level MEMS packaging” refers to this approach. The permanent protection is usually done by wafer-level thin-film over-coating and wafer bonding. This approach has several advantages: First, this process uses conventional fabrication tools. Second, various materials can be used for specific applications. For example, MOEMS devices can be encapsulated using transparent materials. Third, controlled environments such as vacuum and hermetic encapsulation can be obtained. Forth, dicing is the last step, so no die-level process is required. Fifth, this encapsulating structure also can act as an operational part of the MEMS device. In other words, it cannot only provide passive protection, but also contribute additional functions or values. For example, by proper feedthrough configurations and stacking separately processed wafers together, the diced chip can be ready for surface-mounted device (SMD) assembly without 1-level packaging [17].

Another advantage of this approach is that it can implement application specific functions and additional functions, which are usually added in the 1-level packages. For example, environmental access holes for measuring pressure can be integrated in the 0-level package cap instead of conventional TO (Transistor Outline) can package (Figure 1.3 (a)). Additional functions such as thermal and vibration isolation can enhance the performance of the MEMS device without using sometimes complicated and die-level assemblies.

More advanced packaging is possible by incorporating the integration of MEMS into systems during the lower-level processes. This subsystem integration has been realized by conventional wire bonding and mounting into standard packages (Figure

1.3(b-c)), but increasingly compact packaging techniques including multichip modules and 3D chip stacking are being developed for complex MEMS demands. This would replace the widely used hybrid approaches, and enable direct integration to system boards with small footprint. This approach also can reduce manufacturing cost, which is one of most important factors in packaging MEMS. Figure 1.5 illustrates the advanced MEMS packaging trend, which adds more options to the lower-level processes.

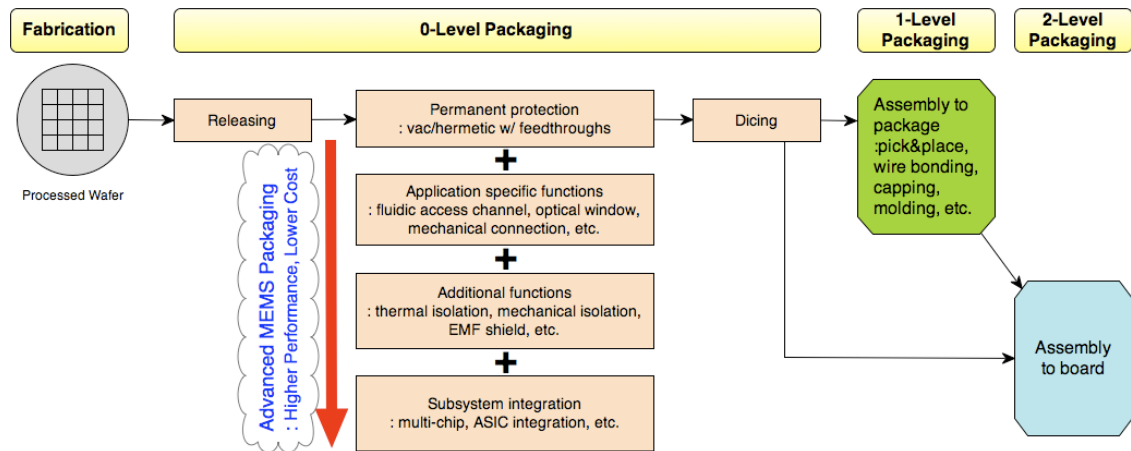


Figure 1.5 Advanced MEMS packaging technology.

1.1.3 MEMS Packaging Requirements

As MEMS and its packaging industry grow, more requirements need to be carefully considered at the beginning of the process including process integration issues and final package specifications. As mentioned before, the latest trend in developing MEMS packaging is adding more options during the lower-level processes (Figure 1.5). Key technological requirements to realize this movement have been summarized in Table 1.4 [8]. These key requirements should be considered at the early stage of developing a MEMS device or system, because they are correlated to the design of the MEMS device.

Table 1.4 Key technological requirements in packaging microsystems [8].

Category		Requirements
General	<ul style="list-style-type: none"> - Long-term stability - Uniformity - Low cost 	<ul style="list-style-type: none"> - Reliability - Reproducibility
<i>Encapsulation /Protection</i>	<ul style="list-style-type: none"> - Wafer-level process - Hermetic or vacuum-sealed - Corrosion resistant - Media compatible - Selective exposure to environments or measurands 	Generic or Standardized Approach
<i>Connection</i>	<ul style="list-style-type: none"> - Electrical/Fluidic/Optical - Sealed/Buffered feedthroughs - Low parasitics (R, C, L) - Small - Re-configurable 	
<i>Assembly</i>	<ul style="list-style-type: none"> - Modularized and batch process - Re-configurable - Reusable - Removable 	

Generally, the package requires long-term stability, reliability, uniformity, reproducibility and cost-effectiveness. In addition to these basic requirements, the MEMS packaging technology should include several necessities in three major technological categories: encapsulation/protection, connection, and assembly.

Encapsulation of the delicate and fragile microstructures is not only for protection during the post processes such as cleaning and dicing, but also for protection during their stable operation. This permanent protection should be done at the wafer-level, and provide proper operational environments. Suitable selective access channels also need to be provided for the MEMS devices to interact with the environment and measurands.

Connections between the MEMS device and outside world are another challenge. These connections need to deliver not only electrical signals but also other measurands. It is also desirable for these connections to be small and have low parasitics.

The MEMS device needs to be assembled into the package seamlessly. Assembling the device in a batch or modular approach allows for compact multi-chip packaging. Conventional hybrid approaches, which require wire bonding, can be substituted.

Furthermore, generic or standardized approach is another desirable feature in developing the advanced MEMS packaging. As mentioned earlier, one of the key issues in the MEMS packaging area is the manufacturing cost, which may reach more than half of the total manufacturing cost [18-20]; this packaging cost generally increases as the performance level of the device is increased. This high cost primarily comes from the non-standard nature of MEMS packaging. Inherent application-dependent requirements of MEMS packaging result in customized packaging solutions that are only compatible with certain processes. Generic MEMS packaging technology allows for fast lead-time in modifying and developing the MEMS, and results in reducing the whole manufacturing cost.

Therefore, developing a generic/standard packaging platform, which can provide additional options and functions that can be applied to a wide range of MEMS devices is essential.

1.2 Environment-Resistant MEMS Package

The objective of this research is to develop a new generic wafer-level packaging technology that can be applied to a wide range of MEMS devices with environmental resistance. This technology needs to satisfy many of the requirements that have been discussed in section 1.1. The packaging process needs to be done at the wafer-level. It

should provide proper environmental control and feedthroughs for the stable operation of the packaged device. It also needs to be generic, so that it permits the incorporation of a wide range of MEMS devices. To realize this generic approach, new assembly and connection technologies, which are easily re-configurable and re-usable, need to be developed.

Additional functions and values need to be incorporated during this wafer-level packaging procedure. These additional functions are intended to enhance the performance of the device, and to reduce the size and cost because these functions are incorporated at the wafer-level during lower-level packaging processes. Out of many functional options, we include components for thermal isolation and temperature control, and components for protection against mechanical vibration and shock in our work. Environmental parameters, especially temperature and vibration, can easily compromise the output of a MEMS device, and can induce undesirable long-term effects.

Figure 1.6 illustrates the conceptual view of the proposed generic environment-resistant package.

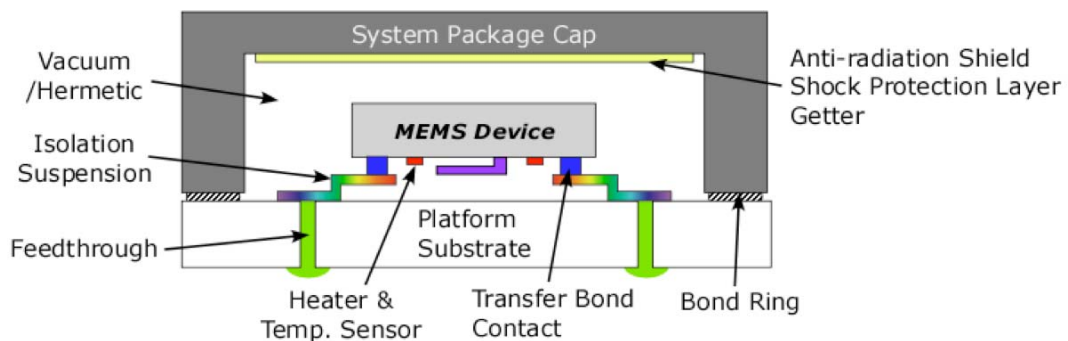


Figure 1.6 Illustration of the generic environment-resistant package concept.

The package consists of a platform substrate where the MEMS device is located and an encapsulating cap substrate. Feedthroughs for signal transfer to the external world

are implemented in the package. These two package substrates are fabricated at the wafer-level, and the MEMS device is batch assembled on the isolation platform, which is supported by suspensions. These isolation suspensions provide signal paths and additional functions including thermal isolation and vibration isolation.

Thermal stability during the operation of the device can be provided by oven-controlling the device at a certain temperature, which is higher than the maximum external temperature. Low power oven control can be realized using an integrated heater, temperature sensor and the isolation suspension with high thermal resistance. Mechanical disturbances also can be filtered out by suspending the device using the isolation suspensions. Mechanical isolation is provided through two elements: isolation suspensions that damp out the low level and higher frequency vibration signals, and shock absorption layers that cushion the device during high g shocks.

This approach results in the development of a modular technology that permits the incorporation of MEMS devices, such as gyroscopes and accelerometers, into a miniature housing. Note that in this implementation, the MEMS chip is fabricated on a separate substrate, is then mounted on the platform substrate, and is capped on top with a vacuum package cap.

This environment-resistant package and its design are categorized into five key technical areas – thermal isolation, mechanical isolation, device transfer, vacuum packaging, and feedthrough formation. Each of these key technical challenges will be discussed in Chapter 2.

1.3 Contributions

This research makes several important contributions, including:

- Wafer-level power-efficient environmental isolation packaging technology.
- Design, analysis, and development of micromachined suspensions for optimum thermal, mechanical, and electrical performance.
- Generic MEMS device flip-chip transfer/assembly technique.
- Wafer bonding technology for wafer-level vacuum packaging.
- Multi-level chip- and wafer-level bonding technology.
- Vertical feedthrough technology.
- Packaging and operation of a high performance inertial-grade gyroscope.

1.4 Thesis Organization

Chapter 2 will give a review of the relevant key technologies to realize the wafer-level environment-resistant packaging technology. Design and fabrication issues and solutions are reviewed. Chapter 3 presents design and fabrication results of the new packaging technology using meandering suspensions made out of metal. Chapter 4 presents a packaging technology using thin glass suspensions. Actual devices including thermal test chips, Pirani gauges and gyroscopes have been packaged and tested using this technology. Chapter 5 details a modified packaging technology presented in Chapter 4. Low-power oven-controlled operation of the packaged gyroscopes has been demonstrated. Finally, Chapter 6 concludes the thesis and suggests future works.

Chapter 2

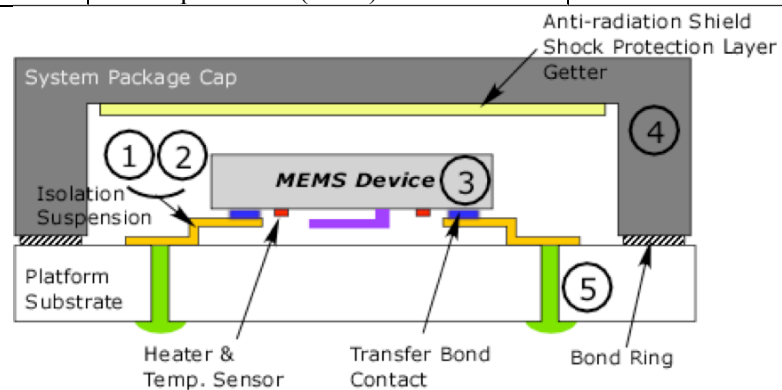
Development of Key Technologies for the Environment-Resistant Package

The objective of this new packaging approach is to provide a generic wafer-level package with additional functionalities for environment-resistant microsystems. To realize this, several key technologies should be developed as shown in Table 2.1. It should be noted that these technologies are not stand-alone but correlated to each other. Therefore, all requirements should be considered in deciding a solution in each area.

In this chapter, these key technologies and their challenges will be discussed. In sections 2.1 and 2.2, analytical models for thermal and mechanical isolation will be discussed. MEMS device integration techniques will then be introduced in section 2.3, and followed by wafer-level vacuum packaging technologies in section 2.4. Finally, feedthrough technologies for signal transfer will be presented in section 2.5. Related background will also be reviewed before presenting each of these technologies.

Table 2.1 Key challenges in environment-resistant package.

Section	Key Challenges	Objectives	Approach
2.1	Thermal isolation	<ul style="list-style-type: none"> - High performance - Low power oven-control (-50 °C to +70 °C at 80 °C and >13,000 K/W for <10 mW power) 	<ul style="list-style-type: none"> - Suspended device using isolation suspensions with high thermal resistance. - Vacuum package - Anti-radiation shield - Integrated heater and temp. sensor
2.2	Mechanical isolation	<ul style="list-style-type: none"> - High performance - Robustness - Vibration (>1kHz) and shock (20,000 g) isolation 	<ul style="list-style-type: none"> - Vibration isolation using isolation suspension - Shock stop, shock absorption layer
2.3	Device integration	<ul style="list-style-type: none"> - Low cost - Batch process - Accurate alignment (<25 μm) - High temperature stability (>400 °C) 	<ul style="list-style-type: none"> - Generic device integration
2.4	Wafer-level vacuum package	<ul style="list-style-type: none"> - Low cost - High stability - High vacuum (<10 mTorr with <1 mTorr/yr leak) - High uniformity - Low process temperature (<400 °C) 	<ul style="list-style-type: none"> - Wafer bonding - Getter
2.5	Feedthroughs	<ul style="list-style-type: none"> - Low cost - Small footprint with >16 feedthroughs - Low parasitics (<2 Ω) 	<ul style="list-style-type: none"> - Vertical feedthroughs



2.1 Thermal Isolation

2.1.1 Thermal Resistance of the Environment-Resistant Package

External temperature can easily corrupt the output of a microinstrument, and can induce long-term undesirable effects that are not correctable using electronics. The performance of precision MEMS instruments such as inertial sensors [21, 22], resonators [23], pressure sensors [24], and IR sensors [25] is affected by external temperature change. For example, thermal expansion or thermal mismatch induces material stiffness change and causes temperature drift [26]. Therefore, the thermal stability of a MEMS device is one of critical issues in the MEMS industry.

Table 2.2 Temperature stabilization techniques in MEMS.

	Application	Technology	Ref.
Passive	RF MEM Capacitor	Geometrical design optimization	[27]
	Resonator	Composite material	[28]
	Resonator	Geometrical design optimization	[29]
Active	Resonator	Oven-control	[23] [30] [31]
	Gas sensor	Oven-control	[32]
	Pressure sensor	Circuitry	[24]
	Resonator	Mode comparison	[33]
	Oscillator	Electronic circuitry	[34]
	Pressure sensor	Oven-control	[35]
	Accelerometer	Oven-control	[36]

Thermally-induced performance variations in microsystems can be mitigated by passive or active temperature compensation. Table 2.2 shows several examples of the temperature stabilization techniques used in microsystems. The passive temperature

stabilization techniques utilize optimized designs [27, 29] or suitable materials [28], which have little dependency on the ambient temperature. However, using these techniques, the temperature stability could compromise other aspects of device performance. The active techniques, therefore, have the potential to give more reliable temperature stability but require consumption of additional power.

Among the active techniques, the oven-control technique is most widely used. This technique provides a MEMS device with a constant temperature by heating up or cooling down the device to a certain fixed temperature. The device temperature is then servo-controlled using a heater (or cooler), temperature sensor and control circuitry. The advantage of this technique is that it excludes the original source of the performance drifts. Therefore, it assures the controlled device of an invariable environment, no matter what mechanism is involved in the performance instability from the ambient temperature change.

Heating a MEMS device is generally a more power-efficient way than cooling, although in certain applications, MEMS devices show better performance at lower temperatures [21]. However, oven controlling by cooling requires a larger input power than that by heating because of thermodynamic entropy loss of the system. Device heating is achieved by simply integrating a heater into the package.

It is critical that the oven-controlled device be thermally isolated from the environment to minimize the necessary input power. Unless the device is thermally isolated, the heat from the device will be directly conveyed and dissipated to the environment. In that case, the necessary power to heat the device can become very large, or the device may be unable to reach a desired temperature with acceptable input power.

An early commercial application that employed thermal isolation was a diode detector in a high-bandwidth frequency synthesizer produced by Hewlett-Packard [37]. Thermally-isolated structures have been extensively used in many other MEMS applications, such as infrared detectors [38], gas chromatography [39], and thermal accelerometers [40, 41]. In these applications, isolation of the thermal structure has been used to isolate it from an external heat sink. This is often achieved by bulk micromachining a silicon substrate, or alternately by surface micromachining utilizing a thin film sacrificial layer.

Thermal isolation can be quantified by analyzing the thermal resistance, R_{th} , of a given thermal path between the device and the ambient. Just as an electrical resistance is associated with the flow of electricity, thermal resistance is associated with the flow of heat. A general definition of the resistance of the thermal path is the ratio between the temperature increase above the reference, ΔT , and the heat flow rate, q , given by [42]

$$R_{th} = \frac{\Delta T}{q} = \frac{T_{device} - T_{surrounding}}{q} \quad (2.1)$$

A high thermal resistance is required to minimize power dissipation for heating. For example, when the device is maintained at 80 °C and the operating temperature is -50 °C ($\Delta T=130$ °C), then >13,000 K/W of thermal resistance is required to reduce the necessary input power to <10 mW.

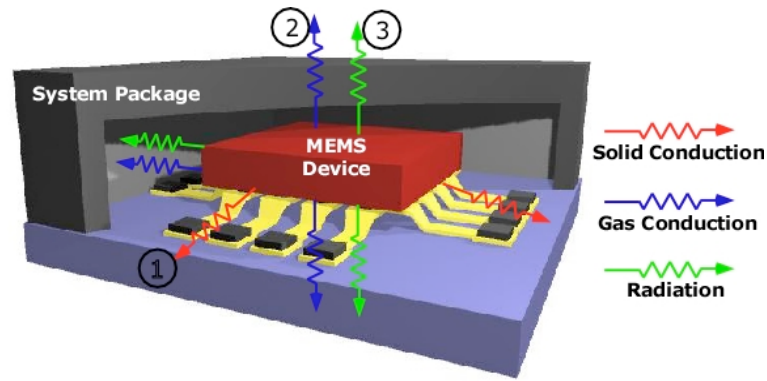


Figure 2.1 Major heat dissipation modes: (1) solid conduction, (2) gas conduction, and (3) radiation.

To increase the total thermal resistance in the system, three major heat transfer modes should be controlled: conduction, convection and radiation. In a micro-scale vacuum package, the convection is negligible, and the conduction can be categorized into two types: solid conduction and gas conduction. Figure 2.1 illustrates how heat is lost through radiation and these two types of conduction.

2.1.2 Heat Dissipation in Micro-package

2.1.2.1 Solid Conduction

Solid conduction

Solid conduction involves heat transfer by atomic interactions in the form of lattice vibrations, and can be quantified in terms of a rate equation known as Fourier's law and equivalent thermal circuit analysis as mentioned earlier [42]. For a one-dimensional plane wall having a temperature distribution, the rate equation is expressed as:

$$q''_{sol} = -k_{sol} \frac{dT}{dx} \quad (2.2)$$

The heat flux, q'' (W/m^2) is the heat transfer rate per unit area perpendicular to the direction of transfer, and it is proportional to the temperature gradient, dT/dx , in this direction. The proportionality constant, k_{sol} , is the thermal conductivity (W/mK), and is a material property.

Under steady state conditions, the heat flux is expressed as:

$$q''_{sol} = -k_{sol} \frac{\Delta T}{L} \quad (2.3)$$

The heat flow rate, q_{sol} (W), through a plane wall (or beam) with cross-sectional area A and length L can be expressed as:

$$q_{sol} = q''_{sol} A = -k_{sol} \Delta T \frac{A}{L} \quad (2.4)$$

Given Equation 2.4, the thermal resistance for solid conduction in a plane beam can be expressed as

$$R_{th,sol} \equiv \frac{\Delta T}{q_{sol}} = \frac{1}{k_{sol}} \frac{L}{A} \quad (2.5)$$

Isolation suspension

The environment-resistant package is designed to suspend the MEMS device using support suspensions (also called isolation suspensions) in order to thermally isolate the device. Using standard die attach methods, the heat from the oven-controlled device

will be directly conveyed to the package (heat sink), which is also thermally connected to the environment. In that case, the power consumption for oven-control can become very large, or the device may not be able to reach a desired temperature with reasonable input power. Therefore, the device should be suspended to minimize any contact area between the device and the package. Then the suspension is the only heat dissipation path by solid conduction, and it should be designed to have high thermal resistance.

2.1.2.2 Gas Conduction

Gas conduction modes

Gas conduction involves heat transfer through gas molecules, and its modeling at relatively high pressures (molar regime, *Maxwell* region) is distinct from that at relatively low pressures (molecular regime, *Knudsen* region) [43]. At relatively high pressures, the heat conductivity of gases is independent of the pressure. However, at relatively low pressures, the heat conductivity is a function of pressure as shown in Figure 2.2. The area between these two regions is called transmolecular or transient region.

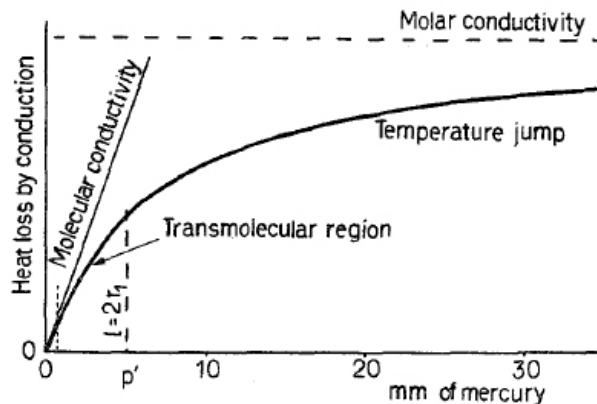


Figure 2.2 Heat loss in air of a 0.01 mm wire placed inside a wide tube. At p' , the mean free path equals the diameter of the wire [44].

The interface between these two regimes can be determined using Knudsen

number, which is given by the ratio of the mean free path of the molecules, λ , to a characteristic dimension of the package which contains the gas molecules, d . In case of MEMS, the dimension of the package cavity is from microns to millimeters.

$$K_n = \frac{\lambda}{d} \quad (2.6)$$

Gas conduction in molar regime: $K_n \ll 0.01$

At high pressures, heat transfer behavior is characterized by intermolecular collisions of the gases, because the mean free path is small ($<0.2 \mu\text{m}$) as compared to the dimension of package. The thermal conductivity of gas, k_{gas} , is then independent of the pressure, and similar expressions used for solid conduction can be applied for the one-dimensional analysis:

$$R_{th, gas} = \frac{1}{k_{gas}} \frac{L}{A} \quad (2.7)$$

Table 2.3 Thermal conductivity, k_{gas} (W/mK), for some gases at $T = 0 \text{ }^\circ\text{C}$ [43].

Monatomic		Diatomic	
He	1.44×10^{-1}	H ₂	1.75×10^{-1}
Ar	1.63×10^{-2}	N ₂	2.39×10^{-2}
Kr	8.79×10^{-3}	O ₂	2.43×10^{-2}
Ne	4.56×10^{-2}	CO	2.22×10^{-2}
Hg	5.02×10^{-3}	Air	2.43×10^{-2}
Polyatomic		CO ₂	1.42×10^{-2}

Gas conduction in molecular regime: $K_n \gg 1$

At low pressures, the mean free path of gas molecules is much larger (i.e., ~1 mm at 75 mTorr / 25 °C) than the package that accommodates the gas. So the transport energy from the oven controlled device to the enclosing package wall does not include intermolecular collisions as shown in Figure 2.3.

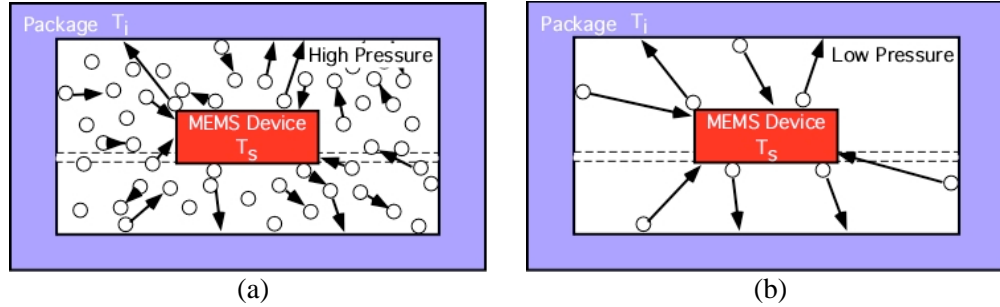


Figure 2.3 Schematic illustration of gas conduction mechanism at (a) high pressures, and (b) low pressures.

When a gas molecule, originally at T_i , strikes a hot surface (T_s), complete interchange of energy does not occur at the first collision. In fact, it may often require many collisions for this to occur. Knudsen showed that the increase in molecular temperature is directly proportional to the temperature difference between the surface and the incident molecules [45]. This process of heat transfer is characterized by the *accommodation coefficient*, α .

$$\alpha = \frac{T_r - T_i}{T_s - T_i} \leq 1 \quad (2.8)$$

where T_r is the temperature of the reflected gas molecules, T_i is the temperature of the incident gas molecules, and T_s is the temperature of the surface. We should note that T_r is not clearly defined unless the molecules leaving the surface have a *Maxwellian* distribution of velocities.

Considering heat transfer in monoatomic gases at low pressure, the energy acquired by the monoatomic molecules from a hot surface (T_s) to a cold surface (T_i) per unit area of the hot surface, per unit time can be expressed as [43]:

$$q''_{gas,mono} = \frac{\alpha}{2} \cdot \frac{pv_i}{T_i} (T_s - T_i) \quad (2.9)$$

where v_i is the average velocity at T_i .

For diatomic and polyatomic gases, translation energy, rotational energy and vibrational energy of the gas molecules need to be considered. A detailed calculation leads, in these cases, to the relation [43]:

$$q''_{gas,poly} = \alpha_s \Lambda_0 p \left(\frac{273.2}{T_i} \right)^{1/2} (T_s - T_i) \quad (2.10)$$

where $\alpha_s = (\alpha_1 \alpha_2) / (\alpha_1 + \alpha_2 - \alpha_1 \alpha_2)$, and α_1, α_2 are the accommodation coefficients for the hot and cold surfaces, respectively, and where Λ_0 is the *free molecular conductivity* at 0 °C. It should be noted that the rate of energy transfer at low pressure is proportional to the pressure. As mentioned earlier, this is not the case at relatively high pressures. Table 2.4 shows values of the molecular free conductivity, Λ_0 , measured for some gases.

Table 2.4 Values of molecular heat conductivity [43].

Gas	Λ_0 [$Wm^{-2}K^{-1}mTorr^{-1}$]	Gas	Λ_0 [$Wm^{-2}K^{-1}mTorr^{-1}$]
H ₂	60.72×10^{-2}	He	29.35×10^{-2}
H ₂ O	26.49×10^{-2}	Ne	13.07×10^{-2}
N ₂	16.63×10^{-2}	O ₂	15.57×10^{-2}
Ar	9.29×10^{-2}	CO ₂	16.96×10^{-2}

The thermal resistance at low pressure can be obtained by substituting Equation 2.9 or 2.10 into Equation 2.5.

Vacuum packaging and gas conduction

The heat loss through gas conduction is large for most MEMS device packaged at atmospheric pressure. As mentioned earlier, gas conduction at relatively high pressures is not dependant on the pressure level within the package. Figure 2.4 shows the thermal resistance of gas conduction at atmospheric pressure as a function of the packaged device size. It is assumed that the thickness of the packaged device is 0.5 mm, and its width and length is same (Figure 2.4 (a)). The gap between the device and the package wall (heat sink) is assumed 150 μm . As the device size increases, the thermal resistance due to gas conduction decreases dramatically. Even with Ar gas, which has one of the lowest gas conductivities, a thermal resistance of only 2250 K/W is achieved when the packaged device size is $1 \times 1 \times 0.5 \text{ mm}^3$ ($d = 1 \text{ mm}$). Because there are additional heat loss mechanisms, including solid conduction and radiation, the total thermal resistance is less than this value.

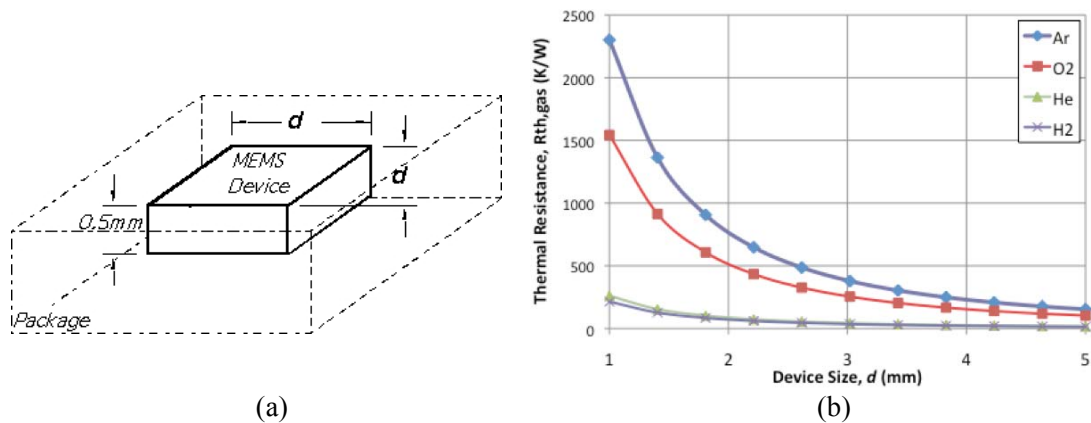


Figure 2.4 (a) Definition of a device size in the environment-resistant package. The thickness of the device is assumed 0.5mm. (b) Thermal resistance of gas conduction at atmospheric pressure and at 0 °C. The gap between the device and package wall is assumed 150 μm .

Therefore, to increase the thermal resistance due to gas conduction, vacuum packaging is essential. Figure 2.5 shows the thermal resistance due to gas conduction

when the device is vacuum packaged. It is assumed that the environment temperature is 0 °C, and the accommodation coefficient is 0.9. As mentioned earlier, the thermal resistance is a function of the pressure level and the device size. As illustrated in Figure 2.5 (a), given a $1 \times 1 \times 0.5 \text{ mm}^3$ device, at 10 mTorr (Ar), the thermal resistance is $> 250,000 \text{ K/W}$, which is 100 times larger than that at atmospheric pressure.

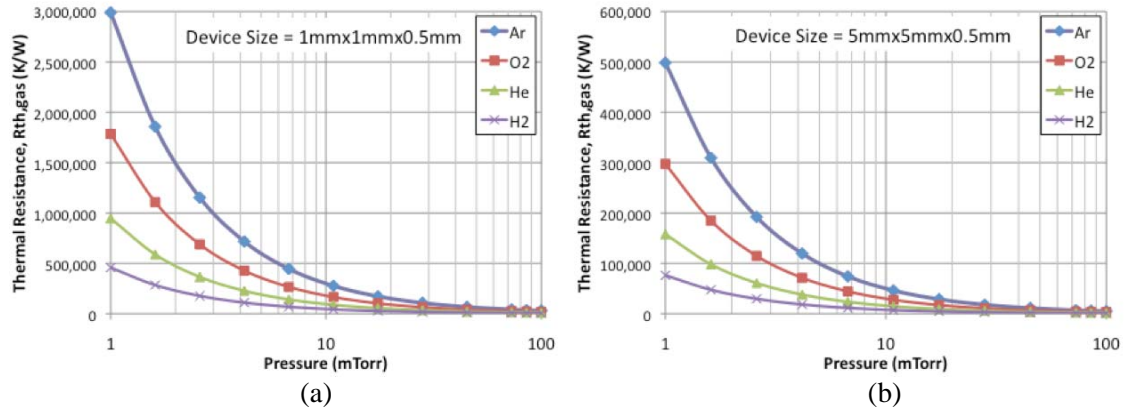


Figure 2.5 Thermal resistance of gas conduction in a vacuum package at 0 °C. It is a function of pressure and device size. The accommodation coefficient, α , is assumed 0.9.

2.1.2.3 Radiation

Radiation

Thermal radiation is an important heat dissipation mechanism especially in vacuum environment. Radiation is energy emitted by matter that is at a finite temperature in the form of electromagnetic waves. Unlike conduction and convection, radiation does not require the presence of a material medium. Although this energy emission occurs from both solid surfaces and gases, the radiation emitted from gases can be neglected in vacuum [42].

The heat flux emitted by a solid surface is prescribed by the *Stefan-Boltzmann law* and the *emissivity*, ϵ .

$$q''_{rad} = \epsilon\sigma T_s^4 \quad (2.12)$$

where ϵ is the *emissivity*, σ is the *Stefan-Boltzmann constant* ($\sigma = 5.56 \times 10^{-8} \text{ W/m}^2\text{K}^4$), and T_s is the absolute temperature of the surface. The emissivity is a radiative property of the surface with values in the range $0 \leq \epsilon \leq 1$, and provides a measure of how efficiently a surface emits energy relative to a blackbody.

Radiation shields

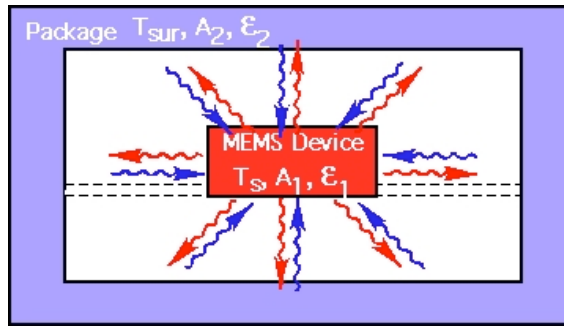


Figure 2.6 Radiation in environment-resistant package.

In an oven-controlled package, the packaged device is enclosed by a closely spaced, isothermal surface (T_{sur}) as shown in Figure 2.6. Since there are only two surfaces, the net rate of radiation transfer from the device surface is equal to the net rate of radiation transfer to the surrounding surface. The net radiation exchange between the surfaces can be expressed as [42]:

$$q_{rad} = \frac{\sigma(T_s^4 - T_{sur}^4)}{\frac{1 - \epsilon_1}{\epsilon_1 A_1} + \frac{1}{A_1 F_{12}} + \frac{1 - \epsilon_2}{\epsilon_2 A_2}} \quad (2.13)$$

where F_{12} is the view factor which is the fraction of the radiation leaving surface 1 that is taken by surface 2, and it can be assumed to be $F_{12} = 1$ when the two surfaces are closely spaced. Opaque, diffuse and gray surface behavior is also assumed, and the gas molecules within the enclosure are assumed not to affect this energy exchange.

The thermal resistance of thermal radiation loss between two surfaces is given by:

$$R_{th,rad} = \frac{\Delta T}{q_{rad}} = \frac{(\epsilon_1^{-1} + \epsilon_2^{-1} - 1)}{\sigma(T_s + T_{sur})(T_s^2 - T_{sur}^2)A} \quad (2.14)$$

where $A_1=A_2=A$ and $F_{12} = 1$ [42]. Heat loss by thermal radiation become important as the size (surface area) of the oven-controlled device gets large as shown in Figure 2.7.

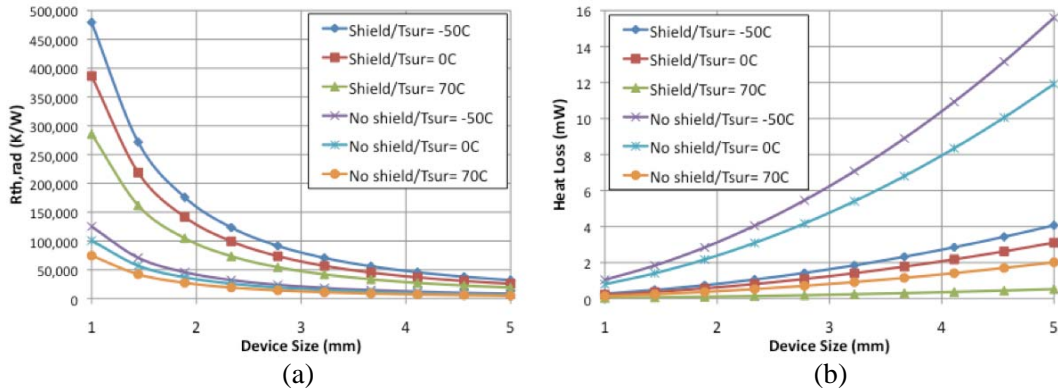


Figure 2.7 (a) Thermal resistance and (b) heat loss by radiation with varying the packaged die size in the environment-resistant package. The emissivity of the shield material is assumed 0.1.

It should be noted that heat loss by radiation could be reduced by using radiation shields with low emissivity (high reflectivity) materials. The emissivity of the device surface (silicon) is 0.52.

2.1.3 Thermal Isolation Package Design

2.1.3.1 Summary of Thermal Isolation Design

Table 2.5 summarizes the three thermal mechanisms considered in designing the package. To achieve a low power oven-controlled package, high thermal resistance in each heat loss mode is necessary.

Table 2.5 Summary of variables for each thermal mode.

Thermal Mode	Thermal Resistance (R_{th})	Variables
Solid conduction	$R_{th,sol} = \frac{1}{k_{sol}} \frac{L}{\bar{A}}$	<ul style="list-style-type: none"> • Suspension material (k_{sol}) • Suspension design (L, \bar{A})
Gas conduction	$R_{th,gas} = \left(\alpha_s \Lambda_0 P \left(\frac{273.2}{T_i} \right)^{1/2} A \right)^{-1}$	<ul style="list-style-type: none"> • Pressure (p) • Device size (A) • Environment temperature (T_i)
Radiation	$R_{th,rad} = \frac{(\epsilon_1^{-1} + \epsilon_2^{-1} - 1)}{\sigma(T_s + T_{sur})(T_s^2 - T_{sur}^2)} A$	<ul style="list-style-type: none"> • Surface properties (ϵ_1, ϵ_2) • Device size (A) • Environment temperature (T_i) • Oven-control temperature (T_s)

Figure 2.8 shows the proposed approaches to increase the thermal resistance in each mode. First, solid conduction can be controlled by suspending the heated element using suitable isolation suspensions. A wafer-level vacuum encapsulation can minimize heat loss by gas conduction. Finally, a radiation shield using high reflective material is a possible solution to increase the thermal resistance due to radiation.

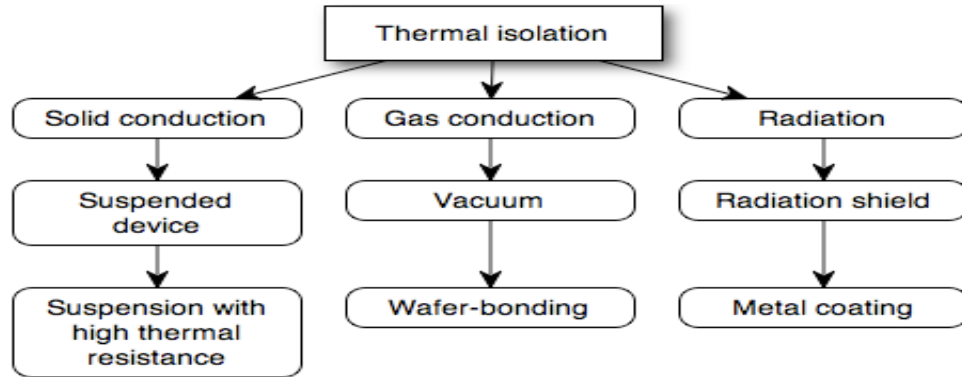
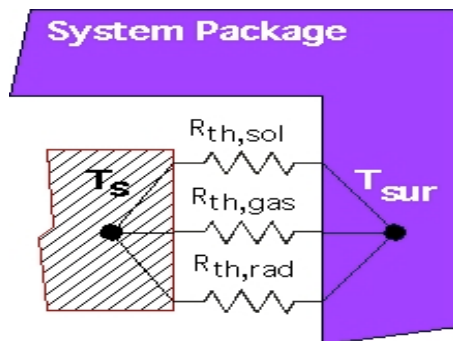


Figure 2.8 Key approaches to achieve thermal isolation in environment-resistant package.

2.1.3.2 Design Strategy

The total thermal resistance of the package can be modeled by a lumped circuit model as shown in Figure 2.9 and Equation 2.15. All the heat loss paths are linked in parallel from the heated element (heat source) to the external package (heat sink). Before designing the package, we should determine the package specifications such as device size, external package size, and target power consumption.



$$\begin{aligned}
 R_{th,total} &= R_{th,sol} \parallel R_{th,gas} \parallel R_{th,rad} \\
 G_{th,total} &= G_{th,sol} + G_{th,gas} + G_{th,rad}
 \end{aligned}
 \tag{2.15}$$

Figure 2.9 A lumped thermal circuit model for the environment-resistant package.

Figure 2.10 shows the design procedure for the thermally isolated package. The main procedure involves apportioning each thermal loss mechanism a limited thermal budget (maximum power consumption). First, package specifications need to be decided.

These specifications can be categorized into two types: first, *operation specification* including operating temperature, target power consumption and required pressure level inside the package, and second, *device specification* including device size, number of feedthroughs, and device materials. Once the two specifications are determined, the thermal resistance due to gas conduction and radiation is determined, because these values are a function of pressure, material properties, and device size. Finally, the thermal resistance due to solid conduction is determined. It should be noted that the thermal resistance due to solid conduction is solely determined by the isolation suspension design.

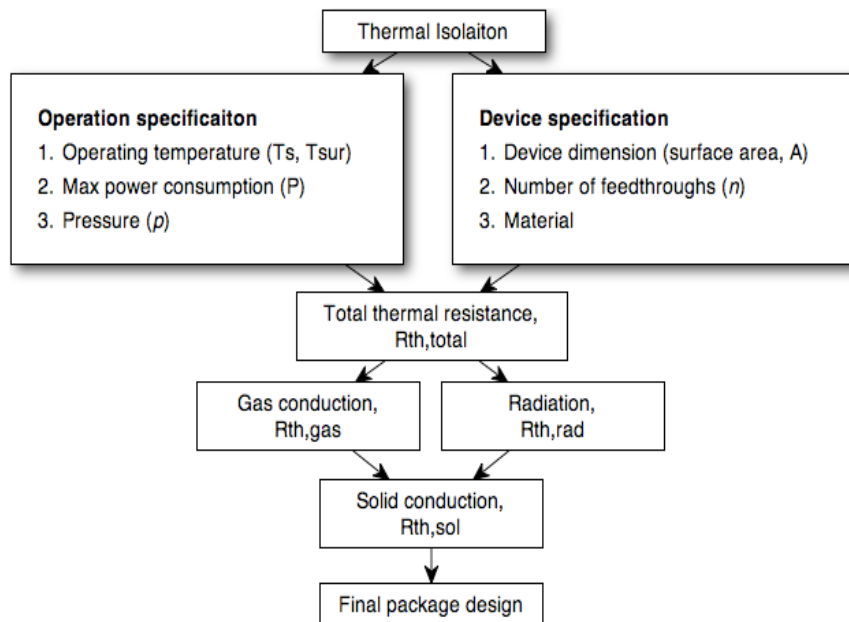


Figure 2.10 Design procedure for thermally isolated package.

Figure 2.11 shows simulation results of the thermal resistance and the heat loss by gas conduction and radiation with varying device size. The thermal resistance or heat loss from solid conduction can be obtained from the total thermal budget. The thermal budget signifies the minimum total thermal resistance (or maximum total heat loss)

needed to satisfy target power consumption. The package design needs to be optimized in order to properly distribute the thermal budget through the three heat loss modes. For example, if the device size is $3 \times 3 \times 0.5 \text{ mm}^3$, the power dissipated through the gas conduction and radiation is 6.5 mW (Figure 2.11 (b)). We then have room of 3.5 mW for the heat loss through solid conduction if the total thermal budget is 10 mW. The assumptions for this simulation data are: an accommodation coefficient, $\alpha=0.9$ (O_2); a pressure, $p = 10\text{mTorr}$; a gap between the device and package = $150 \text{ }\mu\text{m}$; a device temperature, $T_s = 80 \text{ }^\circ\text{C}$; and a surrounding temperature, $T_{\text{sur}} = -50 \text{ }^\circ\text{C}$.

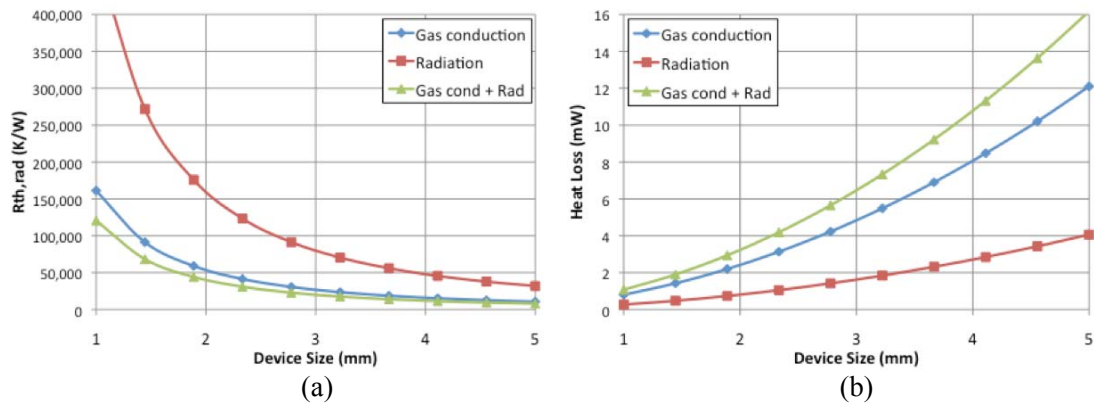


Figure 2.11 (a) Thermal resistance and (b) heat loss of gas conduction and radiation. The thermal resistance or heat loss of solid conduction can be obtained from the total thermal budget. Assumption: $\alpha=0.9$, O_2 , $p=10\text{mTorr}$, gap btw device and package= $150 \text{ }\mu\text{m}$, $T_s=80 \text{ }^\circ\text{C}$, and $T_{\text{sur}}=-50 \text{ }^\circ\text{C}$.

Given the total thermal resistance and heat loss through gas conduction and radiation, Figure 2.12 shows the minimum necessary thermal resistance and resultant heat loss through solid conduction for two different thermal budgets. For example, if the device size is $3 \times 3 \times 0.5 \text{ mm}^3$, 6.5 mW of power is dissipated by gas conduction and radiation (Figure 2.11 (b)). Then we have room for 3.5 mW of heat loss by solid conduction if the total thermal budget is 10 mW (Figure 2.12 (b)). However, if the device size is larger than $3.7 \times 3.7 \times 0.5 \text{ mm}^3$ and thermal budget is 10 mW, then there is no

way to satisfy the thermal budget because more than 10 mW of power is already dissipated through gas conduction and radiation.

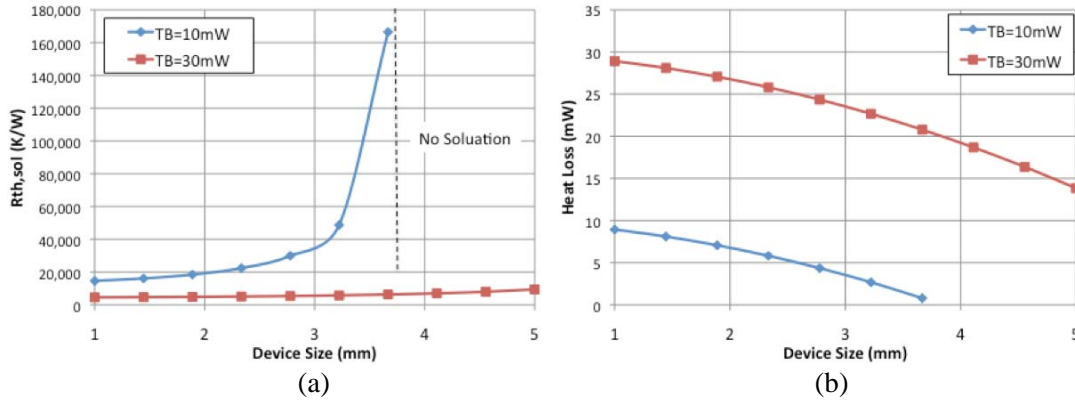


Figure 2.12 (a) Minimum necessary thermal resistance and (b) heat loss through solid conduction under the total thermal budget (TB) of 10 mW and 30 mW. In TB= 10 mW case, there is no budget left for solid conduction when the device size is larger than $3.7 \times 3.7 \times 0.5 \text{ mm}^3$, because the heat loss by gas conduction and radiation is already larger than 10 mW.

Figure 2.13 shows the portion of the heat loss for each heat loss mode. As the device size increases, the heat loss through gas conduction becomes dominant. Therefore, the high vacuum environment is critical for minimizing the total heat loss.

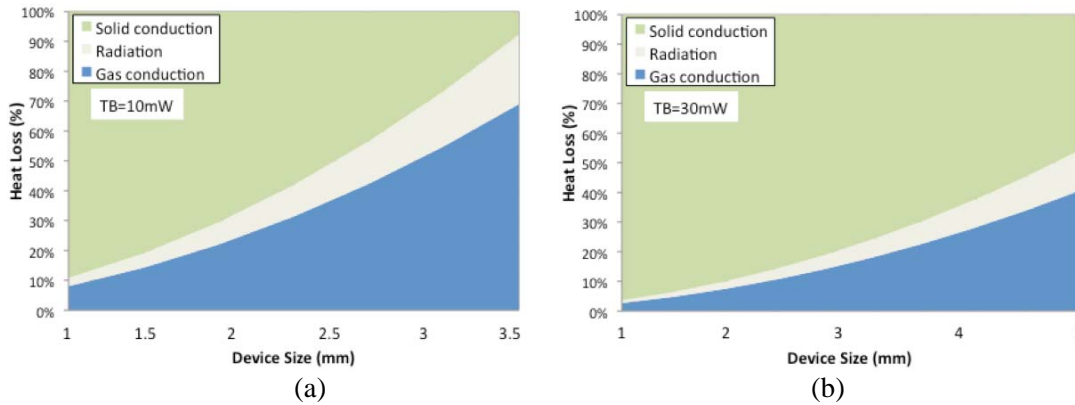


Figure 2.13 Percentage contribution of each heat loss modes under thermal budget (TB) of (a) 10 mW and (b) 30 mW. As the device size becomes large, gas conduction and radiation become important. Assumed $\alpha=0.9$, $p=10 \text{ mTorr}$, $T_s=80 \text{ }^\circ\text{C}$, $T_{sur}=0 \text{ }^\circ\text{C}$, $\epsilon_1=0.52$, and $\epsilon_2=0.1$.

2.1.3.3 Thermal Isolation Suspensions

We have studied two types of thermal isolation suspensions. One is made of evaporated or electroplated metal, and the other is made out of thin Pyrex glass. The metal suspensions are located around the MEMS device and support the device over the substrate as shown in Figure 2.14 (a). They also provide electrical signal path and vibration isolation. To increase the thermal resistance through solid conduction, they have meandering shape. The implementation of metal isolation suspensions in the package will be described in Chapter 3.

In the second type of suspensions, crab-leg shaped thin glass beams support the MEMS device as shown in Figure 2.14 (b). The glass isolation suspensions also provide high thermal resistance and vibration isolation simultaneously. Separate interconnection lines for signal feedthrough are required because glass is not a conductive material. Detailed implementation of the glass isolation suspensions will be described in Chapter 4.

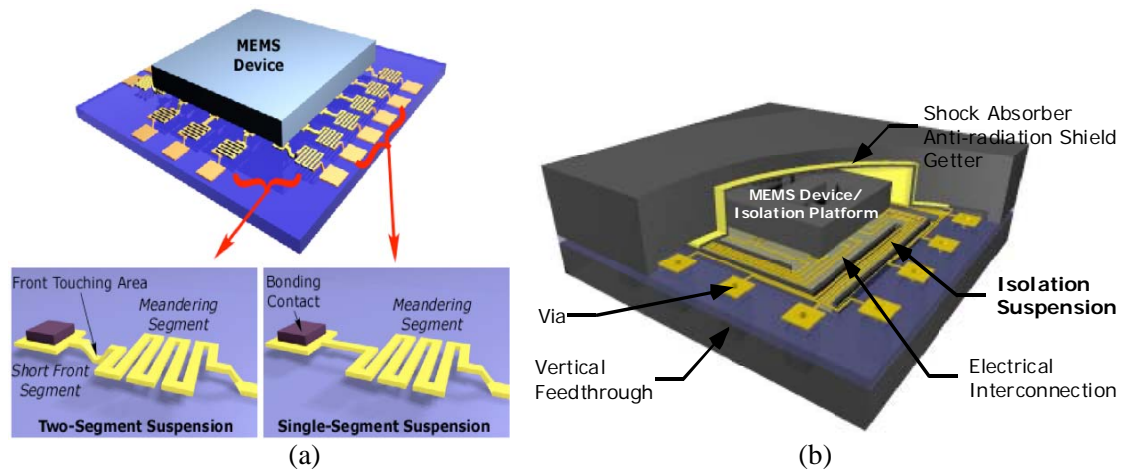


Figure 2.14 Schematic illustration of the two types of isolation suspensions. (a) Meandering metal isolation suspensions (Chapter 3), (b) Glass isolation suspensions (Chapter 4).

2.2 Mechanical Isolation

The push for higher performance and reliability of MEMS devices often requires isolating the device from external mechanical disturbances. The major sources for mechanical disturbances are vibration and shock, which may degrade device performance or ultimately damage the device structure.

2.2.1 Vibration Isolation

2.2.1.1 Vibration Isolation in MEMS

The most effective way to reduce unwanted vibration is to stop or modify the source of the vibration. However, most MEMS devices are exposed to environmental vibrations, which is usually not avoidable. Therefore, it is desirable to design a vibration isolation system to isolate the device from the source of vibration. This can be done by using highly damped materials such as suspensions to change the stiffness and damping between the source of vibration and the device that is to be protected from these vibrations. The problem of isolating a *device* from a source of vibration can be analyzed in terms of reducing the vibration *displacement* transmitted through base motion of the package (base excitation problem) [46].

Vibration from the environment or package is transferred to the packaged device through elastic suspensions, which can be modeled by springs and dampers as shown in Figure 2.15.

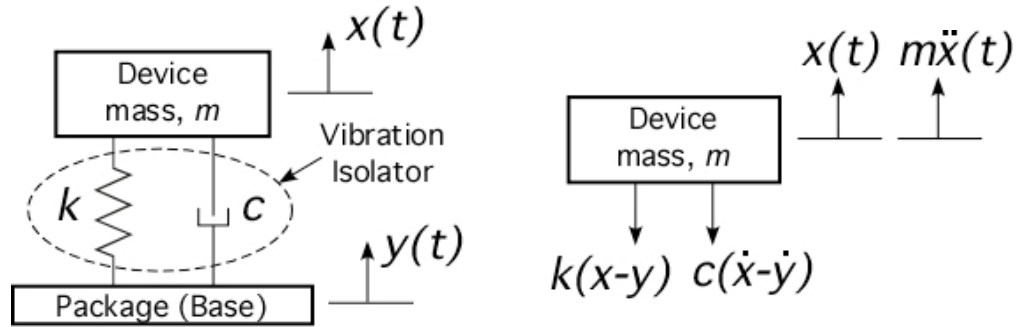


Figure 2.15 Modeling of the base excitation problem [46]. The motion of the device (mass, m) is excited by prescribed harmonic displacement of the package (base) through the spring and damper.

Summing the relevant forces on the device (mass m in Figure 2.15) yields the equation of motion:

$$m\ddot{x} + c(\dot{x} - \dot{y}) + k(x - y) = 0 \quad (2.16)$$

where c is the damping coefficient, and k is the spring constant. The inertial force $m\ddot{x}$ is equal to the sum of the two forces acting on m , and the gravitational force is balanced against the static deflection of the spring. When the base (package) moves harmonically:

$$y(t) = Y \sin \omega_b t \quad (2.17)$$

where Y denotes the amplitude of the base motion and ω_b represents the frequency of the base oscillation. Substitution of $y(t)$ into the equation of motion results in:

$$m\ddot{x} + c\dot{x} + kx = cY\omega_b \cos \omega_b t + kY \sin \omega_b t \quad (2.18)$$

Calculating the particular solution of this differential equation yields an expression of the ratio of the maximum response magnitude to the input placement magnitude which is called the *displacement transmissibility*:

$$\frac{X}{Y} = \left[\frac{1 + (2\zeta(\omega_b / \omega_n))^2}{(1 - (\omega_b / \omega_n)^2)^2 + (2\zeta(\omega_b / \omega_n))^2} \right]^{\frac{1}{2}} \quad (2.19)$$

where ζ is *damping ratio*, ω_n is the *undamped natural frequency* in rad/s. The damping ratio is defined by

$$\zeta = \frac{c}{c_{cr}} = \frac{c}{2m\omega_n} = \frac{c}{2\sqrt{km}} \quad (2.20)$$

where c_{cr} is the *critical damping coefficient*.

Equation 2.18 can be used to describe how vibration is transmitted from the environment to the device as a function of the frequency ratio ω_b / ω_n as shown in Figure 2.16. It should be noted that near $\omega_b / \omega_n = 1$, or resonance, the maximum amount of environmental motion is transferred to the device. For values $\omega_b / \omega_n > \sqrt{2}$, the displacement ratio is always less than 1, and the motion of the device will be of smaller amplitude than that of the package.

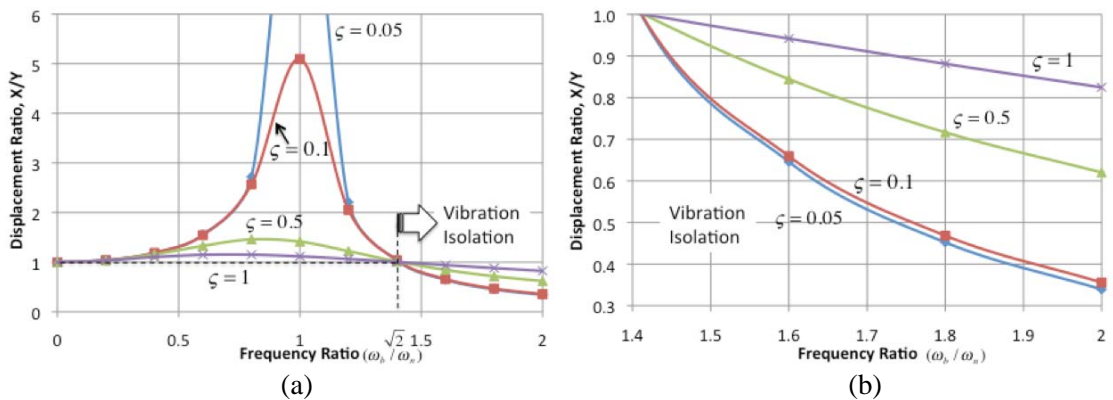


Figure 2.16 (a) Displacement transmissibility as a function of the frequency ratio. The dimensionless deflection X/Y is less than unity when the frequency ratio of the package vibration is larger than $\sqrt{2}$, where the vibration isolation occurs. (b) Magnification of the isolation area.

Another quantity of interest in the base excitation problem is the force transmitted to the device as the result of a harmonic displacement of the package. The force is also transmitted to the device through the spring and damper. Hence, the force transmitted to the mass is the sum of the force in the spring and the force in the damper. This force is balanced by the inertial force of the mass. In a similar manner to Equation 2.19, the ratio of transmitted forces, called the *force transmissibility*, can be derived:

$$\frac{F_T}{kY} = \left(\frac{\omega_b}{\omega_n} \right)^2 \left[\frac{1 + (2\zeta(\omega_b / \omega_n))^2}{(1 - (\omega_b / \omega_n)^2)^2 + (2\zeta(\omega_b / \omega_n))^2} \right]^{\frac{1}{2}} \quad (2.21)$$

where F_T is the magnitude of the transmitted force. This equation expresses how displacement of the package (Y) results in a force magnitude applied to the device as shown in Figure 2.17 (a). Unlike the displacement transmissibility, the force transmitted does not necessarily fall off for $\omega_b / \omega_n > \sqrt{2}$ as shown in Figure 2.17 (b).

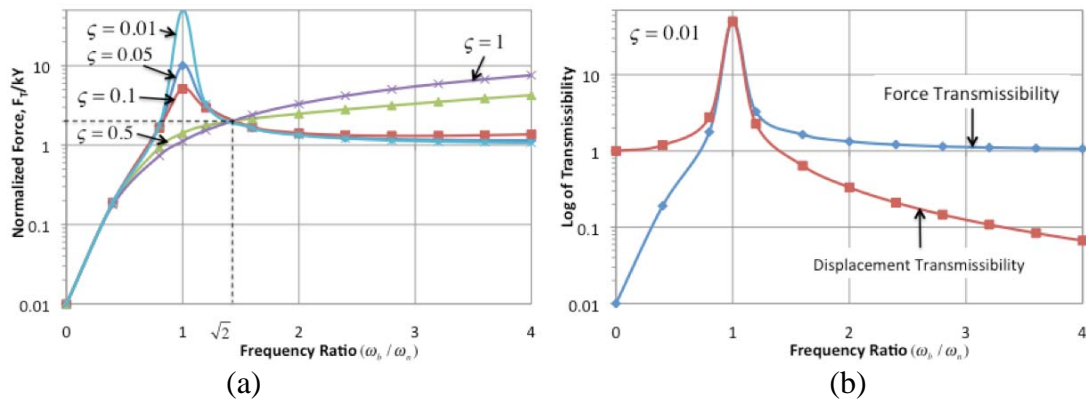


Figure 2.17 (a) Force transmissibility as a function of the frequency ratio for $\zeta = 0.01, 0.05, 0.1, 0.5$ and 1.0 . (b) A comparison between force transmissibility and displacement transmissibility for a damping ratio of $\zeta = 0.01$ on a semi-log plot.

The formulas for transmissibility of displacement and force are useful in the design of the package to provide protection from unwanted vibration.

In the environment-resistant package, vibration isolation is provided by the isolation suspension (spring) and gas molecules (damper). The damping effect from the gas molecules is negligible at vacuum [47]. In that case, the damping ratio is expected to be very small. The spring constant of the isolation suspension is then the dominant factor to be considered in designing the vibration isolator.

2.2.1.2 Vibration Isolation using Isolation Suspension

As mentioned in the previous section, we have developed metal and glass isolation suspensions. To achieve vibration isolation, the suspensions, which are used for thermal isolation, need to act as a low-pass filter. The suspensions then can reject high frequency environmental vibrations. This can be done by using long, thin, and flexible suspension. However, the suspensions should also have enough stiffness to support the MEMS device. Therefore, the suspension design should include and satisfy all requirements of high thermal resistance for thermal isolation, high stiffness for supporting the device, and high flexibility for vibration isolation. Detailed analysis on the vibration isolation can be found in Yoon's dissertation [47].

2.2.2. Shock Protection

Most MEMS devices have micro-sized free-moving or suspended structures. Although they are durable to shock because of the effects of scaling laws, environmental shock can degrade a device performance or allow a crack to form in a microstructure. This shock can be minimized by reducing the structural gap between the moving element and the stationary element. Furthermore, by adding a protectoral structure, the shock protection that the MEMS package provides can be enhanced even more.

Two possible approaches to reduce the external shock for a MEMS package have been developed by Yoon [2, 3]. The first technique is a nonlinear spring utilizing a single micro beam or a cascade of closely spaced micro beams. The compliance of these beams reduces the impulse delivered to the device as it impacts the nonlinear spring. Experimental results have demonstrated a 95 % impulse reduction through these spring stops [48].

The second shock protection technique uses a soft coating as a shock stop. Polymers such as Parylene provide significant shock protection [49]. However, polymers are not compatible with vacuum packaging due to outgassing. Instead of using polymer, a soft metal layer (i.e. gold) with a suitable thickness is also effective for shock protection. Experimental results show that gold coated around the shock stop provides 40% impulse reduction [48].

The details on this mechanical isolation are provided in Yoon's publications and dissertation [47]. These shock protection methods have been designed specifically for implementing into the environment-resistant package presented in this dissertation.

2.3 Device Transfer/Assembly Techniques

2.3.1 Device Transfer Techniques

A generic package should accommodate a wide variety of individual MEMS chips or wafers, in either a hybrid or integrated fashion. Our approach is to assemble and package MEMS devices after they are fabricated using any given process. Therefore, it is important to develop a device transfer or assembly method to realize our generic package technology.

Using our approach, a MEMS device or microstructure is fabricated on one wafer (the device wafer) and then transferred to another wafer (the platform wafer) to implement additional functionalities such as thermal isolation, vibration isolation, and a vacuum environment. This frees the MEMS designer from considering process compatibility issues between the MEMS device and the package fabrication. This is attractive for MEMS applications using special materials, which cannot be fabricated monolithically. For example, a MOEMS device can be integrated on a quartz or glass substrate to provide the optical transparency. This post-assembly technique also allows for the possibility of the separate fabrication of MEMS and CMOS while achieving performance comparable to monolithic technologies [50].

Several requirements should be considered in developing a transfer technology:

1. The transfer process should be able to handle individual MEMS chips or wafers.
2. The performance of the transferred device should not change.
3. Transfer should be done with accurate alignment.
4. A batch process is preferred.
5. The device should not be damaged during the transfer process.
6. A low temperature process is preferred.
7. The bonding contact should provide both mechanical and electrical connection.
8. The bonding contact should be stable during the post packaging process.

2.3.2 MEMS Flip-Chip Transfer Techniques

2.3.2.1 MEMS Device Transfer Methods


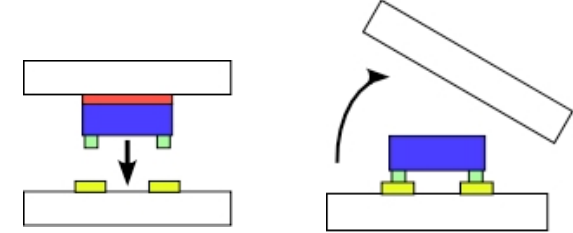
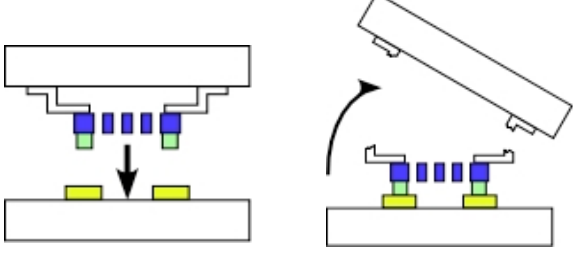
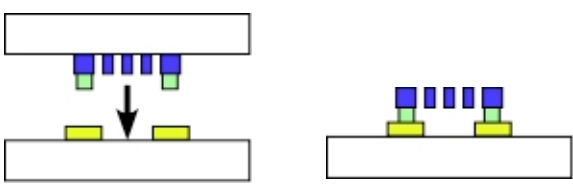
Flip-chip assembly techniques have been developed and used in many MEMS applications [51]. Flip-chip bonding involves attaching the die, top-face-down, on a substrate. Electrical and mechanical connections are made between bond pads on the die and pads on the package substrate. This attachment is intimate with relatively small spacing between the die and the substrate depending on the bonding method used. Unlike wire bonding which requires that the bond pads are positioned on the periphery of the die to avoid cross wiring, flip-chip attachment allows the placement of bond pads over the entire die resulting in either a decrease in footprint or an increase in the number of input/output connections. This is also attractive in 3-D MEMS packaging because it allows for a number of distinct closely-packed chips with multiple levels of embedded electrical traces. The flip-chip technique however may not be compatible with many MEMS with moving parts, especially in the out-of-plane direction.

There are two types of flip-chip transfer techniques as shown in Table 2.6: one is direct chip-level transfer and the other is wafer-level transfer. The chip-level transfer does not require any post process after chip assembly. However, this technique requires chip handling and alignment during transfer [52]. Flip-chip bonding using alignment pedestals has been developed to achieve high alignment accuracy [53]. Another issue with this technique is that chip-level bonding is generally a serial process.

The wafer-level approach, on the other hand, enables batch process using a wafer-to-wafer aligning and bonding process with a commercial wafer-bonding tool. However, it requires removal or separation of the device carrier wafer after bonding. Typically, the

MEMS devices or structures are fabricated on a handle wafer with adhesive layers or tethers. The handle wafer is then aligned to another substrate. After transfer bonding, the handle wafer is separated by removing the adhesive layer or breaking the tethers as illustrated in Table 2.6.

Table 2.6 MEMS device transfer techniques.

	Process	Note
Chip-level		<ul style="list-style-type: none"> - Direct chip-to-chip or chip-to-wafer bonding. - Need guiding method for chip alignment. - Ref. [52-61]
Wafer-level		<ul style="list-style-type: none"> - Separate device wafer by removing adhesive layer between device and wafer. - Ref. [62, 63]
		<ul style="list-style-type: none"> - Tether breaking tech. - Separate device wafer by breaking tethers which are supporting the device and wafer. - Ref. [41, 64-69]
		<ul style="list-style-type: none"> - Etch away the handle wafer after transfer bonding. - Selective etching of the device wafer using EDP - Ref. [62, 70, 71]

2.3.2.2 MEMS Device Transfer Bonding Methods

Careful consideration should be given in choosing a bonding method for flip-chip transfer, because it has strong effects on the packaging process and characteristics. The contacts should not degrade during post packaging processes. The bond should not crack over time and should not suffer from creep. To do this, the chip transfer bonding

processes employ metal alloys, organic, or inorganic adhesives as intermediate bonding layers. Various bonding methods have been developed for the MEMS device transfer as shown in Table 2.7. The choice of a bonding method depends on it having a suitable bonding temperature, bonding pressure, material compatibility, contact resistance, and mechanical properties.

Table 2.7 MEMS device transfer bonding techniques.

Bonding Tech.	Process	Note
Thermo-compression bonding	- Au-Au, cold welding, room temperature. - Au-Al, 200 °C.	- Clean contact surface and high bonding pressure are required. - Ref. [41, 67, 72]
Solder bonding	- Indium, cold welding, room temperature. - Indium, 156 °C. - SnPb (63/37). - Sn, 250 °C. - SnAg3.5, 250 °C. - SnPb, 350 °C.	- Low temperature process. - Re-melting issue during subsequent high temperature process. - Ref. [55-57, 66, 68, 69]
Polymer	- Conductive polymer. (Epo-Tek K/5022-115BE)	- Low temperature process. - Incompatible with vacuum packaging. - Ref. [53]
Electroplating	- Nickel electroplating	- Ref. [63]
TLP bonding	- In-Au, 300 °C. - Ni-Sn, 300 °C.	- Ref. [61, 73]
Stud bump bonding	- Au stud bump and conductive adhesive.	- Ref. [54, 55]
Mechanical joint	- Micro Velcro [74, 75] - Microrivets [76, 77] - Micro-brush [78]	- Low temperature process - Mechanical joint of two parts using micro-structure - Ref. [58, 59]

2.3.3 Generic Device Transfer Techniques

Three different wafer-level and die-level device transfer techniques have been proposed and developed in this work. The first is a wafer-level device transfer technique using wafer-level bonding and device singulation by silicon deep etching. The second

technique is a batch die-level device transfer technique using transient liquid phase (TLP) bonding. Finally a low-temperature press-on device transfer technique using a “micro-brush” has been developed.

A brief introduction of these three technologies will be presented here, and detailed results of these techniques will be presented in Chapter 3, 4 and Appendix.

2.3.3.1 Wafer-level Device Transfer Technique (Wafer Bonding and Device Isolation using DRIE)

Figure 2.18 illustrates a schematic view of the wafer-level device transfer technique. First, the bottom platform wafer and top device wafer are prepared separately. The bonding contacts are patterned on one or both sides of the wafers.

The materials chosen for the contacts depend on the chosen bonding method. For a vacuum package, outgassing issue should be considered in this material selection. Metal thermal compression bonding or TLP bonding techniques are known to have relatively low outgassing. After wafer-level bonding, the dies are separated by silicon DRIE from the backside of the device wafer. A precise timed etch is required to protect the bottom substrate from the plasma attack at the end of the etching process.

This technique is attractive when the size of the device and that of the platform/substrate are similar. If the platform is larger than the device, the area around the device, which will be removed, becomes large. As this wasted area increases, the process cost will increase.

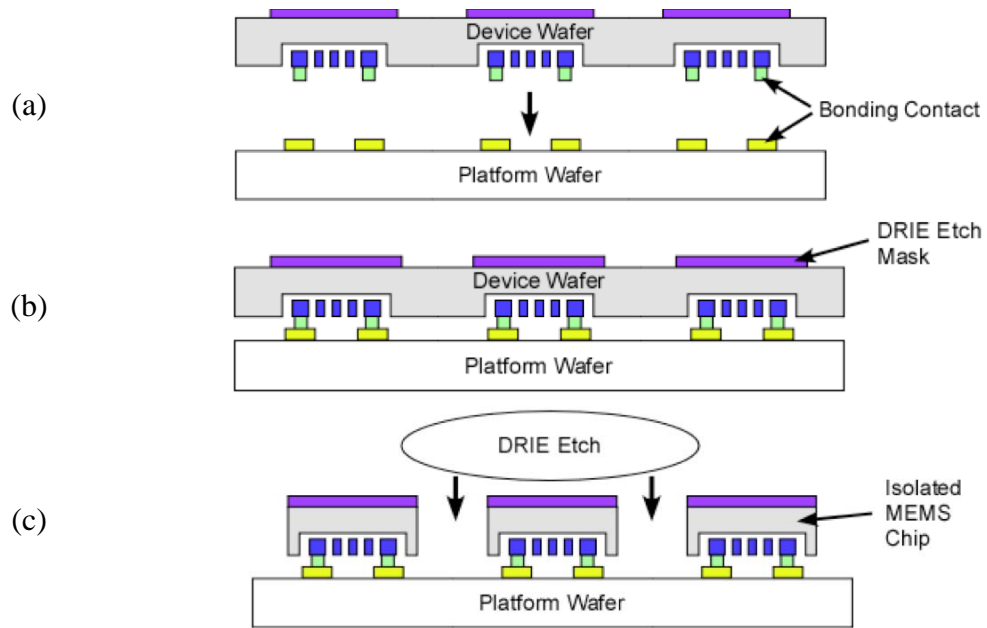


Figure 2.18 Procedure of wafer-level device transfer and DRIE isolation technique. (a) Device wafer and platform wafer are aligned by a commercial wafer bonding machine. On the device wafer, MEMS structure is patterned and backside DRIE etch mask is formed. (b) Two wafers are bonded. Bonding contacts form mechanical and electrical connection. (c) Each die is isolated by DRIE etch.

2.3.3.2 Batch Die-Level Device Transfer Technique

Figure 2.19 illustrates the process of transferring a MEMS device using a guide wafer in a batch die-level transfer technique. This approach allows for batch die-level attachment using standard wafer bonding equipment.

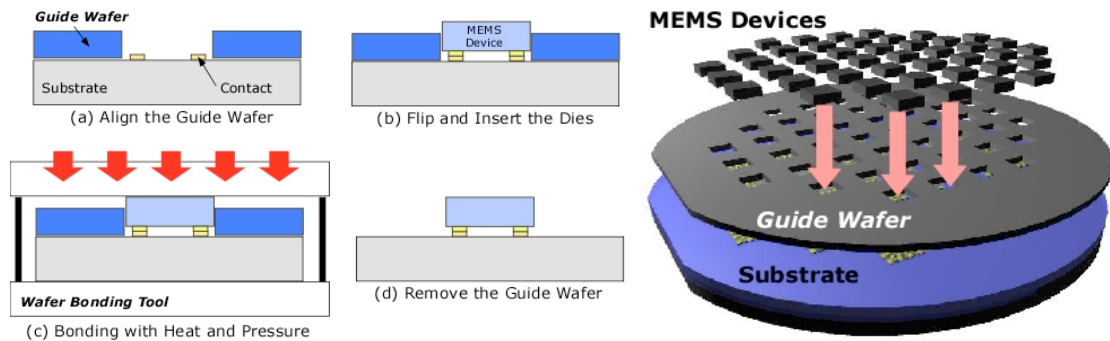


Figure 2.19 Illustration of the batch die-level transfer technique.

This transfer technique has several advantages. First, all of the MEMS devices can be transferred at the same time using a wafer bonder. Second, by changing the guide wafer design, devices with different sizes, shapes and contact locations can be transferred. Third, devices can be precisely aligned.

This technique has been implemented in a package with glass isolation suspension, and detailed results are discussed in Chapter 4.

2.3.3.3 Low-Temperature Press-on Micro-Brush Technique

The third approach, illustrated in Figure 2.20, utilizes the mechanical engagement of arrays of high-aspect-ratio metal posts forming a micro-brush structure [79]. The micro-brush structures obtained by patterning high-aspect ratio photo-resist pillars and then by covering them with metal layer. The press-on micro-brush connection is achieved by directly mating two micro-brush surfaces. Interlocking is accomplished by applying pressure to the upper sample. The alignment between two micro-brush patterns is done by the naked eye.

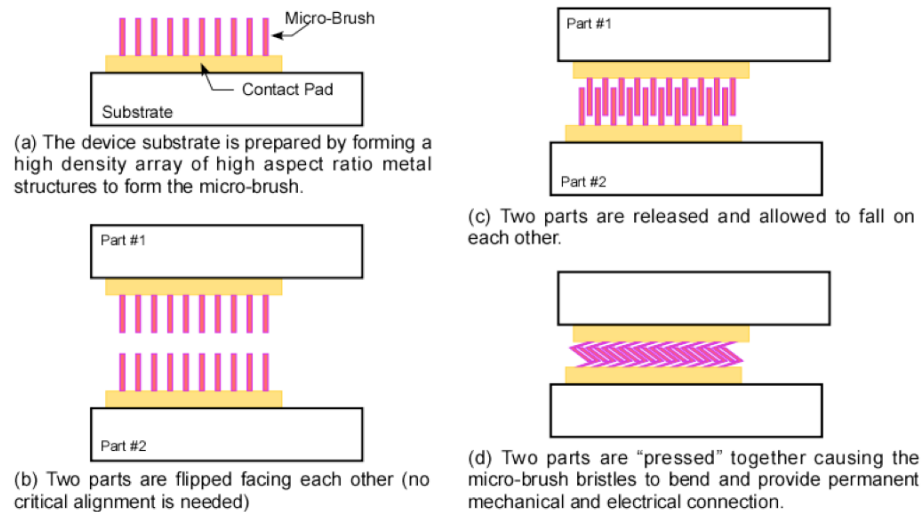


Figure 2.20 Schematic views of the micro-brush press-on connection technique.

This technique offers a number of advantages. First, the attachment is performed at room temperature and does not need any high temperature steps. Second, there is no need for exact alignment. Third, this technique can be applied as easily to a single die as to a full wafer. It is also applicable to printed circuit boards or any application where mechanical and electrical connection is needed. Finally, this technique can be performed at the end of a fabrication process, and it does not require any special processing steps. The detailed process and results will be discussed in Appendix.

2.4 Wafer-level Vacuum Encapsulation

2.4.1 MEMS Wafer-level Encapsulation Approach

Released MEMS structures in wafer form are susceptible to the environment. As a result, they can be damaged during post-fabrication steps such as dicing, pick-and-place, and wire bonding. Therefore, protection directly after fabrication and release is required. This is called 0-level packaging [80]. An encapsulating cap can provide vacuum/hermetic or an inert ambient gas that is sometimes critical for MEMS device operation. This capping process is usually done by surface or bulk micromachining at the wafer-level.

Figure 2.21 shows, schematically, the process steps for wafer-level encapsulation using surface micromachining. The MEMS structure is first covered by a sacrificial layer, and then the first encapsulation layer is deposited. Access holes for removing the sacrificial layer are patterned in the thin film layer. During removal of the sacrificial layer, the MEMS structure can be released simultaneously. Finally the second

encapsulation layer is deposited under a controlled atmosphere such as vacuum or inert ambient.

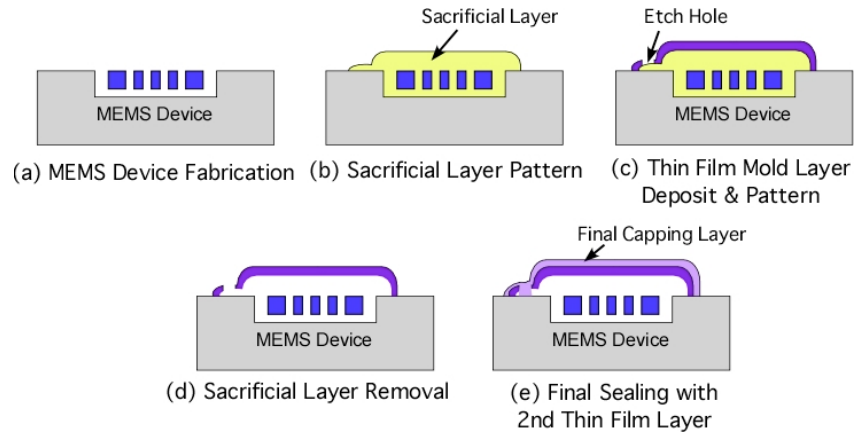


Figure 2.21 MEMS device encapsulation using surface micromachining.

Figure 2.22 illustrates a package fabricated using bulk micromachining. Typically, a cap wafer that contains etched cavities on its surface is bonded to a device wafer in order to encapsulate the MEMS device. Wafer bonding type depends on the application, and process compatibility. The atmosphere inside the cavity can be controlled during the bonding step. Cap parts may be diced into single cap in case lateral signal feedthroughs are used.

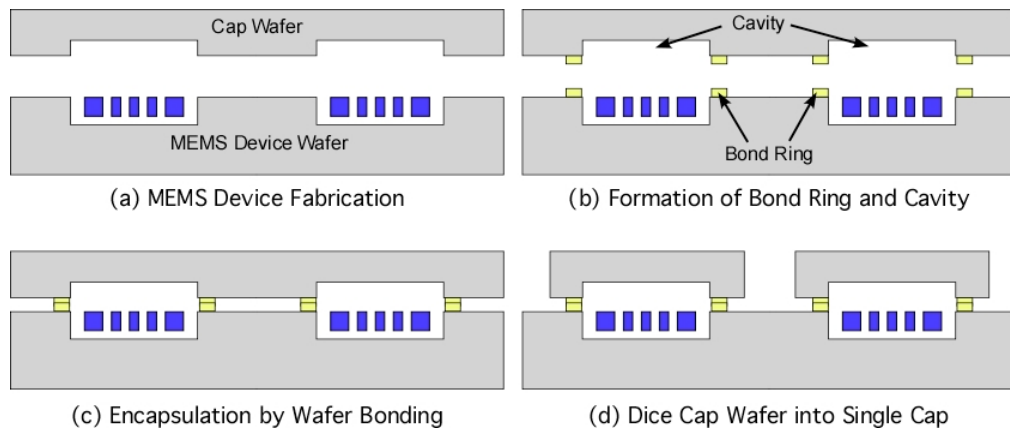


Figure 2.22 MEMS packaging using bulk micromachining (wafer bonding).

Table 2.8 compares these two approaches. A simple and small package is possible using the surface micromachining approach. However, it is difficult to achieve low vacuum pressures using this approach because of two issues. First, especially when the sacrificial layer is a polymeric material, complete removal of that layer through a small access hole is not easy. Small amounts of residue can severely affect the vacuum level inside the cavity. Second, a getter layer is typically required to maintain high vacuum, and it can be difficult to deposit such a layer in this configuration. A vacuum package using a thermally decomposing sacrificial layer [81], and using silicon epitaxial encapsulation layer [82], has been developed to overcome this issue.

Table 2.8 Comparison of two different MEMS packaging approaches [83].

Packaging Tech.	Surface Micromachining	Bulk Micromachining (Wafer Bonding)
Process integration	Difficult	Flexible
Package size/profile	Small	Large
Cost	Low	High
Die area used	Small	Large
Further packaging complexity	High	Low
Mechanical strength	Low	High

MEMS packaging using the bulk micromachining (wafer bonding) approach provides strong and flexible capping by selecting suitable cap material. This cap can also provide additional functionality such as signal (vertical) feedthroughs, additional electrodes, and room for a getter layer. However, it consumes a larger footprint, and as a result can cost more per unit for manufacturing. In the following section, various types of wafer bonding, which have been used for the MEMS package, will be reviewed.

2.4.2 Wafer-to-Wafer Bonding

Wafer bonding is a process by which two wafers are adhered to each other. Originally, the term wafer bonding referred to bonding performed at room temperature without any gluing layer or outside force [84]. The first systematic investigation of bonding two optically polished glass plates was performed in 1936 by Lord Rayleigh [85]. However, it did not have any noticeable technological impact until the middle 1980s. As the microelectronic industry grew up, widespread interest in modern wafer bonding techniques was generated. It served as a substitute process for growth of thick epitaxial layers of single-crystalline silicon or as a process for making SOI (silicon-on-insulator) wafers [86, 87].

Wafer bonding of two silicon wafers without any intermediate layer is now called direct wafer bonding, and the term wafer bonding generally includes all kinds of bonding. In particular, a wide array of different types of wafer bonding techniques (i.e. anodic bonding, solder bonding and polymer bonding) has been developed specifically for MEMS and MEMS packaging applications.

2.4.2.1 Wafer Bonding in MEMS Packaging

Wafer bonding has been found to be a powerful, reliable, and versatile technique in the fabrication of MEMS devices such as pressure sensors [88], accelerometers [89-91], MEMS microphones [92], micropumps [93, 94], and microvalves [95]. It allows for the creation of unique structures such as buried cavities, and enables materials to be integrated when no conventional deposition technique is available.

In addition to allowing for the fabrication of a variety of MEMS structures, wafer bonding is also widely used for MEMS packaging. Historically, some of the earliest uses of wafer bonding were for the packaging of pressure sensors [96]. In particular, as the wafer-level packaging concept got more attention, wafer bonding processes became readily acknowledged in the MEMS industry.

By employing wafer bonding in packaging, effective controls surrounding MEMS devices at the wafer-level are possible. Wafer bonding provides a cavity for free moving structures, a vacuum/hermetic environment for high performance, and fabrication with dissimilar materials. It is also possible to save overall cost by eliminating costly individual chip-packaging steps.

In the following sections, bonding techniques widely used in MEMS packaging are discussed.

2.4.2.2 Categorization of Wafer Bonding Techniques

The wafer bonding processes that are most commonly utilized in the MEMS area can be categorized into three categories: direct bonding, anodic bonding and intermediate-layer bonding [97]. Table 2.9 summarizes the most common wafer bonding technologies [98].

Table 2.9 Summary of common wafer bonding technologies [98].

Process Parameters for Wafer Bonding							
General Method	Electric Field	Direct Bonding		Intermediate-Layer			
Bonding Process	Anodic	SDB	Plasma Activated	Glass Frit	Thermal Compression (metal-metal)	Eutectic	Adhesive
CMOS Compatibility	×	×	✓	×	✓	☑	☑
Temp. Range	~1000°C	×	✓	×	×	✓	×
	<450°C	✓	×	✓	✓	✓	✓
	<300°C	×	×	✓	×	☑	✓
	RT	×	×	☑	×	×	×
Vac. Compatibility	Low <1Torr	✓	✓	✓	✓	✓	✓
	High <10mTorr	✓	✓	☑	×	✓	×
Surface Roughness (both surface)	<1μm	×	×	×	✓	✓	✓
	<20nm	×	×	×	✓	✓	✓
	<2nm	✓	×	✓	✓	✓	✓
	<0.5nm	✓	✓	✓	✓	✓	✓
Environment	Cleanroom Class	100	10	10	1000	10	100
Sensitivity to Particle	Low	×	×	×	✓	×	✓
	Medium	✓	×	×	×	✓	✓
	High	×	✓	✓	×	×	×
Industrial Environment	Low Volume	✓	✓	R&D	✓	✓	✓
	High Volume	✓	✓	×	✓	×	✓

✓ Fully compliant ☑ Compliant with certain limitations or boundary conditions × Not compliant

Direct wafer bonding

Using direct bonding, wafers are bonded without an intermediate layer or electric field. This technique usually utilizes some form of annealing during contact to increase

the bond strength. Additional activation treatment on the bonding surface can also enhance the bonding strength [99, 100]

Direct bonding offers the advantage in some circumstances of being stable at high-temperatures, thus permitting a wide range of subsequent processes. Additionally, silicon-to-silicon direct bonds produce structures with far less thermal expansion mismatch problems as compared to anodic or eutectic bonding. However, extreme care is required in preparing the wafer surfaces, because generally the wafers should have surface roughness of no greater than 10 Å and a bow of less than 5 µm (on a 4 inch wafer) [101, 102]. As a result, it is very challenging to achieve vacuum sealing using direct bonding.

Anodic bonding

In 1969, Wallis and Pommerantz first developed anodic bonding [103]. It was initially developed for the bonding of metal to glass, and subsequently the metal was replaced by silicon. In the case of silicon-to-glass anodic bonding, a glass and silicon substrate are put into contact, and are heated to 300-400 °C with a voltage of 200-1000 V applied. The electric field and temperature cause sodium ions in the glass to migrate away from the bonding interface leaving behind negative fixed charges. This fixed charge causes a high electric field across the wafers, which presumably encourages strong bonding between the two interfaces.

Anodic bonding is not desirable for many advanced microelectronic devices because of the presence of mobile ions. However, it does have a larger tolerance to surface roughness than direct bonding, and a relatively high bonding strength (> 350 psi).

As a result, it has been widely applied for vacuum/hermetic encapsulation of MEMS devices such as pressure sensors [104], gyroscopes [105], accelerometers [106], flow sensors [107] and infrared sensors [108].

Anodic bonding of glass-to-glass [109, 110] or silicon-to-silicon with an intermediate glass layer have also been developed [111-113] for MEMS packaging. These techniques can minimize the stress issues induced from thermal expansion mismatch.

Intermediate-layer bonding

A wide range of intermediate layers has been used for wafer-to-wafer bonding in MEMS packaging. These approaches include:

- a. Solder/Eutectic/Transient Liquid Phase (TLP) bonding*
- b. Polymer bonding*
- c. Glass Frit bonding*
- d. Thermo-compression bonding*

All these bonding techniques use materials with low melting temperatures or high ductility for gluing two wafers together. The advantages of the intermediate-layer bonds are: they have large tolerance of surface roughness because of planarization capability, low temperature bonding is possible with suitable material combinations, thermal mismatch stresses can be minimized because of the low bonding temperatures and relatively thin gluing layer.

Solder bonding, eutectic bonding and TLP bonding are similar in nature. Metal alloys or metal-silicon alloys have lower melting point than pure material. They reach a

liquid phase at the bonding temperature, adhering the two wafers together after cooling. Suitable material combinations are determined by the alloy's melting point, bonding strength, and process compatibility. TLP bonding has one difference in the formation of intermetallic compounds, which are stoichiometrically stable materials. These compounds are stable up to a certain re-melting point, which is generally higher than the actual bonding temperature. Therefore, it has the advantage of allowing for a bond at a relatively low temperature, which can handle much larger temperatures.

Polymeric materials such as SU-8 [114], BCB (benzocyclobutene) [115, 116], CYTOP (fluorocarbon polymer) [117, 118], PMMA (polymethylmethacrylate) [119], Polyimide [120], MYLAR [121], and Parylene (poly-paraxylylene) [122] have all been used for wafer bonding. They have relatively low melting or low glass-transition temperatures, so that low temperature bonding is possible. However, this technique will be difficult to apply to vacuum encapsulation because of its lack of hermeticity and existence of outgassing.

Glass frit is a low melting-temperature glass paste mixture that is used as a bonding agent [123]. Its advantages are that it is non-conductive, and can be conformally patterned by screen-printing over non-planar surfaces. It also provides production-worthy bonding strength, and allows for vacuum sealing with a suitable getter layer [124, 125]. However, this bonding technique has limited resolution, $\sim 150 \mu\text{m}$, and requires relatively high bonding temperatures, $\geq 450 \text{ }^\circ\text{C}$, which are not compatible with CMOS processes [126]. Glass frit also generally contains lead, which will be banned from use in microelectronics.

Thermo-compression bonding utilizes ductile metal layers (i.e. gold) that are patterned on both wafers. Bonding is performed at a high pressure and high temperature which allows for a permanent attachment by inter-diffusion of metal atoms, and has been widely used due to its process simplicity [127]. However, the atomic inter-diffusion requires a highly clean and flat surface, which results in a low tolerance to surface roughness than other intermediate layer bonding technologies.

2.4.3 Vacuum Encapsulation

Many MEMS devices require a vacuum environment. Vacuum encapsulation in particular enhances performance of resonating sensors by minimizing gas molecular damping. However, vacuum encapsulation and maintaining high vacuum is still a challenge in MEMS packaging. Major sources of vacuum degradation are (1) leakage, (2) outgassing after sealing, and (3) gas permeation through the substrate or bond ring as shown in Figure 2.23.

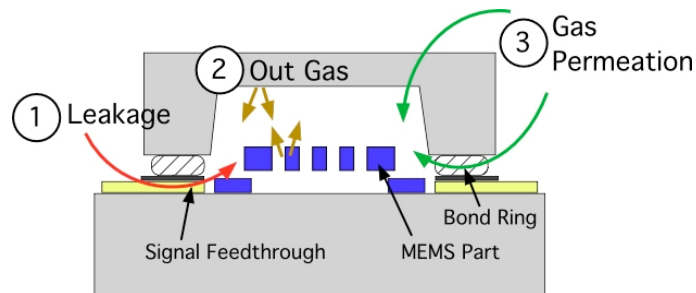


Figure 2.23 Major sources of vacuum degradation.

The leakage of gas molecules is mostly due to the surface roughness over the bonding seal or imperfections on the surface, which are often caused by electrical feedthroughs. This effect can be reduced by choosing a suitable bonding method that has a large tolerance to surface roughness. Furthermore, the step height due to lateral signal

feedthrough can be eliminated by using additional surface flattening process or using a vertical feedthrough.

After vacuum sealing, gas molecules can be desorbed or vaporized from cavity wall or MEMS structure. This process is called outgassing. Typically H₂O is the dominant outgassing molecule [128]. In particular, electroplated materials or polymer materials are known to generate many gaseous atoms. These outgassing issues have been resolved by using a getter material inside the package or by high temperature bake outs under a vacuum atmosphere. The getter materials are typically Ti-Zr-V alloys [129] or pure Ti [130] that have strong affinities to gas molecules. These getter layers often requires high temperature activation steps, which can deteriorate a package created using a temperature wafer bonding technique.

Gas permeation through enclosing walls or the bond rings is another potential source of increased pressure over time. The permeation rate of gas molecules depends on the packaging materials, pressure differences, and thicknesses. Glasses, ceramics, silicon nitrides, metals, and some pure crystals allow low permeation rates. Material thickness is a key factor in preventing any gas permeation. For instance, in one study, the amount of permeated gas decreased hundred times when the thickness of the package wall is increase from 10 μm to 1 mm [131].

In our work, we have used bulk micromachining methods for vacuum encapsulation. Anodic bonding and Au-Si eutectic wafer bonding method have been utilized for wafer-level encapsulation. The NanoGetter™ from ISSYS, Inc. has been employed for the getter material. Detailed implementations of the wafer-level vacuum encapsulation will be discussed in Chapter 3, 4 and 5.

2.5 Vertical Feedthroughs

2.5.1 Feedthroughs in MEMS packaging

In wafer-level MEMS packaging, two types of feedthrough configurations are used: lateral and vertical feedthroughs. Lateral feedthroughs consume a significant die area, and are often the cause of leakage/failure in a vacuum package due to non-planar surfaces. They also require a wire bonding step for 1-level packaging, because a step height due to 0-level packaging prevents surface mounting processes.

Vertical feedthroughs can help to overcome many of these issues. First, they generally reduce footprint, because large areas for wire bonding can be located over or under the package. Second, the step heights of the feedthroughs can often be eliminated allowing for a wide range of bonding methods to be applied for sealing the device. Third, there is the potential for eliminating the 1-level package, if the package is designed to be compatible with surface mount technology (SMT).

Most vertical feedthroughs are based on through-wafer vertical holes filled with conductive material. These holes are formed by wet etching, laser/mechanical drilling, sandblasting or Deep Reactive Ion Etching (DRIE). Table 2.10 summarizes some of the vertical feedthroughs developed for MEMS packaging.

Table 2.10 Summary of vertical feedthrough techniques for the MEMS packaging application.

Substrate	VIA Formation Tech.	VFT Material	Ref.
Glass	DRIE	Electroplated Ni	[132, 133]
Glass	Wet etching	Thin film metal/solder	[134, 135]
Glass	Sand blasting	Wire bonding	[136]
Silicon	DRIE	Electroplated Cu	[137-139]
Silicon	DRIE	Poly Si	[140, 141]
Sapphire	Laser drilling	Conductor-filled liquid	[142]
Ceramic	Micro-machining	Ag	[143]

2.5.2 Vertical Feedthroughs for the Environment-Resistant Package

To realize our project goals, our feedthroughs should have a small footprint, small parasitic capacitance, and be robust to minimize any leakage. They also should be compatible with wafer-level processes.

Here we have proposed and developed two types of vertical feedthroughs. The first type is a vertical feedthrough through a glass wafer as shown in Figure 2.24. This was first developed by Chae *et. al.* [134, 135], and modified so that a more generic approach would be possible. The feedthrough holes are formed by wet etching, and filled with a conductive material. Before wet etching the glass substrate, a metal or silicon plug is patterned to prevent any leakage. This is a simple and robust technique for small size packages ($<2 \times 2 \times 0.6 \text{ mm}^3$). Detailed implementation of this feedthrough in the environment-resistant package will be discussed in Chapter 3.

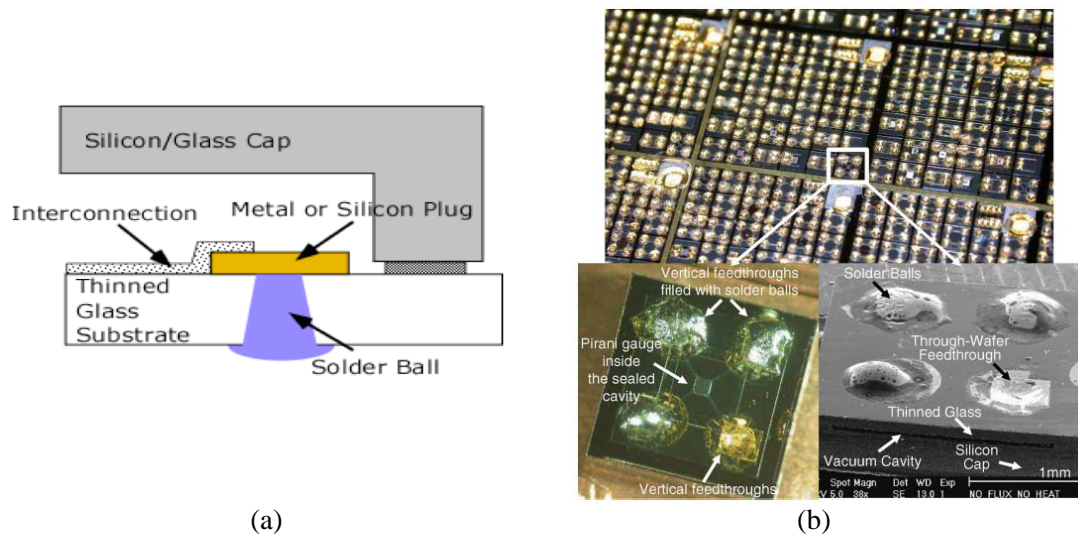


Figure 2.24 (a) Schematic view of the vertical feedthroughs in a thinned glass substrate. (b) Optical and SEM photos of vertical feedthroughs through a glass substrate. A MEMS Pirani gauge is vacuum packaged for measuring a pressure level inside the package [135].

The second type of vertical feedthrough is formed on a glass-silicon bonded substrate as shown in Figure 2.25. This feedthrough can be located either on a device wafer or on a cap wafer. The thickness of the glass is thin enough to be wet etched with only a small undercut. After forming the via using wet etching, the silicon feedthrough is electrically isolated by DRIE. Via hole on the glass is filled with a thin film metal layer for electrical connection to the MEMS device. Detailed implementation will be discussed in Chapter 4 and Chapter 5.

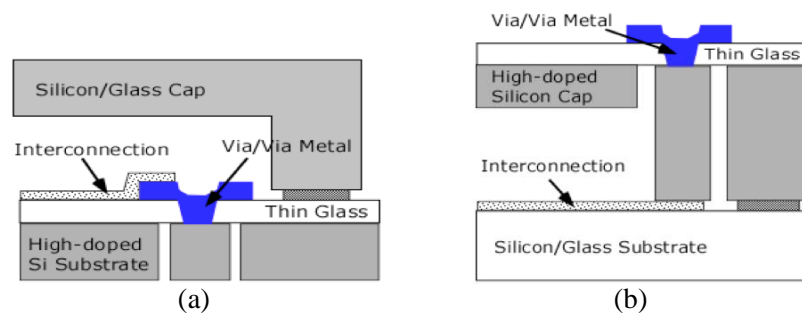


Figure 2.25 Schematics of the proposed vertical feedthroughs in thin glass/silicon wafer. (a) Bottom feedthrough located in the platform substrate, (b) Top feedthrough located in the cap substrate.

2.6 Summary

In chapter 2, five key technologies for the environment-resistant package have been introduced. Thermal isolation is provided by oven-controlling the MEMS device utilizing an integrated heater. To minimize the necessary input power for heating the device, the isolation suspensions/platform, radiation shield, and vacuum encapsulation have been employed in the package. The isolation suspensions also provide vibration isolation. Soft metal coating for shock protection is adopted. To realize a generic packaging approach, three different device transfer/assembly technologies have been developed. Wafer-level vacuum encapsulation with vertical feedthroughs enables both 0-

level and 1-level packaging simultaneously. The vacuum package also allows for high performance in many MEMS applications.

There are many other methods developed for the five key areas. These technologies have advantages in their performance. However, to realize our objectives, all these five technologies should be merged seamlessly. Combining these five technologies into one package is challenging, because these technologies are not stand-alone but correlated to each other. In Chapter 3 and Chapter 4, implementation of these five technologies will be discussed in detail. In Chapter 5, low power oven-controlled package utilizing these technologies will be presented.

Chapter 3

Generic Environment-Resistant Package with Meandering Metal Suspension

3.1 Package Design

3.1.1 Package Concept

A generic wafer-level package for high performance MEMS devices has been developed (Figure 3.1) [79]. This package simultaneously provides thermal and mechanical isolation by suspending the device utilizing meandering metal suspensions. The suspensions are designed to have high thermal resistance through solid conduction for the low power oven-control. By meandering the suspension, the footprint can be minimized while maintaining a high thermal resistance. The suspensions also act as electrical signal paths. The MEMS devices are fabricated on a separate wafer, and then batch transferred onto the suspensions prior to their final release. A micro heater and temperature sensor are integrated on the MEMS device for oven-controlling the device at a fixed temperature. Separating the fabrication of the device and the package allows almost any type of device to be packaged with minimal changes to the device design and

fabrication. The isolation structures, including the MEMS device and suspensions, are placed on a glass wafer (called platform substrate) where vertical feedthroughs are implemented. The vertical feedthroughs allow for direct flip-chip bonding onto a printed circuit board, which can potentially eliminate the cumbersome wire bonding step. Vacuum encapsulation is performed by bonding a silicon cap wafer with cavities to the platform substrate at the wafer-level. An anti-radiation layer, a shock absorption layer and a getter layer are all deposited on the cap wafer.

The micro-oven efficiency can be improved by making the meandering metal suspensions longer and thinner. However, because of the large mass (milli-grams) of the MEMS device, large forces caused by environmental vibrations could cause loss of thermal isolation due to touch-down of the device or breakage of the suspension. The simultaneous requirements of high thermal and mechanical isolation make the suspension design challenging. Various types of meandering suspensions have been tested.

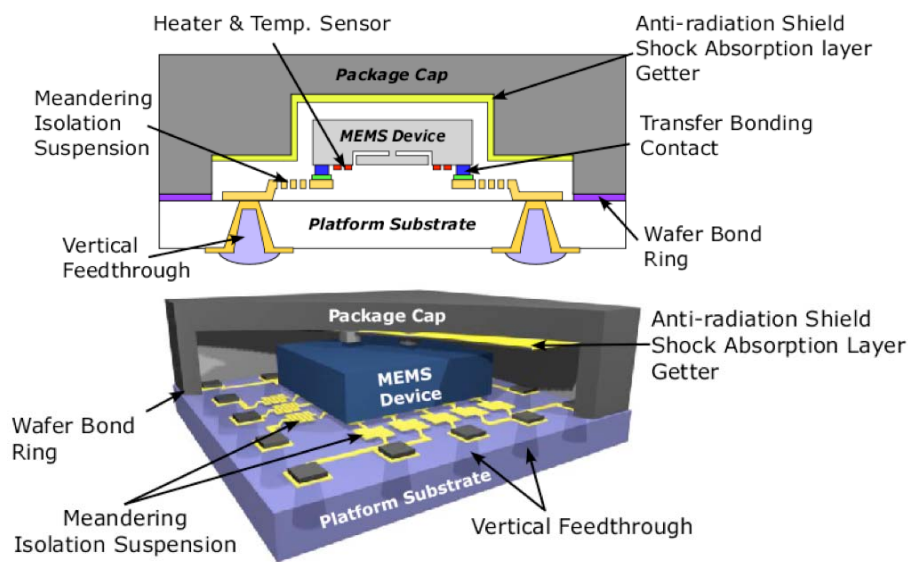


Figure 3.1 Schematic illustration of the generic environment-resistant package with meandering metal suspensions. The MEMS device is flip-chip transferred on the

meandering isolation suspensions, and vacuum encapsulated.

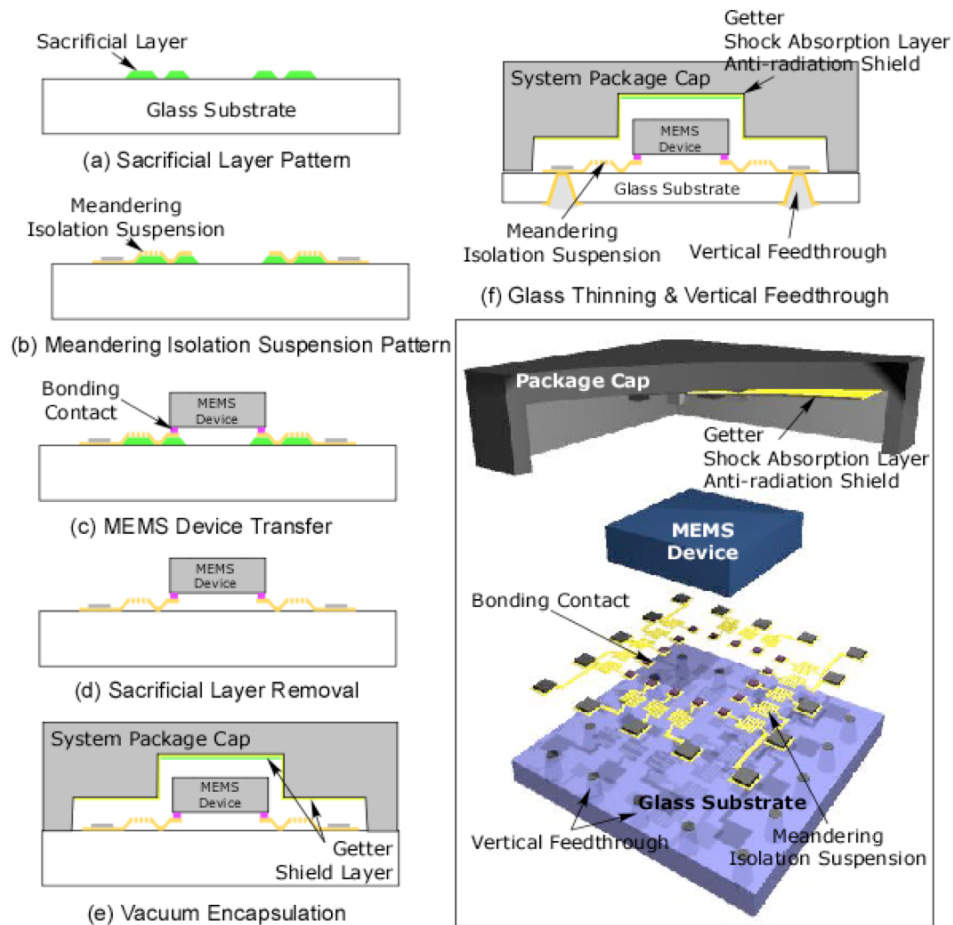


Figure 3.2 Illustration of the fabrication procedure and exploded view of the package.

3.1.2 Packaging Process

Figure 3.2 shows the fabrication process for the package with meandering metal suspensions. First, a sacrificial layer is patterned on a glass substrate (called platform substrate, Figure 3.2 (a)). The sacrificial layer can be either a polymer such as polyimide or thermally decomposable material (Unity™). Then, a metal layer is deposited or electroplated to form the suspensions. After defining the suspensions, if needed, contact metal is patterned for subsequent wafer-level transfer bonding. This completes the

fabrication of the glass platform substrate (Figure 3.2 (b)). The devices to be packaged are fabricated on a separate wafer (called device wafer) and then bonded to the isolation suspensions using the wafer-level transfer technique (Figure 3.2 (c)). This transferring technique is reviewed in section 2.3.3.1 of Chapter 2. Singulation of each die is performed by DRIE around the device. The thickness of the singulated dies can be reduced in this step in order to reduce thermal mass and weight. A die-level assembly instead of the wafer-level transfer is also possible using a suitable bonding mechanism such as “micro-brush” technique (described in Appendix). The transferred devices and suspensions are released by removing the sacrificial layer, preferably using a dry etch (Figure 3.2 (d)).

Vacuum encapsulation is done by bonding a silicon wafer with cavities to the platform substrate at the wafer-level (Figure 3.2 (e)). This cap wafer can be made of glass or other materials depending on its applications and bonding techniques. The depth of the cavities is determined by the height of the transferred devices. A shock absorption layer made of gold for mitigating impacts from an environmental shock is covered inside of the cavities. This layer can act as an anti-radiation shield layer to reduce the heat loss through radiation. A getter layer for maintaining high vacuum is also coated on the cavity wall. After wafer-level encapsulation, the glass substrate is thinned down by wet etching. Finally, vertical feedthroughs are formed on the thinned glass substrate (Figure 3.2 (f)).

3.1.3 Chapter Overview

In the following sections, each process step will be discussed in detail. First, the isolation suspension design and fabrication will be detailed in section 3.2, followed by a

description of the sacrificial layers for suspending the structure in section 3.3. The MEMS device transfer technique and vertical feedthroughs will be presented in sections 3.4 and 3.5. Finally, thermal resistance measurement result of the package will be shown in section 3.6, followed by a chapter summary in section 3.7.

3.2 Meandering Metal Isolation Suspension

3.2.1 Meandering Metal Isolation Suspension

3.2.1.1 Metal Isolation Suspension

As explained in the previous section, the MEMS device is suspended by metal isolation suspensions connected around the die. The metal suspensions are designed to provide high thermal resistance through solid conduction, vibration isolation, and electrical signal paths. Other materials such as polymers, glass or dielectric layers would require additional interconnection lines for signal feedthrough, because they are not electrically conductive. Furthermore, polymeric materials are not compatible with vacuum packaging and high temperature processes, because they typically outgas and degrade the vacuum level. Silicon would be a good candidate for the suspension material, because it has good mechanical and electrical properties. Either a poly-silicon layer can be deposited or a silicon wafer can be bonded onto the glass wafer in order to realize the silicon suspensions. However, a high temperature process is generally required to deposit a poly-silicon layer, which would not be compatible with glass. As well, a bonded silicon wafer on the glass would need to be thinned down to a suitable thickness, which would increase the process cost and complexity.

The metal suspension can provide both mechanical support and electrical signal path. Thin film metal deposition such as evaporation and sputtering is simple, and only requires lithography, metal deposition and lift-off (or metal etching) step. Because metal has good ductility, it can help to reject any environmental vibration.

3.2.1.2 Two Types of Meandering Suspension

As described in section 2.1 in Chapter 2, the isolation suspensions should provide thermal isolation, mechanical support and electrical connection. These three characteristics should be considered in the design of the isolation suspensions. To increase the thermal resistance of the suspensions, the suspensions need to be long and thin. However, mechanical stiffness and electrical conductance decrease as the suspension length increases.

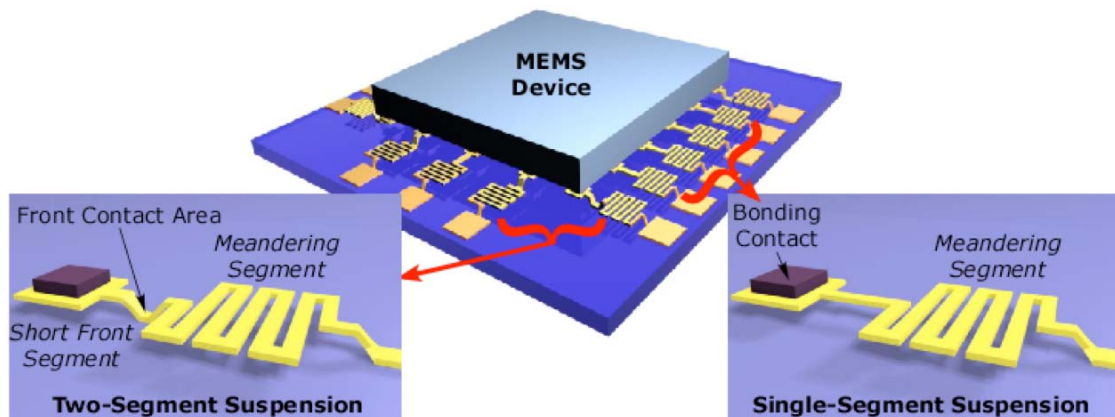


Figure 3.3 Schematic illustration of the two types of isolation suspensions. Two-segment suspension (left) provides mechanical support, and the single-segment suspension (right) enhances the thermal resistance.

To overcome these challenges, two types of isolation suspensions are applied: a *single-segment* meandering suspension, and a *two-segment* meandering suspension consisting of a meandering segment and a straight segment (Figure 3.3). Although the

single-segment meandering suspension design provides a large thermal resistance, it does not provide sufficient mechanical stiffness. Therefore, a combination of the single- and two-segment suspension designs is used as a more practical approach. In the two-segment suspension design, the short front segment (beam) connects to the suspended device and significantly increases mechanical stiffness, while the long meandering segment connects to the output pad on the insulating substrate. The connection point between the two segments touches the substrate to provide the large mechanical stiffness. However, because the touchdown area is small compared with the output pad area, only a minimal amount of heat is dissipated through these contact points.

3.2.1.3 Suspension Design Optimization

The suspension design is optimized according to the package specifications. The preliminary design parameters are summarized in Table 3.1. The target power consumption for the heater is less than 10 mW over an environment temperature range from -50 to 70 °C while the isolation platform is oven-controlled at a fixed temperature of 80 °C.

Table 3.1 Design parameters for the isolation suspension design.

Design Parameter	Value
Dimension of MEMS device	$3 \text{ mm} \times 3 \text{ mm} \times 350 \text{ }\mu\text{m}$
Total number of suspension	18 EA (8 two-segment suspensions)
Suspended gap	$2\sim 5 \text{ }\mu\text{m}$
Maximum power consumption	10 mW
Operating environment temperature	$-50 \sim 70 \text{ }^\circ\text{C}$
Oven-control temperature	$80 \text{ }^\circ\text{C}$

These requirements can be achieved by providing a high thermal resistance ($>13,000$ K/W) between the environment and the heated element (See equation 2.1 from section

2.1.1 in Chapter 2). Figure 3.4 illustrates the heat dissipation paths for the package, and a lumped thermal circuit model used for thermal analysis. As illustrated, the two-segment suspensions have two heat loss paths. Part of the heat is dissipated at the front contact area, and the rest goes through the meandering segment. The single-segment suspensions only have one heat loss path from the heated device to environment. At equilibrium, the temperatures of the glass substrate and package cap are assumed to be the same as the environment temperature.

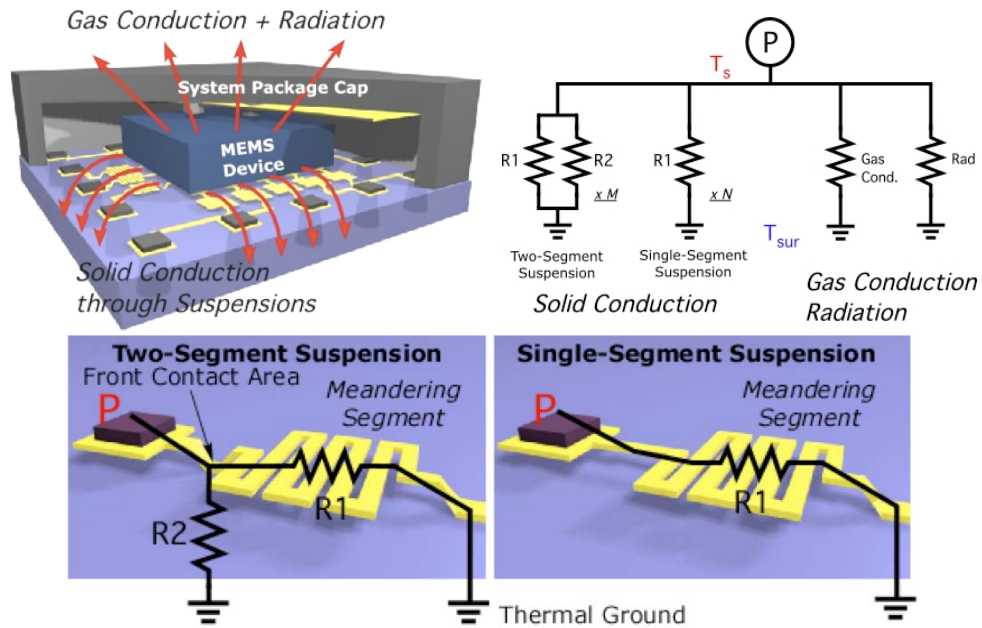


Figure 3.4 Schematic illustration of the thermal loss paths, and the lumped thermal circuit model in the package.

As mentioned above, the suspensions need not only provide high thermal resistance but also high stiffness to support the large isolation platform. The total mass of the MEMS device in our application is 7.3 milli-grams (this corresponds to the mass of a silicon device of 3 mm on a side and 350 μm thickness: Table 3.1). Under this condition, the mechanical spring constant of the suspensions should be at least 144 N/m to limit the maximum deflection to $<0.5 \mu\text{m}$ for the isolation structure under a 1g gravitational

forces. The total spring constant, k , for simple suspended beams with a rectangular cross section is given by:

$$k = nEw\left(\frac{t}{L}\right)^3 \quad (3.1)$$

where, n is total number of the beams, E is Young's modulus, t is the thickness, w is the width and L is the length [144]. Our analysis indicates that using a simple suspended rectangular beam, there are no material and dimension combination which would allow us to satisfy both our thermal and mechanical requirements.

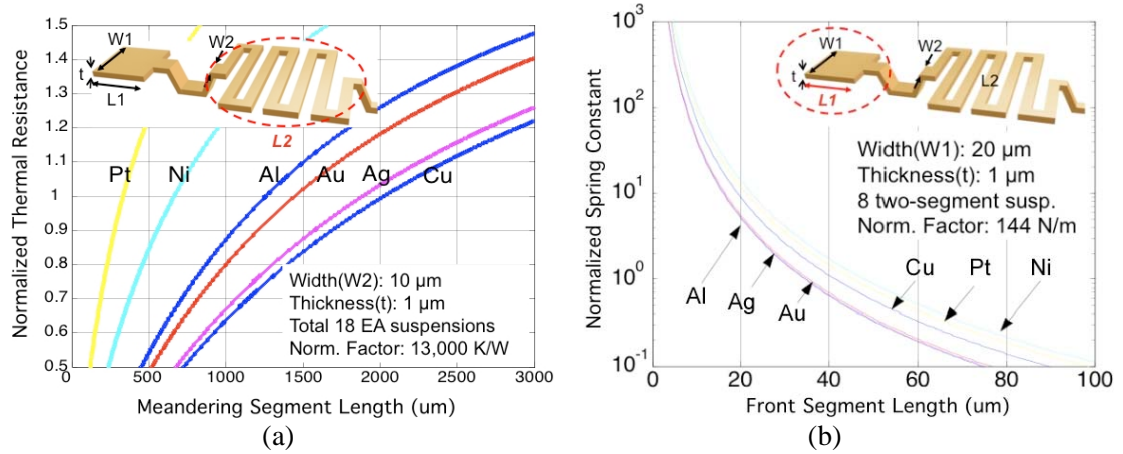


Figure 3.5 Simulation results of normalized total thermal resistance and spring constant with varying the length of the isolation suspension and suspension materials.

Figure 3.5 shows MATLAB simulation results for a combination of the single- and two-segment suspension designs. The total thermal resistance and spring constant as a function of suspension dimensions for different suspension materials have been calculated. These simulation results are normalized to a spring constant of 144 N/m and a thermal resistance of 13,000 K/W, respectively. These simulations are modeled using 8 two-segment suspensions plus another 10 single-segment suspensions (a total of 18 leads). The total number of suspensions is determined by the MEMS device

specification. The modeling parameters are shown in Table 3.2. The plots in Figure 3.5 can be used to select the dimensions of the suspensions and their material. For example, using gold suspensions, the front segment length needs to be shorter than 40 μm , and the meandering segment length needs to be longer than 1500 μm .

Table 3.2 Modeling parameters for the isolation suspension design.

Modeling Parameter	Value
Suspension thickness	1 μm
Front segment width	20 μm
Meandering segment width	10 μm
Front touching area	20 $\mu\text{m} \times 10 \mu\text{m}$
Pressure inside encapsulation	100 mTorr
Emissivity of shielding metal (ϵ)	0.1
Normalization factors	13,000 K/W, 144 N/m

3.2.1.4 Plain Metal Isolation Suspension

In order to test the effectiveness of the isolation structure, test chips with a heater and temperature sensor are fabricated and transferred. The silicon test chip is aligned and flip-chip attached on the meandering suspensions at the die-level (Figure 3.6). The micro heater and temperature sensor are used for measuring the thermal resistance of the package. Sacrificial layer under the meandering suspension is not removed.

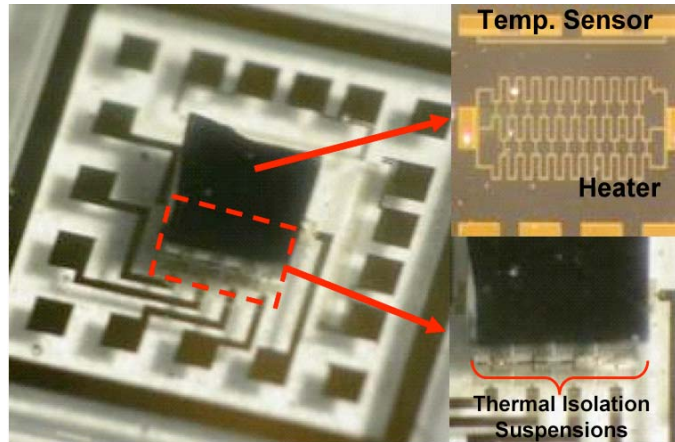


Figure 3.6 Picture of a package die before encapsulation. A silicon test chip with integrated heater and temperature sensor is attached on the meandering isolation suspensions.

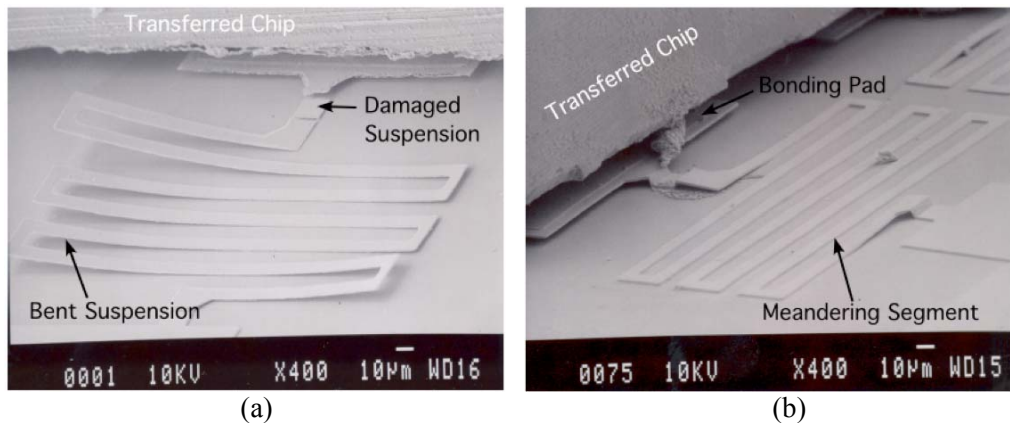


Figure 3.7 SEM pictures of the isolation suspension made out of evaporated gold. The suspension suffers damage, bending and stiction after sacrificial layer removal.

Figure 3.7 shows thin film meandering isolation suspensions after removing the sacrificial layer. The suspensions are made out of an evaporated 1 μm -thick Au layer, and the test chip is transferred before sacrificial layer removal. In this test, thermally decomposable sacrificial layer, Unity™, has been used.

There are several issues in fabricating the suspensions using thin film metal layer: the residual stress of the metal layer causes bending after releasing (Figure 3.7 (a)); the

center area of the meandering suspension touches the substrate due to this bending, and heat would be dissipated through that area; stiction of the whole suspension to the substrate is also observed (Figure 3.7 (b)); the front segment of the suspension does not provide enough mechanical support, so that the whole structure is not suspended; and some parts of the suspension, especially at the touch-down region, are damaged as shown in Figure 3.7 (a).

3.2.2 Enforced Metal Isolation Suspension

As shown above, plain thin film suspensions suffer from residual stress and stiction during sacrificial layer removal. We have proposed two modified suspension designs that can provide a larger mechanical supporting force: (1) hollow beam enforced suspension, and (2) inverse T-shape enforced suspension.

3.2.2.1 Hollow Beam Suspension

To further increase the stiffness of the suspension, the beam can be shaped as a pipe, ‘hollow beam’, as shown in Figure 3.8, instead of a plain slab. By utilizing this hollow beam design at the front segment, the stiffness can be increased without significantly reducing the thermal resistance.

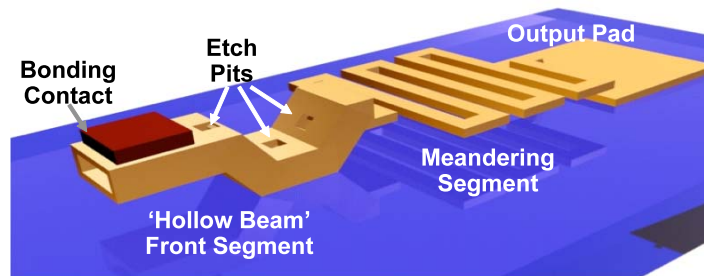


Figure 3.8 Schematic illustration of the hollow beam suspension. The front hollow beam enhances the stiffness.

After the first sacrificial layer is patterned, the bottom metal suspension part is formed (Figure 3.9 (a-b)). The second sacrificial layer is patterned on the front segment of the bottom suspension (Figure 3.9 (c)). On top of the second sacrificial layer, another metal layer is deposited and patterned. Etch pits can help to remove the sacrificial layer inside the hollow beam (Figure 3.9 (d)). Finally, the MEMS device is transferred and the sacrificial layers are removed (Figure 3.9 (e)).

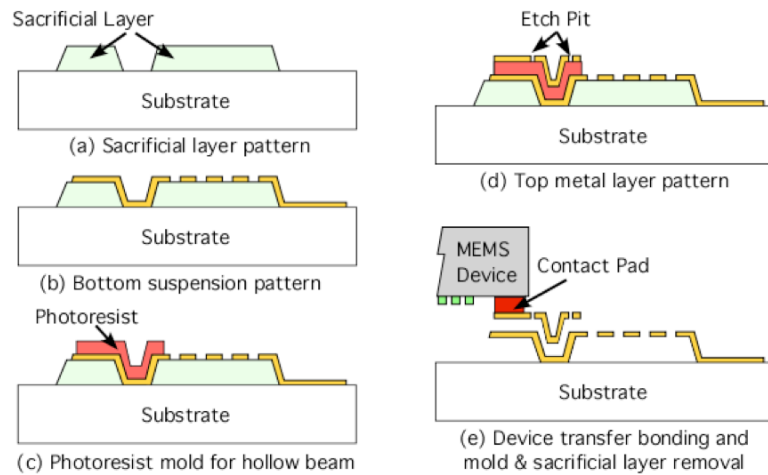


Figure 3.9 Process procedure for the hollow beam suspension.

Simulation results shows that a suspension with a 100 μm long hollow beam segment and a 0.5 μm -thick meandering segment improves thermal isolation that is $\sim 1.3\times$ and spring constant that is $\sim 1000\times$ (Figure 3.10) larger than a suspension with 100 μm long rectangular plain front beam segment and 1 μm -thick meandering segment. The total thermal resistance and spring constant are normalized with the same parameters shown in Table 3.2. The ' t_b ' is the thickness of the bottom metal layer.

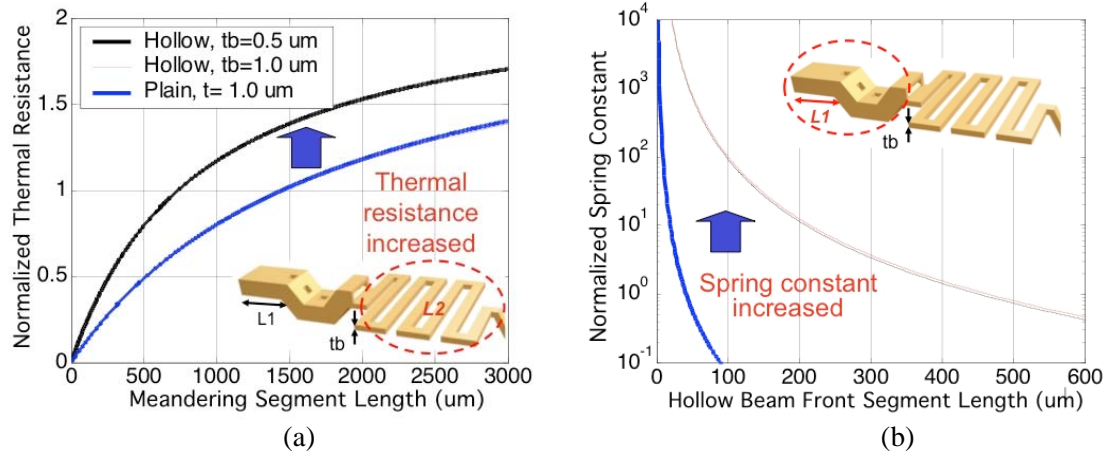


Figure 3.10 Simulation results of (a) normalized thermal resistance and (b) normalized spring constant for the hollow beam suspension made out of gold.

Using this hollow beam design, the stiffness of the front-segment increases, but that of the meandering segment does not. Therefore, the same issues described in section 3.2.1.4 cannot be resolved completely. The meandering segments would still suffer from the stress-induced bending and stiction during sacrificial layer removal.

3.2.2.2 Inverse T-shape Meandering Suspension

Suspension modeling

To overcome the stiction and bending issues in the isolation suspension fabrication, inverse T-shape suspension has been investigated (Figure 3.11). This design is similar to the hollow beam design described in 3.2.2.1, except that the width of the top vertical part is small. By reducing the vertical part width, the cross-sectional area can be reduced that is desirable in minimizing the thermal loss.

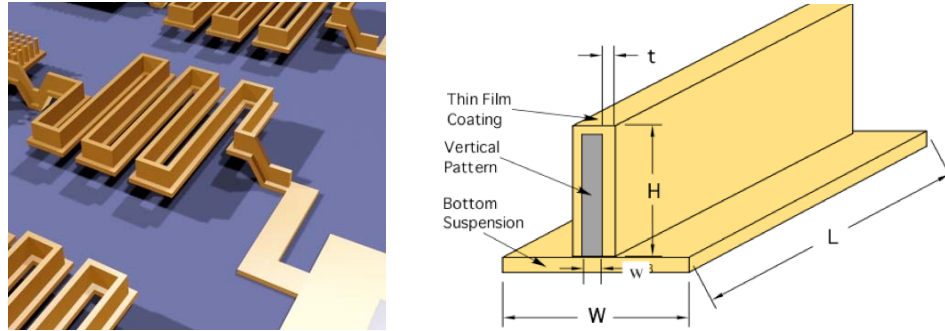


Figure 3.11 Schematic illustration of the inverse T-shape suspension.

The Plain bottom suspension is formed on the sacrificial layer, and then a photoresist mold is patterned for the vertical mold (Figure 3.12 (a-b)). The second metal layer is sputtered around this photoresist mold. The second metal layer is defined with wet etching using the same mask layout that is used for patterning the first bottom suspension (Figure 3.12 (c)). Finally, the sacrificial layer under the suspension is removed (Figure 3.12 (d)).

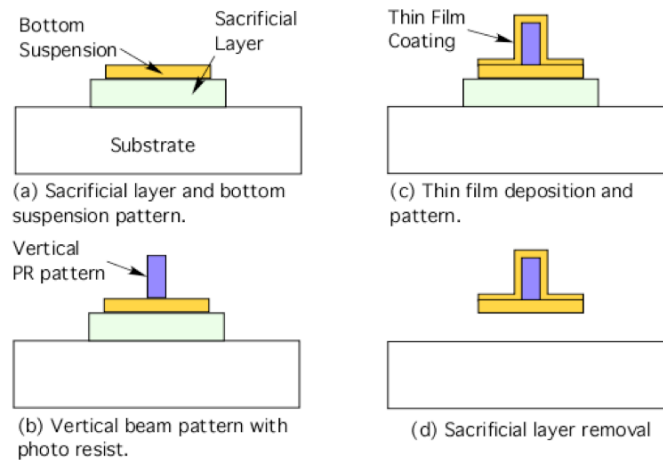


Figure 3.12 Process procedure for the inverse T-shape metal suspension.

The vertical enforced beam improves spring constant by $\sim 100\times$ as shown in Figure 3.13. However, the thermal resistance decreases due to the increased cross-

sectional area. This can be compensated by increasing the total length of the meandering segment of the suspension.

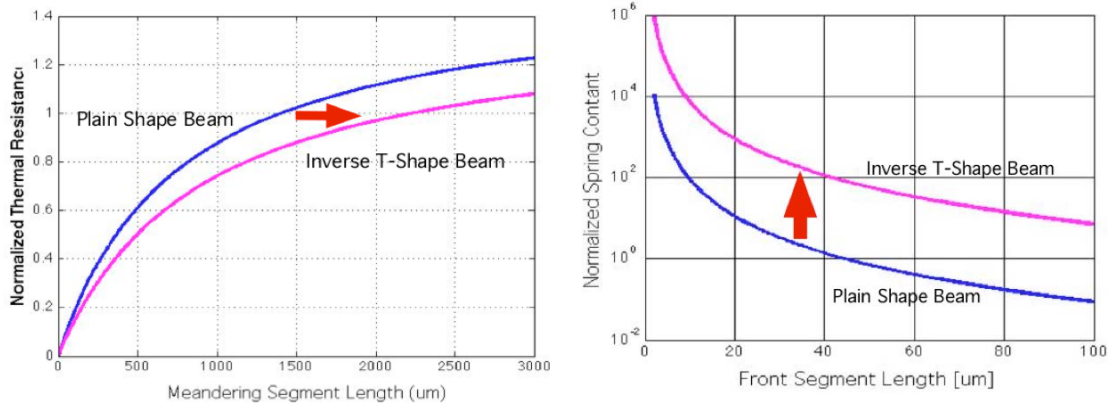


Figure 3.13 Simulation results of normalized thermal resistance and spring constant for the inverse T-shape suspensions made out of gold. The thermal resistance includes radiation and gas conduction. $H=10\ \mu\text{m}$, $t=0.2\ \mu\text{m}$, $w=4\ \mu\text{m}$, and $W=20\ \mu\text{m}$. Other modeling parameters are shown in Table 3.2.

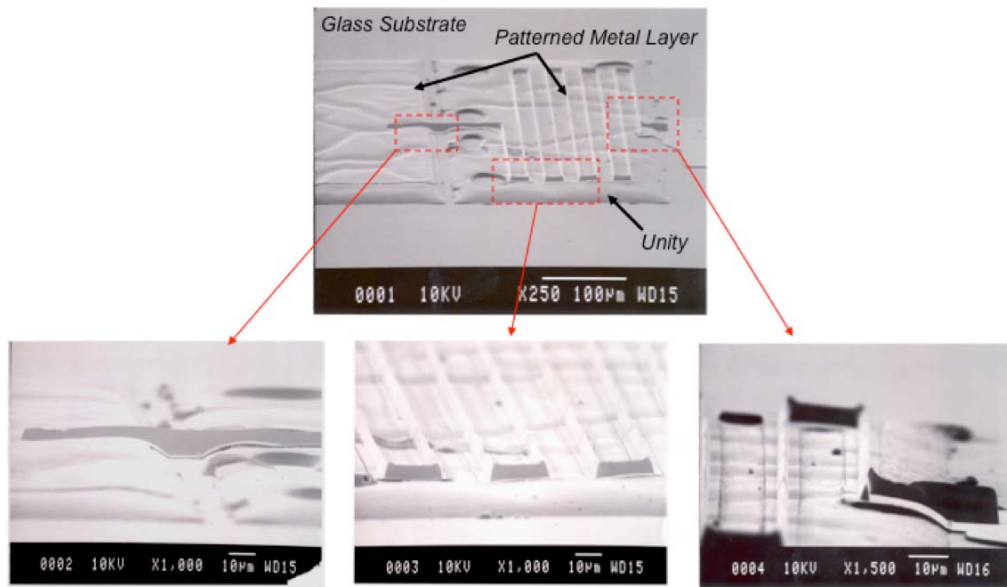


Figure 3.14 SEM views of the inverse T-shape isolation suspension made of thin film gold. Sacrificial layer of Unity™ is not removed.

Fabrication results

Figure 3.14 shows the inverse T-shape isolation suspension before release. The suspension is made of gold, and the sacrificial layer is Unity™. The suspension forms wavy shape because the sacrificial layer under the metal takes on this shape at elevated temperatures during the metal evaporation or sputtering.

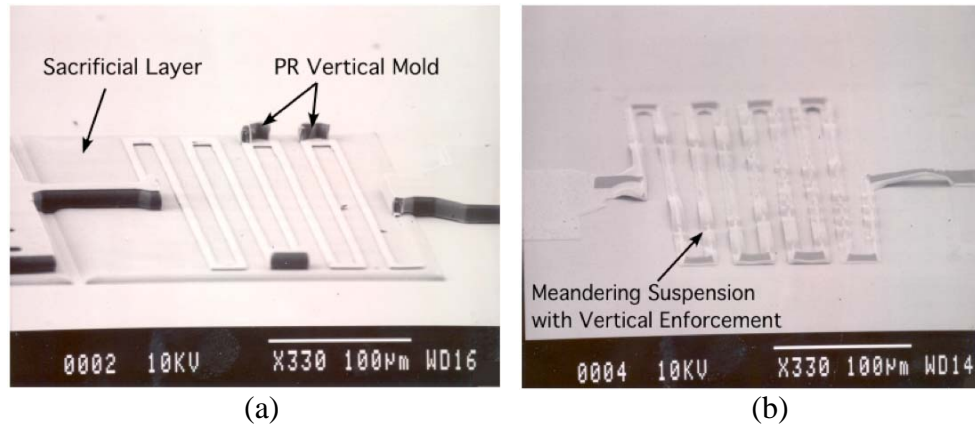


Figure 3.15 SEM views of inverse T-shape isolation suspension. (a) Vertical photoresist pattern is damaged, and (b) meandering suspension is stuck down to the substrate after removing the sacrificial layer of Unity™.

The inverse T-shape suspension design has issues in patterning the vertical photoresist mold and releasing the structure (Figure 3.15). The vertical photoresist mold on the bottom suspension layer suffers damage during process (Figure 3.15 (a)). Even with the vertical structure, some portions of the suspension are stuck down to the substrate after release. The release process is done by thermal decomposition of Unity™ at 270 °C. At that temperature, the suspension may lose its mechanical stiffness, so that it collapses down to the substrate.

3.2.3 Electroplated Metal Suspension

Suspension modeling

Electroplated nickel has been investigated as the suspension material to resolve the stress and stiction issues involved in fabricating the thin film metal suspensions. As described earlier, the thin film suspensions with plane shape or enforced shapes are challenging to pattern and release. Using evaporation or sputtering, it is also difficult to obtain thicker structures, which will enhance the stiffness. Nickel has a high Young's modulus and a low thermal conductivity. These mechanical and thermal characteristics are advantageous as compared to most metals. Furthermore, using electroplating, significantly thicker metal layer can be obtained with much lower residual stress.

Figure 3.16 illustrates a process flow for the electroplated metal suspension. The seed layer of Cr/Au is covered after patterning the sacrificial layer of Unity™ (Figure 3.16 (a-b)). A thick photoresist is used as electroplating mold (Figure 3.16 (c)). After the electroplating step, the photoresist mold and seed layer are removed (Figure 3.16 (d-e)). MEMS devices are then transferred on the suspensions. Finally, the sacrificial layer is removed to release the structure (Figure 3.16 (f)).

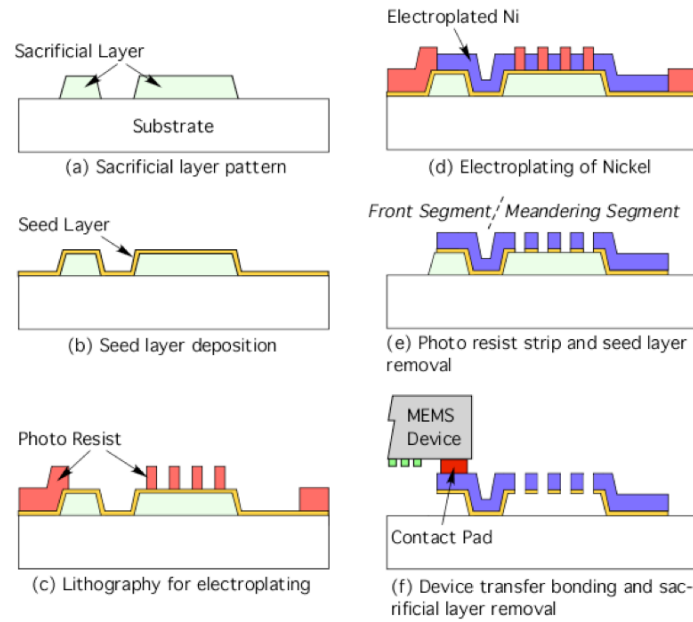


Figure 3.16 Process flow of the electroplated metal suspension.

Figure 3.17 shows thermal and mechanical simulation results of the package utilizing electroplated nickel suspensions. The thermal resistance of the electroplated suspension is smaller than that of the thin film suspension because the thickness of the electroplated suspensions has increased. With this material and thickness, to achieve less than 10 mW of power consumption over $\Delta T = 130\text{ }^{\circ}\text{C}$, the length of the meandering segment would need to be $>5\text{ mm}$. This results in a spring constant that is 10 times larger than that of the inverse T-shape suspension.

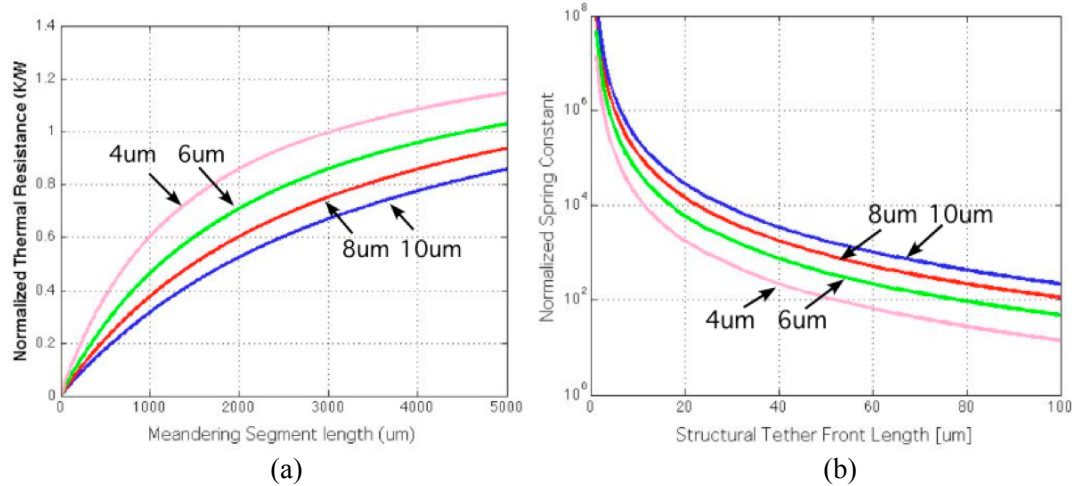


Figure 3.17 Simulation results of (a) normalized thermal resistance and (b) normalized spring constant of the electroplated nickel suspensions with varying the suspension thickness. The thermal resistance includes radiation and gas conduction. Modeling parameters are shown in Table 3.2.

Fabrication results

Figure 3.18 shows electroplated nickel suspension after the sacrificial layer removal. This suspension has a thickness of $\sim 8 \mu\text{m}$, and is suspended over the substrate by $\sim 4 \mu\text{m}$. Unity™ is used as the sacrificial layer, and it is thermally decomposed in a temperature oven at $270 \text{ }^\circ\text{C}$. Once again, the wavy shape of the suspension is from the waviness of the sacrificial layer under the suspension.

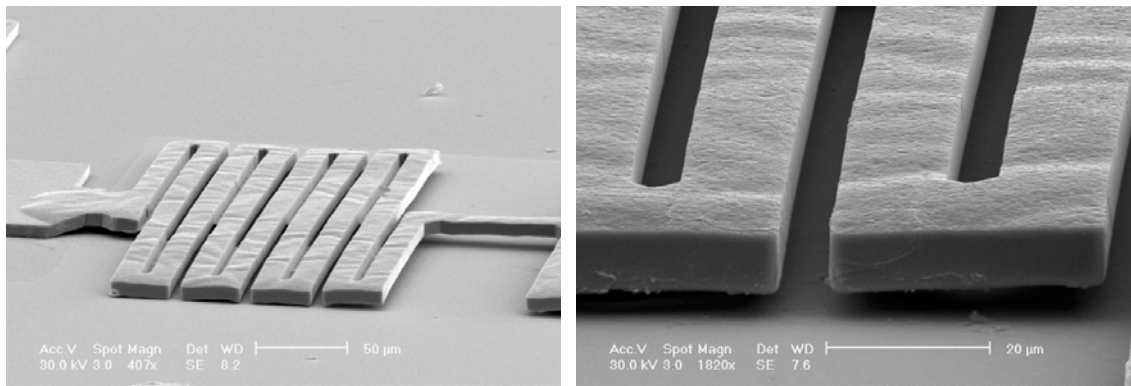


Figure 3.18 SEM view of the nickel electroplated suspension after sacrificial layer removal.

With the electroplated nickel, successful release has been demonstrated. The meandering segment is fully suspended over the substrate, and it does not show any bending due to residual stress.

3.3 Sacrificial Layers

To suspend the MEMS device, it is critical to remove the sacrificial layer under the connection pads and suspensions completely. This is typically done by either wet or dry etching. Using a wet process for releasing the structure is relatively easier and more cost effective than dry etching. However, it is undesirable to put a released MEMS device in wet chemicals, since this increases the chances of stiction and could alter the operation of the device. Therefore, dry release process is more suitable in our works.

Three types of sacrificial layers have been investigated: photoresist, polyimide, and Unity™.

3.3.1 Photoresist and Polyimide Sacrificial Layer

Photoresist is the simplest sacrificial layer since it is photo-patternable and can be removed by oxygen plasma etching (ashing). However, photoresist tends to outgas during subsequent high temperature processes such as soft baking and metal deposition. Figure 3.19 this photoresist sacrificial layer, which outgases during the soft bake step for patterning the isolation suspension. The outgassing has created large voids, which damaged the pattern in that area.

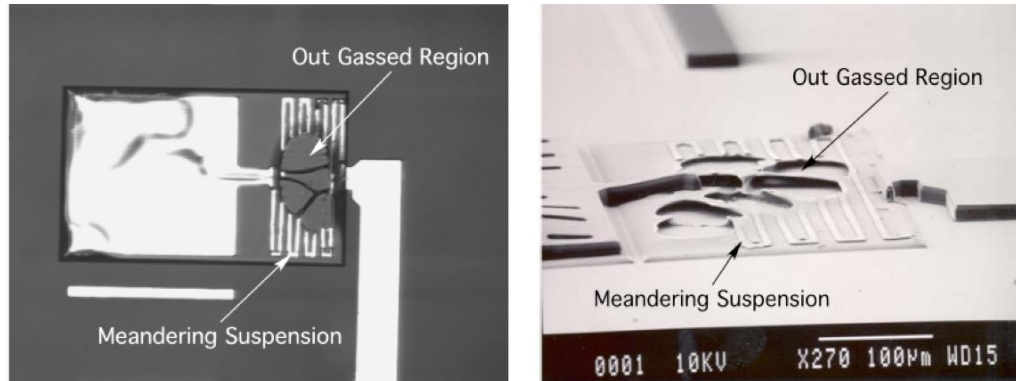


Figure 3.19 Pictures of photoresist sacrificial layer with meandering metal suspension. Outgassing has damaged the photoresist pattern causing large voids under the meandering suspension.

As compared to photoresist, polyimide is more stable at high temperature (up to ~ 400 °C) once it is cured, and is dry etchable. Photodefineable Polyimide is also available, but it is typically for thin layer patterning. A thick layer (6-8 µm) of non-photodefineable Polyimide (PI-2611, HD Microsystems™) is spin coated on a glass substrate with an adhesion promoter (VM651, diluted to 0.1% in DI water, HD Microsystems™). Soft bake is then done at 110 °C for 3 min on a hot plate to remove solvents and other outgassing species. It is then cured at 350 °C for 30 min in nitrogen environment. The cured Polyimide is then patterned by dry etching with aluminum and photoresist etch mask. Dry etch conditions are O₂ at 85 sccm, CF₄ at 15 sccm, pressure at 250 mTorr, and a 100W power. Metal isolation suspensions are then defined on the Polyimide sacrificial layer.

The sacrificial polyimide should be etched away to release the device structure. This should be isotropic undercut etch (horizontal etching), because the sacrificial polyimide layer is under the device and suspension elements. Figure 3.20 is the view through the glass substrate after dry release etching. The etching conditions are O₂ at 85 sccm, CF₄ at 15 sccm, pressure at 350 mTorr, and a 200W power. Chamber pressure

during dry etching has been increased to promote horizontal etching. It is typically difficult to achieve isotropic etching characteristics using plasma-assisted etching even with high pressure and low power. Half of the polyimide layer is left under the suspension, and most of the layer under the contact pad is not etched away after 2 hours of etching. The horizontal etching rate has decreased as the undercut depth has increased, because the etching gas has a harder time reacting with the Polyimide. At some point, the horizontal undercut etching ceases, and the remaining polyimide is unable to be removed completely.

Excessively long dry etching is undesirable, because it causes physical damage on the surface of the suspension or the transferred device. Over heating due to long exposure of plasma could induce burning of the polyimide.

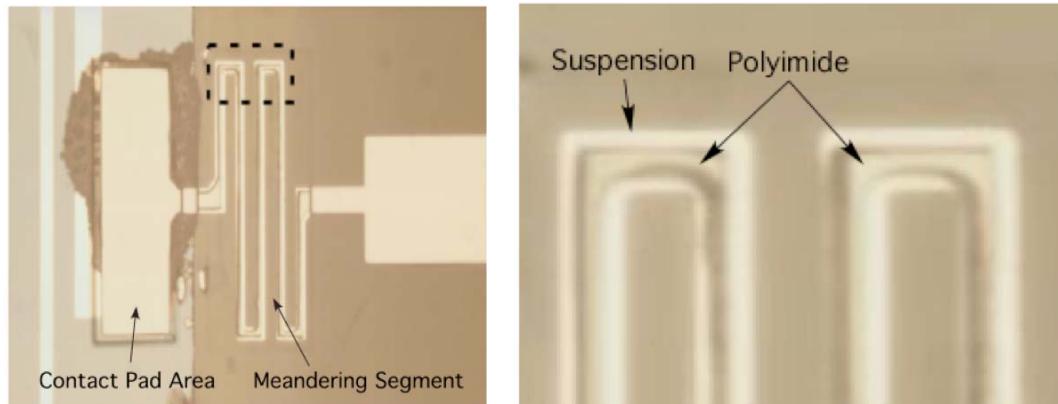


Figure 3.20 View from the back side (through glass substrate) after oxygen plasma etch for the polyimide sacrificial layer removal. The width of the meandering suspension is 20 μm .

3.3.2 Thermally Decomposing Sacrificial Layer: Unity™

Thermally decomposable material called Unity™ (Promerus LLC, Brecksville, OH, USA) has been investigated as the sacrificial layer. As shown in Section 3.3.1, it is difficult to etch a photoresist or Polyimide sacrificial layer away completely using lateral

dry etching. Unity™ undergoes thermal decomposition into gases at high temperatures. As a result, wet or dry etching is not needed to remove the sacrificial layer. In previous applications, it has been used as a sacrificial layer to form a cavity in a wafer-level vacuum package [81, 145].

Unity™ is spin coated on a bare glass substrate, and then patterned by oxygen plasma etching using a masking material of Ti or Cr/Au. After completing all the post processes including isolation suspension fabrication and chip transfer, the platform substrate is placed vertically in an oven, and heated up to 270 °C with a nitrogen atmosphere. It is critical to heat or cool the sample at a slow ramping rate as shown in the oven temperature profile (Figure 3.21). Rapid heating or cooling may leave polymeric residue behind.

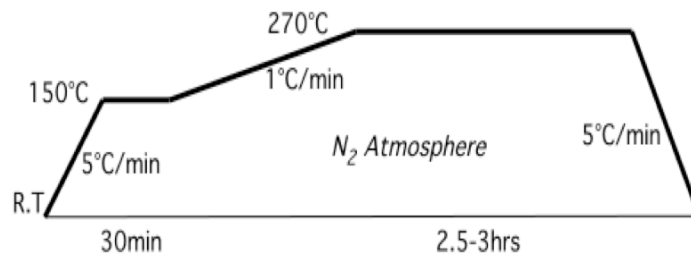


Figure 3.21 Oven temperature profile for the thermal decomposition of the Unity™.

Figure 3.22 shows released inverse T-shape and electroplated nickel isolation suspensions after the thermal decomposition of Unity™. Some parts of the inverse T-shape suspensions stick down to the substrate, because the metal beams possibly lose their stiffness at that high temperature. The stiction of the suspension is not desirable because most of the thermal loss would be through these stuck areas. In contrast to the T-shape suspension, the electroplated nickel suspension is completely suspended over the substrate.

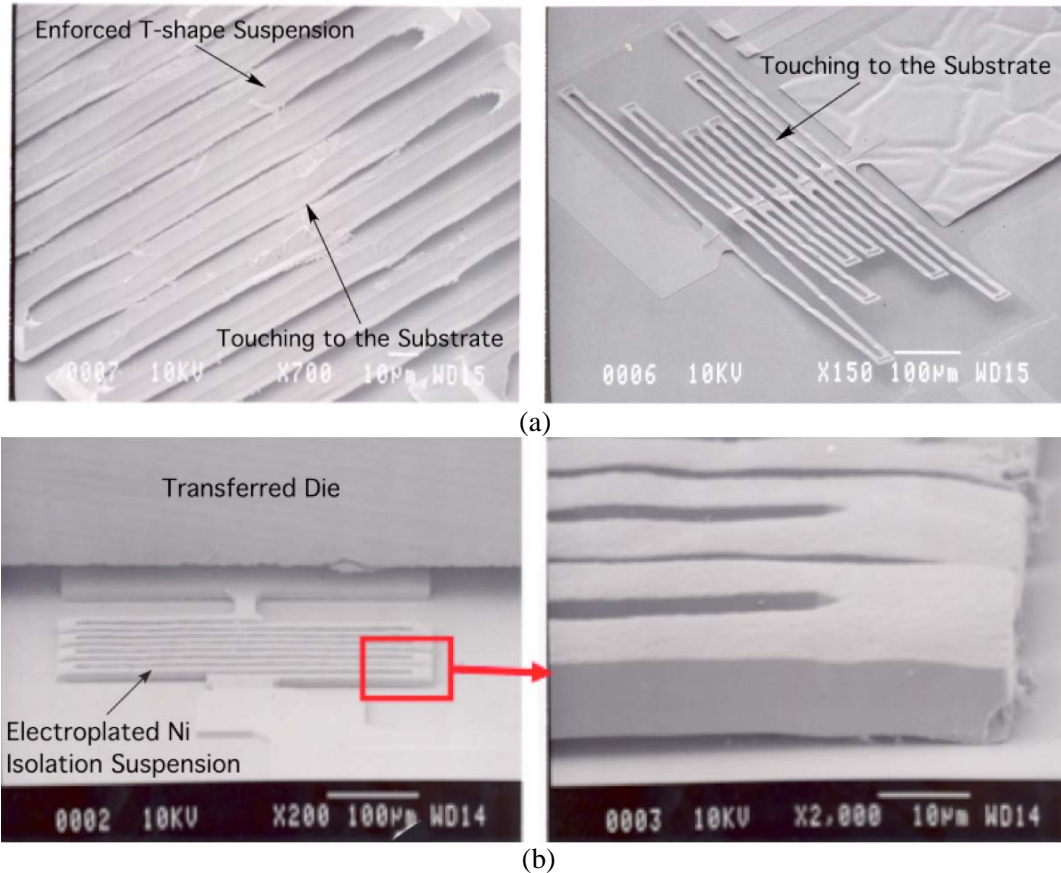


Figure 3.22 Released isolation suspensions after thermal decomposition of Unity™. (a) Inverse T-shape suspension, (b) electroplated nickel suspension.

Another issue in this process is the shrinkage and cracking of Unity™ during the post processes (Figure 3.23). It is a similar problem to the one explained in section 3.3.1, where a photoresist sacrificial layer is used. As in that case, this causes a wavy shape in the suspension. In particular, this occurs during metal layer evaporation or sputtering. To minimize this problem, the sacrificial layer should be exposed as little as possible during post process. Reducing the deposition rate during the metal evaporation can also help to resolve this issue.

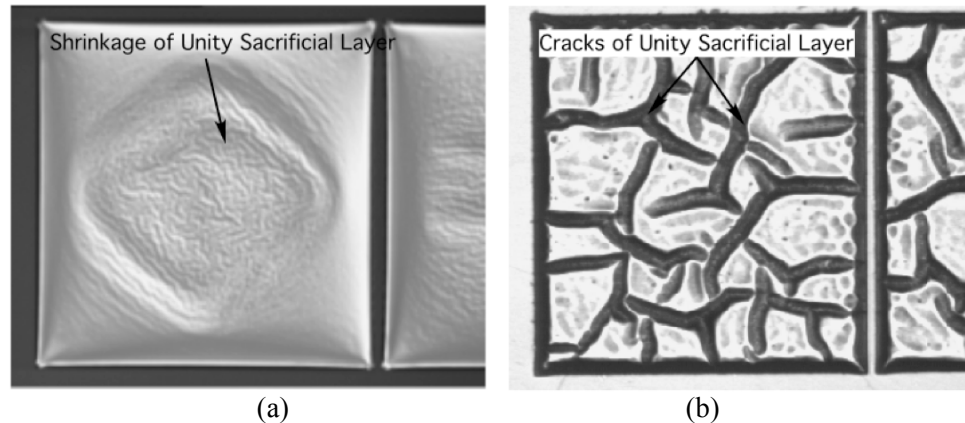


Figure 3.23 Picture of the Unity™ (Top views) (a) after oxygen plasma RIE for 45 min with etch mask of Ti (700 Å), and then (b) sputtering of Cr/Au seed layer for the nickel electroplating. The sacrificial layer suffers shrinkage and cracking of the surface during the processes with elevated temperature.

3.4 MEMS Device Transfer

3.4.1 Wafer-level Device Transfer Technique

As introduced in section 2.3.3.1, the wafer-level device transfer technique has been investigated. In this process, the device wafer and the platform wafer are bonded at the wafer-level, and the devices are singulated using DRIE. Advantages of this technique are: the devices can be assembled with accurate alignment (<20 μm tolerance) by the wafer-level aligning; all the devices are batch transferred at a time; this generic assembly approach for device integration enables its broad and cost-effective application.

First, the glass platform wafer including the isolation suspensions and the device wafer including MEMS devices are prepared separately as shown in Figure 3.24.

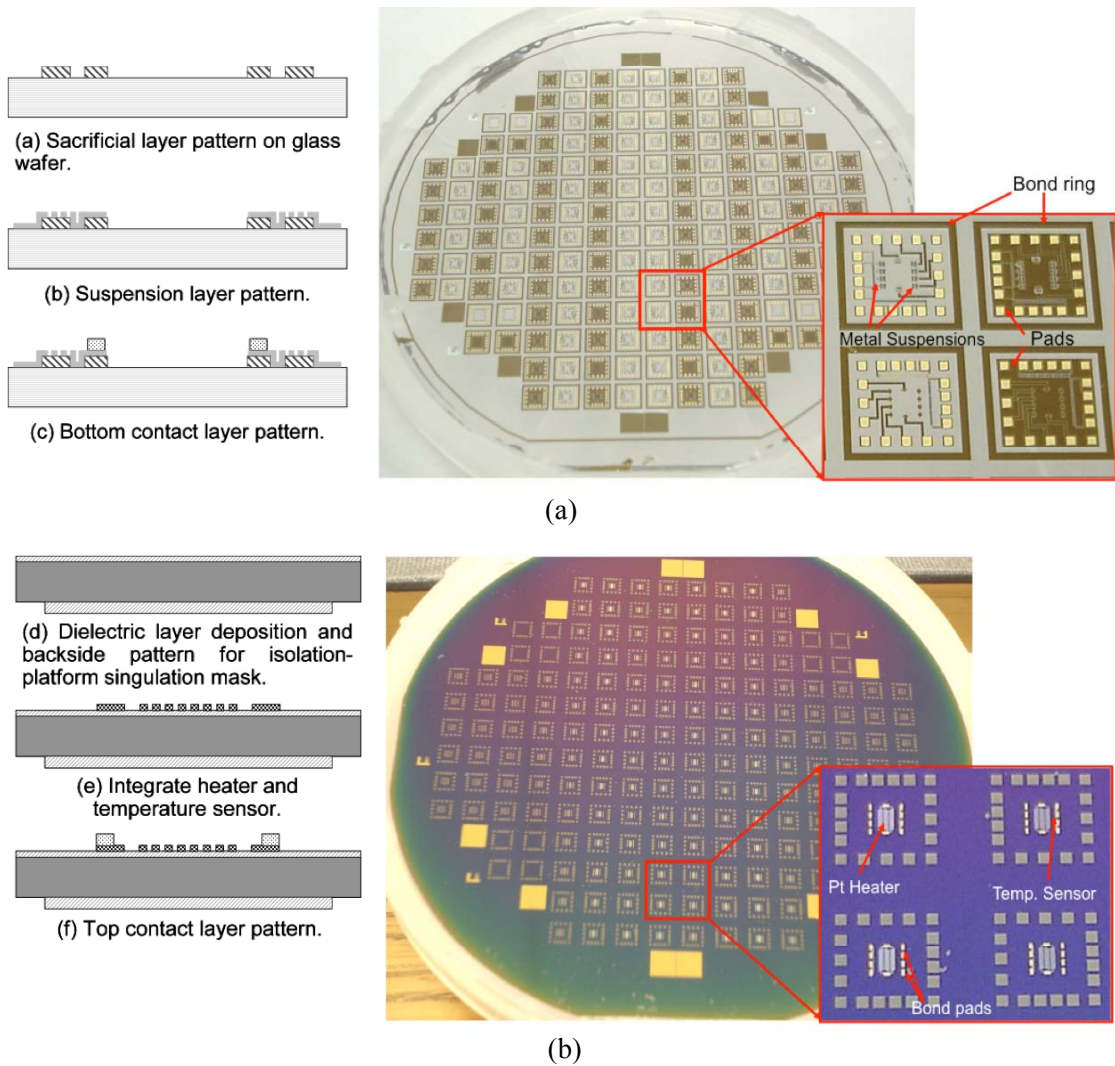


Figure 3.24 Wafer-level views of (a) glass platform wafer with isolation suspensions and (b) device wafer. Temperature sensor and heater are formed on the device part for a thermal characteristics measurement. On each side, bond pads made out of gold are patterned for Au-Au thermocompression bonding.

Suitable contact materials are patterned on each side. Two bonding techniques have been used: Au-Au thermocompression bonding; and In-Au TLP (Transient Liquid Phase) bonding. For the Au-Au thermocompression bonding, evaporated gold contacts ($\sim 1 \mu\text{m}$ thickness) are patterned on each pad. For the In-Au TLP bonding, indium contacts are patterned on the device wafer and gold contacts are patterned on the platform

wafer. The backside of the device wafer is patterned with a PECVD oxide layer as an etch mask during the die singulation using DRIE to etch the silicon.

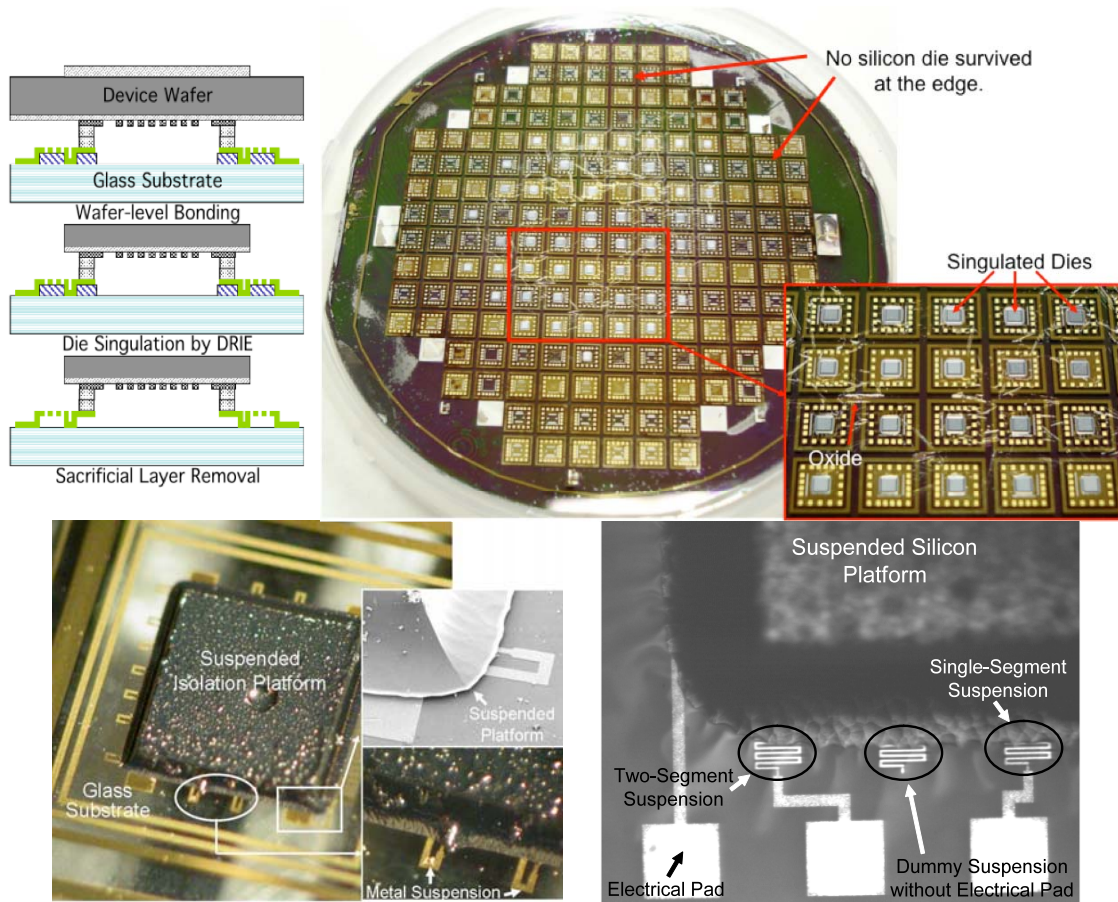


Figure 3.25 Wafer-level views after the device transfer and singulation processes. Au-Au thermocompression bonding is used for the die attachment.

These two wafers are then aligned and bonded at the wafer-level by a commercial wafer-bonding tool. The dies are then separated physically by silicon DRIE from the backside of the device wafer. A precise timed-etch is required to protect the bottom substrate from the plasma etch at the end of the etching process. Figure 3.25 shows photographs of the fabricated wafer after device singulation. The surface of the transferred die is rough because it is thinned during the DRIE step. The thickness of the transferred die can be adjusted by changing the thickness of the PECVD oxide mask. As

soon as the oxide layer is etched away during the DRIE, the thickness of the device starts to decrease. The gap between the device and the glass substrate is 6-8 μm defined by the sacrificial layer. The suspension metal is 1 μm of evaporated gold, and a Au-Au compression bond at 400 $^{\circ}\text{C}$ is used to transfer the device die to the isolation glass wafer.

3.4.2 Issue in Wafer-level Transfer Bonding

The wafer-level transfer bonding involves the transferring of all of the individual chips onto the suspensions at the same time. As shown in Figure 3.25 in previous section, not all the dies survived after the DRIE step (~30% survived). There are two causes for this problem: first, wafer-level bonding is not uniform across the wafer, and second, the sacrificial layer or suspension metal is not hard enough to endure the bonding force at high temperature.

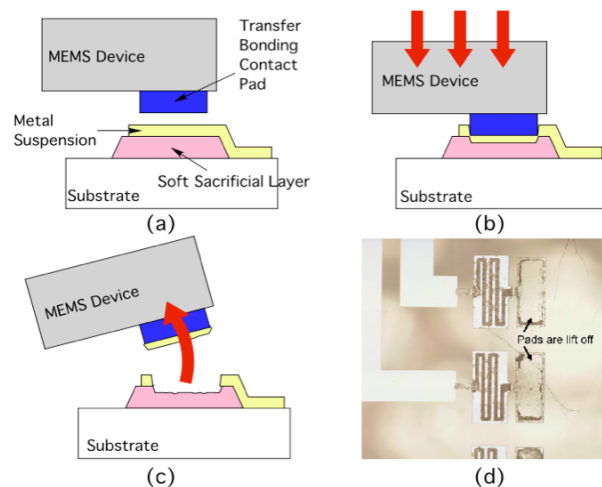


Figure 3.26 (a-c) Schematic illustrations for the mechanism of the suspension damage during the transfer bonding. (d) Picture of the damaged suspension after the device transfer process.

Figure 3.26 illustrates how the suspension metal and sacrificial layer are damaged, and how the transferred dies are detached after the bonding step using this

technique. As mentioned earlier, two types of contact bonding have been applied: Au-Au thermocompression bonding, and In-Au TLP bonding. These bonding techniques are done at high temperatures (300-400 °C) and high bonding pressures (500-1000 Torr). Under these conditions, the sacrificial layer is softened and does not effectively support the bonding pressure causing the damage around the contact pads (Figure 3.26 (b)). The damaged section does not hold the transferred device. To avoid this issue, harder sacrificial material or thicker metal suspension should be used. Other bonding types using lower temperature and lower pressures also help to resolve this issue.

3.5 Vertical Feedthroughs on Glass Wafer

Figure 3.27 illustrates the process flow for the vertical feedthrough fabrication on a glass wafer. This was first developed by Chae *et. al.* [134, 135], and modified for our applications. Electroplated nickel plugs are first patterned on the glass wafer to prevent gas leakage through the feedthroughs (Figure 3.27 (a)). After the post-process steps, including isolation suspension fabrication, device transfer, and wafer-level vacuum encapsulation, the glass substrate is thinned down to ~100 μm by HF wet etching (Figure 3.27 (b)). Via holes are then patterned by another HF wet etching (Figure 3.27 (c)). Cr/Au/Photoresist etch mask is used for this wet etching. After via formation, a gold metal layer is filled inside the vertical feedthrough hole (Figure 3.27 (d)).

Low cost vertical feedthroughs can be realized with this technique, since they are achieved using wet processing at the wafer-level. However, as shown in Figure 3.27 (d), the thin glass can be deflected inward due to the pressure difference, especially for large package sizes.

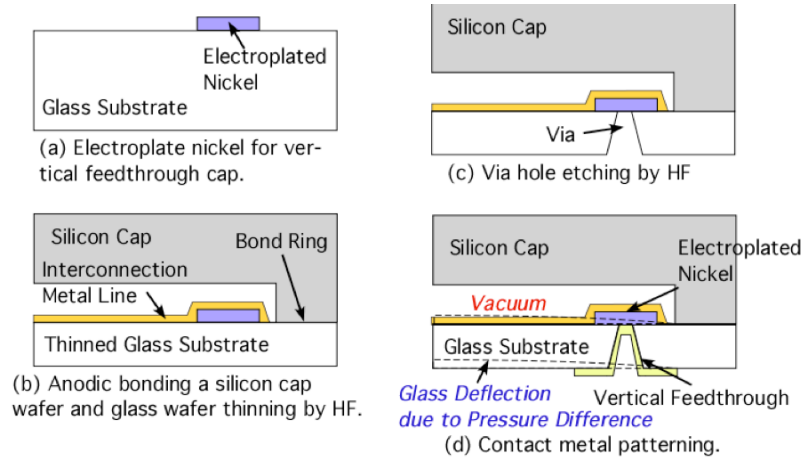


Figure 3.27 Process flow of vertical feedthroughs on the thin glass substrate using wet etching.

Figure 3.28 shows surface profile views observed by the non-contact optical surface profiler, Zygo NewView 5000™. The package dimension in this picture is 5 mm by 5 mm, and glass thickness is $\sim 100 \mu\text{m}$. A total 18 vertical feedthroughs are integrated in each package. The glass is deflected inward by $\sim 2.5 \mu\text{m}$ due to the pressure difference. The amount of deflection depends on the thickness of glass, the size of the footprint, and the vacuum level in the cavity. This deflection may cause touching of the glass substrate to the suspensions and the transferred device, which will increase thermal loss during oven-control or damage the device. The deflection of the package also results in a residual stress, which may cause unwanted effects on the performance of the packaged device.

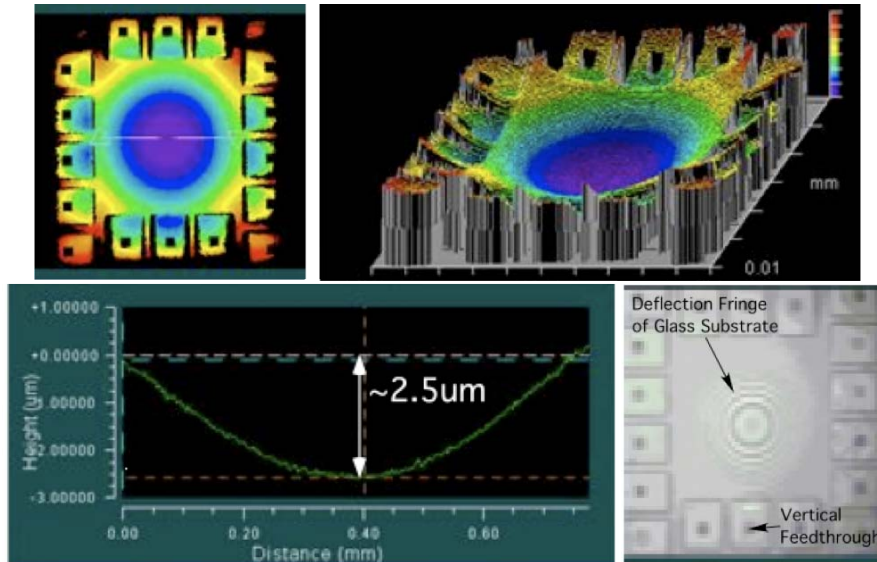


Figure 3.28 Zygo measurement of the vacuum encapsulated package die. The thin glass substrate is deflected inside due to the pressure difference.

This issue can be resolved by using thicker glass. However, using a thicker glass wafer and conventional wet etching process, the long etching times cause peeling-off of the etch mask. Furthermore, using a thicker glass wafer increases the size of the feedthroughs, because wet etching is an isotropic process.

3.6 Thermal Resistance of the Package

3.6.1 Test Platform Fabrication

A thermal isolation platform has been fabricated in order to measure the package thermal resistance (Figure 3.29). The thermal resistance can be obtained by measuring the power consumption for heating up the suspended device to a certain temperature. As the thermal resistance increases, smaller amount of power is required to heat a given thermal mass. Thermal test chips with a heater and temperature sensor have been fabricated and transferred onto the isolation suspensions for this task. The heater and

temperature sensor are made out of thin film gold, and has resistances of $\sim 100 \Omega$ and $1 \text{ k}\Omega$ respectively. The thin film metal heater or sensor can be simply integrated, and show good linearity. The test die is attached on the isolation suspension using silver epoxy at the die-level. The isolation suspension is made of electroplated nickel, and the sacrificial layer for releasing the structure is Unity™. The sacrificial layer is thermally decomposed at $270 \text{ }^\circ\text{C}$, in a nitrogen atmosphere.

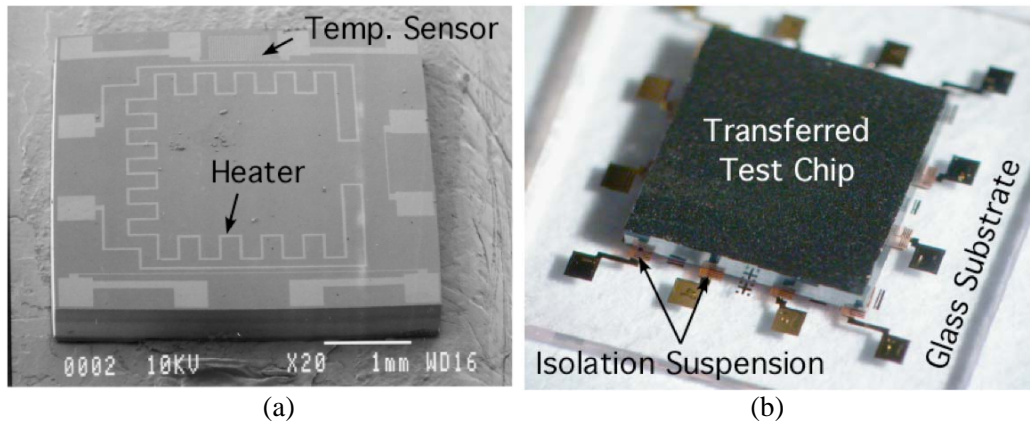


Figure 3.29 (a) SEM picture of the thermal test chip with heater and temperature sensor, and (b) picture of the thermal test platform for measuring thermal resistance. The thermal test chip is transferred on the meandering isolation suspensions made out of electroplated nickel.

Table 3.3 summarizes the design parameters of the isolation platform and test chip for measuring the thermal resistance.

Table 3.3 Design parameters of the isolation package for thermal resistance measurement.

Design Parameter	Value
Dimension of test die	$4.5 \text{ mm} \times 4.5 \text{ mm} \times 0.5 \text{ mm}$ Silicon
Total number of suspension	12 EA (4 two-segment suspensions)
Suspended gap	$5\text{-}8 \mu\text{m}$
Suspension thickness	$8 \mu\text{m}$, Electroplated Ni
Front segment width	$20 \mu\text{m}$
Meandering segment width	$10 \mu\text{m}$
Front touching area	$20 \mu\text{m} \times 10 \mu\text{m}$
Sacrificial layer	Unity™

Figure 3.30 shows SEM views of the fabricated isolation package without encapsulation. The chip includes the heater and temperature sensor for the thermal resistance measurement, and is transferred onto the nickel electroplated suspension using conductive paste at the die-level. The chip and suspensions are fully suspended by $\sim 8 \mu\text{m}$ over the glass substrate after the thermal decomposition of Unity™.

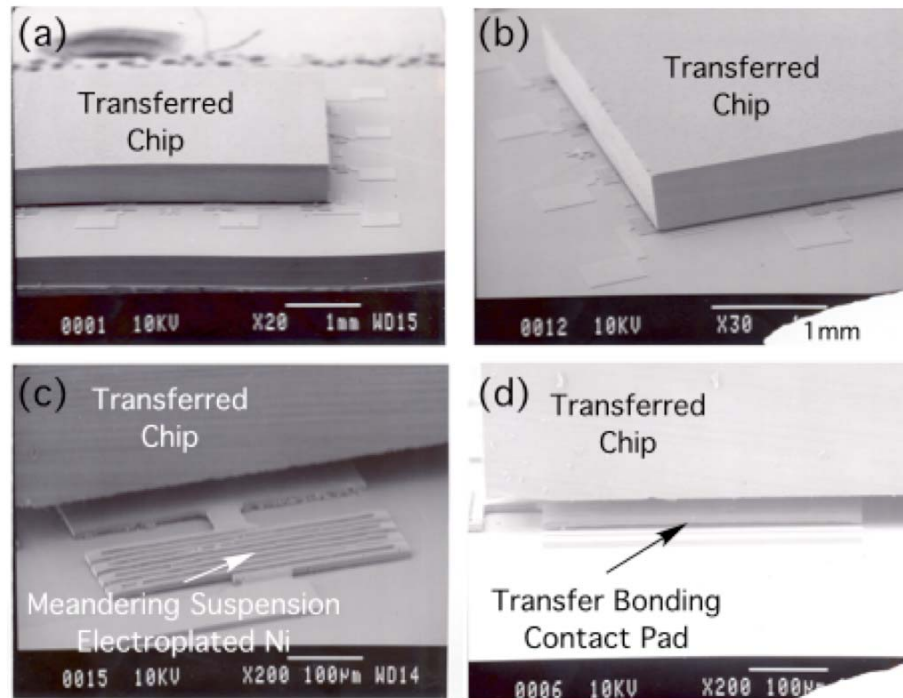


Figure 3.30 SEM views of the thermal test platform. The electroplated nickel isolation suspensions support the chip above the glass substrate.

3.6.2 Thermal Resistance Measurement Results

Figure 3.31 shows the connections of the test chip to the package. One current source applies a current across the heater, while another current source applies a current across the temperature sensor. A multimeter measures the voltage across the temperature sensor in a four-point probe configuration. The current sources that apply current to the heater and the temperature sensor are controlled through a computer and National

Instruments GPIB (General Purpose Interface Board) ports. A range of currents is swept through the heater where the power generated by the heater is recorded. While the heater current is swept, using a four-point probe with a constant current, the resistance of the sensor is recorded. This creates a resistance change vs. input heater power plot. From this data, the thermal resistance can be extrapolated. The resistance of the sensor is measured every 125 milliseconds for a period of 4 minutes, and it can be converted into temperature using TCR (Temperature Coefficient of Resistance) of the temperature sensor.

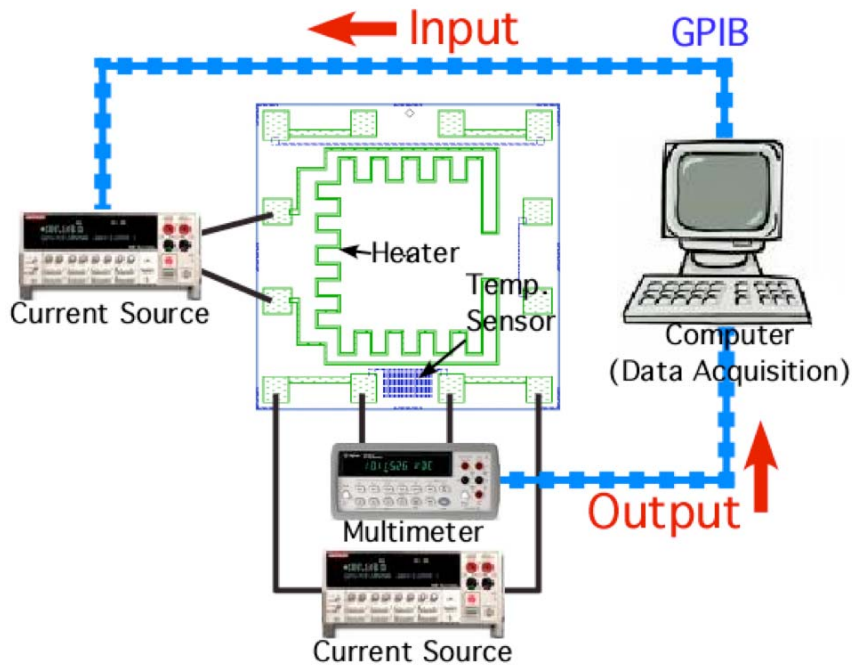


Figure 3.31 Schematic test setup for measuring the thermal resistance of the thermal platform.

Figure 3.32 shows results of the thermal resistance measurement. It shows the power used to heat the test chip to a certain temperature (over temperature from a reference temperature), and the slope of this data is the thermal resistance. This thermal resistance measurement is taken in a vacuum chamber (<1 mTorr), and performed before

and after the sacrificial layer removal. After thermal decomposition of the Unity™ sacrificial layer, the thermal resistance increases by around 10 times. This demonstrates that the heat loss through the sacrificial layer is very large, and shows why it is critical to release all of the structure to minimize power consumption. As illustrated in Figure 3.32 (b), the measured thermal resistance of 3580 K/W corresponds to a ~ 36 mW power consumption for oven control with $\Delta T = 130\text{ }^{\circ}\text{C}$.

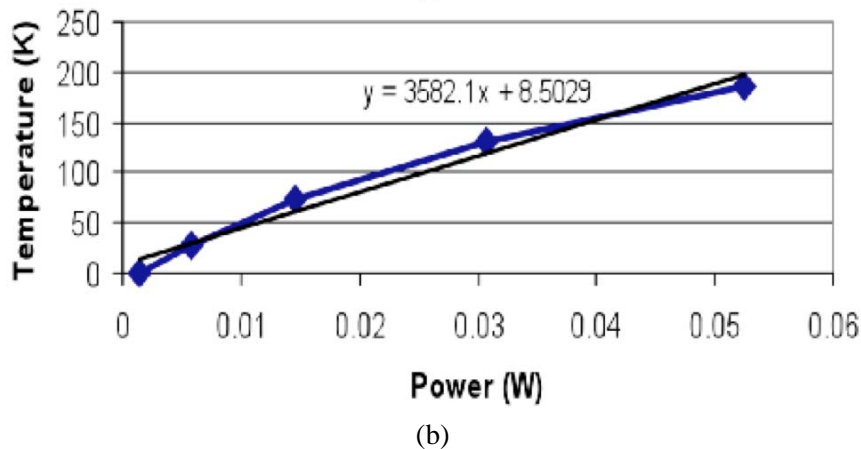
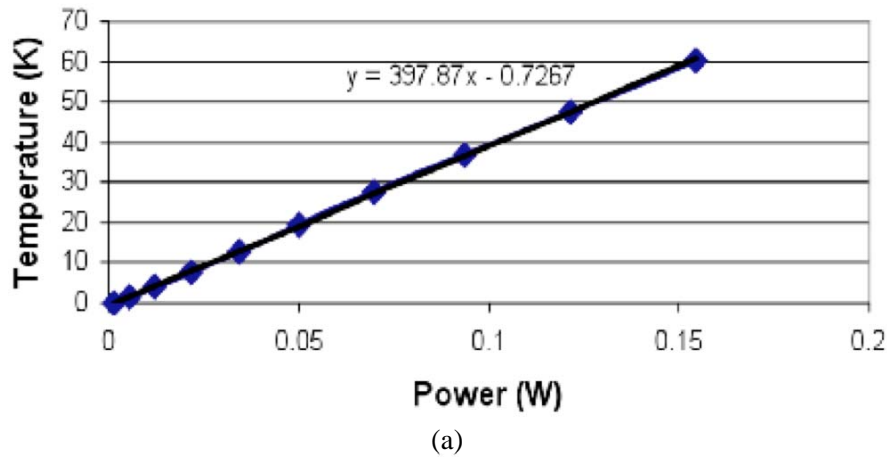


Figure 3.32 Thermal resistance measurement results: (a) before releasing the thermal platform (397.87 K/W) and (b) after releasing the thermal platform (3582.1 K/W).

This test has been done without anti-radiation layer, so it does not take into account the radiation effect. A larger thermal resistance is expected when it is fully enclosed by the anti-radiation shield. The actual vacuum level in the complete vacuum

package will be different from that in the vacuum chamber that the thermal test has been done in. Therefore, more accurate testing is needed with a full package including vacuum encapsulation, feedthroughs, and an anti-radiation shield.

3.7 Summary

In Chapter 3, a new generic environment-resistant package employing meandering metal suspensions has been presented. The suspensions provide thermal isolation, mechanical isolation, and electrical signal paths. Various suspension designs have been investigated. A MEMS device is transferred onto the suspensions at the wafer- or die-level. Using this assembly technique, a wide range of MEMS devices can be packaged. The wafer-level hermetic/vacuum packaging with vertical feedthroughs allows for a controllable environment and cost-effective process.

In developing key processes including suspension fabrication, structure release, device assembly and vertical feedthrough, many process challenges have been observed. Table 3.4 summarizes the key challenges in each fabrication step. It should be noted that each process is correlated to each other.

Table 3.4 Summary of key challenges in developing the environment-resistant package technology.

Key Processes	Challenging Issues
Isolation suspensions	- Suspension bending from residual stress after release - Structure stiction after release - Sacrificial layer pattern
Structure release	- Sacrificial layer removal
Device transfer	- Transfer bonding strength/yield - Transfer bonding temperature and pressure
Vertical feedthroughs	- Glass deflection - Residual stress in package

This package has demonstrated high thermal resistance over wide environmental temperature ranges ($\Delta T = 130\text{ }^{\circ}\text{C}$) with less than 40 mW of power consumption. The new generic assembly approach for instrument-platform integration enables its broad and cost-effective application.

Chapter 4

Generic Environment-Resistant Package with Glass Suspension using Batch Die-level Device Transfer Technique

4.1 Introduction

In this chapter, we present and demonstrate a new environment-resistant MEMS package with thin glass isolation platform/suspensions. MEMS devices are fabricated separately, and they are integrated into the platform wafer using the newly developed “batch die-level transfer technique” to realize a generic packaging approach. This cross-platform package provides thermal/vibrational isolation using the glass isolation platform, and wafer-level vacuum encapsulation with vertical feedthroughs. By using the thin glass as the isolation platform/suspensions material instead of metal, we resolve many of the fabrication issues that occur from suspending the device using the metal suspensions (Chapter 3). Combining the glass platform and the batch transfer technique, MEMS devices can be suspended over the substrate without using any sacrificial layer. New vertical feedthroughs formed on a glass-silicon bonded wafer show more robustness than those made on the glass wafer. This vertical feedthrough technique enables direct flip-

chip assembly on a circuit board. Table 4.1 is a design comparison chart between the packages with metal suspensions and the packages with glass suspensions.

Table 4.1 Design parameters of the isolation package for thermal resistance measurement.

Design	Package with Metal Suspension (Chapter 3)	Package with Glass Suspension (Chapter 4)
Suspension materials	Thin film metal Electroplated metal	Thin glass
Interconnection	Suspension act as the interconnection	Separate interconnection
Sacrificial layer	Required	Not required
Substrate	Glass wafer	Thin glass-silicon bonded wafer
Transfer technique	Wafer-level transfer Die-level transfer	Batch Die-level Transfer
Transfer bonding restriction	Low temperature, low pressure required	Less restrictive
Vertical feedthroughs	Feedthroughs in glass	Feedthroughs in glass/silicon

In section 4.2, the design principles for the packages with the glass suspensions are presented. In section 4.3, the fabrication process is described in detail. The generic batch die transfer technique is also detailed in this section. Section 4.4 describes the test results and section 4.5 gives some concluding remarks.

4.2 Environment-Resistant Package Design

4.2.1 Package Design Overview

The proposed package provides environmental protection using a silicon-glass-silicon wafer-bonded structure as shown in Figure 4.1. It consists of three parts; (i) a silicon-glass bonded platform wafer with an isolation platform and feedthroughs, (ii) a transferred MEMS device, and (iii) a silicon cap wafer for final vacuum encapsulation.

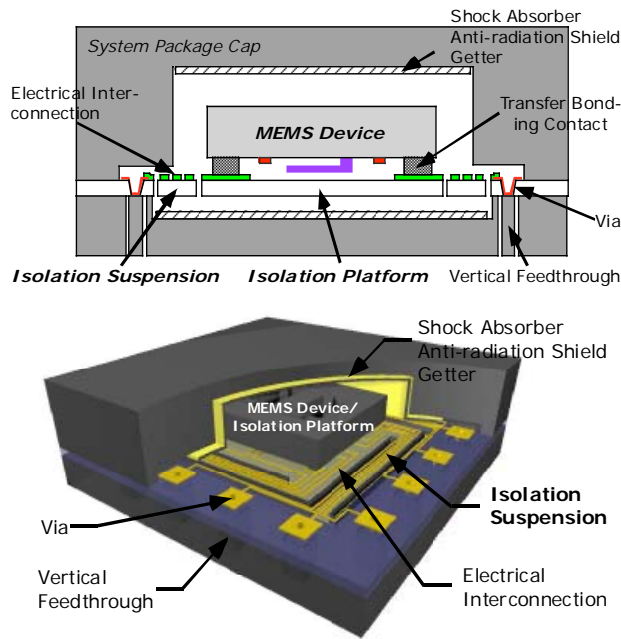


Figure 4.1 Schematic illustrations of the environment-resistant package with glass isolation platform/suspensions.

Using this approach, a MEMS device is flip-chip attached onto a glass isolation platform, which is in turn supported by crab-leg shaped glass suspensions over a shallow recess formed on a silicon support wafer. The MEMS chip is mechanically and electrically connected by metal bonding contacts, which are patterned on the isolation platform. Metal interconnection lines on the isolation suspension beams transfer electrical signals between the MEMS device and vertical feedthroughs. The packaged MEMS chip is oven-controlled for thermal stabilization by maintaining it at a temperature higher than the maximum environment temperature using a heater and temperature sensor. The heater and temperature sensor can be integrated either on the MEMS device or on the isolation platform. The heated structure is thermally isolated from the environment by the glass suspensions, anti-radiation shield, and vacuum encapsulation to minimize power dissipation. The isolation suspensions are designed with sufficient stiffness for mechanical support, and flexibility for rejecting

environmental vibrations. Encapsulation using a silicon cap wafer provides a vacuum environment inside the package cavity. Shock absorption layers [47, 49] for preventing damage from severe environmental shock, and a getter layer [146] for maintaining high vacuum are formed inside the package. Finally, the vertical silicon feedthroughs are formed by silicon DRIE from the backside of the platform substrate.

4.2.2 Isolation Suspension Design

The environment-resistant package is designed to provide thermal and vibration isolation utilizing oven-control of the device, isolation platform/suspensions, anti-radiation shield, vacuum environment, and shock absorption layer.

The packaged device is oven-controlled to eliminate performance drift due to temperature change. To minimize the necessary input power, the heated structure should be thermally isolated from the environment. As mentioned earlier in Chapter 2, vacuum encapsulation and an anti-radiation shield layer can minimize the heat loss through gas conduction and radiation respectively.

The glass isolation suspensions, which support the isolation platform and the MEMS device, should provide high thermal resistance by minimizing solid conduction. The heat is dissipated not only through the glass suspensions, but also through the metal interconnection lines patterned on the suspensions. Therefore the thermal resistance of the solid conduction, $R_{T,sol}$, is given by:

$$R_{th,sol} = \left(\left(\rho_{T, glass} \frac{L_{glass}}{A_{glass}} \right)^{-1} + \left(\rho_{T, metal} \frac{L_{metal}}{A_{metal}} \right)^{-1} \right)^{-1} = \frac{\rho_{T, glass} \rho_{T, metal} L}{\rho_{T, glass} A_{metal} + \rho_{T, metal} A_{glass}} \quad (4.1)$$

where, $\rho_{T, glass}$ and $\rho_{T, metal}$ are thermal resistivities of the glass and the interconnection metal respectively, L is the length of the suspension ($L_{glass} = L_{metal}$), and A is cross

sectional area [42]. The total thermal resistance can be obtained from Equation 2.15 in Chapter 2. To increase the thermal resistance, the length needs to be large, and the width and thickness need to be small. Figure 4.2 shows a MATLAB calculation with a model package. The device is assumed to be maintained at 80 °C, and other parameters for this analysis are shown in Table 4.2. In this model analysis, the power input necessary for heating the device is ~40 mW when the environment temperature is -50 °C, and decreases as the environment temperature increases.

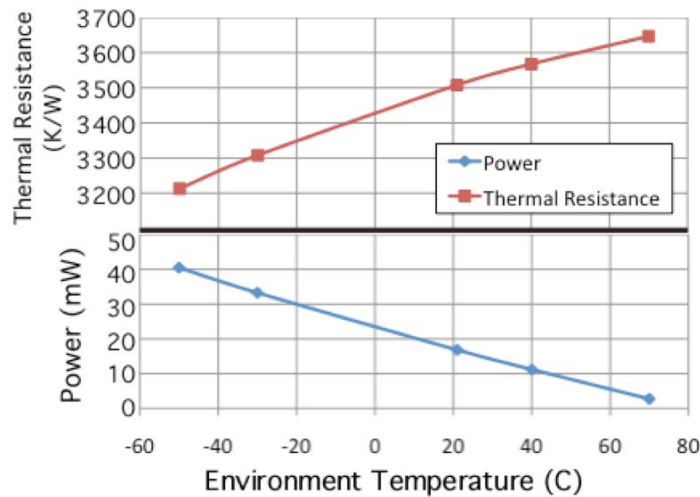


Figure 4.2 MATLAB[®] simulation results. (Top) Thermal resistance and (Bottom) power consumption versus environment temperature. The device is assumed to be heated at 80 °C.

Table 4.2 Summary of parameters for thermal analysis using MATLAB[®].

Parameters		Data
Device	Material	Silicon
	Size (L×w×t)	4.5×4.5×0.5 mm ³
Glass platform	Material	Glass
	Size (L×w×t)	Platform: 4.8×4.8×0.1 mm ³
		Suspension: 6×0.6×0.1 mm ³
Metal interconnection	Material	Gold
	Number	12
	Size (L×w×t)	6000×25×0.3 μm ³
Pressure	-	30 mTorr
Radiation	Emissivity	0.1
Oven-control	Device	80 °C
	Environment	-50 ~ +70 °C

As mentioned earlier, environmental vibration can be rejected by the flexible isolation suspensions. The vibration cut-off frequency, ω , can be obtained by [46, 144]:

$$\omega = \sqrt{\frac{k}{m}} = 2\sqrt{\frac{Ewt^3}{mL^3}} \quad (4.2)$$

where, k is the spring constant of the crab-leg shaped glass suspension structure, m is the total mass of the suspended MEMS chip and the isolation platform, E is Young's modulus of the suspension, w is width, t is thickness, and L is length. The suspension design is optimized to have both sufficient stiffness to support the platform and flexibility to reject high frequency vibration. The thin glass is a suitable material for satisfying these requirements, because glass has a relatively high Young's modulus (62.75 GPa) and a low thermal conductivity (1.13 W/m°C). It also can be batch processed by wet etching at the wafer-level.

The glass isolation suspension has been designed to have a cut-off frequency of ~1 kHz. Figure 4.3 shows modal analysis results using ANSYS®. The 1st mode is observed in vertical direction at ~993 Hz Figure 4.3 (b), and the 2nd and 3rd modes are in rotational direction at ~1910 Hz (Figure 4.3 (c)). Calculated spring constant in the vertical direction is 1230 N/m. The spring constant is large enough to support the platform structure. The vertical deflection due to the gravitational force is less than 0.3 μm. Simulation results are summarized in Table 4.3.

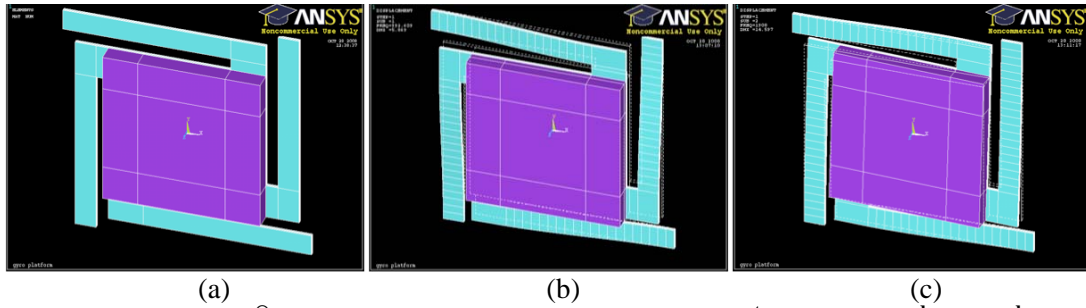


Figure 4.3 ANSYS® simulation results. (a) Modeling, (b) 1st mode, (c) 2nd and 3rd modes.

Table 4.3 Summary of ANSYS® simulation for mechanical analysis.

Parameters		Data
Device	Material	Silicon
	Size (L×w×t)	4.5×4.5×0.5 mm ³
Glass platform	Material	Glass
	Size (L×w×t)	Platform: 4.8×4.8×0.1 mm ³
		Suspension: 6×0.6×0.1 mm ³
Mechanical analysis	1 st mode	992.61 Hz
	2 nd mode	1908.2 Hz
	3 rd mode	1908.3 Hz
	4 th mode	21629 Hz
	Spring constant	1230 N/m

Shock absorption layers using thick soft metal layer (e.g., gold) can reduce the external shock [49]. This metal layer also functions as the anti-radiation shield layer.

4.3 Fabrication

Figure 4.4 shows the process flow and an exploded view of the package. The packaging process is independent of the MEMS device fabrication process. It is divided into three major steps; (i) preparation of the platform substrate (Figure 4.4 (a-e)), (ii) MEMS chip transfer/integration (Figure 4.4 (f)), (iii) final encapsulation and vertical feedthrough formation (Figure 4.4 (g)). Fabrication details for each of these steps are provided in sections 4.3.1, 4.3.2, and 4.3.3 respectively.

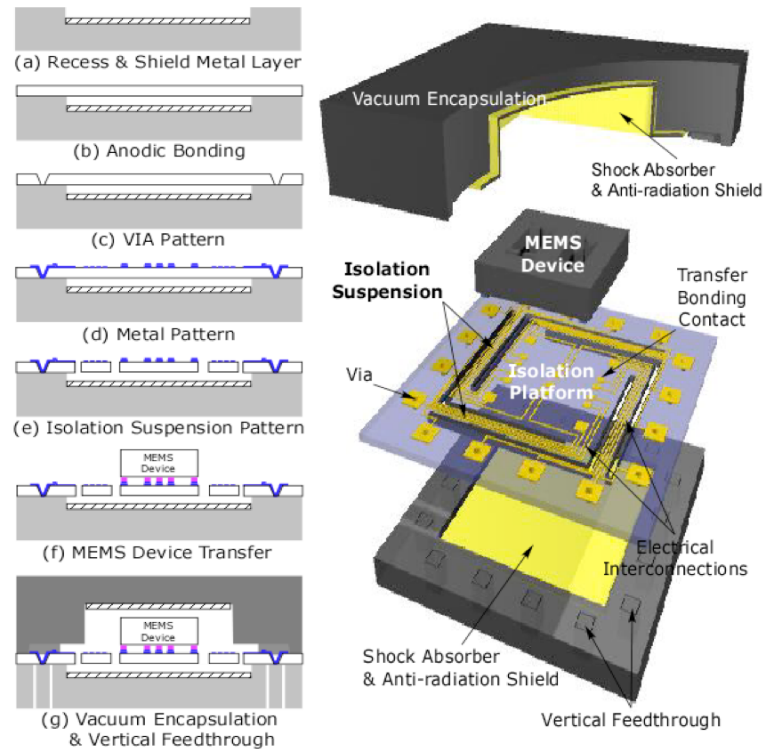


Figure 4.4 Fabrication procedure and exploded view of the environment-resistant package.

4.3.1 Platform Substrate Fabrication

The platform substrate provides thermal/mechanical isolation and signal feedthroughs. It consists of a 100 μm thick Pyrex 7740 glass wafer and a high-doped silicon wafer ($<0.01 \Omega\text{-cm}$). The thin glass wafer is patterned into the isolation platform/suspensions. The high-doped silicon wafer minimizes the electrical resistance of the feedthroughs.

A recess of $\sim 10 \mu\text{m}$ is first formed in the silicon wafer and is coated with a metal layer (Figure 4.4 (a)). The metal layer (e.g., gold) is for the anti-radiation shield and shock absorption [49].

The silicon wafer is then anodically bonded to the thin glass wafer at $350 \text{ }^\circ\text{C}$ / 400V using a SUSS MicroTec SB6e wafer bonder. It is necessary for the bonder

chamber to be over-pressurized ($P_{\text{bonder}} = T_{\text{bonding}}/T_{\text{R,T}} \cdot P_{\text{R,T}}$) during the bonding step. This prevents the pressure difference between the recessed cavity and the atmosphere after cooling down to room temperature. A low bonding voltage is also preferred to prevent stiction of the glass to the bottom of the recess due to the electrostatic force. The thin glass is robust in handling and processing, because the silicon wafer provides support (Figure 4.4 (b)).

Via holes for the electrical signal connection are formed by wet etching the glass with 49% HF solution (Figure 4.4 (c)). An evaporated Cr/Au (1000 Å/4000 Å) and AZ9260 thick photoresist are used for wet etching mask layers. Vias are then filled with a sputtered Ti/Au layer and patterned for electrical connections. The metal layer is conformally covered inside the via as shown in Figure 4.5.

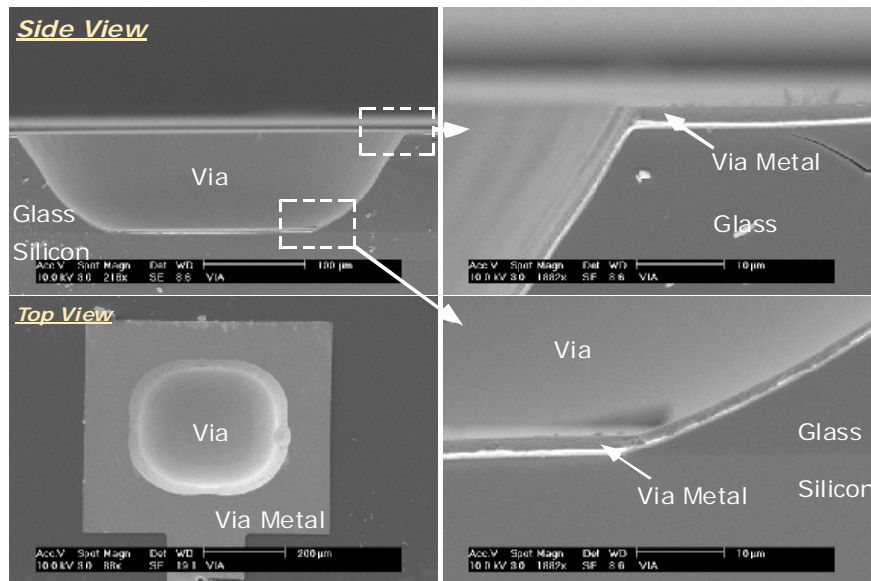


Figure 4.5 SEM views of via hole in the glass with metallization.

Once it is annealed at 360 °C for 30 min, ohmic metal-semiconductor contacts with < 2 ohm of contact resistance are obtained. Figure 4.6 is the I-V measurement data between two connected contacts before and after the annealing processes. The annealing

step can be skipped, because it experiences high temperature during the final vacuum encapsulation bonding.

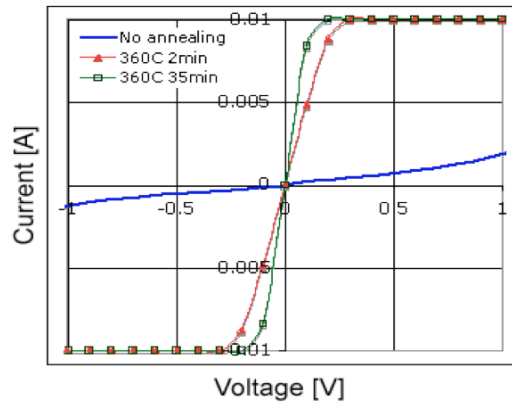


Figure 4.6 I-V curve of the via contacts. Two connected contacts are measured.

Metal interconnection lines and MEMS chip bonding pads ($\text{Ti/Au} = 300 \text{ \AA} / 3000 \text{ \AA}$) are then defined on the glass wafer (Figure 4.4 (d)). Next, isolation platform/suspensions are patterned by wet etching the glass with 49% HF (Figure 4.4 (e)). Sputtered Cr (4000 \AA) and AZ9260 photoresist (25 \mu m) are used for wet etching mask layers. The isotropic wet etching shows 1:1.2 of under-cut ratio. It should be noted that the metal interconnection pattern is not damaged during wet etching of the glass or stripping of the etch mask layer.

Figure 4.7 shows the fabricated platform substrate. Contact pads for MEMS device transfer bonding are patterned on the glass isolation platform, and interconnection lines connect these pads to the feedthroughs. The glass isolation platform is suspended over the substrate by $\sim 10 \text{ \mu m}$. The platform substrate is ready for the next device transfer step.

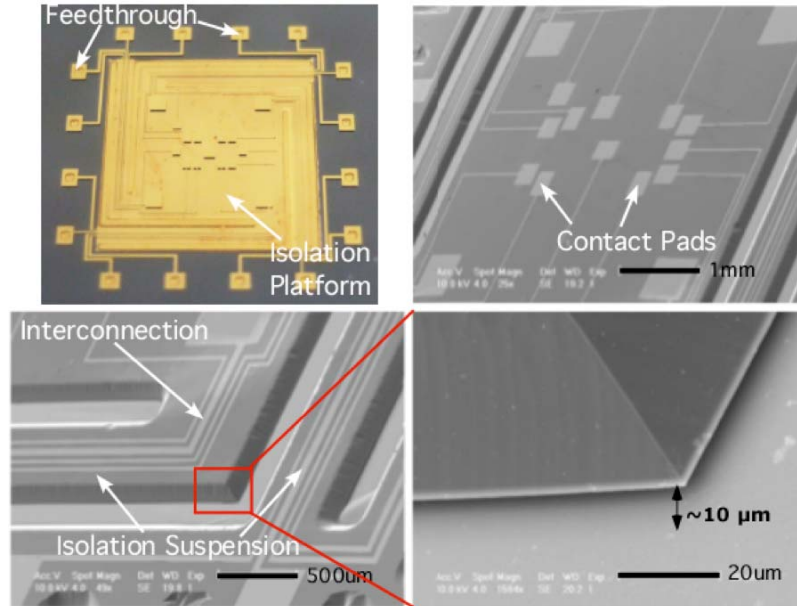


Figure 4.7 Pictures of the glass isolation platform and suspensions. Bonding contact pads for the device flip-chip transfer are formed on the glass platform. The platform is suspended over the substrate by $\sim 10 \mu\text{m}$.

4.3.1.1 Deep Glass Wet Etching

In this work, glass processing is one of the core challenges, and allows for creation of the vias, isolation platform, and isolation suspensions. Glass has high chemical resistance, high heat resistance, high electrical isolation, and optical transparency. However, it is challenging to make microstructures using glass due to the difficulty in precisely machining this material. There has been a lot of work to improve glass etching/machining techniques [147].

Glass can be processed using three major methods: micromachining, dry etching, and wet etching. Micromachining techniques including ultrasonic drilling [148], ECDM (Electro Chemical Discharge Machining) [95, 149], and sand blasting [150] have been used for perforating glass substrates. However, these techniques result in rough surfaces, and sometimes are not compatible with clean room processes. Dry etching [132, 133,

151] of glass allows for high aspect ratio etching, which is important in fabricating micro-channels. A drawback of dry etching is high process cost due to slow etch rates and serial processes. Wet etching is the most widely used process, because it is simple and cost-effective. However, it is difficult to obtain a high aspect ratio structure, because glass wet etching is an isotropic process. In many cases, there is also a limitation in etch depth, because the etchant (mostly HF-based solution) is so destructive that most masking materials cannot undergo long etch times.

Important factors in wet etching of glass are glass material properties, mask material, and surface condition. We have used 100 μm -thick Corning Pyrex 7740 glass wafer for the isolation platform/suspension layer. This substrate can be anodically bonded to a silicon wafer, and also shows constant etch rates in HF-based solution [147]. Various mask materials can be used including photoresist, Cr/Au, silicon [152] and silicon carbide [153]. Mask material selection depends on the etch depth and process compatibility. The Cr/Au/photoresist layer is commonly used for etching up to $\sim 100 \mu\text{m}$ depths.

The surface condition of glass is critical especially in deep wet etching. In our work, we pattern via holes and isolation platform/suspensions on the thin glass that is anodically bonded to the support silicon wafer. There is sodium segregation on the glass surface, because sodium ions move to the anode side during the anodic bonding. The surface with sodium segregation shows weak adhesion to the masking material.

Figure 4.8 shows an etch profile of 100 μm -thick Pyrex 7740 glass patterned by a 49% HF solution for 15 min. The etch mask is Cr/Au/photoresist with a thickness of 1000 \AA /4000 \AA /25 μm respectively. The sample is intentionally only partly anodic

bonded. Upper left portion contains segregated sodium on the surface due to the anodic bonding, and lower right portion does not. With the same etching condition, the sodium-segregated region shows a rough profile with a large amount of undercut etching.

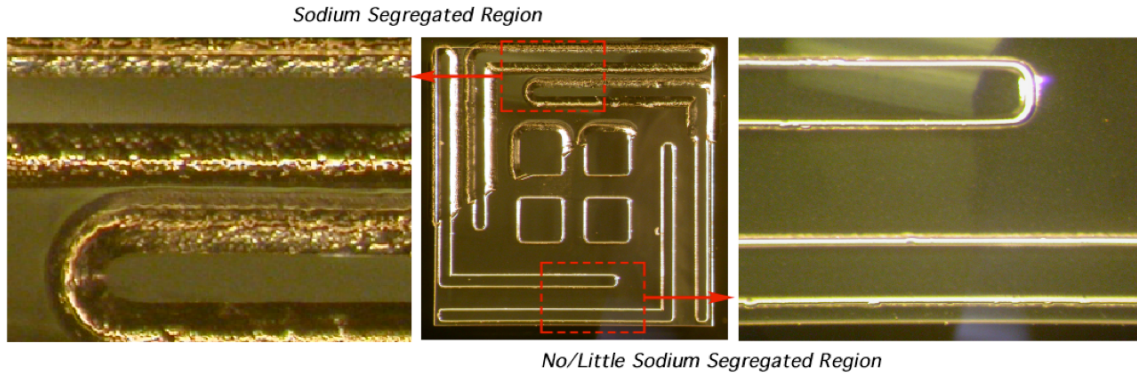


Figure 4.8 Glass etching profile difference with and without sodium segregation (100 μm -thick Pyrex 7740, 49% HF etching for ~ 15 min, masking material of Cr/Au/photoresist, 1000 \AA /4000 \AA /25 μm)

To resolve this issue we pre-etch the glass surface in BHF (Buffered Hydrofluoric) acid for 3-5 min. This pre-etch presumably removes the sodium segregation, and enhances the adhesion of the masking materials (Cr/Au/Photoresist). Figure 4.9 shows the glass etch profile with and without the BHF pre-etching. With the pre-etching, clean and smooth sidewalls have been obtained with an isotropy of 1:1.2. Instead of Cr/Au/photoresist mask, sputtered Cr/photoresist (4000 \AA /25 μm) also showed similar results.

Notching defects on the glass edge occur during glass etching with metal etch mask (Figure 4.9 (b)). These defects come from breaking of the metal masking layer due to its tensile stress, and can be reduced by using multiple layers of masking material such as Cr/Au/Cr/Au [147].

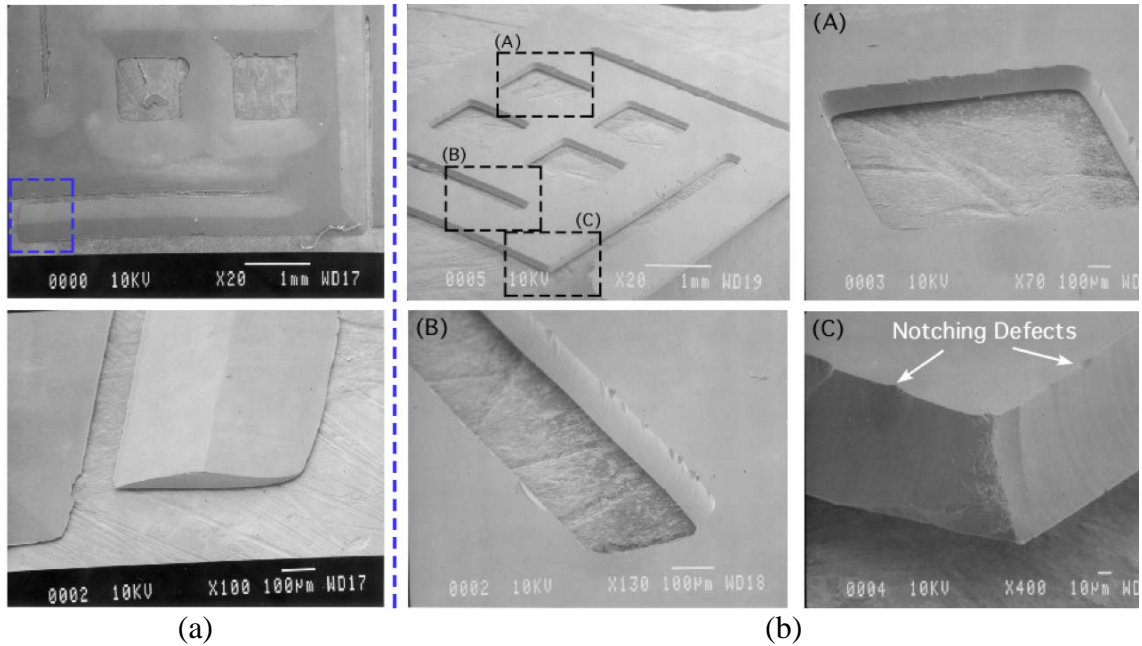


Figure 4.9 SEM views of etched glass (a) without and (b) with BHF pre-etching for 5 min before the deep glass wet etching. (100 μm -thick Pyrex 7740, 49% HF etching for \sim 15 min, masking material of Cr/Au/photoresist, 1000 \AA /4000 \AA /25 μm)

4.3.2 Generic Batch Die-level Transfer Technique

We have developed a new batch chip transfer technique for integrating MEMS devices on the isolation platform as introduced in section 2.3.3.2 in Chapter 2. This is a crucial step for realizing a generic packaging approach, because the MEMS device is separately fabricated and needs to be assembled into the package seamlessly. It has several requirements including: strong mechanical attachment, good electrical connection, high temperature stability, accurate alignment, and batch processes.

The generic batch die-level transfer technique consists of three steps (Figure 4.10): (i) selective contact metal deposition on the MEMS devices using a soft shadow mask, (ii) alignment of the devices with the isolation platform using a guide wafer, (iii) bonding of the devices for permanent mechanical and electrical attachment.

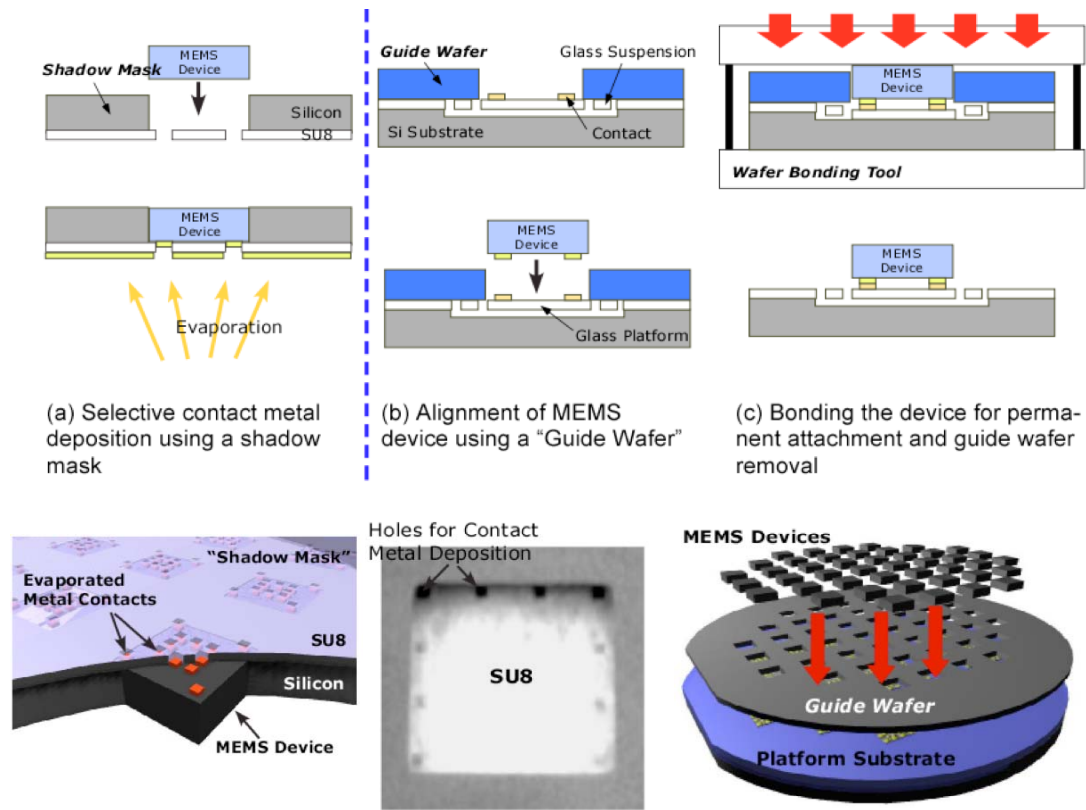


Figure 4.10 Schematic flow of the generic batch die-level transfer technique. (a) Selective pad material deposition, and (b-c) batch device transfer bonding.

Before transferring the MEMS chips, suitable metal contacts are deposited on the MEMS die utilizing the shadow mask (Figure 4.10 (a)). The shadow mask is made of a photo-patterned SU8 film ($\sim 50 \mu\text{m}$) on a silicon wafer with slots for inserting the chips. First, SU8 is spin coated on the silicon wafer, and patterned using photo lithographic technique. Second, the slots for the chip are formed by silicon DRIE from the backside of the wafer. These slots are designed to have a loose fit resulting alignment tolerance, which will be discussed in section 4.3.2.2. The MEMS devices are then flipped-over and placed in these slots for the contact metal evaporation. These metal layers are deposited only on the contact pads of the MEMS chips. By using the soft SU8 material as the shadow mask, the metal contacts can be deposited without any damage to the device.

Using this method the metal contacts can be patterned on any type of MEMS device without any restrictions. The MEMS device also can be fabricated without considering the contact metal patterning that may not be compatible with device fabrication.

After metal contact deposition, the devices are aligned and bonded onto the isolation platform utilizing a micromachined “guide wafer” and a commercial wafer bonder (Figure 3.8 (b-c)). The guide wafer has through-wafer holes where each MEMS chip can be placed also with a loose fit. The guide wafer is first aligned with the platform substrate using a SUSS MicroTec MA/BA6 wafer aligner. The MEMS devices are then flipped-over and placed in the holes (Figure 3.8 (b)). Finally, the transfer bonding is done in the SUSS MicroTec SB6e wafer bonder (Figure 3.8 (c)). The thickness of the guide wafer is smaller than that of the MEMS devices, so that only the devices are pressed during the bonding step. Figure 4.11 shows the transferred dies on the platform substrate. All the dies are integrated with good bonding strength and alignment. The resultant bonding quality and alignment tolerances for this step will be discussed in sections 4.3.2.1 and 4.3.2.2 respectively.

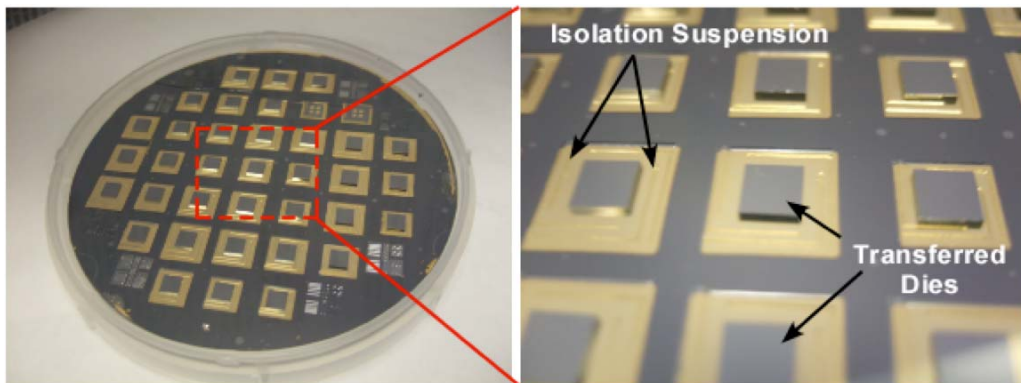


Figure 4.11 Wafer-level picture of the platform substrate with transferred dies. The transferred dies are permanently bonded on the glass isolation platform, and suspended over the substrate.

It is notable that the suspended structure can be fabricated without using any sacrificial layer. The glass platform is supported by the flexible crab-leg shape glass suspensions. Therefore, when the die is being bonded to the platform, the suspensions bend and the platform touches down on the bottom silicon wafer, but spring back up due to the relatively high stiffness of the suspensions. This technique also helps to keep the package clean, because of not using any polymeric sacrificial layer. The polymeric sacrificial layer can be a source of vacuum degradation, unless it is etched away completely. Figure 4.12 shows the fully suspended isolation platform with the MEMS chip transferred. The whole structure is suspended over the substrate by $\sim 10\ \mu\text{m}$.

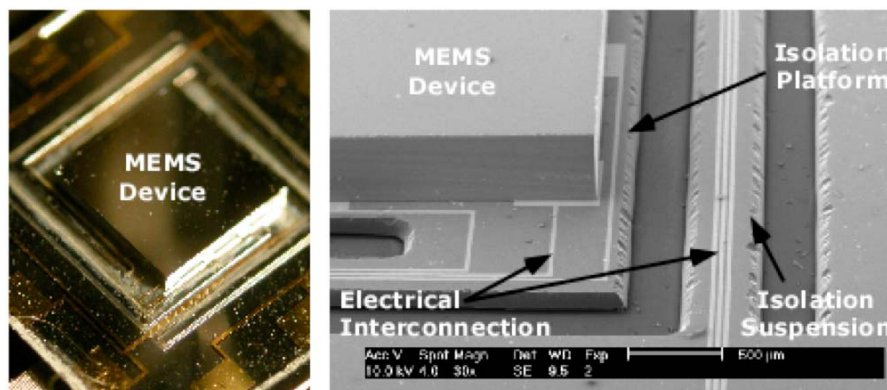


Figure 4.12 Picture of the isolation platform/suspensions with transferred device. The isolation platform is suspended over the substrate by $\sim 10\ \mu\text{m}$.

Another advantage of this technique is that different types of devices can be transferred on the same wafer. The devices do not need to be fabricated using the same technology.

4.3.2.1 In-Au Transient Liquid Phase (TLP) Transfer Bonding

An In-Au Transient Liquid Phase (TLP) bonding technique is applied in this die transfer step. TLP bonding technologies including In-Au and Ni-Sn combinations have been used for mating two structures and bonding wafers [73, 83, 154, 155]. In our work,

2 μm thick Indium contacts are deposited on the MEMS device side using the soft shadow mask discussed earlier, and 0.3 μm thick gold contacts are patterned on the glass isolation platform. Under the indium layer, another gold layer or adhesion layer such as Ti or Cr can be deposited if needed. A thin layer of gold (500 \AA) is also deposited on top of the indium contact to prevent oxidation of the indium. The bonding conditions are: a bonding temperature of 300 $^{\circ}\text{C}$, a vacuum pressure of 10 μTorr , and a bonding force of 300-500 Torr.

TLP bonding shows good thermal, mechanical and electrical properties. During the bonding, the indium and the gold react to form intermetallic compounds. Once the intermetallic compounds are formed, they remain stable up to 495 $^{\circ}\text{C}$, which is higher temperature than the formation temperature [73, 156]. Therefore, the bonded contacts do not degrade during subsequent high temperature processes, even though the transfer bonding is done at lower temperature. Figure 4.13 shows the bonded interface after the transferred MEMS chip is torn from the glass isolation platform. As illustrated, the bonding contacts are strong enough to rip the glass from under the bonding pad. The measured electrical contact resistance is less than 1 Ω .

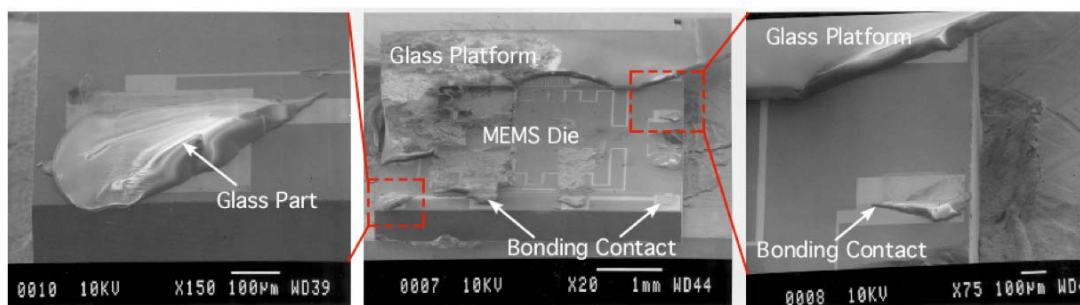


Figure 4.13 SEM pictures of the transfer bonded die on the glass platform. The glass platform is torn-apart for testing the mechanical strength of the In-Au TLP bonded contacts. Glass parts on the glass platform are ripped-off and transferred onto the MEMS device side.

4.3.2.2 Alignment Tolerances

One of the key challenges in this batch transfer technique is the alignment tolerance during device integration. Both the contact metal evaporation using the soft shadow mask, and the chip transfer bonding using the guide wafer require good alignment. Figure 4.14 shows a MEMS device (gyroscope) with two layers of contact metal deposited. The two contact metal layers are evaporated using two different shadow mask wafers. Comparing with the actual layout, the misalignment is less than $\pm 10 \mu\text{m}$.

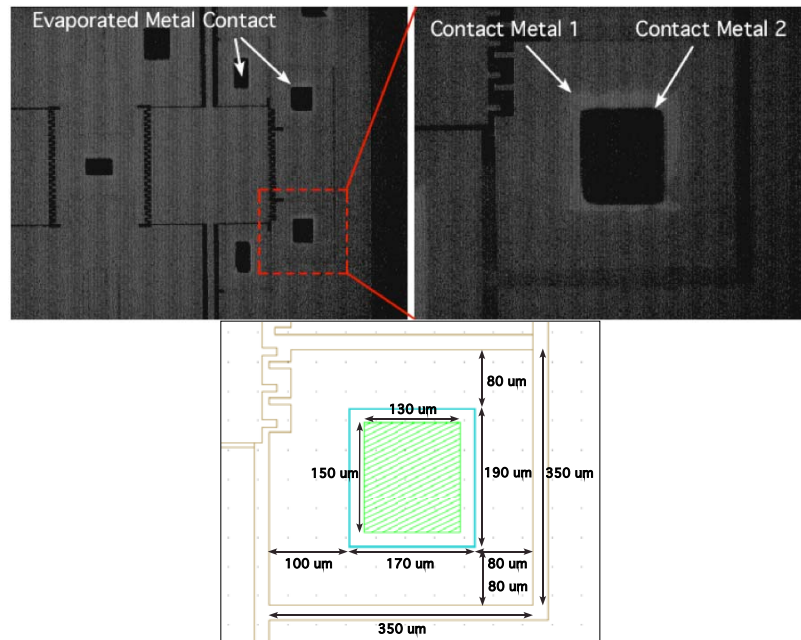


Figure 4.14 Picture of the gyroscope die with selective pad materials deposited using the shadow mask (Top). Layout and dimensions of the contact pad.

To measure the misalignment of the batch device transfer technique, alignment marks have been patterned on the glass platform as shown in Figure 4.15. Vertical and horizontal misalignments are measured from the distance between the alignment marks and the edge of the transferred die.

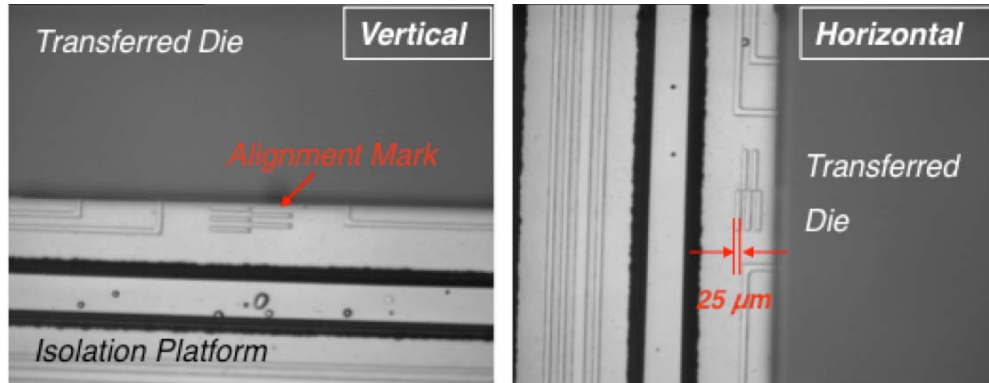


Figure 4.15 Alignment marks for measuring misalignment. The width of each alignment bar is 25 μm .

Table 4.4 shows the measurement results after the batch die transfer. As illustrated, the misalignment ranges from 0 to 150 μm in each direction, with an average of around 35 μm .

Table 4.4 Misalignment measurement data.

Device Type (gp04-5-#3)	Die Number	Vertical Misalignment [μm]	Horizontal Misalignment [μm]
Gyroscope Dies	1	25	50
	2	10	60
	3	50	40
	4	35	5
	5	30	50
	6	50	0
	7	25	50
	8	25	65
	9	0	15
	10	25	50
Pirani Gauge Dies	a	15	30
	b	25	25
	c	25	0
	d	15	30
	e	150	40
	f	40	75
<i>Average Misalignment</i>		34	36.5

4.3.3 Wafer Bonding and Vertical Feedthrough

Vacuum encapsulation is achieved using wafer-level bonding with a recessed silicon cap wafer (Figure 4.4 (g)). The recessed cavity can be formed by DRIE or wet etching, and is covered with a metal layer for shock absorption and radiation shield. A getter layer is necessary to achieve and maintain a good vacuum environment.

Wafer bonding can be done using a variety of bonding techniques including anodic bonding and Au-Si eutectic bonding. Anodic bonding has the advantage that an extra bond ring layer is not needed, thus reducing process steps. However, the bonding surface needs to be very clean and flat. The applied high voltage or electrostatic force during anodic bonding can potentially damage packaged devices. On the other hand, the Au-Si eutectic bond can accommodate a non-flat surface profile and moderate roughness because a liquid is formed during bonding. Other types of bonding methods could also be applied once they are developed to the point where they are compatible with vacuum packaging.

Au-Si eutectic bonding has been applied in this work. Figure 4.16 shows sequential pictures of the package dies before and after eutectic bonding. Wafer bonding is performed at 390 °C in a SUSS MicroTec SB6e bonder. A gold bond ring on the glass shares the same mask layout with the metal interconnection lines. A gold bond ring on the silicon cap wafer is electroplated to $\sim 4 \mu\text{m}$ thick on top of a Cr/Au (200 Å/ 5000 Å) seed layer. The bond ring width is $\sim 200 \mu\text{m}$. During bonding silicon diffuses into the Au allowing for the formation of a soft Au-Si eutectic layer and uniform contact across two mating wafers [146]. The bonding strength is high enough to rip the glass from under the bond ring when the bonded dies are torn apart intentionally (Figure 4.17).

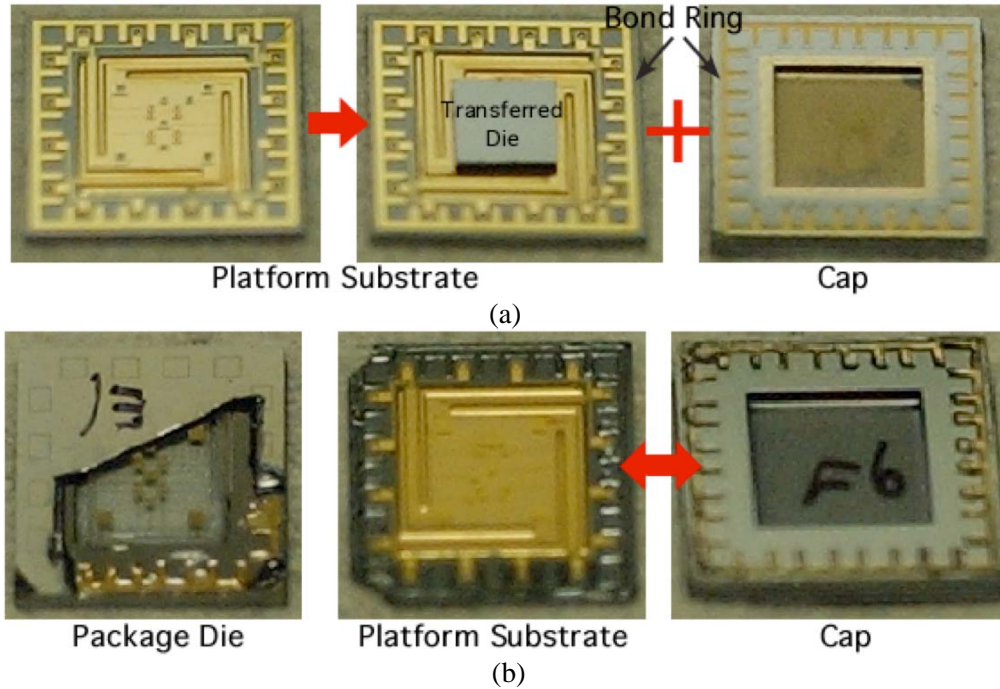


Figure 4.16 (a) Pictures of the platform substrate die and encapsulation cap die. (b) Pictures of the complete package which is torn apart for the visual inspection.

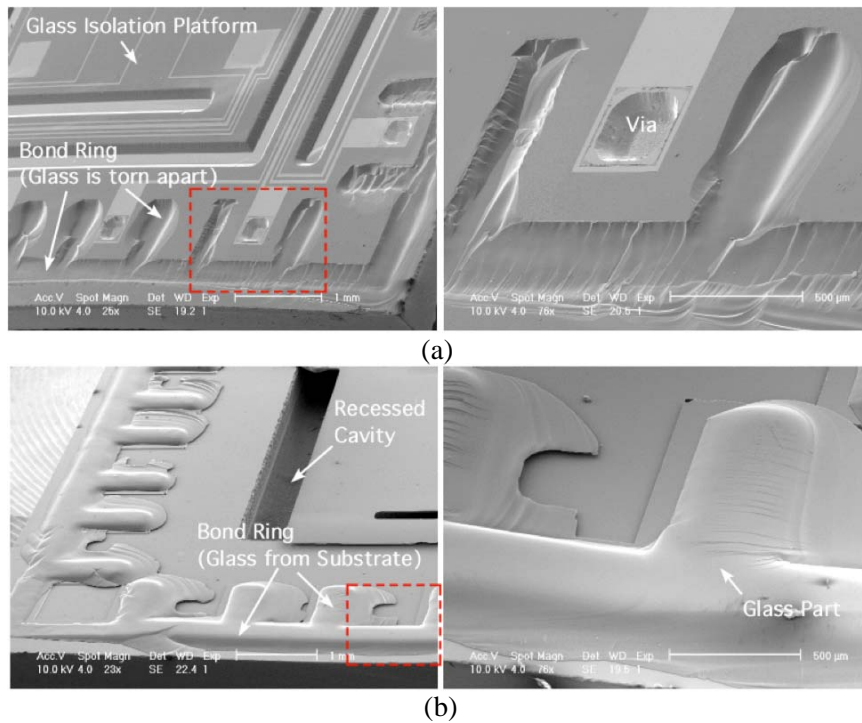


Figure 4.17 SEM pictures of the Au-Si eutectic bonded package. (a) Platform substrate, and (b) encapsulation cap. Package is torn apart for the visual inspection. The glass part on the bond ring is ripped off from the platform substrate.

As described in Chapter 2, a getter material is required to maintain a high vacuum inside the cavity. ISSYS, Inc. has developed a getter material, called NanoGetter™, which has demonstrated a vacuum level in the sub-mTorr range [124, 125]. We have implemented NanoGetter™ in our package to achieve lower pressure levels.

As described earlier, after wafer bonding, the vertical feedthroughs are electrically isolated by silicon DRIE through the support silicon wafer from the backside. The vertical feedthrough technique reduces the footprint of the package, and, unlike lateral feedthroughs, enables direct flip-chip attachment of the package onto a circuit board. Figure 4.18 shows cross section views of the vertical feedthroughs. The top area of the feedthrough is $1.1 \text{ mm} \times 0.9 \text{ mm}$. They are robust enough to be diced across the feedthroughs as illustrated in Figure 4.18. The resistance of the feedthrough (including the contact resistance of the via) is small, $< 2 \Omega$, because the silicon substrate is highly-doped ($< 0.01 \Omega\text{-cm}$). The parasitic capacitance between the vertical feedthrough and the package is small, $< 0.6 \text{ pF}$ (by calculation), because the feedthrough is separated by air-gap.

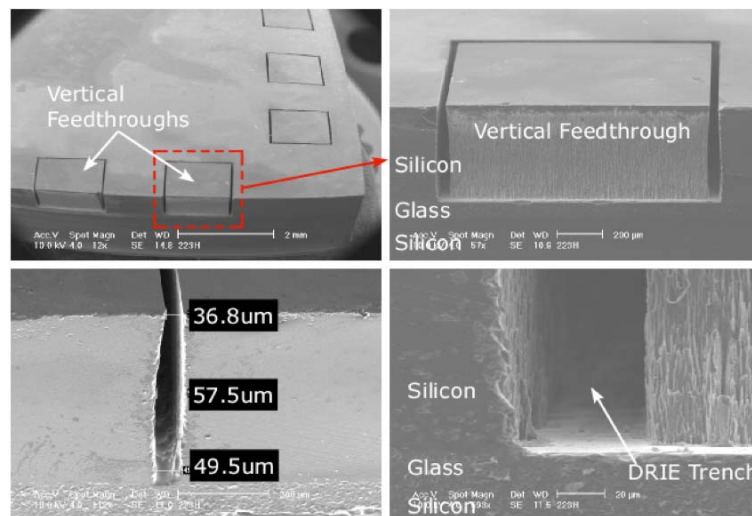


Figure 4.18 SEM pictures of the silicon vertical feedthroughs.

Figure 4.19 shows pictures of the complete package. The size of the package is $12 \times 12 \times 1.6 \text{ mm}^3$, and the package accommodates 12 feedthroughs. The package can be attached onto a circuit board using wire bonding or flip-chip attachment.

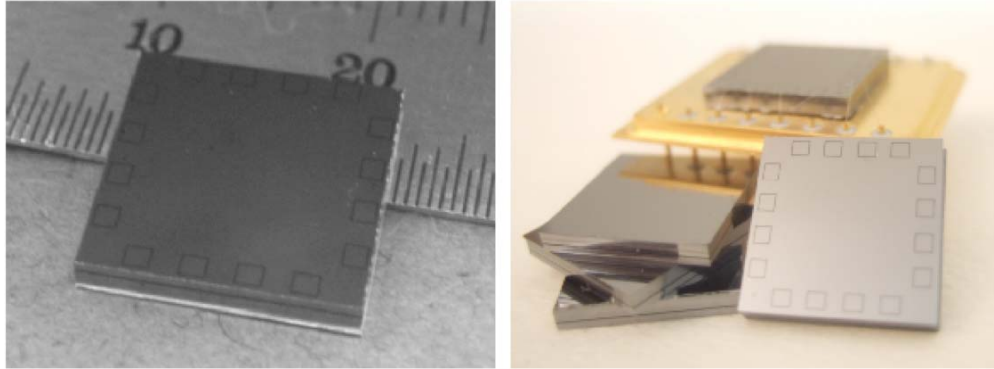


Figure 4.19 Pictures of the complete package die.

4.4 Test Results

Three different types of devices have been packaged to demonstrate the performance of the environment-resistant package. Thermal test chips with an integrated heater and temperature sensor have been packaged to measure the total thermal resistance of the package. Pirani gauges have been packaged to directly measure the vacuum level inside the package. Finally, gyroscopes have been packaged and tested. The size of all of the test chips is $4.5 \times 4.5 \times 0.5 \text{ mm}^3$. The thermal test chip and the Pirani gauge chips have been transferred on the same platform wafer using the batch die-level transfer technology (Figure 4.20).

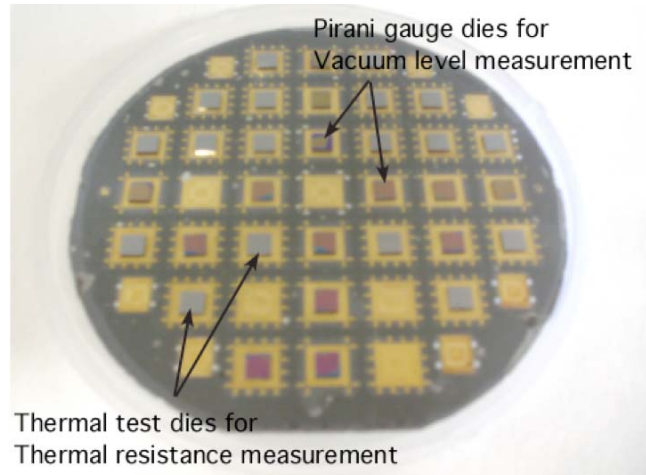


Figure 4.20 Wafer-level view of the platform substrate with transferred thermal test dies and Pirani gauge dies.

4.4.1 Thermal Resistance Measurement

Thermal resistance has been measured by packaging the thermal test chip. The test chip has an integrated heater and temperature sensor made of thin film gold (Figure 4.21). The chip size is $4.5 \times 4.5 \times 0.5 \text{ mm}^3$, and the resistance of the heater and temperature sensor is $\sim 100 \Omega$ and $\sim 1 \text{ k}\Omega$ respectively.

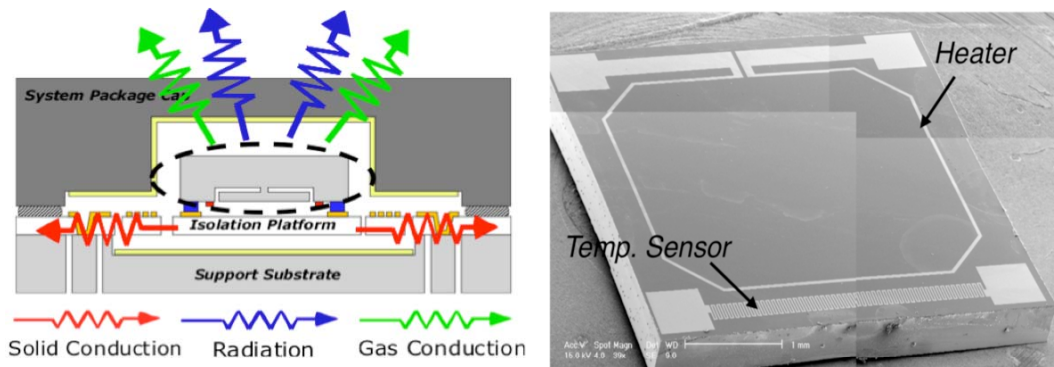


Figure 4.21 Schematic illustration of the heat dissipation paths in the package, and SEM picture of the thermal test die with the heater and temperature sensor.

The same test setup, described in section 3.6.2, has been used for testing. Once again, the packaged chip is heated by flowing current through the heater, and the power

consumption for heating is measured. All the heat transfer mechanisms – solid conduction, gas conduction and radiation – contribute to the heat loss in this test. A temperature change is obtained by measuring the resistance change of the temperature sensor. The thermal resistance is calculated by $R_{T,total} = \Delta T / P$ (Equation 2.1)

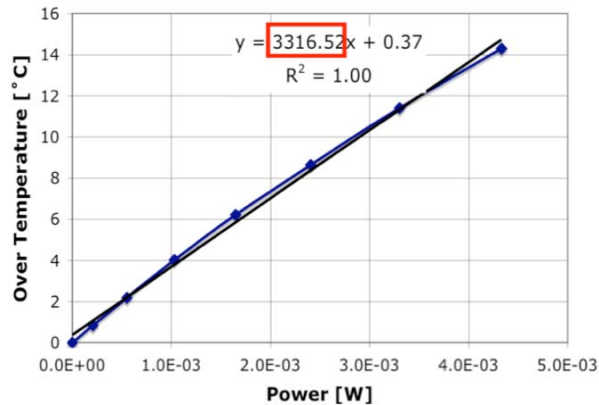


Figure 4.22 Thermal resistance measurement result. The slope of the data curve shows 3316 K/W of thermal resistance.

The package provides about 3,300 K/W of thermal resistance between the thermal test device and the environment as shown in Figure 4.22. This corresponds to less than 40 mW of power consumption when the heated chip is at 80 °C and the environment is at –50 °C ($\Delta T = 130$ °C). If a chip with the same size is packaged without thermal isolation, more than 1 W of power is required according to calculations.

4.4.2 Vacuum-level Measurement

The vacuum level inside the package has been directly measured using the Pirani gauge chips. The Pirani gauge was designed by Warren Welch III, and its process is described in detail elsewhere [83]. A thin film Pt heater is suspended by thin dielectric bridges at the center of the die (Figure 4.23). It is designed to minimize heat loss by solid conduction (heat dissipation through the bridges). Radiation can be ignored at low

temperature, and gaseous convection can be neglected because the Pirani gauge is located in a package where no external forced gas convection exists. Therefore, the predominant dissipation mechanism is gas conduction [135].

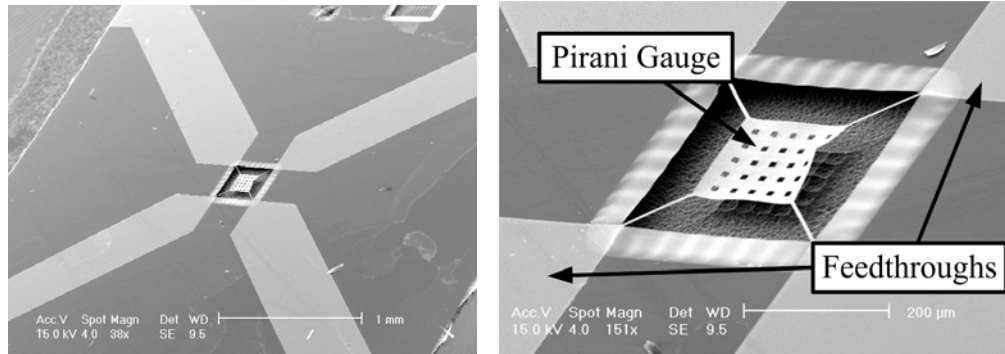


Figure 4.23 SEM views of the Pirani gauge die and closed-up view of the suspended Pt heater [83].

By measuring the thermal resistance using the packaged Pirani gauge, the pressure level inside the package can be obtained. As mentioned earlier, at low pressures, the mean free path of gas molecules is much larger (~ 1 mm at 70 mTorr/25 °C) than the distance between the heating element (Pt heater) and the heat sink (Pirani gauge chip substrate, ~ 50 μm). Therefore, heat loss due to gas conduction from a hot surface to a cold surface does not include intermolecular collisions, and it is proportional to the pressure level [44]. The thermal resistance of the Pirani gauge increases as the number of gas molecules decreases.

The thermal resistance between the suspended Pt heater and the substrate is measured by flowing increasing amounts of current through the heater. As the current increases, more joule heating occurs in the suspended element and the temperature rises. This temperature rise can be measured by measuring the change in resistance of the Pt heater versus a null value taken at very small currents where joule heating has not occurred. The temperature change can be plotted versus the power consumed for joule

heating in the suspended structure. The slope of this line is the thermal resistance of gas conduction.

To determine the vacuum inside the package, a Pirani gauge characterization plot needs to be obtained. The thermal resistance of the Pirani gauge is measured by varying the pressure level inside a test vacuum chamber. A gas access hole is drilled on the test package wall, and it equals the pressure between the package and the vacuum chamber. Figure 4.24 shows the Pirani gauge characterization plot.

The measured thermal resistance of the packaged Pirani gauge is $\sim 760,000$ K/W. This value corresponds to ~ 30 mTorr pressure (Figure 4.24).

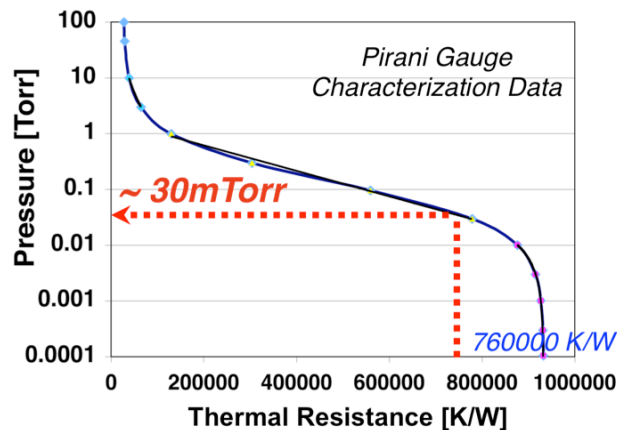


Figure 4.24 Characterization data of the Pirani gauge. The vacuum packaged Pirani gauge shows 760000 K/W which corresponds to ~ 30 mTorr of base pressure inside the package.

4.4.3 MEMS Gyroscope Packaging

MEMS gyroscopes have been vacuum packaged and tested. The gyroscope was designed and fabricated by Prof. F. Ayazi's group at the Georgia Institute of Technology [157]. It is made on a SOI (Silicon-on-Insulator) wafer and requires 12 electrodes for its operation. The heater and temperature sensor can be integrated on the gyroscope die for

oven-control as shown in Figure 4.25. However, in our testing, gyroscopes without heater and temperature sensor have been packaged.

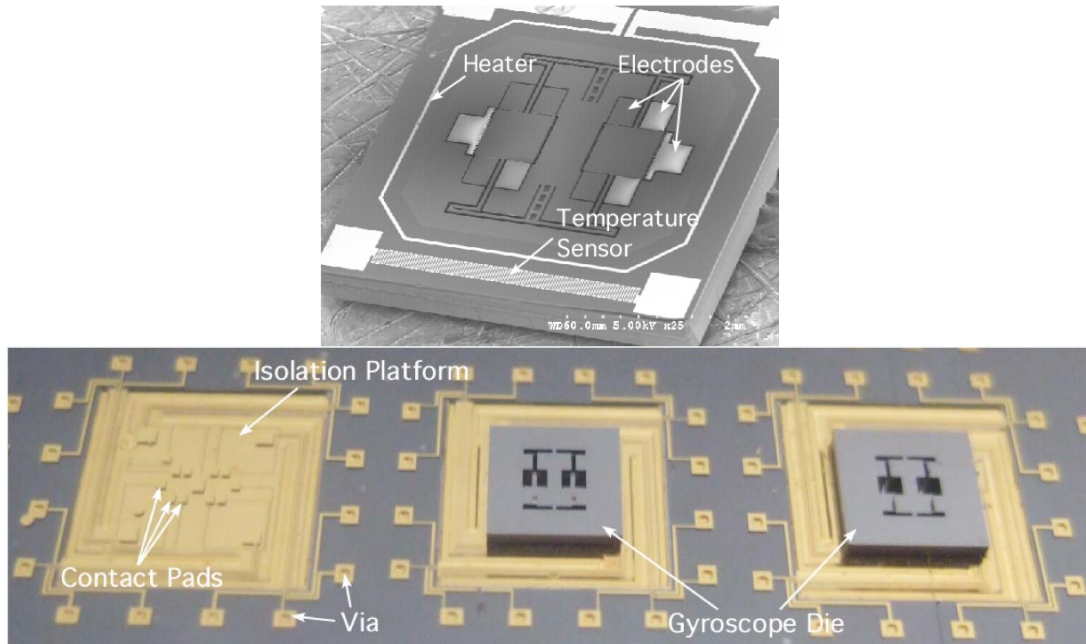


Figure 4.25 SEM picture of the gyroscope with integrated heater and temperature sensor (Top). Picture of the isolation platforms with and without transferred gyroscope (Bottom).

The techniques described in section 4.3 have been used for packaging these devices. Figure 4.26 shows SEM views of the packaged gyroscopes. The cap in the figure is intentionally broken for visual inspection.

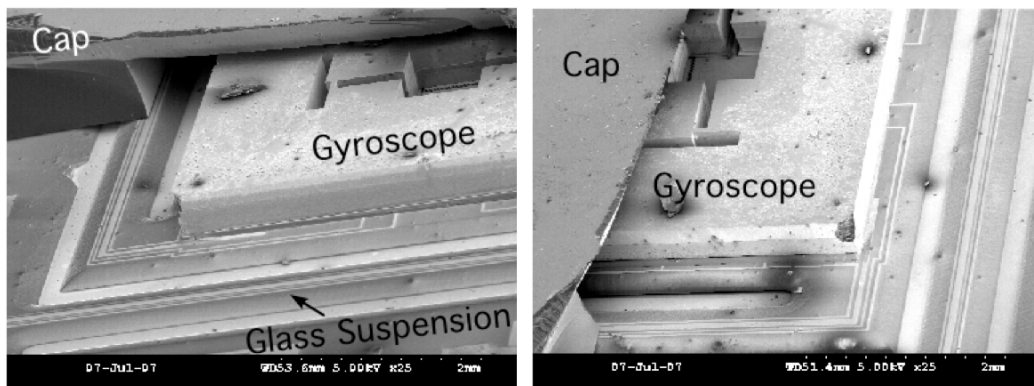


Figure 4.26 SEM pictures of the packaged gyroscope. Part of the encapsulation cap is torn apart for the visual inspection.

The operational test of the packaged gyroscope has been performed at the Georgia Institute of Technology. Figure 4.27 shows the test board with the wire bonded package, and the measured gain chart. The packaged gyroscope shows mechanical resonance at ~14,600 Hz, and a quality factor (Q factor) of around 700.

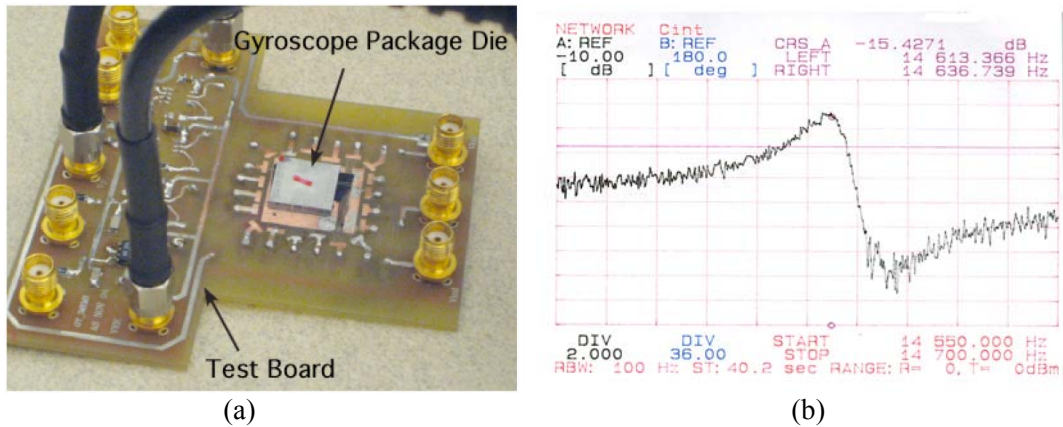


Figure 4.27 (a) Test board with the gyroscope package die. (b) Gyroscope gain analysis data. Center frequency is ~14,600 Hz, and Q factor is ~ 700.

The Q factor is lower than expected by $\times 30 \sim 50$. Two major possible reasons are: higher pressure levels than expected inside the cavity, and the absence of a shield metal layer between the gyroscope device and the glass platform. High pressure levels (low vacuum) may come from outgassing during wafer bonding or from ineffective NanoGetter™ activation. Furthermore, the gap between the gyroscope surface and the glass platform is 2-3 μm . As a result, there may be unwanted potential difference between these two surfaces, and that may cause unstable operation. This electrical potential difference could be minimized by putting a shield layer with the proper electrical potential on the glass platform surface.

4.5 Summary

In this chapter, we have presented a new generic packaging technology including a glass isolation platform/suspensions, a generic batch die-level transfer technique, wafer-level vacuum encapsulation, and glass-silicon combined vertical feedthroughs. Three different types of devices including thermal test chips, Pirani gauge chips, and MEMS gyroscopes have been packaged using this technology. Table 4.5 summarizes this new packaging technology.

Table 4.5 Summary of Chapter 4.

Packaging Technology	Glass isolation platform/suspensions	Thermal & vibration isolation High performance
	Batch die-level device transfer	Generic device assembly
	Wafer-level vacuum encapsulation	High performance
	Glass-silicon vertical feedthrough	0/1-level package, Small size
Demonstration	Thermal test chip package	Thermal resistance measurement
	Pirani gauge chip package	Vacuum level measurement
	MEMS gyroscope package	Package performance evaluation

By using the thin glass isolation platform, both thermal and vibration isolation can be achieved. The glass material has good thermal and mechanical properties, and it can be patterned using wet etching processes.

The batch die-level transfer technique for integrating individual MEMS chips realizes a generic packaging approach. This transfer technique has several advantages. First, a variety of MEMS devices can be integrated since the chips are packaged after they are fabricated using almost any given process. Therefore, the design time and process cost can be reduced. Second, the electrical and mechanical connection between

the MEMS device and the package is performed at the same time. Third, this provides flexibility in selecting the transfer bonding methods and pad materials, since the any material required for bonding can be deposited after the MEMS device fabrication. In addition to various combinations of TLP bonding, other die attachment approaches, such as thermocompression and solder bonding can also be used. Forth, it is possible to suspend the device over the substrate without using any sacrificial layer. Therefore, additional steps for removing the sacrificial layer are not required. Fifth, this approach provides flexibilities in designing the MEMS device because the contact pads do not need to be located only around the perimeter of the MEMS device.

Glass-silicon vertical feedthrough can be implemented in the developed package using three simple processes of wet etching, metal filling and silicon DRIE. The feedthrough with wafer-level bonding enables merging 0-level and 1-level packaging processes. The package die can be flip-chip assembled on a circuit board without wire bonding. This provides flexibility in choosing wafer bonding method, and reduces the risk of gaseous leakage.

By packaging three different types of devices, the performance and feasibility of this technology has been demonstrated. This package provides a large thermal resistance ($\sim 3,300$ K/W) and environmental vibration isolation (higher than ~ 1 kHz). The package also delivers good vacuum (< 30 mTorr) and vertical signal feedthroughs with small resistances (< 2 ohm). A fully packaged MEMS gyroscope has also been demonstrated. While the packaged gyroscope is functional with a $Q = 700$, its performance needs to be improved.

Chapter 5

Low-Power Oven-Controlled Environment-Resistant Package

5.1 Introduction

This chapter presents the design and performance of a modified environment-resistant package technology. The basic concept of the package design is the same as the previous version detailed in Chapter 4. Major design modifications include:

- (i) The location of the vertical feedthroughs has been moved from the bottom substrate to the top cap substrate.
- (ii) A heater and temperature sensor have been placed on the glass isolation platform.
- (iii) A shallow recess has been patterned on the glass platform.
- (iv) An electrical potential shield layer has been placed on the glass platform.
- (v) Anodic bonding has been applied in the final vacuum encapsulation.

This modified packaging technology is evaluated by packaging Pirani gauges and gyroscopes. Long-term vacuum measurement has been done by measuring the thermal resistance of the packaged Pirani gauges. The performance of the packaged gyroscopes has been improved by increasing the gap between the device surface and the isolation platform surface, and by adding an electrical potential shield layer under the gyroscope.

The gyroscopes have also been tested under oven-control using the integrated heater and temperature sensor.

In section 5.2, the design principles for the modified packages are presented. In section 5.3, the fabrication process is described in detail. Section 5.4 describes oven-control techniques. In section 5.5, test results are presented in detail. Finally, section 5.6 gives some concluding remarks.

5.2 Package Design

As described earlier, the package design has been modified in several areas (Figure 5.1). Major modifications are summarized in Table 5.1.

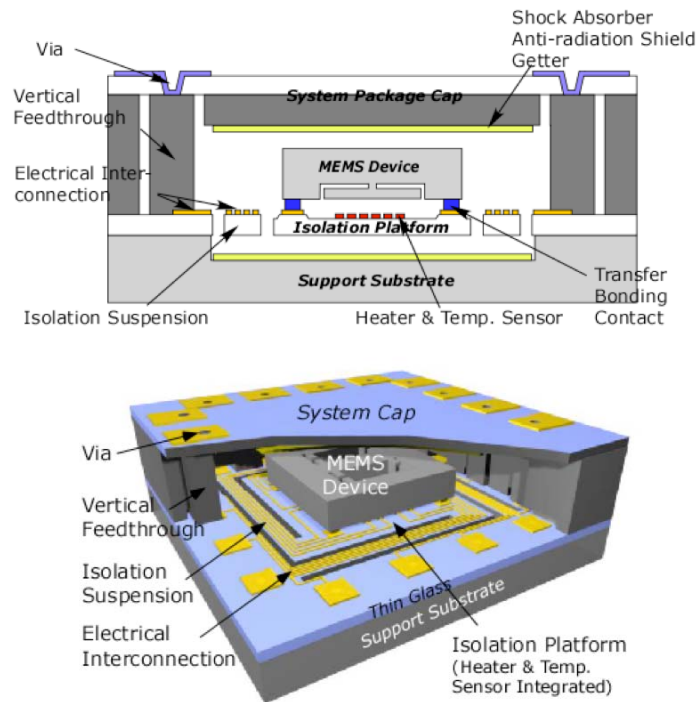


Figure 5.1 Schematic illustrations of the modified package.

Table 5.1 Summary of major modifications in the new package design.

Package Components	Modifications
Package Structure	- Si (500 μm)/Glass (100 μm)/Si (1000 μm)/Glass (100 μm)
Vertical Feedthroughs	- Glass/silicon feedthroughs in cap substrate - Reduced size and pitch of the feedthroughs - Feedthrough numbers: 20 and 24
Isolation Platform	- Shallow recess - Heater and temperature sensor - Electrical potential shield
Vacuum Encapsulation	- Anodic bonding

As illustrated in Figure 5.1, the package consists of two silicon and two thin glass wafers. The bottom substrate for the isolation platform is made out of a silicon-glass bonded wafer, and the top cap substrate for the vacuum encapsulation and vertical feedthroughs is made out of a highly-doped silicon and thin glass bonded wafer combination. Similar techniques to those described in Chapter 4 have been used for vertical feedthrough formation. Because the fabrication of the feedthroughs is finished before mating the two substrates, vacuum encapsulation bonding is the last process step. Using this modified technique, process steps can be distributed evenly in preparing the platform substrate and the cap substrate. The size and pitch of the vertical feedthrough have also been reduced to accommodate increased feedthrough numbers (20 and 24).

A shallow recess on the glass platform increases the gap between the platform surface and the device surface. This can prevent stiction of the device surface to the glass platform during anodic bonding, and a relatively thick layer can be patterned on the platform without touching the device surface. The heater and temperature sensor are integrated on the glass platform instead of on the device. This can eliminate additional processes for implementing the heater and sensor on the MEMS device, and allows for greater flexibility in designing the device. Using the heater and the temperature sensor,

the device is oven-controlled at a temperature higher than the maximum environmental temperature. An electrical potential shield provides stable operations of the transfer device.

Anodic bonding has been applied instead of Au-Si eutectic bonding, because by using anodic bonding, no additional bond ring is required. As mentioned above, the increased gap between the device and the platform surface helps to prevent stiction due to electrostatic forces during anodic bonding.

5.3 Fabrication

5.3.1 Fabrication Steps

Figure 5.2 shows the fabrication process sequence and the exploded view of the modified environment-resistant package. The fabrication steps are similar to the previous version of the environment-resistant package described in section 4.3, except for the three major differences mentioned earlier: (a) modified vertical feedthroughs, (b) modified glass isolation platform design, and (c) anodic bonding for the final vacuum encapsulation.

A recess of $\sim 10\ \mu\text{m}$ is first formed on a silicon wafer and is coated with a shock absorption layer (e.g., gold). The wafer is then anodically bonded to a $100\ \mu\text{m}$ -thick glass wafer. A shallow recess of $\sim 10\ \mu\text{m}$ is wet etched on the thin glass (Figure 5.2 (a2)). The recess increases the gap between the glass platform and the MEMS device, which will be flip-chip bonded over the recess. Metal interconnection lines, heater and temperature sensor are then defined using Ti/Pt/Au layers (Figure 5.2 (a3)). Next, isolation platform/suspensions are patterned by wet etching the glass (Figure 5.2 (a4)).

MEMS chips are then batch transferred onto the glass platform using the In-Au TLP bonding technique (Figure 5.2 (a5)). This batch transfer technique is described in detail in section 4.3.2.

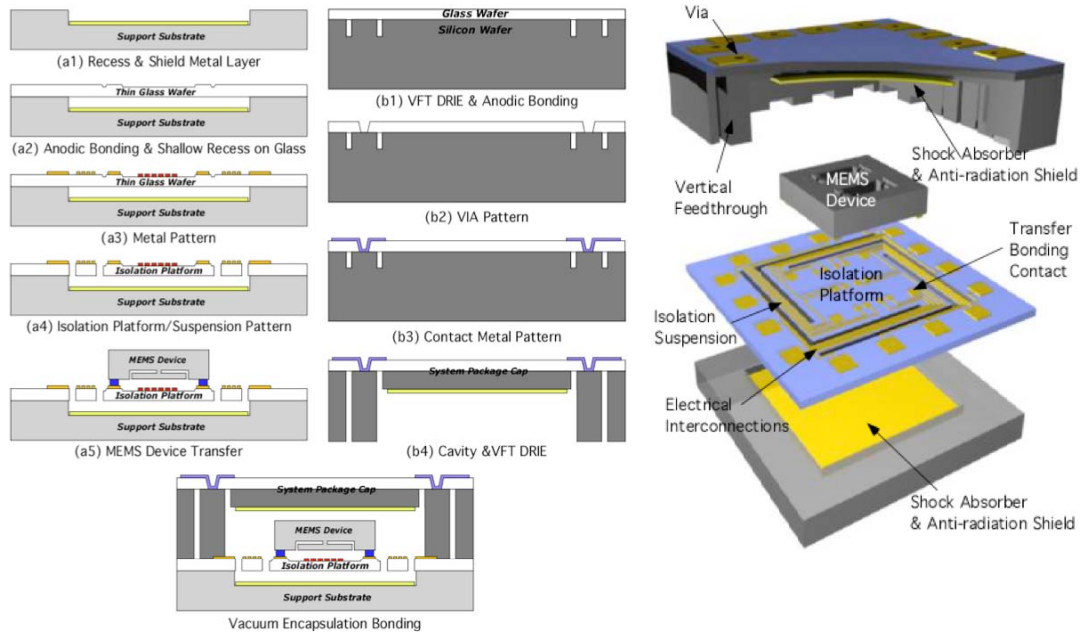


Figure 5.2 Package process flow and exploded view.

Cap fabrication starts with a silicon DRIE step for the vertical feedthroughs on a highly-doped silicon wafer ($<0.01 \Omega\text{-cm}$). The depth of the DRIE trench defines the final cavity depth. The silicon cap wafer is anodically bonded to a second $100 \mu\text{m}$ -thick glass wafer (Figure 5.2 (b1)). Via holes are formed by wet etching the glass using 49% HF solution with a Cr/Au/photoresist masking layer (Figure 5.2 (b2)). An Al contact metal is then patterned over these via holes (Figure 5.2 (b3)). The vertical feedthroughs and the package cavity are then defined by a second DRIE of the silicon wafer (Figure 5.2 (b4)). A getter layer, anti-radiation shield layer, and shock absorption layer are deposited inside the cavity. Finally, the platform substrate containing the MEMS chip and the package cap substrate are anodically bonded at the wafer-level.

5.3.2 Fabrication Results

Figure 5.3 shows wafer-level views of the prepared platform, cap and completed package. The thickness of the completed package wafer is 1.7 mm.

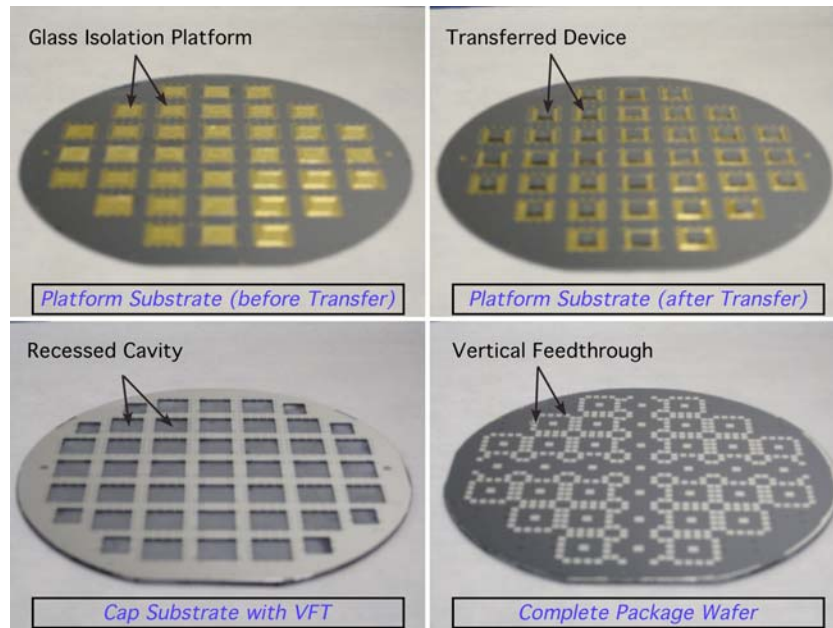


Figure 5.3 Wafer-level pictures of processed substrates in each step.

Figure 5.4 shows die-level views before and after complete packaging. The package die size is $1.2 \times 1.2 \times 0.17 \text{ cm}^3$. Vertical feedthroughs numbering 16, 20, and 24 are integrated in each package as shown in Figure 5.4. Sizes of the feedthroughs are $800 \times 1100 \text{ }\mu\text{m}^2$, $700 \times 1000 \text{ }\mu\text{m}^2$, and $600 \times 600 \text{ }\mu\text{m}^2$ for the package with 16, 20 and 24 feedthroughs respectively. The calculated parasitic capacitances between these feedthroughs and the packages are around 0.6 pF, 0.5 pF, and 0.3 pF respectively. The contact metal at the center of the die is an auxiliary electrical connection to the package body.

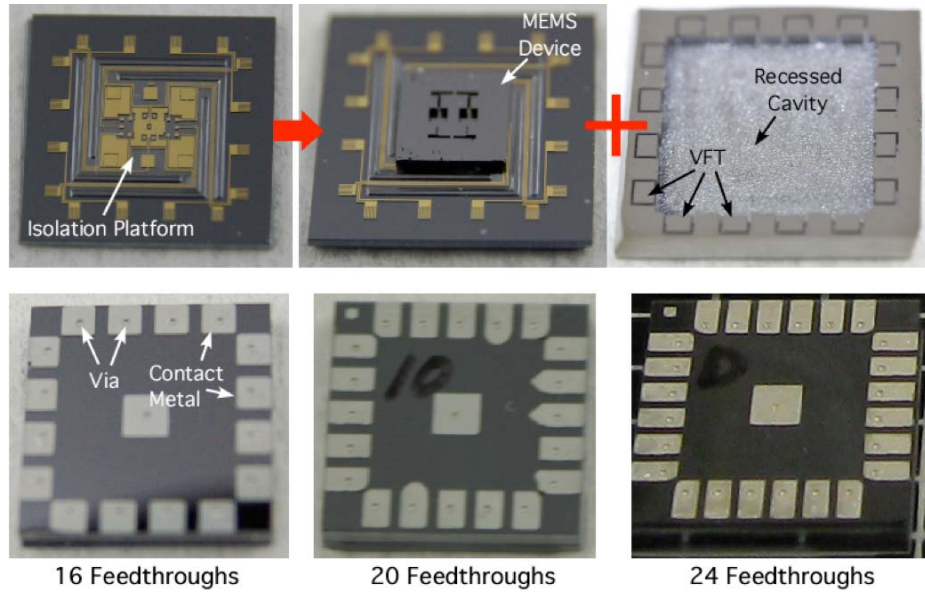


Figure 5.4 Die-level views of the packaging sequence (Top). Complete package with different feedthrough numbers (Bottom).

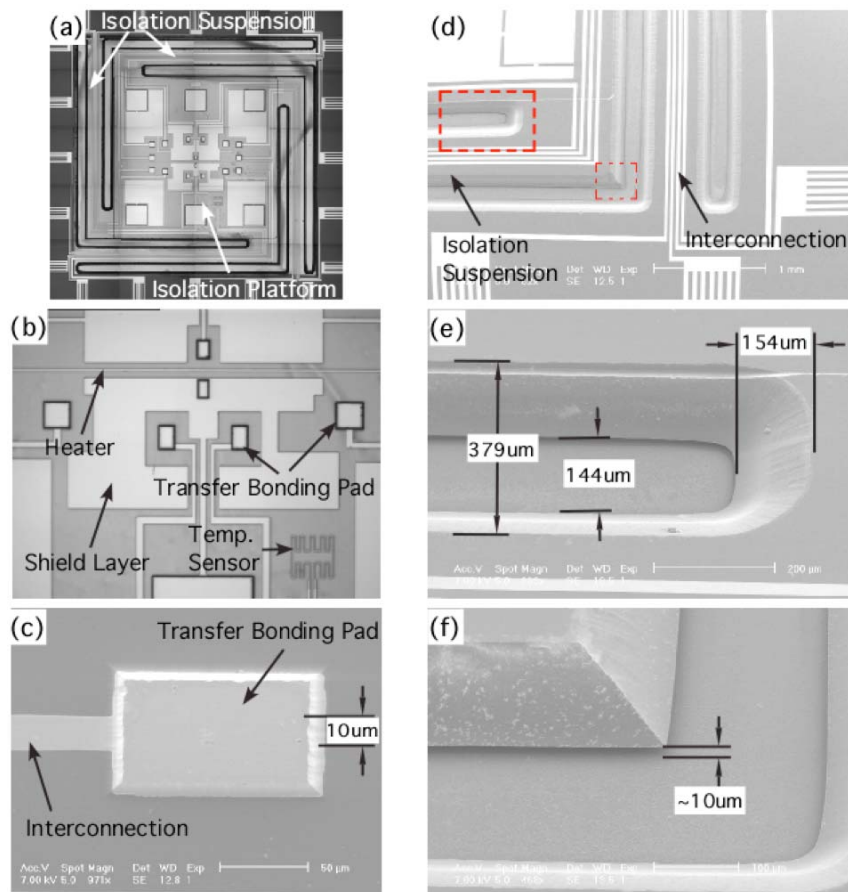


Figure 5.5 Pictures of the fabricated isolation platform and suspensions.

Figure 5.5 shows photographs of the isolation platform and suspensions. The heater, temperature sensor, and metal shield layer are integrated on the platform (Figure 5.5 (b)). The platform is recessed about 10 μm except for the transfer bonding contact regions (Figure 5.5 (c)). The platform and suspensions are wet etched with an undercut ratio of 1:1.5 (Figure 5.5 (e)). The initial masking layer opening width is 100 μm . The platform is suspended over the substrate by $\sim 10 \mu\text{m}$ (Figure 5.5 (f)).

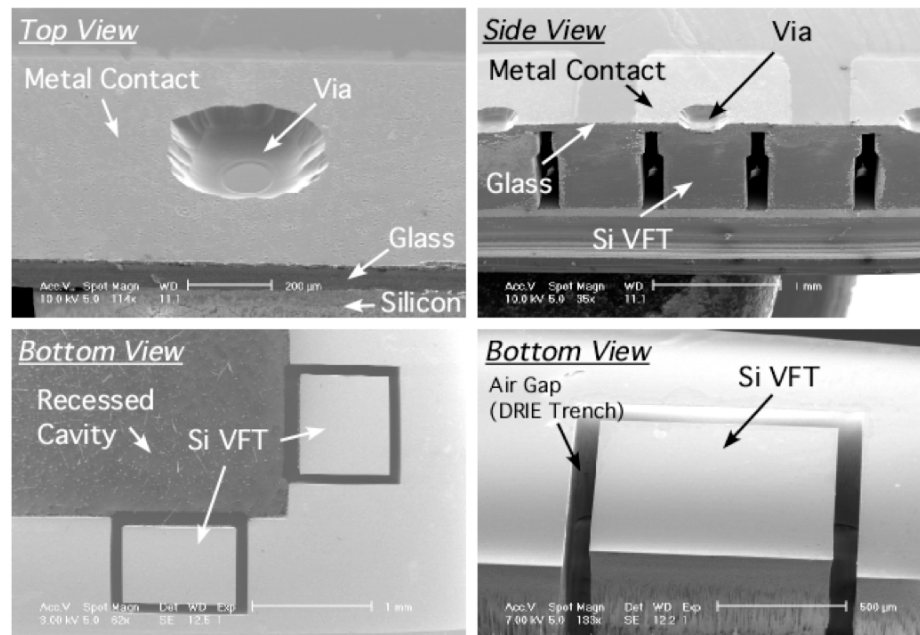


Figure 5.6 SEM pictures of the feedthroughs in the cap wafer.

Figure 5.6 shows SEM images of the vertical feedthroughs. The via holes are conformally covered by the contact metal layer. The contact resistance of these feedthroughs is less than 1 Ω . The feedthroughs are electrically and physically isolated by air gaps (silicon DRIE trenches).

Figure 5.7 shows SEM pictures of the complete package. The electrical connections between the interconnect metal lines and the silicon vertical feedthroughs are

formed during the final anodic bonding. The bond ring width is $\sim 500 \mu\text{m}$. The package die is diced for visual inspection. It is mechanically robust to survive dicing.

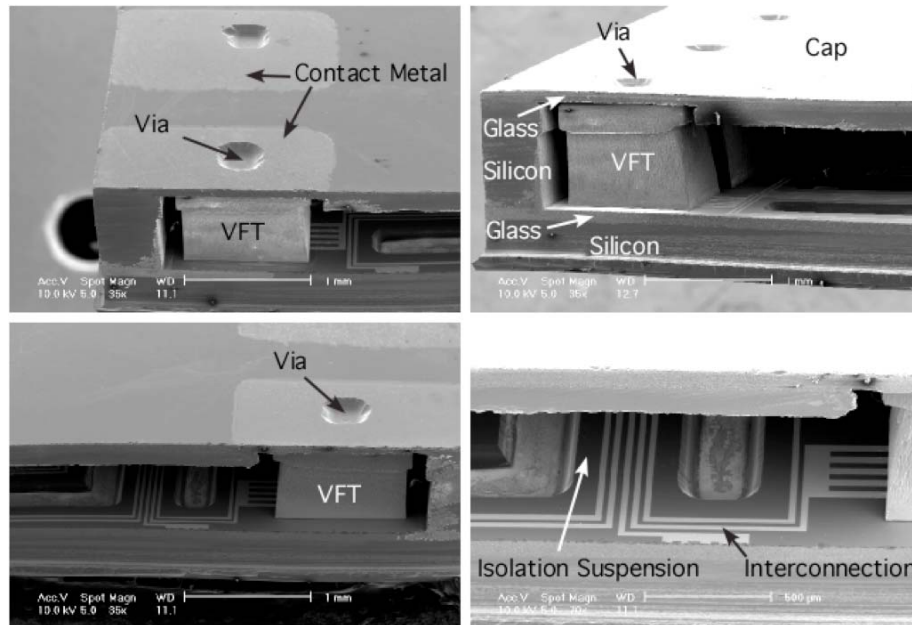


Figure 5.7 SEM pictures of the complete package. The package chip is diced across the die for the visual inspection.

Figure 5.8 shows packaged die with a MEMS device on the isolation platform. The silicon cap region is torn apart for visual inspection. The outer anodic bonded area cannot be torn off without damaging the whole package due to the very high bond strength.

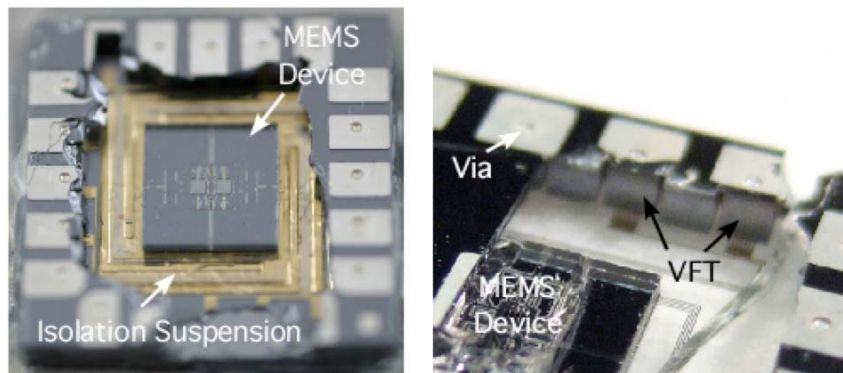


Figure 5.8 Picture of the complete package die. Center of the encapsulation cap is torn apart for the visual inspection.

5.4 Test Results

Performance has been evaluated by packaging Pirani gauges and mode-matched tuning fork gyroscopes (M²-TFGs) [157].

5.4.1 Vacuum Measurement

The vacuum levels inside the package cavity have been directly measured using the Pirani gauge chip discussed in section 4.4.2. The same measurement setup has been used for measuring the thermal resistance of the vacuum packaged Pirani gauge. The Pirani gauge characterization plot has been created again in a vacuum chamber (Figure 5.9 (a)). This plot shows that the Pirani gauge cannot measure vacuum levels below 6 mTorr, because the thermal resistance change flattens out below 6 mTorr. Figure 5.9 (b) shows the long-term pressure measurement data from the packages after bonding. The pressures inside the cavities range from 6 mTorr to 23 mTorr, and have remained stable for > 1 year without any obvious leaks.

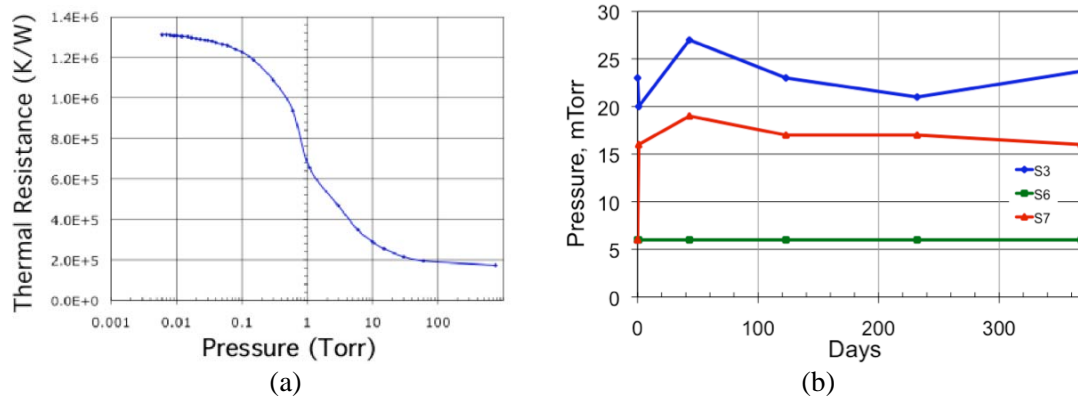


Figure 5.9 (a) Characterization plot of the packaged Pirani gauge, and (b) Long-term vacuum measurement data of the packaged Pirani gauge.

5.4.2 Packaged Gyroscope Characterization

The Mode-Matched Tuning Fork Gyroscope (M^2 -TFG) prototypes have been fabricated on a 100 μm -thick single crystalline silicon substrate using SOG (Silicon-on-Glass) process [91, 158] (Figure 5.10 (a)). The M^2 -TFG design and preliminary tests have been done by F. Ayazi's group at the Georgia Institute of Technology. Detailed design and operation mechanism of this gyroscope can be found in [157]. It requires 16 signal feedthroughs, and the gyroscope die size is $4.5 \times 4.5 \times 0.6 \text{ mm}^3$. The vacuum packaged gyroscope has been wire bonded on a test circuit board for characterizing its performance (Figure 5.10 (b)). The packaged M^2 -TFG characterization has been performed at the Georgia Institute of Technology.

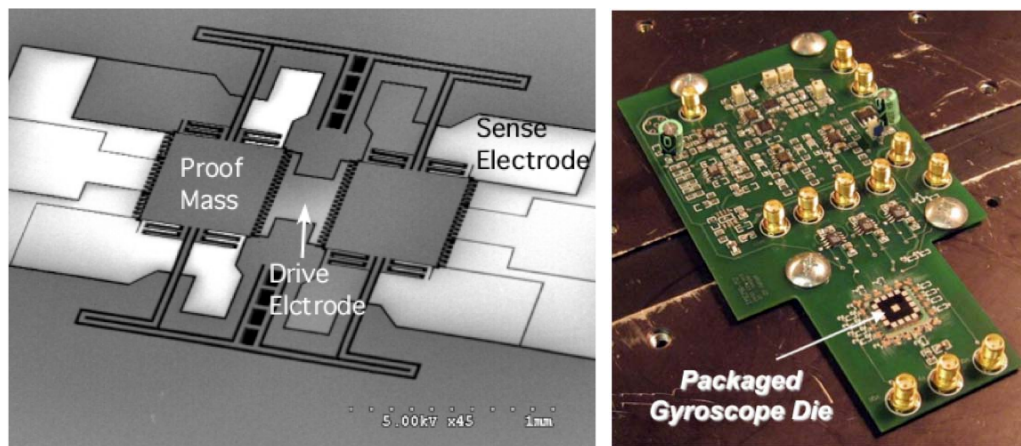


Figure 5.10 (a) SEM picture of the gyroscope die, and (b) test circuit board for the packaged gyroscope operation. (Georgia Institute of Technology)

The packaged gyroscope demonstrated high-Q resonant operating modes. Figure 5.11 shows frequency response plots of the vacuum packaged gyroscope under *mode-matched operation*. The effective Q-factor is more than 65,000 when the environment temperature is $-5 \text{ }^\circ\text{C}$. The Q-factor increases as the temperature decreases.

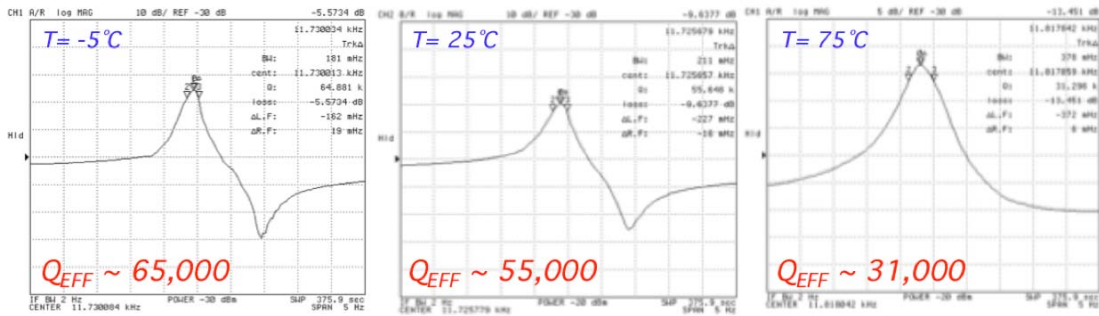


Figure 5.11 High-Q mode-matched operation of the vacuum packaged M²-TFG prototype at -5°C , 25°C , and 75°C of environment temperature. (Tested at Georgia Institute of Technology).

Figure 5.12 (a) illustrates the response of the device to a 0.01 deg/s (or 36 deg/hr) sinusoidal rotation at 0°C . In this set-up, the device undergoes ± 1.6 degrees of sinusoidal rotation at 1 mHz (time-period = 1000 s). It is evident from the device response that rotation rates below earth-rate ($\sim 12\text{-}15\text{ deg/hr}$) can be measured using the vacuum packaged M²-TFG, potentially making it suitable for navigation-grade applications such as gyro-compassing.

Allan variance analysis has been performed with Zero-Rate-Output (ZRO) data collected over a period of 6 hours at two constant temperature settings. Figure 5.12 (b) shows the measured Angle Random Walk (ARW) and bias instability values of $0.025\text{ }^{\circ}/\sqrt{\text{hr}}$ and $0.72\text{ }^{\circ}/\text{hr}$, respectively, when operated at constant 25°C . The ARW and bias instability values are improved at -5°C to $0.012\text{ }^{\circ}/\sqrt{\text{hr}}$ and $0.55\text{ }^{\circ}/\text{hr}$, respectively.

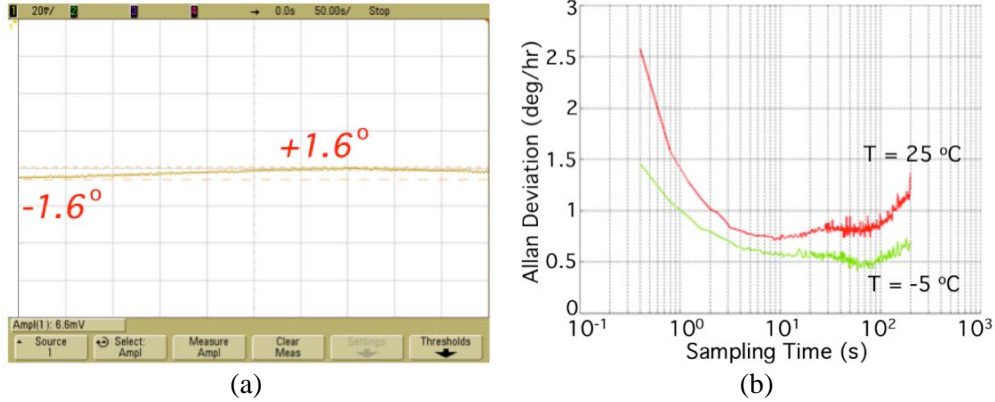


Figure 5.12 (a) Response to 0.01 deg/s (36 deg/hr) sinusoidal input rotation signal at T = 0 °C, (b) Root Allan variance plot of the vacuum packaged M²-TFG prototype at T = 25 °C and -5 °C. (Tested at Georgia Institute of Technology)

5.4.3 Vacuum Package Characterizations

As shown in the previous section 5.5.2, the vacuum packaged gyroscope shows high performance. The package also needs to provide a stable and robust environment to maintain high performance.

The high Q-factor of the gyroscope is an indication of the high vacuum encapsulation of this package. As described in section 5.5.1, the high vacuum encapsulation has been proven by the Pirani gauge data. Figure 5.13 shows the drive mode frequency response of the vacuum packaged gyroscope, and the drive Q-factor versus pressure levels plot of an *unpacked* gyroscope. The drive mode Q-factor of the vacuum packaged gyroscope is >50,000 at room temperature (Figure 5.13 (a)). The unpackaged gyroscope die has been tested in a temperature controllable vacuum probe station. As shown in Figure 5.13 (b), the gyroscope requires <10 mTorr to achieve such a high Q-factor. This is further evidence that the package provides a high vacuum environment.

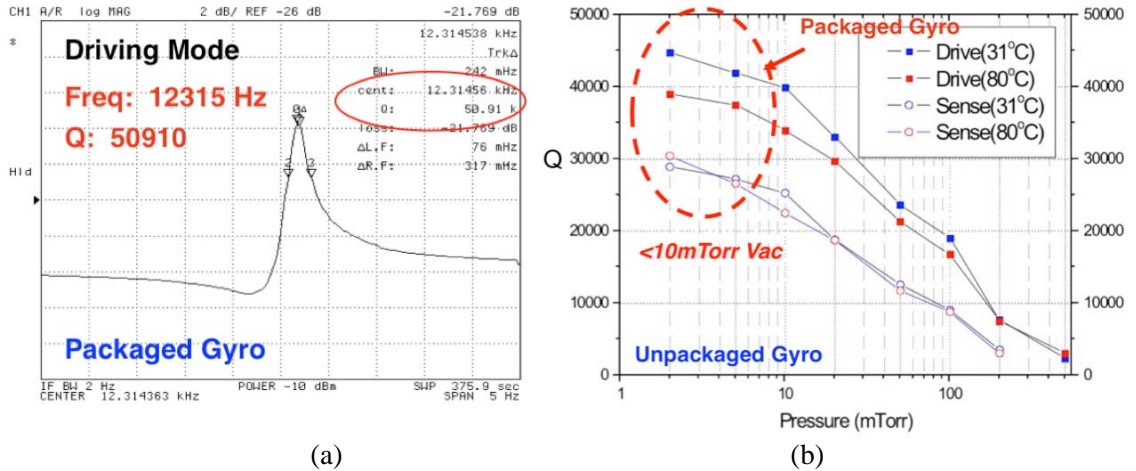
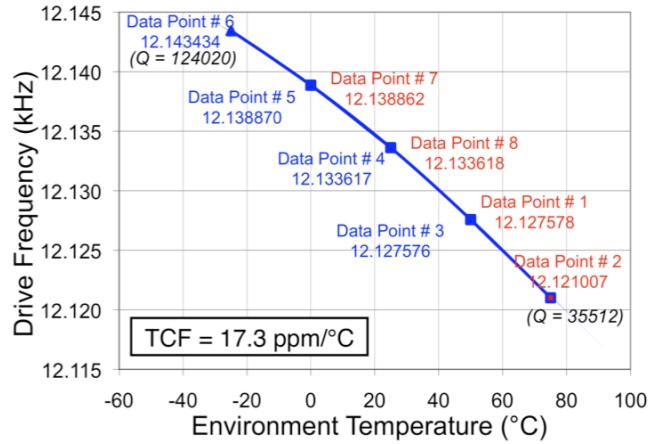


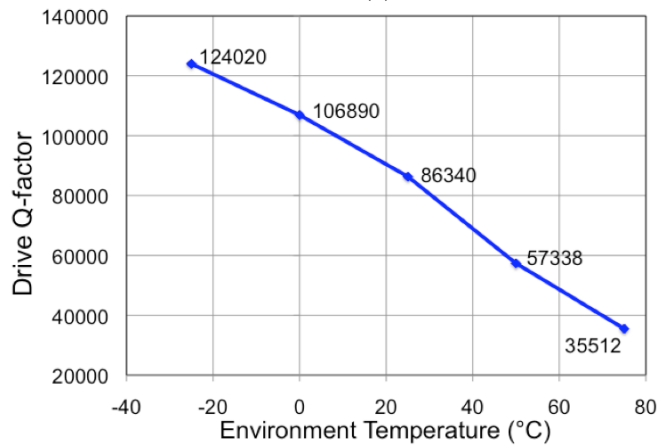
Figure 5.13 (a) Drive frequency response of the packaged gyroscope at 25 °C, and (b) quality factor of the unpackaged gyroscope with varying environment pressure level. High quality factor of the packaged gyroscope indicates that the vacuum level inside the package is less than 10 mTorr.

The vacuum packaged M²-TFG has been tested in a temperature chamber. Figure 5.14 shows the drive frequency change versus environmental temperature change from -25 °C to 70 °C. The drive frequency varies at 17.3 ppm/°C over a temperature range of 100 °C, but stays on average <1 ppm at the same temperature without any hysteresis during thermal cycling (Figure 5.14 (a)). The drive Q-factor reaches 124,000 at -25 °C, and 35,000 at 75 °C (Figure 5.14 (b)). The drive Q-factor is higher than that under mode-matched operation shown in Figure 5.11.

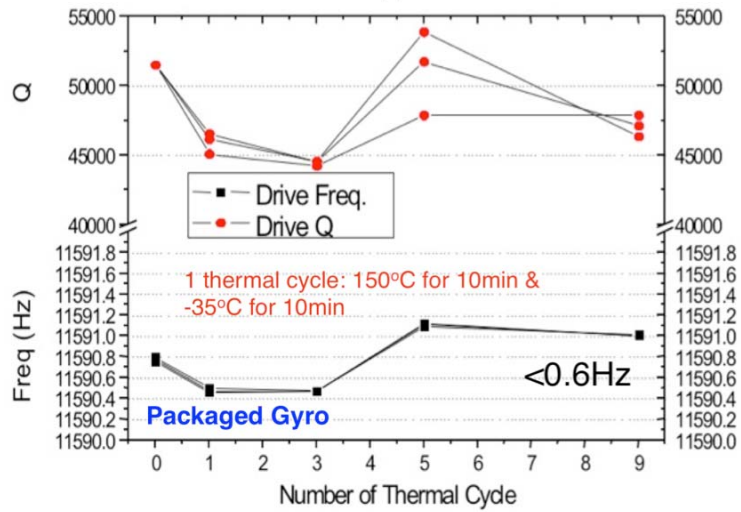
Thermal cycling at two extreme temperatures has been performed (Figure 5.14 (c)). The package experiences 150 °C for 10 min and -35 °C for 10 min during one thermal cycle. Each frequency response and Q-factor is measured at room temperature.



(a)



(b)



(c)

Figure 5.14 Temperature characteristics of the packaged gyroscopes. (a) Drive frequency variation with environment temperature cycling from $-30\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ (Tested at Georgia Institute of Technology). (b) Drive quality factor versus environment temperature. (c) Drive frequency and quality factor measurement data after thermal cycling test. The package experiences $150\text{ }^{\circ}\text{C}$ for 10 min and $-35\text{ }^{\circ}\text{C}$ for 10 min during one thermal cycle.

Table 5.2 shows the drive frequency of the gyroscope before and after packaging. This shows that the package does not affect the resonant frequency of the gyroscope. It also should be noted that the package provides effective protection during the dicing process, which involves severe vibrations.

Table 5.2 Drive mode frequency measured after major packaging step.

	Before Transfer (Drive mode freq.)	After Packaging (Drive mode freq.)	After Dicing (Drive mode freq.)
Die #1	-	15432 Hz	15423 Hz
Die #2	15597 Hz	15599 Hz	15598 Hz
Die #3	-	11748 Hz	11749 Hz
Die #4	-	11656 Hz	11655 Hz

5.4.4 Low-Power Oven-Control Performance

As shown in section 5.5.3, the resonant frequency of the gyroscope changes with environmental temperature variations. This frequency variation can be reduced by oven-controlling the gyroscope. Figure 5.15 is a schematic illustration for the oven-control test. The package die is placed in a temperature chamber operating from $-30\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$. A constant current of 1 mA is flowing through the temperature sensor, and a constant voltage (V_{heater}) is applied to the heater. The heater and temperature sensor are connected to a comparator chip which is connected to another voltage source for regulating the on/off set point (V_{set}). First, the heater heats the platform and gyroscope die until the temperature reaches to a set point ($80\text{ }^{\circ}\text{C}$). Once it reaches to the set point, the heater then keeps on/off controlled by the comparator and the feedback signal from the temperature sensor. The set point, V_{set} , is obtained from the temperature coefficient of resistance (TCR) of the temperature sensor made of thin film Pt.

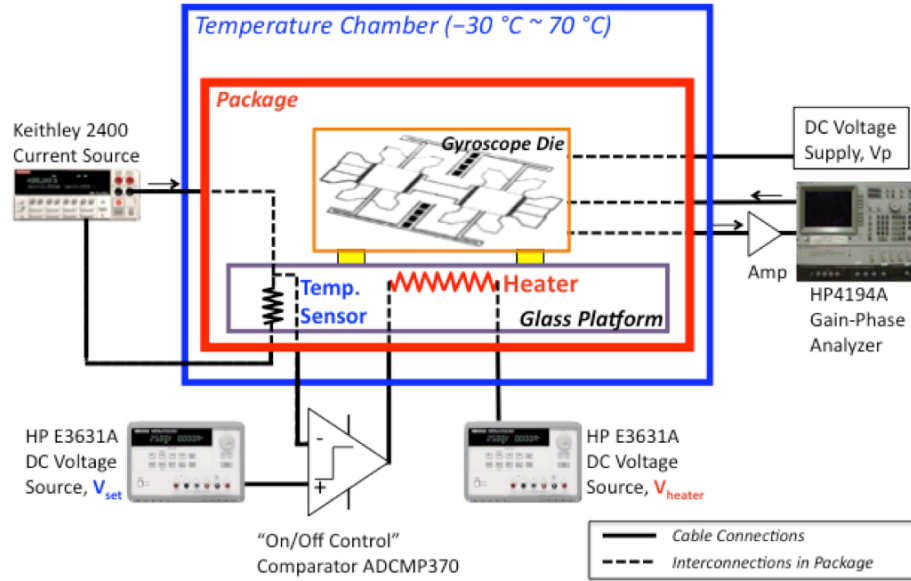


Figure 5.15 Schematic diagram for the oven-controlled gyroscope package test.

Table 5.3 summarizes the parameters for the oven-control test. The heater voltage, V_{heater} , needs to be high enough so that the platform can rise to the set temperature. As the V_{heater} increases, the time to reach the set point decreases.

Table 5.3 Summary of parameters for oven-control test.

Parameters	Values
Heater	<ul style="list-style-type: none"> - Material: Ti/Pt/Au 300 Å / 1000 Å / 3000 Å - Resistance: 200~250 Ω at Room temperature - $V_{heater} = 5$ V - Set point: 80 °C
Temperature Sensor	<ul style="list-style-type: none"> - Material: Ti/Pt 300 Å / 1000 Å - Resistance: 750~800 Ω at Room temperature - TCR: 2.7×10^{-3} - Cont. Current: 1 mA
Comparator	<ul style="list-style-type: none"> - ADCMP370 - Bias: 5 V
Temperature Chamber	- -30 °C ~ +70 °C ($\pm 0.5^\circ\text{C}$)

Figure 5.16 shows the measured drive frequency versus the environment temperature. As mentioned earlier, the drive frequency varies as the environment

temperature changes due to thermal expansion/contraction of materials. Without oven-control, the frequency changes 18.54 ppm/°C. The drive frequency variation decreases down to 0.96 ppm/°C, when the heated structure is oven-controlled at 80 °C. The drive frequencies are measured three times and averaged, and the standard error is ±0.005 Hz. This frequency change may come from a non-uniform temperature distribution across the gyroscope, because the heater is located on the platform and heat is transferred only through the bonding contact pads and radiation.

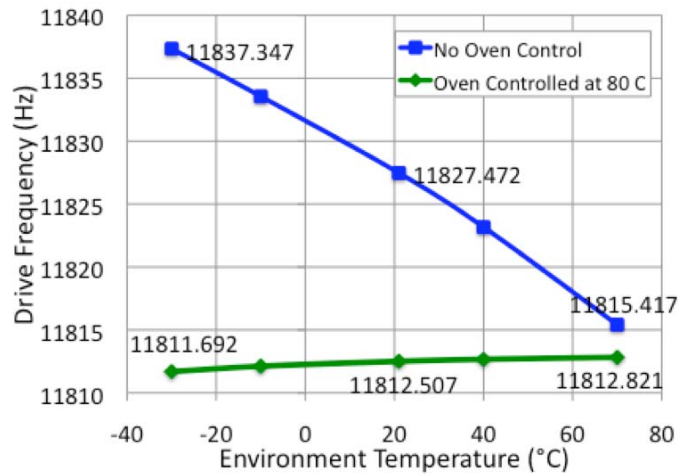


Figure 5.16 Drive frequency change with varying environment temperature (-30 °C ~ +70 °C).

Higher frequency stability of 0.22 ppm/°C is obtained using compensated oven-control (Figure 5.17), where the temperature setting is modified based on the actual environment temperature. The compensated temperature setting is obtained from the temperature dependency data of the drive frequency operating without oven-control (Figure 5.16)

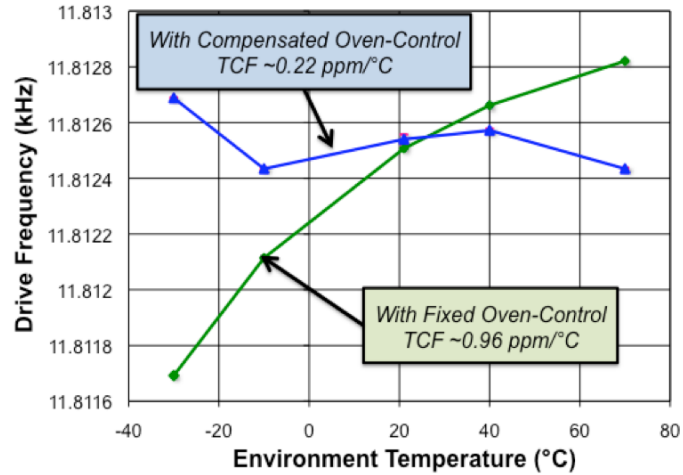


Figure 5.17 Drive frequency change with varying environment temperature (-30 °C ~ +70 °C) utilizing fixed oven-control and compensated oven-control.

Power consumption for the oven-control has been measured (Figure 5.18 (a)) to be 33 mW when heating the device to 80 °C with an ambient temperature of -30 °C; it decreases as the environment temperature increases. This corresponds to a thermal resistance of 3,300 K/W.

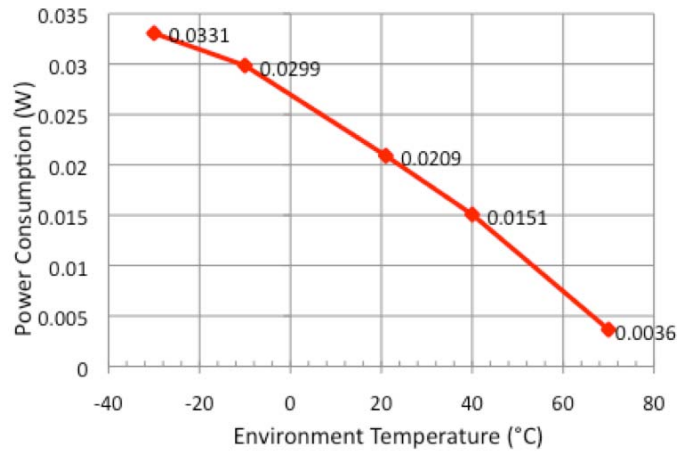


Figure 5.18 Measured power consumption for the oven-control with varying the external temperature.

5.5 Discussion

5.5.1 Package Size Optimization

Minimization of the package size is a critical factor in reducing total manufacturing cost. The package size is determined by the isolation suspension size, vertical feedthrough size and wafer bond ring size. The length of the suspension is determined by the MEMS device size, and the width is determined by the thermal and mechanical requirements. The width needs to be narrow to increase the thermal resistance and flexibility while providing enough stiffness for supporting the MEMS device. An alternative way to reduce footprint is to use dry etch in patterning the glass isolation suspension. Wet etching consumes a large area due to its isotropic etching characteristics. However, dry etch is not a batch process and is not a cost effective method.

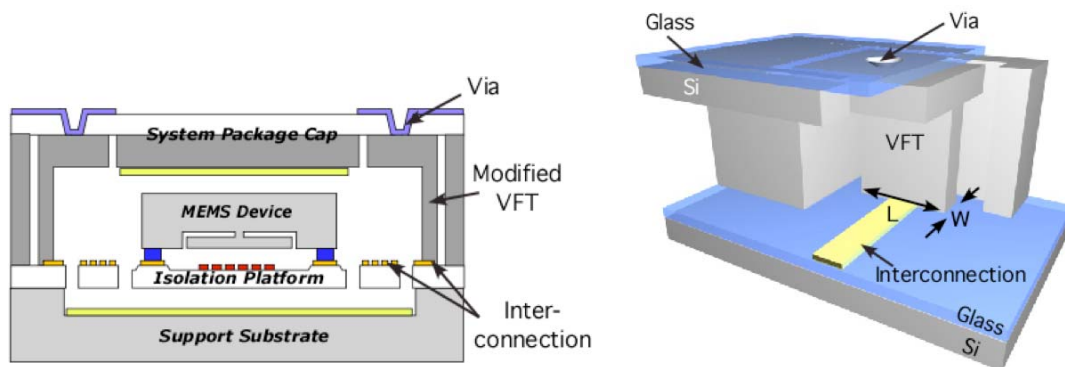


Figure 5.19 Schematic illustrations of the package with modified vertical feedthrough.

The vertical feedthroughs also consume area. As long as they provide low parasitics, they should be made as small as possible. Figure 5.19 shows a modified vertical feedthrough design to reduce the footprint area while maintaining the size of the

via the same. Preliminary experimental results show that a contact size of $100 \text{ (W)} \times 500 \text{ (L)} \mu\text{m}^2$ has contact resistance of $< 2 \Omega$.

The vertical feedthroughs are formed by the through-wafer DRIE. The height of the MEMS device determines the thickness of the cap wafer. As the thickness of the cap wafer increases, the etch time for patterning the feedthrough increases. This long time of silicon dry etch limits the minimization of the feedthroughs because of the limitation of the etch mask material or lateral etching. Therefore, the performance of the silicon DRIE tool is one of the factors in deciding the size of the vertical feedthroughs. Other factors such as contact resistance and robustness, which are related to the size of the feedthroughs are also important.

The bond ring width for vacuum sealing also needs to be optimized. The width needs to be small while maintaining the pressure inside the cavity and providing mechanical strength. It is desirable to study the relationship between the bond ring width and reliability of the vacuum seal.

5.5.2 Oven-Control Technique

In this chapter, we have demonstrated an oven-controlled package using an integrated heater and temperature sensor. Two major factors are involved in oven-control: (1) temperature measurement (by the temperature sensor) and (2) temperature control (of the heater).

For temperature measurement, two factors should be considered: proper temperature sensor selection, and proper sensor location. Generally, a temperature transducer senses temperature and converts it into current or voltage. Several factors should be considered in designing and selecting a temperature sensor: accuracy, stability,

response time, reliability, reproducibility, linearity of output, and operating temperature range [159]. There are a wide variety of sensors for measuring temperature including resistors, thermocouples, diodes/transistors and infrared/radiation sensors. Platinum resistors have been widely used for measuring temperature due to their stable, accurate, and linear performance over wide temperature ranges [160]. The thin film platinum sensor can also be easily integrated with desired electrical resistances using micro-fabrication techniques.

The location of the temperature sensor is important in order to minimize error in measuring the actual temperature. Figure 5.20 illustrates possible error sources in our package design. The actual temperature of the device ($T_s(r)$) at r_{s1} is not the same as the temperature measured by the integrated temperature sensor at r_{s2} . There are thermal resistances between the device and temperature sensor (R_{12}), between the device and the environment (R_{s-env}), and between the temperature sensor and the environment (R_{ts-env}). All these factors cause inaccurate temperature measurement in oven-controlling the device. To minimize this inaccuracy, the device and the temperature sensor need to be close to each other to minimize R_{12} , and other thermal resistances of R_{s-env} and R_{ts-env} need to be large. Heat between the device and the platform is only delivered through the bonding contacts and radiation. The thermal resistance between these two elements, R_{12} , can be reduced by adding additional auxiliary bonding pads for better thermal delivery.

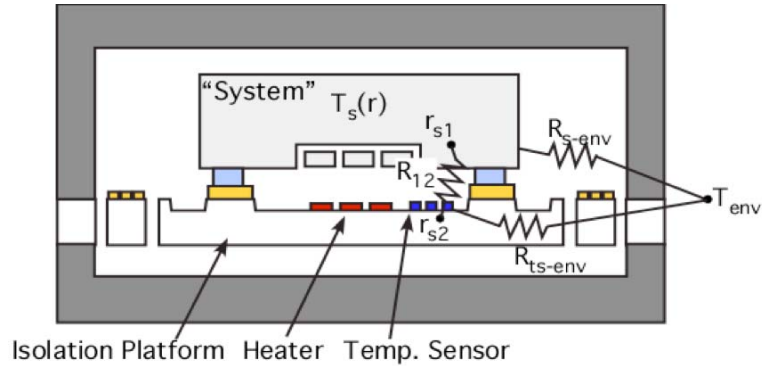


Figure 5.20 Schematic view of temperature measurement process in the environment-resistant package.

Alternative ways to measure temperature have been investigated to overcome the above-mentioned issues and increase the accuracy in oven-controlling the device. The general goal of measuring the temperature and oven controlling is to maintain the performance of the packaged device under environmental temperature variations. Some devices such as resonators [161, 162] and gyroscopes [21] have been used as temperature sensors utilizing the temperature dependency of the resonance amplitude. The resonance amplitude change due to temperature variation is used as a feedback signal in an oven-control system. In this system, the integrated heater is controlled to eliminate the change of the resonance amplitude.

The feedback control technique needs to be considered carefully in high-performance device packaging. Although on-off control is a cost-effective control technique, it is a nonlinear process because its set point (load) is not centered between the two output states (on and off states) [163]. The resulting temperature cycle often looks like saw-tooth and is not exactly centered about the set point. To minimize this nonlinearity, a derivative action can be implemented by adding a small resistance element to the on-off controller output [163]. By heating faster than the process itself, the

resistive element warms the temperature sensor enough to turn off the heater before the actual temperature reaches the set point. This additional operation can avoid overshoot and shorten the period and amplitude of the cycle. Advanced control techniques such as PID (Proportional, Integral, Derivative) control can eliminate issues including overshooting, ringing, and steady-state error, but require complicated control systems.

In general, the choice of proper temperature measurement and control technique depends on the device application, required performance level, and manufacturing cost.

5.6 Summary

In this chapter, a modified generic environment-resistant package technology has been presented. This package provides an oven-controlled environment with low power consumption, and long-term stable vacuum encapsulation with new robust vertical feedthroughs. By packaging a high performance MEMS gyroscope, the feasibility of this technology has been demonstrated. With the low-power oven-control, the thermal stability of the packaged gyroscope has been enhanced by 80×. This approach is suitable for many different high performance MEMS devices including resonators, accelerometers, infrared imagers, or any application requiring low power oven control, vibration isolation, and hermetic/vacuum packaging for stable operation.

Chapter 6

Conclusion

6.1 Summary

We have developed and demonstrated a generic wafer-level vacuum packaging technology for high performance microinstruments. This package provides high thermal and mechanical isolation by utilizing isolation suspensions and a platform, which allows for low power oven-control and vibration rejection. This generic packaging technology allows for handling and packaging a wide variety of MEMS devices. The package is capable of long-term stable vacuum encapsulation, and provides robust vertical feedthroughs.

To realize this packaging technology, several key approaches, including (1) thermal isolation from the environment, (2) vibration and shock protection, (3) generic MEMS device batch transfer, (4) wafer-level vacuum packaging, and (5) vertical feedthroughs with minimum footprint have been investigated.

Two types of isolation packages using these key technologies have been fabricated. The first package utilizes meandering metal suspensions, and has a simple design concept and possibly better mechanical isolation properties due to the ductile metal suspension. The second package utilizes glass suspensions and overcomes some of

the fabrication issues associated with metal suspensions. Both packages provide >3000 K/W of thermal resistance, which corresponds to less than 50 mW of power input to maintain the device at 80 °C when the environment temperature is at -50 °C. The glass suspensions are designed to reject high frequency (> 1 kHz) vibration, and the shock absorption layer protects the device from external shock.

The batch device transfer technique allows for the generic assembly of the devices onto the isolation suspensions/platform. This technique provides an accurate alignment, robust mechanical attachment, and electrical connections with low contact resistance. Incorporating the glass suspension, suspended structures have been realized without using any sacrificial layer. Dissimilar MEMS devices fabricated by different methods have been transferred and vacuum packaged on the same substrate.

Wafer-level vacuum encapsulation using wafer bonding has been demonstrated and evaluated by packaging Pirani gauges. Both gold-silicon eutectic bonded and anodically bonded package show high strength and uniformity across the wafer. The package has maintained a vacuum pressure of ~ 6 mTorr for ~ 1 year.

Two types of vertical feedthroughs have been investigated. The vertical feedthroughs on a thin glass wafer, which is suitable for small size package, allows for a low manufacturing cost. The vertical feedthroughs on the glass-silicon bonded wafer provide robust, low resistance and reliable signal paths without any vacuum leak.

By packaging a high performance MEMS gyroscope, the feasibility of this technology has been demonstrated. The package provides stable and reliable surrounding conditions in operating the gyroscope. With the low-power oven-control, the thermal stability of the packaged gyroscope has been enhanced 80 times.

Table 6.1 Summary of the environment-resistant package using glass isolation suspensions.

Categories	Features	Results
General	- Package size* : $12 \times 12 \times 1.7 \text{ mm}^3$ - Device size: $4.5 \times 4.5 \times 0.6 \text{ mm}^3$ (Pirani gauge chip and Gyroscope chip)	
Thermal Isolation	- Suspended device by isolation suspensions ($5 \times 0.6 \times 0.1 \text{ (L} \times \text{W} \times \text{T) mm}^3$) - Vacuum sealing with anti-radiation shield - Heater on platform: Ti/Pt/Au ($\sim 250 \Omega$) - Temp. sensor: Ti/Pt ($\sim 800 \Omega$) - Oven-control temperature: $80 \text{ }^\circ\text{C}$ (Environment temp: $-30 \text{ }^\circ\text{C} \sim 70 \text{ }^\circ\text{C}$)	- High thermal resistance: $>3,300 \text{ K/W}$ - Low power consumption: $<30 \text{ mW}$ - Drive freq. stability of gyros: $0.22 \text{ ppm}/^\circ\text{C}$ (with compensated oven-control)
Mechanical Isolation	- Suspended by glass isolation suspension - Shock absorption layer (gold)	- Vibration isolation, $<1 \text{ kHz}$ (analysis)
Device Transfer	- Batch die-level transfer using soft shadow mask and guide wafer - Generic batch process - Low temperature TLP contact bonding (In-Au): $<300 \text{ }^\circ\text{C}$	- High yield: $>90\%$ - Accurate alignment: $<35 \mu\text{m}$ - Stable contact: up to $>400 \text{ }^\circ\text{C}$ - Low contact resistance: $<1 \Omega$
Vacuum Packaging	- Au-Si eutectic bonding - Anodic bonding - Getter layer (Nano-getter [®]) - Bond ring width $200 \sim 500 \mu\text{m}$	- High vacuum level, $<10 \text{ mTorr}$ for $>1 \text{ year}$ - Low process temperature: $<370 \text{ }^\circ\text{C}$ - High Q-factor of vac. package gyroscope: $Q_{\text{eff}} \sim 65,000$ (mode-matched at $25 \text{ }^\circ\text{C}$)
Feedthrough	- Vertical feedthroughs on glass-silicon bonded substrate - Highly-doped silicon: $<0.01 \Omega\text{-cm}$ - Footprint: $600 \times 600 \mu\text{m}$	- Small footprint with 16, 20 and 24 feedthroughs - Low electrical resistance: $<2 \Omega$ - Low parasitic cap. : $<0.3 \text{ pF}$ (analysis)

* The package size is mostly decided by the device size, feedthrough size, isolation suspension width and bond ring width.

This new packaging approach is suitable for many different high performance MEMS devices including resonators, accelerometers, infrared imagers, or any application requiring low power oven control, vibration isolation, and hermetic/vacuum packaging

for stable operation. Table 6.1 summarizes the features and experimental results of the environment-resistant packages using the glass isolation suspensions.

6.2 Future Work

6.2.1 Generic Packaging

The environment-resistant package technology provides a generic platform for packaging various types of MEMS devices, including those that have a very thick MEMS device supported on a substrate. Figure 6.1 shows an illustration of a package design for packaging such a device. This device will be packaged using the same technologies, which have been developed for packaging the mode-matched tuning fork gyroscope designed at the Georgia Institute of Technology (Chapter 5). To accommodate the large thickness of the device, a hole is formed on the glass platform. The heater is patterned around the device for uniform heating.

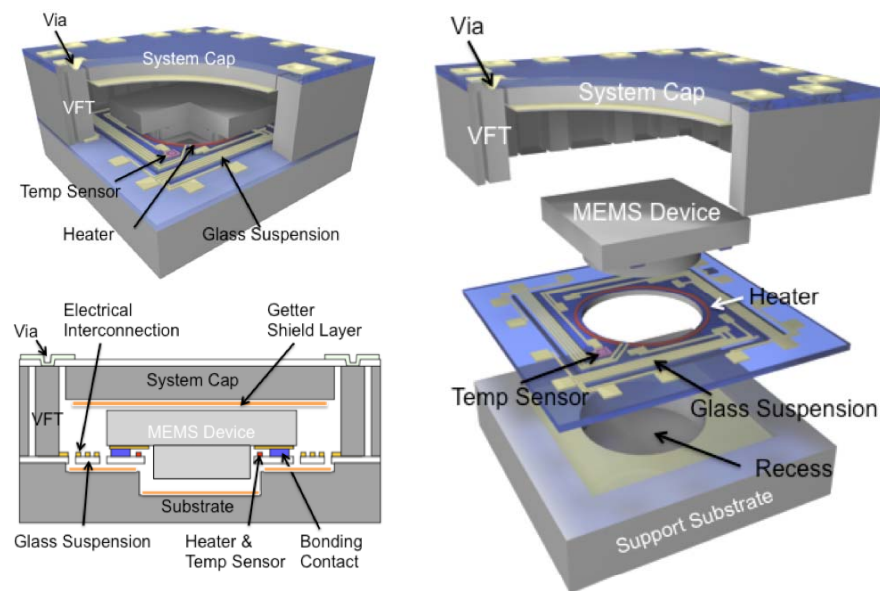


Figure 6.1 Schematic views of the environment-resistant package of a large MEMS device.

Oven-control techniques have been widely used in crystal oscillators or resonators including OCXO (Oven Controlled Crystal Oscilloscope). Traditional OCXO technology uses SC-cut crystals with high Q (around 500,000 for a 10 MHz round crystal). The crystal element is oven-controlled at a temperature 5-10 °C higher than the maximum operation temperature.

The main issues in the commercial products are the high current needed for heating the crystal, and the package size. Figure 6.2 shows a commercially available OCXO [164]. A commercial OCXO with the lowest power consumption requires ~ 1.5 W (in steady-state) with an initial warm-up power consumption around 3 to 4 W [164]. This is mostly because the commercial OCXOs use a separate vacuum-sealed crystal, which is mounted onto a PCB board. The heat is directly dissipated through this board, thus providing very low thermal isolation. The size of the package becomes large due to this packaging approach ($> 2 \times 1 \times 1 \text{ cm}^3$). The smallest OCXO available in the market comes in a DIP-14 package, which is not small enough to fit in today's portable devices [165].

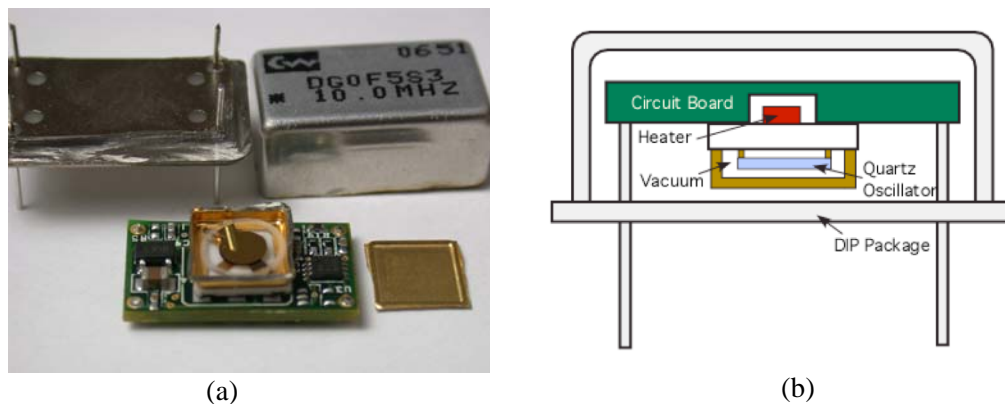


Figure 6.2 (a) A disassembled view of a commercial OCXO (Connor-Winfield Co., 14 PIN DIP 5.0V Stratum 3 HCMOS OCXO), and (b) a schematic illustration.

By packaging a crystal resonator on the isolation platform and vacuum encapsulation using the technology presented here, a small size OCXO with low power consumption can be obtained.

6.2.2 Optimization of the Package and Oven-Control System

The optimization and standardization of the package design and process is suggested. As discussed in section 5.5.1, the size of each component including vertical feedthroughs, isolation suspensions and the bond ring can be optimized to minimize the whole package size and the manufacturing cost.

Maximum process temperature is determined by the wafer bonding technique. Alternative bonding techniques including solder bonding and TLP bonding can be applied to reduce the process temperature.

Characterization of the vertical feedthroughs is also suggested. Besides the electrical resistance, other parasitics such as parasitic capacitance need to be characterized.

To enhance thermal stability, the oven-control system, including the temperature sensor and the heater can be optimized. In the case of a packaged resonating device, the resonance amplitude can be used for temperature sensing. Optimization of the temperature sensor location can also minimize the temperature measurement errors. More sophisticated control scheme such as PID (Proportional-Integral-Derivative) can improve the temperature control accuracy.

6.2.3 Extended Applications

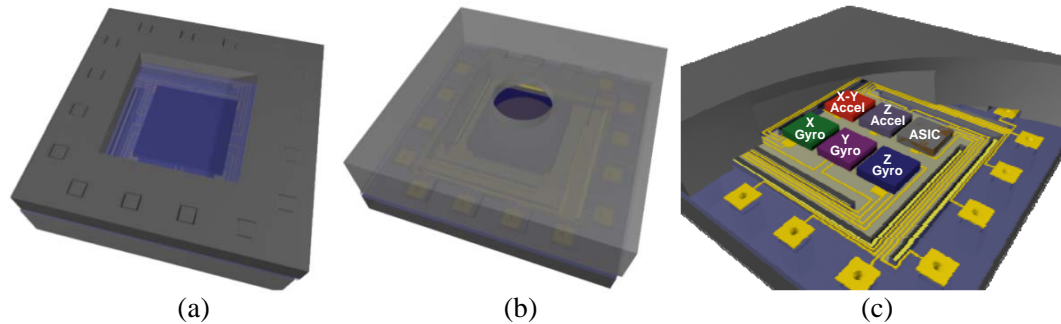


Figure 6.3 Package applications. (a) *Transparent packaging: CMOS image sensors, IR sensors.* (b) *Package with outlet: Pressure sensors, Microphones.* (c) *Multiple MEMS packaging.*

This developed package has many potential applications, as shown in Figure 6.3. The key technologies developed in this work can be modified for each application. The package can have transparent window for image sensing devices or IR sensing devices. Multiple chips, including MEMS device and ASIC, can be packed in one package. These chips can be fabricated using different processes, and then transferred onto one package die. The package may be extended to bio-MEMS applications, which mostly involve fluidics. Instead of electrical vertical feedthroughs, fluidic access paths may be formed.

This developed packaging technology has a large flexibility in design and fabrication. Therefore, it is suitable to accommodate a wide range of state-of-the-art MEMS technologies.

Appendices

A. Micro-Brush Press-On Contact: A New Technique for Room Temperature Electrical and Mechanical Attachment

A.1 Introduction

Packaging and assembly are two of the most important functions in manufacturing of micro and nano electro mechanical systems (MEMS/NEMS). Transfer of electrical signals and mechanical attachment of a device substrate to another part is often required. This is typically done by using solders of various types followed by a reflow which ranges typically from 100 °C to 300 °C. However, in many applications, it is desirable to form both the mechanical and electrical contacts at room temperature, and to avoid using special materials and solders.

This technique, illustrated in Figure A.1, overcomes these limitations by utilizing the mechanical engagement of arrays of high-aspect-ratio metal posts forming a micro-brush structure. The micro-brush contacts are formed by a simple process on top of a typical output pad on a chip (Figure A.1 (a)). The micro-brush connections are simple and behave the same way as when two dense hairbrushes are brought together and pressed, and thus become entangled (Figure A.1 (b-c)). When pressed, the metal posts

permanently bend and provide the required mechanical support and electrical connection (Figure A.1 (d)). Because of the large number of posts, and the large surface area provided by them, both the mechanical and electrical connections are quite high quality.

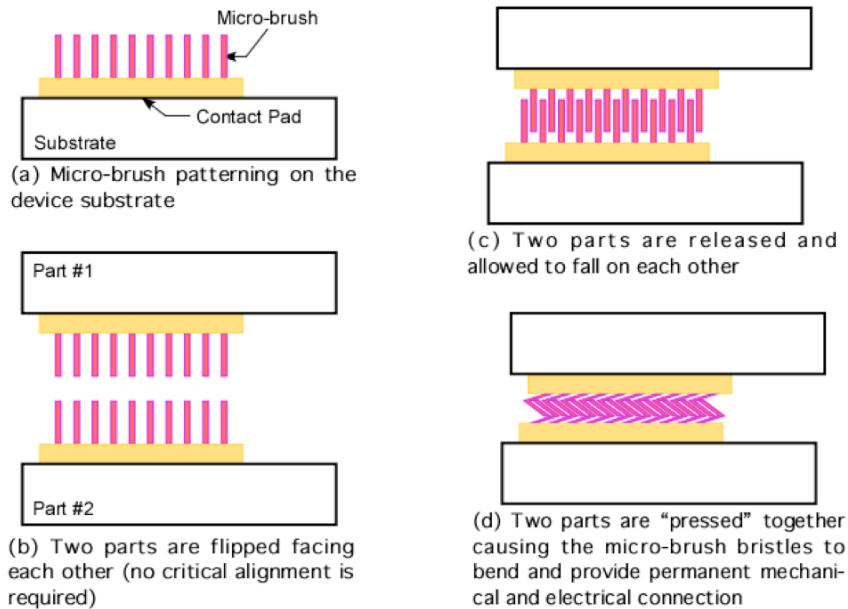


Figure A.1 Schematic procedure of the micro-brush press-on connection technique.

This technique offers a number of advantages. First, the attachment is performed at room temperature and does not need any high temperature steps. It is possible to deposit a thin layer of solder, or other eutectic materials, on top of the micro-brush to allow an optional solder contact (Figure A.2 (c)), in which case a solder reflow step will be needed. Second, there is no need for exact alignment. If any portions of the micro-brushes on the two sides overlap, mechanical and electrical connection can be made. Third, this technique can be applied as easily to a single die as it can to a full wafer. It is also applicable to printed circuit boards or any application where mechanical and electrical connection is needed. Finally, this technique can be performed at the end of a process and does not require any special processing steps.

The only known reported technique for mechanical attachment of devices was reported in [74, 75] and was called the micro Velcro. The mechanical structure, operation, fabrication, and design of the micro Velcro is different than the micro-brush presented here.

A.2 Design and Fabrication

To improve mechanical strength and reduce electrical contact resistance, the number and height of metal posts in the micro-brush should be increased. This requires the posts to have a very small foot print and a high aspect ratio. Figure A.2 shows a simple fabrication process, and a schematic illustration of a test sample. First, AZ9260 photoresist is spin coated on a wafer and soft-baked at 90 °C for 30 minutes in an oven. A glass wafer is used for this testing which makes it easy to align two samples manually. Then it is exposed and developed in AZ400K developer. It is necessary to reduce exposure and develop time by 40-60% of conventional time to get small, high aspect ratio structures. The patterned wafer is hard-baked at 110 °C for 30 min in an oven. The diameter of each photoresist post is 2 μm and the spacing between posts is 4 μm . A layer of chromium (300 Å) and gold (5000 Å) is sputtered directly on the patterned photoresist. The micro-brush structure is diced for a bonding test as illustrated in Figure A.2 (d). One can optionally deposit solder, or a soft contact metal like indium, to further improve mechanical/electrical contact quality Figure A.2 (c). In this case, a solder reflow is needed right after the press-on attachment at a nominal temperature.

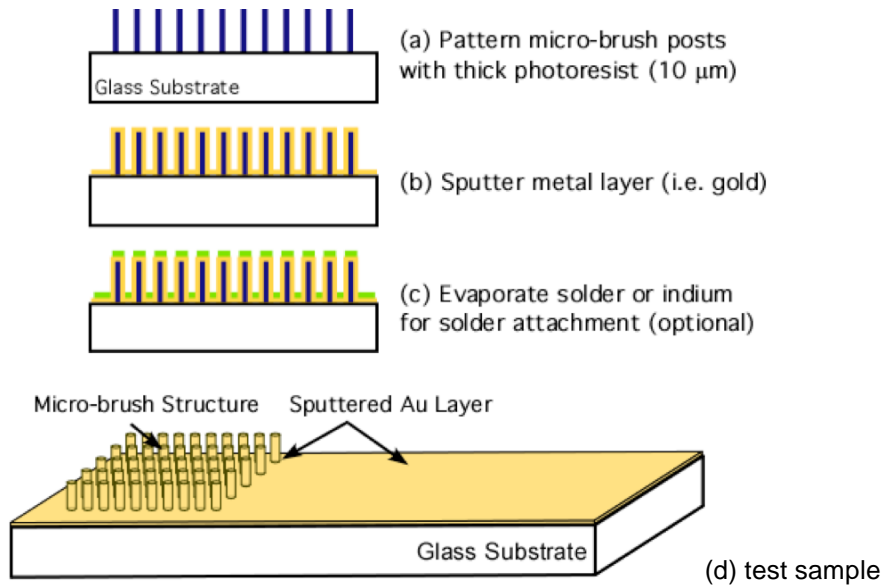


Figure A.2 Process flow of the micro-brush structures, and a schematic illustration of a test sample.

Figure A.3 shows SEM pictures of the fabricated micro-brush structure. The test micro-brush sample comprises 10,000 individual posts (3 μm diameter, 10 μm height, with spacing of 3 μm , providing an areal density of $\sim 2,700,000$ per cm^2).

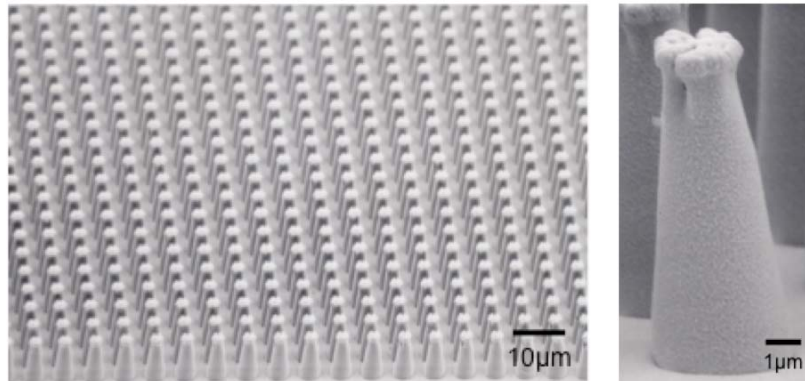


Figure A.3 SEM pictures of the fabricated micro-brush structures.

A.3 Testing

Test dies containing gold metal pads with gold micro-brush regions have been fabricated and tested for their electrical and mechanical performance. The press-on micro-brush connection is achieved by directly mating two micro-brush surfaces. Interlocking is accomplished by applying pressure to the upper sample. The alignment between two micro-brush patterns is done by naked eye.

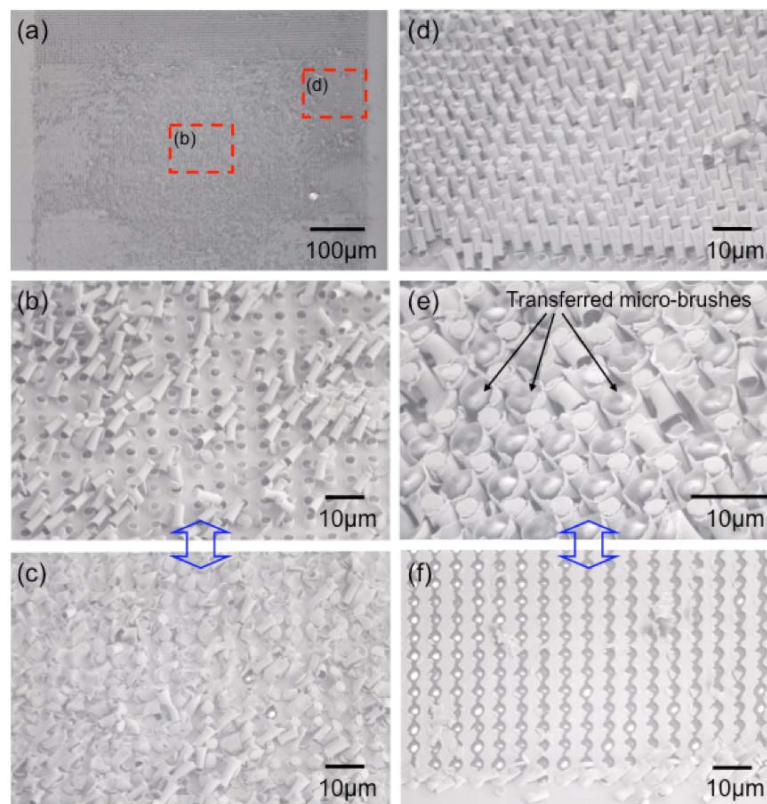


Figure A.4 SEM pictures of micro-brush surface after separation. (a) Whole micro-brush structure surface. (c) Counter part surface of (b). (e) Magnified view of a part of (d). (f) Counter part surface of (d) and (e).

The bonded samples are separated to investigate the surface structure by SEM. As shown in Figure A.4, when interlocked samples are forced apart, some of the metal posts are transferred from one substrate to the other. Obviously, this is a destructive test, but it

clearly indicates that the posts do interlock and that the connection is strong enough to break the posts upon separation. The electrical resistance of the contact between the two substrates has also been measured by a test setup shown in Figure A.5, and is shown to be less than 1Ω , which is quite adequate for most applications.

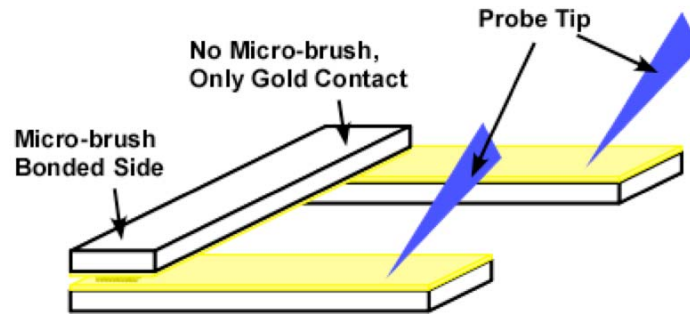


Figure A.5 A schematic illustration of an electrical resistance measurement test.

Solder or metal eutectics can also be optionally used. In some samples, indium has been deposited on the gold posts. The indium is heated to $200 \text{ }^\circ\text{C}$ for 10 minutes, causing it to melt and form a eutectic solder with gold [73, 154]. The solder creates a permanent physical connection and increases the mechanical strength or electrical conductivity. Because of solder reflow, the two samples do not need to be pressed together very hard.

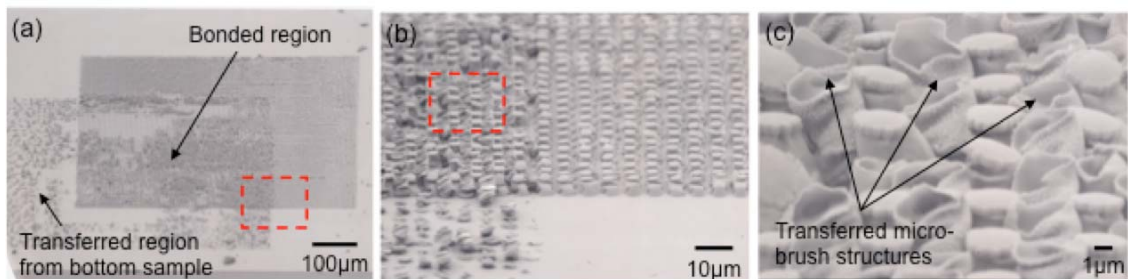


Figure A.6 SEM pictures of an upper micro-brush sample after being forced apart.

Test structures of this type have also been fabricated and tested. As shown in Figure A.6, micro-brush structures have again been transferred from one side to the other in the regions where micro-brushes overlap. There is some transfer in other regions as well

because of the solder. Electrical measurements of the solder-assisted micro-brush contacts have also shown a resistance of about 1Ω , very close to the first case with no solder, as expected.

The mechanical strength is sufficient to attach two test dies together and maintain the mechanical connection even after handling the individual dies.

A.4 Applications

The micro-brush technique can be used in many applications where both transfer of electrical signals and mechanical attachment of a device substrate to another part is required. One of the applications, shown in Figure A.7, is to transfer a MEMS device on a substrate for a thermally isolated microsystem packaging [79]. The micro-brushes are patterned on each 12 electrical pads, and the MEMS device die is pressed-onto the substrate. The attachment can be performed at room temperature, and does not need exact alignment.

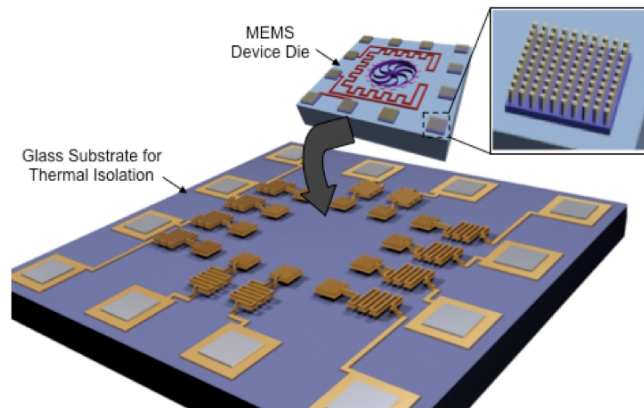


Figure A.7 A schematic view of a MEMS device transfer on a substrate using the micro-brush technique.

A.5 Summary

A new technique called micro-brush bonding for easy mechanical attachment and electrical interconnection between two parts has been proposed. Each of the two parts can be either a single die or a full wafer. They can be attached together in selected areas containing the “micro-brush” by simply “pressing” them together. A mechanical bonding of the two substrates with the micro-brush structures is successfully tested, and the electrical resistance of the bonded contact is less than 1 Ω . The bonding tests can be performed at room temperature without exact alignment. The test result shows that the micro-brush technique has the possibility to be used in many MEMS/NEMS applications.

B. Process Cost Analysis

Cost analysis for the environment-resistant package has been done on the basis of the charging system of LNF (Lurie Nanofabrication Facility) at the University of Michigan (December 2008). Process costs of the three different package techniques described in chapter 3, 4 and 5 have been analyzed (Tables B.1, B.2 and B.3). Only major steps including lithography, evaporation, wafer bonding and etching process are considered. The process cost for preparing MEMS devices is not considered. The clean room access fees, materials, and photo-masks need to be included in the total cost.

The total cost shown in each analysis is for one wafer process. The silicon DRIE, electroplating and wafer bonding process are not batch process. Therefore, the costs of these processes are multiplied by the number of the processing wafers. However, the costs of other processes including evaporation, lithography, and wet etching are independent of the number of wafers.

It should be noted that the silicon DRIE process is large fraction of the total cost (~15%). The cost of the DRIE increases as the number of the process wafer increases. Therefore, it is desirable to change this DRIE step to a batch process such as silicon wet etching.

Table B. 1 Cost calculation of the package in chapter 3.

Package in Chapter 3 (Ni electroplated isolation suspension with sacrificial layer of Unity™)		
#	Process	Cost (\$)
A	Preparing platform substrate	
<i>1</i>	<i>Sacrificial layer pattern</i>	
1.1	Sacrificial layer coating (Unity™)	
1.2	Evaporation (sacrificial layer etch mask)	70
1.3	Lithography	20
1.4	RIE (sacrificial layer etching)	20
<i>2</i>	<i>Suspension pattern</i>	
2.1	Evaporation (seed layer)	70
2.2	Lithography	20
2.3	Electroplating (nickel)	20
<i>3</i>	<i>Contact metal pattern (optional)</i>	
3.1	Lithography	20
3.2	Evaporation	70
B	Preparing cap wafer	
<i>1</i>	<i>Cavity formation</i>	
1.1	Lithography	20
1.2	Si DRIE	100
<i>2</i>	<i>Shield layer</i>	
2.1	Lithography	20
2.2	Evaporation	70
C	Device transfer (wafer-level device transfer)	
<i>1</i>	<i>Wafer bonding (In-Au TLP or Au-Au thermo-compression)</i>	40
<i>2</i>	<i>Device singulation using Si DRIE</i>	60
D	Vacuum packaging and feedthroughs	
<i>1</i>	<i>Wafer bonding (anodic bonding)</i>	40
<i>2</i>	<i>Vertical feedthroughs</i>	
2.1	Glass thinning by wet etching	20
2.2	Lithography	20
2.3	Glass wet etching (VFT)	20
2.4	Evaporation	70
Total cost		790

Table B. 2 Cost calculation of the package in chapter 4.

Package in Chapter 4 (Glass isolation suspension with VFT on platform substrate)		
#	Process	Cost (\$)
A Preparing platform substrate		
<i>1</i>	<i>Shallow recess</i>	
1.1	Lithography	20
1.2	Si DRIE	20
1.3	Evaporation (shield layer)	70
<i>2</i>	<i>Isolation platform and suspension</i>	
2.1	Wafer bonding (thin glass wafer)	40
2.2	Evaporation (wet etch mask)	70
2.3	Lithography	20
2.4	Glass wet etching (Via)	20
2.5	Lithography	20
2.6	Evaporation (interconnection)	70
2.7	Lithography	20
2.8	Evaporation (contact metal)	70
2.9	Evaporation (wet etch mask)	70
2.10	Lithography	20
2.11	Glass wet etching (isolation suspension)	20
B Preparing cap wafer		
<i>1</i>	<i>Cavity formation</i>	
1.1	Lithography	20
1.2	Si DRIE	100
1.3	Evaporation (shield layer)	70
<i>2</i>	<i>Wafer bond ring pattern</i>	
2.1	Evaporation (seed layer)	70
2.2	Lithography	20
2.3	Electroplating (gold)	20
C Device transfer (batch die-level transfer technique)		
<i>1</i>	<i>Evaporation (contact metal, w/ shadow mask)</i>	70
<i>2</i>	<i>Transfer bonding</i>	40
D Vacuum packaging and feedthroughs		
<i>1</i>	<i>Wafer bonding (Au-Si eutectic bonding)</i>	40
<i>2</i>	<i>Feedthrough formation</i>	
2.1	Lithography	20
2.2	Si DRIE	60
Total cost		1,080

Table B. 3 Cost calculation of the package in chapter 5.

Package in Chapter 5 (Glass isolation suspension with VFT on cap wafer)		
#	Process	Cost (\$)
A Preparing platform substrate		
<i>1</i>	<i>Shallow recess</i>	
1.1	Lithography	20
1.2	Si DRIE	20
1.3	Evaporation (shield layer)	70
<i>2 Isolation platform and suspension</i>		
2.1	Wafer bonding (thin glass wafer)	40
2.2	Evaporation (wet etch mask)	70
2.3	Lithography	20
2.4	Glass wet etching (shallow recess)	20
2.5	Lithography	20
2.6	Evaporation (interconnection)	70
2.7	Lithography	20
2.8	Evaporation (heater, temperature sensor)	70
2.9	Evaporation (wet etch mask)	70
2.10	Lithography	20
2.11	Glass wet etching (isolation suspension)	20
B Preparing cap wafer		
<i>1</i>	<i>Via formation</i>	
1.1	Lithography	20
1.2	Si DRIE	40
1.3	Wafer bonding (glass)	40
1.4	Evaporation (wet etch mask)	70
1.5	Lithography	20
1.6	Glass wet etching (via)	20
1.7	Evaporation (contact metal, w/ shadow mask)	70
<i>2 Cavity formation</i>		
2.1	Lithography	20
2.2	Si DRIE	100
2.3	Evaporation (shield layer)	70
C Device transfer (batch die-level transfer technique)		
<i>1</i>	<i>Evaporation (contact metal, w/ shadow mask)</i>	70
<i>2</i>	<i>Transfer bonding</i>	40
D Vacuum packaging		
<i>1</i>	<i>Wafer bonding (anodic bonding)</i>	40
Total cost		1,170

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