THE UNIVERSITY OF MICHIGAN

INDUSTRY PROGRAM OF THE COLLEGE OF ENGINEERING

LOGICAL OPERATIONS ON ELECTRONIC DIFFERENTIAL ANALYZERS

Robert N. Linebarger

Instrumentation Engineering
Program

September, 1960

IP-466

PREFACE

This work was performed by Robert N. Linebarger as a research project in partial fulfillment of the requirements for the Professional Degree, Instrumentation Engineer, at The University of Michigan, Ann Arbor, Michigan, August, 1960.

ACKNOWLEDGMENTS

The author wishes to acknowledge his appreciation for the guidance and encouragement of Professors R. M. Howe and D. T. Greenwood of The University of Michigan in the preparation of this study. In addition, sincere appreciation is extended to the faculty of the Instrumentation Engineering Program, The University of Michigan, for the Henry E. Riggs Fellowship which has made possible this study and the professional degree program during the past year.

In particular, special thanks go to my wife, Joyce, without whose helpful encouragement and many patient hours of effort this thesis would not have been possible.

TABLE OF CONTENTS

TABLE OF CONTENTS CONT'D

SUMMARY

Circuits for performing logic can be easily implemented using diode circuitry on differential analyzers. Conventional "and", "or", "negate" logical circuitry can be realized using three basic modes of binary signal inputs and outputs.

Logical expressions involving ordering relations can also be conveniently implemented by using operational amplifiers. In particular, it is possible to implement expressions involving both continuous inputs for ordering relations and boolean variable inputs within a single amplifier circuit. Standard Boolean Algebra reduction techniques are available for simplifying these logical expressions, in addition to set theory class inclusing-exclusion principles.

It is also possible to implement a logical system, described by a modified Boolean Algebra, which operates with the maximum and minimum of a set of continuous input signals. A summary of rules for reduction of logical expressions is given, and the circuitry for realizing any of the valid boolean identities is shown to be derived from a basic operational amplifier circuit.

Applications of the above ordering logic are made to an optimalizing control system and a duty cycle optimizing controller.

LIST OF SYMBOLS

A, B, C, ...	Continuous Signal Constants
X, Y, Z, ...	Continuous Input Signals to Logic Network
e, t, ...	Binary output signals from operational amplifier
x, y, z, ...	Binary input signals to logic network
$\bar{t}$, $\bar{e}$,	Boolean Algebra complement of input signal t, e, ...
$\subseteq$	Class inclusion operator
$\cdot$	Logical "and" operator
+, V	Logical inclusive "or" operator

CHAPTER 1

INTRODUCTION

1.1 General

In the past, applications of differential analyzer equipment have in general been restricted to systems involving continuous signals. It is the purpose of this paper, however, to demonstrate that computer amplifiers, with associated non-linear circuitry, possess very effective logical properties. This is particularly true when dealing with logical operations on continuous signals, such as comparisons, maximization, or minimization.

Three basic logical operations on differential analyzer equipment are described: (1) Conventional "and", "or", "negate" logic, (2) ordering relation logic, and (3) continuous signal logic. In addition, applications of the above logical operations to an optimalizing control system and a duty cycle optimizing system are described, including logical implementation and results.

1.2 Basic Logical Properties of Operational Amplifiers with Diode Input Circuitry

Operational amplifiers as used on conventional differential analyzer equipment are primarily used for linear operations upon computed variables. They possess four basic characteristics, however, that allow effective logical operations to be performed. These characteristics are:

(1) Power gain through system

(2) Linear input-output relationship

(3) High sensitivity to input polarity when operated with no external feedback impedance

(4) Continuous signal inputs of either positive or negative polarity

Because of their high gain, conventional operational amplifiers, with no external feedback impedance, can be used as binary devices. Figure 1-1 shows a conventional amplifier system used for binary output.

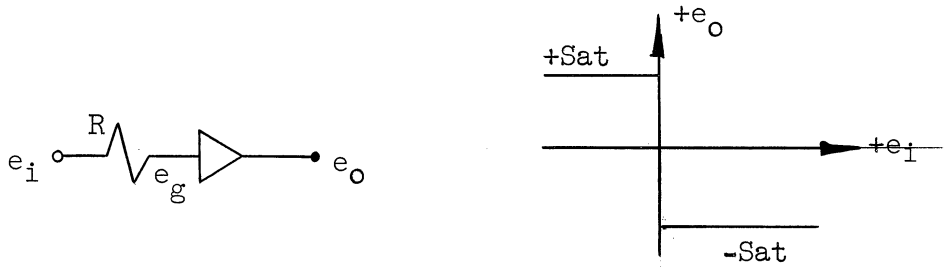


Figure 1-1 (a) Conventional System for Binary Output
(b) Input-Output Voltage Relationships

The grid voltage point, e_g, becomes highly sensitive to input polarity and magnitude. Thus, with either binary or continuous input signals having two possible polarities, a binary amplifier output can be obtained.

The amplifier binary output can be amplitude limited by using a matched zener diode pair shunting circuit shown in Figure 1-2.

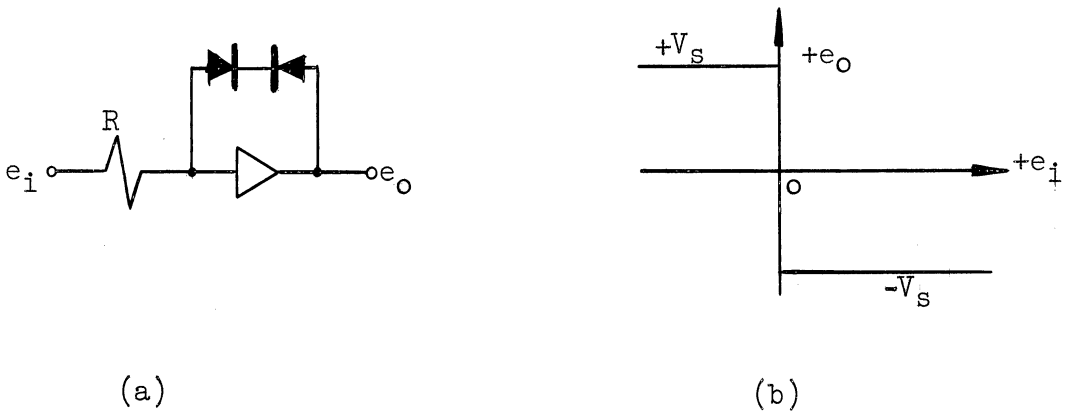


Figure 1-2 (a) Zener Diode Limited Amplifier
(b) Input-Output Voltage Relationships.
$|V_s|$ controlled by zener diode breakdown voltage.

Assuming no grid current drawn and the existance of a virtual ground at point e_g for all time, the amplifier output will drive to either of its zener diode saturating levels depending upon the polarity of the input voltage.

Note that for the above type of element, the polarity of the input signal represents the binary nature of the signal. Thus, input signals may be continuous, multileveled discrete, or binary. The binary output of the element will be controlled strictly by the polarity of the input. Typical binary inputs then become as shown in Figure 1-3.

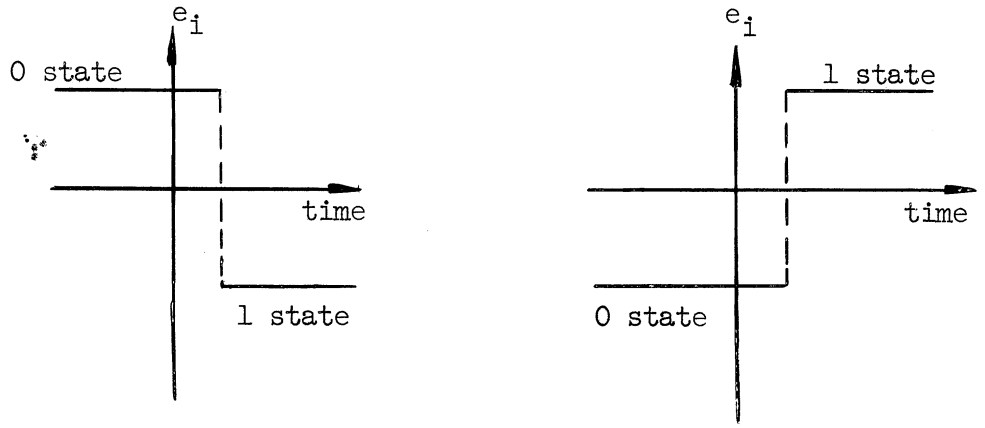


Figure 1-3 Typical Notation for Binary Input Signals.

By placing a small bias signal on the input, the binary output may be made sensitive to amplitudes of the input, as shown in Figure 1-4.

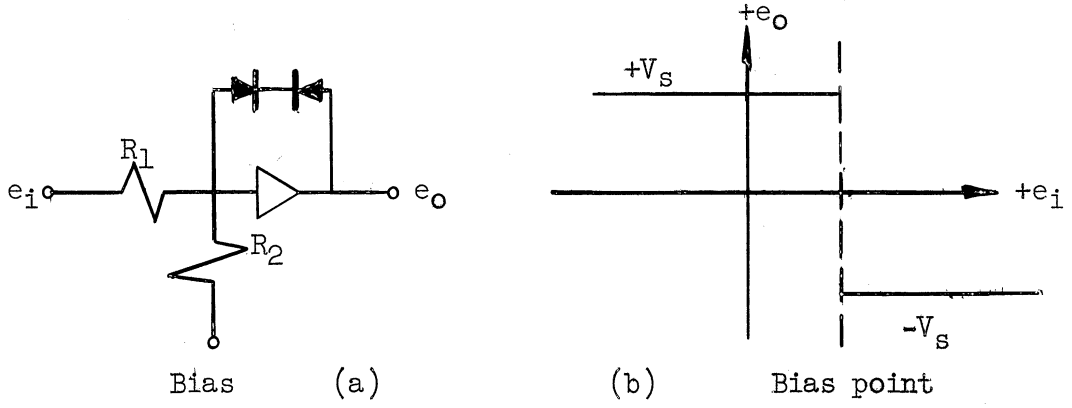


Figure 1-4 (a) Amplitude sensitive binary element
(b) Input-output voltage relationships

In this case, depending upon the polarity of the bias signal, only a single polarity signal with two levels need be used. Note that the response of the element, Figure 1-4(b), is equivalent to that of Figure 1-2 with the switching point moved by the bias value, allowing single polarity inputs to give a binary output depending upon their magnitude.

By shunting the amplifier with a conventional diode, one of the saturation levels may be reduced to near ground potential. Figure 1-5 shows two such circuits and the binary outputs generated. Note that the zero level voltage will have a slight bias due to the voltage drop through the diode.

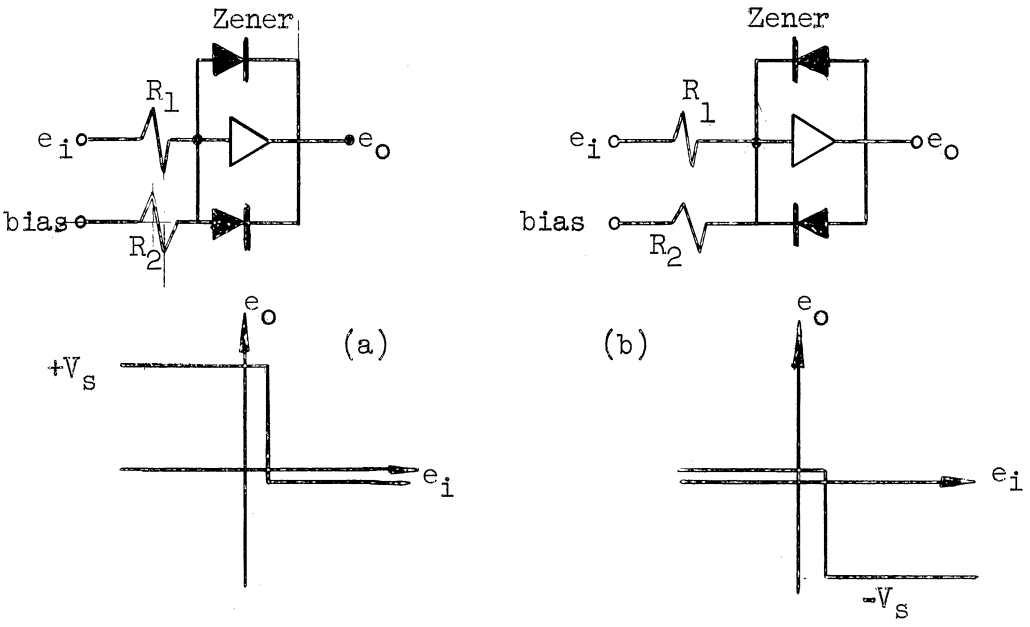


Figure 1-5 Circuits for Generating Zero Voltage Binary Output Level.

1.3 Operation Modes

In conventional switching systems using operational amplifiers, three possible operating modes are available for binary input signals. Figure 1-6 shows these operating modes for a conventional binary output.

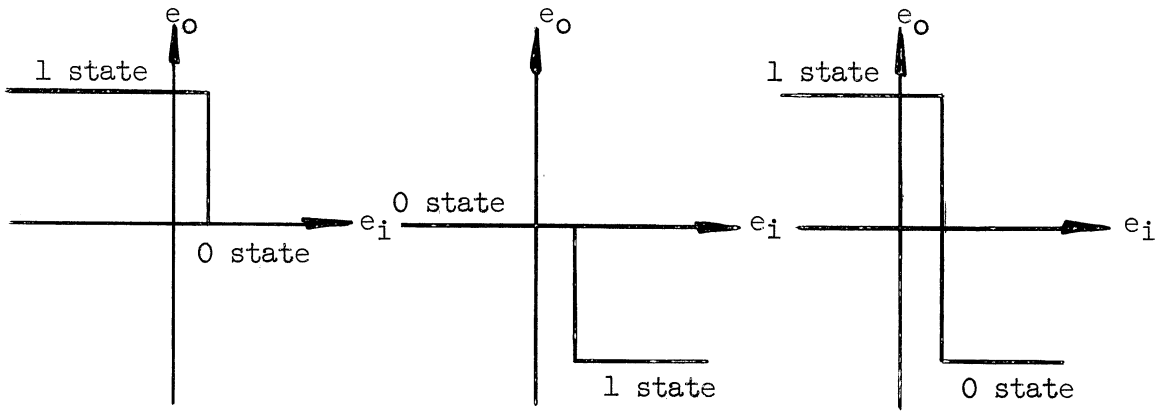


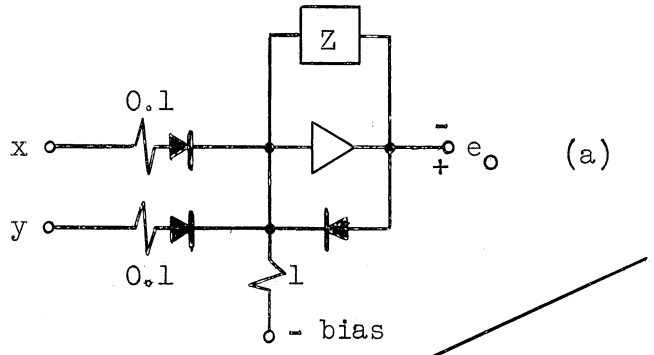
Figure 1-6 Typical Input Output Relations for Conventional Binary Signal Operating Modes

Note that each of the modes of operation may have their 0 and 1 state notation reversed, giving six possible combinations of binary signal notation.

CHAPTER 2

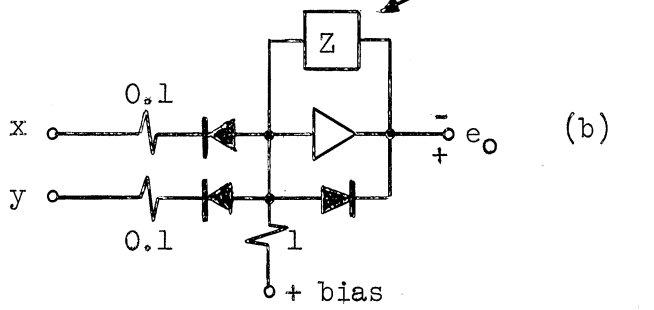
CONVENTIONAL "AND", "OR" LOGICAL OPERATIONS

Using the three possible modes shown in Figure 1-6, conventional "and", "or", "negate" logic may be implemented using operational amplifiers with diode circuits. These logic circuits are directly analogous to conventional active circuitry used for digital computer logic. When operating in modes 1 and 2, however, additional bias inputs must be used to guarantee proper circuit performance for zero level signal inputs. Figure 2-1 shows the inclusive "or", x or y or both, function implementation for the three modes of inputs. Thus, in Figure 2-1 (a) for example, if the x input is



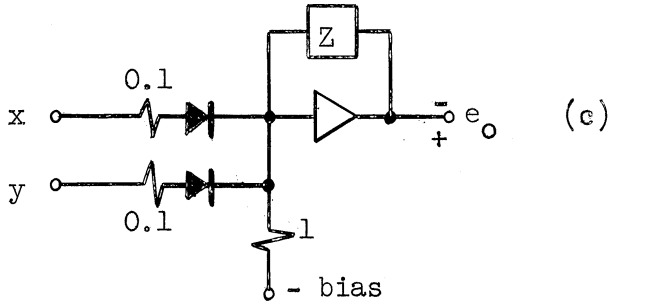
(a) Mode 1 $e_{o_-} = -(x + y)$

NOTE: This notation implies a matched zener diode pair-see Figure 1-4(a)



(b) Mode 2 $e_{o_+} = -(x + y)$

NOTE: The top polarity indicates amplifier output under input controls. The bottom polarity is output when the bias controls.



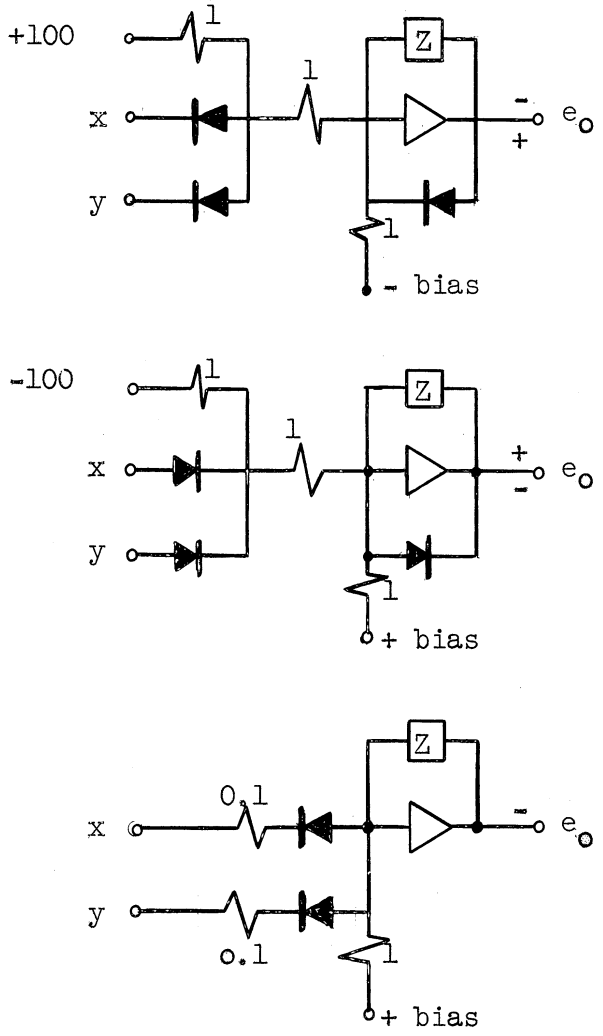
(c) Mode 3 $e_{o_-} = -(x + y)$

Figure 2-1 Inclusive "or" Circuits for Three Modes of Operation.

positive or the y input positive or if they are both positive, the amplifier output is negative. Only when both inputs are negative are both input diodes blocked. In this condition the negative bias takes control, and the amplifier output becomes positive. Hence, the negative amplifier output represents an input of x or y or both, the inclusive "or" function. The operation of the two other circuits of Figure 2-1 are directly analogous. Note that all three modes of operation require zener shunting diodes to control the limiting saturation values. In addition, a slight bias voltage is applied to insure the amplifier output going to the opposite state when both diodes are cut off. In all three modes, it is assumed that the 1 state voltage is of sufficient magnitude to avoid a threshold effect from either the input diodes or bias input.

Because of the sign reversal in the operational amplifier, the outputs appear in the dual form of the mode being used, i.e., having opposite polarity. This characteristic will later be shown to be a definite advantage in simplifying logic implementation.

Figure 2-2 shows the "and" circuit implementation for all 3 modes of inputs. Thus, in Figure 2-2 (a) for example, if both the x input and the y input are simultaneously positive, both diodes are blocked. In this condition, the negative bias takes control and the output becomes positive. The negative amplifier output then represents the input of both x and y together, the logical "and" function. Again, the operation of the other two circuits of Figure 2-2 are directly analogous.



(a) Mode 1 $e_{o_-} = -(x \cdot y)$

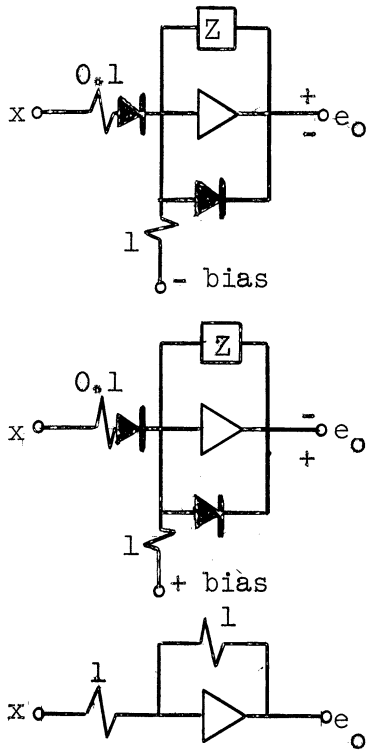
(b) Mode 2 $e_{o_-} = -(x \cdot y)$

(c) Mode 3 $e_{o_-} = -(x \cdot y)$

Figure 2-2 "and" Circuit Implementation of 3 Operating Modes.

Note that for implementing the "and" operation in Figure 2-2, two bias signals must be used, the first to control the input grid when the logical condition is met and the second to take control when the condition fails. Mode 3 operation displays the simplest implementation technique.

Figure 2-3 shows the implementation for complementation elements in the three modes of operation.



(a) Mode 1 $e_{o_{\pm}} = \bar{x}$

(b) Mode 2 $e_{o_{\pm}} = \bar{x}$

(c) Mode 3 $e_o = \bar{x} = -x$

Figure 2-3 Complementation Circuits for 3 Operating Modes.

Complementation using modes 1 and 2 are directly analogous to signal inversion except for the limiting effect upon the output. Again note that mode 3 allows the simplest implementation - a simple inverter becomes the complementation device with no diodes required.

It is of interest to note the resemblence of the circuits of Figures 2-1(a), 2-2(a) and 2-3(a) to the operational circuits of conventional digital logic elements for binary inputs, as shown in Figure 2-4.

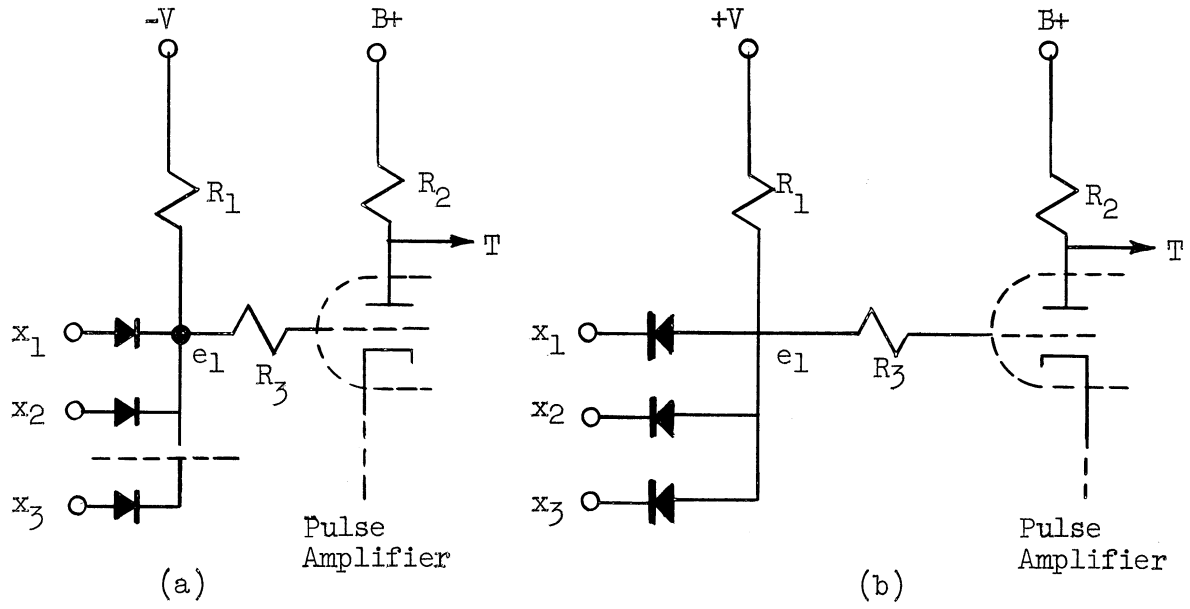


Figure 2-4 Conventional Pulsed Signal Logical Circuitry
(a) Inclusive "or" (b) "and" Circuit.

The analogy between the two systems, pulse circuit logic and operational amplifier logic, carries over completely since the operational amplifier acts only as a power gain device for its logic. For binary input signals, the linear characteristics of the amplifier are not needed. However, for ordering logic operations, and maximum-minimum signal logic to be described later, the linear characteristics of operational amplifier equipment provide convenient logical outputs.

Using binary input signals of mode 1, 2, and 3 operation, it has been shown that logical elements can be constructed from operational amplifier equipment in a very straightforward fashion. Hence, logical expressions in canonical form (see Appendix 1) can be implemented quite quickly for experimentation on analog equipment.

CHAPTER 3

LOGICAL OPERATIONS INVOLVING ORDERING RELATIONS

3.1 Basic Circuits

The existance of a virtual ground at the input to an operational amplifier allows effective ordering relation logical operations to be performed. By means of diode circuitry, the complete logical system, as derived in Appendix 1, can be implemented using operational amplifiers.

The previous chapter has shown that operational amplifier circuits can operate effectively as binary logical elements, summarized in Figures 2-1, 2-2, and 2-3. If a modification is now made in the diode placement, an interesting logical element involving ordering relations is created as shown in Figure 3-1.

X,Y = Continuous Signals

t = Binary Signal

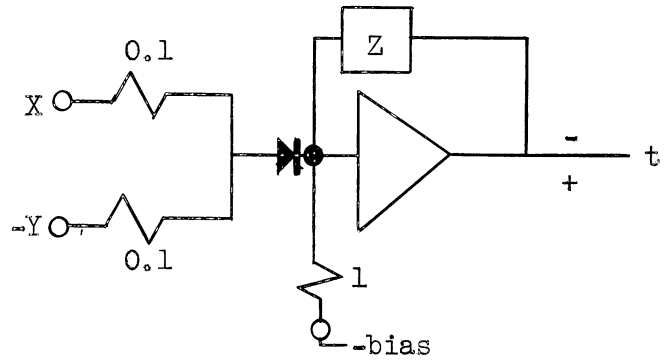


Figure 3-1 Basic Logic Circuitry for Ordering Relations.

Assuming the inputs X, Y to be continuous variables such that

$$0 < X < E_{+ref}$$

$$0 < Y < E_{+ref}$$

Then from Figure 3-1, the following boolean expression can be written

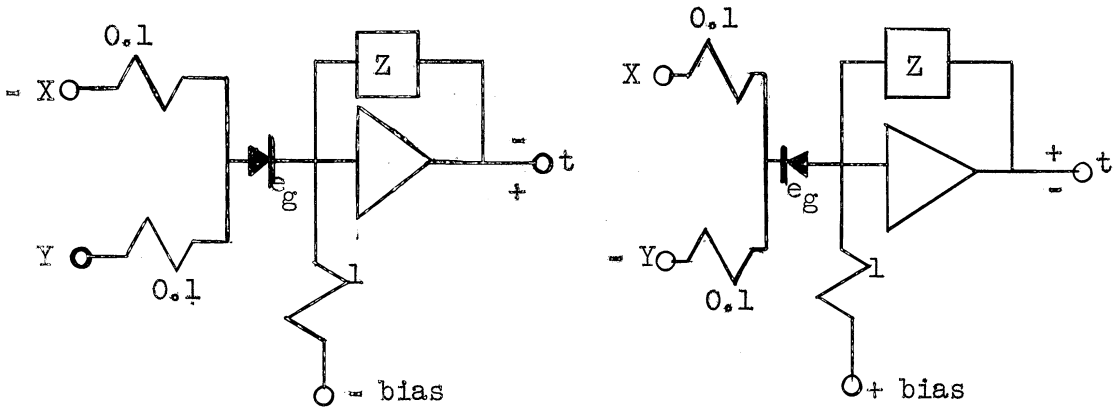
for the output:

$$t_{-} = (X > Y) \qquad (3\text{-}1)$$

Where: t_{-} = Binary output of amplifier operating in mode 1, 2, or 3 depending upon validity of boolean expression on right hand side of equation

( ) = Denotes a boolean expression involving ordering relations and continuous input variables.

Likewise, by either reversing input variable polarities or diode direction, the dual operation may be generated, as shown in Figure 3-2.



(a) $t_{-} = (X < Y)$ (b) $t_{+} = (X \leqslant Y)$

Figure 3-2 Dual Ordering Relation Circuitry.
(a) by reversing input signal polarities
(b) by reversing diode direction and bias

Hence, because of the virtual ground existing at point e_g (Figure 3-2), the operational amplifier continuously compares the two input signals and generates a binary output according to the larger of the two inputs. The action is a special case of the response of an open feedback amplifier to multiple inputs, as shown in Figure 3-3.

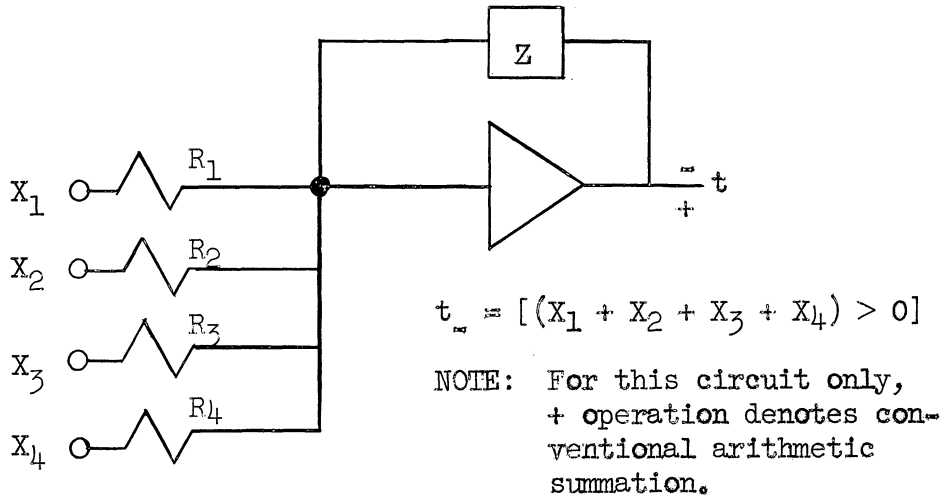


Figure 3-3 Ordering Relation of Conventional Open Loop Amplifier Operation With Multiple Inputs.

The action of the diodes in Figure 3-2 serve to eliminate any coupling between two or more pairs of inputs to the same amplifier.

The basic ordering relation logic may be implemented using the principle of logical duality. As discussed in Appendix 1, for each unique circuit configuration there are two possible outputs, each the dual of the other. For the basic ordering relation, a summary of the possible circuit configurations is presented in Figure 3-4.

3.2 Canonical Forms

As discussed in Appendix 1, the canonical forms of ordering relationships may be implemented using a single operational amplifier. First consider the disjunction normal form (Maxterm) given by Equation (3-2)

$$t_- = (X > A) + (Y > B) + (Z > C) \quad \text{----} \qquad (3\text{-}2)$$

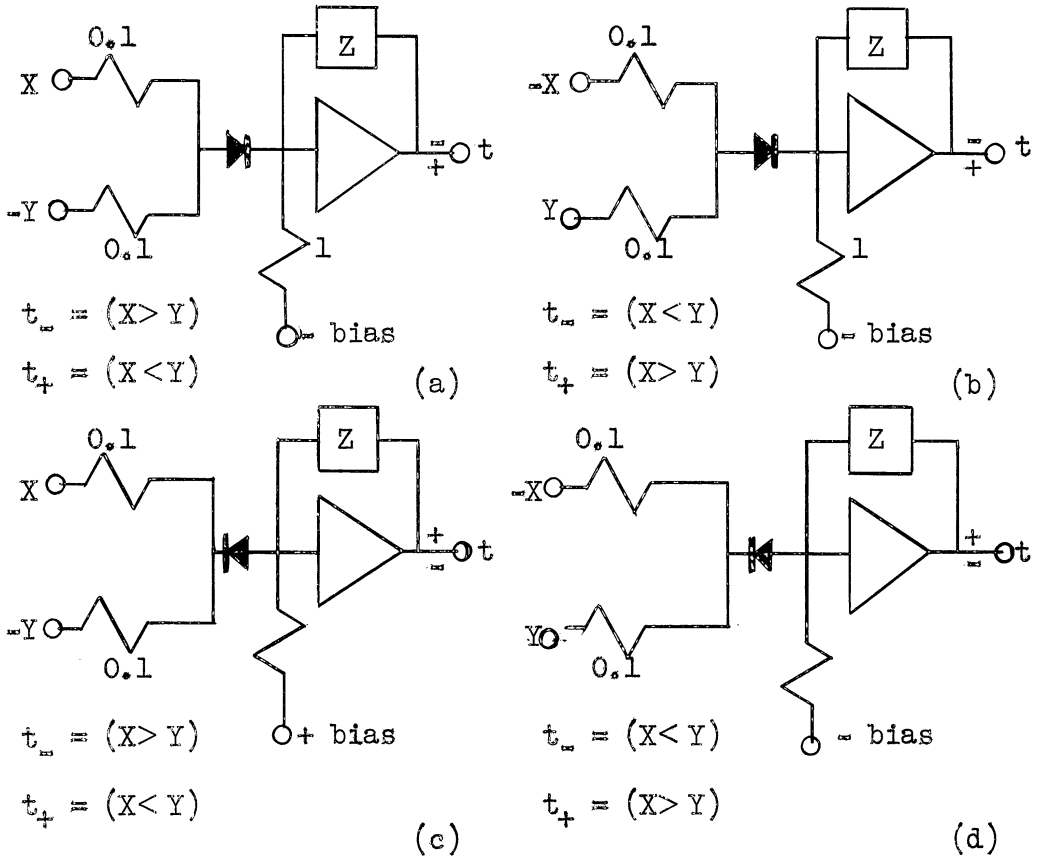


Figure 3-4 Circuit Duals for Basic Ordering Relation Logic

Figure 3-5 shows the implementation for the first three terms of Equation (3-2). From Figure 3-5, if any one of the diodes conduct, the amplifier output becomes negatively saturated. Hence, if the relations (X > A) or (Y > B) or (Z > C) or any combination of them are true, the amplifier is driven hard into negative saturation, limited by the zener diode breakdown voltage. This element then generates an inclusive "or" function using ordering relations.

$t_- = (X > A) + (Y > B) + (Z > C)$

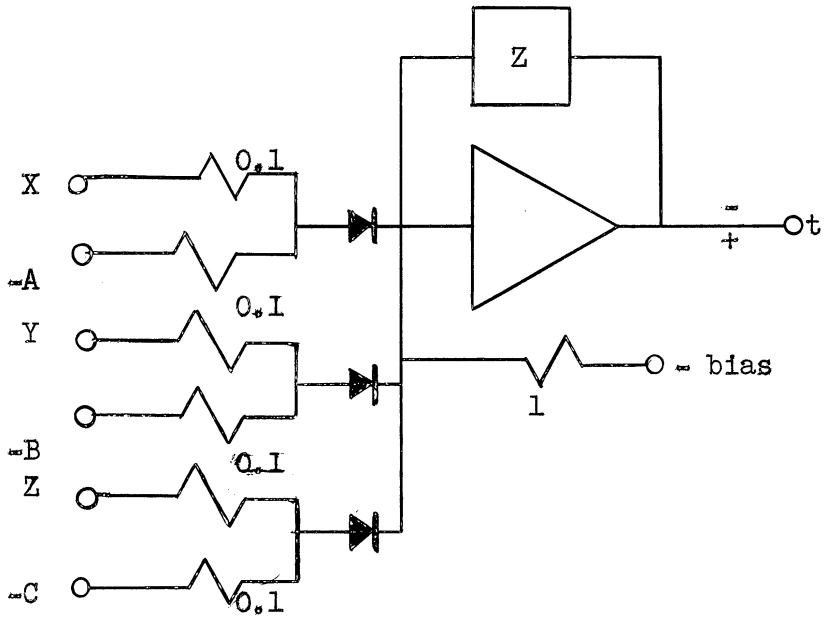


Figure 3-5 Implementation for Maxterm Form of Ordering Relation Logical Expression.

Likewise consider the conjunctive normal form expression (Minterm) given by Equation (3-3) below:

$$t_- = (X > A) \cdot (Y > B) \cdot (Z > C) \ldots . \qquad (3\text{-}3)$$

Figure 3-6 shows the implementation for the first three terms of Equation (3-3).

$t_- = (X > A) \cdot (Y > B) \cdot (Z > C)$

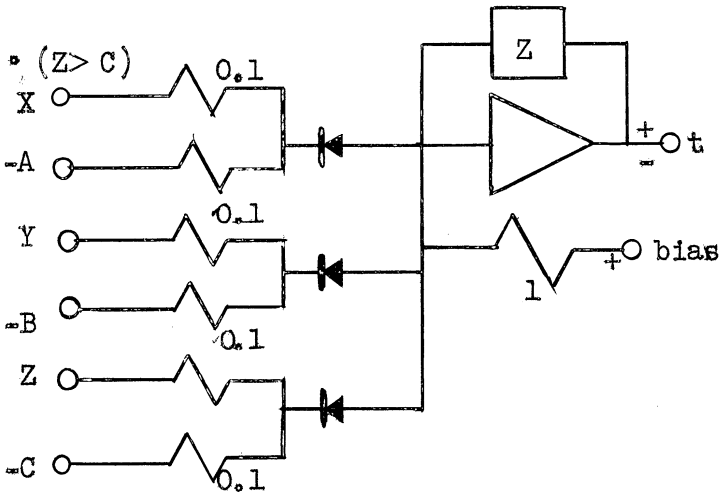


Figure 3-6 Implementation for Minterm Form of Ordering Relation Logical Expression.

Examining Figure 3-6, only when all diodes are not conducting does the output become negatively saturated, due to the small bias voltage present on the grid. Hence, $(X > A)$ and $(Y > B)$ and $(Z > C)$ are simultaneously required to be true in order to block the diodes and give a negative output. This element then generates the logical "and" function for ordering relations in minterm form.

3.3 Complementation

As was mentioned in Chapter 2, mode 3 operation of the above circuit outputs (Figures 3-5, 3-6) allows complementation to be easily performed by either one of the following two methods:

(a) Polarity reversal of inputs

(b) Diode direction reversal and reversal of output notation and bias voltage

Treating the "or" circuit first, using Equation (3-2)

$$t_- = (X > A) + (Y > B) + (Z > C) \tag{3-2}$$

Theorem 7 of Appendix 1 (DeMorgan's laws) generates the following complementary function from Equation (3-2)

$$t_+ = \bar{t}_- = \overline{(X > A) + (Y > B) + (Z > C)} \tag{3-4}$$

$$= \overline{(X > A)} \cdot \overline{(Y > B)} \cdot \overline{(Z > C)} \tag{3-5}$$

Now using Equation (A-4) from Appendix 1

$$\begin{aligned} \overline{(X > A)} &= (X < A) \\ \overline{(Y > B)} &= (Y < B) \\ \overline{(Z > C)} &= (Z < C) \end{aligned} \tag{3-6}$$

Substituting the above expressions into Equation (3-5)

$$t_+ = (X < A) \cdot (Y < B) \cdot (Z < C)$$

Hence, the positive output from the amplifier of Figure 3-5 generates the conjunctive form for the complements of the individual relations. For many cases, the disjunctive form involves the dual ordering relation of Equation (3-2), as given in Equation (3-7).

$$\begin{aligned} t_- &= (X \lessdot A) + (Y < B) + (Z < C) \\ &= (\overline{X > A}) + (\overline{Y > B}) + (\overline{Z > C}) \end{aligned} \qquad (3\text{-}7)$$

This equation can be implemented in two forms: (1) By reversing the polarity of the continuous inputs or (2) reversing the diode direction, bias voltage, and output notation. Figure 3-7(a) shows the implementation using the first method while 3-7(b) shows the second method.

$t_- = (X < A) + (Y < B) + (Z < C)$ (a)

$t_+ = (X < A) + (Y < B) + (Z < C)$ (b)

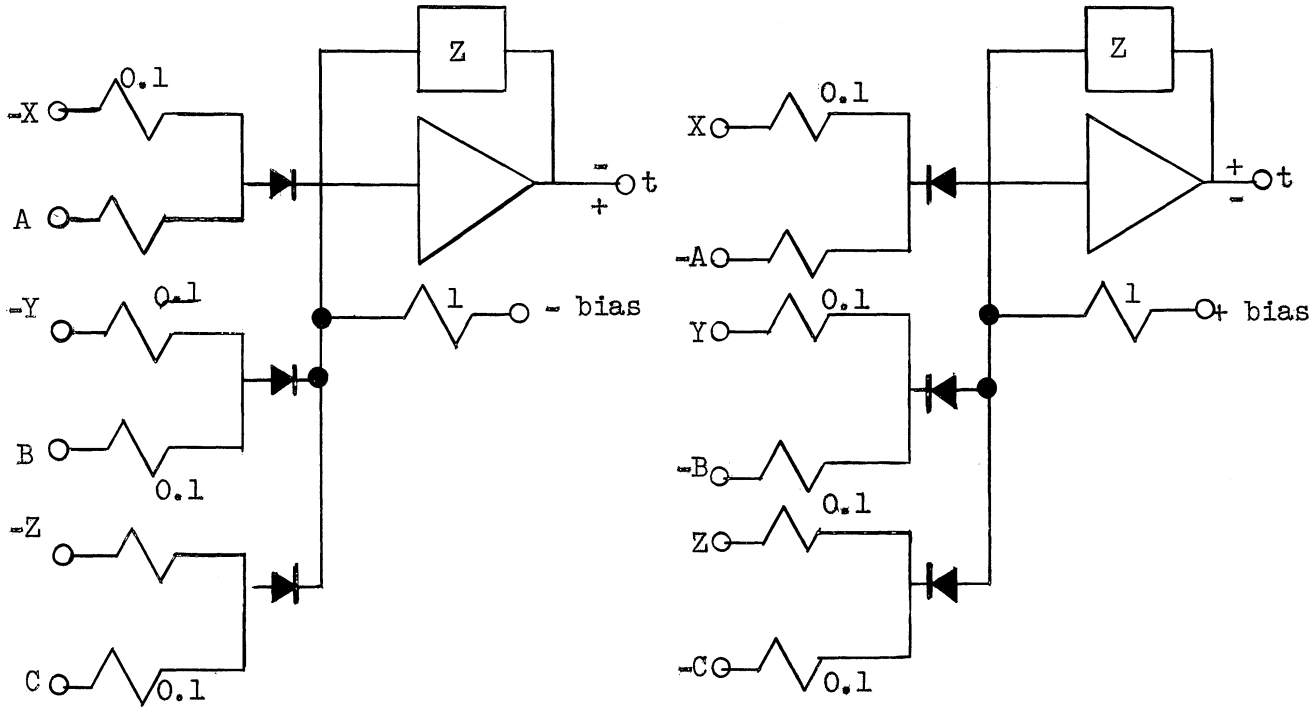
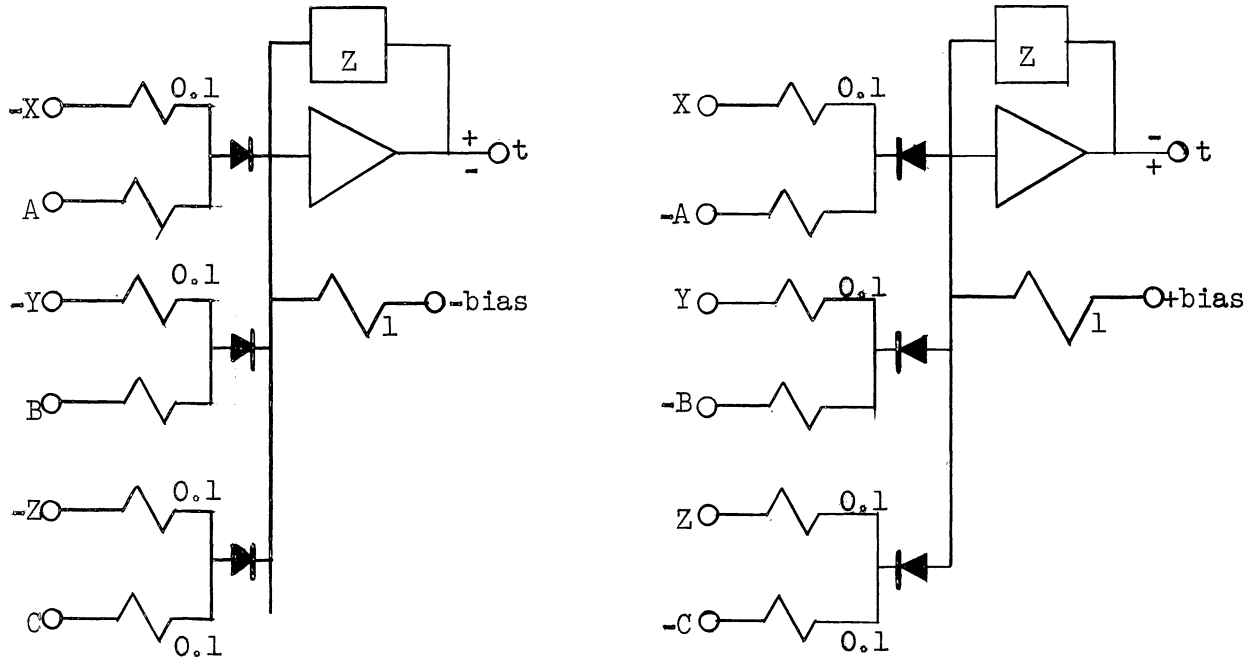


Figure 3-7 Complementation Circuits for Ordering Relations
(a) Polarity reversal method
(b) Diode direction and notation reversal method

In a similar fashion, the conjunctive normal form for the complements of the input relations may also be easily implemented as shown in Figure 3-8.

Hence, following conventional Boolean Algebra rules as outlined in Appendix 1, the dual structure of ordering relation logic is seen to be



(a)

$t_+ = (X > A) \cdot (Y > B) \cdot (Z > C)$

(b)

$t_- = (X > A) \cdot (Y > B) \cdot (Z > C)$

Figure 3-8 Implementation for Conjunctive Form of Ordering Relations.
(a) Reversed input signal polarity method
(b) Reversed diode and notation method

analogous to the dual form of conventional "and", "or" logic. As expected, the ordering relations, "<", ">" together with the "+", "·" operations form a dual logic system as noted in Table 3-1.

TABLE 3-1

DUAL FORM OF ORDERING RELATION LOGIC SYSTEM

Operation	Dual
+	•
•	+
<	>
>	<

Following general Boolean Algebra techniques, if an ordering relation expression S is given, its complement $\bar{S}$ may be found by the following set of rules[1]:

(1) Substitute + for • and • for + everywhere in the original expression, keeping the same parenthesis notation.

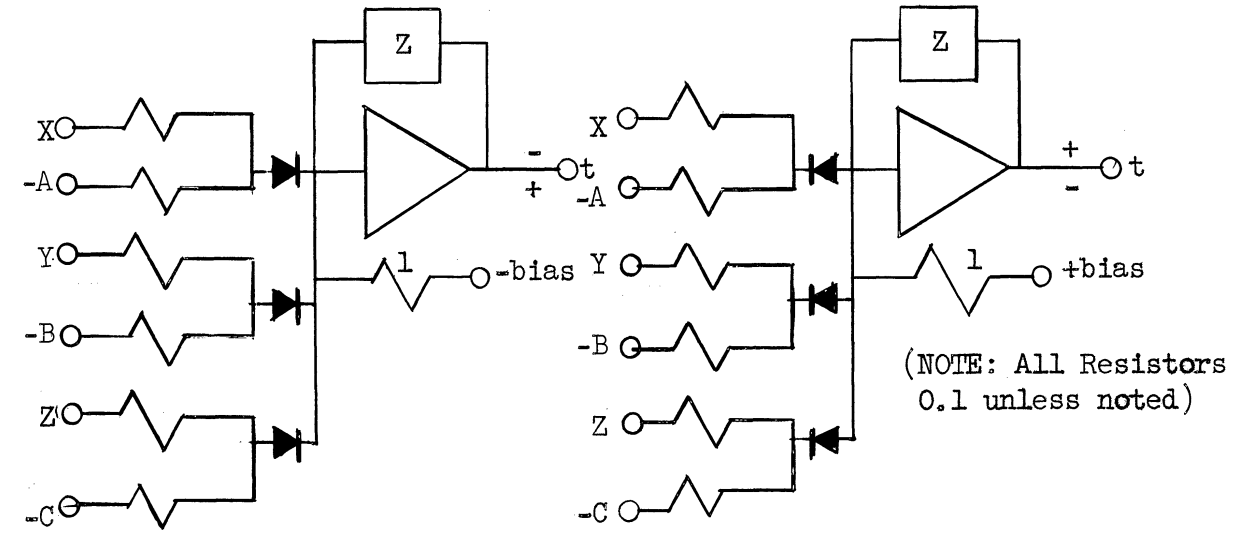
(2) Substitute > for < and < for > within each set of ordering relation parentheses.

The dual nature of the two basic circuits, "or", "and" are summarized in Figures 3-9(a) through 3-9(d).

It is interesting to note that mixtures of ordering relations may also be used within expressions such as Equation (3-8).

$$t = (X > A) + (Y < B) + (Z < C) \tag{3-8}$$

Equation (3-8) is implemented by reversing the polarity of the input signals for the second and third terms, as shown in Figure 3-10. The rules of complementation previously discussed apply to mixed systems of expressions also, as in Equation (3-8).

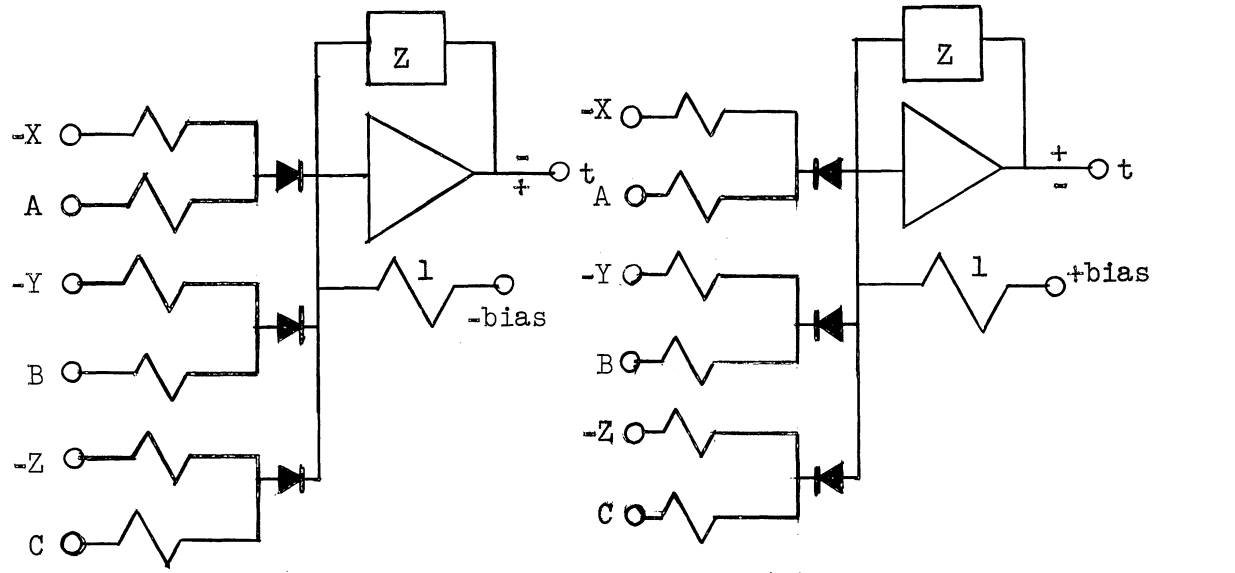


$t_- = (X > A) + (Y > B) + (Z > C)$

$t_+ = (X < A) \cdot (Y < B) \cdot (Z < C)$

$t_- = (X > A) \cdot (Y > B) \cdot (Z > C)$

$t_+ = (X < A) + (Y < B) + (Z < C)$



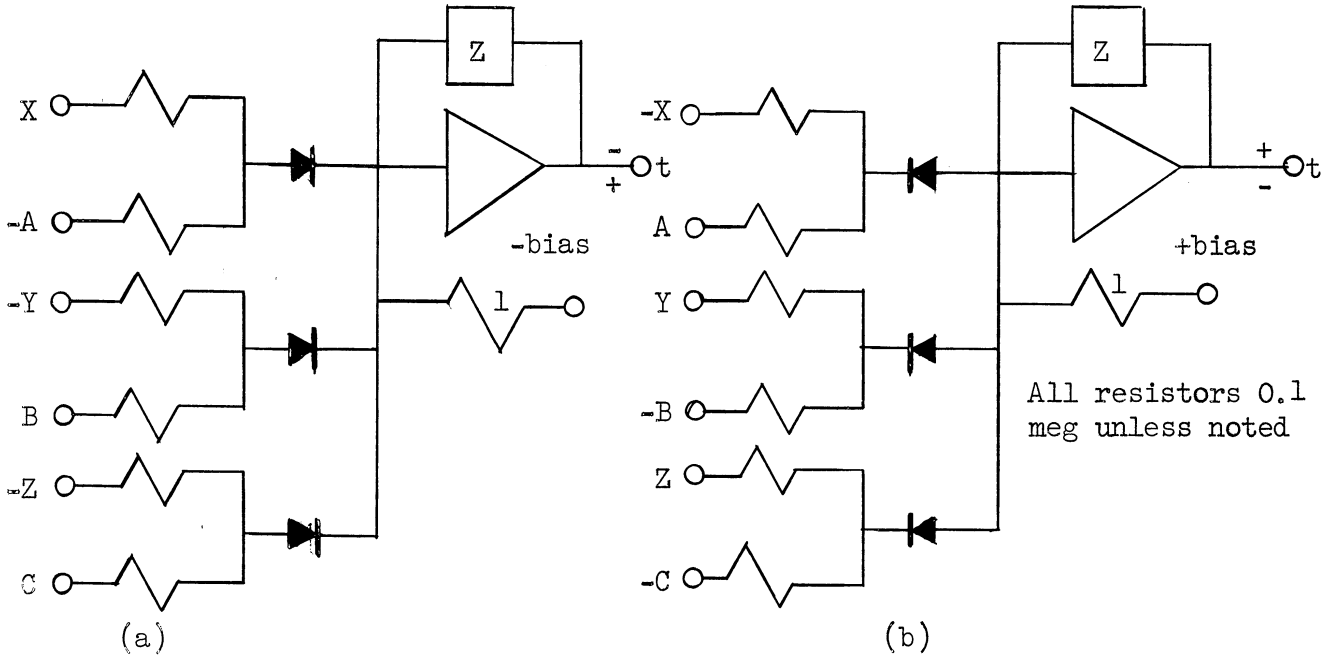
$t_- = (X < A) + (Y < B) + (Z < C)$

$t_+ = (X > A) \cdot (Y > B) \cdot (Z > C)$

$t_+ = (X > A) + (Y > B) + (Z > C)$

$t_- = (X < A) \cdot (Y < B) \cdot (Z < C)$

Figure 3-9 Summary of Duality Principle in Basic Circuits for Ordering Relation Logic.



$t = (X > A) + (Y < B) + (Z < C)$ $\qquad$ $t = (X > A) + (Y < B) + (Z < C)$

Figure 3-10 Implementation for Mixtures of Ordering Relations Within the Same Expression.

3.4 Mixed Expression Containing Continuous Variables and Boolean Functions

Ordering relation logic may also be used with conventional Boolean functions in canonical form. For expressions of the form:

$$t = [(X > A) + (Y > B) + (Z < C)] + w + r + \ldots \qquad (3\text{-}9)$$

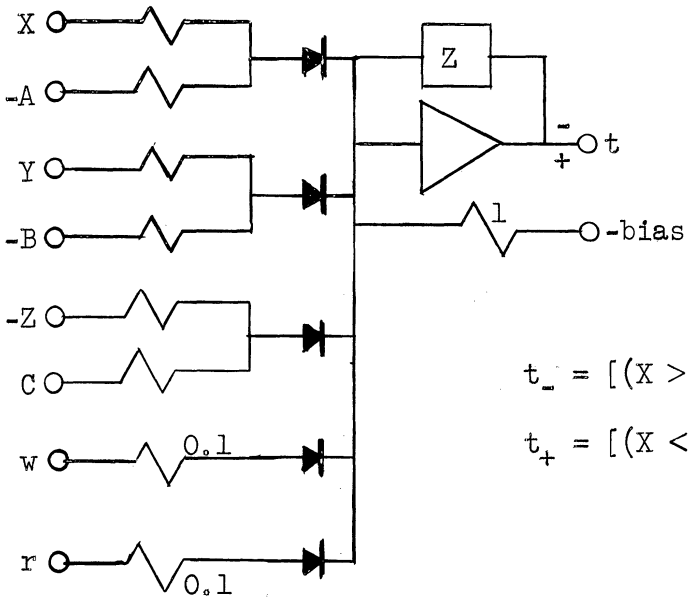
where: X, A, Y, B, Z, C = Continuous variables

w, r, ... = Boolean variables in mode 3

the circuit is shown in Figure 3-11. Similarly, conjunctive expressions may also be implemented of the form:

$$t = [(X > A) + (Y > B) + (Z < C)] * w * r \ldots \qquad (3\text{-}10)$$

The circuit for this type of expression is shown in Figure 3-12.

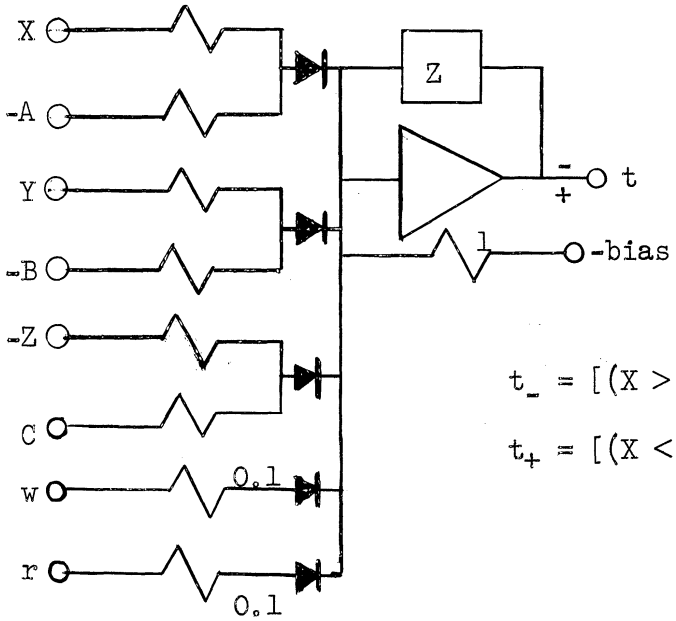


All resistors 0.5 meg unless noted

$$t_- = [(X > A) + (Y > B) + (Z < C)] + w + r$$

$$t_+ = [(X < A) \cdot (Y < B) \cdot (Z > C)] \cdot \bar{w} \cdot \bar{r}$$

Figure 3-11 Circuit for Mixed Continuous-Boolean Inputs in Disjunctive Form.



All resistors 0.5 meg unless noted

$$t_- = [(X > A) + (Y > B) + (Z < C)] \cdot w \cdot r$$

$$t_+ = [(X < A) \quad (Y < B) \quad (Z > C)] + \bar{w} + \bar{w}$$

Figure 3-12 Circuit for Mixed Continuous-Boolean Inputs in Conjunctive Form.

The one limitation of mixed expressions is that mixed "and", "or" boolean functions may not be used. Only single boolean variables connected by the • operator or the + operator, but not both, may be mixed with continuous ordering relation expressions.

It should be noted at this point that the summing junction input currents caused by the boolean functions should be larger than the maximum possible input current from the ordering relations. This can be insured by proper choice of the binary input resistor magnitudes. Note in Figures 3-11 and 3-12, the binary variable input resistors give a 5 to 1 current ratio for identical input amplitudes of the continuous and binary signals. Hence, if the boolean signal inputs are gain boosted to the maximum level of any of the continuous inputs, the resistor ratio will insure proper operation.

Thus, it is possible to implement logical expressions involving both binary and continuous inputs with a single operational amplifier. The circuit operation follows all the rules of Boolean Algebra applied to ordering relations and binary functions.

3.5 Simplification of Ordering Relation Logical Expressions

In addition to the normal operational rules of Boolean Algebra as outlined in Appendix 1, an additional principle of set theory class inclusion-exclusion may be applied to simplify ordering relation logic expressions. From consistency relations[2], the statements

$$X < Y, \quad X \cdot Y = X, \quad X + Y = Y$$

are all equivalent. In addition, set theory operations may be utilized

to reduce ordering relation expressions. For example,

if $(Y > A)$ and $(Y > B)$ where $(A < B)$

then $(Y > B) \subseteq (Y > A)$

Hence, statement of $(Y > B)$ automatically implies $(Y > A)$. If both expressions appear in an ordering expression, one may be eliminated since it is automatically implied by the validity of the other term.

Example 3-1: Given the expression:

$$t = [(Y < 6) + (Y > 4) \cdot w] \tag{3-11}$$

note that $$\overline{(Y < 6)} = (Y > 6) \subseteq (Y > 4) \tag{3-12}$$

Hence, if $(Y > 6)$ is true, then it must follow that $(Y > 4)$ is also true. The set $(Y > 6)$ may then be substituted for the set $(Y > 4)$ providing the subset $(4 < Y < 6)$ is contained in some other set term in the expression. Since $(Y < 6)$ satisfies this condition, the following substitution may be made:

$$(Y > 6) \rightarrow (Y > 4) \tag{3-13}$$

(The reader should be cautioned to carefully examine the conditions allowing this substitution. This reduction technique is valid only when the subset eliminated is contained in one of the sets of the bracketed portion of the expression). Equation (3-13) then becomes:

$$t = (Y < 6) + (Y > 6) \cdot w \tag{3-14}$$

The substitution can be made since the term $(Y < 6)$ makes the expression true regardless of the validity of the second term for $4 < Y < 6$. Hence, the second term is of importance only for $(Y > 6)$. Rewriting Equation (3-14) by using complementation:

$$t = (Y < 6) + \overline{(Y < 6)} \cdot w \tag{3-15}$$

This is of the form $a + \bar{a} \cdot w$, and from theorem T8 of Appendix 1,

$$a + \bar{a} \cdot w \triangleq a + w \tag{3-16}$$

Hence:

$$t = (Y < 6) + (Y > 6) \cdot w = (Y < 6) + w \tag{3-17}$$

Example 3-2: Given the expression

$$t = (Y > 0) + (Y > 4) \cdot w \tag{3-18}$$

note that $$(Y > 4) \subseteq (Y > 0) \tag{3-19}$$

Since $(Y > 0)$ is an independent term in the expression,

$$t = (Y > 0) + (Y > 4) \cdot w = (Y > 0) + (Y > 0) \cdot w \tag{3-20}$$

This is of the form $a + a \cdot w$, and from theorem T4a of Appendix 1,

$a + a \cdot w \triangleq a$.

Hence $$[(Y > 0) + (Y > 0) \cdot w] = (Y > 0) \tag{3-21}$$

Thus, in addition to the normal simplification techniques of Boolean Algebra, ordering relation logical expressions can be further simplified by using set theory relations, particularly class inclusion-exclusion together with the principle of logical implication.

The conventional mapping methods for binary function simplification are all applicable to ordering logic expressions or to mixed groups of binary variables and ordering relations. In addition, it is anticipated by the author that mapping methods using combined Boolean Algebra-set theory relations can be developed to handle both binary variables and continuous variables inputs to logic systems. At this stage of the investigation, however, the exact form of these mappings is not indicated.

CHAPTER 4

LOGICAL OPERATIONS WITH CONTINUOUS SIGNAL INPUTS

An interesting application of Muller's work[6] can be made by using operational amplifiers as logical summers. Using the derivations of Appendix 2, the following operations are defined:

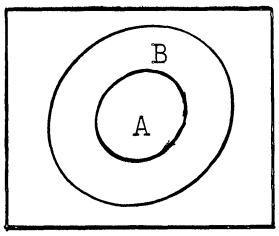
$$A \cdot B = \text{Minimum } [A, B]$$

$$A \vee B = \text{Maximum } [A, B]$$

Where: A, B, ..., X are continuous voltages such that:

$$-E_{ref} < X < +E_{ref}$$

This condition is illustrated by the Venn diagram of Figure 4-1 for two voltages A, B where A < B.



$$A \subseteq B$$

$$\therefore A \cdot B = A$$

$$A \vee B = B$$

Figure 4-1 Venn Diagram for Two Voltages in a Continuous Signal Logic System.

From an examination of conventional digital circuitry, analogous continuous input signal circuits may be found for the above logical operations. Figure 2-4 displays conventional digital circuitry for the inclusive or operation and the "and" operation. Examining Figure 2-4, the junction point, e_1, will always assume the highest voltage of any of the binary inputs. If the inputs vary between zero and some small positive voltage, the output becomes the logical "or" function.

This techniques can be used to implement a circuit for selecting the maximum continuous input signal[7]. Figure 4-2 shows such a circuit using diode inputs to an operational amplifier. Since a -100 volt bias voltage will be impressed on point e_1, any input magnitude between +100 and -100 volts is allowable. As the diode conducts, the voltage of the input signal is impressed on point e_1, changing the current in resistor R_2 from the -200 volt bias. For proper circuit operation, it must be assumed that the voltage inputs have a very low output impedance, or essentially act as a constant voltage source. Hence, point e_1 will rise to the maximum voltage available from the inputs, where the input mode may be analogous to 1, 2, or 3. This circuit then becomes a continuous "V" gate for use in the logic system described in Appendix 2.

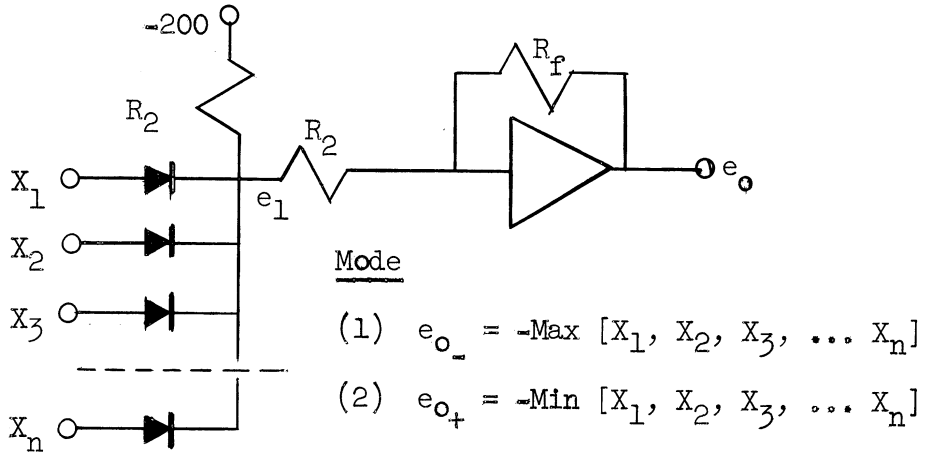


Figure 4-2 Circuit for Maximum Signal Selection.

In a similar fashion, a circuit for selecting the minimum input signal from a set continuous inputs may also be easily implemented using diode circuitry with operational amplifiers. Examining Figure 2-4(b),

the junction point e_1 will always assume the lowest of the binary voltages placed on the circuit. Again, if the inputs vary between zero and some positive voltage, point e_1 will assume the higher binary voltage only if all three inputs are simultaneously positive, thus creating the logical "and" operation. This technique can be adapted for continuous inputs as shown in Figure 4-3. Again, using a +100 volt bias at point e_1, any input magnitude between +100 and -100 volts is allowable. As the diode conducts, the voltage of the input is impressed upon point e_1. Hence, point e_1 will continue to fall until the minimum input voltage is impressed on e_1. As in the maximizer circuit described above, the same assumptions on voltage sources must be made. This circuit then becomes a continuous "•" gate for use with the "$\vee$" gate previously discussed.

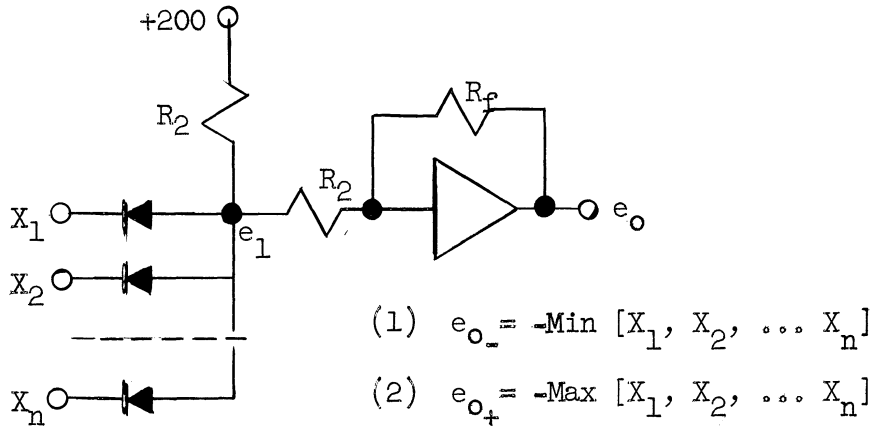


Figure 4-3 Circuit for Minimum Signal Selection.

It is interesting to note the dual operation of the circuits depending upon the mode of input signals being used. Figures 4-2 and 4-3

show that either configuration can be used as a maximizing circuit or as a minimizing circuit, by the choice of operating modes 1 or 2. In addition, mode 3 may also be used together with its dual of operation to form dual circuit responses as above. Thus, any one of the three operating modes allows use of the duality principle in implementation.

Operation of the input signals analogous to mode 1 appears to offer the greatest flexibility in logical implementation since the negative values of input signals allow a dual logical function to be implemented using opposite amplifier output polarity. This condition was also found in Chapter 2 for binary operation. Thus the ability to handle both positive and negative input signals as circuit inputs considerably increases the number of logical functions possible on a single amplifier.

The operation of complementation is quite simply performed using this type of logic. From Appendix 2, Equation (A-47), the complement is defined as:

$$\bar{A} = (1 - A)$$

Since the reference used for the circuits described in this chapter is $+E_{ref}$, the complement of any continuous variable is found from

$$\bar{X} = (E_{ref} - X)$$

This can be implemented by simply summing both $-E_{ref}$ and $+X$ in a conventional summer as shown in Figure 4-4. Note again that mode 1 are assumed for this complementation. Simple polarity changes modify this complementation unit for use in mode 2 operation.

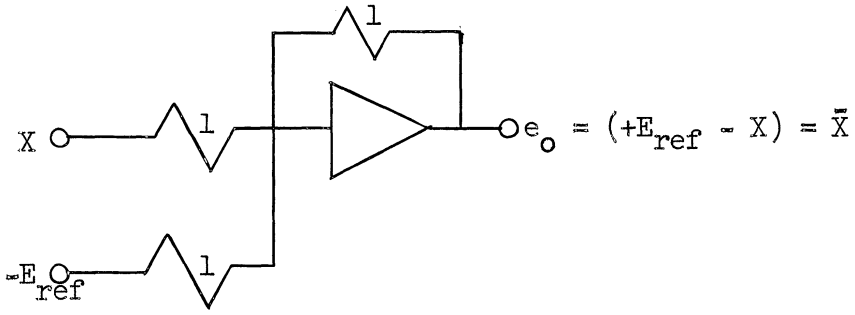


Figure 4-4 Basic Circuit for Complementation.

CHAPTER 5

PRACTICAL LIMITATIONS OF OPERATIONAL AMPLIFIER LOGICAL CIRCUITS

5.1 Conventional Switching

Two definite problems exist in attempting to implement logical expressions using diode circuitry with operational amplifiers. First, solid state diode operation with low voltage inputs create a type of threshold effect which places a limit upon the accuracy of low level voltage comparison. Figure 5-1 shows typical diode current-voltage forward conducting characteristics at room temperature.[8] By placing the diodes in a constant temperature environment of about 120°C, this threshold drop can be reduced to about 0.1

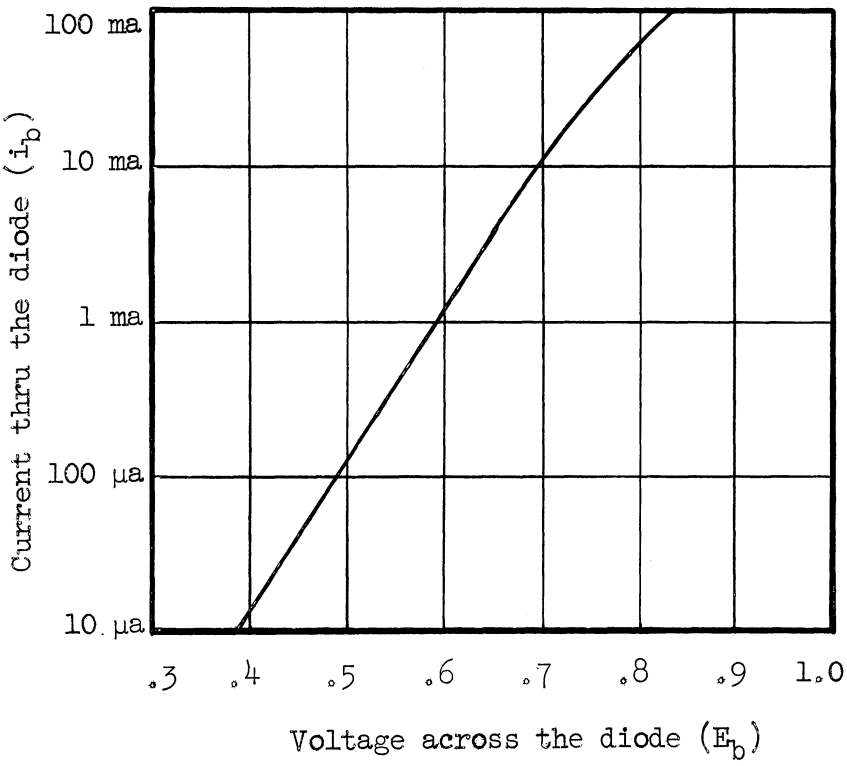


Figure 5-1 Typical Current-Voltage Characteristic of a Silicon Junction Diode at Room Temperature.

or 0.2 volts. However, with higher operating temperatures, there is a significant deterioration of the diode back resistance which may affect circuit operation. Another solution to this problem lies in new semiconductor techniques which indicate that diodes applicable to this type of switching will soon be available with threshold levels of 1 ma. at less than 0.1 volt.* It is felt that this latter figure is sufficiently low for switching applications, taking into account the inherent error in the input signals to the operational amplifier logic circuits.

Second, it will be noted from Figures 3-1 through 3-12 that a small bias signal input is required to insure correct amplifier output when all diodes are blocked. The magnitude of bias voltage needed is less than 0.1 volt, well within the accuracy limitation imposed by the switching diodes. However, depending upon the magnitude of the D. C. amplifier offset voltage referred to the input, the switching speed of the operational amplifier may be slowed by such a low level input, and hence, the amplifier may experience uneven switching rates for positive and negative inputs.

For the frequencies of continuous signals operated upon by most real-time analog computer elements, the switching speeds are entirely adequate. This problem places a limitation, however, on the type of inputs allowed. Because of threshold effects, slowly varying comparison signals cause a "soft switch" to occur, and hence, there are both lower and upper limits on the frequencies of inputs not involving discontinuous changes.

---

* Personal communication with Mr. George MacRoberts, Semiconductor Division, Texas Instruments Co., Cleveland, Ohio.

The "soft switch" threshold effect can be reduced somewhat by minimizing the signal dwell time in the threshold region as shown in Figures 5-2(a) and (b). Since the comparison circuit need be linearly

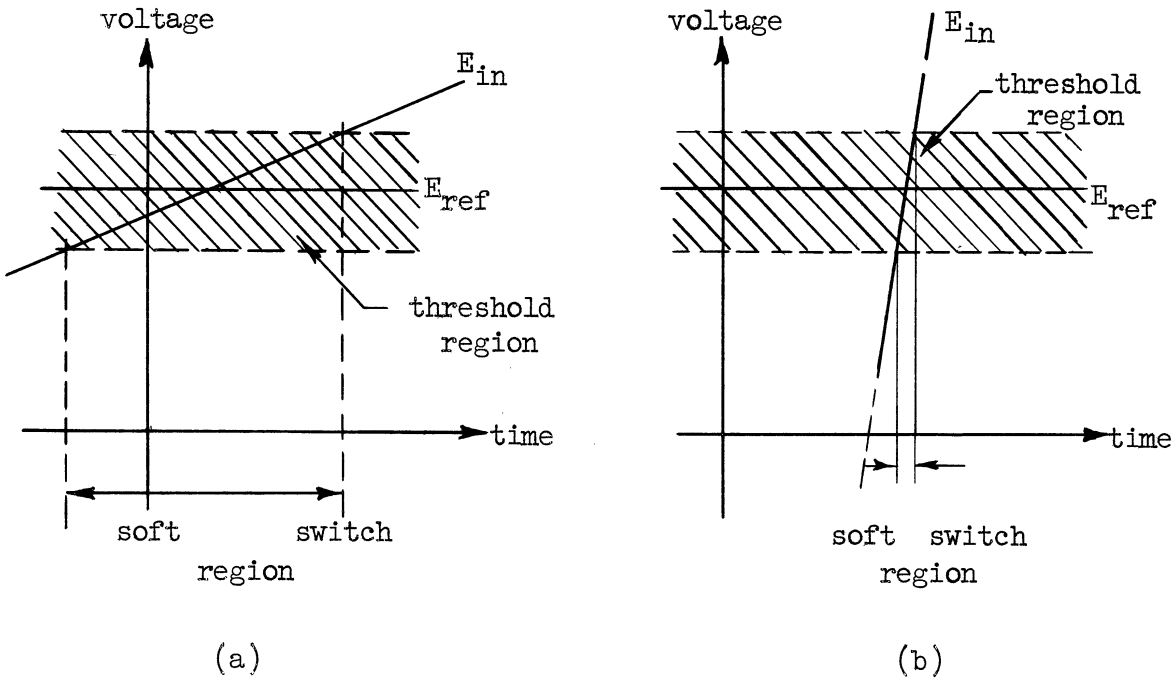


Figure 5-2 Effect of Scaling of Input Variable Magnitude Upon Threshold Effect.
(a) Slowly varying low level signal
(b) Same signal with increased scaling

operating only in the region of the threshold, the input signal may be scaled up in magnitude and the comparison made at a high level. This serves to minimize the time during which the input signal lies within the threshold band. Since binary outputs are desired, scaling problems due to large magnitude input signals are not involved. Note, however that this scaling technique may be used only when the scaled inputs do not exceed the limits of the analog reference voltages, as per conventional analog computer scaling. If both inputs to an ordering logic

input are variables, it may be necessary to form the sum of the inputs in a previous summing amplifier before applying to a logic circuit. Only when both scaled variables can be kept within linear operation limits does the scaling method apply.

5.2 Continuous Signal Logic Circuits

In considering the logical operations of Chapter 4 and Appendix 2, one important point must not be overlooked. The input voltages to maximum or minimum signal selection circuits should not be altered by loading effects. Thus, a constant voltage source is demanded. If the voltage source output impedance is high, significant loading errors will appear in the output. Since it is assumed that most input voltages used will be computer generated, the low output impedance of operational amplifiers will essentially eliminate loading effects. It should also be noted that a small input bias current to the amplifier summing junction can be used to correct for the average diode voltage drop.

When all binary inputs are being used, the bias signal may be increased in magnitude to switch sharply the amplifier when the input logic fails. Since the input signals are discontinuous binary voltages, the threshold effect does not enter into the operation.

CHAPTER 6

AN APPLICATION OF ORDERING RELATION LOGIC TO AN OPTIMALIZING AUTOMATIC CONTROL SYSTEM

6.1 Problem Description

Given a system to be controlled with an output variable as a function of a primary control variable as shown in Figure 6-1.[11] For optimum system

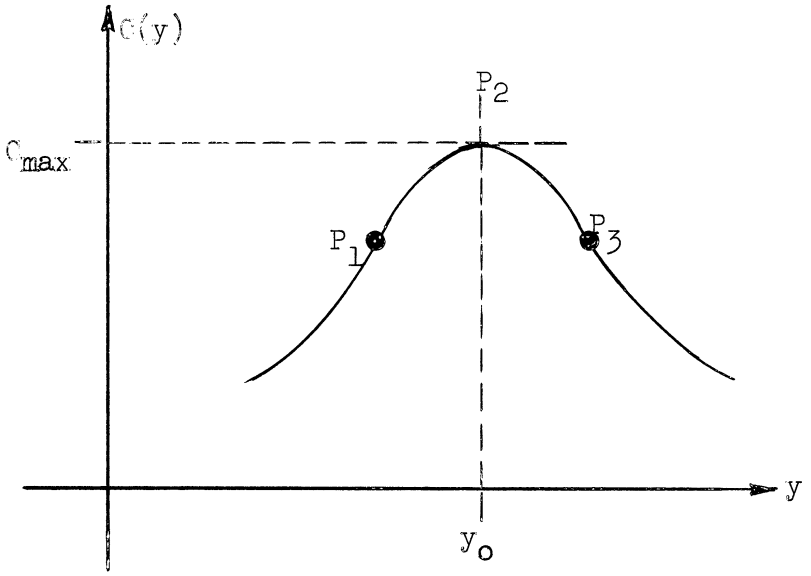


Figure 6-1 System Output Variable With Optimum Peak

operation, the control system is to maximize the value of C(y) at all times. Since the y_o value will shift with time and operating conditions, only the C(y) value and its derivative are available for control purposes. Hence, the following logic system may be written to describe the action of the peak seeking control system. The controller will be assumed to be a bang-bang type with the positive output increasing the value of y and the negative output decreasing y.

$(\dot{C} > 0)$ and $(\dot{Y} > 0)$: Drive +

$(\dot{C} < 0)$ and $(\dot{Y} < 0)$: Drive +

$(\dot{C} > 0)$ and $(\dot{Y} < 0)$: Drive -

$(\dot{C} < 0)$ and $(\dot{Y} > 0)$: Drive -

The logical expression for the control system output can then be written as:

$$T_{+} = (\dot{C} > 0) \quad (\dot{Y} > 0) + (\dot{C} < 0) \quad (\dot{Y} < 0) \qquad (6\text{-}1)$$

Thus, any initial velocity displacement will return the system to the peak of the C(y) relation.

However, there exists a hazard in the switching for Equation (6-1). Since there are two control signals of two values each, there exist four possible signal combinations for the logic circuit. The proper operation of the control system depends upon how the changes of logic state are made in going from one state to another. For example, assume that $(y < y_o)$ initially. If $(\dot{Y} > 0)$ and $(\dot{C} > 0)$, a positive drive signal moves the system toward the peak. As the peak is passed, $\dot{C}$ becomes negative, giving $(\dot{Y} > 0) \cdot (\dot{C} < 0)$. This results in a negative drive signal from the control system. The physical system will lag the control signal by a certain amount, resulting in the possibility of having $\dot{Y} < 0$ while $\dot{C} < 0$. This condition of dynamic lag is not shown by the functional relationship, Figure 6-1, since it is only a static relationship curve.

Hence, at the time of switching from + to - control signals, there will be a portion of time in which $(\dot{Y} < 0) \quad (\dot{C} < 0)$ will occur. This condition will cause a + control signal, driving the system away from the peak. The result is an oscillation about the switching point P_3.

Note that the same condition is true when driving in the opposite direction at point P_1. Keeping this hazard point in mind, the logic system can be easily implemented.

6.2 Basic Logical Circuits

Since the basic control signals are ordering relations, the logic is most easily implemented using direct ordering relation logic on an operational amplifier. The circuit for Equation (6-1) is shown in Figure 6-2.

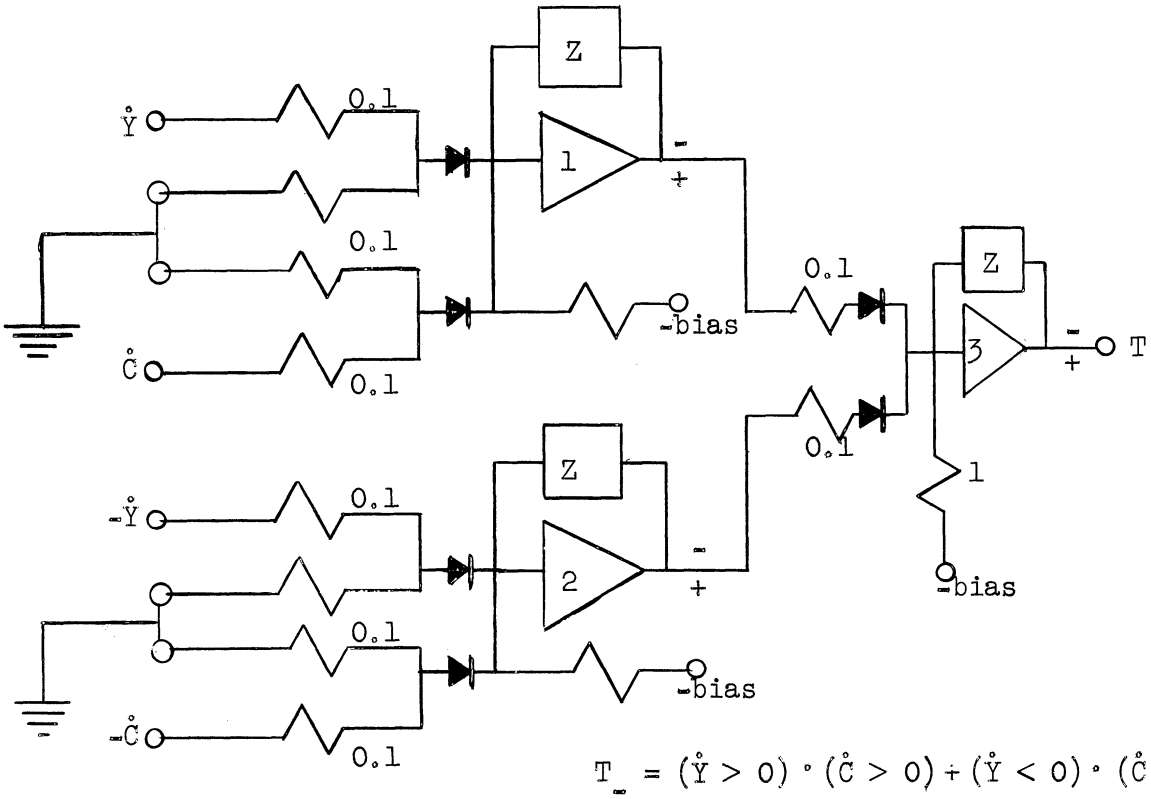


Figure 6-2 Implementation of Logical Expression of 6-1.

The dual logic circuit is shown in Figure 6-3. This implementation will be shown to have advantages for eliminating the hazard switching condition.

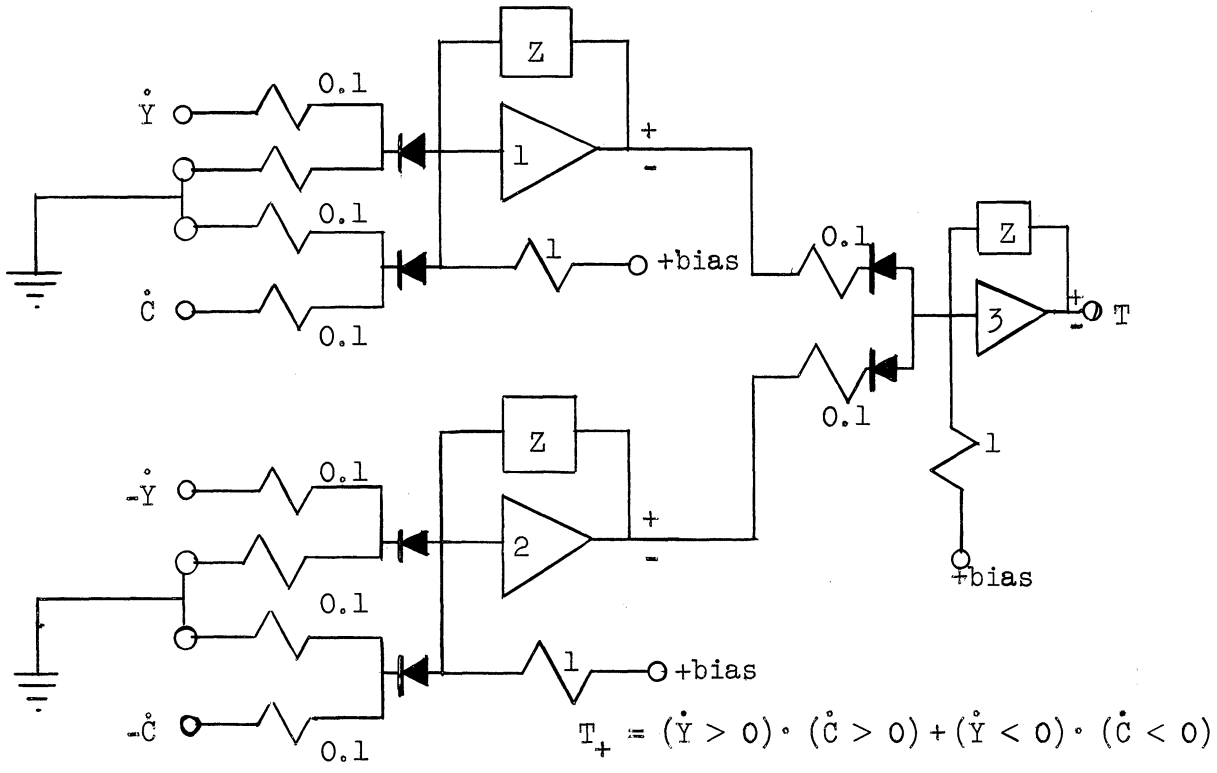


Figure 6-3 Dual Circuit for Implementation of Equation (6-1).

A time plot of the three amplifier outputs of Figure 6-3 versus typical $\dot{Y}$, $\dot{C}$ inputs is given in Figure 6-4 to demonstrate the problem of asynchronous switching. Note that amplifier 3 gives the correct output signals with the exception of the short pulses occurring at times t_2 to t_3 and t_5 to t_6. This is caused by the delay in the $\dot{C}$ switching signal. What is desired then, is a circuit logic which delays the $\dot{Y}$ switch point until $\dot{C}$ has switched. The operation can be implemented rather simply in ordering logic circuitry. Using the same logic circuit as shown in Figure 6-3, a modification is made to the $\dot{Y}$ comparison input of amplifier 2. Instead of the $\dot{Y}$ comparison reference being zero, a voltage K(T) is fed back from amplifier 3 and used as a reference. The value of K ($0 < K < 1$) is adjusted to control the reference voltage. Figure 6-5 shows the modified circuit. Examining Figure 6-4, it is noted that the

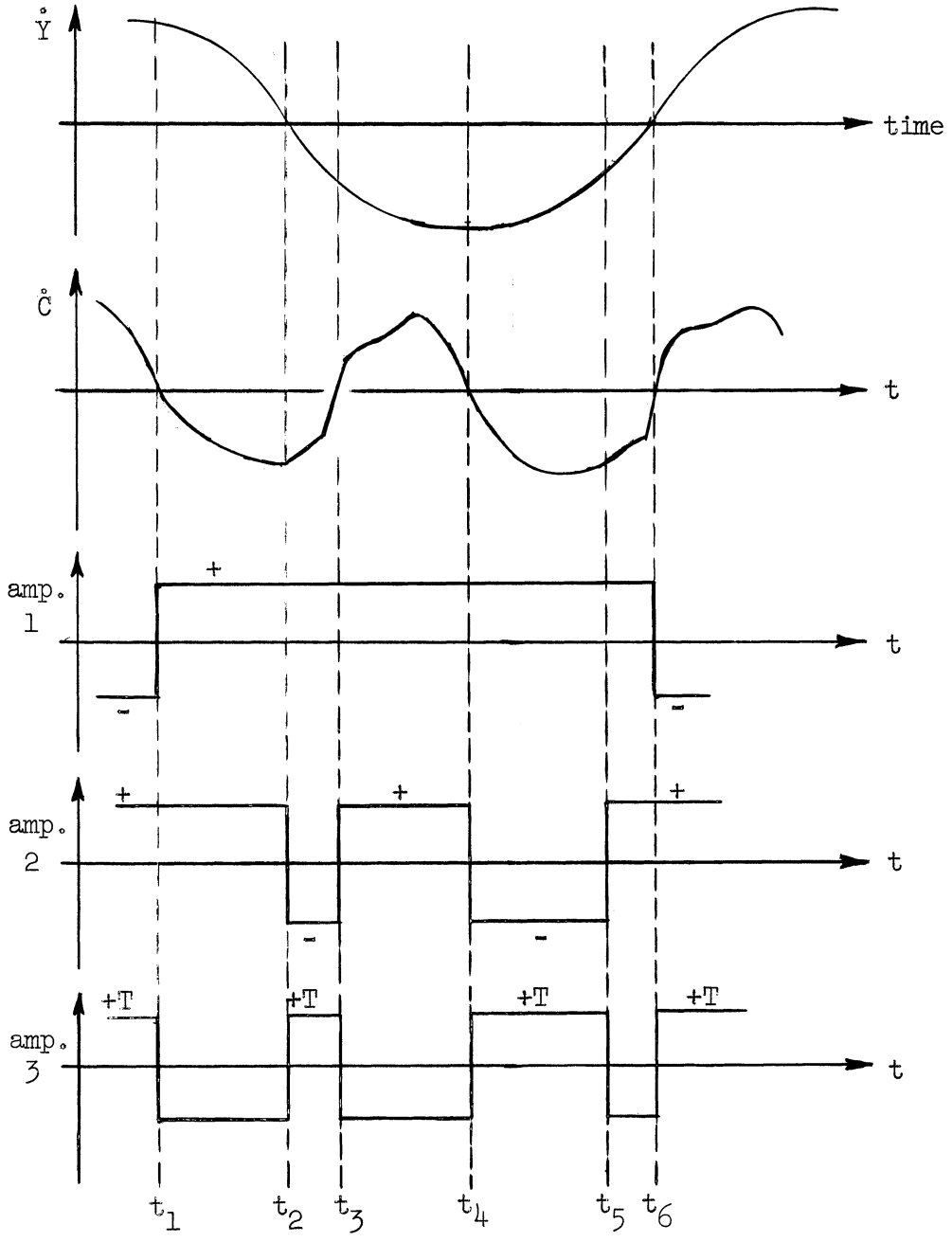


Figure 6-4 Time Plot of Typical Logic System Signals.

output of amplifier 3, +T or -T, will always be of opposite polarity to that of the $\dot{Y}$ input, JUST BEFORE THE HAZARD SWITCHING POINT OCCURS. Hence, by feeding back voltage from amplifier 3 to amplifier 2, a variable bias

voltage for the $\dot{Y}$ switching reference is created whose polarity is always opposite to $\dot{Y}$. Hence, the $\dot{Y}$ switching point can be properly biased in magnitude to match the time lag in the $\dot{C}$ switch.

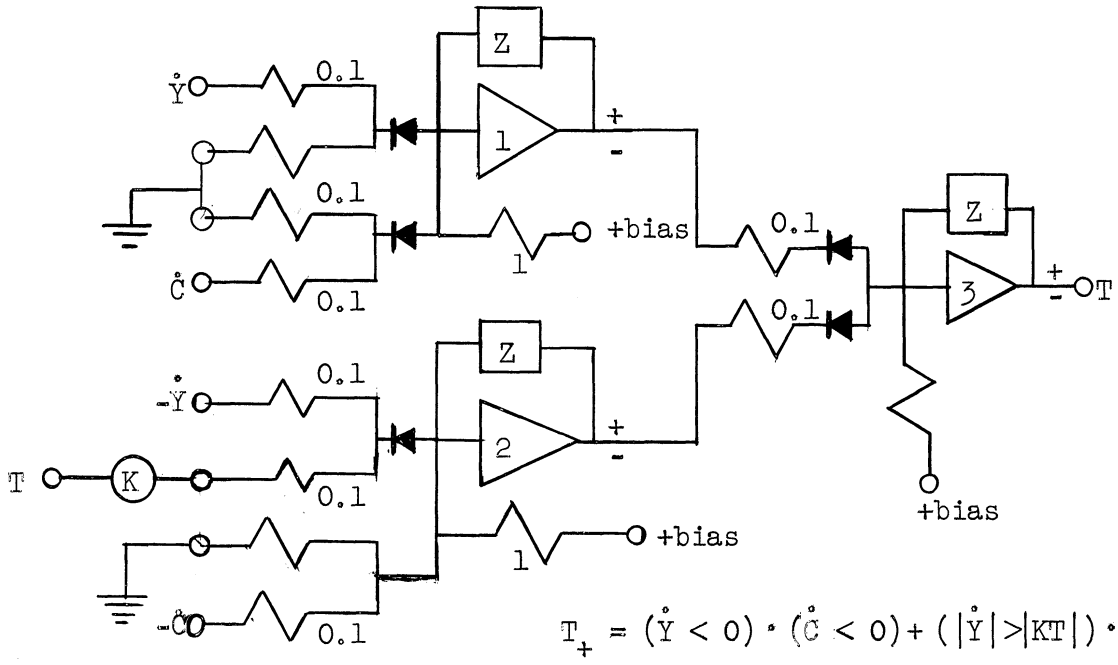


Figure 6-5 Modified Logic Circuitry with Delay Factor to Compensate for C Switching Delay.

Figure 6-6 displays the switching curves for the modified delay time system. Notice that the delay in the $\dot{Y}$ switch takes the form of a hysteresis effect. That is, the lag is always opposite to the direction of switching, either $\dot{Y} > 0$ or $\dot{Y} < 0$. Hence, using the normal logical expression

$$T_+ = (\dot{Y} > 0) \cdot (\dot{C} > 0) + (\dot{Y} < 0) \cdot (\dot{C} < 0) \qquad (6\text{-}2)$$

T_+ can be easily implemented if synchronized switching occurs. If the logic must be asynchronous, delays can be implemented by changing the

reference bias for one of the variables to be sensed. This creates an ordering relation logical expression of the form:

$$(\dot{Y} < -K_1T) \cdot (\dot{C} < 0) + (\dot{Y} > +K_2T) \cdot (\dot{C} > 0) \qquad (6\text{-}3)$$

where $K_1 = K_2$ if the switching curves are symmetrical.

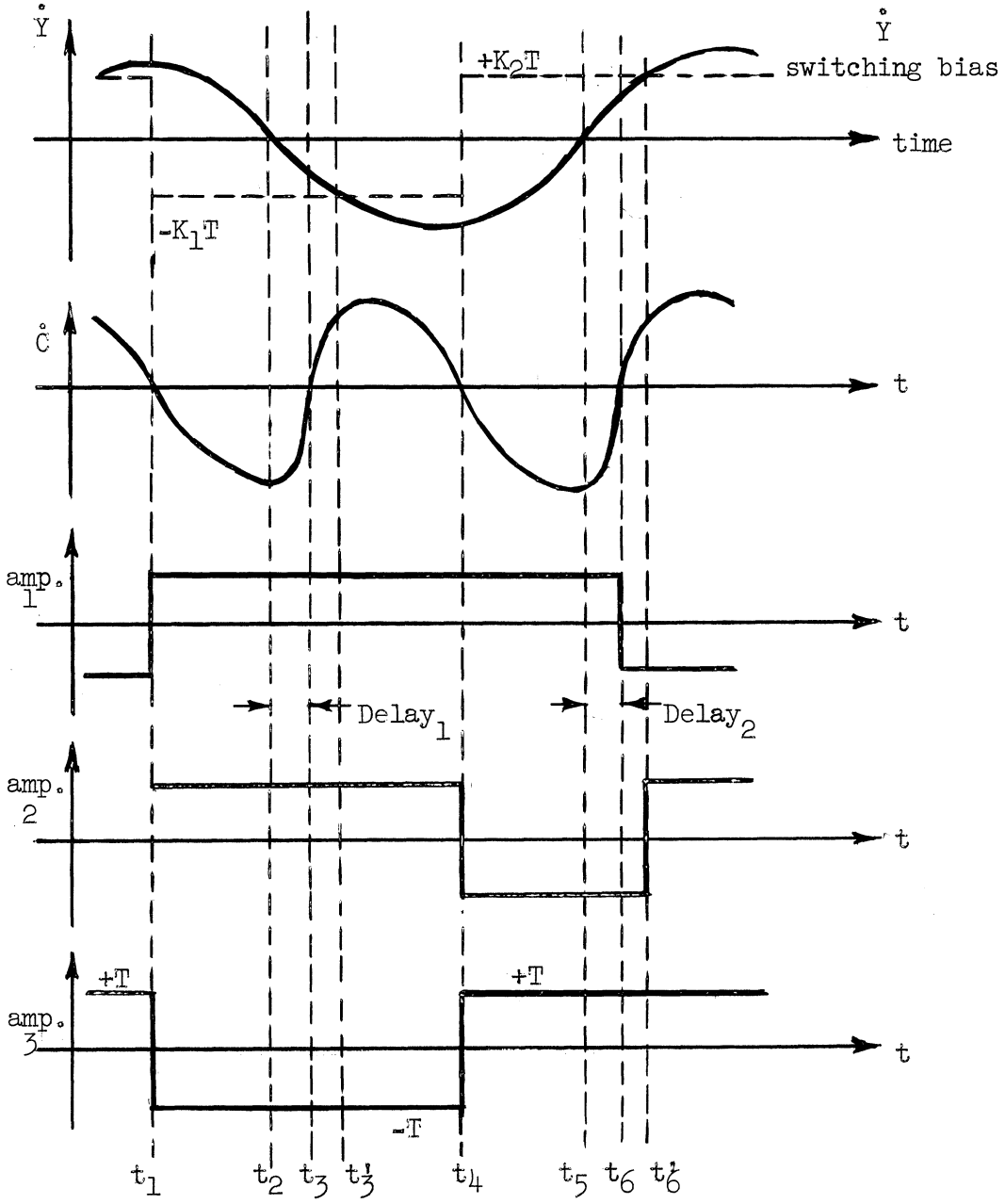


Figure 6-6 Time Plot of Modified Switching System Response.

All of the logic necessary to implement such a nonlinear controlling device can be achieved on conventional operational amplifiers with diode input circuitry. It is interesting to note that the same logic as implemented above may also be used for driving a system to a minimum value of C(y). The only changes required are to reverse the polarity notation for a positive y drive signal and readjustment for asynchronous switching problems.

CHAPTER 7

AN APPLICATION OF ORDERING RELATION LOGIC TO A DUTY CYCLE OPTIMIZER

Given a set of N machines with different power requirements, all connected to a common power source bus as shown in Figure 7-1.

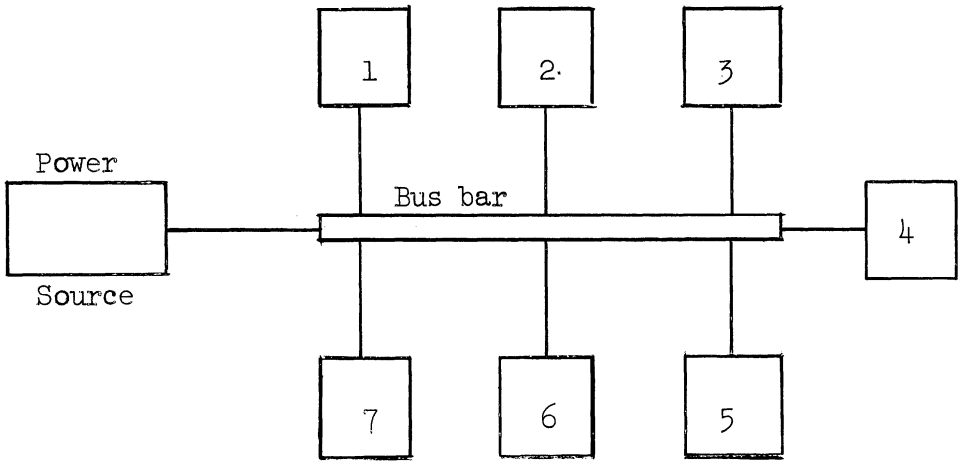


Figure 7-1 Duty Cycle System with Common Power Bus.

The power source capacity is insufficient to carry all machine loadings in parallel, but it is desired to match the loading as closely as possible to the maximum rated capacity of the source. The problem is complicated by each machine having a different power requirement, on-line time, and operation cycle. Thus the total load power required changes abruptly and somewhat randomly as different machines are brought onto and dropped off of the common bus line.

A logic system to allow optimum loading matching, under random conditions, to a given source capacity can be implemented using combinations of ordering relations and binary inputs to an operational amplifier as follows.

Each machine has four stable states of operation as listed below:

1. Off-line, not ready
2. Off-line, ready
3. Coming on-line
4. On-line

In order to allow a machine to come onto the bus line, the following three statements must be simultaneously true:

(a) Machine off-line, ready

(b) Power required by the machine < power remaining in the source

(c) No other machine has come on line within the previous 2 cycles.

Note that decisions (a) and (c) are binary in form while decision (b) involves a comparison.

It is assumed that a continuous voltage is available for the value of the remaining power in the source (before capacity is exceeded), denoted by P_r. Also, each machine presently has "off line, ready" binary signal output circuits. Assuming a transient blocking signal is available for 2 cycles after any machine comes on line, denoted as B, the logical expression for a single machine can be written as

$$w_i = r_i \cdot (P_i < P_r) \cdot (\bar{B}) \cdot (\bar{S}_i) \qquad (7\text{-}1)$$

where: r_i = ith machine ready (mode 3 binary)

S_i = ith machine on line (mode 3 binary)

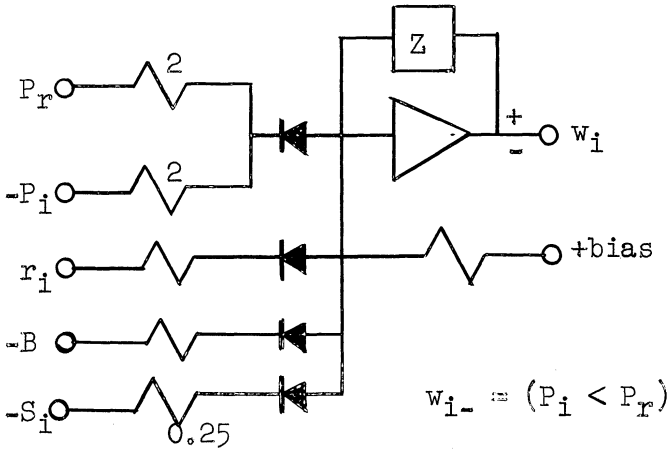
B = transient blocking signal (mode 3 binary)

P_i = ith machine power requirements (mode 1 continuous)

P_r = available source power remaining (mode 1 continuous)

w_i = ith machine on line (mode 3 binary)

The logical implementation of Equation (7-1) is shown in Figure 7-2.



NOTE: All resistors 1 meg. unless noted

$$w_{i-} = (P_i < P_r) \cdot (r_i) \cdot (\bar{B}) \cdot (\bar{S}_i)$$

Figure 7-2 Logical Implementation of Equation (7-1).

Note that by feeding back an input signal, S_i, to the amplifier through a 0.25 megohm resistor, once the machine is turned on S_i controls the amplifier output regardless of the other inputs signals. Hence, the logical circuit acts as a special type of flip-flop circuit, being reset only when the machine goes off line. Because of the r_i input, the circuit is capable of being "set" only when the machine is off line and ready to come on line. This latter condition will depend upon the recovery time necessary after each machine operation and the rate at which material becomes available to the machine.

CHAPTER 8

MISCELLANEOUS APPLICATIONS

It is interesting to note that logical operations on operational amplifiers may also be extended to flip-flop action. Specifically, both minterm and maxterm form expressions may be used to "set" and equivalent flip-flop. Figure 8-1 shows a flip-flop circuit with minterm type input expression. Again, as in Appendix 2 and Chapter 3, note that both ordering relations and binary inputs can be combined as inputs to the same amplifier. Since a two amplifier circuit is used with feedback, the output of amplifier 1 will be driven hard to its positive or negative saturation value, depending upon the zener diode limiting. Amplifier 2 serves as an inverter-reset circuit. Examining Figure 8-1, the logical expression noted must be met for all the diodes to be blocked. When

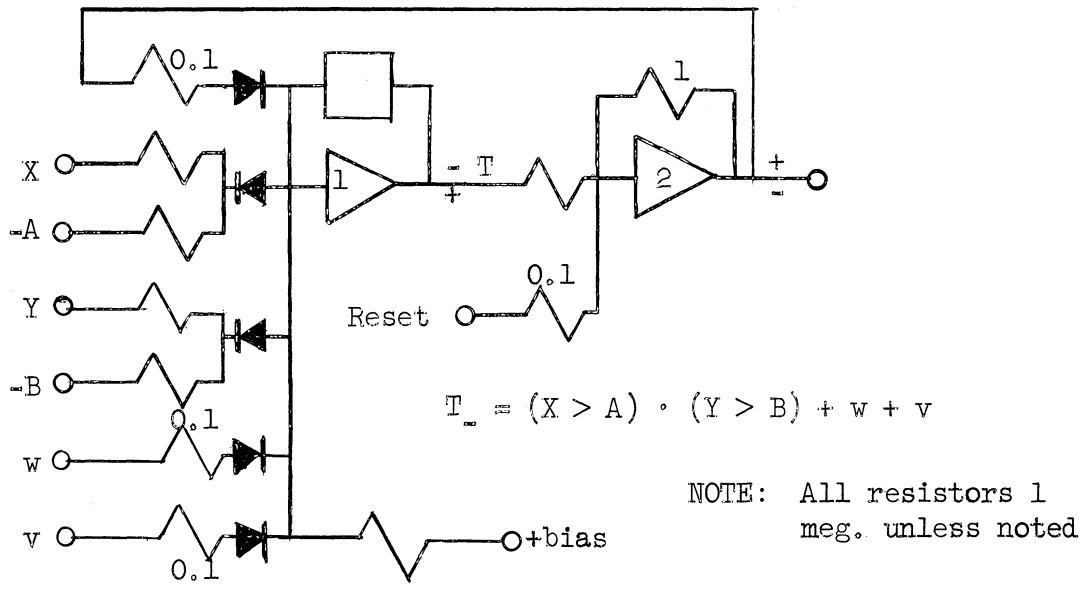


Figure 8-1 Implementation of a Flip-Flop Circuit Using Ordering Relationship and Binary Variables.

amplifier 1 has a positive output, the system will be denoted as in the "set" mode. Whenever the logical expression is met, the output is driven negative. The feedback from amplifier 2 reinforces the input, and amplifier 1 remains saturated in the negative polarity state. If the input "set" conditions are removed, amplifier 1 will return to the positive state whenever a positive reset pulse is applied to amplifier 2. If the input conditions are still in effect when the reset is applied, the circuit returns to the "set" state immediately after removal of the reset pulse. Note that all binary inputs operate in mode 3 while the continuous inputs operate analogously to mode 1. The total expression shown in Figure 8-1 should include a term for the reset value as follows:

$$T_{\_} = [(X > A) \cdot (Y > B) + w + v] \cdot \bar{\bar{R}} \qquad (8\text{-}1)$$

Thus, the expression is dependent upon the reset signal remaining off during the set phase of operation.

CHAPTER 9

EMPIRICAL RESULTS AND CONCLUSIONS

9.1 Threshold Switching Effects

As discussed in Chapter 5, the dwell time in the comparison threshold region determines the speed of switching. Figure 9-3 through 9-6 display this effect for three different dwell times. Note from Figure 9-3 the "soft" switch occurring especially as T goes from T- to T+, requiring almost one full second. Also note that actual switching occurs at the value $(X - A) \cong 0.5$ volts which would be expected for conventional diode drops of approximately 0.5 volts.

Figures 9-4 and 9-5 show improved switching response for input rates of change approximately 7 times that for Figure 9-3. Again note the 0.5 volt diode drop. Finally, Figure 9-6 shows the much improved switching speed when the input signal is scaled up even higher, showing full switching in less than 0.03 seconds.

9.2 Optimalizing Control System Logic with Adjustable Delay

In order to test the action of the control logic circuitry shown in Figure 6-5, a typical physical system with dynamic delays of the form of Figure 9-1 was implemented. The static optimization curve was approximated by the expression:

$$C = K_1 - (Y - K_2)^2 \qquad (9\text{-}1)$$

from which

$$\dot{C} = -2Y + 2K_2 \qquad (9\text{-}2)$$

In order to simulate the dynamic delays between $\dot{Y}$ and $\dot{C}$, the general system of Figure 9-2 was implemented.

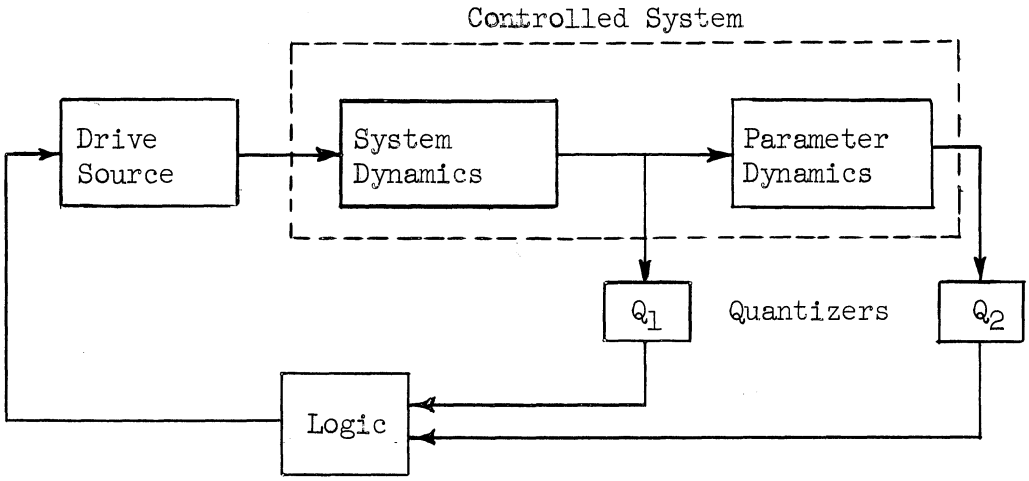


Figure 9-1 Optimalizing Control System.

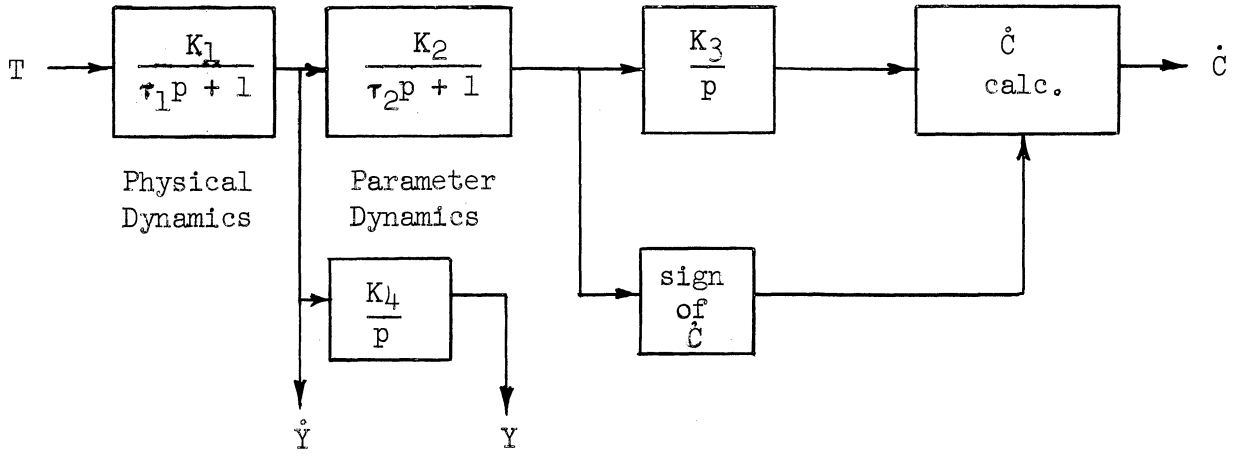


Figure 9-2 Simulated Optimalizing Control System.

An adjustable amount of delay may be placed into the control logic network by feedback methods. Figure 9-7 shows the actions of the optimalizing control system with a hazard switching effect shown in the bottom

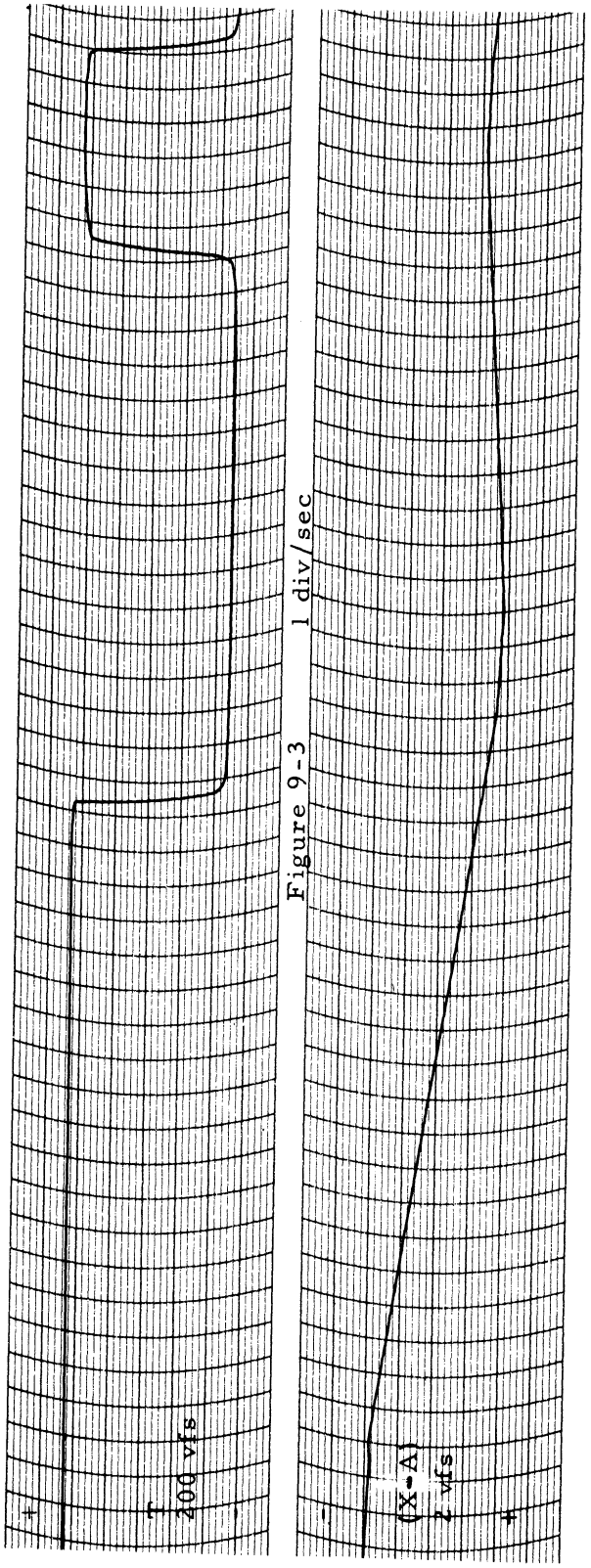


Figure 9-3 1 div/sec

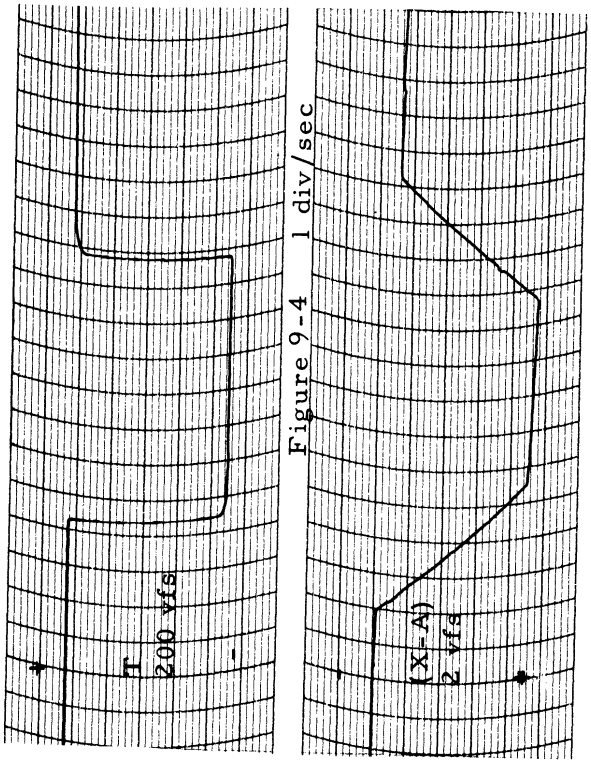


Figure 9-4 1 div/sec

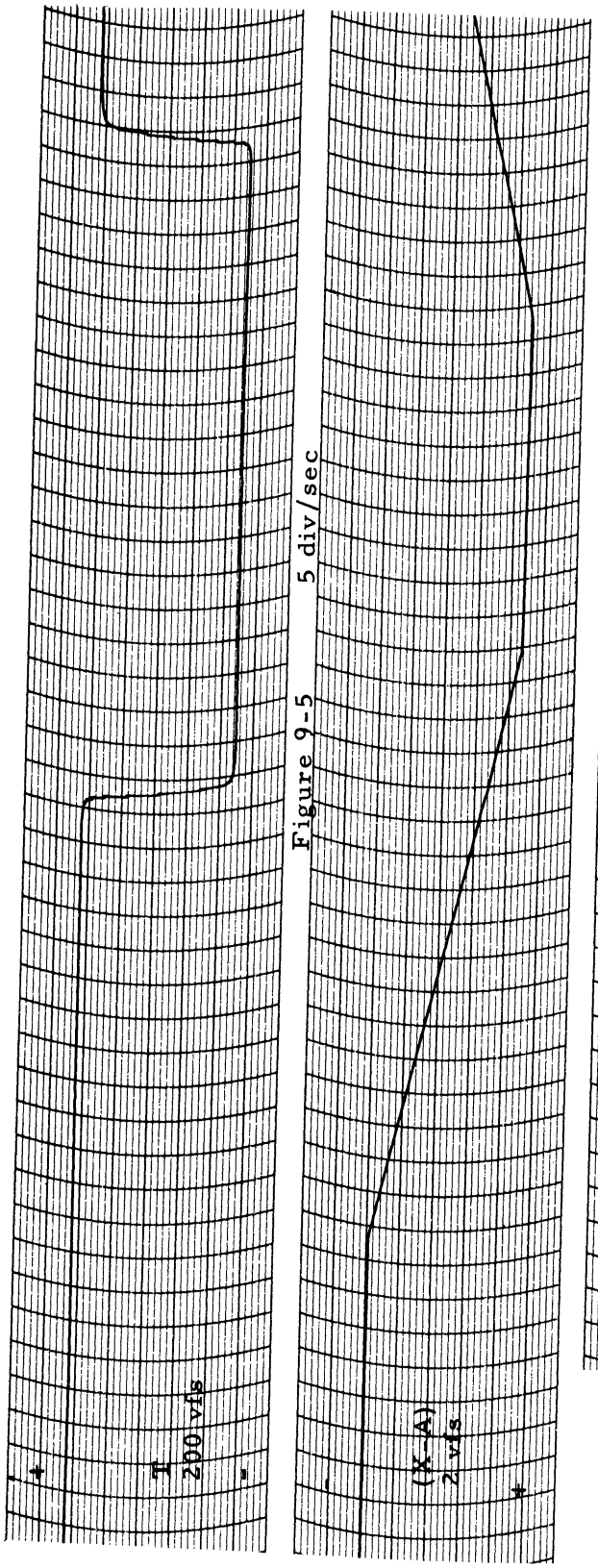


Figure 9-5

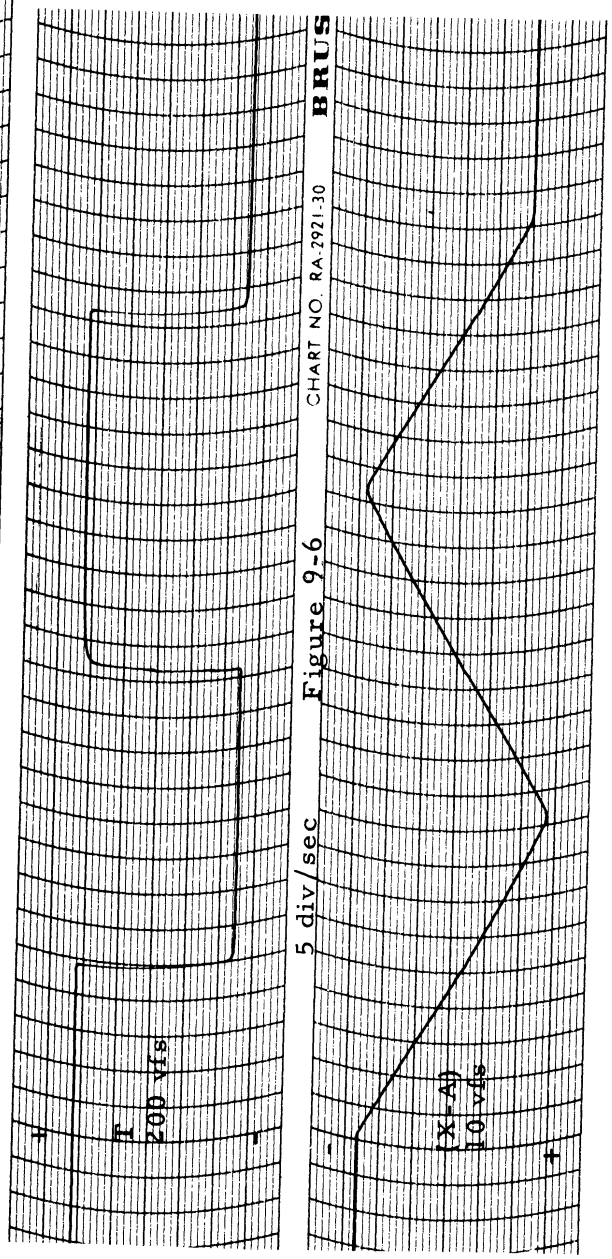


Figure 9-6

trace. This response duplicates the predicted hazard switching response of Figure 6-4. Figure 9-7 is the response for a system hazard delay that is not sufficient to cause a limit cycle away from the optimum point.

Figure 9-8 shows the control system action when a small amount of switching delay is placed in the logic network. Note the improvement in the $\dot{Y}$ signal trace as the hazard switching duration is decreased. Figure 9-9 shows the system response when sufficient switching delay is provided to eliminate the hazard effect. The $\dot{Y}$ response trace shows definite improvement. The above figures may be compared with Figures 9-10(a) and 9-10(b) to evaluate system action. Figure 9-10 shows the limit cycle behavior of the control system when no switching delay is provided to overcome a high degree of hazard switching effect. Note from Figure 9-10(a) that the hazard occurs when the $\dot{Y}$ signal becomes zero. The $\dot{Y}$ output correctly tracks toward the optimum point until the $\dot{Y}$ condition is met, thereafter oscillating about the hazard point.

Figure 9-11(a) and 9-11(b) display proper logic element response with switching delay provided. Note the absence of any ambiguous switching signal in the control output, T, as compared to Figure 9-7(b). Also note the smooth tracking of the $\dot{Y}$ value until the optimum point is reached, thereafter oscillating about the point.

9.3 Typical Flip-Flop Response Using Operational Amplifiers

Flip-flop action with logical inputs is shown to be possible in Chapter 9. Figures 9-12 and 9-13 confirm this response for a conventional "or" circuit and a logical "and" circuit. Figure 9-12 shows

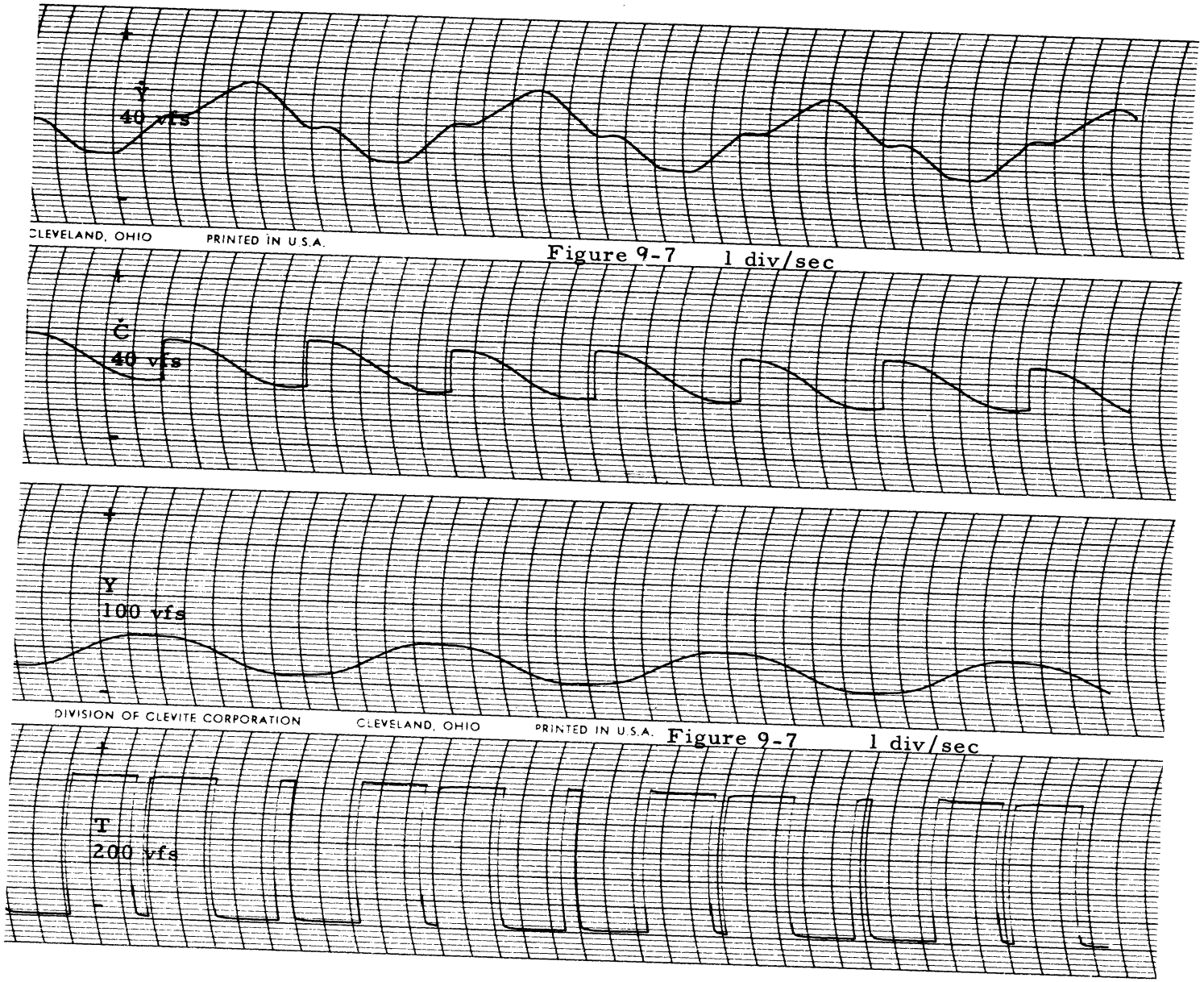
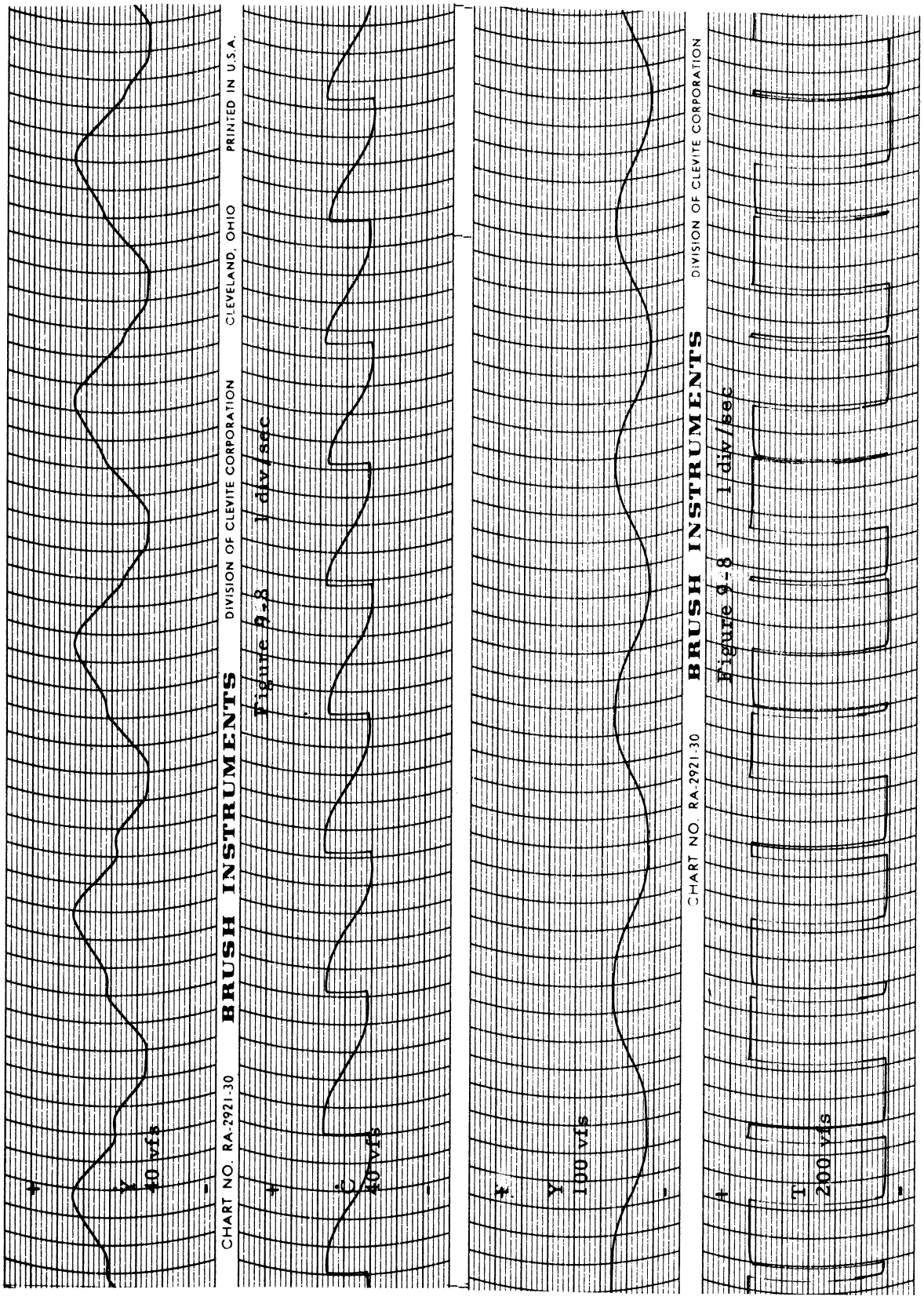
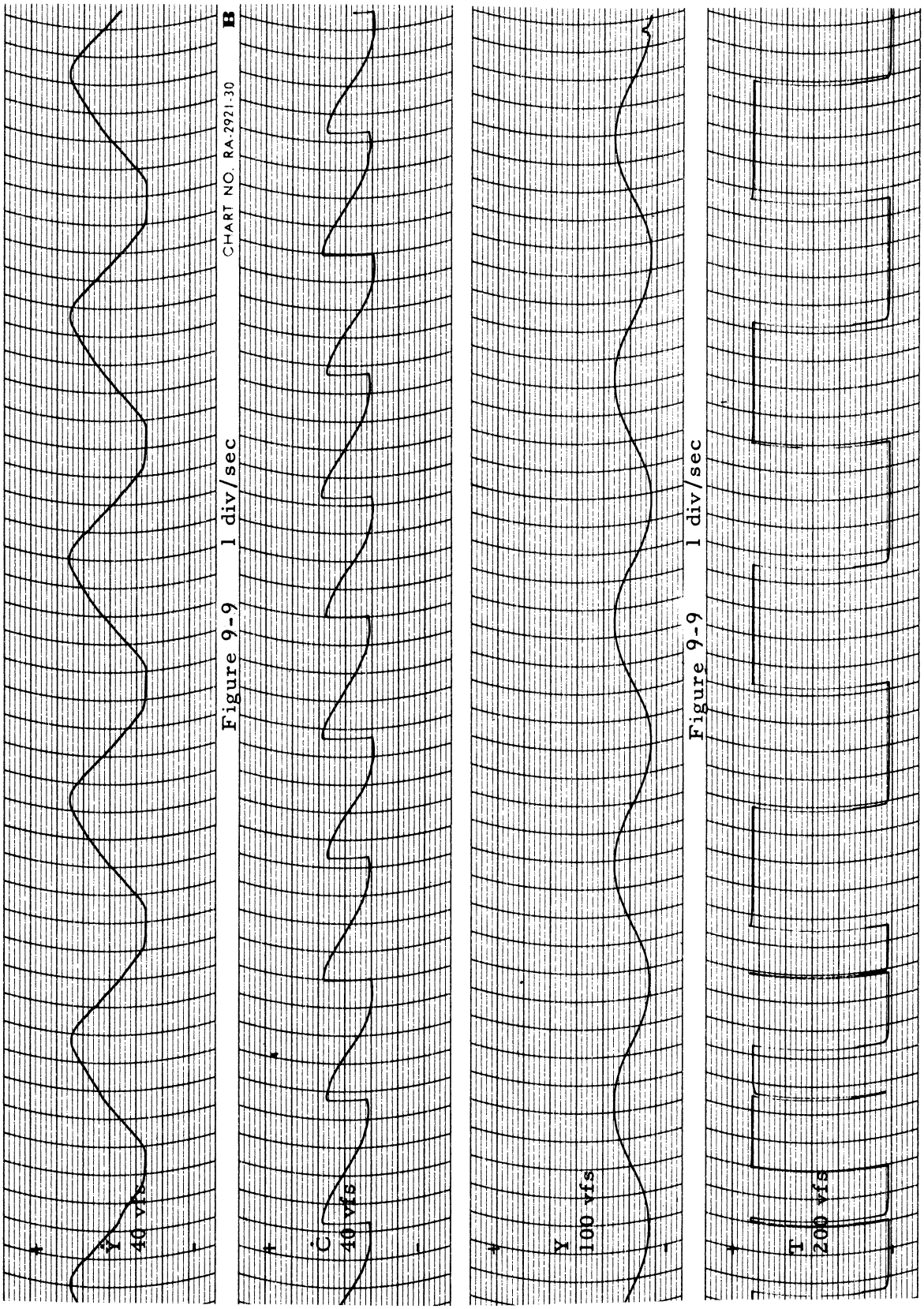
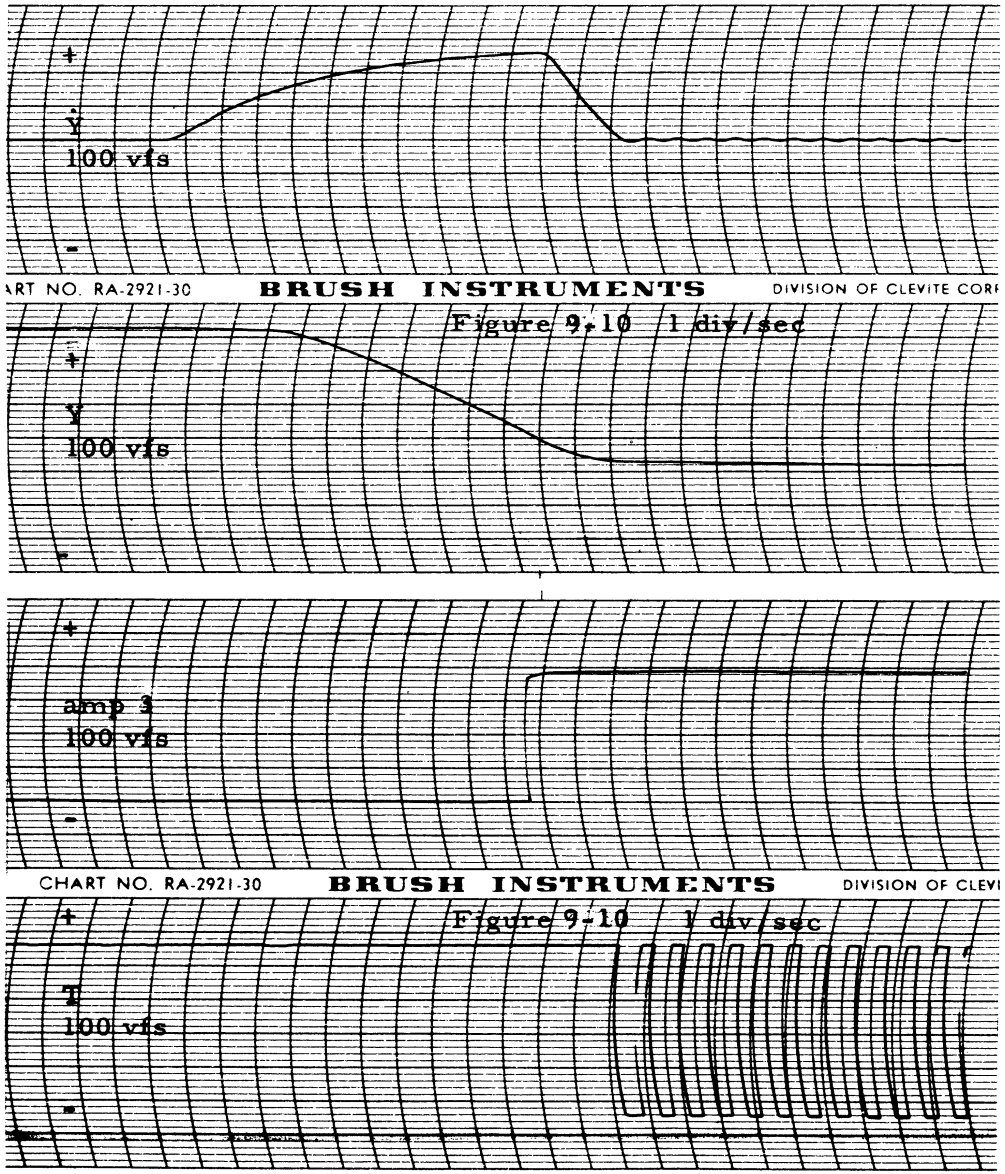


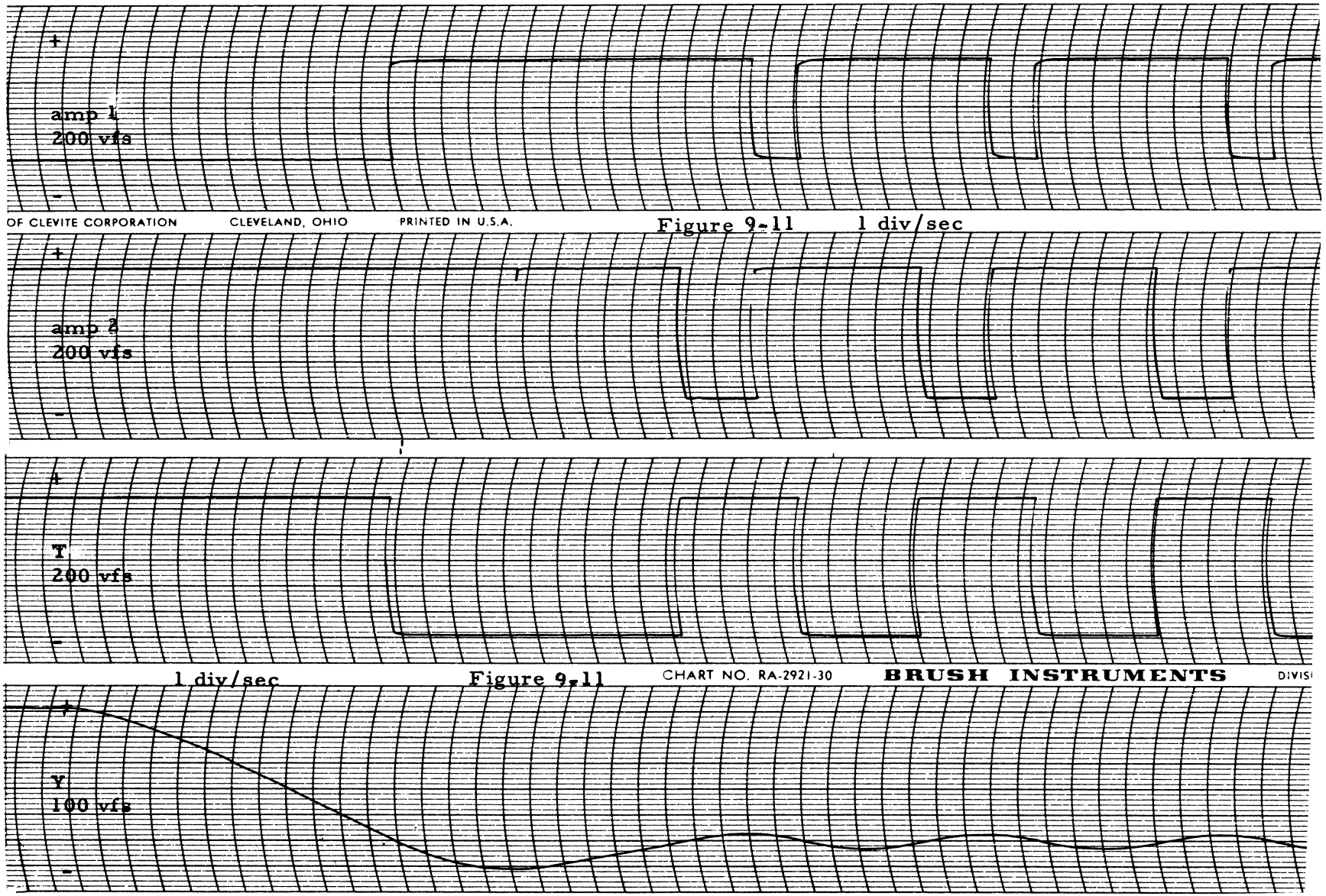
Figure 9-7 1 div/sec

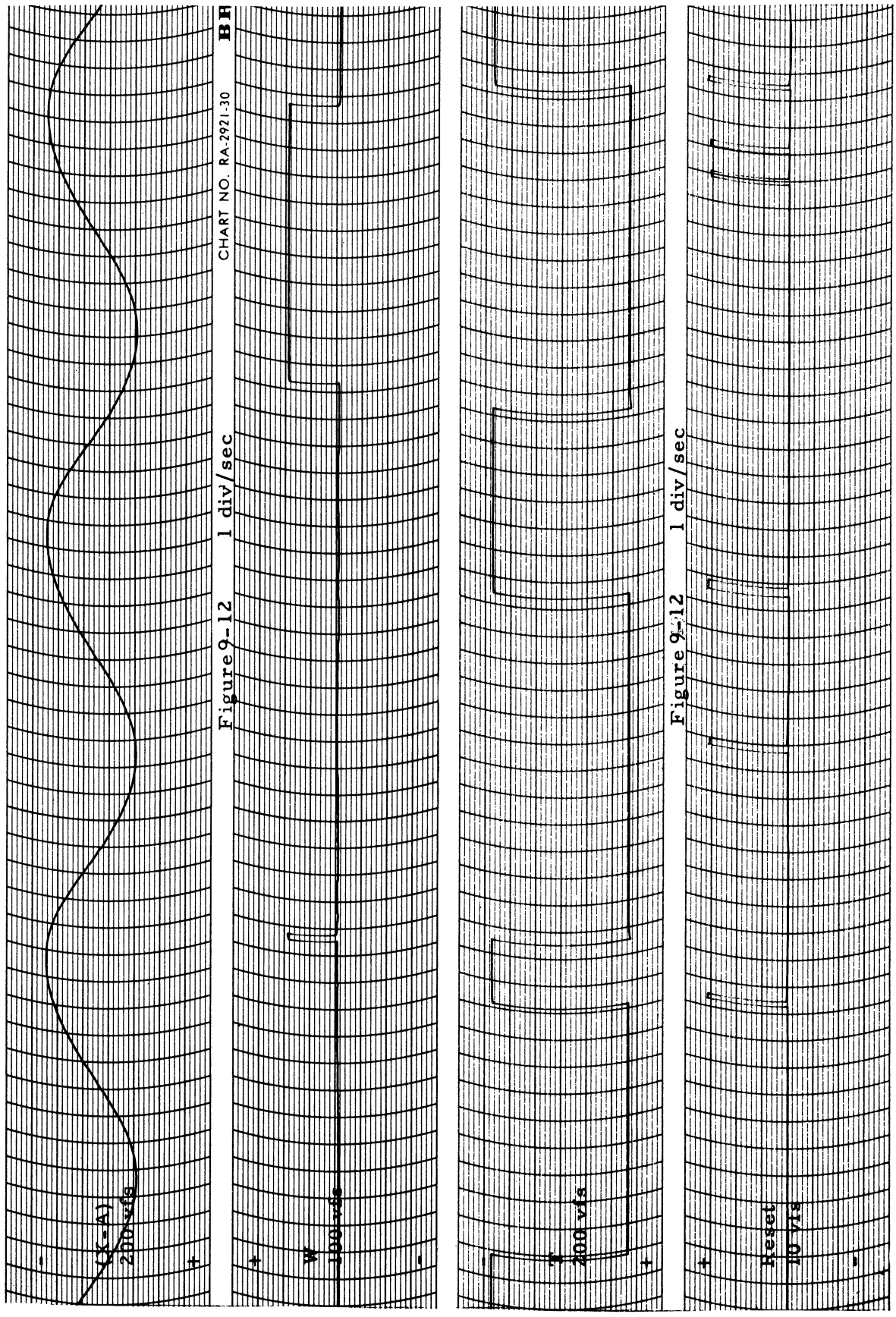
Figure 9-7 1 div/sec

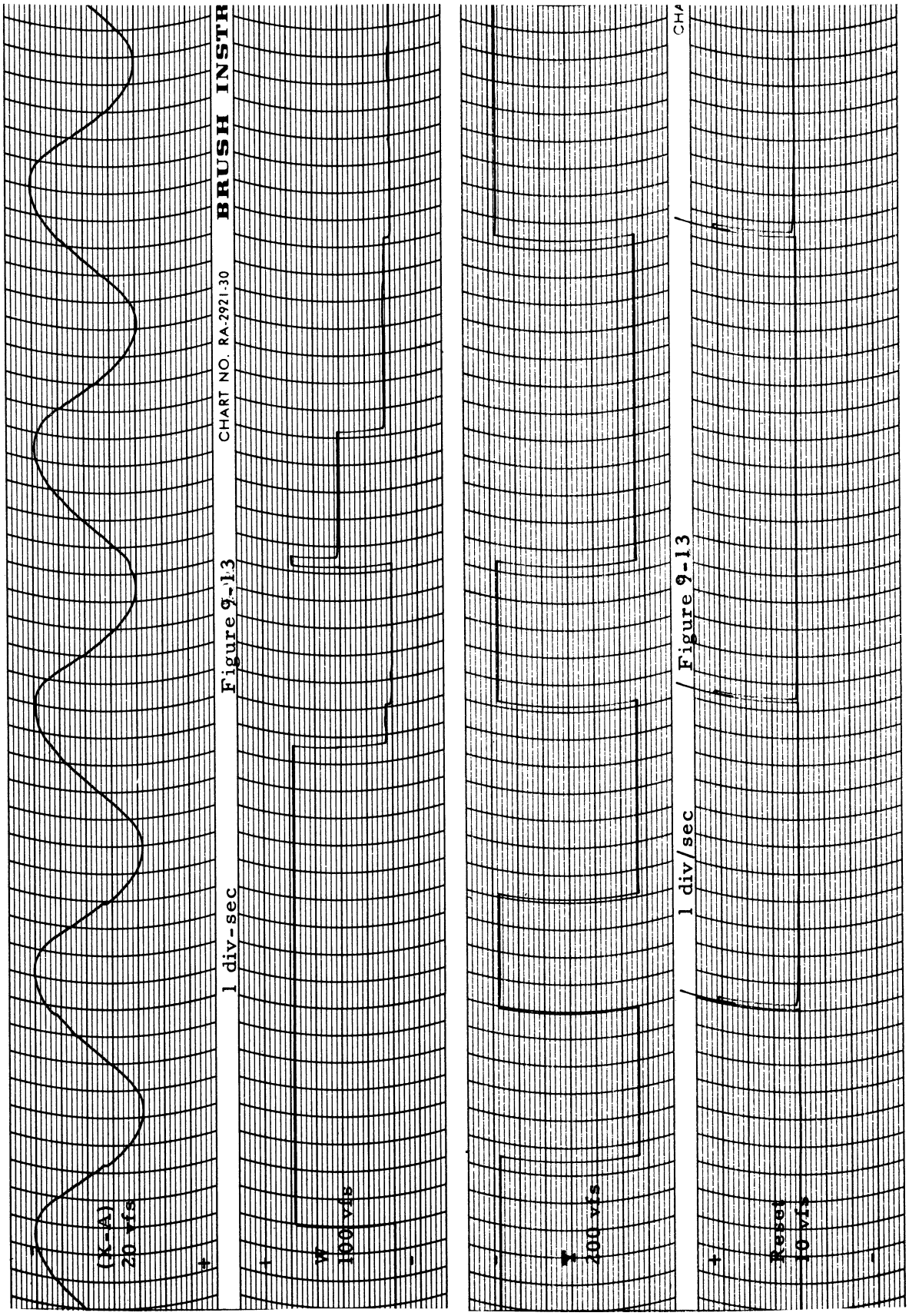

+
X
40 v/s
-
CHART NO. RA-2921-30
BRUSH INSTRUMENTS
DIVISION OF CLEVITE CORPORATION
CLEVELAND, OHIO
PRINTED IN U.S.A.
Figure 9-8 1 div/sec
+
Z
40 v/s
-
+
Y
100 v/s
-
CHART NO. RA-2921-30
BRUSH INSTRUMENTS
DIVISION OF CLEVITE CORPORATION
Figure 9-8 1 div/sec
+
T
200 v/s
-


B
CHART NO. RA-2921-30
Y
40 vfs
+
-
Figure 9-9 1 div/sec
C
40 vfs
+
-
Figure 9-9 1 div/sec
Y
100 vfs
+
-
3
T
200 vfs
+
-


+
Ẏ
100 vfs
-
ART NO. RA-2921-30
BRUSH INSTRUMENTS
DIVISION OF CLEVITE CORP
Figure 9-10 1 div/sec
+
Y
100 vfs
-
+
amp 3
100 vfs
-
CHART NO. RA-2921-30
BRUSH INSTRUMENTS
DIVISION OF CLEVI
Figure 9-10 1 div/sec
+
T
100 vfs
-


+
amp 1
200 vfs
-
OF CLEVITE CORPORATION CLEVELAND, OHIO PRINTED IN U.S.A.
Figure 9-11 1 div/sec
+
amp 2
200 vfs
-
+
T
200 vfs
-
1 div/sec
Figure 9-11
CHART NO. RA-2921-30
BRUSH INSTRUMENTS
DIVISI
+
Y
100 vfs
-


(X-A)
200 v/s
W
100 v/s
CHART NO. RA-2921-30
BR
Figure 9-12 1 div/sec
Reset
10 v/s
Figure 9-12 1 div/sec


BRUSH INSTR
CHART NO. RA-2921-30
Figure 9-13
1 div-sec
(X-A)
20 vfs
+
-
W
100 vfs
+
-
Figure 9-13
1 div/sec
CHA
200 vfs
+
-
Reset
10 vfs
+
-

the response for an input expressions of the form:

$$t_+ = (X > A) + w \qquad (9\text{-}3)$$

Note the action of the reset pulse in Figure 9-12(b) in which R does not effect the circuit output if the input expression is still valid. Figure 9-13 shows the response for the analogous expression to Equation (9-3) above,

$$t_- = (X < A) \cdot w \qquad (9\text{-}4)$$

Note in Figure 9-13(b) the relatively low value of the reset pulse R required to reset the flip-flop action. Also, as expected, once the circuit has been set, the variation in either of the variable inputs, continuous or binary, does not affect the flip-flop output. Figure 9-13(a) displays this effect quite sharply.

9.4 Basic Circuit Operation for Continuous Signal Logic

Logical operations using continuous input signals have already been described in Chapter 4. Figures 9-14 through 9-17 display the dual form of the basic circuits, as predicted in Figure 4-2 and 4-3. Figure 9-14(c) shows the operation of a maximizer circuit for two inputs, shown in Figure 9-14(a) and 9-14(b). Note from the polarity being used that the input signals operate in a continuous mode analogous to mode 1 already described. Hence, the output correctly follows the maximum of the two positive input signals. The basic circuit configuration used for the data of Figures 9-14 and 9-15 is that of Figure 4-3.

When the input mode is changed to operation analogous to mode 2, this same configuration becomes a minimization circuit. Figure 9-15(c) displays the circuit output for continuous negative inputs shown in

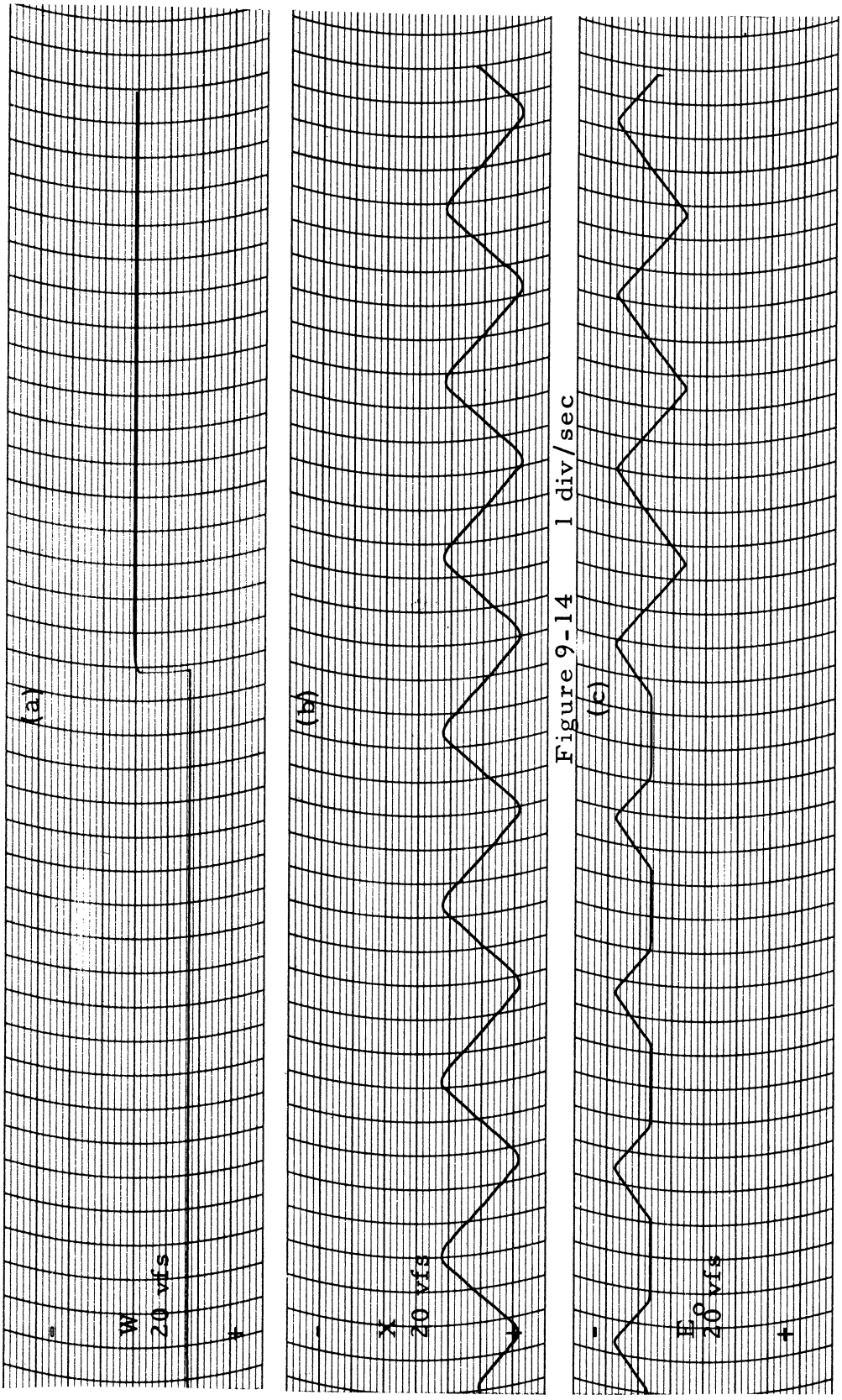


Figure 9-14 1 div/sec

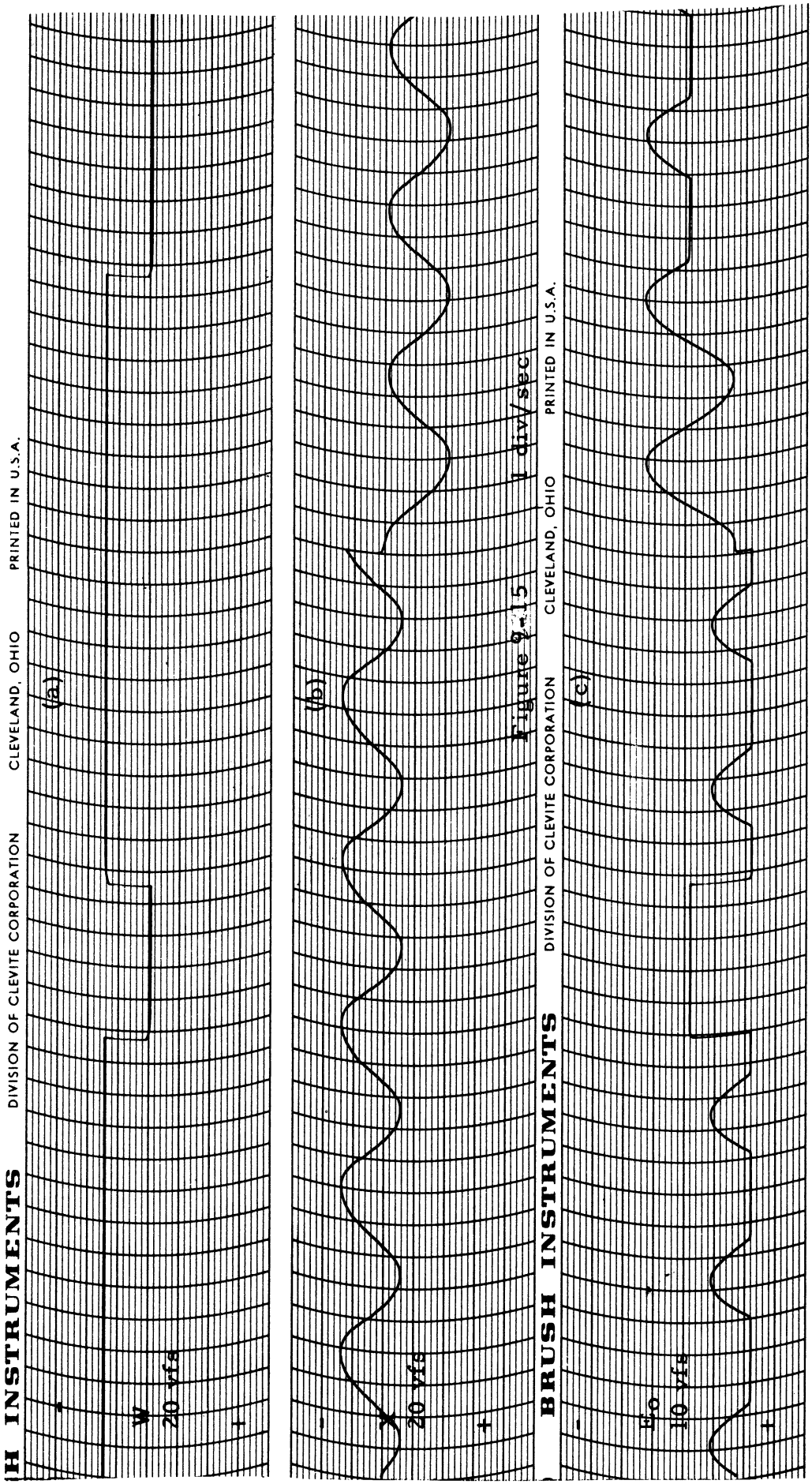

(a)
W
20 v/s
(b)
X
20 v/s
1 div/sec
(c)
E-o
10 v/s
BRUSH INSTRUMENTS
DIVISION OF CLEVITE CORPORATION
CLEVELAND, OHIO
PRINTED IN U.S.A.

Figure 9-15

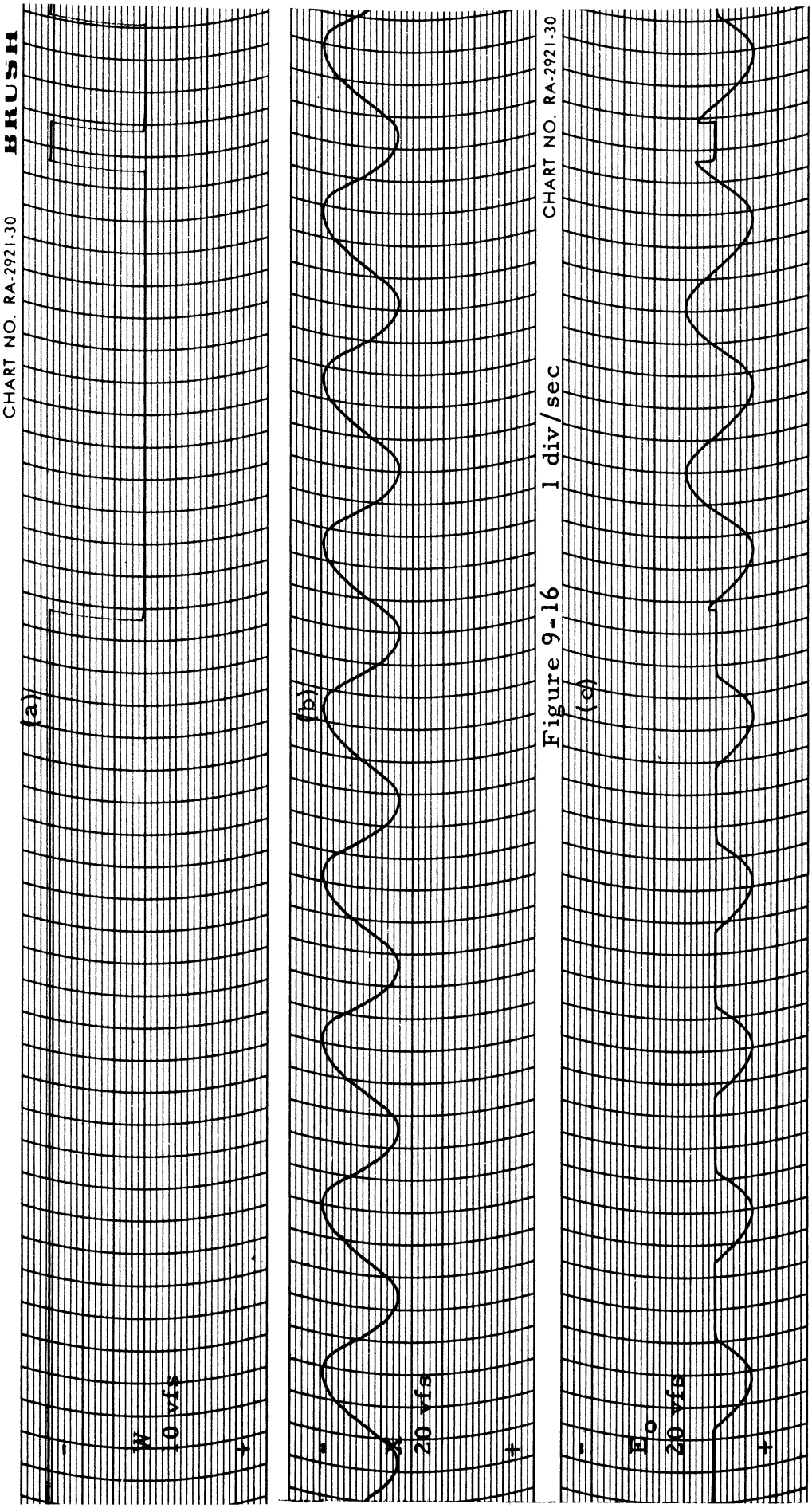


Figure 9-16 1 div/sec
(cp)

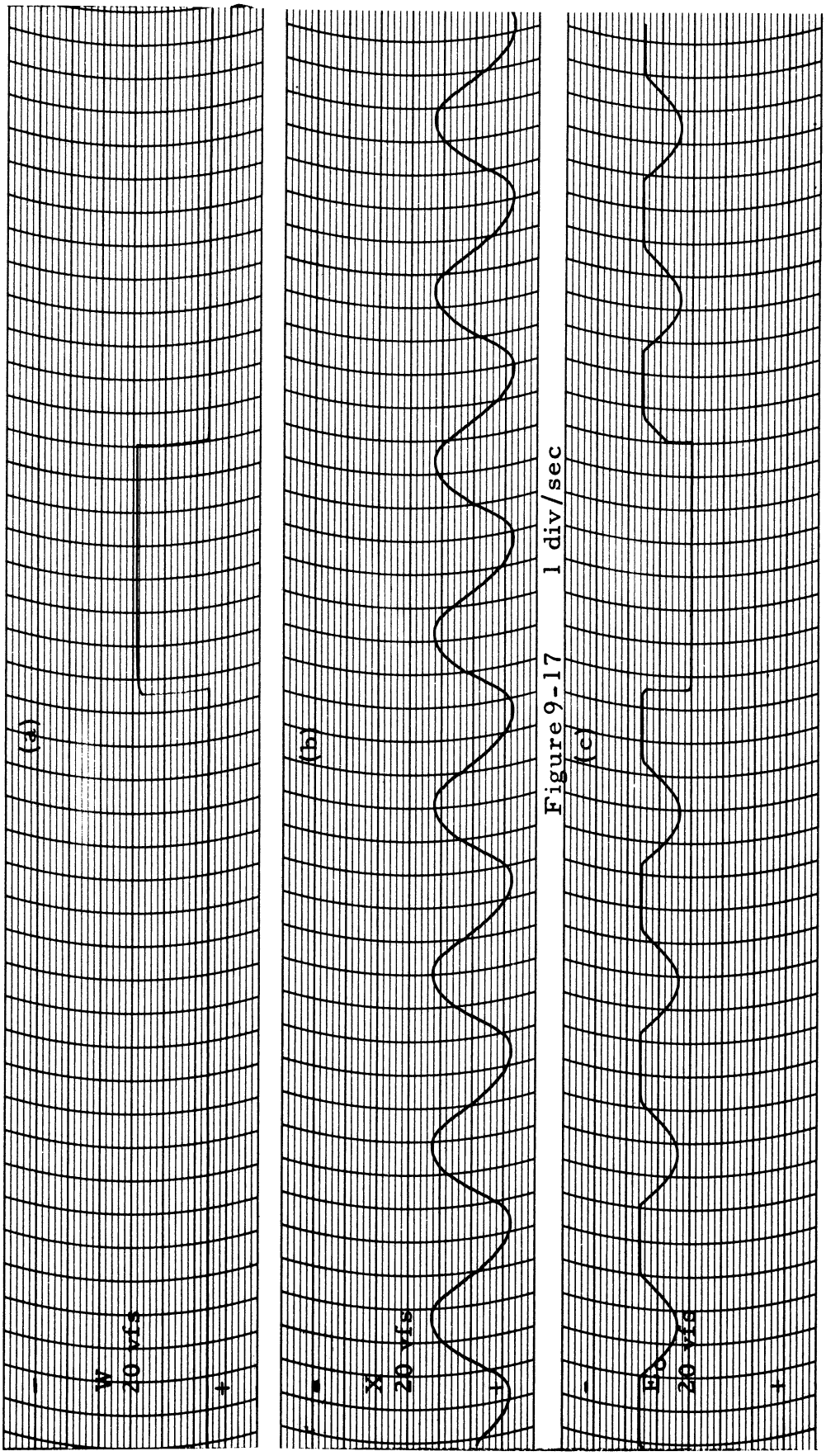


Figure 9-17 1 div/sec

Figure 9-15(a) and (b). The operation is as expected, the output constantly following the minimum of the two input signals. Thus, the same circuit configuration can be used as a signal maximizer or minimizer by proper choice of the mode of operation.

Similar to above, Figures 9-16 and 9-17 display the duality of logical operations for the second configuration used, that of Figure 4-2. Figure 9-16(c) shows the output correctly following the maximum of the two negative inputs, thus performing signal maximization for mode 2 operations. Figure 9-17(c) likewise shows the dual operation when mode 1 input signals are used. Note that (c) correctly follows the minimum signal input as expected.

One additional point should be mentioned concerning operation of the two configurations. Either configuration can be used for maximum or minimum signal selection when mode 3 operation is specified. Similar to the dual form seen above, the maximum or minimum signal will be selected depending upon which maximum voltage, +100 or -100 volts, is chosen as the zero or one reference. Since a full 200 volt bias signal is used, the entire voltage range of the variable available on the computer, -100 to +100 volts, may be used as inputs. However, there is a definite disadvantage in forming the complement of a logical expression if the full voltage range is used for inputs. Thus, operation analogous to mode 1 or mode 2 will permit ease of complementation by simple inversion.

9.5 Conclusions

It has been shown in the derivations of previous chapters, and in the empirical data of this chapter, that rather effective logical operations may be carried out using operational amplifiers on analog computing

equipment. In particular, some forms of logical circuitry involving comparisons and ordering relationships can be implemented quite simply by using operational amplifiers in diode networks.

It is not the purpose of this study to suggest that static logic networks be implemented on computer equipment for permanent control applications. Rather, it is suggested that conventional analog computer equipment can be used quite conveniently for checking out the logical circuitry. Since most control systems are simulated on analog computer equipment for design purposes, the input signals, either binary or continuous in form, are readily available for logical operations. It is interesting to note from Figures 9-7 through 9-13 that basic logical quantities such as delays are also available from this type of logical circuitry. In effect, what has been done in this study is to investigate the basic logical operations available on analog computing equipment and to simulate those operations using conventional operational amplifier circuits.

Chapters 6 and 7 show that this type of logical simulation does have application to some control systems. In particular, the logical control for the optimalizing system of Chapter 6 requires only 3 amplifiers, including the adjustable delay circuitry. Reference (12) indicates conventional logical implementation requires a great deal more equipment. Although it is not within the scope of this study, the author wishes to point out the implications of control logic simulation to applications involving process control and industrial automation. Chapter 7 shows the ease with which an application involving ordering relations can be implemented.

APPENDIX 1

BOOLEAN ALGEBRA TECHNIQUES

To illustrate the application of Boolean Algebra to logical expressions involving operational amplifiers, the basic derivation of the algebra will be given together with a summary of pertinent theorems, stated without proof. For a complete discussion of theorems and proofs, the reader is referred to references (1), (2) and (5) in which rigorous derivations and complete proofs are given for the system.

A-1 Fundamental Derivations

We begin by defining a set K of elements a, b, c,... which are combinable under two operations designated as logical addition "+" and logical product "•" . The postulates of the system may then be stated as follows:

P1a: For every a,b in K, $a + b$ is also in K

P1b: For every a,b in K, $a \cdot b$ is also in K

P2a: For every a in K, there exists an element 0 such that $a + 0 = a$

P2b: For every a in K, there exists an element 1 such that $a \cdot 1 = a$

P3a: For every a,b in K, $a + b = b + a$

P3b: For every a,b in K, $a \cdot b = b \cdot a$ } (commutative law)

P4a: For every a,b,c in K, $a + (b + c) = (a + b) + c$

P4b: For every a,b,c in K, $(a \cdot b) \cdot c = a \cdot (b \cdot c)$ } (associative)

P5a: For every a,b,c in K, $a + (b \cdot c) = (a + b) \cdot (a + c)$

P5b: For every a,b,c in K, $a \cdot (b + c) = (a \cdot b) + (a \cdot c)$ } (distributive)

P6: For every element a of K, there exists an element $\bar{a}$ in K such that

$$\left.\begin{aligned} a + \bar{a} &= 1 \\ a\ \bar{a} &= 0 \end{aligned}\right\} \text{(complementation)}$$

From the above postulates, the following theorems are stated without proof.

T1a: The element 0 is unique

T1b: The element 1 is unique

T2a: $a + a = a$
T2b: $a \cdot a = a$ } (idempotent)

T3a: $a + 1 = 1$

T3b: $a \cdot 0 = 0$

T4a: $a + a \cdot b = a$

T4b: $a \cdot (a + b) = a + a \cdot b = a$

T5: $\bar{a}$ is uniquely determined

T6: $(\bar{\bar{a}}) = a$

T7a: $\overline{(a + b)} = \bar{a} \cdot \bar{b}$
T7b: $\overline{(a \cdot b)} = \bar{a} \vee \bar{b}$ } (DeMorgan's Laws)

T8: $a + \bar{a} \cdot b = a + b$

T9: $a \cdot (\bar{a} + b) = a \cdot b$

T10: $(a + b) \cdot (a + c) = (a \cdot c) + (a \cdot b)$

T11a: $\overline{(a \cdot c + b \cdot c)} = (\bar{a} \cdot c) + (\bar{b} \cdot \bar{c})$

T11b: $\overline{(a + c)\ (b + \bar{c})} = (\bar{a} + c) \cdot (\bar{b} + \bar{c})$

Note the interesting dual nature of the + and $\cdot$ operations. Duality is a result of Boolean Algebra laws and provides symmetry to the logical operations. Given one equation as valid, its dual is also then valid as well as its complement and the dual of the complement. For example, from postulate P5a:

$$a + (b \cdot c) = (a + b) \cdot (a + c) \qquad \text{(A-1)}$$

The dual is formed by replacing all + by • and all • by + as follows

$$a \cdot (b + c) = (a \cdot b) + (a \cdot c) \qquad \text{P5b}$$

The complement of the first expression is by theorem 8:

$$\bar{a} \cdot (\bar{b} + \bar{c}) = (\bar{a} \cdot \bar{b}) + (\bar{a} \cdot \bar{c}) \qquad \text{(A-2)}$$

Using the substitution technique, the dual of Equation (A-2) then becomes:

$$\bar{a} + (\bar{b} \cdot \bar{c}) = (\bar{a} + \bar{b}) \cdot (\bar{a} + \bar{c}) \qquad \text{(A-3)}$$

Thus, by proving the validity of one expression, four dual relations have been proven valid.

Ordering relations involving continuous variables, such as $(A > B)$ and $(A < B)$, may also be considered as statements for which the validity is a binary quantity, true or false, represented by the usual binary system values 1 or 0 respectively. Also, from set theory conditions, which also form a Boolean Algebra, the principle of set complements may be used such that:

$$\overline{(A > B)} \triangleq (A < B) \qquad \text{(A-4)}$$

Thus, the ordering relationship within parenthesis effectively becomes a binary variable with a defined complement in terms of the complement of the ordering relation. All of the previous rules of Boolean Algebra hold when working with ordering functions. In addition, the complement of any ordering variable is easily expressed by reversing the ordering relationship. As an example, using postulate P5b and

Equation (A-4) above,

$$(A > B) \cdot \{(C < D) + (\overline{X > Y})\} \tag{A-5}$$

may be expressed as:

$$(A > B) \cdot (C < D) + (A > B) \cdot (\overline{X > Y}) \tag{A-6}$$

$$= (A > B) \cdot (C < D) + (A > B) \cdot (X < Y) \tag{A-7}$$

Since ordering relationships form boolean variables, they may be logically combined with any other boolean variable, permitting mixed variables in the same expression. To eliminate any confusion due to notation, capital letters will be used for continuous variables while lower case letters will designate binary variables. For example,

$$T = (A > B) \cdot (x + w \cdot r) + z \cdot (W < 5) \tag{A-8}$$

forms a perfectly valid boolean expression.

A.2 Canonical Forms

Boolean Algebra operations require a standard form for comparison of expressions. The two most common forms are the minterm canonical form and the maxterm canonical form, both applicable to ordering relation logical expressions.

The minterm form is obtained by expanding a given expression, using postulate P6, until all combinations of the given function variables are obtained. Each combination occurs in conjunctive form (logical product $\cdot$) with the sets of combinations connected by disjunction (logical sum +).

For an expression involving n variables, each of which have 2 possible states, there are 2^n possible unique combinations.

Example A-1: Expand $(x \cdot y) + (\bar{x} \cdot z) = T$ into minterm form.

Using postulate P6,

$$(x \cdot y) \cdot (z + \bar{z}) + (\bar{x} \cdot z) \cdot (y + \bar{y}) = T \qquad \text{(A-9)}$$

$$= (x \cdot y \cdot z) + (x \cdot y \cdot \bar{z}) + (\bar{x} \cdot y \cdot z) + (\bar{x} \cdot \bar{y} \cdot z) \qquad \text{(A-10)}$$

For ease of notation, each minterm will be denoted by its binary number equivalent, found by writing 0 for a complemented variable and 1 for an uncomplemented variable. Thus, the simplified minterm notation for the example A-1 above becomes:

$$\underset{7}{(1\ 1\ 1)} + \underset{6}{(1\ 1\ 0)} + \underset{3}{(0\ 1\ 1)} + \underset{1}{(0\ 0\ 1)} = T \qquad \text{(A-11)}$$

The decimal equivalents of the binary numbers are known below each minterm and serve as a convenient notation. Thus, the above example can be written as

$$T = m_1 + m_3 + m_6 + m_7 \qquad \text{(A-12)}$$

where the lower case m denotes a minterm form.

In a dual fashion expressions may be expanded until all disjunctive combinations of the input variables are obtained. Each combination is connected by conjunction. Again, for n input variables, there are 2^n possible maxterm combinations.

Example A-2: Expand $T = (x \cdot y) + (\bar{x} \cdot z)$ into maxterm form.

Using theorem T8 (DeMorgan's law) and postulate P5

$$\bar{T} = \overline{(x \cdot y + \bar{x} \cdot z)} = (\bar{x} + \bar{y}) \cdot (x + \bar{z}) \qquad \text{(A-13)}$$

$$= (x \cdot \bar{x}) + (\bar{x} \cdot \bar{z}) + (x \cdot \bar{y}) + (\bar{y} \cdot \bar{z})$$

$$= (\bar{x} \cdot \bar{z}) + (x \cdot \bar{y}) + (\bar{y} \cdot \bar{z}) \qquad \text{(A-14)}$$

Again using theorem T8

$$T = (\overline{\bar{T}}) = (x + z) \cdot (\bar{x} + y) \cdot (y + z) \qquad \text{(A-15)}$$

Now adding 0 to the first term of (A-15)

$$(x + z) + (y \cdot \bar{y}) = (x + z) \div (x + z) \cdot (1) + (y \cdot \bar{y})$$

$$= (x + z) + (x + z) \cdot (y + y) + (y \cdot y) \qquad \text{(A-16)}$$

$$= \{(x + z) + y\} \cdot \{x + z + y\} \qquad \text{(A-17)}$$

$$= (x + y + z) \cdot (x + \bar{y} + z) \qquad \text{(A-18)}$$

Similarly for the second term of (A-15)

$$(\bar{x} + y) = \bar{x} + y + (z \cdot \bar{z}) = (\bar{x} + y + z) \cdot (\bar{x} + y + \bar{z}) \qquad \text{(A-19)}$$

For the third term

$$(y + z) = (y + z) + (x \cdot \bar{x}) = (x + y + z) \cdot (\bar{x} + y + z) \qquad \text{(A-20)}$$

As in the case of minterm expressions, each maxterm will be denoted by the decimal equivalent of the binary number represented. Thus for example A-2,

$$T = (x + y + z) \cdot (x + \bar{y} + z) \cdot (\bar{x} + y + z) \cdot (\bar{x} + y + \bar{z}) \cdot (x + y + z) \cdot (\bar{x} + y + z) \qquad \text{(A-21)}$$

is denoted as:

$$\underset{7}{(1\ 1\ 1)} \cdot \underset{5}{(1\ 0\ 1)} \cdot \underset{3}{(0\ 1\ 1)} \cdot \underset{2}{(0\ 1\ 0)} \cdot \underset{7}{(1\ 1\ 1)} \cdot \underset{3}{(0\ 1\ 1)} \qquad \text{(A-22)}$$

Note from theorem T2b, $M_j \cdot M_j = M_j$

Hence, $$T = M_2 \cdot M_3 \cdot M_5 \cdot M_7 \qquad \text{(A-23)}$$

Where the capital letter M denotes a maxterm form.

A.3 Theorems and Canonical Transformations

Basic relationships exist between minterm and maxterm forms which allow for convenient transformations. It can be easily verified that the proper relationship is as follows:(1)

$$\bar{m}_i = M_{2^n-1-i} \tag{A-24a}$$

$$\bar{M}_i = m_{2^n-1-i} \tag{A-24b}$$

Where: n = number of binary variables

i = particular term considered

The following basic theorems are stated without proof.

$$\sum_{i=0}^{2^n-1} m_i = 1 \tag{A-25}$$

$$\prod_{i=0}^{2^n-1} M_i = 0 \tag{A-26}$$

$$\left.\begin{aligned} m_i \cdot m_j &= 0 \\ M_i + M_j &= 1 \end{aligned}\right\} \quad i \neq j \tag{A-27, A-28}$$

Now denoting by $f_i = 0,1$ the presence or absence of the i^{th} term, functions may be conveniently expressed in either minterm or maxterm form by the following notations:

$$f = \sum_{i=0}^{2^n-1} f_i \cdot m_i = \prod_{i=0}^{2^n-1} (f_i + M_{2^n-1-i}) \tag{A-29}$$

The basic theorems (A-24) through (A-29) are important because they show that any boolean function may be written in both minterm and maxterm form.

Using the above canonical notation, ordering relation variables may also be denoted as being in minterm or maxterm form for simplication. Thus,

$$(Y > 3) \cdot (Z < 5) + (w) \cdot (R > K)$$

is in minterm form while

$$[(Y > 3) + (Z < 5)] \cdot [(w) + (R > K)]$$

is in maxterm form. Standard boolean reduction techniques, including mapping methods, may be applied to all of the above canonical forms. These techniques are particularly well covered in references (1), (2), and (3).

APPENDIX 2

ALGEBRAIC TREATMENT OF CONTINUOUS INPUT SIGNAL LOGIC

Given a system involving variables A, B, C, ..., X which may be normalized to lie in the range $0 \leq X \leq 1$, an interesting logic system may be derived. From the above system, the following operations are defined:

$$\begin{array}{lll} \text{Logical And:} & A \circ B & \text{Minimum } [A,B] \\ \text{Logical Or :} & A \vee B & \text{Maximum } [A,B] \end{array} \qquad \text{(A-30)}$$

Applying lattice theory to such a system[6], it can be shown that any boolean identity, using the $\circ$, $\vee$ relations, is valid if complementation is not involved in the identity.

These identities are summarized below:

$$A \circ A = A \qquad \text{(A-31)}$$

$$A \circ B = B \circ A \qquad \text{(A-32)}$$

$$A \circ (B \circ C) = (A \circ B) \circ C \qquad \text{(A-33)}$$

$$A \circ (B \vee C) = (A \circ B) \vee (A \circ C) \qquad \text{(A-34)}$$

$$A \circ (A \vee B) = A \qquad \text{(A-35)}$$

$$1 \circ A = A \qquad \text{(A-36)}$$

$$0 \circ A = 0 \qquad \text{(A-37)}$$

$$A \vee A = A \qquad \text{(A-38)}$$

$$A \vee B = B \vee A \qquad \text{(A-39)}$$

$$A \vee (B \vee C) = (A \vee B) \vee C \qquad \text{(A-40)}$$

$$A \vee (B \circ C) = (A \vee B) \circ (A \vee C) \qquad \text{(A-41)}$$

$$A \vee B \circ A = A \qquad \text{(A-42)}$$

$$A \vee 0 = A \tag{A-43}$$

$$A \vee 1 = 1 \tag{A-44}$$

The inclusion relation $A \subseteq B$ may also be used and appears as

$$A \cdot B = A \tag{A-45}$$

$$A \vee B = B \tag{A-46}$$

Where $A \leq B$

If the complement relation is defined as:

$$\bar{A} \triangleq 1 - A \tag{A-47}$$

DeMorgan's laws, theorem T7, may also be used. Hence,

$$\overline{A \cdot B} = \bar{A} \vee \bar{B} \tag{A-48}$$

$$A \vee B = A \cdot B \tag{A-49}$$

Also, the rule of involution directly follows from DeMorgan's law:

$$(\bar{\bar{A}}) = A \qquad 1 - (1 - A) = A \tag{A-50}$$

Not all the rules of Boolean Algebra follow however. In particular,

$$a \cdot \bar{a} = 0$$

$$a + \bar{a} = 1$$

P6

must be replaced for continuous variable logic by the expression

$$A \cdot \bar{A} \subseteq B \vee \bar{B} \tag{A-51}$$

Where $A \leq B$

For questionable identities, the validity of an expression may be checked by substitution of the continuous values into both sides of the expression. The following example demonstrates this technique.

Example A-3: Show that the boolean identity

$$(a + b) \cdot (\bar{a} + c) = (a \cdot c) \ (\bar{a} \cdot b) + (b \cdot c)$$

does not hold for continuous signal logic.

Let $A = \frac{1}{2}$, $B = 1$, $C = 1$, $\bar{A} = 1 - \frac{1}{2} = \frac{1}{2}$

Substituting into both sides of the identity

$$(A \vee B) \cdot (\bar{A} \vee C) = (\tfrac{1}{2} \vee 1) \cdot (\tfrac{1}{2} \vee 1) = \tfrac{1}{2}$$

while

$$(A \cdot C) \vee (\bar{A} \cdot B) \vee (B \cdot C) = (\tfrac{1}{2} \cdot 1) \vee (\tfrac{1}{2} \cdot 1) \vee (1 \cdot 1) = 1$$

Thus the two sides are not equivalent and the identity fails.

Using the formal reduction rules of Equation (A-31) through (A-50), logical expressions involving the "$\vee$" and "$\cdot$" relations between continuous signals may be reduced by algebraic methods. However, the systematic reduction methods of Boolean Algebra in general are not allowed since they depend upon the expansion of the function into canonical form. Because of the limitation of complement operations, expressed by Equation (A-51), a canonical form expansion equivalent to that of Boolean Algebra cannot be obtained. It is the authors opinion, however, that a mapping method, analogous to Karnaugh[2] mapping methods can be derived. Although such mappings are not now developed, to the authors knowledge, the amount of research being conducted on many value logic systems indicates that analogous reduction methods should soon be available.

REFERENCES

(1) Phister, Jr., Montgomery. Logical Design of Digital Computers. New York: John Wiley & Sons, Inc., (1958), Chapters 2, 3, 4.

(2) Humphrey, Jr., Watts S. Switching Circuits with Computer Applications. New York: McGraw-Hill Book Co., (1958), Chapters 2, 5, 6.

(3) Caldwell, Samuel H. Switching Circuits and Logical Design. New York: John Wiley & Sons, Inc., (1958), Chapters 3, 5.

(4) Stabler, E. R. An Introduction to Mathematical Thought. Reading, Massachusetts: Addison-Wesley Pub. Co., (1953), Chapter 10, 45-48, 193-210.

(5) Nelson, E. C. "An Algebraic Theory for Use in Digital Computer Design." IRE Trans. on Electronic Computers, EC-3, No. 3, (September, 1954), 12-21.

(6) Muller, D. E. "Treatment of Transition Signals in Electronic Switching Circuits by Algebraic Methods." IRE Trans. on Electronic Computers, EC-8, No. 3, (September, 1959), 401.

(7) Jackson, Albert S. Analog Computation. New York: McGraw-Hill Book Co., (1960), 194-199.

(8) Notes for 1960 Summer Intensive Course in Automatic Control, Lecture Demonstration on Diode Circuits for Function Generation. Instrumentation Engr. Program, University of Michigan College of Engineering, Ann Arbor, Michigan.

(9) Britton, J. R. and Snively, L. C. Algebra for College Students. New York: Rinehart & Company, (1959), 334-336.

(10) Pressman, A. I. Design of Transistorized Circuits for Digital Computers. New York: John R. Rider Pub. Co., (1959), 93-113.

(11) Cosgriff, Robert L. Nonlinear Control Systems. New York: McGraw-Hill Book Co., (1958), 304-306.

(12) Cosgriff, Robert L. "Servos that Use Logic Can Optimize," Control Engineering, (September, 1955), 133-135.

(13) Ledley, Robert S. Digital Computer and Control Engineering. New York: McGraw-Hill Book Co., (1960), 295-315.

(14) Culbertson, James T. Mathematics and Logic for Digital Devices. New York: D. Van Nostrand Co., Inc., (1958), Chapters 5, 6, 8.

(15) Korn, G. A. and Korn, T. M. Electronic Analog Computers. 2nd ed. New York: McGraw-Hill Book Co., (1956), 147-151.