1 April 1968

CONCOMP PROJECT MEMORANDUM

TO: Whom it May Concern

FROM: W. Scott Gerstenberger

SUBJECT: Corrections to Concomp Memorandum 9, "Engineering Design Report: PDP-8/CR01B Card Reader Interface."

Because of a conflict in I/O device addresses between the CR01B Card Reader and the DF-32 Disc on the DEC-338, the Card Reader device addresses have been changed (as of 1 February 1968). The IOT assignments are now as given in the table below. The meanings of the IOT's have not been changed.

Mnemonic	New IOT	Old IOT
CRRS	6701	6631
CRRB	6702 or 6742	6632 or 6672
CRSF	6741	6671
CRSA	6704	6634
CRSB	6744	6674

These changes should be marked on page 2 of your report for future reference.

On page 3, the third line should read, "within 1.5 msec ... "

On page 4, the inputs to the R001 (B24) are now MB4(0), MB5(0), MB7(1), and MB8(1).

T H E U N I V E R S I T Y O F M I C H I G A N

Memorandum 9

ENGINEERING DESIGN REPORT: PDP-8/CR01B CARD READER INTERFACE

Stephen F. Lundstrom

CONCOMP: Research in Conversational Use of Computers
F.H. Westervelt, Director
ORA Project 07449

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ENGINEERING DESIGN REPORT: PDP-8/CR01B CARD READER INTERFACE

Stephen F. Lundstrom

INTRODUCTION

The CR01B card reader is a standard interface option available on the Digital Equipment Corporation PDP-7 computer. This report describes the necessary additions to the standard PDP-7/CR01B card reader interface to allow it be used as a PDP-8/CR01B card reader interface in addition. The description of the additions is preceded by a discussion of the CR01B characteristics of concern to a programmer.

Before beginning the main discussion, a word about the origin of this project is in order. The PDP-7 in the Logic of Computers Group was originally purchased with a CR01B card reader. After a short while, it was observed that the card reader could be used to the best advantage if it was available as an input device on the PDP-8(338). The reasons for this were threefold. First, the PDP-7 has, as standard equipment, high speed paper tape handling equipment while the PDP-8(338) does not. Nor does the PDP-8(338) configuration currently have high speed paper tape handling equipment. Second, the necessary programming support for generation of PDP-8 binary card decks was complete, while plans for corresponding PDP-7 facilities were not yet defined. Third, the plans to interface the PDP-7 to an IBM 1800, which had a card reader, were well under way. It was for these reasons that it seemed practical to consider the interface additions described below.

PROGRAMMING CHARACTERISTICS

The CR01B card reader, with the interface additions, operates under the programmed I/O control on the PDP-8. The instructions available to the PDP-8 programmer and their uses are described below.

Mnemonic Symbol	Operation Executed
CRRS (6631)	Skip on card reader ready flag. When a card is present in the card reader read station and power is on at the card reader, the next instruction is skipped. The flag is turned off during the card feed cycle before column one is read and turned back on after column 80.
CRRB (6632 or 6672)	Read data. This instruction ORs data from the card reader into the AC in a format specified by the previous select instruction (see below), and clears the data ready flag.
CRSF (6671)	Skip on card reader data flag. When the card reader data flag is set, indicating that a card column is present and ready to be read, the next instruction is skipped. This flag is connected to the program interrupt facility.
CRSA (6634)	Select alphanumeric. This instruction enables the reader logic to code punched data in BCD form, so that it can be presented to bits 12-17 of the AC (6-11 in PDP-8) during a CRRB command.
CRSB (6674)	Select binary. This instruction enables the reader logic to present the bits read from the card in binary form so that it can be transferred into the AC bits 6-17 (0-11 in PDP-8) during a CRRB command. Each column is read as a 12-bit binary number.

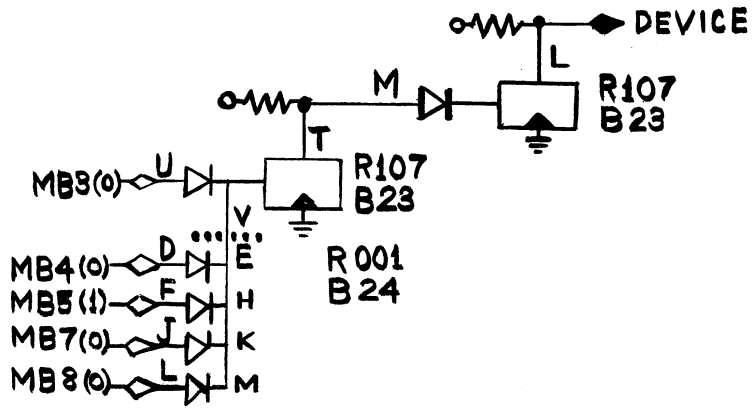
The execution of CRSA or CRSB also moves a new card into position at the read station.

Note that CRRB must be given within 1.5 μsec following setting of the data ready flag. This is because once a card has moved into the read station, it moves completely through with no delays enroute.

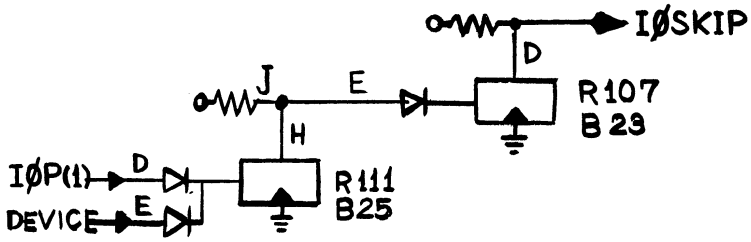
The reader ready status can be read into the AC as part of the I/O status in the PDP-7. On the PDP-8 interface this is a flag that can be skipped on.

INTERFACE ADDITIONS

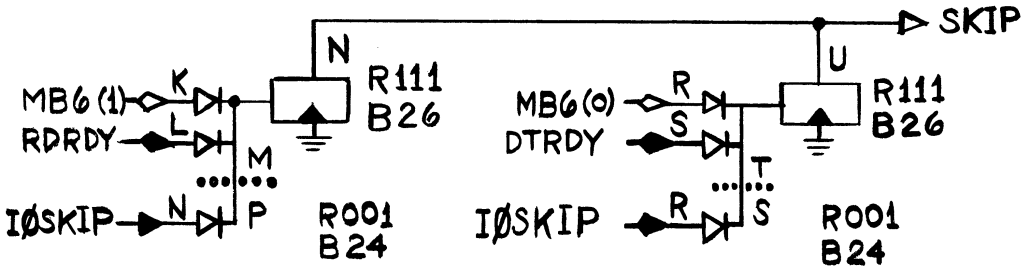
The standard CR01B interface was modified through the addition of the logic required to operate the interface from the PDP-8. This consisted of the cables for the signals to and from the PDP-8 and logic for input-output transfer (IOT) address decoding and accumulator loading. The control signals were wired to the corresponding points at the PDP-7 connector points. The logic diagrams for these additions are on the following pages. The comments to the side of the logic diagrams summarize their various functions.



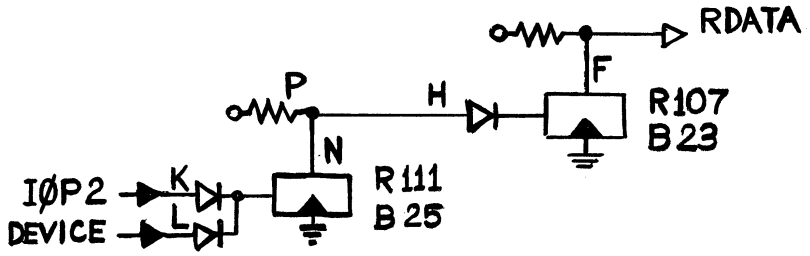
DEVICE SELECTION



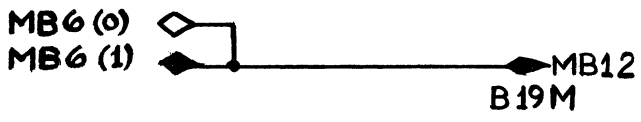
SKIP DECØDING



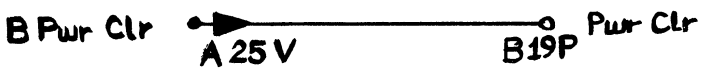
SKIP BUS CØNTRØL



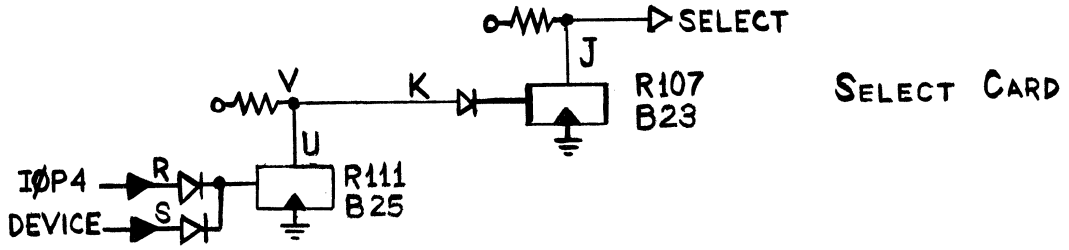
READ DATA INTO ACC.



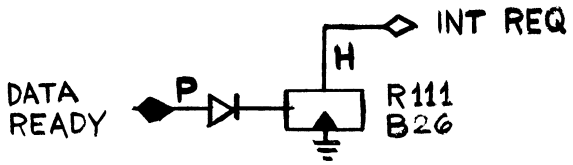
SELECT TYPE OF READ



INITIALIZATION

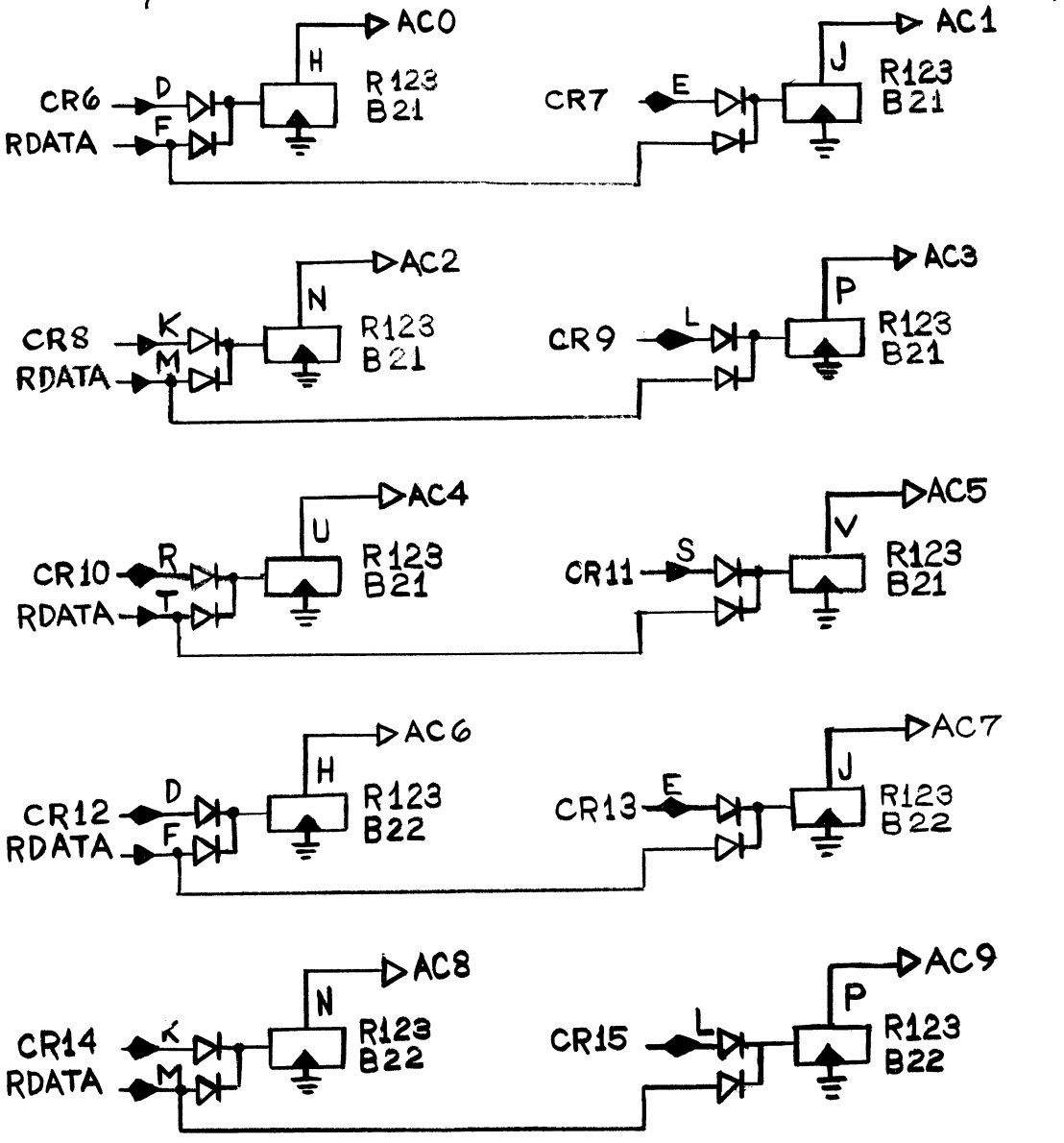


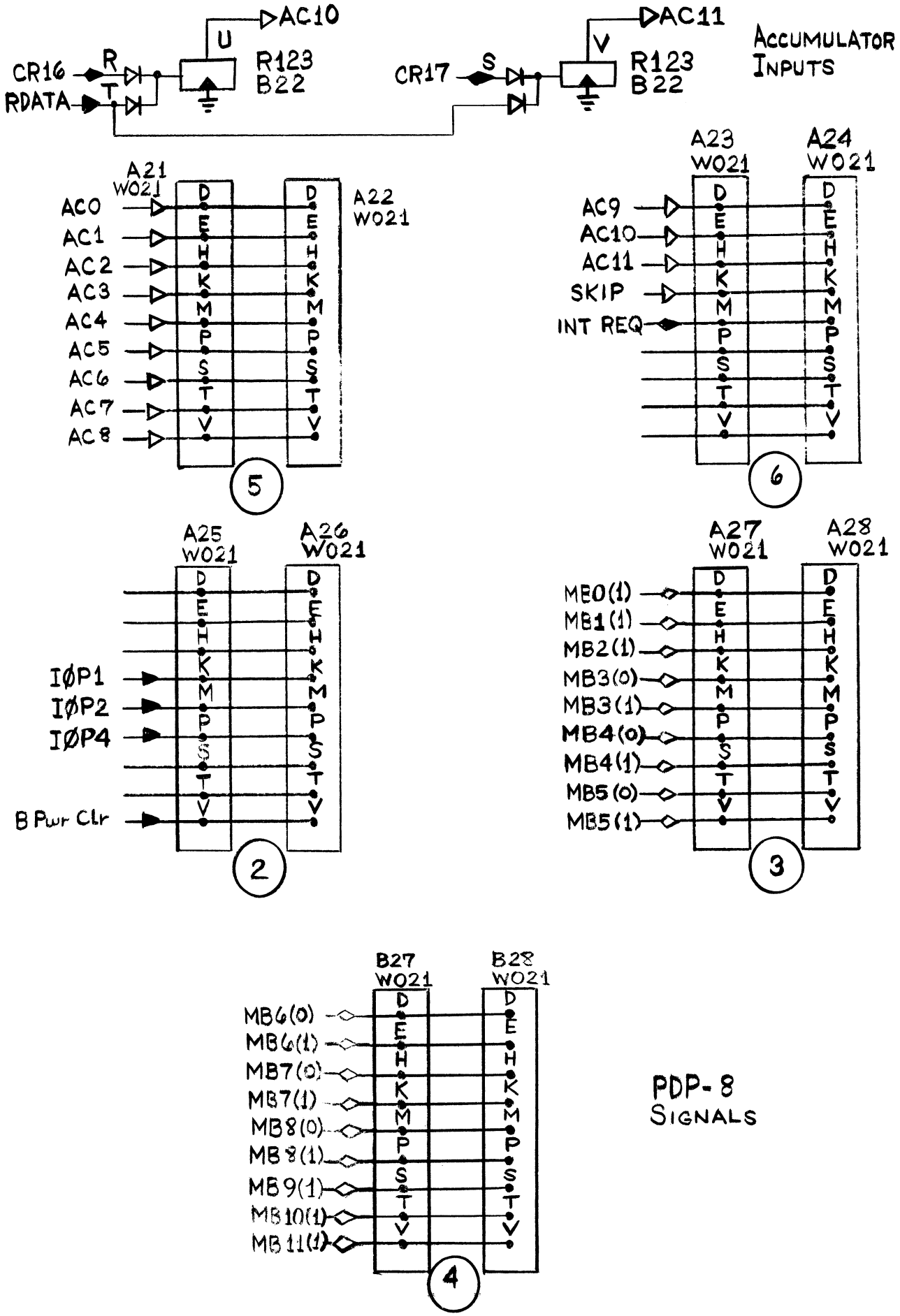
SELECT CARD



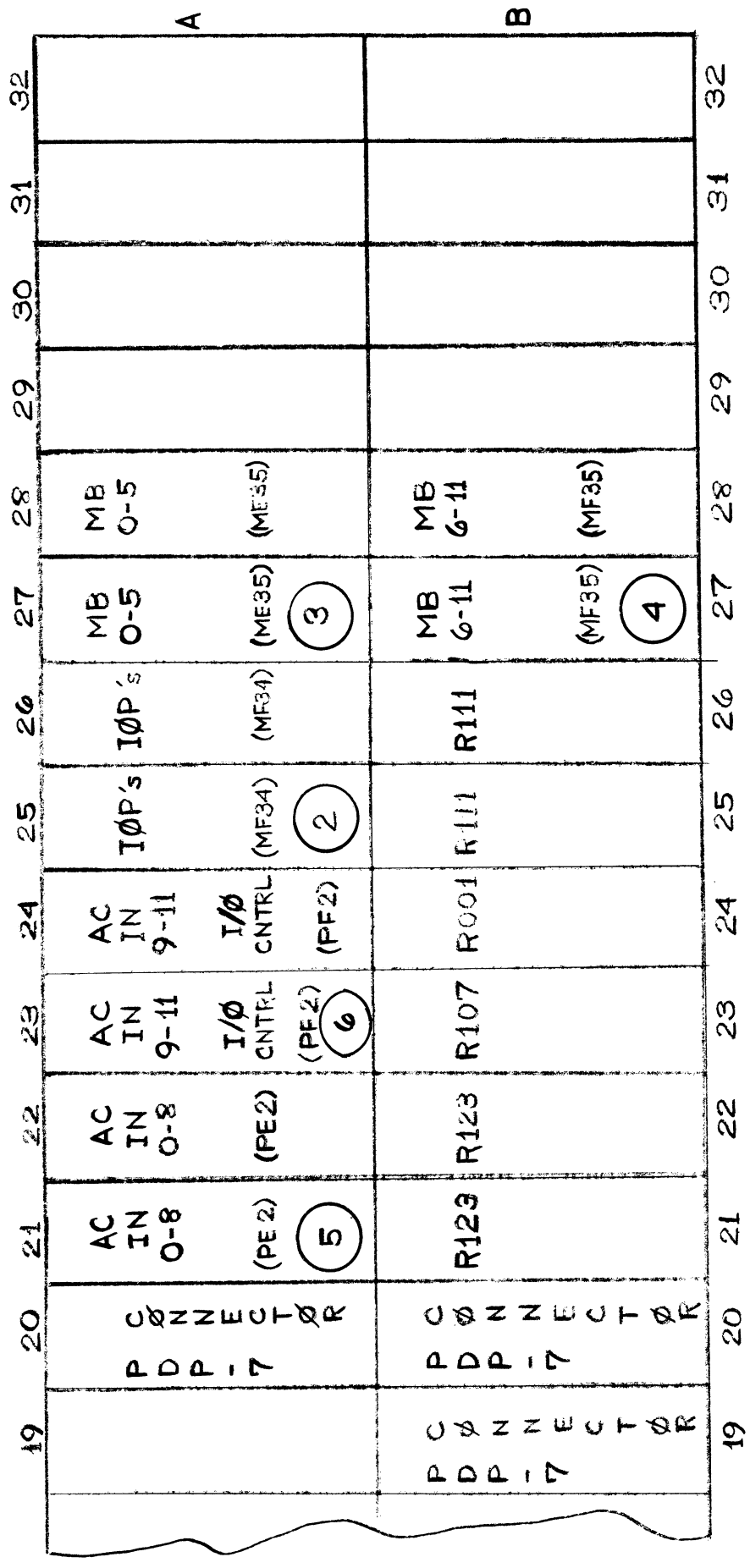
INTERRUPT REQUEST

ACCUMULATOR INPUTS



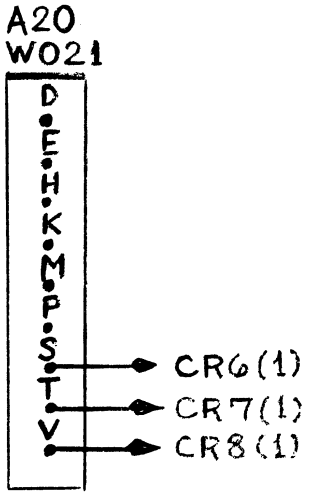
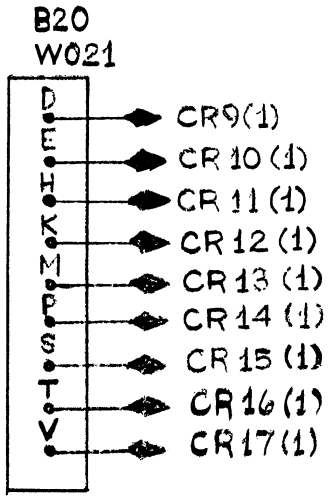
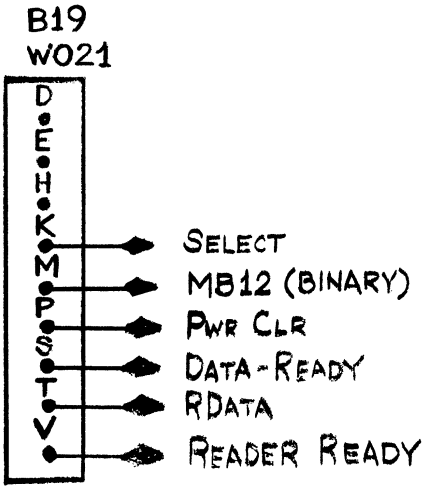


PDP-8
SIGNALS



CR01B

LØGIC ADDITIØNS

LAYOUT DIAGRAM

The connectors shown below are the standard PDP-7 interface connectors. The signals from the interface addition described above are connected to these pins.