THE UNIVERSITY OF MICHIGAN

Memorandum

ENGINEERING DESIGN REPORT: PDP-7/MODIFIED 338 DISPLAY INTERFACE

Stephen F. Lundstrom

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F. H. Westervelt, Director

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ENGINEERING DESIGN REPORT:
PDP-7/MODIFIED 338 DISPLAY INTERFACE

The purpose of the interface to the PDP-7 described below is to allow the modified DEC 338 display control (a DEC 338 display without a PDP-8 processor) to operate with the PDP-7 as its processor. The resulting interface will accept any device that will interface to a PDP-8 except those using the extended data-break facility (three-cycle data break). The addition of such a feature would be a logical extension of the design of this interface but was not attempted because no need existed for it at the time of the original design, and thus it was not economically attractive.

This report will serve as a progress report for those interested in technical progress on the project, and as a maintenance manual for those responsible for system maintenance in the future. Basic design objectives and decisions will be described first. A brief discussion of programming objectives will be followed by a detailed description of the logic involved. An appendix includes a comparison of corresponding interface logic signals on the PDP-8 and the PDP-7.

The only major design decision was to decide what part of the 18-bit PDP-7 word to use to provide the 12-bit PDP-8 data. It was decided to have the data bits associated with the PDP-8 data be the low-order 12 bits. This decision allows the programmer of the modified 338 display to use the high-order bits of core as special flag bits so that the 338 display program may be imbedded in a larger data structure. It also allows use of the LAW (Load Address Word) instruction of the PDP-7 to set up initialization of the display with the programmed accumulator transfer instructions with a minimum of storage requirements. Arguments concerning the instruction field being high-order bits and the sign-bit being the high-order bit were not considered to be overriding because of the different order codes of the two computers and because the PDP-7 generally uses diminished-radix-complement (one's complement) arithmetic while the PDP-8 uses radix complement

(two's complement) arithmetic. Thus representations of negative numbers are different in the two machines. High-order sign-bits are not advantageous as far as the display is concerned, since no data formats have the high-order bit set for negative moves. Logic is provided in the interface to gate the PDP-7 device address (bits 6-11) into the corresponding PDP-8 device address location when not in a data-break cycle. Figure 1 shows the correspondence of accumulator data bits, and Figure 2 shows the correspondence of memory buffer data bits.

PROGRAMMING CONSIDERATIONS

The same device addresses and input-output pulse (IOP) numbers that the 338 system uses are effective in the PDP-7/modified 338 display system except for the locations of the bits in the PDP-7 instructions. PDP-7 subdevice addresses are not used, but the clear-accumulator bit remains effective. As mentioned above, the modified 338 display considers its instructions to be in the low-order 12 bits of memory words. It ignores the contents of the high-order six bits except when storing into the PDP-7 memory on push-jump instructions. In such a case, the high-order bits get set to zeros. This is only in the push-down stack, of course.

GENERAL TECHNICAL SUMMARY

The middle six bits of the twelve-bit PDP-8 buffered memory buffer output are derived as follows. (Bit 3 is shown as typical.)

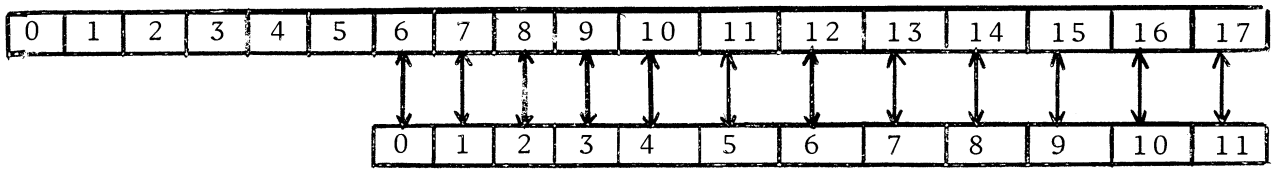


Figure 1. ACCUMULATOR DATA TRANSFER

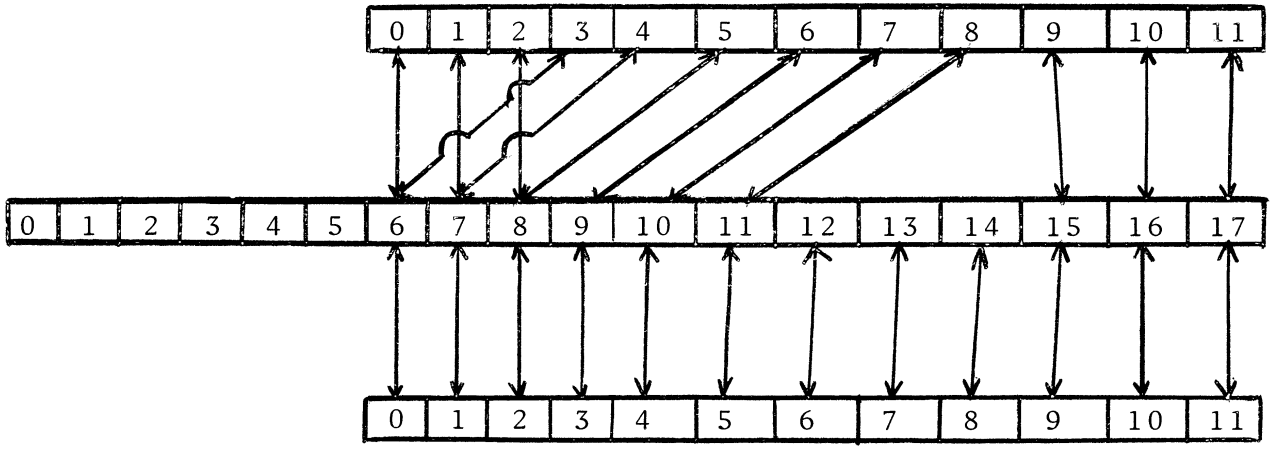


Figure 2. MEMORY BUFFER DATA TRANSFER

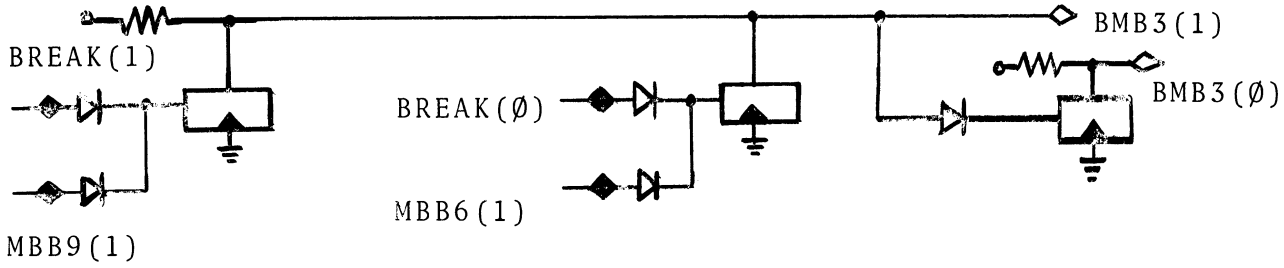


Figure 3. Typical Memory Buffer Bit.

A slight amount of propagation delay is introduced here. The delay is approximately 3x40 nsec = 120 nsec. The time between the loading of the Instruction Register (IR) and the generation of the IOP1 (Input-Output Pulse 1) is 120 nsec minimum. The IR is loaded during T3, which begins 150 nsec after the memory strobe; T3 is 270 nsec long. The setting of the IR should take about 100 nsec. The generation of IOP1 actually takes about 60 to 80 nsec after T5. T5 starts 120 nsec after the end of T3 (or beginning of T4). Thus there is probably about 350 nsec for the worst case of 120 nsec settling. It should be noted that the PDP-7 IOTs are normally generated with different timing than with the PDP-8. The relative times are

	PDP-8	PDP-7
IOP1 to IOP2	1.0 µsec	.450 µsec
IOP2 to IOP4	1.0 µsec	.150 µsec

The difference in timing would not normally cause problems. However, the 338 display control uses IOP2 for an I/O skip instruction. The time required to propagate IOP2, generate the appropriate skip logic, and increment the PDP-7 program counter is longer than 150 nsec. The memory address register of the PDP-7 is set with the contents of the program counter at the

same time that IOP4 is generated. Thus, the skip does not occur at the correct time. To avoid this problem, the Slow Cycle is requested for any such devices. The PDP-7 I/O Slow Cycle has a minimum delay of 1 sec between I/O pulses. Currently the Slow Cycle is forced for all devices, but once the 338 display control can provide its own request, the forced Slow Cycle for all devices can be deleted.

LOGIC DESCRIPTION

The basic problem in the logic was to transform the PDP-7 I/O interface signals to the corresponding PDP-8 I/O interface signals. These are summarized in the Appendix. Accumulator outputs, accumulator inputs, and programmed I/O control signals are all directly compatible signals. The IOP pulses IOP1, IOP2, and IOP4 are all buffered to give cleaner pulses and more driving power. The first IOP pulse, IOP1, is delayed to allow memory buffer and accumulator outputs a chance to settle, since those signals are not buffered and are driving longer lines than usual. It may be wise at some future time to buffer these signals with R650 modules. If this is done, the delay of IOP1 can probably be deleted. The memory address and data input lines to data break have to be complemented. The memory buffer output lines would normally only be complemented, but because of the bit assignments described previously, the middle six bits of the PDP-8 memory buffer output are generated by gating the appropriate PDP-7 MB bits.

The data break control signals basically have the same polarities. Some of the signals expected are not the normal PDP-7 interface signals provided. Thus, one connector has been added to the standard PDP-7 I/O interface connectors to provide these signals. The timing pulses are brought via the high-order PDP-7 data break address lines. When the PDP-7 data break multiplexer is used, the timing pulses are brought

via the same lines as described above, but only on channel zero of the multiplexer. The interface constructed uses two of the multiplexer channels, one for the modified 338 display control and one for the 201A dataphone interface (to be described in a forthcoming report).

Some of the data-break control timing on the PDP-7 is slightly different than that on the PDP-8. Basically, on the PDP-7, Break Request must be dropped after the Address-Accepted pulse. On the PDP-8 the Break Request must be dropped at the beginning of Address Accepted. Besides the difference in basic timing requirements, the PDP-8 Address-Accepted pulse is only 70 nsec long, while the standard PDP-8 pulse is 100 nsec. The PDP-7 does not generate an appropriate Buffered-Break signal. To solve the above problems, a flip-flop which generates the Break signal and gates the memory buffer lines has been added. This flip-flop is set by the PDP-7 Address-Accepted pulse delayed by a W640 pulse amplifier. It is cleared on every PDP-7 clock cycle. The delayed PDP-7 Address-Accepted pulse also generates the corresponding PDP-8 Address-Accepted pulse.

On the following logic diagrams, the connectors on the right-hand side of the drawings correspond to the standard PDP-8 interface connectors. The connectors on the left-hand side of the drawings connect to the appropriate points in the PDP-7.

Logic Diagram 1.1

The low-order 12 bits of the PDP-7 accumulator (buffered) outputs are used to drive the PDP-8 buffered accumulator lines.

The IOP1, IOP2, and IOP4 programmed I/O pulses are buffered in W640 pulse amplifiers (see Logic Diagram 1.7) as are the BT1, BT2A and B Power Clear pulses (see Logic Drawings 1.7 and 1.8).

Logic Diagrams 1.2 and 1.3

The circuits shown develop the PDP-8 buffered memory buffer outputs. Note that the low-order 12 bits of the PDP-7 memory buffer are used. Of those, the low-order three bits and the high-order three bits are simply inverted. The middle six bits, which correspond to the I/O device address during programmed I/O instructions are developed in the circuit shown in Logic Diagram 1.3. Basically, this gate takes the PDP-7 device address when the break cycle is not in effect, and the low-order twelve bits of the PDP-7 memory buffer when the break cycle is in effect. Note that this allows standard PDP-7 programmed I/O programming to be used.

The third connector to the PDP-7 shown in Logic Diagram 1.2 is the connector carrying almost all of the required signals which are not normally provided at the PDP-7 interface and are necessary to generate the required functions at the PDP-8 interface.

Logic Diagram 1.4

The low-order twelve bits of the PDP-7 accumulator are loaded from the PDP-8 accumulator input interface.

The Skip, Interrupt Request, and B Run (1) signals drive the appropriate points in the PDP-7 interface directly. The Clear AC signal is not provided. Note that the functions normally provided by this signal in clearing the accumulator during programmed I/O transfers can be assumed by the programmer of the PDP-7 I/O sequence by microprogramming the Clear AC bit in the IOT instruction. The TT INST and Line (1) signals are associated with the PDP-8 line-adapter interface option and are not supported.

Logic Diagrams 1.5, 1.6, and 1.7 correspond to Logic Diagrams 1.8, 1.9, and 1.10 respectively. These logic diagrams describe that part of the interface involved with the multiplexed data-break facility. If the multiplexer is not used or needed, the circuits shown on Logic Diagrams 1.8, 1.9, and 1.10 may be deleted.

Logic Diagrams 1.5 and 1.8

The circuit shown on this logic diagram develops the necessary logic signals for addressing PDP-7 core addresses during data-break cycle-steals. Note that this interface is currently connected to the Type 173 multiplexer, but may be connected to the corresponding points in the I/O package.

The proper PDP-7 addressing logic is developed by logically inverting the PDP-8 data-address inputs to the interface.

Break Request is inverted and the transfer direction is used to drive the corresponding REQ IN line on the PDP-7. Address Accepted and B Break are generated in Logic Diagrams 1.7 and 1.8. The Increment MB signal is not supported.

Logic Diagrams 1.6 and 1.9

This circuit develops the necessary signals for input of data to the PDP-7 during input data-break cycles. Each of the twelve PDP-8 data-bit inputs are inverted and used to set the low-order twelve bits of the appropriate PDP-7 word.

Cycle Select, Increment CA, and WC Overflow are signals involved in the PDP-8 three-cycle extended data-break facility. This facility is not supported in this interface. Such support would be a logical extension of this interface.

Logic Diagrams 1.7 and 1.10

Address Accepted is delayed slightly and buffered through the W640. The leading edge of the pulse sets the break flip-flop which generates the Buffered Break signal for the PDP-8 side of the interface. The break flip-flop is cleared by PWR CLR (see Logic Diagram 1.12) and BTP6 from the PDP-7. BTP6 is used by the multiplexer for a similar function.

It should be noted that the break flip-flop is required for two reasons. First, the PDP-7 Break (B) is generated at TP6 time of the cycle before the break cycle, while

in the PDP-8, B Break is not logically set until the Address-Accepted pulse starts the data-break cycle. Second, Break (B) in the PDP-7 is logically true for any data break, clock break, or program break.

Logic Diagram 1.11

The two break flip-flops on Diagrams 1.7 and 1.10 are ORed together to provide the gating signal used to gate the memory buffer bits.

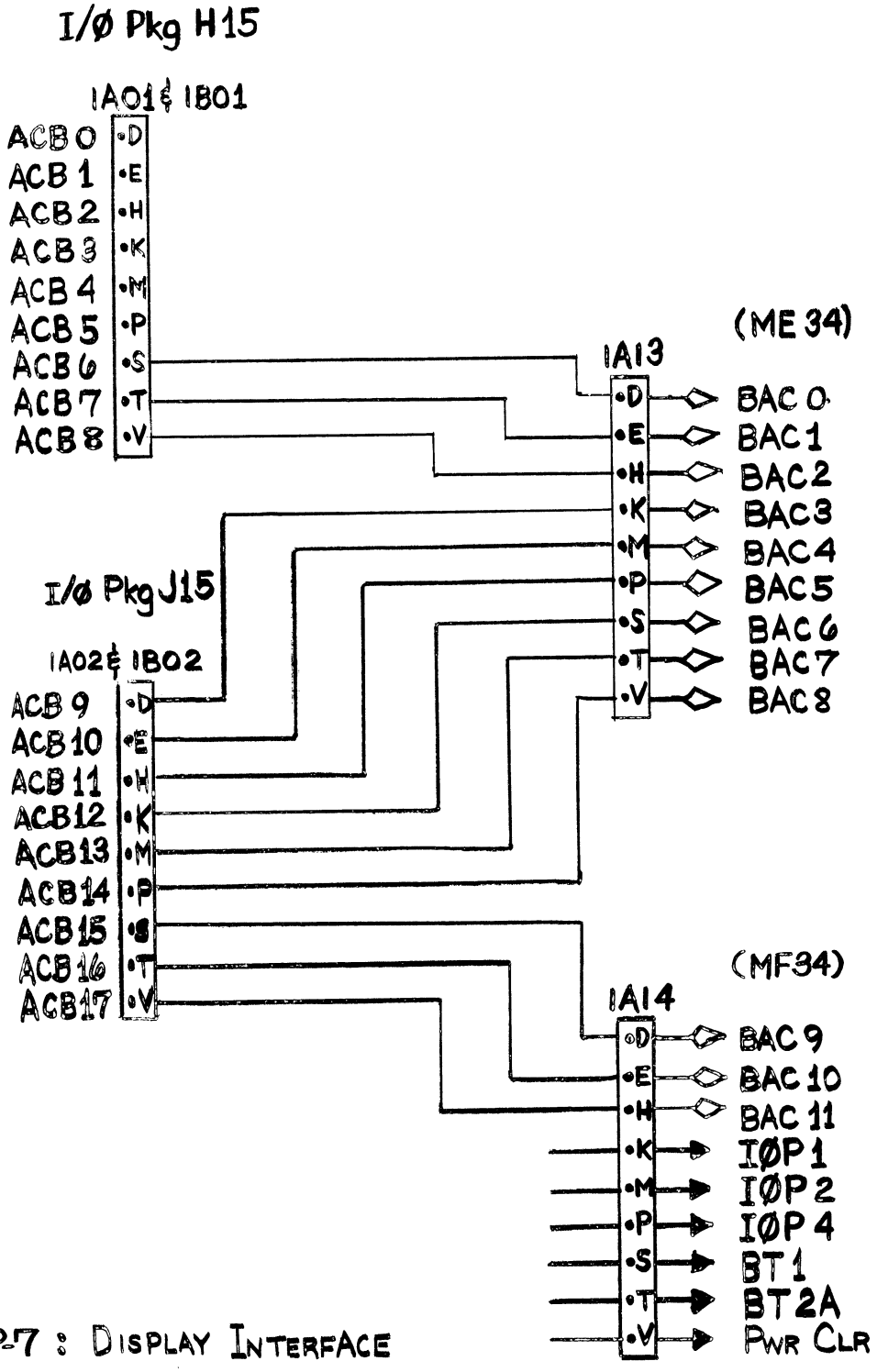
Logic Diagram 1.12

The I/O pulses, IOP1, IOP2, and IOP4 are buffered solely to provide more power to drive cables.

PWR CLR is generated whenever a PDP-7 BEGIN (B) or a PWR CLR NEG signal occurs. Begin (B) is generated whenever the START key is activated. The PWR CLR NEG is generated when the Clear All Flags IOT is executed and during the power-on sequence.

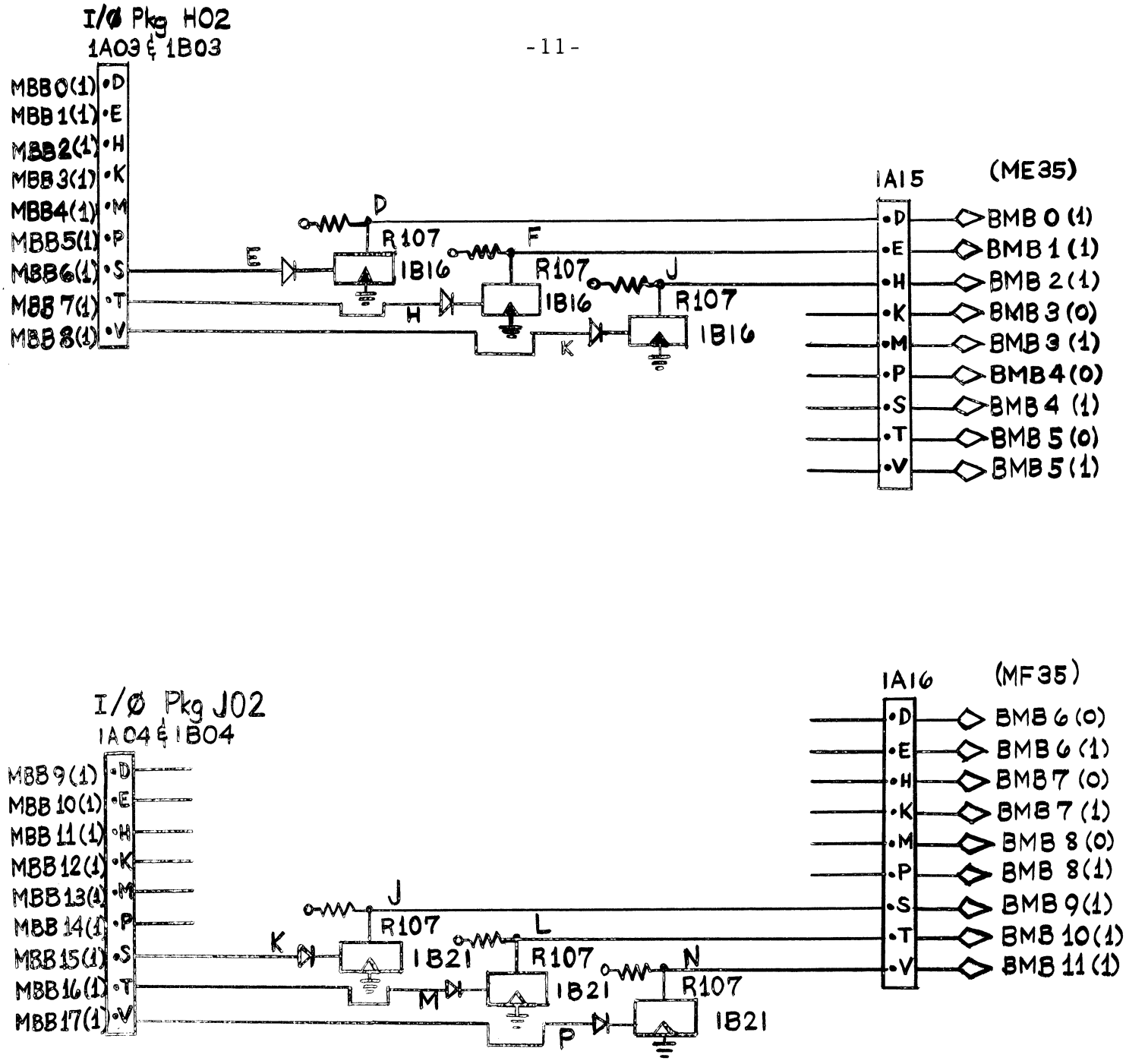
BT1 and BT2, which correspond to core write and core read times in the PDP-8, are generated with the corresponding pulses in the PDP-7, TP6, and TP4 respectively.

Note that IOP1 is delayed to allow the unbuffered signals (BAC, BMB, etc.) to settle before having to decode any IOTs.



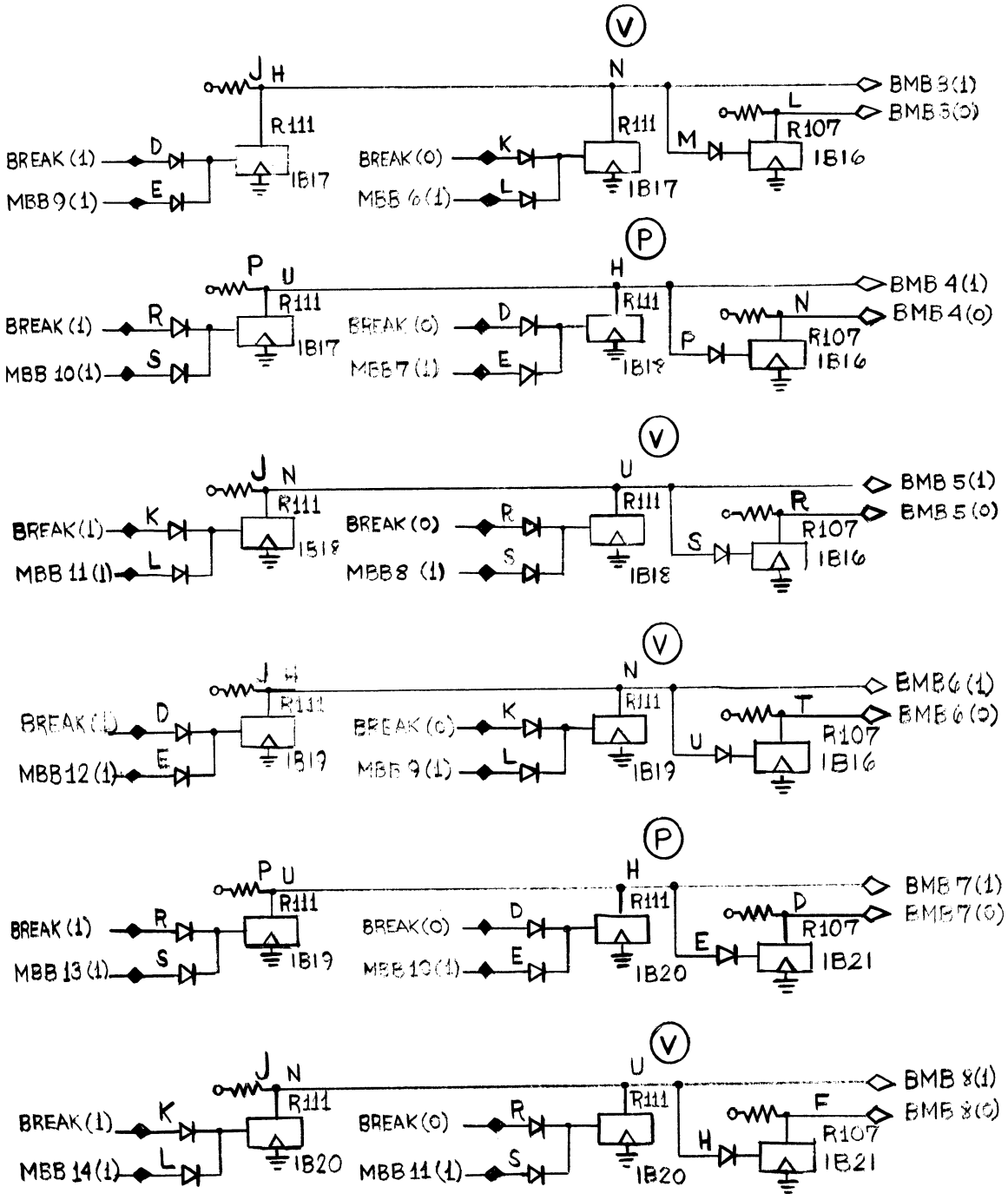
PDP-7 : Display Interface

Logic Diagram 1.1

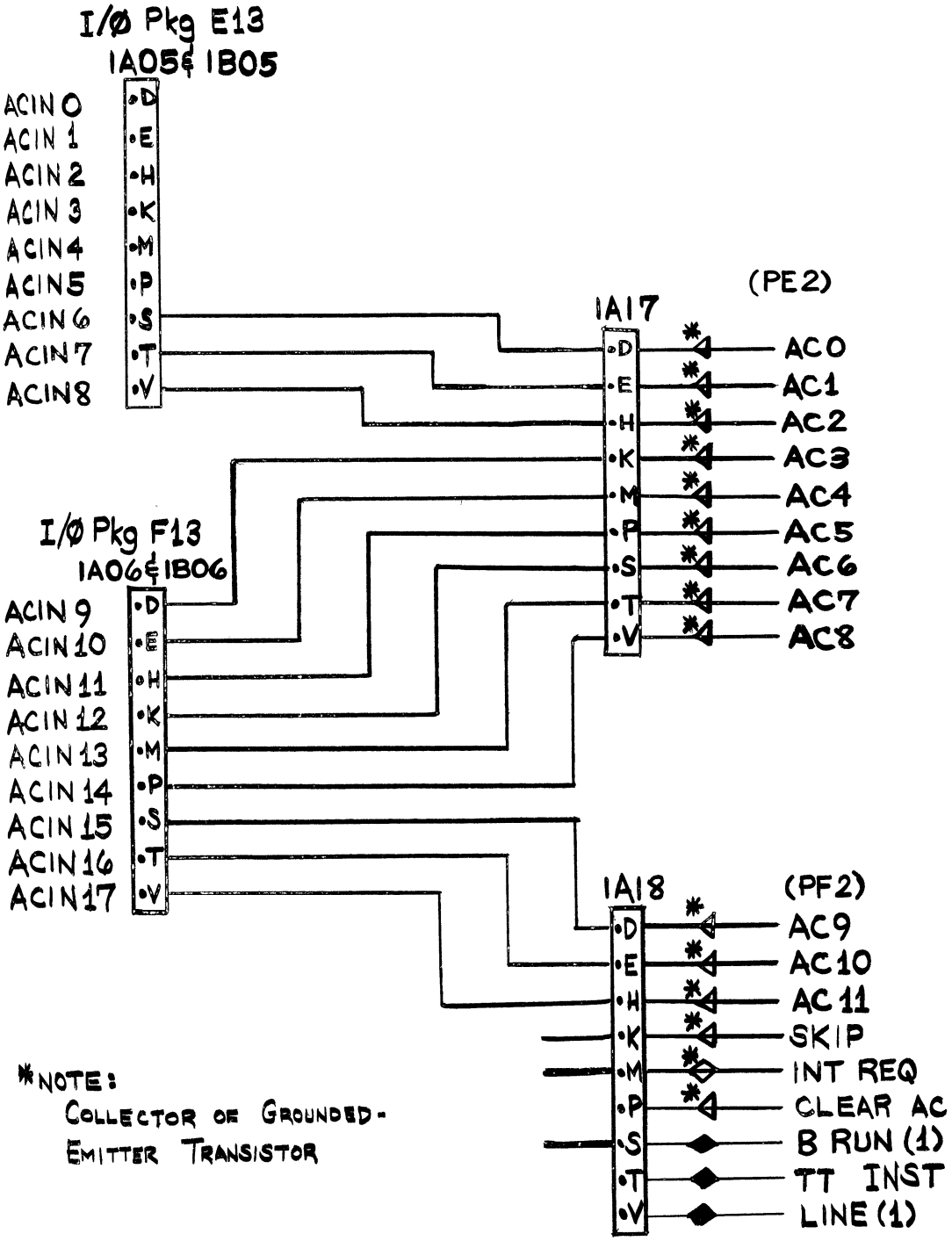


PDP-7: Display Interface

Logic Diagram 1.2

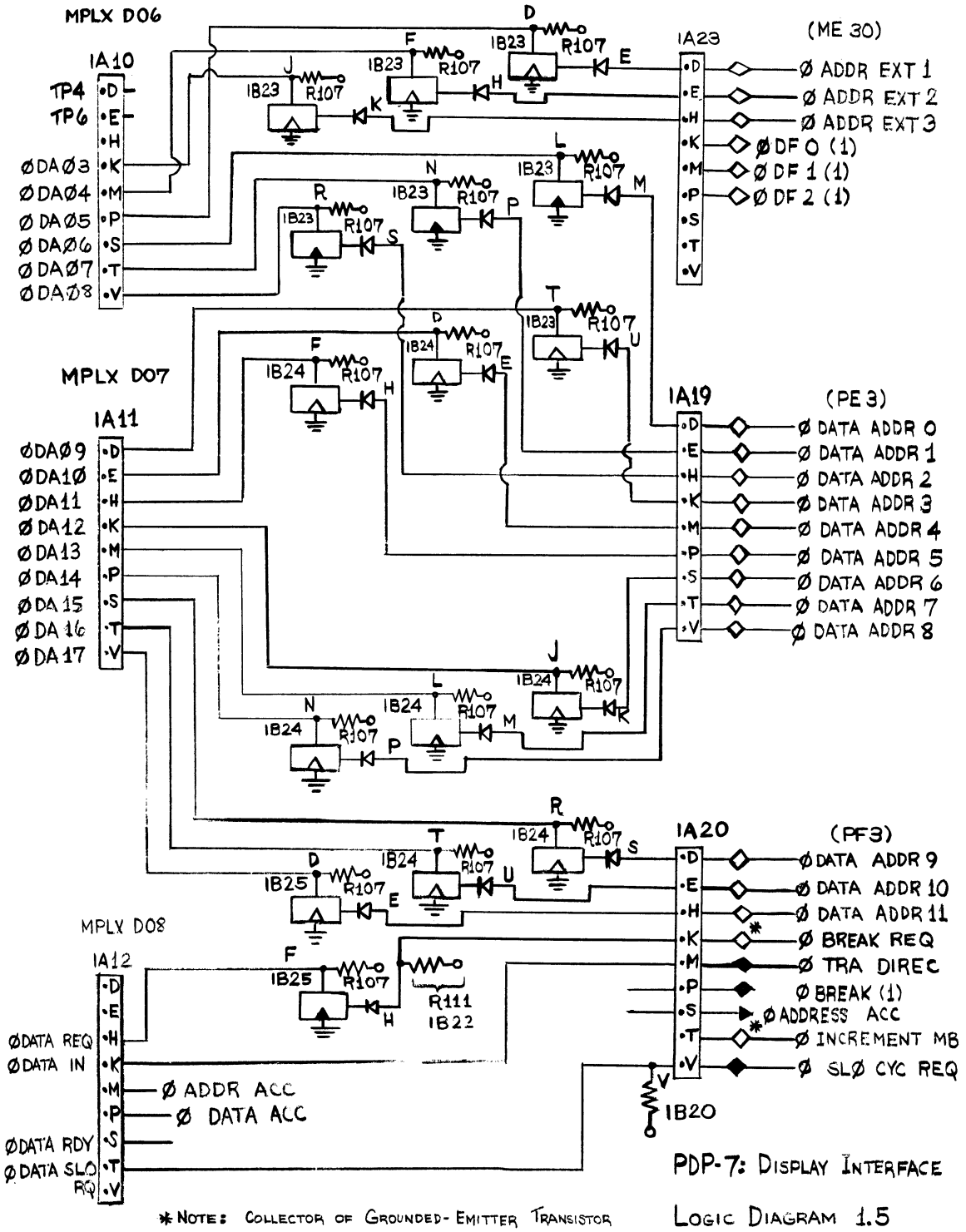


PDP-7: Display Interface
Logic Diagram 1.3



PDP-7: DISPLAY INTERFACE

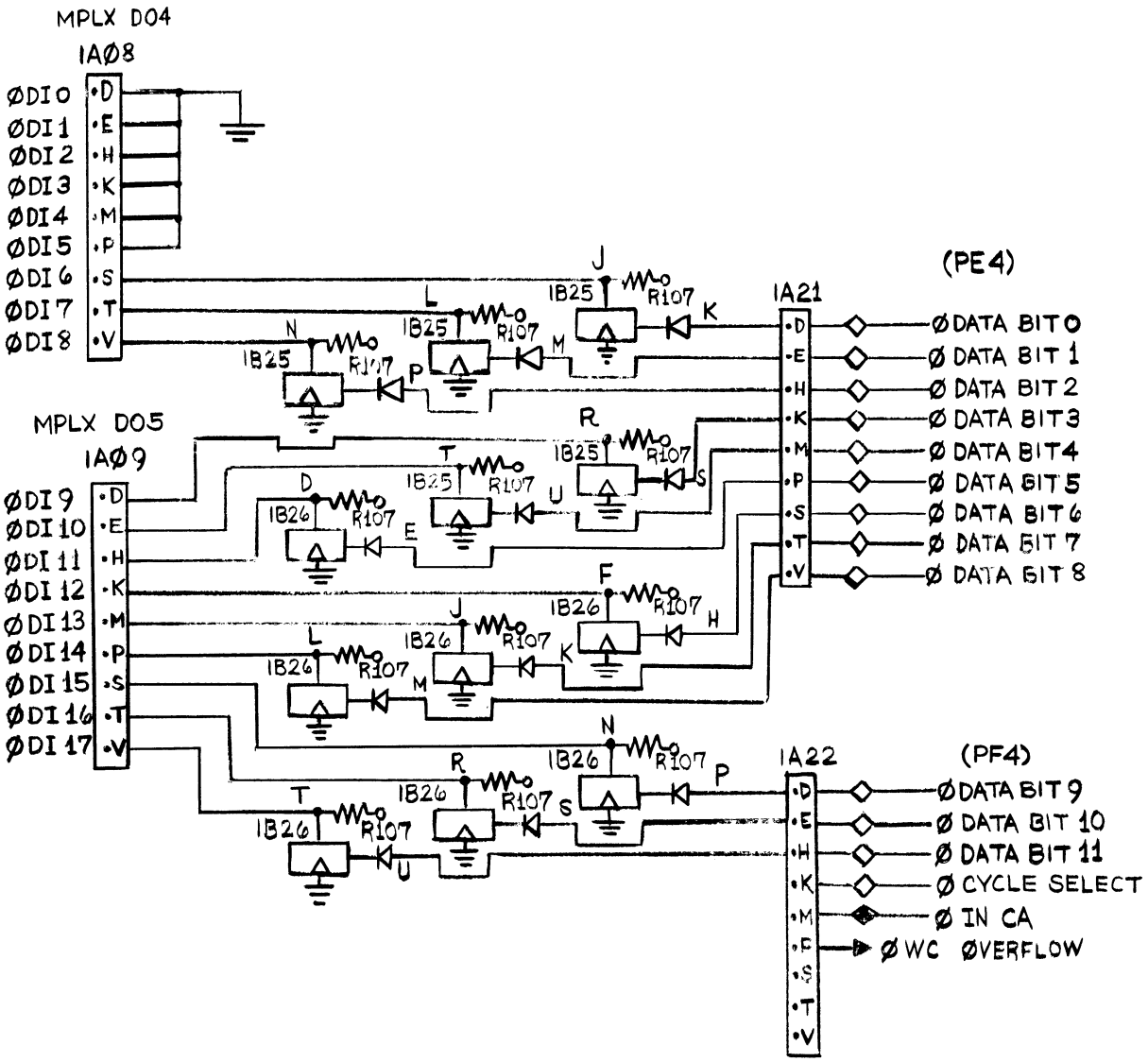
LOGIC DIAGRAM 1.4



PDP-7: Display Interface

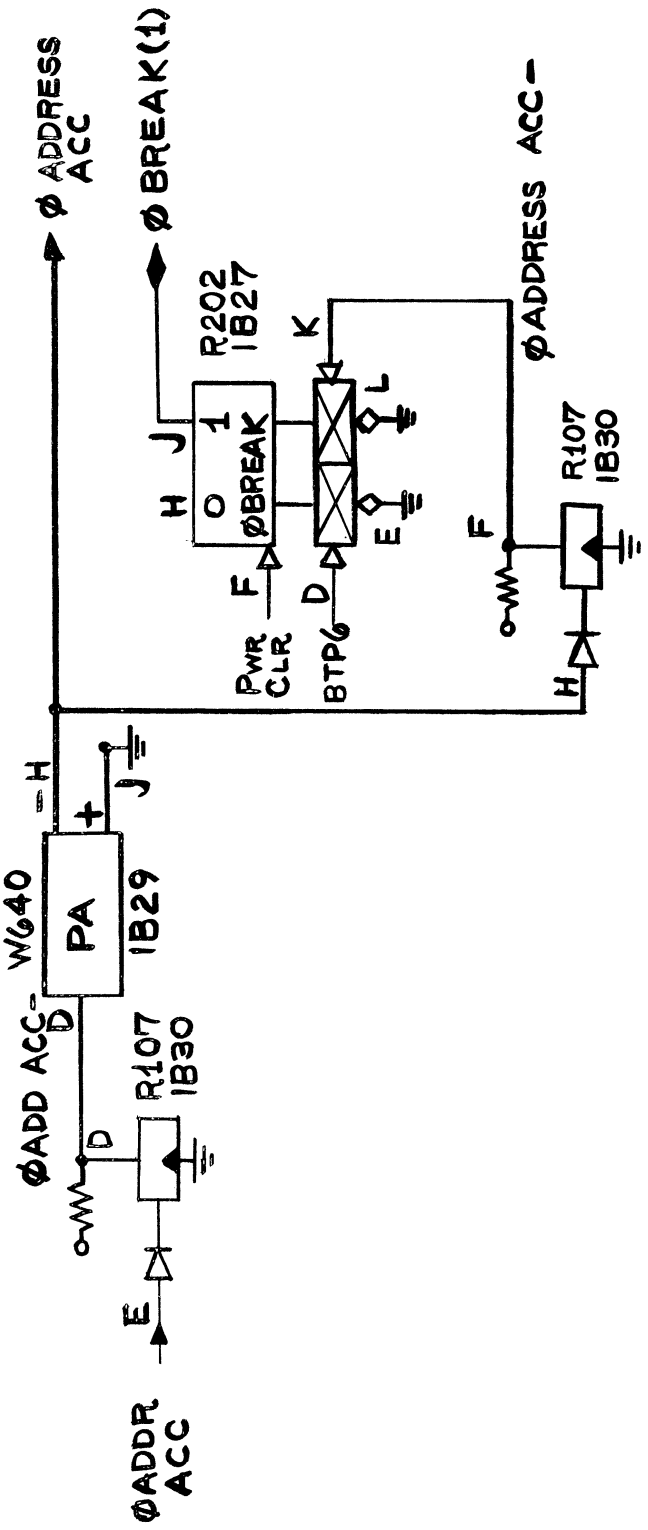
Logic Diagram 1.5

* Note: Collector of Grounded-Emitter Transistor



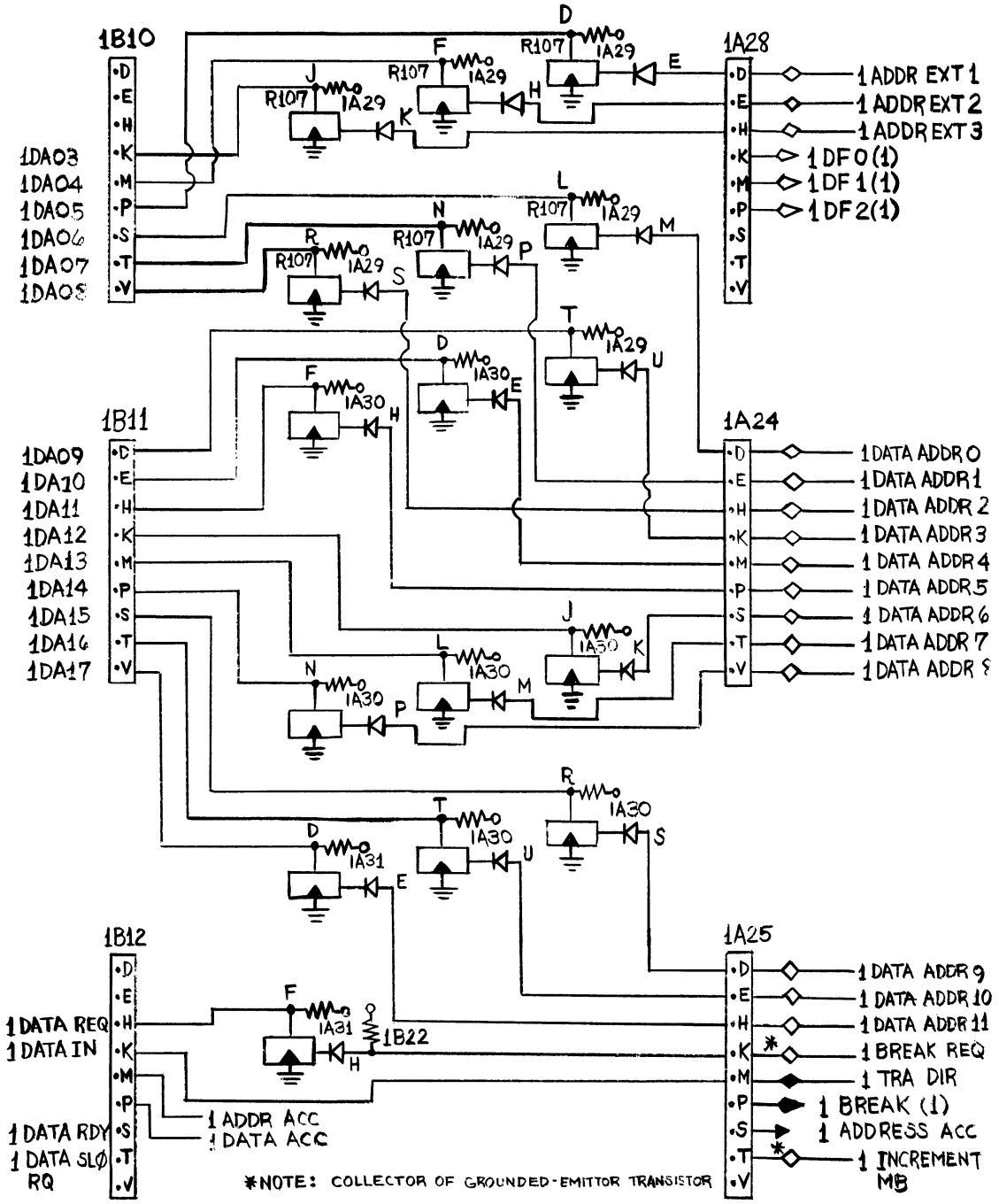
PDP-7: Display Interface

Logic Diagram 1.6



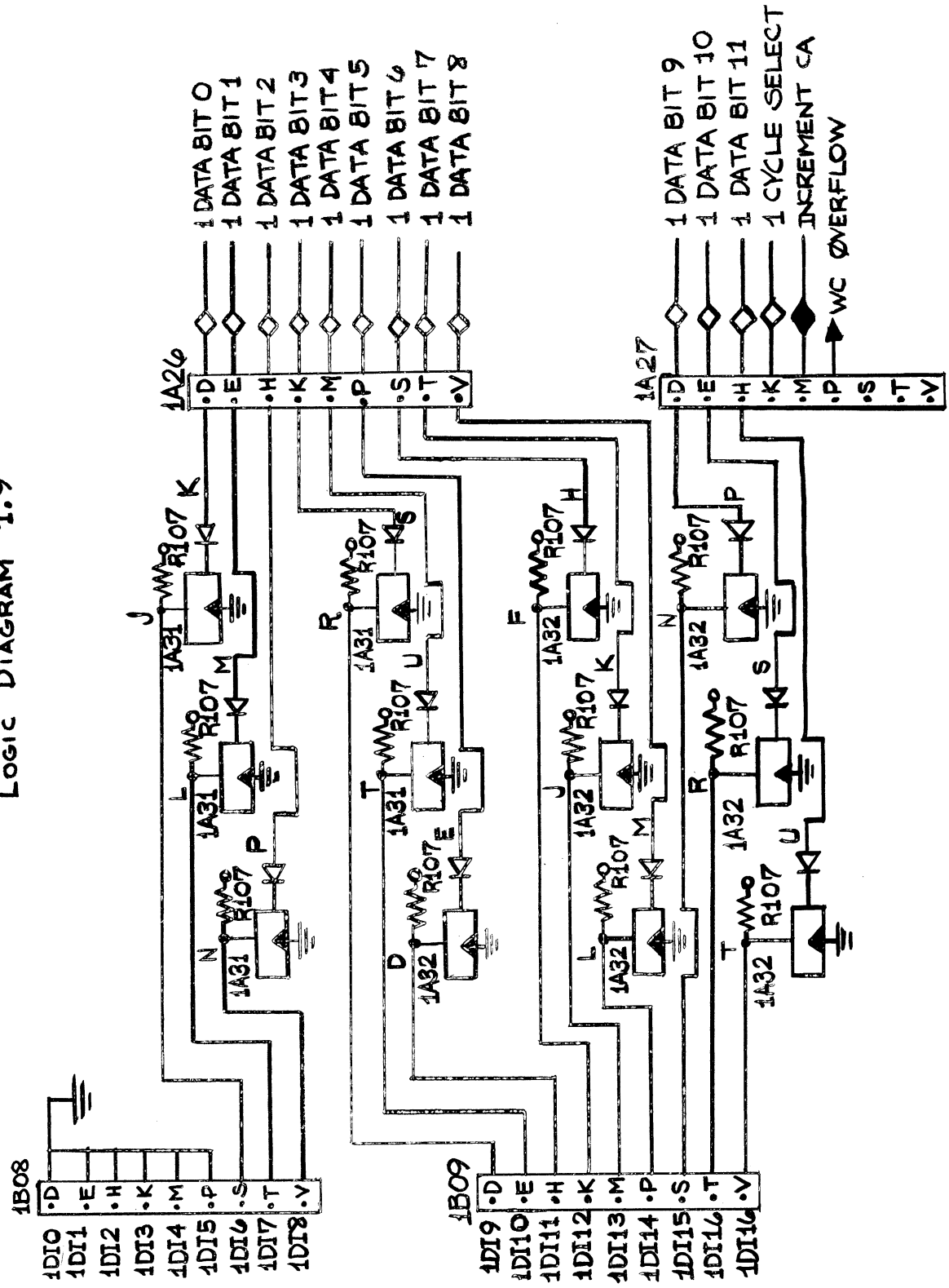
PDP-7: Display Interface

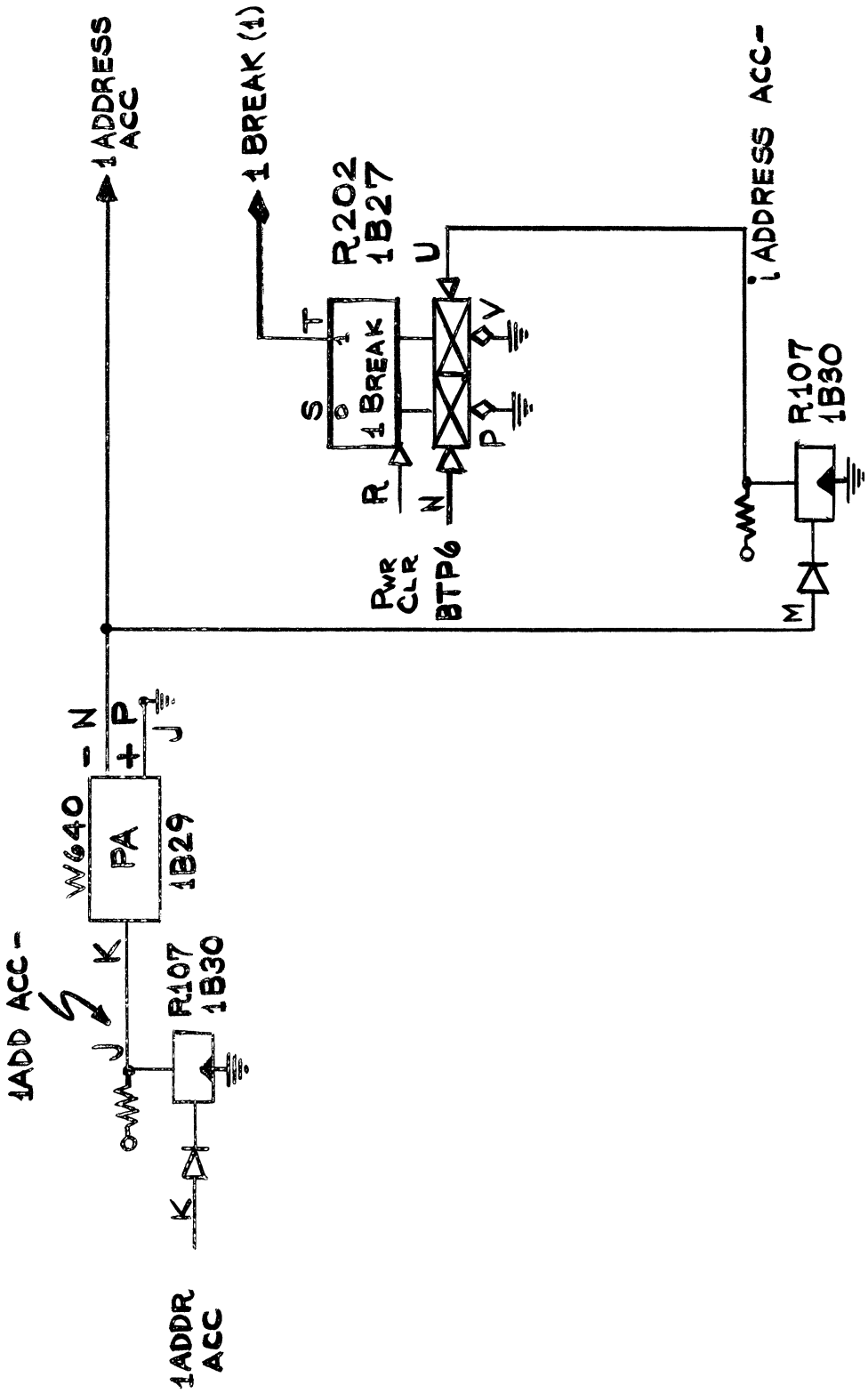
Logic Diagram 1.7



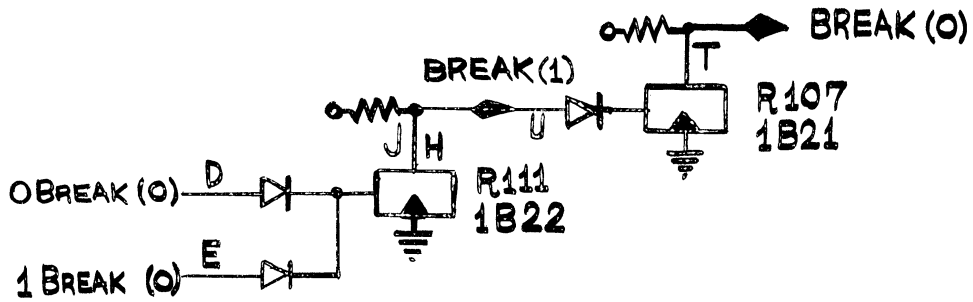
PDP-7: Display Interface
Logic Diagram 1.8

PDP-7: Display Interface
Logic Diagram 1.9

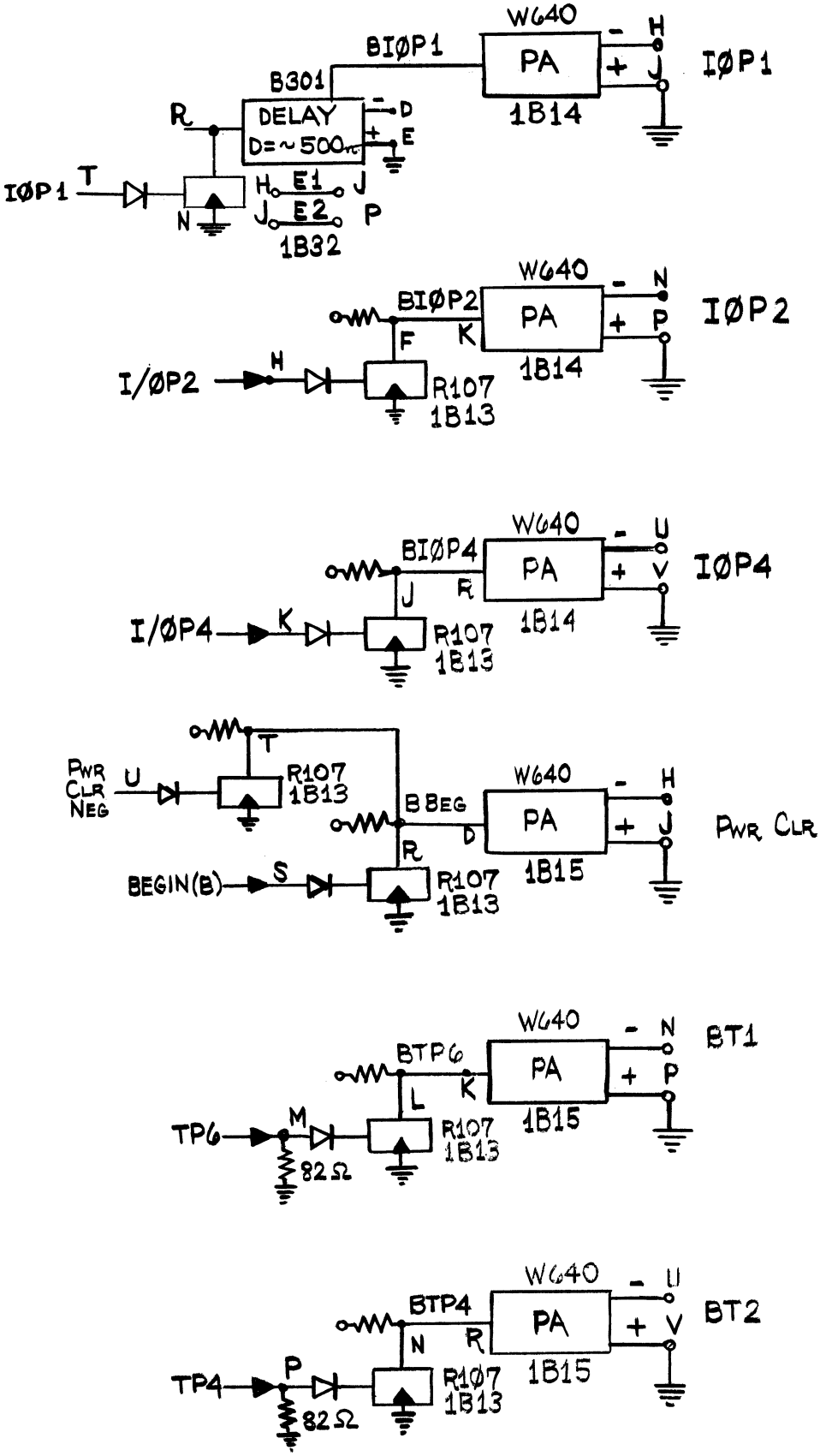




PDP-7: Display Interface
Logic Diagram 1.10



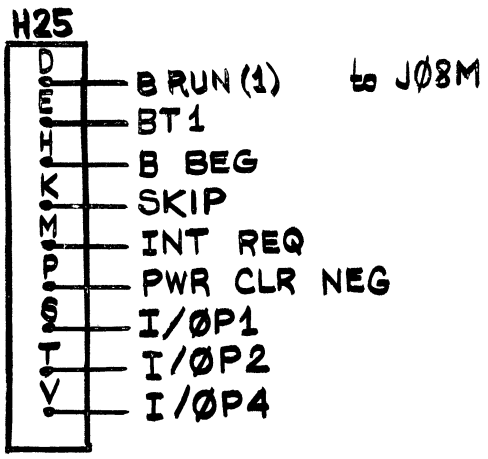
PDP-7: DISPLAY INTERFACE
LOGIC DIAGRAM 1.11



PDP-7: Display Interface
Logic Diagram 1.12

In I/Ø Device

Modify connections to connector slot at H25 to be as follows:



In addition:

ADD	J06K-H32D	TP4
ADD	J06P-H32E	TP6

In Type 173 Multiplexor

ADD	B01D - D06D	TP4
ADD	B01E - D06E	TP6

MODULE LAYOUT

(page 1 of 3)

	1	2	3	4	5	6	7	8	9	10	11
	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21
A	PDP-7 ACC OUT Ø-8 to H15	PDP-7 ACC OUT 9-17 to J15	PDP-7 MBB Ø-8 to HØ2	PDP-7 MBB 9-17 to JØ2	PDP-7 ACC IN Ø-8 to E13	PDP-7 ACC IN 9-17 to F13	MISC I/O SIGNALS ↓	PDP-7 DATA IN Ø-8 CHØ to MLPX DØ4	PDP-7 DATA IN 9-17 CHØ to MLPX DØ5	PDP-7 DATA ADD Ø-8 CHØ to MLPX DØ6	PDP-7 DATA ADD 9-17 CHØ to MLPX DØ7
	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21		WØ21	WØ21	WØ21	WØ21
B	PDP-7 ACC OUT Ø-8	PDP-7 ACC OUT 9-17	PDP-7 MBB Ø-8	PDP-7 MBB 9-17	PDP-7 ACC IN Ø-8	PDP-7 ACC IN 9-17	↓	PDP-7 DATA IN Ø-8 CH1 to	PDP-7 DATA IN 9-17 CH1 to	PDP-7 DATA ADD Ø-8 CH1 to	PDP-7 DATA ADD 9-17 CH1 to

MODULE LAYOUT

(page 2 of 3)

	12	13	14	15	16	17	18	19	2Ø	21	22
	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21	WØ21
		1	2	3	4	5	6	7	8	9	1Ø
	PDP-7										
	DATA	PDP-8	PDP-8	PDP-8	PDP-8	PDP-8	PDP-8	PDP-8	PDP-8	PDP-8	PDP-8
	BRK	BAC	BAC	BMB	BMB	AC	AC	DATA	DATA	DATA	DATA
	CNTL	Ø-8	9-11	Ø-5	6-11	Ø-8	9-11	ADD	ADD	BIT	BIT
	CHØ	OUT	OUT	OUT	OUT	IN	IN	Ø-8	9-11	Ø-8	9-11
A			IOPs					IN	IN	IN	IN
									ADD ACC		
	to										
	MLPX										
	DØ8							CHØ	CHØ	CHØ	CHØ
	WØ21	R1Ø7	W64Ø	W64Ø	R1Ø7	R111	R111	R111	R111	R1Ø7	R111
		BIOP1			BMBØ	BMB3 BMB4	BMB5	BMB6 BMB7	BMB8	BMB7	BREAK(Ø) ØBREAK REQ 1BREAK REQ
	PDP-7 DATA	BIOP2	IOP1	PWR CLR	BMB1				SLO CYC REQ	BMB8	
	BRK CNTL	BIOP4			BMB2	BMB3	BMB4	BMB6	BMB7	BMB9	BREAK(Ø)
	CH1	BTP6	IOP2	BT1	BMB3					BMB1Ø	
B	to	BTP4			BMB4	BMB3	BMB5	BMB6	BMB8	BMB11	
		BBEG			BMB5					BREAK	
			IOP4	BT2	BMB6	BMB4	BMB5	BMB7	BMB8	BREAK(1)	

MODULE LAYOUT

(page 3 of 3)

	23	24	25	26	27	28	29	30	31	32
A	WØ21 11 PDP-8 ADD EXT 1,2,3 CHØ	WØ21 7 PDP-8 DATA ADD Ø-8 IN CH1	WØ21 8 PDP-8 DATA ADD 9-11 IN ADD ACC CH1	WØ21 9 PDP-8 DATA BIT Ø-8 IN CH1	WØ21 1Ø PDP-8 DATA BIT 9-11 IN CH1	WØ21 11 PDP-8 ADD EXT 1,2,3 CH1	R1Ø7 1DAØ5 1DAØ4 1DAØ3 1DAØ6 1DAØ7 1DAØ8 1DAØ9	R1Ø7 1DA1Ø 1DA11 1DA12 1DA13 1DA14 1DA15 1DA16	R1Ø7 1DA17 1DATA REQ 1DI6 1DI7 1DI8 1DI9 1DI1Ø	R1Ø7 1DI11 1DI12 1DI13 1DI14 1DI15 1DI16 1DI17
B	R1Ø7 ØDAØ5 ØDAØ4 ØDAØ3 ØDAØ6 ØDAØ7 ØDAØ8 ØDAØ9	R1Ø7 ØDA1Ø ØDA11 ØDA12 ØDA13 ØDA14 ØDA15 ØDA16	R1Ø7 ØDA17 ØDATA REQ ØDI6 ØDI7 ØDI8 ØDI9 ØDI1Ø	R1Ø7 ØDI11 ØDI12 ØDI13 ØDI14 ØDI15 ØDI16 ØDI17	R2Ø2 ØBREAK 1BREAK		W64Ø ØADDRESS ACC 1ADDRESS ACC	R1Ø7 ØADDACC ØADDRESS ACC 1ADD ACC 1ADDRESS ACC		B3Ø1 BIOP1

APPENDIX

INTERFACE LOGIC SIGNALS
PDP-7A AND PDP-8

References:

- PDP-7 Interface and Installation Manual
- PDP-7A Logic Diagrams
- PDP-8 Interface and Installation Manual

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
E13S	EIC6	→ *	→ *	AC0	PE2D
E13T	EIC7	→ *	→ *	AC1	PE2E
E13V	EIC8	→ *	→ *	AC2	PE2H
F13D	EIC9	→ *	→ *	AC3	PE2K
F13E	EIC10	→ *	→ *	AC4	PE2M
F13H	EIC11	→ *	→ *	AC5	PE2P
F13K	EIC12	→ *	→ *	AC6	PE2S
F13M	EIC13	→ *	→ *	AC7	PE2T
F13P	EIC14	→ *	→ *	AC8	PE2V
F13S	EIC15	→ *	→ *	AC9	PF2D
F13T	EIC16	→ *	→ *	AC10	PF2E
F13V	EIC17	→ *	→ *	AC11	PF2H

(In PDP-7A I/O Device)

ACCUMULATOR INPUTS

*Note: Collector of Grounded-Emitter Transistor

November 1967

To Whom It May Concern:

The attached pages 28 to 34 are corrected pages, superseding those of the same number in the Concomp Memorandum, Engineering Design Report: PDP-7/Modified 338 Display Interface, by Stephen F. Lundstrom, August 1967.

Concomp Project: Research in
Conversational Use of Computers
231 West Engineering Building
Ann Arbor, Michigan 48104

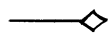
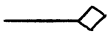
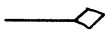
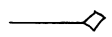
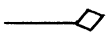
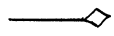
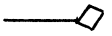
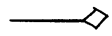
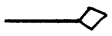
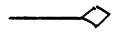
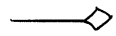
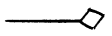
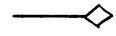
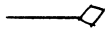
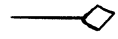
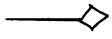
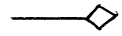
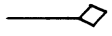
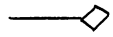
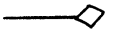
PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
E13S	EIC6	→ *	→ *	AC0	PE2D
E13T	EIC7	→ *	→ *	AC1	PE2E
E13V	EIC8	→ *	→ *	AC2	PE2H
F13D	EIC9	→ *	→ *	AC3	PE2K
F13E	EIC10	→ *	→ *	AC4	PE2M
F13H	EIC11	→ *	→ *	AC5	PE2P
F13K	EIC12	→ *	→ *	AC6	PE2S
F13M	EIC13	→ *	→ *	AC7	PE2T
F13P	EIC14	→ *	→ *	AC8	PE2V
F13S	EIC15	→ *	→ *	AC9	PF2D
F13T	EIC16	→ *	→ *	AC10	PF2E
F13V	EIC17	→ *	→ *	AC11	PF2H

(In PDP-7A I/O Device)

ACCUMULATOR INPUTS

Corrected page 28. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

*Note: Collector of Grounded-Emitter Transistor

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
H15S	ACB6			BAC0	ME34D
H15T	ACB7			BAC1	ME34E
H15V	ACB8			BAC2	ME34H
J15D	ACB9			BAC3	ME34K
J15E	ACB10			BAC4	ME34M
J15H	ACB11			BAC5	ME34P
J15K	ACB12			BAC6	ME34S
J15M	ACB13			BAC7	ME34T
J15P	ACB14			BAC8	ME34V
J15S	ACB15			BAC9	MF34D
J15T	ACB16			BAC10	MF34E
J15V	ACB17			BAC11	MF34H

(In PDP-7A I/O Device)

ACCUMULATOR OUTPUTS

Corrected page 29. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
*2 D27E	PROGRAM INTERRUPT REQUEST	*1	*1	INTERRUPT REQUEST	PF2M
*2 D30D	I/O SKIP	*1	*1	SKIP	PF2K
*2 J08D	I/O P1			IOP1	MF34K
*2 J08E	I/O P2			IOP2	MF34M
*2 J08H	I/O P4			IOP4	MF34P

(In PDP-7A I/O Device)

PROGRAMMED INPUT-OUTPUT SLOW CYCLE CONTROL

Corrected page 30. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

*Note 1: Collector of Grounded-Emitter Transistor

*Note 2: These points not available on normal PDP-7A I/O Interface

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
D06K	ADDR-BIT 03			ADDR EXT 3	ME30H
D06M	ADDR-BIT 04			ADDR EXT 2	ME30E
D06P	ADDR-BIT 05			ADDR EXT 1	ME30D
D06S	ADDR-BIT 06			DATA ADDR 0	PE3D
D06T	ADDR-BIT 07			DATA ADDR 1	PE3E
D06V	ADDR-BIT 08			DATA ADDR 2	PE3H
D07D	ADDR-BIT 09			DATA ADDR 3	PE3K
D07E	ADDR-BIT 10			DATA ADDR 4	PE3M
D07H	ADDR-BIT 11			DATA ADDR 5	PE3P
D07K	ADDR-BIT 12			DATA ADDR 6	PE3S
D07M	ADDR-BIT 13			DATA ADDR 7	PE3T
D07P	ADDR-BIT 14			DATA ADDR 8	PE3V
D07S	ADDR-BIT 15			DATA ADDR 9	PF3D
D07T	ADDR-BIT 16			DATA ADDR 10	PF3E
D07V	ADDR-BIT 17			DATA ADDR 11	PF3H

(CHO-TYPE 173 MULTIPLEXER)

DATA BREAK ADDRESS LINES

Corrected page 31. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
D04S	DATA-BIT 06			DATA-BIT 0	PE4D
D04T	DATA-BIT 07			DATA-BIT 1	PE4E
D04V	DATA-BIT 08			DATA-BIT 2	PE4H
D05D	DATA-BIT 09			DATA-BIT 3	PE4K
D05E	DATA-BIT 10			DATA-BIT 4	PE4M
D05H	DATA-BIT 11			DATA-BIT 5	PE4P
D05K	DATA-BIT 12			DATA-BIT 6	PE4S
D05M	DATA-BIT 13			DATA-BIT 7	PE4T
D05P	DATA-BIT 14			DATA-BIT 8	PE4V
D05S	DATA-BIT 15			DATA-BIT 9	PF4D
D05T	DATA-BIT 16			DATA-BIT 10	PF4E
D05V	DATA-BIT 17			DATA-BIT 11	PF4H

(CHO-TYPE 173 MULTIPLEXER)

DATA BREAK INPUT LINES

Corrected page 32. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
H02S	MBB6(1)			BMB0(1)	ME35D
H02T	MBB7(1)			BMB2(1)	ME35E
H02V	MBB8(1)			BMB2(1)	ME35F
H02S	MBB6(1)			BMB3(0)	ME35K
	or				
J02D	MBB9(1)			BMB3(1)	ME35M
H02T	MBB7(1)			BMB4(0)	ME35P
	or				
J02E	MBB10(1)			BMB4(1)	ME35S
H02V	MBB8(1)			BMB5(0)	ME35T
	or				
J02H	MBB11(1)			BMB5(1)	ME35V
J02D	MBB9(1)			BMB6(0)	MF35D
	or				
J02K	MBB12(1)			BMB6(1)	MF35E
J02E	MBB10(1)			BMB7(0)	MF35H
	or				
J02M	MBB13(1)			BMB7(1)	MF35K
J02H	MBB11(1)			BMB8(0)	MF35M
	or				
J02P	MBB14(1)			BMB8(1)	MF35P
J02S	MBB15(1)			BMB9(1)	MF35S
J02T	MBB16(1)			BMB10(1)	MF35T
J02V	MBB17(1)			BMB11(1)	MF35V

(In PDP-7A I/O Device)

DATA BREAK OUTPUT LINES

Corrected page 33. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
*3 D08H	DATA RQ		*1	BREAK REQUEST	PF3K
*3 D08K	RQ IN	(IN)	(IN)	TRANSFER DIRECTION	PF3M
*2 AØ7P	BREAK(B)			B BREAK	PF3P
*3 D08M	ADDR ACC			ADDRESS ACCEPTED	PF3S
*4 A10D	TP6			BT1	MF34S
*4 A10E	TP4			BT2A	MF34T
*2 C13H	NEG PWR CLR BEGIN (B)			B POWER CLEAR	MF34V
*2 J08M	RUN(1) B			B RUN	PF2S

DATA BREAK CONTROL SIGNALS

Corrected page 34. Stephen F. Lundstrom, Engineering Design Report: PDP-7/Modified 338 Display Interface, Concomp Memorandum, The University of Michigan, August 1967. Corrected November 1967.

*Note 1: Collector of a Grounded-Emitter Transistor

*Note 2: This point not available at normal PDP-7A Interface. Obtained from PDP-7A I/O Device Address given.

*Note 3: CHO-Type 173 Multiplexer Addresses.

*Note 4: Obtained from I/O Device via Type 173 Multiplexer.

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
H15S	ACB6	→	→	BAC0	ME34D
H15T	ACB7	→	→	BAC1	ME34E
H15V	ACB8	→	→	BAC2	ME34H
J15D	ACB9	→	→	BAC3	ME34K
J15E	ACB10	→	→	BAC4	ME34M
J15H	ACB11	→	→	BAC5	ME34P
J15K	ACB12	→	→	BAC6	ME34S
J15M	ACB13	→	→	BAC7	ME34T
J15P	ACB14	→	→	BAC8	ME34V
J15S	ACB15	→	→	BAC9	MF34D
J15T	ACB16	→	→	BAC10	MF34E
J15V	ACB17	→	→	BAC11	MF34H

(In PDP-7A I/O Device)

ACCUMULATOR OUTPUTS

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
D27E *2	PROGRAM INTERRUPT REQUEST	*1	*1	INTERRUPT REQUEST	PF2M
D30D *2	I/O SKIP	*1	*1	SKIP	PF2K
J08D *2	I/O P1			IOP1	MF34K
J08E *2	I/O P2			IOP2	MF34M
J08H *2	I/O P4			IOP4	MF34P
(In PDP-7A I/O Device)					

PROGRAMMED INPUT-OUTPUT SLOW CYCLE CONTROL

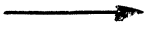
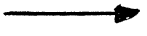
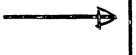
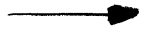
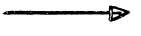
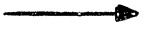
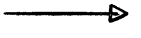
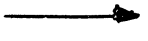
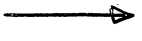
*Note 1: Collector of Grounded-Emitter Transistor

*Note 2: These points not available on normal PDP-7A I/O Interface

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
D06K	ADDR-BIT 03			ADDR EXT 3	ME30H
D06M	ADDR-BIT 04			ADDR EXT 2	ME30E
D06P	ADDR-BIT 05			ADDR EXT 1	ME30D
D06S	ADDR-BIT 06			DATA ADDR 0	PE3D
D06T	ADDR-BIT 07			DATA ADDR 1	PE3E
D06V	ADDR-BIT 08			DATA ADDR 2	PE3H
D07D	ADDR-BIT 09			DATA ADDR 3	PE3K
D07E	ADDR-BIT 10			DATA ADDR 4	PE3M
D07H	ADDR-BIT 11			DATA ADDR 5	PE3P
D07K	ADDR-BIT 12			DATA ADDR 6	PE3S
D07M	ADDR-BIT 13			DATA ADDR 7	PE3T
D07P	ADDR-BIT 14			DATA ADDR 8	PE3V
D07S	ADDR-BIT 15			DATA ADDR 9	PF3D
D07T	ADDR-BIT 16			DATA ADDR 10	PF3E
D07V	ADDR-BIT 17			DATA ADDR 11	PF3H

(CHO-TYPE 173 MULTIPLEXER)

DATA BREAK ADDRESS LINES

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
D04S	DATA-BIT 06			DATA-BIT 0	PE4D
D04T	DATA-BIT 07			DATA-BIT 1	PE4E
D04V	DATA-BIT 08			DATA-BIT 2	PE4H
D05D	DATA-BIT 09			DATA-BIT 3	PE4K
D05E	DATA-BIT 10			DATA-BIT 4	PE4M
D05H	DATA-BIT 11			DATA-BIT 5	PE4P
D05K	DATA-BIT 12			DATA-BIT 6	PE4S
D05M	DATA-BIT 13			DATA-BIT 7	PE4T
D05P	DATA-BIT 14			DATA-BIT 8	PE4V
D05S	DATA-BIT 15			DATA-BIT 9	PF4D
D05T	DATA-BIT 16			DATA-BIT 10	PF4E
D05V	DATA-BIT 17			DATA-BIT 11	PF4H

(CHO-TYPE 173 MULTIPLEXER)

DATA BREAK INPUT LINES

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
H02S	MBB6(1)			BMB0(1)	ME35D
H02T	MBB7(1)			BMB2(1)	ME35E
H02V	MBB8(1)			BMB2(1)	ME35F
H02S	MBB6(1)			BMB3(0)	ME35K
	or				
J02D	MBB9(1)			BMB3(1)	ME35M
H02T	MBB7(1)			BMB4(0)	ME35P
	or				
J02E	MBB10(1)			BMB4(1)	ME35S
H02V	MBB8(1)			BMB5(0)	ME35T
	or				
J02H	MBB11(1)			BMB5(1)	ME35V
J02D	MBB9(1)			BMB6(0)	MF35D
	or				
J02K	MBB12(1)			BMB6(1)	MF35E
J02E	MBB10(1)			BMB7(0)	MF35H
	or				
J02M	MBB13(1)			BMB7(1)	MF35K
J02H	MBB11(1)			BMB8(0)	MF35M
	or				
J02P	MBB14(1)			BMB8(1)	MF35P
J02S	MBB15(1)			BMB9(1)	MF35S
J02T	MBB16(1)			BMB10(1)	MF35T
J02V	MBB17(1)			BMB11(1)	MF35V

(In PDP-7A I/O Device)

DATA BREAK OUTPUT LINES

PDP-7A			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
*3 D08H	DATA RQ	→	*1 →	BREAK REQUEST	PF3K
*3 D08K	RQ IN	→ (IN)	→ (IN)	TRANSFER DIRECTION	PF3M
*2 AØ7P	BREAK(B)	→	→	B BREAK	PF3P
*3 D08M	ADDR ACC	→	→	ADDRESS ACCEPTED	PF3S
*4 A10D	TP6	→	→	BT1	MF34S
*4 A10E	TP4	→	→	BT2A	MF34T
*2 C13H	NEG PWR CLR BEGIN (B)	→	→	B POWER CLEAR	MF34V
*2 J08M	RUN(1) B	→	→	B RUN	PF2S

DATA BREAK CONTROL SIGNALS

*Note 1: Collector of a Grounded-Emitter Transistor.

*Note 2: This point not available at normal PDP-7A Interface. Obtained from PDP-7A I/O Device Address given.

*Note 3: CHO-Type 173 Multiplexer Addresses.

*Note 4: Obtained from I/O Device via Type 173 Multiplexer.