Nano-structured InGaN Light-Emitting Diodes

for Solid-State Lighting

by

Taeil Jung

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Doctoral Committee:

Assistant Professor P. C. Ku, Chair
Professor Pallab K. Bhattacharya
Professor Rachel S. Goldman
Associate Professor L. Jay Guo

To my wife, son, and daughter
for their love and support

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Looking back at the long journey toward this point in my academic career, I am indebted to many people for their help. Although there are too many people to list, I feel that there are some people who must be mentioned by name.

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LIST OF ABBREVIATIONS

2D	2 Dimensional
3D	3 Dimensional
AFM	Atomic Force Microscopy
BHF	Buffered Hydro-Fluoric acid
CCD	Charge-Coupled Device
Cp_2Mg	Bis-cyclopentadienyl Magnesium
CRI	Color Rendering Index
CW	Continuous-Wave
EDX	Energy Dispersive X-ray spectroscopy
EELS	Electron Energy Loss Spectroscopy
EL	Electroluminescence
ELOG	Epitaxial Lateral Over-Growth
FF	Fill Factor
FWHM	Full Width Half Maximum
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HT	High Temperature
HTO	High Temperature Overgrowth
HVPE	Hydride Vapor Phase Epitaxy
IEF	Internal Electric Field
InGaN	Indium Gallium Nitride

IQE	Internal Quantum Efficiency
ISST	*In Situ* Silane Treatment
LED	Light-Emitting Diode
LEEBI	Low Energy Electron Beam Irradiation
LT	Low Temperature
MBE	Molecular Beam Epitaxy
MOCVD	Metal-Organic Chemical Vapor Deposition
MQWs	Multiple Quantum Wells
NBE	Near Band Edge
NH_3	Ammonia
NL	Nucleation Layer
NSSP	Nano-Structured *Semi*-Polar
PE	*Pendeo*-Epitaxy
PEC	Photo-Electro-Chemical
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PL	Photoluminescence
QCSE	Quantum Confined Stark Effect
QW	Quantum Well
RIE	Reactive Ion Etching
RMS	Root-Mean Square
RT	Room Temperature (300 K)
RTA	Rapid Thermal Annealing
SAE	Selective Area Epitaxy
SEM	Scanning Electron Microscope
SiH_4	Silane
SIMS	Secondary Ion Mass Spectroscopy
SiN_x	Silicon Nitride

SSL	Solid-State Lighting
TIR	Total Internal Reflection
TCAD	Technology Computer Aided Design
TD	Threading Dislocation
TEM	Transmission Electron Microscopy
TMI	Trimethyl-Indium
TMG	Trimethyl-Gallium
TR PL	Time-Resolved Photoluminescence
UID	Unintentionally Doped
UTW	Ultra Thin Window
XEDS	X-Ray Energy Dispersive Spectroscopy
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
YBE	Yellow Band Emission

ABSTRACT

Nano-structured InGaN Light-Emitting Diodes
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Chair : P. C. Ku

Solid-state lighting can potentially reduce the electricity consumption by 25%. It requires high efficiency light-emitting diodes across the visible spectrum. GaN and related materials have direct bandgap across the entire visible spectrum and are ideal for future solid-state lighting applications. However, materials defects, polarization charges, and total internal reflection have thus far limited the efficiencies of InGaN LEDs, in particular InGaN LEDs in the green/yellow wavelength range, which are critical in achieving highly efficient LED luminaires with an excellent color-rendering index.

In this Thesis, we have developed and demonstrated that novel *in situ* nano-structured GaN processes in MOCVD are effective in improving the efficiencies of InGaN LEDs. InGaN LEDs grown on quasi-planar *semi*-polar GaN templates were proven to exhibit three times higher internal quantum efficiencies and negligible quantum confined Stark effect using selective area epitaxy. InGaN LEDs grown on nano-structured *semi*-polar GaN templates are also effective to improve the internal quantum efficiency by 31%. The same *in situ* processes are also effective in reducing the defect density by an order of magnitude and increasing the photon extraction efficiency as a factor of two.

The in situ processes include in situ silane treatment and high temperature overgrowth. Both processes require only standard MOCVD tools and hence are cost effective and suitable for mass-production. In situ silane treatment treats c-plane GaN samples with silane under ammonia environment, generating nano-scale truncated cone structures with up to 200 nm scale. These truncated cone structures can be subsequently transformed into pyramidal nanostructures comprising of only (10-11) and (11-22) semi-polar planes using high temperature overgrowth. These processes were applied to both InGaN active region and the LED surface to improve the internal quantum efficiency and the photon extraction efficiency, respectively. Extensive materials, device, and optical characterizations have been carried out in this research.

CHAPTER 1

INTRODUCTION

1.1   Gallium Nitride Materials for Optoelectronic Applications

Gallium nitride based materials, including GaN, AlN, InN, and their alloys, are excellent candidates for short-wavelength optoelectronic applications. Their direct bandgaps extend from ultraviolet to near-infrared. In addition, they exhibit high mechanical and thermal stabilities compared to other III-V *semi*-conductors, making them especially suitable for high-power and high-temperature operations. In recent years, breakthroughs in p-type doping and defect reduction have led to the commercialization of GaN based laser diodes, light-emitting diodes (LEDs), high electron mobility transistors (HEMT) and hydrogen detectors. Despite these advances, many technological challenges such as green gap and substrate growths still remain.

Perhaps one of the most important applications for GaN based materials is solid-state lighting (SSL). Worldwide, lighting constitutes 20% of electricity consumption while its efficiency is much lower than 25%. In contrast, efficiency of space heating has exceeded 90%. To this end, the development of highly efficient and reliable LEDs for

solid-state lighting has been very active in both industry and academia in the past few years. It is projected by the US Department of Energy that by 2015, if successful, solid-state lighting can reduce the overall electricity consumption by 25%.

Unlike GaAs and InP based *semi*-conductors, GaN based materials have suffered from a high density of defects due to very limited availability of lattice-matched GaN substrates. Up to now, most GaN based optoelectronic devices have been fabricated using hetero-epitaxy on foreign substrates such as sapphire (Al_2O_3), silicon carbide (SiC), and aluminum nitride (AlN), and in a very small percentage on silicon. Because of large lattice mismatch, GaN grown on these substrates often exhibits a high density of threading dislocations, typically on the order of $10^8 - 10^{10}$ /cm^2. These defects are still one of the major limiting factors for the performance of GaN based optoelectronic devices, acting as *non*-radiative recombination and scattering centers. Achievement of lower defect density would also improve device reliability, resulting in a longer lifetime. Various defect reduction approaches, such as epitaxial lateral over-growth (ELOG), have been demonstrated and some of the details will be discussed in Chap.1.3.1. As part of this thesis, we have explored a novel approach to using nano-structured GaN to effectively lower the threading dislocation density.

Among various epitaxial techniques that have been developed for GaN based materials, metal-organic chemical vapor deposition (MOCVD) is the leading technology. The typical growth temperature for GaN materials is around 1000 to 1200˚C. This high growth temperature is necessary to improve the crystal quality and is a result of low cracking efficiency of the nitrogen source, ammonia (NH_3), at a low temperature. In

Chapter 2, I will summarize my contributions to successfully ramp up an MOCVD tool for the epitaxial growth of GaN LEDs for this research.

1.2   InGaN LEDs for Solid-State Lighting

The basic component for SSL is a white-light LED. As shown in

Figure 1-1, it can be achieved by mixing various color components, which can be generated either from the direct output of individual LEDs or from color-conversion materials, such as phosphor. To date, commercially available white-light LEDs usually consist of a blue emitter and a yellow phosphor plate. It has been shown that InGaN-based blue LEDs could achieve external quantum efficiency in excess of 70% [1, 2]. However, this di-chromatic configuration typically has a poor color rendering index due to the lack of green and red components. The phosphor conversion process also limits the overall luminous efficiency due to energy loss during downconversion. To achieve luminous efficiency in excess of 200 lm/W and a color rendering index (CRI) in excess of 90, which is required for general illumination, a further improvement in blue LED efficiency and the use of tetra-chromatic configuration (blue + green + yellow + red) is necessary [3].* Unfortunately, the efficiency of both InGaN and AlInGaP LEDs decreases significantly in the green-yellow (500 - 580 nm) range. This efficiency gap is also known as "green gap". Because AlInGaP materials have indirect bandgaps in this wavelength range, to achieve high-efficiency SSL, it is crucial to significantly improve the luminous

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* Note that a trichromatic (e.g. blue + green + red) source cannot achieve a CRI > 90.

efficiency of green and yellow InGaN LEDs. In this thesis, we will address these challenges using nano-structured GaN.
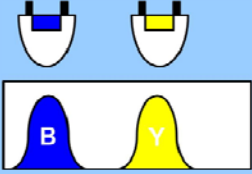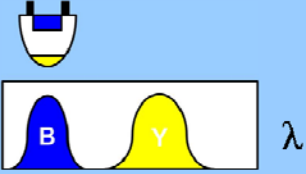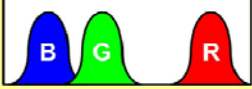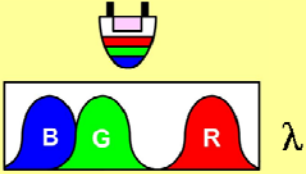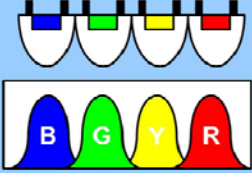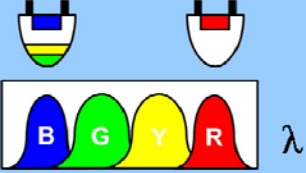
Figure 1-1. Illustration of various potential white-light LEDs configurations (after Ref. [4]).

1.3 Limiting Factors for InGaN LEDs Efficiency

To date, the efficiencies of InGaN LEDs are still limited by materials defects, polarization charges, and photon trapping. In this Section, we will briefly review the state of the art and overview how this research helps address these limitations.

1.3.1   Materials Defects

As mentioned before, the high defect density in GaN based materials grown on foreign substrates increases the *non*-radiative recombination rate and lowers the radiative efficiency. To date, several techniques have been demonstrated to improve the crystal quality and reduce the threading dislocation (TD) density of the GaN layer. Substrate pretreatment at the growth temperature in an ammonia environment, also known as nitridation [5-7], has been shown to be critical for high quality GaN epilayers. The TD density of a typical GaN layer grown on *c*-plane sapphire substrate can be reduced to $10^8/cm^2$ [8] by employing the combination of a low temperature (LT; 450 - 600 ˚C) nucleation layer (NL) and a short annealing at the growth temperature to change the phase of the as-grown NL from cubic to hexagonal [9-11]. As will be discussed in Chapter 2, careful optimization of these low temperature growth sequences can significantly alter the subsequent GaN template growth. To this end, a home-made optical *in situ* monitoring tool (reflectometry) was established and will be discussed extensively in Chapter 2.

In addition low temperature buffer growth, epitaxial lateral overgrowth (ELOG) which is a variation of selective area epitaxy (SAE) has been introduced [12, 13] to further lower the TD density by an order of magnitude to below $10^7/cm^2$. Variations of ELOG including *pendeo-* (from the Latin : hang on or suspended from) epitaxy (PE) [14] and multi-step ELOG are also effective to further reduce the TD density. Additional techniques such as TiN nano-porous network [15] and anodic aluminum oxide nano-

mask [16] have also been proposed and demonstrated. All these methods, however, require *ex situ* processing and hence will add complexity and cost to the manufacturing. In this thesis, we will explore and generalize an *in situ* silane treatment approach to effectively lowering the TD density by an order of magnitude.

1.3.2   Polarization Charges

Due to the *non*-cubic symmetry of GaN materials, compressively-strained active regions in InGaN LEDs exhibit both spontaneous and piezoelectric polarization charges. These polarization charges induce a strong internal electric field (IEF), typically on the order of MV/cm, in the active region, resulting in both efficiency droop at a high injection current density and the decrease of radiative efficiency with an increasing emission wavelength. The IEF can separate electrons from holes and increase electron leakage, resulting in low internal quantum efficiency (IQE) and efficiency droop [17], respectively. The suppression of the IEF, which is expected to increase IQE and the current density at which efficiency droop occurs, can be achieved by reducing the lattice mismatch in hetero-structures or growing them on *semi*-polar (e.g. {10-11} and {11-22}) and *non*-polar (e.g. *a*-plane and *m*-plane) surfaces. Because indium incorporation is more difficult on non-polar planes than on *semi*-polar planes, it is more advantageous to fabricate long-wavelength green-yellow LEDs on *semi*-polar planes to suppress the IEF.

At least three approaches to fabricating *semi*-polar InGaN LEDs have been reported thus far. These include the growth of a GaN epilayer on spinel substrates [18],

on bulk GaN substrates [19-27], and on the sidewalls of pyramidal or ridge GaN structures created on planar polar GaN surfaces using SAE [28-35]. GaN grown on spinel substrates have so far exhibited a high density of threading dislocations and stacking faults, thereby compromising the potential improvement of efficiency from the lowering of IEF. The use of bulk *semi*-polar GaN substrates has demonstrated the advantage of a lower IEF for the enhanced efficiency of green and yellow LEDs [25, 26]. However, limitations such as prohibitively high wafer cost and small substrate size need to be resolved before this approach can become more practical. On the other hand, the SAE technique can create *semi*-polar planes on polar GaN surfaces.

High quality polar GaN films have been fabricated from a variety of substrates including sapphire, 6H-SiC, and bulk GaN by MOCVD. Using growth rate anisotropy and three-dimensional growth, different *semi*-polar and *non*-polar GaN planes can be generated on *c*-plane GaN [13]. In Chapter 3, we will show that high quality InGaN multiple quantum wells (MQWs) which exhibit IQE as large as a factor of three compared to polar MQWs can be grown on pyramidal GaN microstructures. This approach, however, requires *ex situ* patterning processes and does not easily produce a planar structure for electrical contacts. In this thesis, a new *semi*-polar LED structure is investigated, which is enabled by a novel epitaxial nanostructure, namely the nano-structured *semi*-polar (NSSP) GaN, which can be fabricated directly on *c*-plane GaN but without the issues of the SAE technique mentioned above [36]. NSSP GaN also eliminates the issues of excessive defects for GaN grown on spinel substrates and lowers the cost of using bulk *semi*-polar GaN substrates. As we will show later, the surface of NSSP GaN consists of two different *semi*-polar planes: (10-11) and (11-22). Therefore it

is expected that InGaN active regions fabricated on NSSP GaN can exhibit a low IEF, and hence much improved IQE.

1.3.3 Photon Extraction

After photons are generated from the active region in LEDs, they need to escape the device in order to be useful. When light travels from a medium with a higher refractive index to a medium with a lower refractive index, total internal reflection (TIR) occurs at the interface. In InGaN LEDs, photons experiencing TIR at LED surfaces can be re-absorbed by the active region or trapped in the device due to a waveguiding effect as shown in Figure 1-2. In a simple InGaN LED, only 4% of photons generated from the active region can escape from each device surface. It has been shown that surface textures on LED surfaces can greatly reduce TIR and improve photon extraction efficiency as illustrated in Figure 1-2. To date, many surface texturing techniques such as photonic crystal structures [37] and photo-electrochemical etching of GaN surfaces [38] have been introduced. Notably, the photo-electrochemical etching of nitrogen-terminated GaN surface has been successfully implemented into commercial blue LEDs [2]. However, these approaches all require additional *ex situ* patterning processes which add significant costs. In this thesis, we investigate an *in situ* process to fabricate nano-structured GaN surfaces on LEDs which effectively improves the photon extraction efficiency.
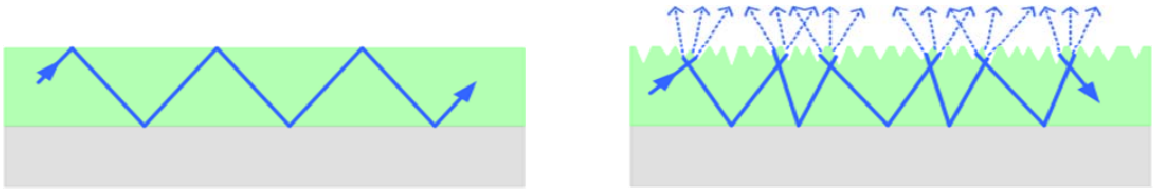
Figure 1-2. Light traveling within waveguides (left) with a smooth interface and (right) with a rough interface (after [39]).

1.4   Organization of the Thesis

The objective of this thesis is to investigate cost-effective nanofabrication techniques that can significantly improve the efficiency of the state-of-the-art InGaN LEDs in both blue and green/yellow ranges for high performance solid-state lighting. The organization of this thesis is as follows.

In Chapter 2, a summary of the MOCVD techniques for InGaN LEDs is given. In Chapter 3, we study the dependence of InGaN LED IQE on {10-11} *semi*-polar planes using SAE. In Chapter 4, fabrication and characterization of novel and cost-effective nano-structured GaN templates will be described. Using *in situ* silane treatment (ISST) and high temperature overgrowth (HTO), the formation of nano-scale inverted cone structures and nano-structured *semi*-polar (NSSP) templates has been obtained. In Chapter 5, we study InGaN *semi*-polar LEDs based on NSSP templates. An improvement of internal quantum efficiency is demonstrated. A green *semi*-polar InGaN LED grown on a *c*-plane substrate is also demonstrated. In Chapter 6, current spreading in NSSP

InGaN LEDs will be discussed. In Chapter 7, the application of ISST for the improvement of photon extraction efficiency of an InGaN LED will be discussed. In Chapter 8, we will summarize and make suggestions for future work.

CHAPTER 2

METAL-ORGANIC CHEMICAL VAPOR DEPOSITION FOR GALLIUM NITRIDE OPTOLECRONICS

2.1   Gallium Nitride Growth

As mentioned in the Introduction, gallium nitride (GaN) and related alloys are excellent candidates for future solid-state lighting. To date, III-nitride epitaxial growth has been limited by the lack of sufficiently large single crystal substrate for homo-epitaxial growth. Therefore, the growth of GaN and related materials has been largely based on hetero-epitaxy using hydride vapor phase epitaxy (HVPE), metal organic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE). Among these techniques, MOCVD is the leading technology due to the advantages on material quality, scalability, and cost [40]. The material quality of GaN grown by MOCVD has been excellent owing to its relatively high growth temperature (1000 - 1200˚C) [41, 42].

To date, various substrate materials including sapphire (Al_2O_3), silicon carbide (SiC), and silicon have been studied for GaN growth (Table 2-1). Although GaN substrates have been recently introduced in markets through bulk material growth on

foreign substrates using HVPE and laser cutting along specific crystal planes, the cost has been prohibitively high. On the other hand, GaN grown on *c*-plane (0001) sapphire substrate exhibits stable growth over a wide range of growth conditions despite high dislocation density at the interface between the substrate and epitaxial layer. In this research, I have helped ramping up an MOCVD system together with Dr. Hongbo Yu. In this Chapter, I will summarize the MOCVD technologies and defect reduction strategies for InGaN light-emitting diodes (LEDs) epitaxy that will be used throughout this Thesis.

Material		Crystal Structure / Growth Plane	Lattice Const. (Å)	Lattice Mismatch w/ GaN (%)	Thermal Expansion Coeff.(10^{-6}/K)
III-Nitride	AlN	Wurtzite / (0001)	a = 3.112 / c = 4.982	2.5	
	GaN	Wurtzite / (0001)	a = 3.189 / c = 5.186	0	5.6(a) ; 7.7(c)
	InN	Wurtzite / (0001)	a = 3.548 / c = 5.703	-10.1	
Substrate	Al_2O_3	Rhonbohedral / Rotated 30°	a = 4.765 / c = 12.982	13.9	
	GaAs	Cubic / (111)	a = 5.653	-20.2	
	$LiAlO_2$	(100)	a = 5.169 / c = 6.267	-6.3(b) -1.4(c)	7.1(a) ; 7.5(c)
	$LiGaO_2$	Orthorhombic / (001)	a = 5.402 b = 6.372 c = 5.007	0.1	6(a) ; 9(b) ; 7(c)
	$MgAl_2O_4$	(111)	a = 8.083	-10.3	7.45
	Si	Cubic / (111)	a = 5.431	-17.0	
	SiC	Wurtzite (6H) / (0001)	a = 3.081 / c = 15.117	3.5	4.2(a) ; 4.0(c)
	ZnO	Wurtzite / (0001)	a = 3.250 / c = 5.207	2.1	2.9(a) ; 4.75(c)

Table 2-1. Properties of III-nitride and various substrate materials (data after [41, 43]).

2.1.1 GaN Growth Using MOCVD

Due to a large lattice mismatch between GaN and sapphire, it is important to contain the defects near the GaN/sapphire interface such that the defect density can be minimized in the device region. Such optimization is achieved using *in situ* reflectometry [44, 45]. A home-made reflectometry system shown in Figure 2-1 was established in our 3 x 2" Thomas-Swan Close-Coupled Showerhead (CCS) MOCVD system. White light is reflected from the sample surface and monitored by a spectrometer during the growth. The reflectivity is sensitive to both the surface morphology and the epitaxial layer structure.
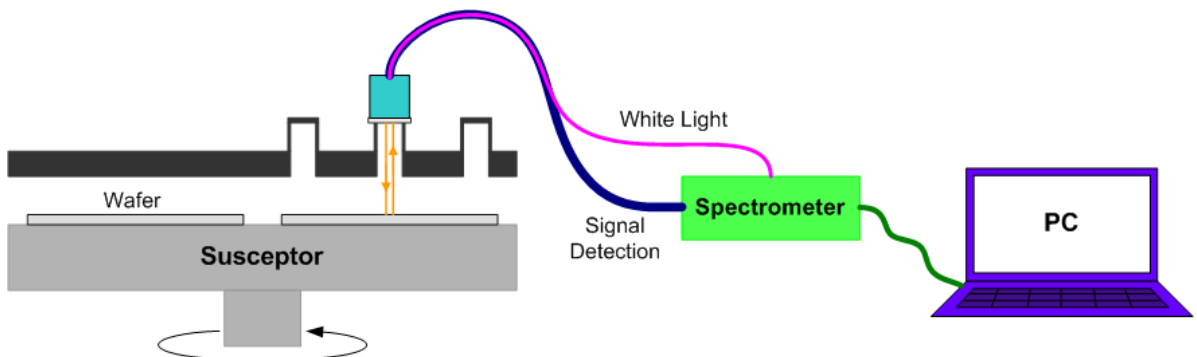
Figure 2-1. Illustration of a home-made *in situ* reflectometry system integrated into the MOCVD system.
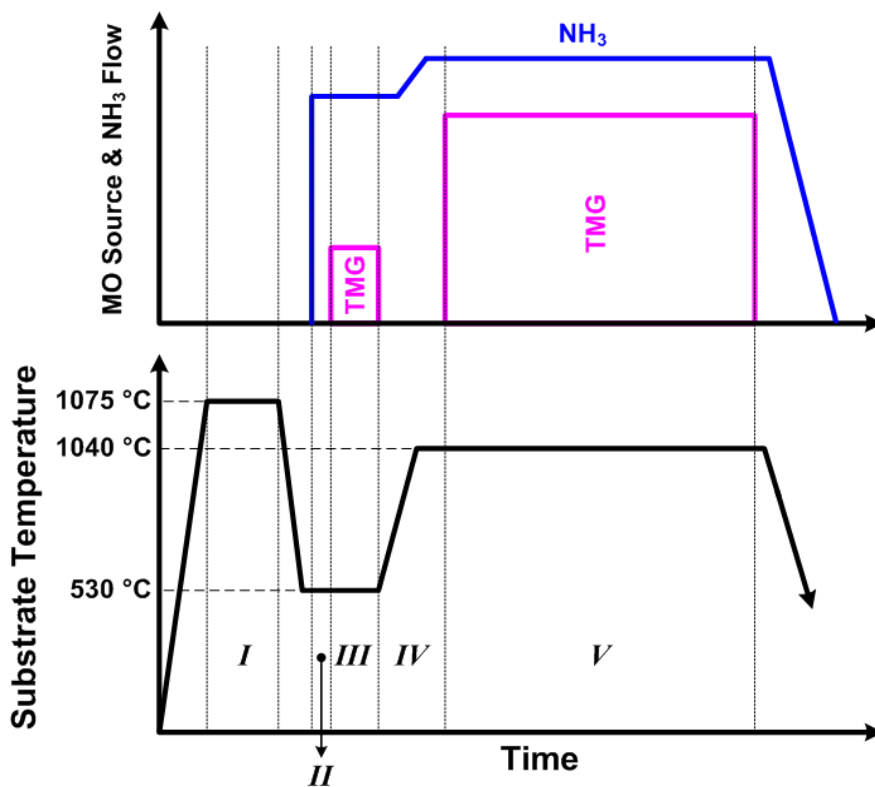
Figure 2-2. Typical growth conditions for GaN templates used in this research.

	Description	Temperature (˚C)	V/III Ratio
I	HT Cleaning	1075	N/A
II	Nitridation	530	N/A
III	LT Nucleation	530	9140
IV	Annealing of LT Nucleation Layer	530 → 1040	N/A
V	HT GaN	1040	1230

Table 2-2. Typical growth conditions for GaN templates used in this research.

Typical growth conditions for GaN templates used in this research are summarized in Figure 2-2 and Table 2-2. Unless otherwise mentioned, *c*-plane sapphire substrates were used. The five steps outlined in Table 2-2, including high temperature (HT) cleaning, nitridation, low temperature (LT) nucleation, annealing of LT nucleation layer, and HT GaN growth, are crucial for high quality GaN epilayer.

Figure 2-3 and Table 2-3 show the corresponding *in situ* reflectometry signal. In the following, we will describe how the reflectometry signal can be used to optimize the GaN template growth. Unless otherwise mentioned, we will refer to the reflectometry signal shown in Figure 2-3.
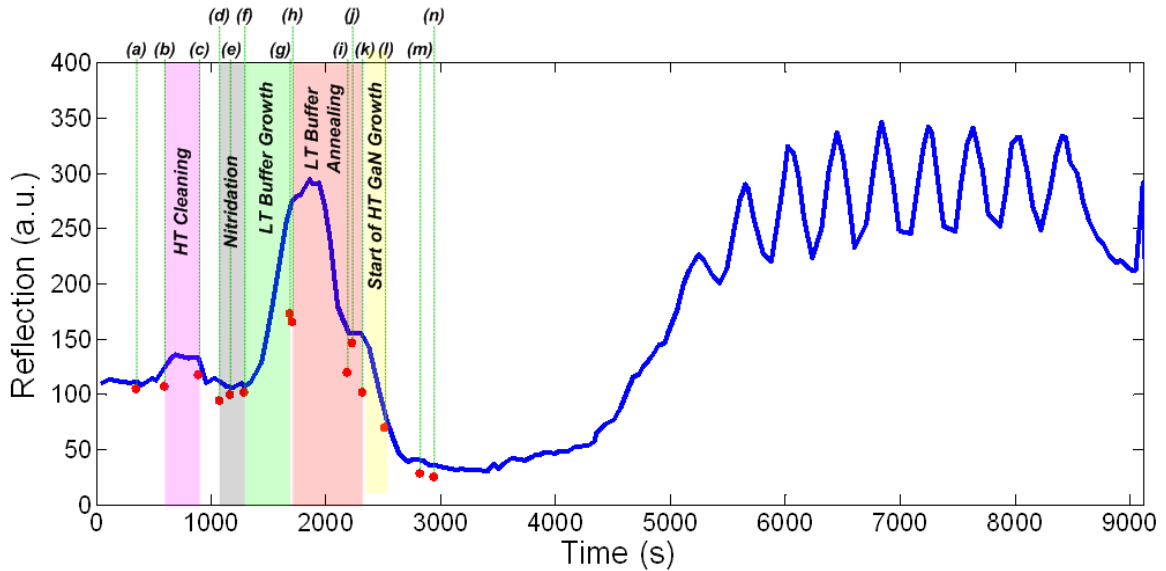
Figure 2-3. *In situ* reflectometry trace of GaN template growth (Sample ID : UM-S07-254). The highlighted areas correspond to important sub-steps during the epitaxy.

(a) Beginning of temperature ramp-up for HT cleaning

(b) Beginning of *HT cleaning*

(c) End of *HT cleaning*

(d) Beginning of NH$_3$ ramp-up (beginning of *nitridation*, NH$_3$ on)

(e) *Nitridation*

(f) Beginning of *LT nucleation*

(g) End of *LT nucleation*

(h) Beginning of temperature ramp-up for *annealing of LT nucleation layer*

(i) End of temperature ramp-up for *annealing of LT nucleation layer* at 1020 ˚C

(j) End of annealing at 1020 ˚C and beginning of *HT GaN growth* : TMG ramping (30 → 60 sccm), NH$_3$ (2000 sccm), i.e. V/III = 1524 → 889

(k) Beginning of TMG and NH$_3$ ramping (T = 1020 ˚C) : TMG$_1$ ramping (60 → 90 sccm), NH$_3$ (2000 → 2650 sccm), i.e. V/III = 889 → 628

(l) Beginning of HT GaN growth (T = 1020 ˚C)

(m) Beginning of HT GaN T ramp-up (T = 1020 → 1040 ˚C)

Table 2-3. Details of GaN epilayer growth (based on the data for sample ID : UM-S07-254).

2.1.1.1   High Temperature Cleaning

Initially, as the sample temperature is ramped up, the reflectivity increases due to the increase of the refractive index of the sample. Kim et al. has thoroughly studied the effect of initial thermal cleaning on the sapphire substrate and experimentally demonstrated that this thermal treatment can effectively reduce the surface roughness of the substrate [46]. Generally, the flat surface is preferred for the GaN nuclei to be formed uniformly, which is critical to the crystal quality of the final GaN epilayer. The specific condition for the HT cleaning should be optimized by examining the treatment temperature and time. In our GaN growth, the optimal treatment temperature and time were set to be 1075 ˚C and 5 minutes, respectively. Moreover, HT surface annealing can effectively eliminate surface moisture.

2.1.1.2 Nitridation

Nitridation [5, 7] is the process of NH_3 preflow under hydrogen (H_2) ambient to prepare the surface for growth. During nitridation, NH_3 reacts with the surface oxygen atoms on the sapphire substrate. Due to the replacement of the oxygen atoms by the nitrogen atoms and the diffusion of the nitrogen atoms into a certain depth, the exposed surface becomes a smooth amorphous state. Because this change of surface morphology is on the order of tens of angstrom, the corresponding reflectivity change is not significant. It has been shown that with a proper nitridation condition, GaN epilayers with lower dislocation density and better electrical and optical properties can be achieved [7]. However, as mentioned above, suitable combination of reactor conditions such as temperature, treatment time, and NH_3 flow rate must be considered. In our GaN growth, the nitridation was optimized at 530 ˚C for a total of 210 seconds under 3 slm of NH_3 flow.

2.1.1.3 Low Temperature Nucleation

As mentioned in Section 1.3.1, several approaches have been introduced to reduce the threading dislocation (TD) density in growing the GaN template. Specifically, the use of low temperature nucleation layer (LT NL) has been shown to be simple yet effective. A threading dislocation density as low as $10^8/cm^2$ has been reported [8].

As GaN is nucleated on sapphire, the cubic phase islands are first formed at a temperature of 450 - 600 ˚C. These islands are subsequently transformed into the wurtzite phase [8]. The increase of the reflectivity during the LT NL growth is attributed to the increase of reflection from the flat top surfaces of nuclei. Basically, we know that the reflection from GaN is about twice stronger than that from sapphire due to the difference in refractive indices. As the islands become denser (i.e. the growth time of LT NL becomes longer), total reflection from the top surface of nuclei becomes up to 200% of reflection from sapphire substrate assuming that the entire surface is covered by GaN islands. Even though the islands are not coalesced completely to form a crystalline layer, this is still possible because the distances between the adjacent islands are too small compared to the optical wavelength. Once the reflectance exceeds twice that of the sapphire (as shown in Figure 2-3), the islands continue to coalesce further, which results in larger GaN grains and a thicker NL. Here, the size of the nucleation islands and the thickness of the NL are critical to obtain high quality GaN epilayer. To show that, we have compared a series of GaN templates with different NL conditions. All conditions were kept the same[†] except the growth time of the LT NL was varied, resulting in different LT NL thicknesses. The thickness of the LT NL was extrapolated by analyzing the reflectometry data as the reflection ratio at the end of LT NL growth to the sapphire substrate ($R_{LT\,NL}\,/\,R_{Sapphire}$). The qualities of the GaN templates were characterized using photoluminescence (PL) and x-ray diffraction (XRD). From these results, the best GaN template quality can be obtained when $R_{LT\,NL}\,/\,R_{Sapphire}$ is around 2.6 which corresponds to a 40nm thick NL, at the given growth conditions.

[†] LT NL growth temperature = 530˚C, V/III = 9140, LT NL annealing time = 420 seconds, HT GaN growth temperature = 1040˚C, V/III = 1230, growth time = 4300 seconds.
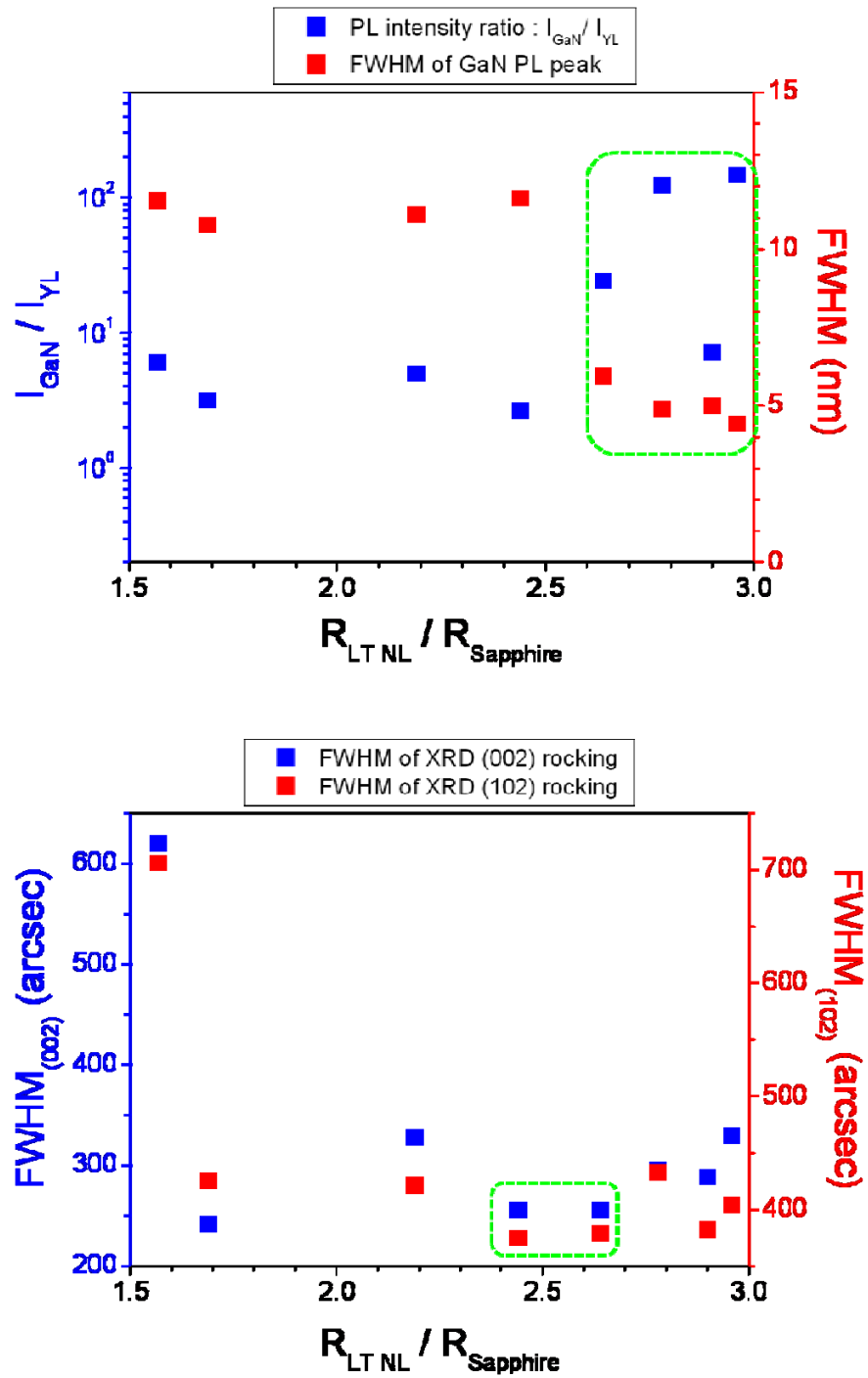
Figure 2-4. The comparison of GaN template qualities with respect to the reflection ratio between the LT NL surface and the sapphire substrate.

2.1.1.4 Annealing of Low Temperature Nucleation Layer

In GaN hetero-epitaxy with a large lattice mismatch, the initial growth on the surface follows the Volmer Weber model [47], i.e. GaN island growth dominates. In order to obtain smooth GaN templates, these islands need to be transformed into the layer-by-layer growth mode using an NL annealing process. During annealing, the substrate temperature is gradually increased up to around 1030 - 1050 °C under NH_3 overpressure. Temperature ramping rate, reactor pressure, and NH_3 flow can control the NL decomposition rate, which determines the surface roughness at the end of the annealing process [48, 49]. In Figure 2-3, after point *(h)* at which LT NL annealing begins, slight increase of reflectance is normally observed. The increase continues until around 800 °C at which GaN decomposition process starts to occur. Once the reflection intensity peaks, it begins to drop due to the increase in surface roughness. Initially randomly distributed islands start to be transformed into relatively uniform islands due to the decomposition of the NL and the migration of the gallium ad-atoms.

Koleske et al. proposed that the NL decomposition rate is a function of the temperature, reactor pressure, NH_3 flow, and NL layer thickness [48, 49]. Because the decomposition rate follows the Arrhenius relation with the increase of temperature, a shorter annealing time is expected to achieve the same surface roughness using a higher temperature ramping rate. In addition, the decomposition rate in H_2 carrier gas increases with respect to the increase of reactor pressure and decreases with NH_3 flow. At a higher NH_3 flow, more nitrogen precursors will be delivered to the surface, lowering the decomposition rate. Concerning the NL thickness, it is known that a thicker NL exhibits a

higher decomposition rate. When the NL becomes thicker, GaN islands grow larger due to the coalescence of the adjacent islands, which increases the area where decomposition takes place. Hence, the optimization of the NL annealing process must be carried out carefully considering all possible effects of each parameter.

During the annealing process, the reflectivity first decreases due to the increase of surface roughness. Further annealing results in a slight increase of reflectivity because at a higher temperature, the surface morphology becomes smoother. However, if we anneal the surface even further, the surface roughness increases again, which results in the decrease of reflection intensity [48, 49]. This phenomenon can be explained by considering the volume of the GaN islands. At the transition point (*(k)* in Figure 2-3), the volume of the islands per unit area becomes the highest which is preferable for the subsequent HT GaN growth. As a rule of thumb, the position of this (reflectometry trace) shoulder is dominated by the highest temperature of the annealing process [50]. In summary, the goal of the low temperature nucleation and the subsequent annealing is to achieve a surface morphology with proper density and sizes of the islands for the following HT GaN growth.

As shown in Figure 2-5, even a slight change of the island distribution caused by a slight difference of the NL thickness and temperature ramping rate (Table 2-4) can result in a significant difference in the following HT GaN growth under the same conditions. In general, it takes longer for an NL with a rougher surface and smaller islands to be transformed into the 2D growth mode. The conditions to achieve high crystal quality GaN on sapphire are mostly related to the growth and annealing of the LT NL.

2.1.1.5 HT GaN Growth

As soon as the sapphire surface is covered with suitable volume, uniformity, thickness, and density of GaN islands, HT GaN growth can be followed. This HT GaN itself can be divided into two parts (Figure 2-6). Part I corresponds to the initial stage of HT GaN growth when the growth mode is transitioned from 3D to 2D, which affects the crystal quality significantly. In part II, GaN epilayer becomes thicker because the growth mode as well as growth condition is stabilized for 2D mode. Several strategies to control the GaN growth in each regime will be briefly discussed in the following.

The growth in part I is a buffer step to prepare a surface suitable for HT GaN growth. During this step, the oscillation of the reflectometry signal becomes increasingly obvious. Initially, the reflectivity continues to drop due to the increase of surface roughness induced by the coagulations of the islands, i.e. 3D growth. As time goes by, the 3D growth mode is suppressed and the 2D growth mode is enhanced. Once the surface becomes flattened due to the enhanced 2D growth, layer by layer growth of GaN begins, which causes the reflectivity to increase. The duration of this part of growth can be optimized by tweaking the reactor pressure, V/III ratio, and growth rate [51, 52]. For example, in the case of a low V/III ratio, it takes longer to recover the reflection intensity, which implies that the change of the growth mode (3D $\rightarrow$ 2D) occurs more slowly.   The reflectivity recovery time is critical to oscillation amplitude in part II. In general, a larger oscillation amplitude corresponds to a better crystal quality.
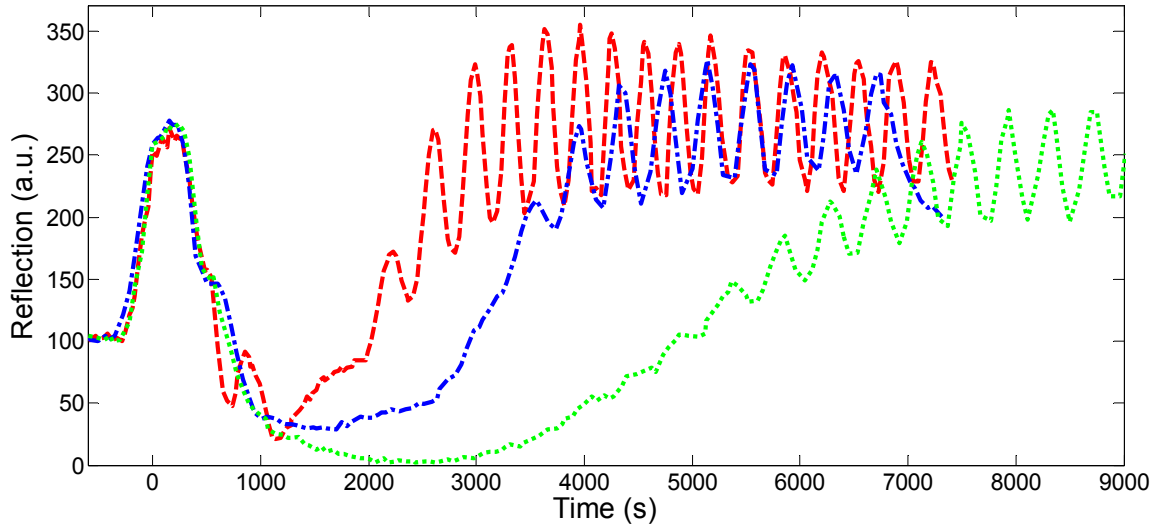
Figure 2-5. Comparison of reflectance data for three different samples : Red, Blue, and Green lines correspond to sample IDs UM-S07-223, UM-S07-254, and UM-S07-261, respectively.

Sample ID		UM-S07-223	UM-S07-254	UM-S07-261
LT NL Growth	Temp. (˚C)	530	530	530
	III/V	9140	9140	9140
	R_1 / R_0	2.527	2.592	2.587
LT NL Annealing	Temp. ramping rate (˚C/min.)	70	63.1	63.1
	Pressure (Torr)	200	200	200
	NH_3 flow (sccm)	2500	2500	2500
	R_2 / R_0	1.574	1.459	1.512
HT GaN	Growth rate (nm/Hr)	1388.31	1148.28	1135.32
XRD	(002) (arcsec)	255.6	280.8	295.2
	(102) (arcsec)	378	360	417
PL	I_{GaN} / I_{YL}	23.79	0.46	74.14
	FWHM (nm)	5.92	11.08	7.68

Table 2-4. Summary of LT NL growth and LT NL annealing conditions for the three samples shown in Figure 2-7 and the comparison of HT GaN crystal quality through XRD and PL ($R_0 = R_{Sapphire}$, $R_1 = R_{LT NL}$, and $R_2 = R_{NL\ Annealing}$).
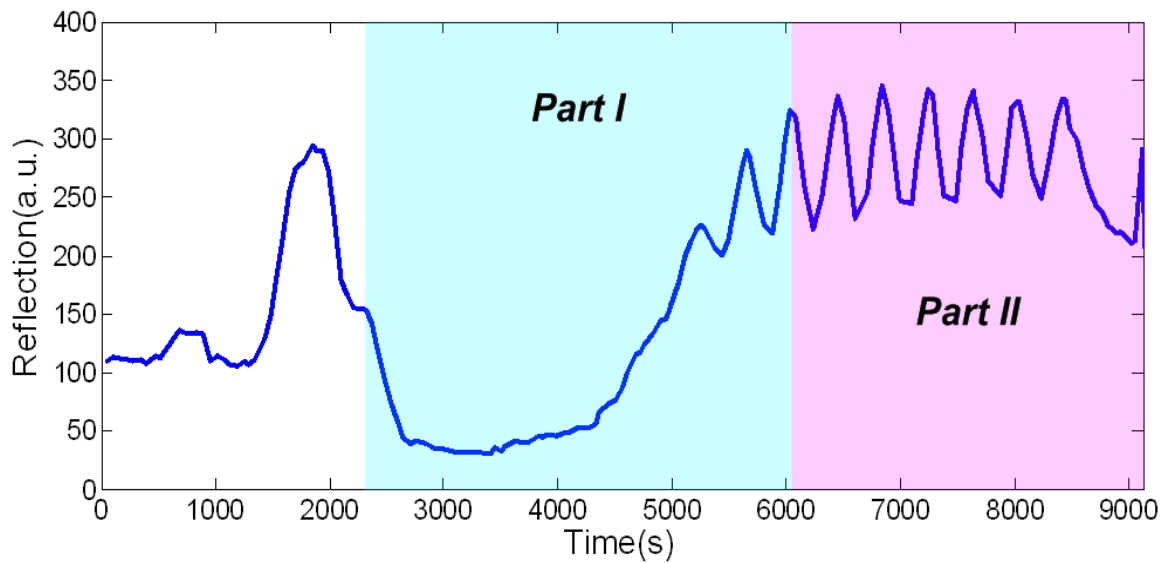
Figure 2-6. Two different growth parts in HT GaN growth (reflectance trace of UM-S07-254).

The part II of the HT GaN growth is stable in a wide range of growth conditions because the growth occurs in a mass transfer limited region. Nevertheless, several key factors will still affect the crystalline structure, including the growth temperature, trimethyl-gallium (TMG) flow, NH_3 flow, V/III ratio, and reactor pressure. As shown in Figure 2-7, the growth rate increases as the group III flow increases but decreases as the V/III ratio and growth temperature increase. The growth rate is one of the key parameters to determine optical and electrical properties of GaN epilayer especially for p- or n- type doped cases. This will be discussed in more details in the next Section.
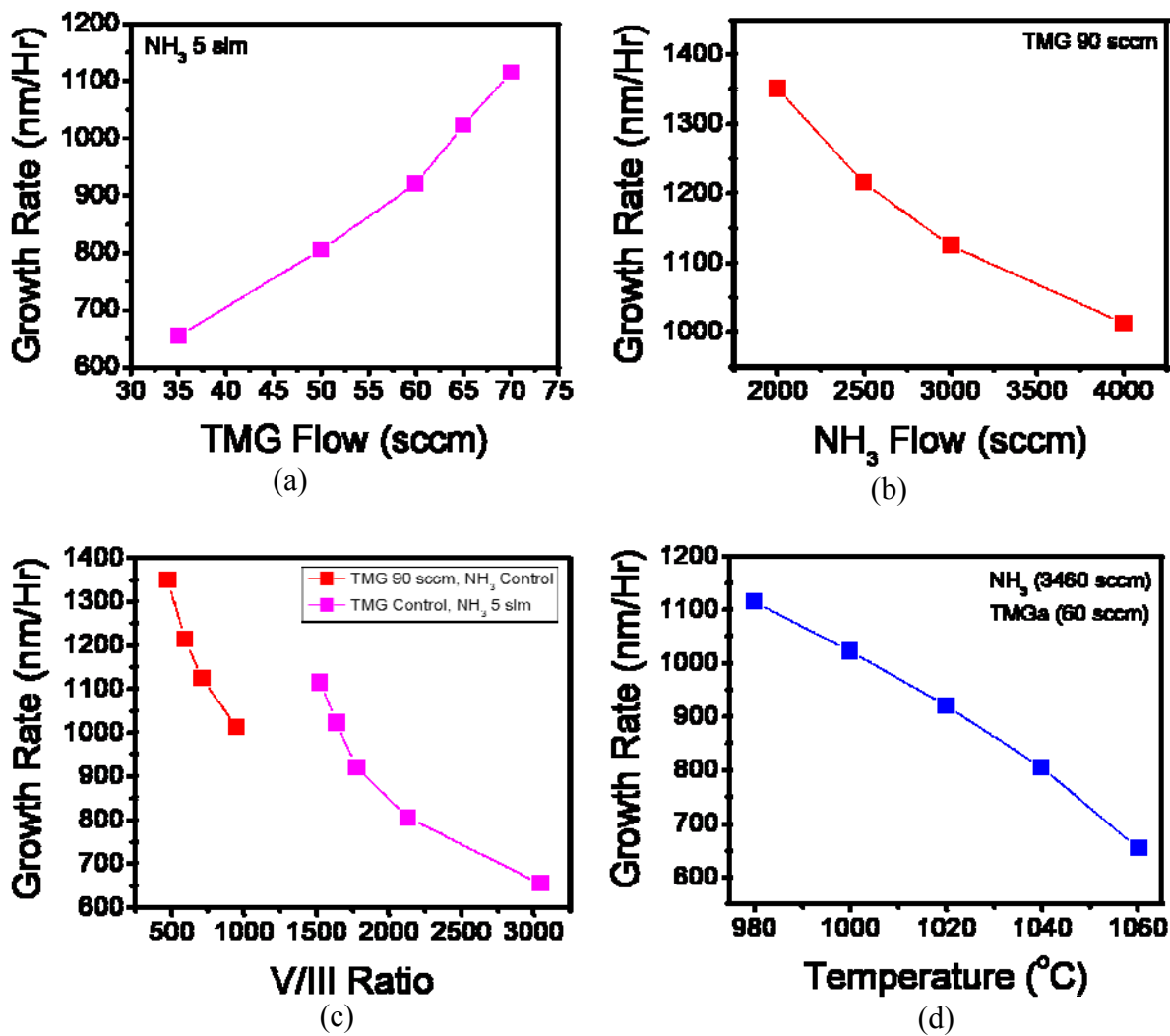
Figure 2-7. The dependence of the growth rate on (a) TMG flow, (b) NH$_3$ flow, and (c) V/III ratio at given TMG flow and NH$_3$ flow, and (d) growth temperature (fixed parameters : reactor pressure = 200 torr, rotation speed = 100 rpm).

2.1.2   GaN Doping

2.1.2.1   N-type Doping

Usually, unintentionally doped (UID) GaN is n-type with a carrier concentration as low as 10^{16}/cm^3. The carrier concentration can be considerably increased by intentional silicon doping using silane (SiH$_4$) [53]. The carrier concentration in an n-type GaN epilayer is closely related to the carrier mobility (Figure 2-8). The carrier mobility decreases exponentially as the doping concentration increases due to enhanced carrier scattering within the crystalline structure. Both the carrier concentration and mobility can be controlled by the growth rate and SiH$_4$ flow.
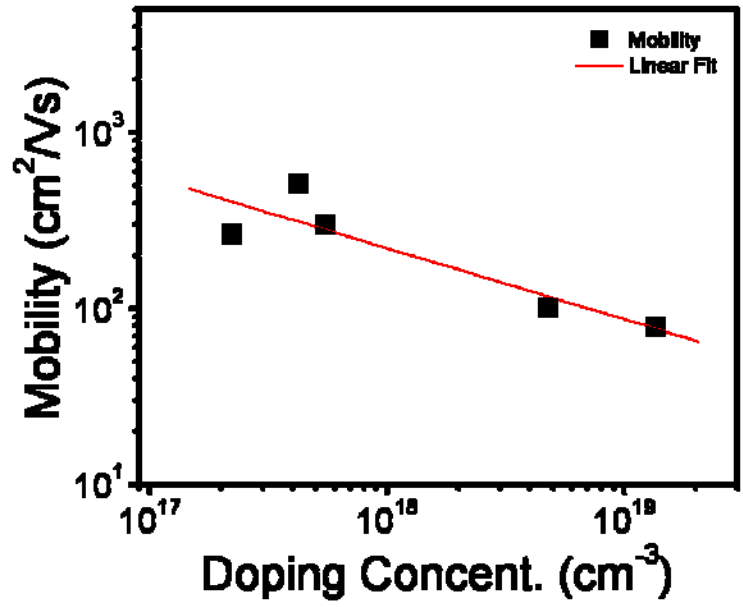
Figure 2-8. Relationship between the carrier mobility and the doping concentration in silicon doped n-type GaN (GaN:Si).
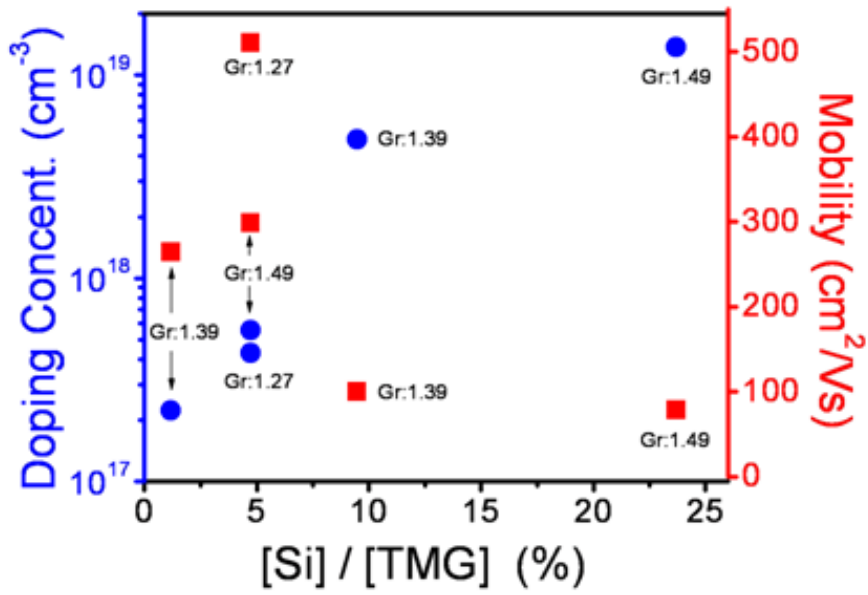
Figure 2-9. Doping concentration and carrier mobility with respect to the silane vapor-phase mole fraction ([Si]/[TMG]) and the growth rate (Gr ; μm/hour) in n-type GaN:Si.

2.1.2.2 P-type Doping

P-type doping has long been a show stopper for GaN based electronic and optoelectronic devices. In 1989, the first p-type GaN, doped with magnesium (Mg) and treated with low energy electron beam irradiation (LEEBI), was reported by Amano et al. [54]. However, the basic mechanism of the treatment had been unknown and as a result the experiment had not been reproducible until 1992 when Nakamura et al. experimentally demonstrated p-type Mg doped GaN (GaN:Mg) by post annealing treatment and ascertained the mechanism of hydrogen passivation of acceptors [55, 56]. Simply by adopting a thermal annealing step, p-type GaN could be obtained reliably, which made it possible for device applications.

Five samples were prepared with varying bis-cyclopentadienyl magnesium (Cp$_2$Mg) flow (50, 100, 200, 250, and 375 sccm). All samples were thermally activated in MOCVD reactor at 720 ˚C for 20 minutes under N$_2$ ambient. Samples were characterized by Hall and photoluminescence (PL) measurements. The dependence of the carrier concentration and mobility on Cp$_2$Mg flow is shown in Figure 2-10 and 2-11. The doping concentration increases but the carrier mobility decreases as Cp$_2$Mg flow increases, similar to the n-type samples. The optical properties of the Mg-doped GaN epilayers with different carrier concentrations are presented in Figure 2-12. The shift of the PL peak position is attributed to the Mg acceptors with different concentrations [57, 58]. The transition energy decreases and is proportional to the acceptor concentration. The sample was also characterized by secondary ion mass spectroscopy (SIMS). About 7 % of total Mg atoms were activated through thermal annealing (Figure 2-13).
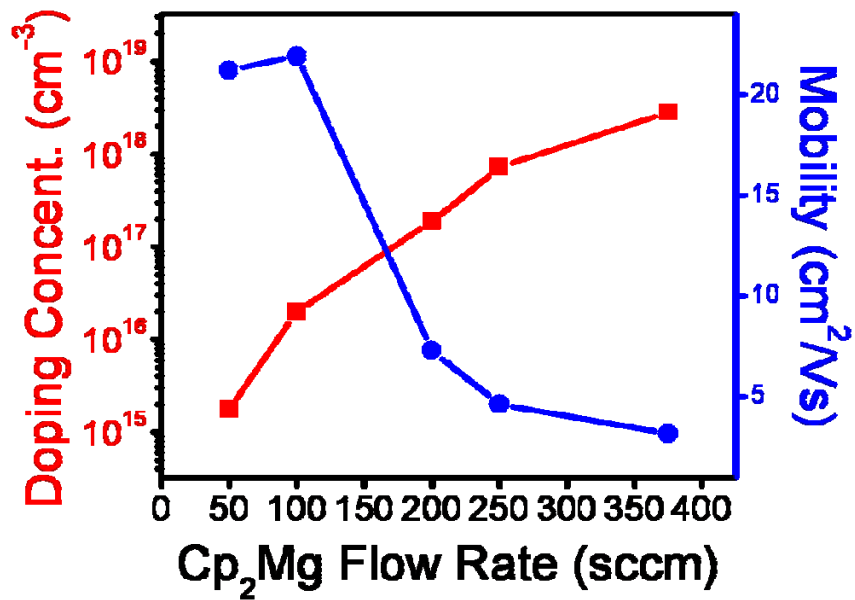
Figure 2-10. Measured doping concentration and carrier mobility of p-type GaN:Mg for different Cp$_2$Mg flow.
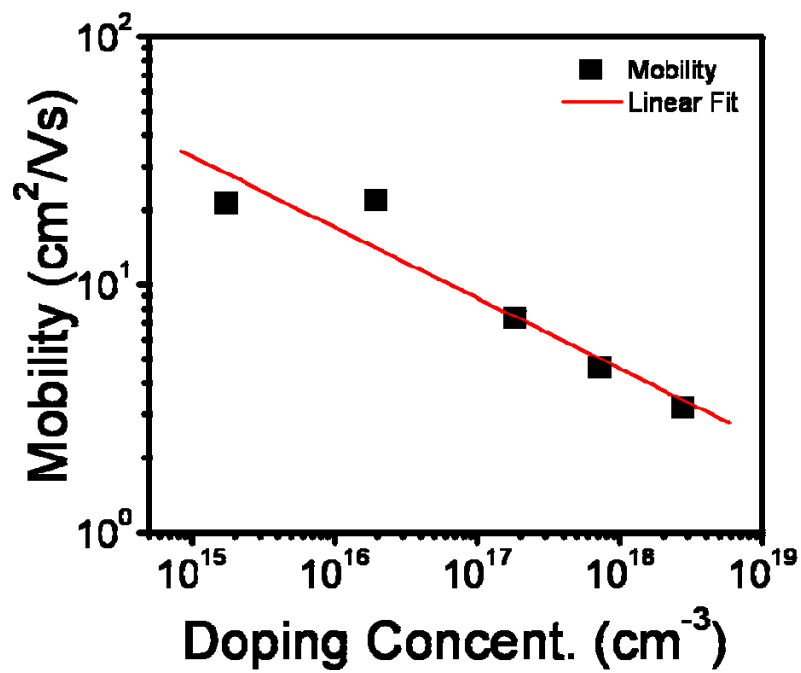
Figure 2-11. Mobility vs. doping concentration of p-type GaN:Mg.

(a)

(b)
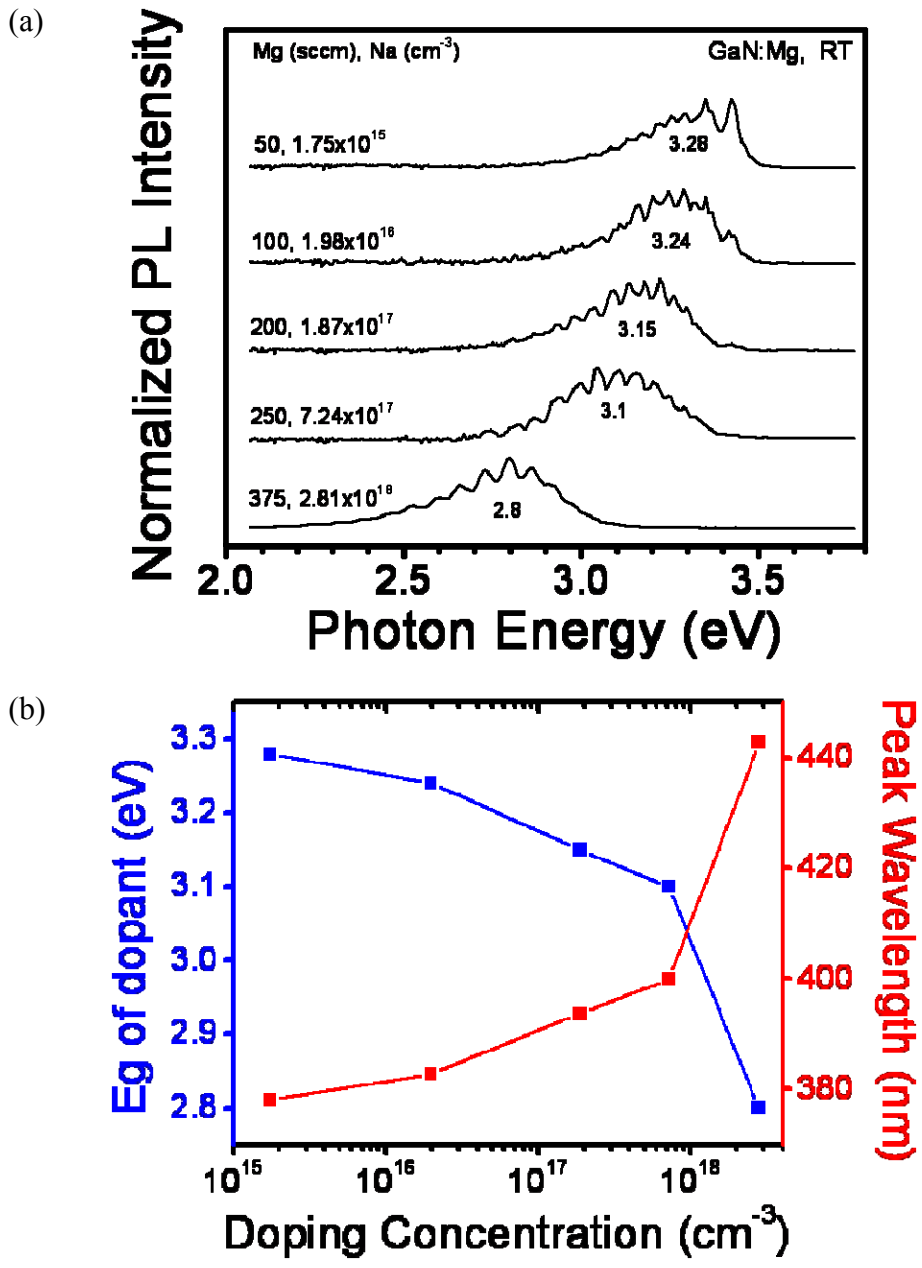
Figure 2-12. Optical properties of GaN:Mg with different carrier concentration; (a) room temperature PL spectra and (b) the Mg-related PL peak with respect to different doping concentrations.
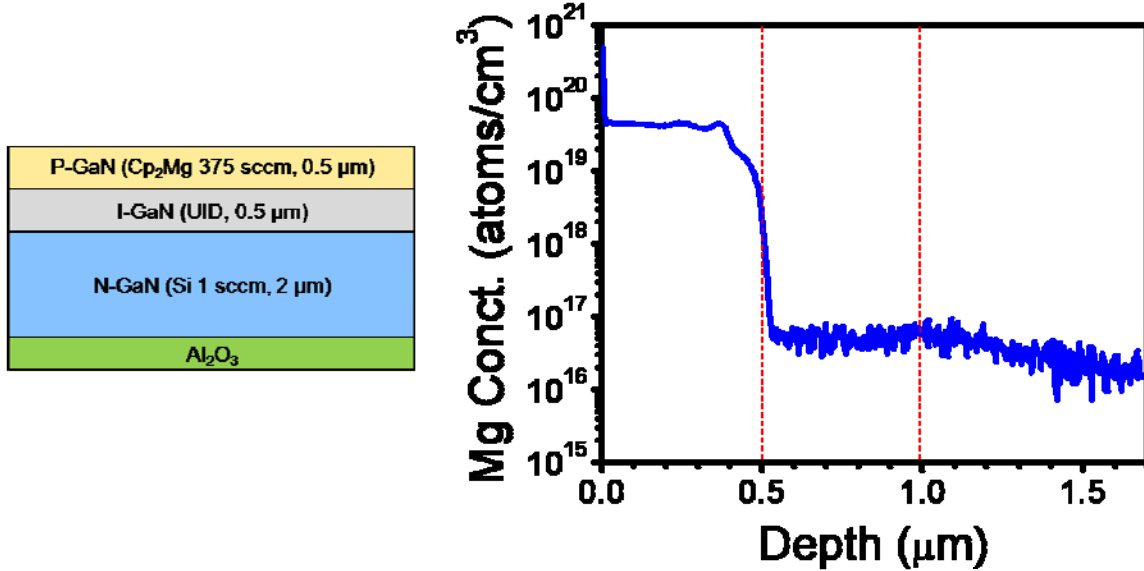
Figure 2-13. As-grown PIN structure (left) and the corresponding SIMS analysis (right).

2.2   InGaN Quantum Wells

There are several control parameters to determine the characteristics of InGaN QWs. These parameters can be categorized into two parts, the structural control and the compositional control. These parameters are not independent.

Parameters for structural control include QW thickness, barrier thickness, the number of QWs, and the surface roughness of the underlying layer. Thinner QW and thicker barrier can reduce the quantum confined Stark effect (QCSE) for QWs grown on *c*-plane substrates. In general, QWs grown on a smooth surface tend to exhibit stronger photoluminescence. High temperature barrier growth, H_2 treatment during the barrier growth, and interruption between the QW and barrier growth can improve the surface morphology of the QW, resulting in better optical properties [59-62].

Parameters for compositional control include growth rate, growth temperature, trimethyl-indium (TMI) flow, and reactor pressure. For example, QWs with high indium contents require lower growth temperature and higher growth rate in order to reduce the indium desorption from the surface [63, 64]. However, for the growth of high indium content QWs, indium segregation and indium phase separation can occur. During post QW growth processes such as HT barrier growth and thermal annealing of p-type GaN, the indium atoms at the interface between the QW and the barrier can segregate into the barriers, eventually degrading the optical properties of the QWs [65, 66]. To minimize the indium segregation and improve the interface morphology, additional treatments such as H_2 interruption and TMI pretreatment, have been introduced [67-70]. TMI pretreatment is also beneficial to enhance the quantum efficiency of the QW.

2.2.1   InGaN Quantum Well Growth Optimization

In this Section, several examples will be discussed to demonstrate the optimization of InGaN QWs in our TS MOCVD. Table 2-5 shows the summary of the growth conditions in details.

Sample ID	Quantum Well Growth					GaN Barrier Growth				PL Measurement	
	Temp. (˚C)	TMG_2 (sccm)	TMI (sccm)	[In]/[In+Ga] (%)	V/III	Temp. (˚C)	TMG_1 (sccm)	TMG_2 (sccm)	V/III	Peak λ (nm)	FWHM (nm)
UM-S07-138	780	1.50	200	80.5	8901.4	780	4.878	1.50	12652.2	397.3	11.3
UM-S07-140	780	1.00	200	86.1	9519.1	780	5.500	1.00	12652.1	428.3	32.4
UM-S07-141	780	0.70	200	89.9	9932.6	780	5.873	0.70	12652.4	453.6	46.8
UM-S07-142	780	1.10	212.9	85.7	8901.1	780	5.500	1.10	12422.9	443.9	30.6
UM-S07-143	780	1.23	208.6	84.0	8901.6	780	5.330	1.23	12427.6	442.5	27.2
UM-S07-169	800	1.39	203.6	82.0	8901.8	800	5.140	1.39	12427.9	430.8	29.1
UM-S07-172	800	1.23	208.6	84.0	8901.6	800	5.330	1.23	12427.6	440.9	38.5
UM-S07-207	805	1.23	208.6	84.0	8901.6	805	5.330	1.23	12427.6	412.3	26.9
UM-S07-209	773.7	1.23	208.6	84.0	8901.6	773.7	5.330	1.23	12427.6	544.7	63.1
UM-S07-212	800	1.23	208.6	84.0	8901.6	800	5.330	1.23	12427.6	434.0	30.8

Table 2-5. Summary of growth conditions for InGaN QW and GaN barrier and the results from the PL measurement (QW growth time = 3 minutes; GaN barrier growth time = 10 minutes; NH_3 flow for both QW and GaN barrier = 4 slm; reactor pressure = 400 torr; N_2 ambient condition).

2.2.1.1   Growth Temperature Optimization

The growth temperatures of the QWs and barriers are perhaps the most critical parameter that will affect the emission wavelength and photoluminescence characteristics. In Figure 2-14, the comparison of samples UM-S07-207, UM-S07-209, and UM-S07-212 shows how the growth temperature affects the characteristics of the QW. The peak emission wavelength redshifts as the growth temperature decreases, which is attributed to a lower growth rate and reduced indium evaporation and hence a higher indium solid composition. However, the emission linewidth increases as the growth temperature decreases. Usually, a high growth temperature can improve the crystal quality and surface morphology of both the QWs and barriers. As discussed, smooth and dislocation-free underlayer is favorable to achieve a sharp interface between the InGaN QW and GaN barrier which results in a narrow emission linewidth. To obtain a longer emission wavelength, a lower growth temperature is required to achieve a high indium content but at the expense of a larger emission linewidth. To resolve this matter, techniques such as HT GaN barrier growth, growth interruption with H_2 treatment, and TMI pretreatment have been proposed in recent years [67, 70].
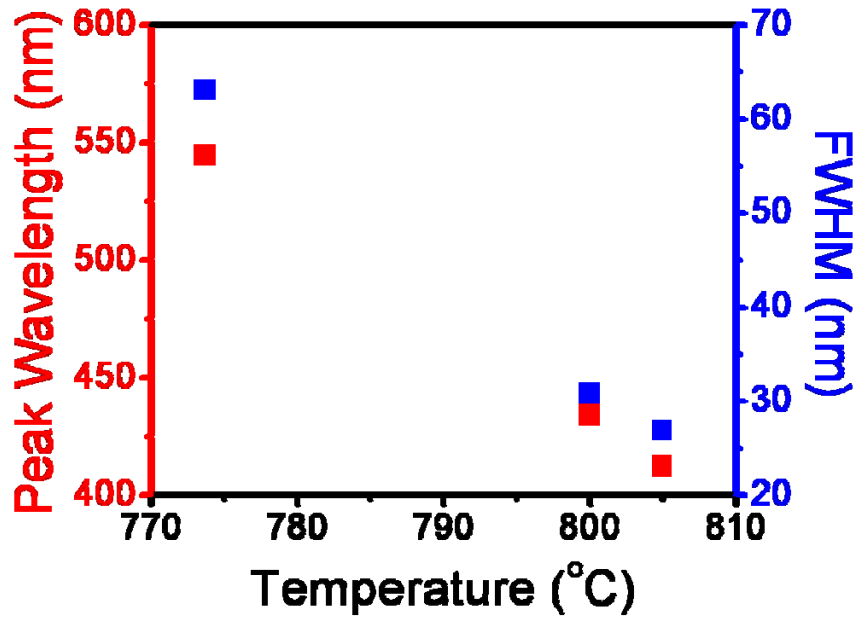
Figure 2-14. PL measurement data of the QWs grown at different growth temperatures (sample IDs : UM-S07-207, UM-207-209, UM-S07-212)
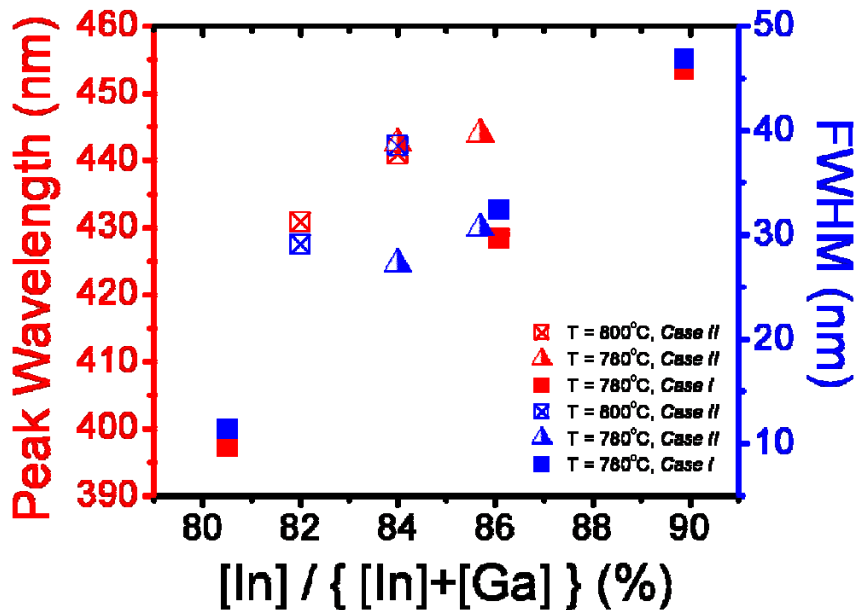
Figure 2-15. PL measurement data of the QWs grown with different indium vapor-phase mole fractions at two different growth temperatures ; growth temperature = 800 ˚C with *Case II* (sample IDs : UM-S07-169, UM-S07-172), growth temperature = 780 ˚C with *Case II* (sample IDs : UM-S07-142, UM-S07-143), and growth temperature = 780 ˚C with *Case I* (sample IDs : UM-S07-138, UM-S07-140, UM-S07-141); *Case I* - TMGa flow control with varying V/III and *Case II* - both TMGa and TMI flow control with a constant V/III.

2.2.1.2 Indium Mole Fraction Control

In addition to the growth temperature, it is also critical to control the indium vapor-phase mole fraction, i.e. the ratio of moles of indium flow to the total group III flow ([In] / {[In]+[Ga]}). Figure 2-15 shows how the indium mole fraction changes the emission wavelength, which unfortunately is not linear due to the increasing difficulty of incorporating indium. For all cases, both the emission wavelength and linewidth increase with the increase of indium mole fraction. The increase of the emission linewidth can be partially attributed to the indium phase separation. There is a limitation to accomplish high indium content by solely adjusting indium mole fraction. Therefore, a combination of the low growth temperature and high indium mole fraction is required for longer wavelength (green/yellow) InGaN QWs.

2.3 Summary

In this chapter, III-nitride growth using MOCVD was discussed. GaN epitaxy on *c*-plane sapphire substrate was reviewed and the optimization of the crystal quality was demonstrated. High temperature cleaning, nitridation, LT nucleation, annealing of LT nucleation layer, and HT GaN growth were performed successively to achieve high quality GaN epilayer. In particular, LT nucleation layer thickness is crucial to determine the subsequent decomposition rate of nuclei while optimized annealing of nucleation layer can allow us to achieve proper density and volume of nuclei for the following 3D growth mode. In the early stage of HT GaN growth, growth mode transformation from

3D into 2D occurs and techniques have been developed to enhance the growth mode evolution, such as growth rate modification. Once HT GaN growth becomes stabilized, GaN growth rate can be adjusted by V/III ratio and growth temperature. To achieve high crystal quality, it is essential to monitor and adjust the growth conditions using *in situ* reflectometry at each growth step.

To fabricate III-nitride optoelectronic devices, n-type and p-type GaN are required and can be obtained using Si and Mg dopants, respectively. In general, SiH_4 and Cp_2Mg are used for the precursors of Si and Mg. Doping concentration can be controlled by material growth rate and dopant mole flow. For p-type material, additional thermal annealing process is required to activate Mg dopants.

At last, InGaN QW growth was discussed. The optical property of InGaN QW is determined by growth temperature, indium mole fraction, growth rate, and the thicknesses of QW and/or GaN barrier. In addition, the quality of QW critically depends on the morphology of the underlying layer.

CHAPTER 3

SEMI-POLAR InGaN LEDs USING SELECTIVE AREA EPITAXY

In this chapter, we present the internal quantum efficiency (IQE) of the InGaN multiple quantum wells (MQWs) grown on *semi*-polar GaN. As discussed in the Introduction, the internal electric field (IEF) in *c*-plane InGaN MQWs can significantly lower the IQE of InGaN light-emitting diodes (LEDs). It has been theoretically postulated that InGaN MQWs grown on *non*-polar or certain *semi*-polar planes can greatly reduce the IEF and increase the IQE [71]. In this Chapter, we describe our experimental demonstration of this theory. Due to the difficulties of obtaining high quality *semi*-polar GaN templates, it has been challenging to experimentally characterize the IQE of *semi*-polar InGaN MQWs. Using selective area epitaxy, high quality *semi*-polar MQWs have been obtained, allowing us to study the physics without being masked by materials defects. To our knowledge, this was the first such experimental reports for {10-11} *semi*-polar plane.

3.1 Fabrication of InGaN *Semi*-polar LEDs Using Selective Area Epitaxy

As discussed in chapter 1.3, the use of the *semi*-polar plane can largely eliminate the polarization charge induced IEF. Three different approaches were mentioned for *semi*-polar GaN template growth, including growth of a GaN layer on spinel substrates, on bulk GaN substrate, and on the sidewalls of pyramidal or ridge GaN structures using selective area epitaxy (SAE). In addition to being cost effective, SAE of III-nitride is a useful technique for the integration of optoelectronic devices because it can precisely control the position, dimension, composition, and shape of the device during the epitaxial growth. As a result, InGaN LEDs can be monolithically integrated with silicon driving circuitry. In this Section, we will describe the epitaxial growth of high quality *semi*-polar GaN templates using SAE.

During SAE, the growth only occurs on the part of a substrate that is not covered by the SAE mask. Typical mask materials include silicon dioxide (SiO_2), silicon nitride (SiN_x), tungsten (W), and gallium oxide (Ga_2O_3). Depending on the growth conditions and initial substrate orientation, there can be three possible types of GaN regrowth topology as shown in Figure 3-1 [13, 72-75]. The second and the third types are useful for nanowire growth [76] and epitaxial lateral over-growth (ELOG), respectively. The first one will be used in this Chapter to generate *semi*-polar GaN templates.

The experimental procedure to generate (10-11) *semi*-polar planes on a *c*-plane GaN template is summarized as follows. First, a 50 nm thick SiN_x mask was deposited using plasma-enhanced chemical vapor deposition (PECVD) on a 1.5 μm thick GaN film. Circular apertures with a diameter of 4 μm and spacing of 30 μm were defined on the

mask using photolithography and BHF (buffered hydrofluoric acid) wet etching. The GaN hexagonal pyramids with {10-11} sidewalls were obtained using SAE. This is because under typical GaN growth conditions, the growth rate along the [10-11] direction is the slowest [13]. *Semi*-polar GaN templates formed by SAE have very smooth surfaces as a result of the self-limiting epitaxial process. They also exhibit lower defect density as compared to *semi*-polar templates directly grown on foreign substrates. These properties are very useful for the fabrication of high quality InGaN *semi*-polar LEDs.
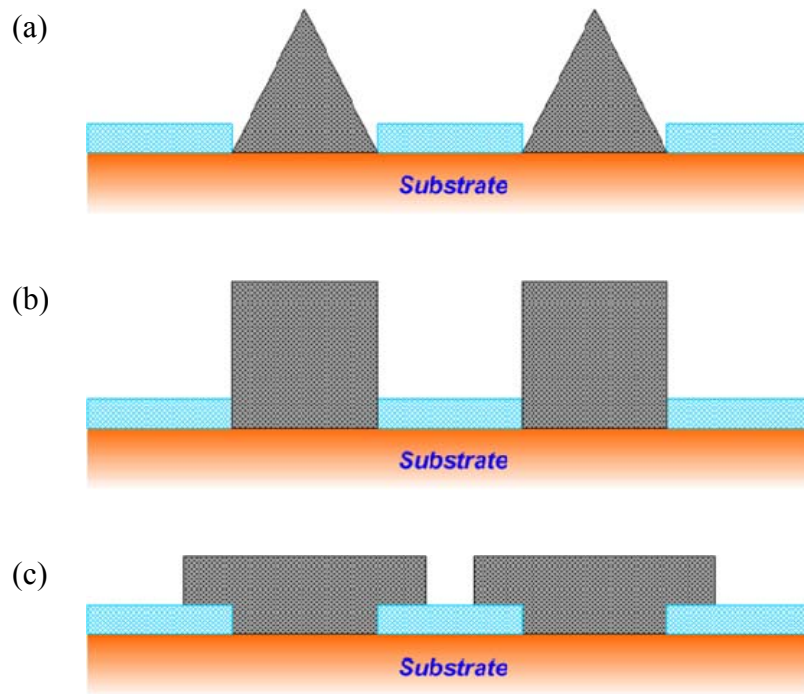
Figure 3-1. Schematics of three possible SAE regrowth topologies: (a) triangular cross section, (b) vertical side wall type 1, and (c) vertical side wall type 2.

Five pairs of InGaN/GaN multiple quantum wells (MQWs) were subsequently grown on the *semi*-polar planes (Figure 3-2). For comparison, a control sample with five

InGaN/GaN MQWs on the (0001) GaN template was prepared. The thickness of InGaN quantum well (QW) and indium content were measured to be 3 nm and 12 % using x-ray diffraction, respectively. Two different QW growth temperatures, 750 ˚C and 770 ˚C, were used to achieve 3 nm and 5 nm of QW thickness and the GaN barrier thickness was adjusted to be three times of QW thickness.
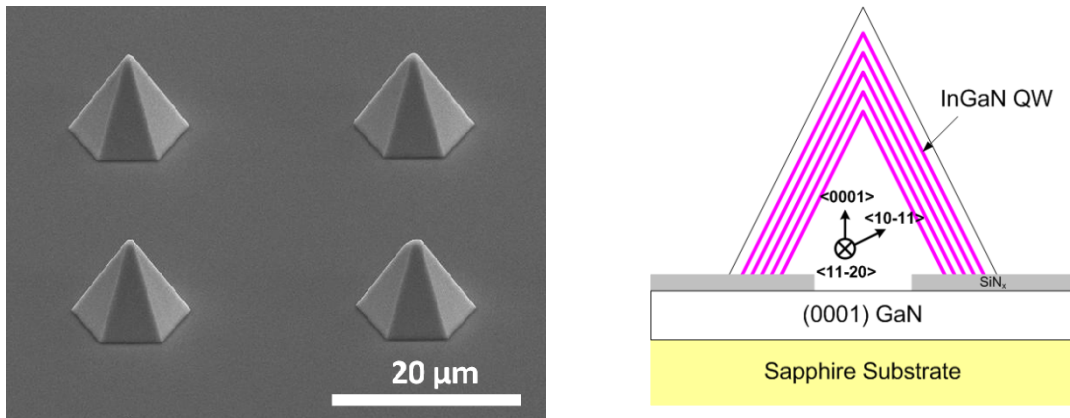
Figure 3-2. (Left) SEM image of the generated {10-11} *semi*-polar planes using SAE; (Right) Schematic of five MQWs grown on {10-11} *semi*-polar planes.

3.2   Optical Properties of InGaN *Semi*-polar MQWs

Room temperature (RT; 300 K) photoluminescence (PL) measurements were used to characterize the optical properties using a 325 nm He-Cd laser with a spot size of approximately 100 μm. Figure 3-3 (a) shows the RT PL from three samples; 5 nm InGaN QWs grown at 770 ˚C, 5 nm InGaN QWs grown at 750 ˚C, and 3 nm InGaN QWs grown at 770 ˚C. Each PL curve was dominated by a strong blue emission from InGaN MQWs. The highest peak energy with 2.78 eV can be achieved from 3 nm MQWs grown at 770

°C. As the QW thickness was increased to 5 nm, the emission peak was red-shifted to 2.68 eV as expected. When the growth temperature of the MQWs was lowered to 750 °C, the peak energy became further red-shifted to 2.57 eV for 5 nm MQWs, which is attributed to the increase of indium content in MQWs.

(a)

(b)
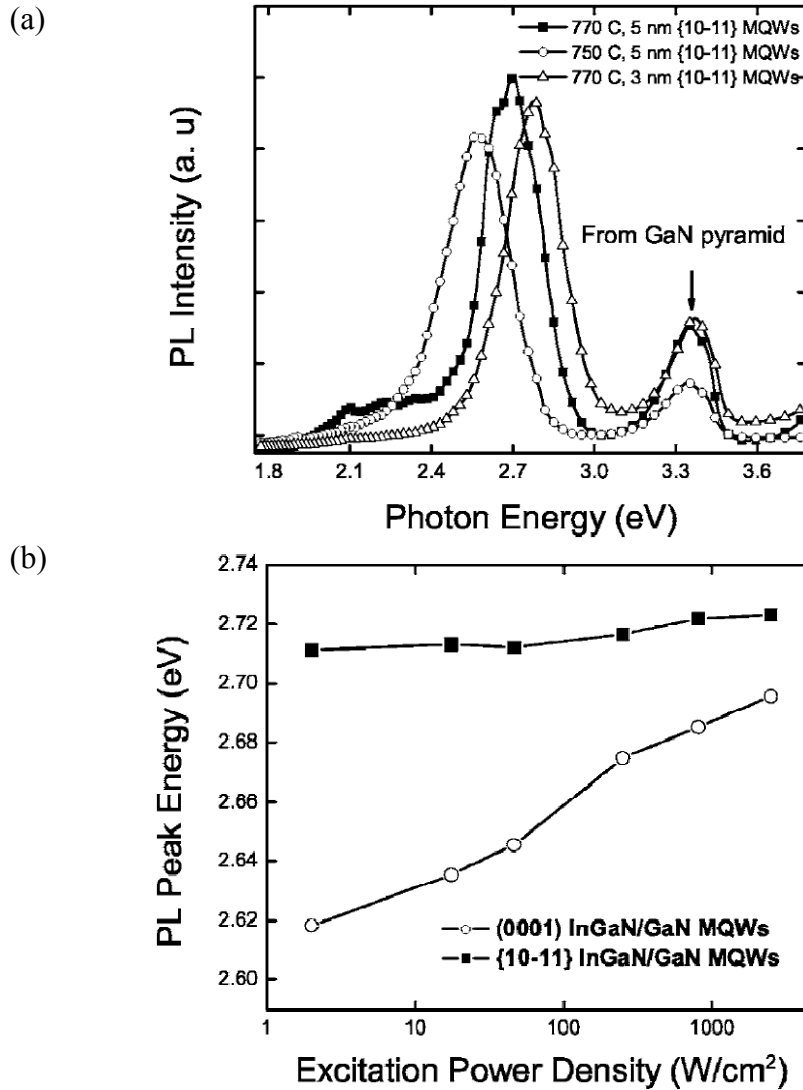
Figure 3-3. (a) RT PL measurement data of the three samples and (b) RT excitation dependent PL measurement showing reduced QCSE in {10-11} *semi*-polar InGaN MQWs.

RT excitation dependent PL measurement was performed for (0001) and {10-11} InGaN MQWs to assure the IEF in the MQWs. Figure 3-3 (b) shows that the PL peak energy of {10-11} MQWs stays almost the same but that of (0001) MQWs exhibits up to 80 meV blueshift with the increase of excitation power density. This reduced quantum confined Stark effect (QCSE) confirms the suppression of IEF in MQWs grown on the {10-11} *semi*-polar plane.
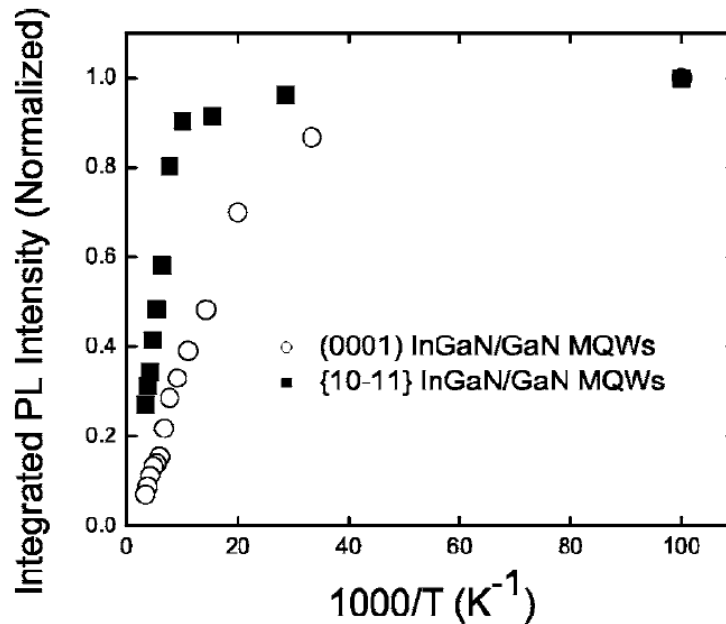
Figure 3-4. Temperature dependence of the integrated PL intensity for both (0001) and {10-11} InGaN/GaN MQWs. The intensities are normalized to their values at 10 K.

The internal quantum efficiencies (IQE) for both (0001) and {10-11} InGaN MQWs were obtained using temperature dependent PL measurements. Assuming the IQE at low temperature (10 K) as 100 %, the IQEs could be calculated using integrated PL

intensities. Figure 3-4 shows the Arrhenius plot of integrated PL intensity for each which was normalized to its integrated PL intensity at 10 K. The estimated IQE of {10-11} InGaN MQWs at room temperature was three times higher than that of (0001) InGaN MQWs, confirming the enhanced performance of light emitters on {10-11} *semi*-polar plane using SAE.

3.3   Summary

In this Chapter, the optical properties of the *semi*-polar {10-11} InGaN/GaN MQWs grown by SAE were investigated. The emission wavelength of the MQWs was well controlled by adjusting the MOCVD growth parameters and the IEF was remarkably reduced in comparison with the (0001) MQWs. The emission peak energy decreases monotonically with increasing temperature. The IQE of the *semi*-polar MQWs is about three times as high as that of the (0001) MQWs. Our experimental results suggest that *semi*-polar {10-11} structures fabricated by SAE are promising for high performance III-nitride light emitters.

CHAPTER 4

NANO-STRUCTURED *SEMI*-POLAR GALLIUM NITRIDE TEMPLATES USING *IN SITU* PROCESSING

In this chapter, a novel *in situ* fabrication method to create nano-structured gallium nitride (GaN) will be discussed and demonstrated. Two processes, namely *in situ* silane treatment (ISST) and high temperature overgrowth (HTO), will be combined to generate nano-scale structures on a GaN epilayer. The overall fabrication process is illustrated in Figure 4-1. The *in situ* silane treatment process can produce randomly distributed nano-scale inverted cone structures with a typical lateral dimension of about 200 nm on a *c*-plane GaN template. A successive HTO process can convert the truncated cone structures into a nano-structured *semi*-polar (NSSP) plane. Compared to other approaches, such as photo-electrochemical etching [38, 77], our approach does not require any additional *ex situ* process and uses only standard metal-organic chemical vapor deposition (MOCVD) tools. Hence, the proposed processes are cost effective and allow one to avoid possible contamination during the *ex situ* processes.

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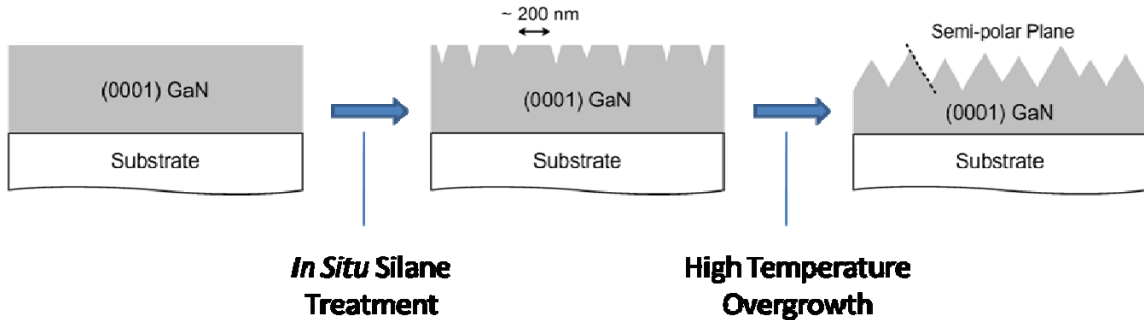
Figure 4-1. Illustration of *in situ* silane treatment and high temperature overgrowth for nano-structured *semi*-polar GaN templates.

4.1 *In Situ* Silane Treatment

4.1.1 Overview of *In Situ* Silane Treatment

In situ silane treatment (ISST) is a process in which a GaN surface is exposed to a mixture of silane (SiH_4) and ammonia (NH_3) at a typical GaN growth temperature. Previously, short (< 1 minute) ISSTs have been demonstrated as an effective approach to lower the threading dislocation in GaN [78-80]. In this section, we will demonstrate that not only is ISST effective for defect density reduction in GaN but a long ISST (>> 1 minute) can be used to create nano-structured GaN.

ISST has several advantages over other threading dislocation (TD) density reduction methods because it does not require any additional *ex situ* patterning processes as required in epitaxial lateral over-growth (ELOG) and *pendeo*-epitaxy (PE). To date, the mechanism of ISST is not well understood. Tanaka et al. proposed that the mixture of SiH_4 and NH_3 acts as an anti-surfactant which prohibits GaN desorption at the surface

and changes the subsequent growth from two-dimension (2D) to three-dimension (3D) [81, 82]. Pakula et al. reported that the exposed surface was selectively etched during ISST and they believed that the TD density reduction was related to the lateral overgrowth over the pits [83]. Some groups ascribe ISST as the formation of a SiN_x nano-mask on the surface and nano-scale ELOG occurred during the subsequent material growth [78-80]. Although the exact mechanism is still under debate, this technique has been applied for the growth of GaN epilayers on different substrates, such as sapphire, silicon carbide (SiC), and silicon [82, 84].

In this section, we will discuss on investigations of the formation, materials and optical properties of nano-structured GaN formed by ISST processes.

4.1.2   Formation of Nano-structured GaN Surface

In this subsection, the change of the surface morphology after ISST was examined. Samples were grown on c-plane GaN templates using the Thomas-Swan close-coupled showerhead (TS CCS) MOCVD system. Detailed growth conditions for GaN templates have been described in Section 2.1.1. During the ISST process, the TMGa was switched off and 40 sccm of diluted SiH_4 (50 ppm in H_2) was introduced into the reactor for a certain duration under an NH_3 environment. The silane source used in an ISST process is the same as that used for n-type doping in GaN. Figure 4-2 and Table 4-1 illustrates and describes the detailed growth conditions of GaN template growth and ISST. An ISST process which was longer than a few minutes at the given condition can create nano-scale

truncated cone structures on the exposed as-grown GaN template. The image taken by

atomic force microscopy (AFM; Digital Instruments Nanoscope) in Figure 4-3 shows that

noticeable surface roughness starts to develop after about 2 minutes of ISST.
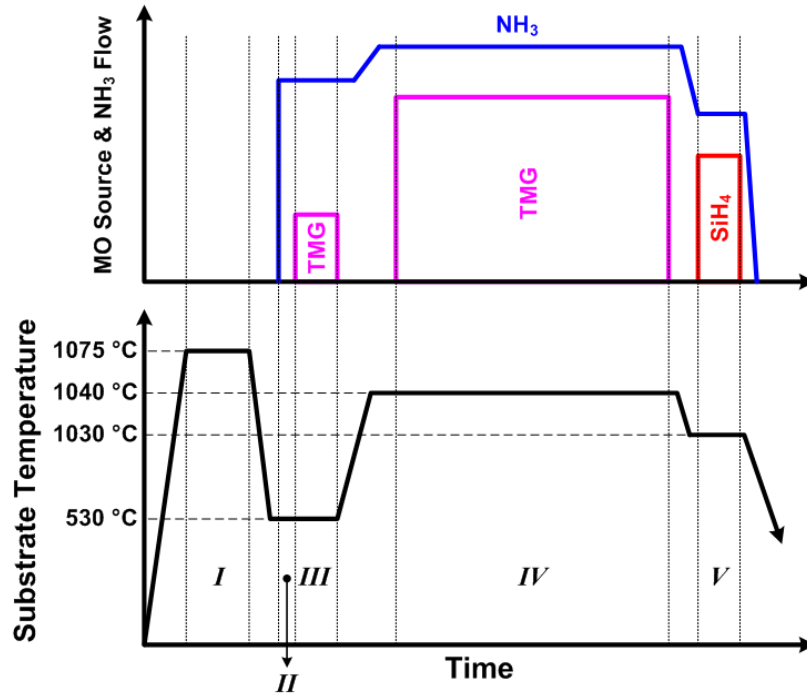
Figure 4-2. Growth conditions used for the combined GaN template growth and ISST process.

	Description	Temperature (°C)	V/III Ratio	SiH$_4$ Flow (sccm)
I	Substrate Annealing	1075	-	-
II	Nitridation	530	-	-
III	LT NL	530	9140	-
IV	HTO GaN	1040	1230	-
V	ISST	1030	-	40

Table 4-1. Growth conditions for GaN template growth and ISST process.
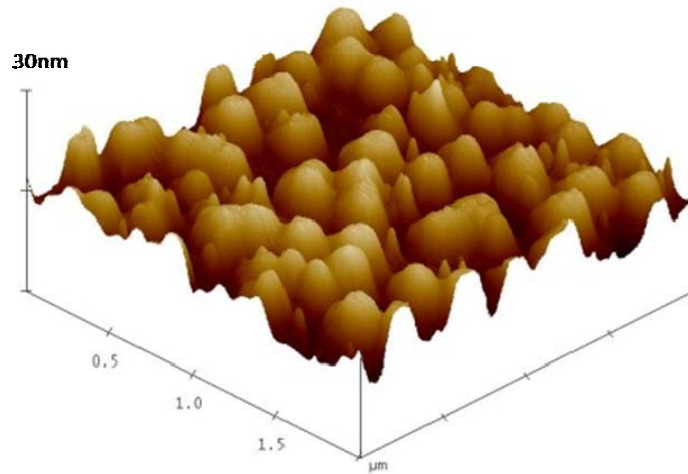
Figure 4-3. AFM image of 150 sec ISST-treated sample.

To understand the surface morphology change with respect to the ISST process time, a series of samples with different ISST treatment times were examined. The images taken by scanning electron microscope (SEM; FEI Nova Nanolab) clearly show surface morphology evolution in Figure 4-4. Nano-scale structures start to form with an increasing ISST time and nano-scale inverted cone structures were clearly observed after 5 minutes of ISST. The root-mean square (RMS) surface roughness of each sample was measured by AFM and plotted in Figure 4-5. The plot shows that the roughness increases linearly before decreasing after 5 minutes. This is attributed to the merging of adjacent truncated cone structures.
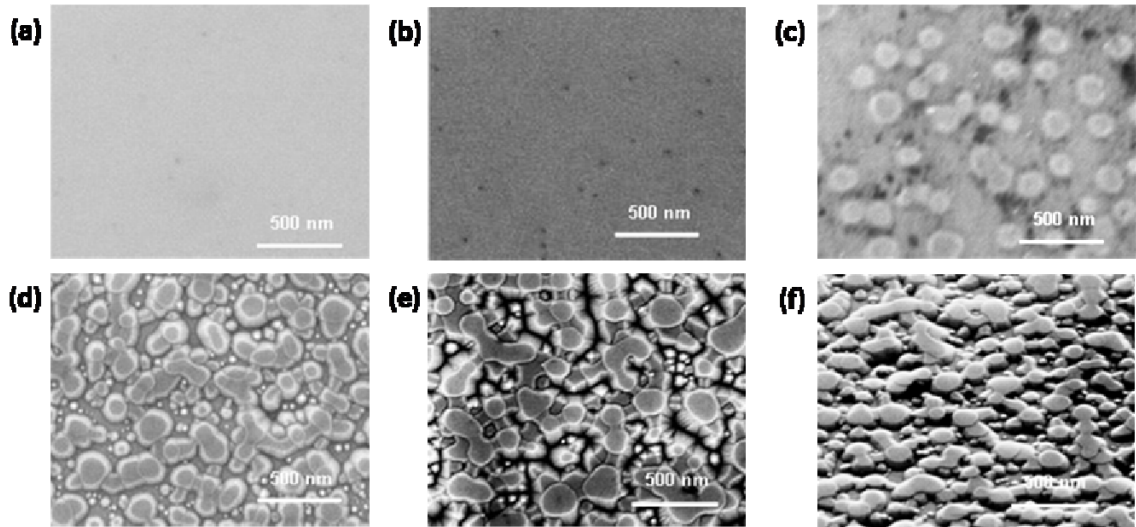
Figure 4-4. SEM images showing the surface morphology of ISST-treated samples with different ISST times (a) 0 sec, (b) 60 sec, (c) 150 sec, (d) 300 sec, (e) 600 sec. The bird's eye view of the 300 sec sample in (f) clearly shows nano-scale truncated cone structures.
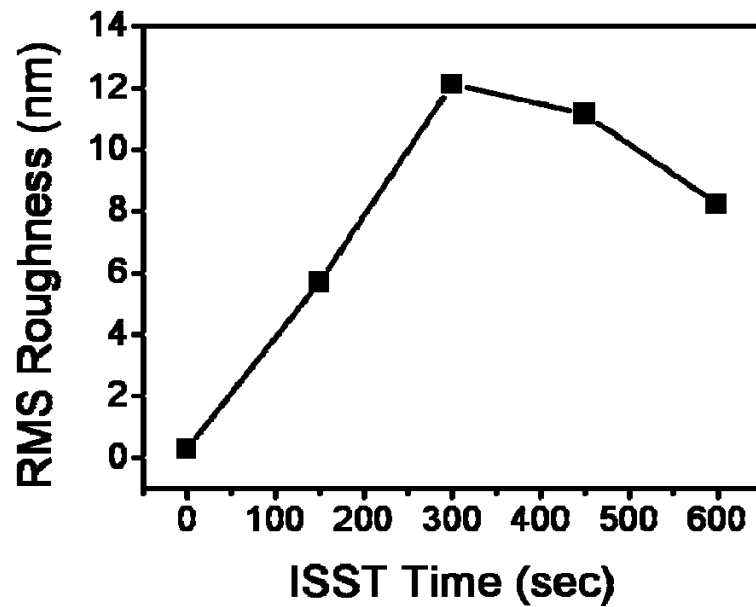
Figure 4-5. RMS surface roughness versus ISST time.

4.1.3 Mechanism of *In Situ* Silane Treatment

In this subsection, we investigate the mechanism for *in situ* silane treatment. As mentioned in 3.1.1, several mechanisms have been introduced including porous Si_xN_y deposition [78-80], etching model [83], and anti-surfactant model [81, 82]. Because the surface roughening was observed even without a GaN overlayer, it is unlikely to be the anti-surfactant model. We have conducted surface analysis to gain a fundamental understanding of the ISST mechanism. Although the conclusion still requires further atomic scale analysis, the surface roughness data shown in Figure 4-5 has supported the etching model. One major challenge in surface analysis is to search for the signature of any porous monolayer-thick Si_xN_y film at the ISST interface. So far, we have not been able to prove the existence of Si_xN_y deposition during the ISST process.

4.1.3.1 Experiment 1: *In Situ* Silane Treatment With and Without Silane Flow

First, we investigated whether silane was a functional agent in the ISST process. Two samples were prepared, one with 5 minute ISST and the other without the SiH_4 flow but with the rest of conditions the same. The AFM images in Figure 4-6 reveal that the surface of the sample with 5 minute ISST was transformed into nano-scale structures, but that of the sample without SiH_4 remained smooth. This implies that silane is responsible for the surface roughening.
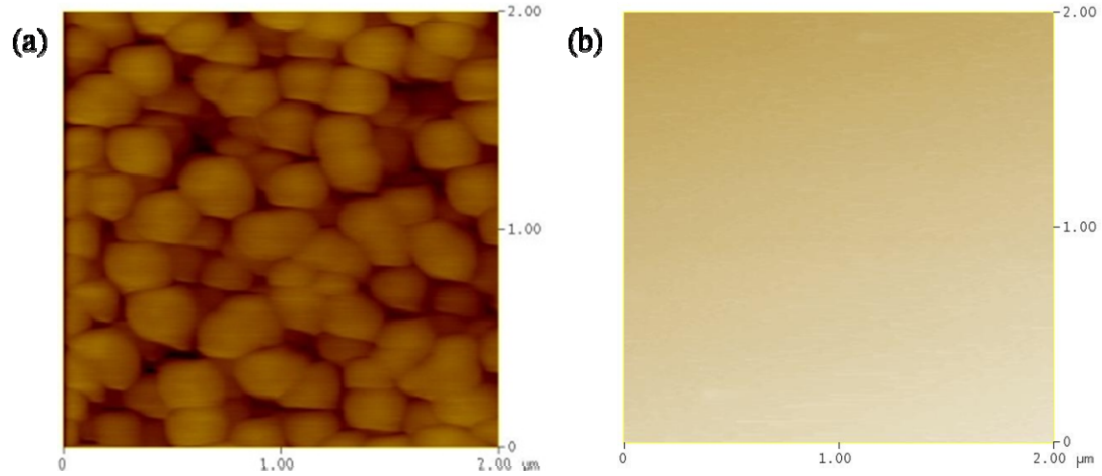
Figure 4-6. AFM images of two samples: (a) ISST for 5 min and (b) ISST but no SiH$_4$ flow for 5 min.

4.1.3.2   Experiment 2: Elemental Analysis of ISST-treated Surface Using EDX

Energy dispersive x-ray spectroscopy (EDX) with an ultra thin window (UTW) detector was used for the elemental analysis of an ISST treated surface. Two samples were investigated, one with 5 minute ISST and the other without ISST. The results depicted in Figure 4-7 show that both samples have almost identical elemental traces in which Si element was not observed on each examined surface. These results are opposite to the observation of Datta et al. in which they confirmed *non*-uniform Si distribution at the interface between sapphire and GaN [80]. However, EDX itself has some technical limitations. EDX is generally suited to detecting elements of high atomic number. Additionally, a specimen must be prepared with a few hundred angstroms thickness for an accurate quantitative analysis. Due to the small thickness of the Si$_x$N$_y$ film that can be possibly deposited on the ISST-treated samples, an EDX measurement may not elucidate

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the existence of Si atom on the surface. Therefore, different elemental analysis must be performed.
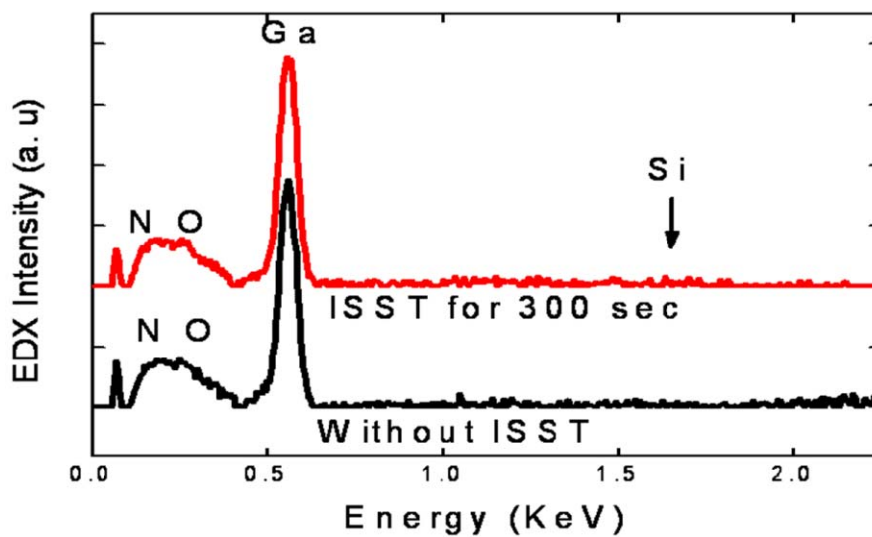
Figure 4-7. EDX data of two samples, one with 5 min ISST and the other without ISST.

4.1.3.3 Experiment 3: Elemental Analysis of ISST Surface Using XPS

Another elemental analysis was performed using x-ray photoelectron spectroscopy (XPS; Katos Axis Ultra XPS). Compared to EDX, XPS is a surface technique which can provide detailed elemental information of a sample within 30 nm from the surface. Four samples, each with a 7 mm x 7 mm size, were prepared as follows:

(i)   Si (111) wafer

(ii)   GaN template

(iii)   1.2 nm SiN_x deposition on GaN template

(iv)   5 minute ISST without SiH_4 flow on GaN template

(v)   5 minute ISST on GaN template

A Si (111) wafer and a 1.5 μm GaN template were used as control samples. For a reference sample, a 1.2 nm-thick SiN_x layer was deposited on a GaN template using plasma-enhanced chemical vapor deposition (PECVD). The measurement results were summarized in Figure 4-8. Figure 4-8 (a), (b), and (c) show the clear difference of Si (111) sample from the rest. In the Si sample, the silicon elemental trace was observed as evidenced by Si 2s or Si 2p (at 99 eV) and Si 2p 2/3 (at 149 eV). However, we did not observe any silicon trace even in the sample with an intentionally deposited thin SiN_x layer. The peak at 154 eV in Figure 4-8 (c) corresponds to a rare earth element, dysprosium (Dy) 4p, 4p 3/2, and 4d 5/2. This Dy element detection may result from

contaminations during PECVD related processes. Hence, we proceeded with another technique, electron energy loss spectroscopy.
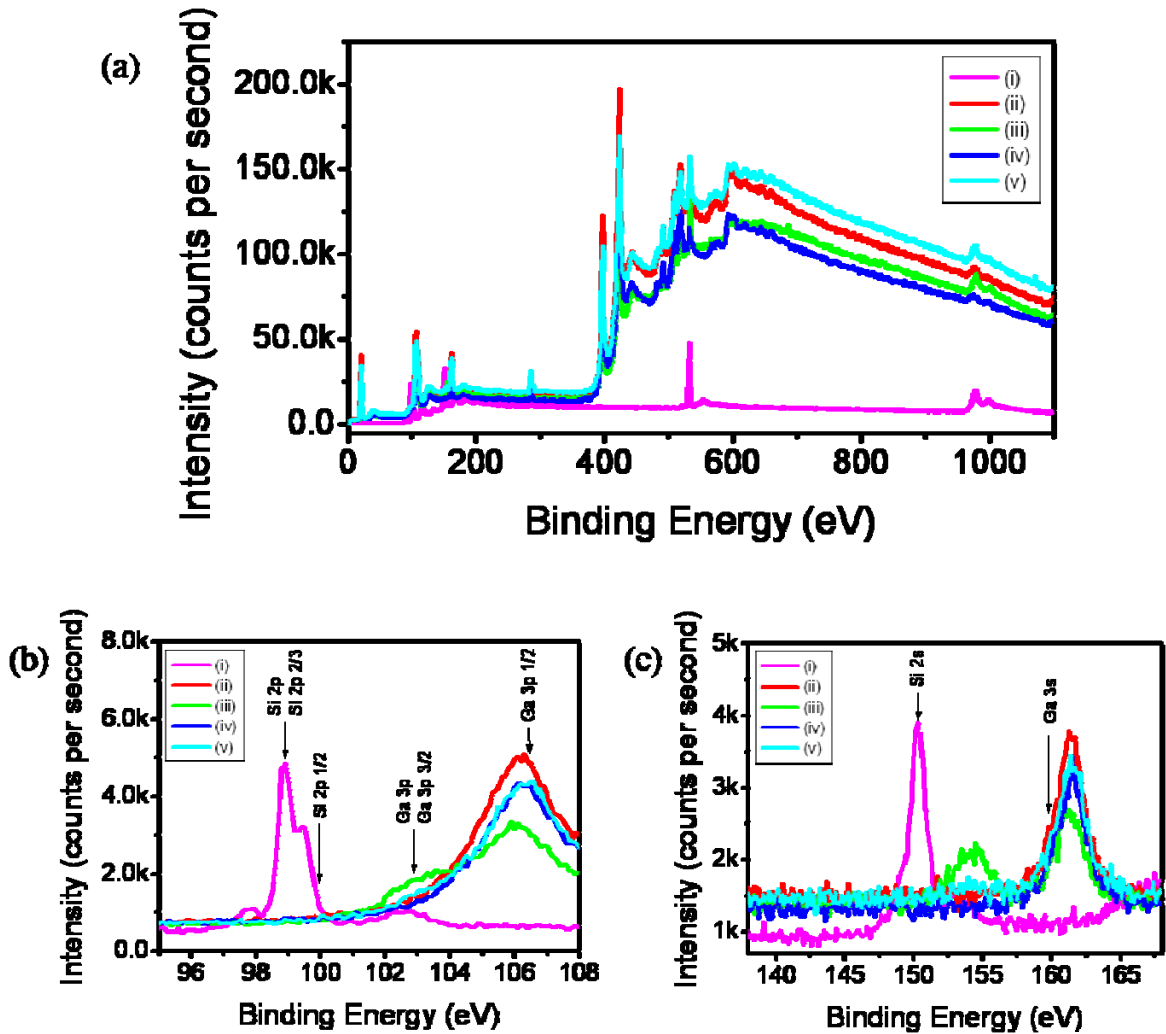
Figure 4-8. XPS data of the samples: (i) Si (111) wafer, (ii) GaN template, (iii) 1.2 nm SiN_x on GaN, (iv) 5 min ISST without SiH_4 flow, and (v) 5 min ISST on GaN.

4.1.3.4 Experiment 4: Elemental Analysis of ISST-treated Surface Using EELS

Using electron energy loss spectroscopy (EELS), an ISST-treated sample was examined with a spatial resolution < 1 nm. The focused electron beam size of the EELS is 2 Å which is small enough to detect a Si atom. For the analysis, a sample was prepared as follows. A 1.5 μm-thick GaN template was grown on a *c*-plane sapphire substrate and then 5 minutes of ISST was performed. Subsequently, a 3.9 μm GaN layer was overgrown on the treated surface. A standard transmission electron microscopy (TEM) specimen preparation method was applied on the sample. The specimen was bonded on a Si wafer and then cut into small pieces by a dicing saw. Afterwards, the sample was mounted on a molybdenum ring and then thinned by manual grinding and ion milling. As shown in the TEM image of Figure 4-9 (a), the sample was scanned along a 0.4 μm long line (shown by the green line in the figure) across the ISST interface. The EELS spectrum and detection data were shown in Figure 4-9 (b) and (c), respectively. Although there are small shoulders of Si trace along the inspected line, the number of electrons counted stays almost the same along the inspection line. This is attributed to a possible contamination either during the material growth or during the TEM specimen preparation, in particular during ion milling. We argue the Si trace is unlikely to have originated from the reactor contamination because the surface morphology change during ISST is unambiguous. During ion milling, Si atoms, which were bombarded by ions and detached from the bonded Si wafer, could be exposed to the chamber and then they might be re-deposited onto the specimen surface. Hence, currently we are conducting another EELS analysis by replacing the silicon mount with a sapphire mount. The use of a sapphire mount is

expected to minimize the silicon contamination during the TEM specimen preparation.

Further analysis is currently underway.
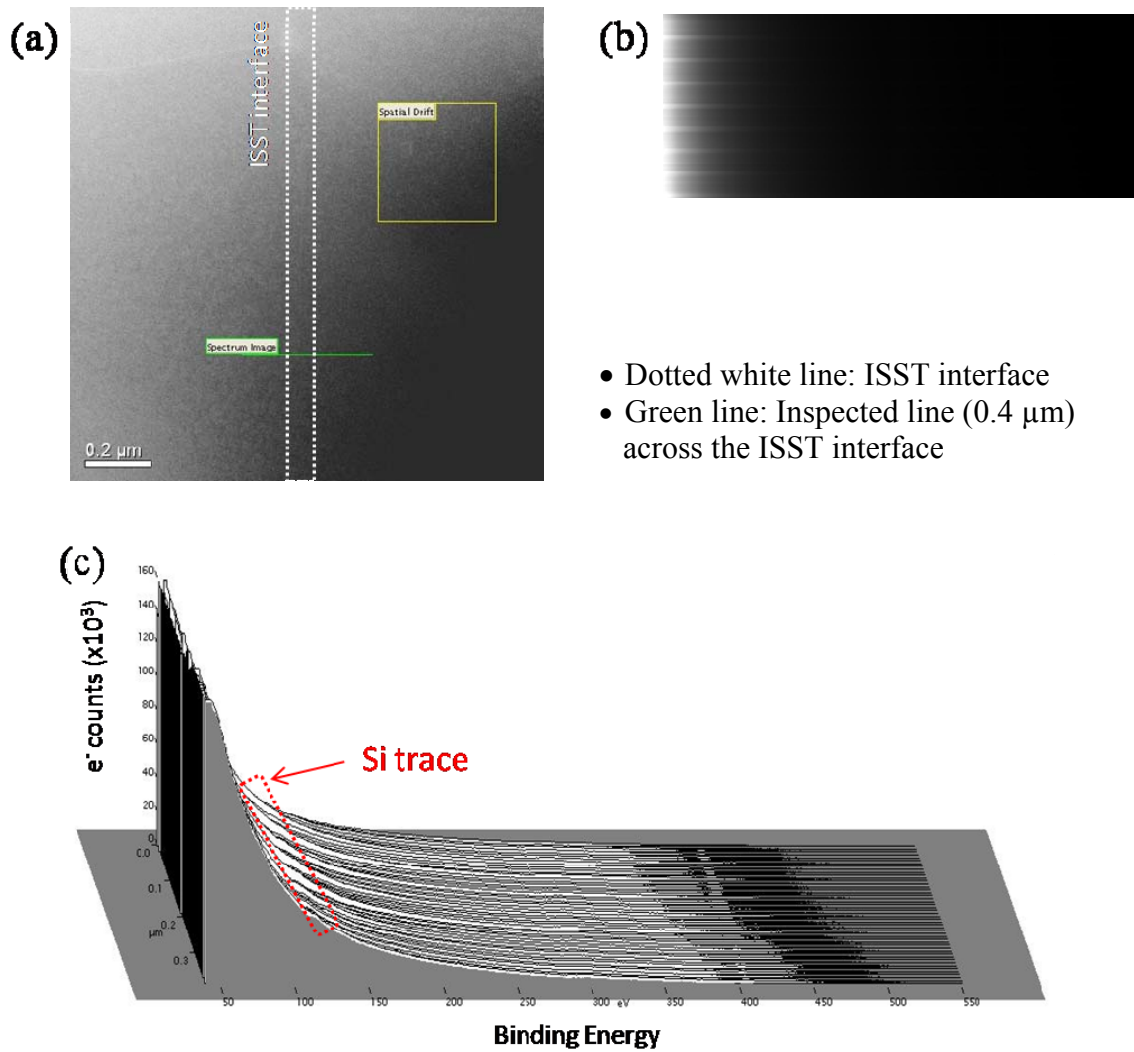
Figure 4-9. EELS analysis: (a) TEM image of inspected region, (b) EELS spectrum, and (c) EELS data.

4.1.4   Threading Dislocation Density Reduction Using *In Situ* Silane Treatment

Although the mechanism of ISST is not yet clear, the effect of ISST on TD density reduction has been confirmed. The as-grown sample used for EELS analysis had a 3.9 μm-thick GaN overlayer grown on the ISST-treated GaN surface. We have performed cross-sectional TEM using JEOL 2010F Field Emission Gun Analytical Electron Microscope. The results (Figure 4-10) showed nearly an order of magnitude TD density reduction, from 10^8/cm^2 to 10^7/cm^2, in the GaN overlayer.
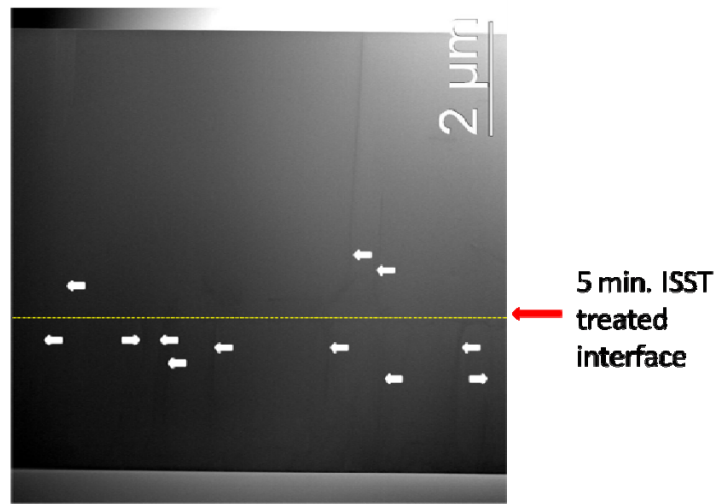
Figure 4-10. TEM image (JEOL 2010F) showing TD (marked by white arrows) density reduction above the ISST-treated interface.

Additionally, the overgrown GaN was characterized by photoluminescence (PL) and x-ray diffraction (XRD) compared with a GaN template without ISST. Room temperature (RT; 300 K) PL measurements were performed using a He-Cd laser with 325

nm excitation with a focused spot size of approximately 100 μm. The PL signals of both samples were dominated by a near band edge (NBE) emission at 362 nm. The GaN on ISST-treated surface and the GaN template have comparable linewidth of 6.57 nm and 5.99 nm, respectively. The intensity of the overgrown GaN becomes 31% stronger than that of the GaN template (Figure 4-11). The measured XRD data were summarized in Table 4-2. The reduction of both (002) and (102) rocking curve linewidths was attributed to the reduction of the density of defects.
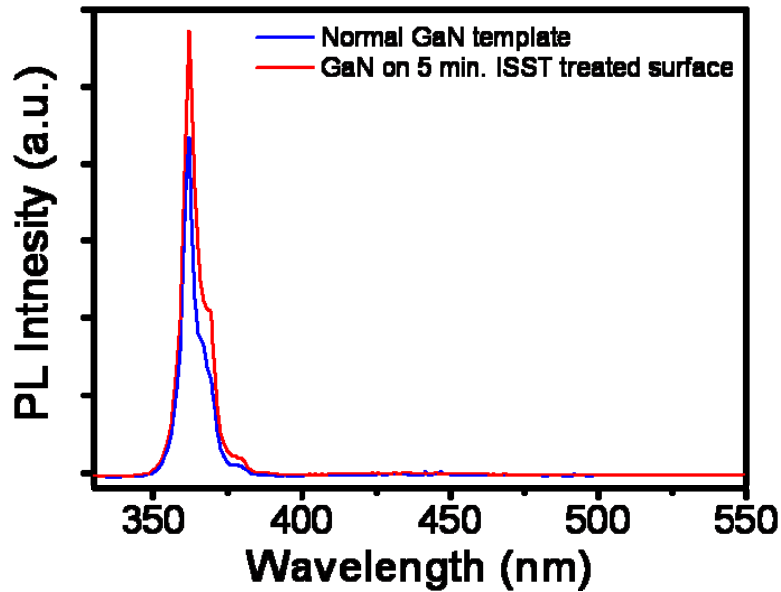
Figure 4-11. Photoluminescence comparison of a normal GaN template to a GaN overlayer grown on a 5-minute ISST-treated surface.

Sample Description	(002) rocking	(102) rocking
Normal GaN Template	224.7 arcsec	371.0 arcsec
GaN on 5 min. ISST-treated surface	172.8 arcsec	255.6 arcsec

Table 4-2. Summary of XRD measurements for GaN grown on an ISST-treated surface.

In conclusion, from TEM, PL, and XRD characterizations, ISST is an effective technique for TD density reduction in GaN materials.

4.2   High Temperature Overgrowth

4.2.1   Formation of Nano-structured *Semi*-polar Plane

As mentioned at the beginning of this chapter, a combination of ISST and HTO can produce nano-structured *semi*-polar (NSSP) planes on a GaN template. Figure 4-12 illustrates the formation of NSSP plane formation along with the SEM images showing surface morphology evolution after each step. The ISST was performed for 5 minutes under 40 sccm of diluted SiH_4 flow and 2.5 slm of NH_3 at 1030˚C.

After the ISST process, substrate temperature and reactor pressure were elevated to 1100 ˚C and 600 torr to grow a thin GaN layer for 10 minutes. This specific process was referred to as high temperature overgrowth (HTO). As shown in Figure 4-12 nano-scale sharp *semi*-polar planes were formed after HTO. It is attributed to the growth rate anisotropy of GaN, which transforms the truncated cone structures of ISST-treated surface into a *semi*-polar surface. At high temperature and high pressure, the growth rate of *semi*-polar planes (10-11) and (11-22) are slowest compared to other planes. This was verified by SEM and cross-sectional TEM (Figure 4-12 and Figure 4-13) from the formation of sharp (10-11) and (11-22) *semi*-polar planes.
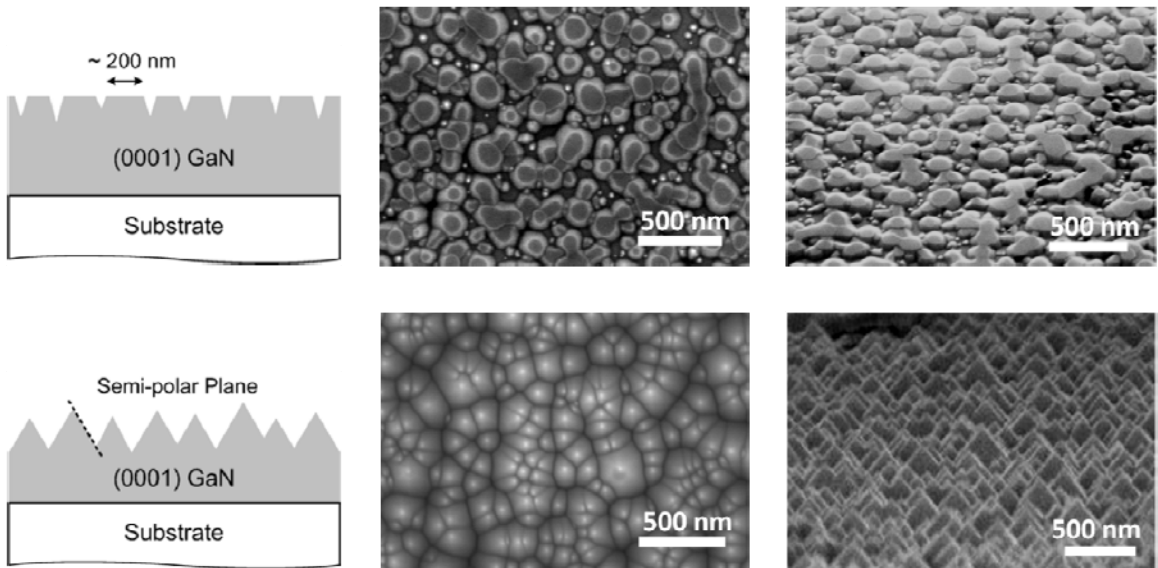
Figure 4-12. Illustrations of the NSSP plane formation: surface morphologies after 5 min ISST (upper) and after HTO (lower).

The as-grown sample was prepared with a standard TEM specimen preparation technique. The wafer of interest was glued on another wafer by an adhesive. The orientation of cutting edge was carefully controlled because there can be a measurement error if the crystal orientation is misaligned. The bright field TEM images in Figure 4-13 showing the cross-section of nano-scale *semi*-polar pyramids, and the crystal angle of each structure was measured. Two different *semi*-polar planes, (10-11) and (11-22), were observed on the same NSSP GaN template. If an InGaN active region is deposited on such planes, approximately 85% of internal electric field can be suppressed in the green and yellow emission range compared to an active region grown on *c*-plane GaN [71].

Therefore, the internal quantum efficiency of NSSP quantum wells is expected to be improved. Further details will be discussed in the next chapter.
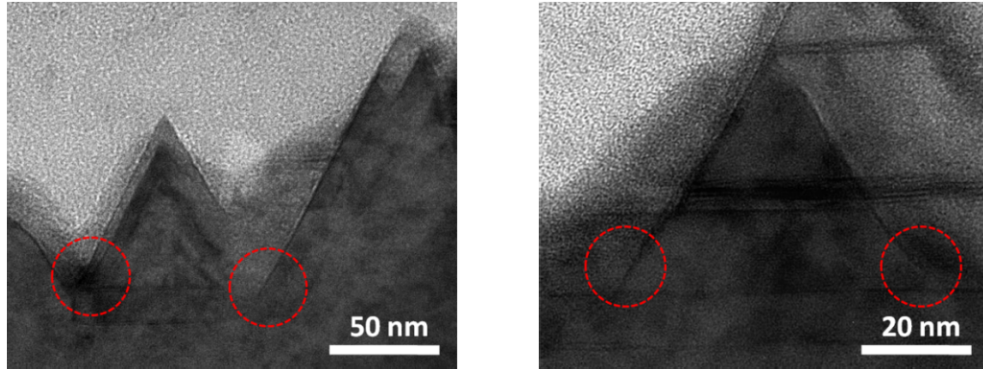
Figure 4-13. TEM images showing the cross section of NSSP GaN template. Two crystal angles are observed: 62.5° (left) and 57.2°(right) which correspond to (10-11) and (11-22) *semi*-polar planes.

4.3 Optical Properties of Nano-structured GaN

4.3.1 Properties of *In Situ* Silane Treatment Treated GaN Template

Optical properties of an ISST-treated GaN surface were examined using PL measurement at room temperature. Three samples with different treatment times (0 sec, 150 sec, and 600 sec) were characterized. As shown in Figure 4-14, the emission from each sample shows a band-edge emission at 3.42 eV and broad yellow band emission (YBE) centered at around 2.2 eV. Although it is still controversial, YBE has been explained by a transition between a shallow donor state and a deep acceptor state. A gallium vacancy (V_{Ga}), an acceptor type defect, is believed to be the main source for this

transition [41, 85, 86]. The gallium vacancy introduces a deep acceptor level around 1.1 eV above the valance band and the transitions between the shallow donor and the deep acceptor levels give rise to YBE (Figure 4-15). With an increasing ISST time, YBE becomes increasingly stronger while the increase in band-edge emission is more gradual with time. This is explained using the etching model of ISST. During ISST, the etching of a GaN is related to the decomposition of Ga-N bonds followed by desorption of Ga and N atoms from the surface. Because the ISST process is performed under NH_3 environment at a high temperature (1030°C), V_{Ga} can be generated during the process. Hence, if the duration of treatment becomes longer, more V_{Ga} will be generated.
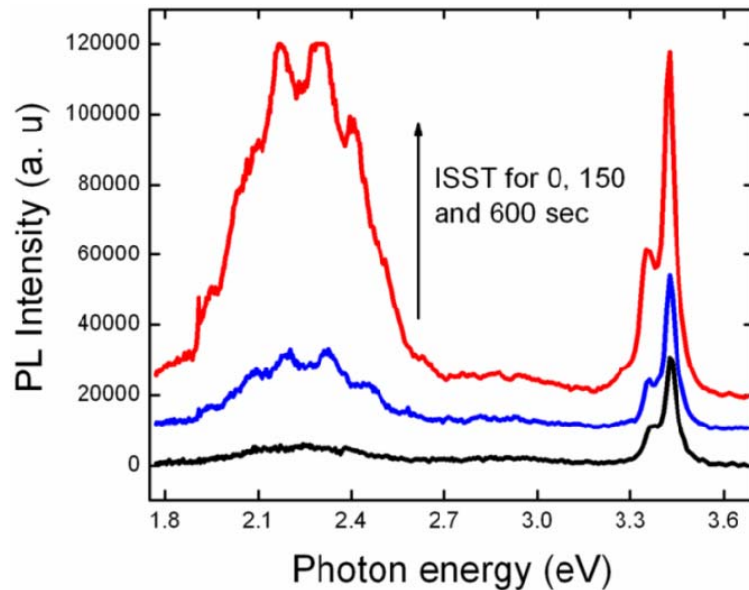
Figure 4-14. Room temperature photoluminescence of ISST-treated GaN templates with different ISST times.
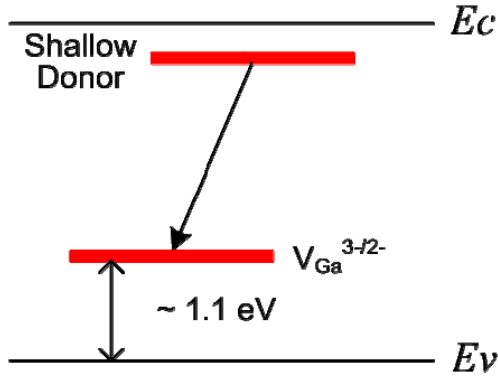
Figure 4-15. Illustration of a possible origin for yellow band emission in GaN (after Ref. [41]).

4.3.2 Optical Properties of Nano-structured *Semi*-polar GaN Template

The optical properties of an NSSP GaN template were examined using RT PL measurement in comparison with a 2 μm-thick *c*-plane GaN template. As shown in Figure 4-16, the luminescence from each sample was dominated by a band-edge transition at 3.42 eV (362 nm). The comparable linewidths of 41.2 meV and 36.6 meV were observed for the NSSP GaN and normal GaN templates. The intensity of band-edge emission in the NSSP GaN template was about 3 times stronger than that in the GaN template. We attribute this enhancement to two effects: the reduction of total internal reflection and the Bragg effect. As described in section 1.3.3, surface texturing can reduce total internal reflection at the sample surface. As will be shown in Chapter 7, ISST-treated surface can increase luminescence by a factor of two. This factor alone, however, does not explain a factor of 3 enhancement in luminescence. The Bragg effect may account for the rest. Each nano-scale pyramidal structure is around 50 − 100 nm which is between $\lambda/4n$ to $\lambda/2n$ where λ is the emission wavelength and n is the refractive

index of GaN. These nano-structures can enhance surface coupling of light propagating at a shallow angle with respect to the sample surface.
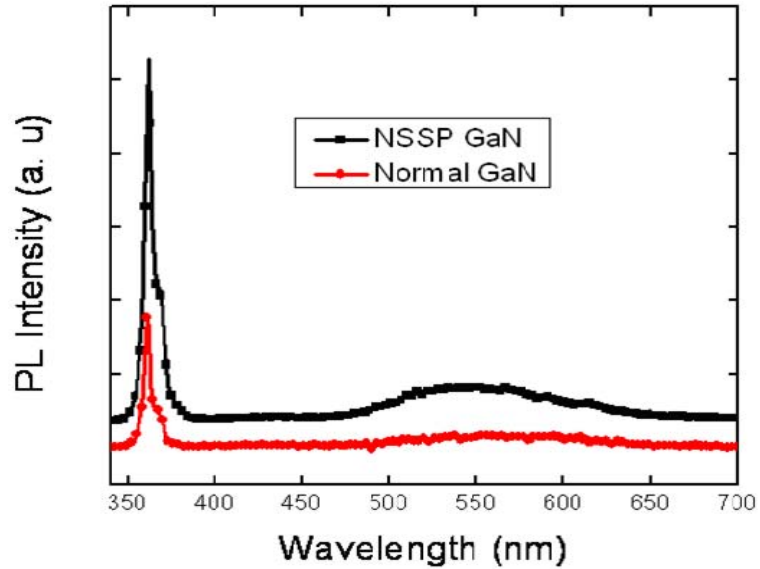
Figure 4-16. Room temperature photoluminescence spectra of NSSP GaN template and normal *c*-plane GaN template.

Yellow band emission was observed for both samples. Compared to the NSSP template, the *c*-plane sample exhibited a lower yellow band luminescence. As discussed in the previous section, the creation of gallium vacancies during ISST may increase the YBE.

4.4   Summary

In this chapter, novel cost-effective approaches to fabricating nano-structured GaN were demonstrated. In an *in situ* silane treatment process, a GaN surface is treated by silane under ammonia environment. *In situ* silane treatment can create randomly distributed nano-structures on a planar GaN surface. The surface roughness as well as surface morphology can be controlled by the treatment time. The RMS surface roughness peaked at around 5-minute ISST. To investigate the underlying mechanism of ISST, different analytical methods have been performed. One order of magnitude TD density reduction was observed in a GaN overlayer grown on ISST-treated GaN surface. However, further characterizations are still required and are currently underway.

The combination of ISST and HTT can generate nano-structured *semi*-polar GaN. Two *semi*-polar planes, (10-11) and (11-22), coexist as confirmed by TEM. Increased YBE was observed for each of ISST treated GaN and NSSP GaN, which was attributed to the increase of gallium vacancies during ISST.

CHAPTER 5

NANO-STRUCTURED *SEMI*-POLAR InGaN LEDs

The efficiency of an InGaN light-emitting diode (LED) is critically dependent on internal electric field (IEF) exhibiting in its active region. As a result, the crystallographic orientation of the active region in a LED is a key factor for the LED performance. As discussed in Chapter 2, InGaN LEDs grown on *non*-polar and *semi*-polar GaN templates have been shown to possess improved internal quantum efficiency (IQE) due to reduced IEF [31]. However, issues such as wafer cost and small wafer size have limited these approaches from large scale production. For these reasons, commercially available LEDs today are still fabricated on polar *c*-plane substrates. In this chapter, a novel InGaN LED structure based on a nano-structured *semi*-polar (NSSP) GaN template as described in Chapter 3 will be investigated. This new structure can be fabricated on a mature *c*-plane substrate including low cost sapphire without any *ex situ* patterning. In the following, we will discuss the fabrication and characterization of an NSSP InGaN LED.

5.1 InGaN/GaN Active Region on NSSP GaN

Figure 5-1 illustrates the procedure of fabricating an NSSP InGaN LED. Starting from an NSSP GaN template, InGaN/GaN multiple quantum wells (MQWs) are deposited. A p-type layer is overgrown on the MQWs to form a p-n junction and planarize the surface of the device. The details of forming an NSSP GaN template have been given in Chapter 4.
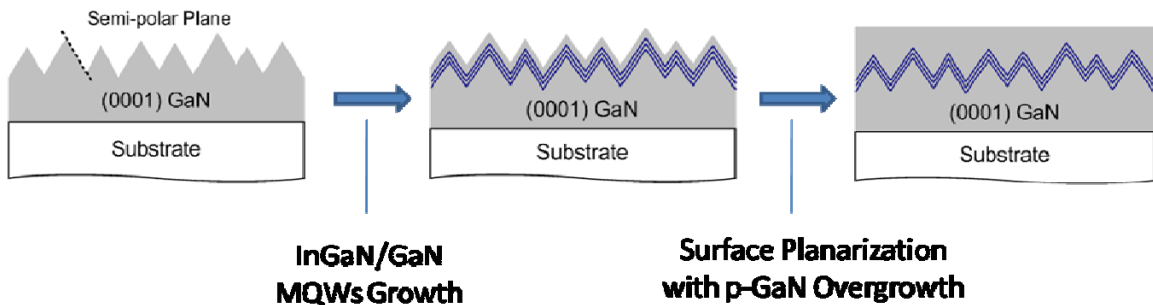
Figure 5-1. Illustration of an NSSP InGaN LED fabricated on NSSP GaN template.

5.1.1 NSSP InGaN/GaN MQWs

The characteristics of InGaN MQWs grown on an NSSP GaN template were investigated in comparison with MQWs grown on a planar GaN template. For the planar MQWs, a 2 μm-thick GaN epilayer was deposited on a *c*-plane sapphire substrate. Subsequently, the substrate temperature was lowered to 780°C for the growth of MQWs using a nitrogen carrier gas at 400 Torr reactor pressure (Table 5-1). For the NSSP

MQWs, almost the same growth processes were performed except the insertion of ISST and HTO for the formation of NSSP GaN. The nominal thicknesses of InGaN quantum well and GaN barrier are 3 nm and 10 nm, respectively, as confirmed by transmission electron microscopy (TEM). 17Cross-sectional TEM image showing NSSP MQWs.Figure 5-2. 17Cross-sectional TEM image showing NSSP MQWs. shows the cross-sectional TEM image of the as-grown NSSP InGaN MQWs. The three quantum wells were clearly seen and marked by white arrows. From TEM, the crystal orientation of the NSSP MQWs was shown to consist of two different *semi*-polar planes: (10-11) and (11-22). According to theoretical calculations, IEF in either of these two *semi*-polar planes is only around 15% of that in *c*-plane MQWs [71].

Layer	Growth Temp. (°C)	Reactor Pressure (Torr)	TMG Flow (μmol/min)	TMI Flow (μmol/min)	NH₃ Flow (mmol/min)	V/III Ratio	Growth Rate (nm/Hr)	Thickness (nm)
UID GaN	1040	200	125	-	118	942	1270	1970
InGaN	780	400	3.9	16.1	178	8901	60	3
GaN Barrier	780	400	14.4	-	178	12427	60	10

Table 5-1. Summary of MQW growth condition.
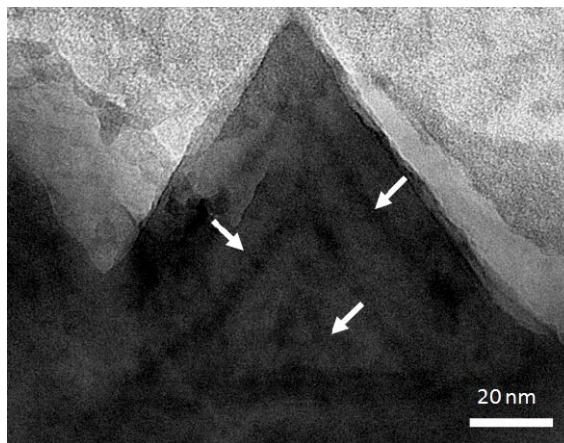
Figure 5-2. 17Cross-sectional TEM image showing NSSP MQWs.

5.1.1.1　Photoluminescence study of NSSP InGaN/GaN MQWs

The optical properties of NSSP MQWs were characterized by excitation- and temperature- dependent photoluminescence (PL) measurements. By performing these experiments, the IEF and IQE in an NSSP active region can be experimentally analyzed. All measurements were performed in comparison to a polar *c*-plane MQW sample.

Figure 5-3 shows the comparison of PL intensity for both samples at room temperature (RT; 300 K). It can be seen that the PL intensity of the NSSP MQWs is 3.3 times stronger than that of the polar MQWs. This enhancement has been explained in Section 3.3.3 for the NSSP GaN template.
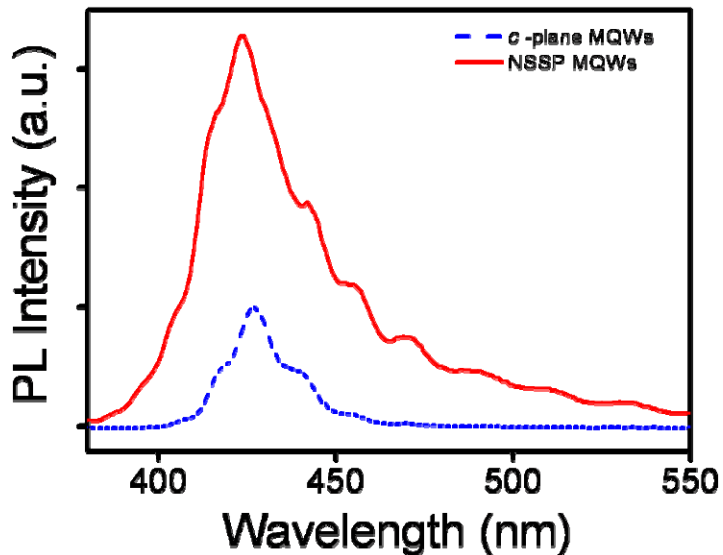
Figure 5-3. Photoluminescence intensity comparison of NSSP and polar MQWs at room temperature.

The PL peak wavelengths of both samples were measured at various excitation intensities and shown in Figure 5-4. The peak wavelength of polar MQWs blue shifted as the excitation intensity increased, which was attributed to the quantum confined Stark effect (QCSE) caused by IEF. Stronger excitation increases the polarization charge screening in the quantum well and reduces the IEF in polar MQWs. In contrast, the peak wavelength of NSSP MQWs remained nearly a constant regardless of increasing excitation intensity, confirming the suppression of IEF.
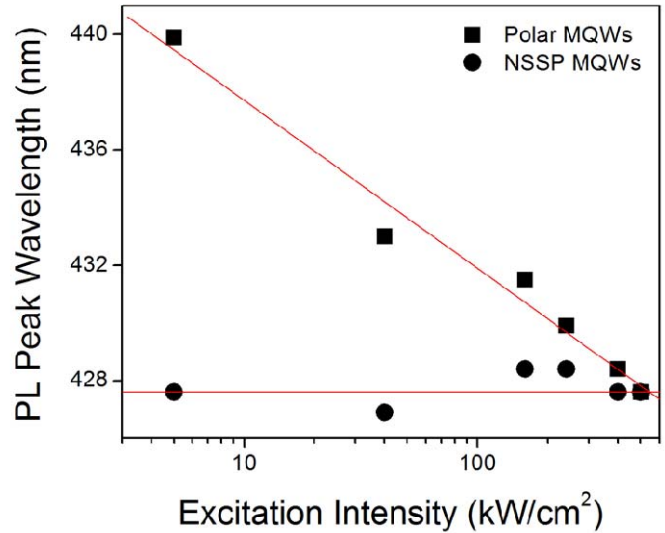
Figure 5-4. Photoluminescence peak wavelength as a function of excitation intensity. The two straight lines are for guides only.

Figure 5-5 shows the results of temperature dependent PL measurements. By assuming the IQE is unity at low temperature (10 K), the IQEs of NSSP and polar MQWs can be deduced to be 25% and 19%, respectively, at 5 kW/cm^2 excitation intensity; and 21% and 16%, respectively, at 500 kW/cm^2 excitation intensity (Table 5-2). The

suppression of the IEF in NSSP active region improves the IQE by nearly 31%. This value is expected to be further improved by careful optimizations of the growth conditions.
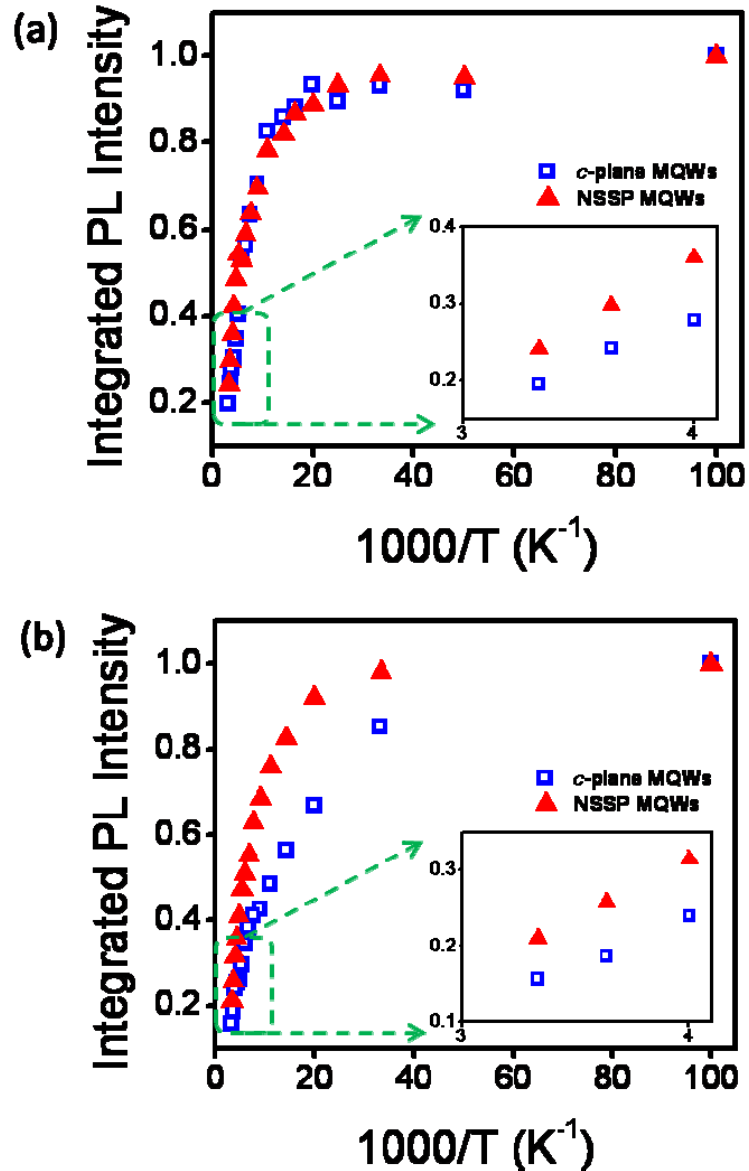
Figure 5-5. Arrhenius plots obtained from temperature dependent PL for NSSP and polar samples with excitation intensity of (a) 5 kW/cm^2 and (b) 500 kW/cm^2.

Excitation Intensity (kW/cm^2)	IQE of NSSP MQWs (%)	IQE of c-plane MQWs (%)	IQE Improvement of NSSP MQWs compared to c-plane MQWs (%)
5	25	19	31.6
500	21	16	31.3

Table 5-2. IQE comparison of NSSP MQWs and polar MQWs.

5.1.1.2 Time-resolved Photoluminescence Study of NSSP InGaN/GaN MQWs

To further characterize the optical properties of an NSSP active region, the NSSP MQWs and c-plane polar MQWs were investigated by time-resolved photoluminescence (TR PL) using a triple-frequency output of a mode-locked titanium-sapphire laser (Spectra-Physics Tsunami). The excitation wavelength was centered at 260 nm with a 130 fs pulse width and a repetition rate of 80 MHz. The average laser intensity at the sample surface was estimated to be 1 kW/cm^2. The room-temperature TR PL signal as shown in Figure 5-6 was dispersed through a 0.5 m monochrometer and was recorded by a silicon-based single photon detector (id Quantique id-100) with a timing resolution of 50 ps. The monochrometer grating was tuned to the peak emission wavelength of each sample. To extract radiative and *non*-radiative lifetimes, the following equations were used:

$$\eta_{Int} = \frac{1}{1 + \tau_r / \tau_{nr}}$$

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}}$$

Equation 5.1

where τ_{PL}, τ_r, and τ_{nr} are PL, radiative, and *non*-radiative lifetimes, respectively; η_{Int} is IQE, which was obtained from the temperature dependent PL measurement with the assumption that η_{Int} was 100% at low temperature (10 K). The results are summarized in Table 5-3. It can be perceived that, although the radiative lifetime was reduced considerably in the NSSP sample due to the absence of QCSE, the *non*-radiative lifetime was also reduced. This explains why only a 31% improvement in IQE was observed in the NSSP sample while a factor of three improvement in IQE was previously measured in *semi*-polar InGaN/GaN MQWs grown on a micro-scale pyramidal GaN surface using SAE as discussed in Chapter 3 [31]. The physical mechanism of the decreased *non*-radiative lifetime is still under investigation. However, it can be partly attributed to the generation of gallium vacancies during the ISST process. Because the gallium vacancies were not in the InGaN active region, it is believed that the *non*-radiative recombination can be further minimized by optimizing the HTO conditions after the ISST process and therefore annealing the defects.
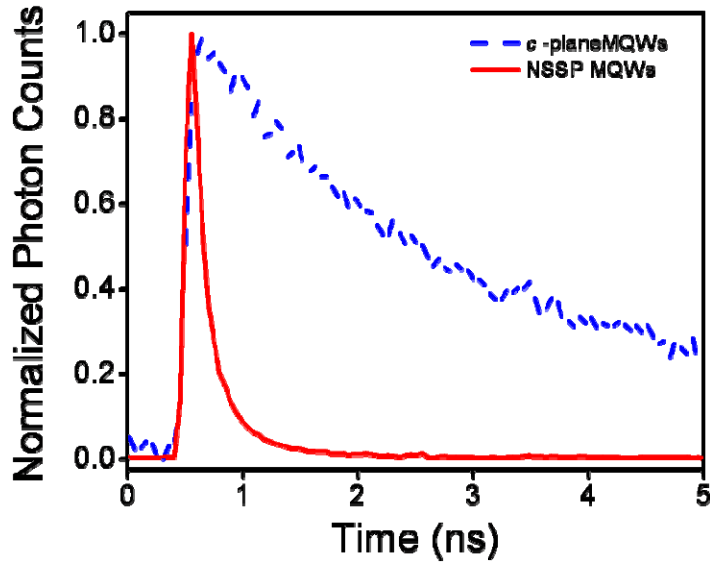
Figure 5-6. Comparison of room temperature TRPL between NSSP and polar MQWs.

	NSSP MQWs	c-plane MQWs
η_{Int}	25 %	19 %
τ_{PL}	0.16 ns	2.90 ns
τ_r	0.64 ns	15.26 ns
τ_{nr}	0.21 ns	3.58 ns

Table 5-3. Summary of TR PL results.

5.1.2   NSSP InGaN/GaN LEDs

5.1.2.1   Planarization

In this section, an electrically injected InGaN LED structure based on NSSP GaN template will be examined. The procedure of the epitaxial growth of NSSP LEDs was already illustrated in Figure 5-1. After the MQW growth, a 230 nm of Mg-doped p-type

GaN epilayer was deposited at 1000˚C. The p-type dopants were activated by a thermal activation process at 780 ˚C under N_2 ambient for 10 minutes. The measured doping concentrations of the n-GaN and the p-GaN layers were 4 x 10^{18}/cm^3 and 8.1 x 10^{17}/cm^3, respectively. The growth conditions used for all layers were very similar to those used in a planar LED except for the addition of ISST and HTO processes. The entire epitaxial sequence was performed in one shot starting from a two-inch *c*-plane sapphire substrate. No electron blocking layer was included to allow us to focus the studies on the optical and electrical properties of the nano-structured active region.

As shown in Figure 5-7, the as-grown LED surface has been mostly planarized except for a low density of micro-scale pits (3.3 x 10^5 /cm^2). These micro-scale pits are attributed to the threading dislocations reaching the surface although many of them disappeared during the p-GaN growth. Further optimizations of the p-GaN thickness and growth conditions are believed to be able to improve the surface morphology.
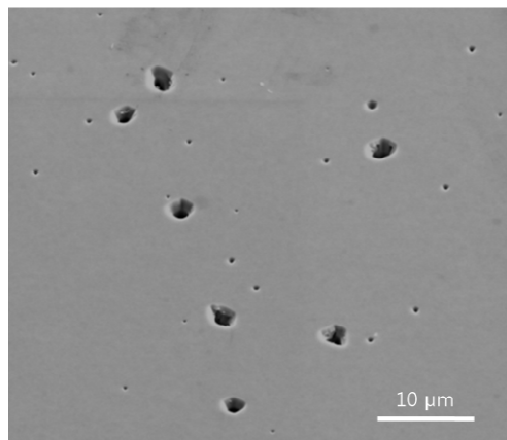
Figure 5-7. SEM image to show the surface morphology after p-GaN planarization.

5.1.2.2   LED Fabrication

The as-grown NSSP LED structure was fabricated using a simple top-light-emitting mesa structure (Figure 5-8). The mesa area was 350 μm by 350 μm and was defined by conventional photolithography and reactive ion etching (RIE; LAM 9400). A thin metal film consisting of 5 nm of Ni and 5 nm of Au was deposited across the entire mesa as a transparent electrode. After the p-ohmic contact formation, the sample was annealed at 450 °C for 10 minutes under N_2 environment using a rapid thermal annealing (RTA; JetFirst-150 RTP). 370 nm of Au and 380 nm of Ti/Au were deposited by an e-beam evaporator as p-type and n-type ohmic contacts, respectively. The details of the LED fabrication process are shown in the Appendix A.
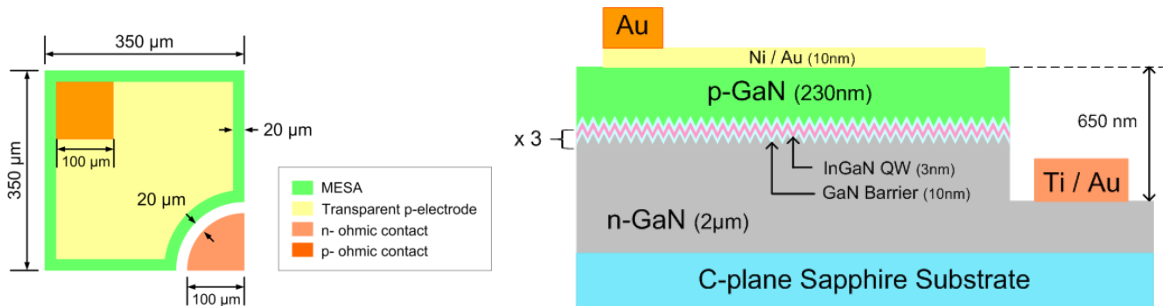
Figure 5-8. Device structure of NSSP LED grown on *c*-plane sapphire substrate: (left) top view, (right) cross sectional view.

5.1.2.3   Electrical and optical measurements

The fabricated LEDs were characterized by standard electroluminescence (EL) measurements at room temperature without intentional cooling. The EL spectra under a range of continuous-wave (CW) current injection are shown in Figure 5-9. The inset

shows the charge-coupled device (CCD) image of the device under current injection. Uniform light emission across the mesa was observed. The peak emission wavelength was ~ 543 nm and did not show any blue shift with increasing current. Instead, as shown in Figure 5-10, the peak wavelength showed a slight red shift (< 2 nm across the measurement range) possibly due to Joule heating. The absence of QCSE in the measurement range was attributed to the suppression of IEF in *semi*-polar MQWs and agreed well with previous results on the PL characterization of blue-emitting NSSP MQWs shown in Chap.5.1.1.1. The full-width-half-maximum (FWHM) EL linewidth increased slightly with increasing injection and was comparable to that of *semi*-polar green and yellow LEDs grown on *semi*-polar bulk GaN substrates [25, 26] .
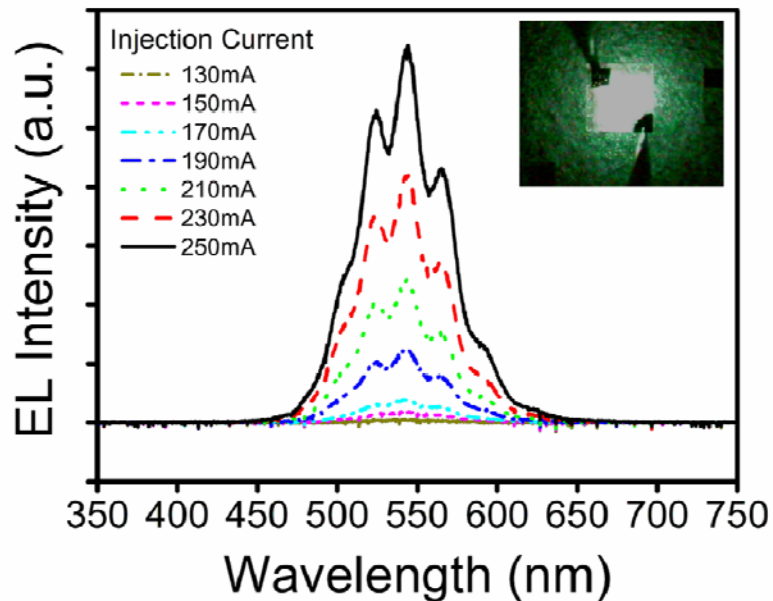
Figure 5-9. Electroluminescence spectra of NSSP LED for different injection currents.
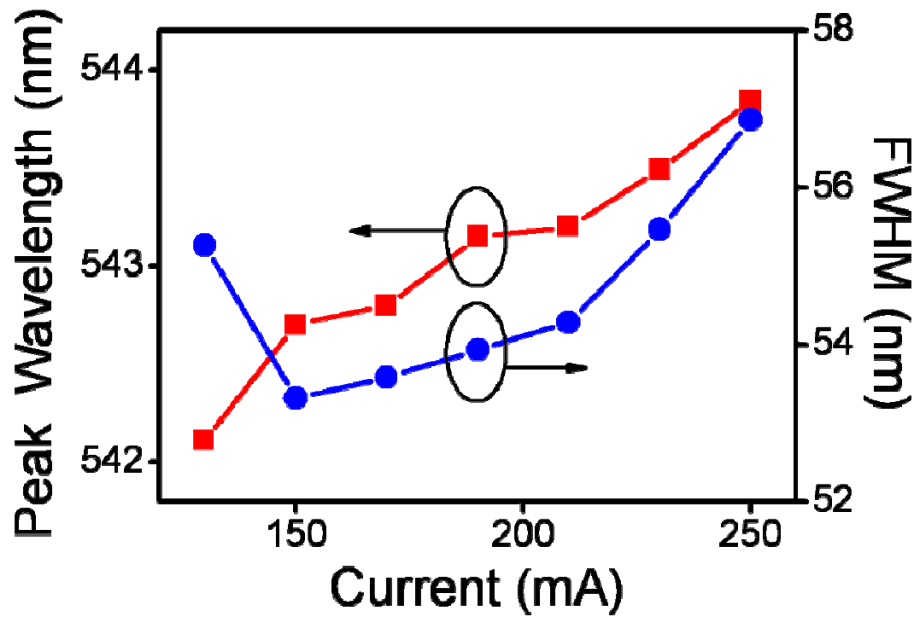
Figure 5-10. Peak wavelength and FWHM linewidth of EL spectra in NSSP LED.
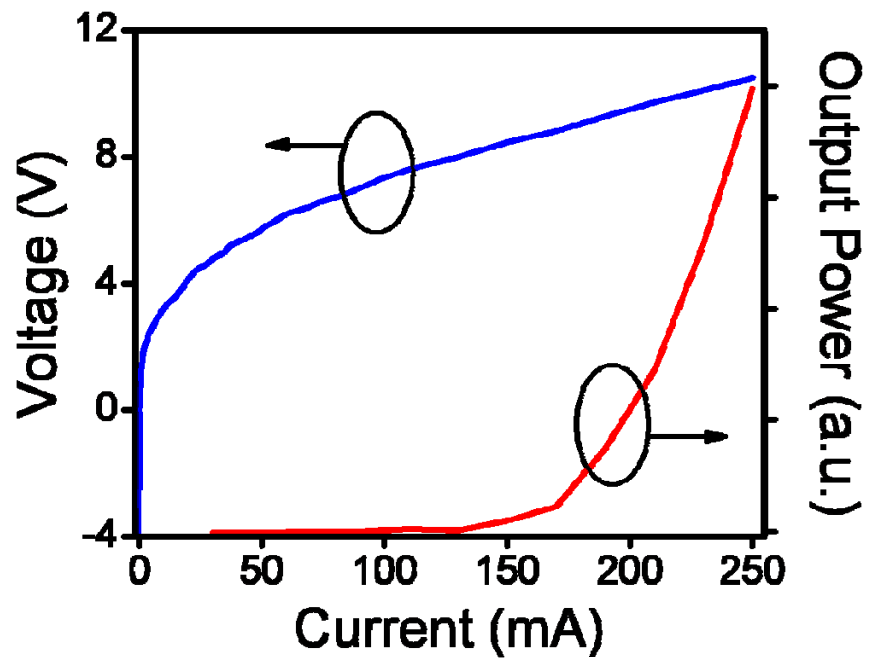
Figure 5-11. L-I and I-V curves of NSSP LED.

The I-V and L-I characteristics of NSSP LEDs are shown in Figure 5-11. The turn-on voltage was 4.2 V at 20 mA, and this high operating voltage is attributed to the un-optimized growth conditions of the NSSP template and the p-GaN current spreading layer. These micro-scale pits observed on the surface of LED (Figure 5-7) could also degrade the electrical properties possibly due to increased contact resistance. By optimizing the p-GaN layer thickness and planarization conditions, the formation of micro-scale pit can be minimized and therefore the electrical characteristics of the LED are expected to be improved.

5.2   Summary

In this Chapter, the properties of the NSSP light emitters were examined. Active regions were grown on NSSP GaN starting from a *c*-plane sapphire substrate. From RT PL, 31% enhancement in IQE was observed in NSSP MQWs as compared to *c*-plane planar MQWs. A further improvement of the IQE is possible as suggested by TRPL measurements. We believe an optimization of ISST and HTO conditions can considerably increase *non*-radiative lifetime.

Nano-structured *semi*-polar LEDs were fabricated using a conventional top-light-emitting structure and measured using standard characterizations, including EL, IV, and LI. To our best knowledge, this was the first *semi*-polar green LEDs grown on low cost *c*-plane sapphire substrates. The measured EL spectra showed negligible QCSE with a peak

wavelength around 543 nm. The EL linewidth was comparable to that of *semi*-polar

LEDs fabricated on *semi*-polar bulk GaN substrates.

CHAPTER 6

CURRENT SPREADING IN NANO-STRUCTURED *SEMI*-POLAR InGaN LEDs

As discussed in Chapter 1, strong piezoelectric field in *c*-plane InGaN light-emitting diodes (LEDs) severely limits their efficiencies for green/yellow emission. Devices fabricated on *semi*-polar and *non*-polar GaN have shown significant improvements in radiative efficiencies. The suppression of the internal electric field in *semi*-polar and *non*-polar LEDs also minimizes the shift of the emission wavelength with injection current, providing better color stability. In chapter 5, we demonstrated the first green *semi*-polar LED grown on *c*-plane sapphire substrate using a nano-structured *semi*-polar (NSSP) GaN template generated by the *in situ* technique.

In this Chapter, we will study the current spreading across the non-planar NSSP active region, which is crucial for device efficiency and reliability. To further investigate the electrical characteristics across the nano-structured active region, we have performed technology computer aided design (TCAD) simulations using Synopsys Sentaurus.

6.1 Staircase-Like Doping Profiles

To investigate the current spreading in the nano-structured region, p-i-n structures with different doping profiles were simulated as shown in Figure 6-1.. Because the internal electric field (IEF) is suppressed in the *semi*-polar active region, the simulation of simple p-i-n GaN hetero-structures is sufficient to elucidate the characteristics of current spreading to the first order. Simple top-down 2 dimensional (2D) structures were used for all three cases. In Figure 6-1., each color represents a different doping concentration. The planar doping profile can be achieved by growing a thin-layer of unintentionally doped GaN before performing the *in situ* silane treatment (ISST) and high temperature overgrowth (HTO) processes. The materials were assumed to be perfect, that is all non-ideal factors such as interface traps and defects were not considered. This is expected not to be an issue for the study of current spreading. The doping concentrations for p-type, intrinsic, and n-type from the top of each structure were set to be 5×10^{17} /cm^3, n-type 5×10^{16} /cm^3, and 1×10^{18} /cm^3, respectively. The electron and hole mobilities were assumed to be 350 and 10 cm$_2$/V-s, respectively, based on our experimental data. Both n- and p-contacts were approximated to be Ohmic.

(a)   (b)   (c)
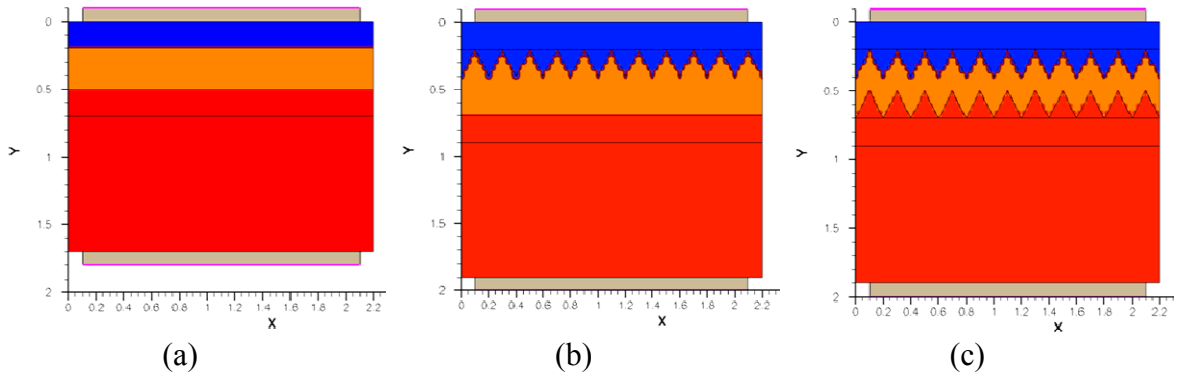
Figure 6-1. Electrical characteristics simulated using Synopsys Sentaurus for three different p-i-n structures consisting of p-type GaN (blue), unintentionally-doped GaN (orange), and n-type GaN (red); (a) Type I: planar p-i-n, (b) Type II: p-i-n with NSSP interface between i and p, and (c) Type III: p-i-n on NSSP plane.
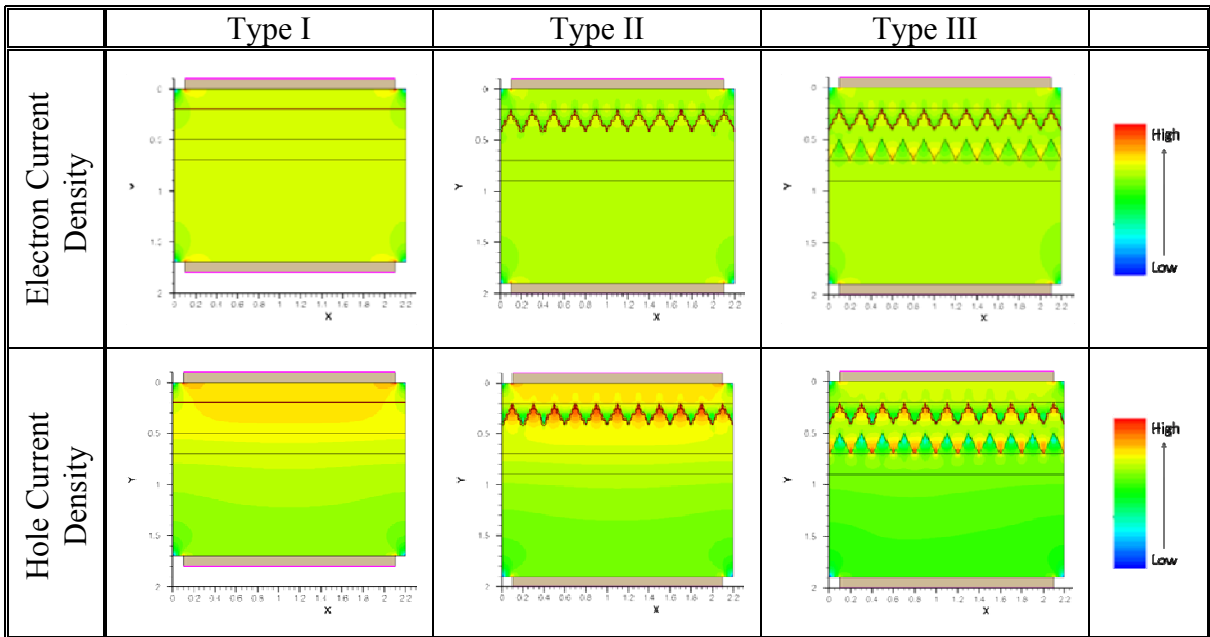
Figure 6-2. The calculated electron and hole current densities for the three p-i-n structures shown in Figure 6-1.
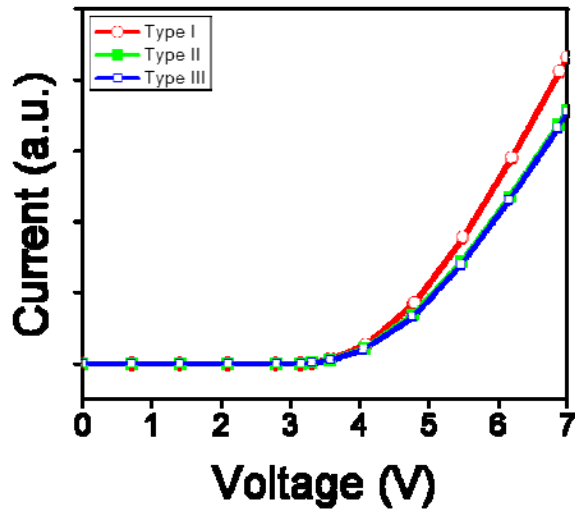
Figure 6-3. Calculated IV curves for Type I, Type II, and Type III.

The calculated electron and hole current densities and the IV curves are shown in Figure 6-2 and Figure 6-3, respectively. The calculated results show non-uniform electron and hole current spreading within the nano-structured region at the p-i and i-n interfaces. The hole current is less uniform due to a much lower mobility. Despite a seemingly worse uniformity in Type III, Type II and Type III exhibit similar IV characteristics; but both exhibit higher turn-on voltages than Type I does at a fixed current (20 mA), which agrees with our experimental results discussed in Chapter 5.

We also simulated the device region near the mesa edge (Figure 6-4, 2 μm width) and found that Type III had slightly worse current uniformity than Type II did. This was attributed to the current crowding near the mesa edge. As a result, in this region, Type III has a slightly worse IV characteristic than Type II does (Figure 6-5). But since a typical

LED mesa has a lateral dimension of >> 100 μm, it is expected that this difference will

not be significant.

	Type I	Type II-1	Type III	
Simulated Structure				
Electron Current Density				High ↑ Low
Hole Current Density				High ↑ Low
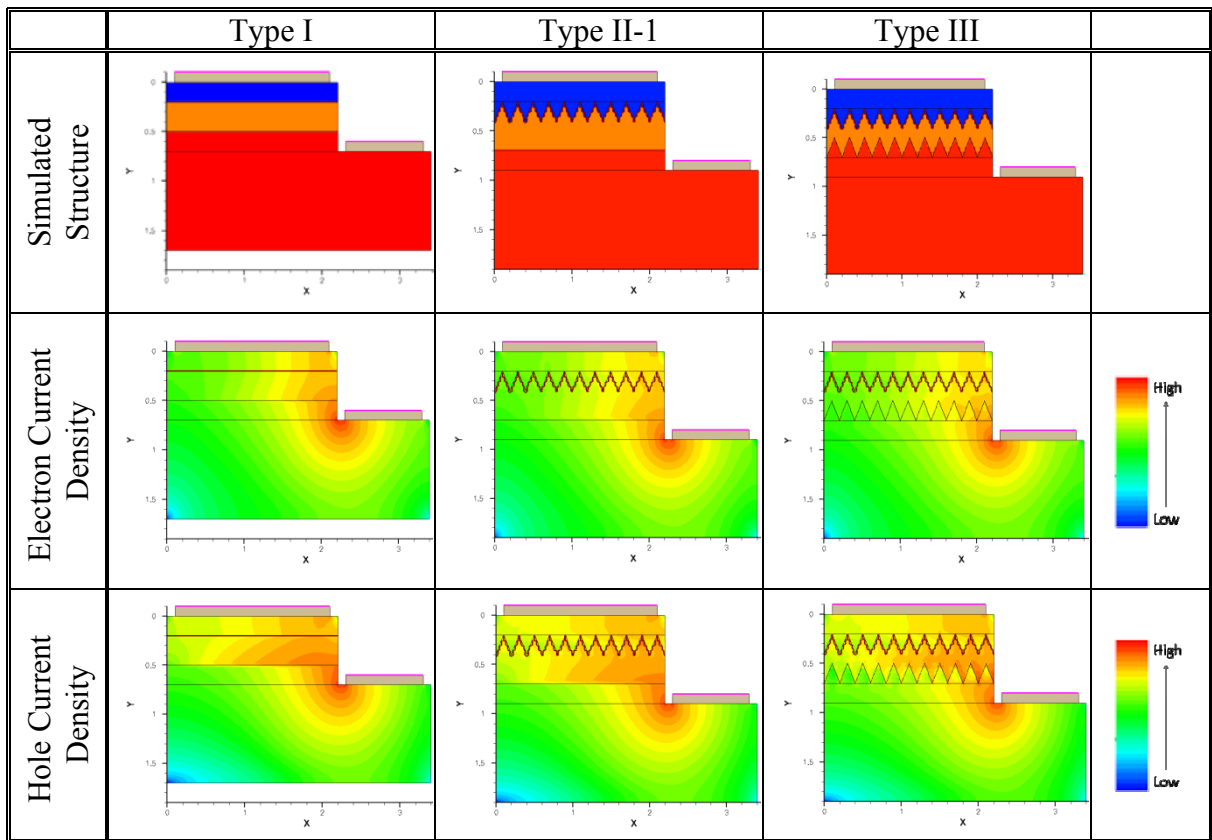
Figure 6-4. Calculated p-i-n mesa structures, electron and hole current densities for the simulated structures, Type I, Type II, and Type III.
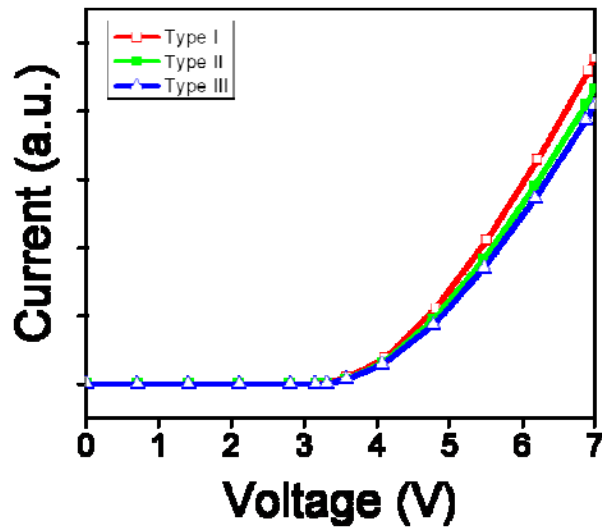
Figure 6-5. Calculated IV curves for p-i-n mesa structures, Type I, Type II, and Type III.

6.2   Graded Doping Profiles

To improve the current spreading in the NSSP active region, a series of graded doping profiles were considered. The 100 nm thick active region is divided into three layers; 30nm thick upper layer, 40 nm thick middle layer, and 30 nm thick lower layer. Different doping profiles that have been considered are summarized in Figure 6-6 and Figure 6-7. The calculated electron and hole current densities were also depicted in Figure 6-6 and Figure 6-7. For further investigation of the middle regions in which quantum wells (QWs) will be formed, the electron and hole current densities were measured at the center of the intrinsic area along x direction (0.2 μm – 0.3 μm). From the summarized data in Figure 6-8, Type V which has n-type upper and lower layers is most effective to improve the carrier spreading especially for the hole current density, which

agrees with experiments for planar InGaN/GaN QWs [87-89]. Compared to Type I, electron and hole current densities in Type V were improved up to 27% and 92%, respectively, although the uniformity is still not ideal. In terms of the IV characteristics, Type V shows a 30% higher current than Type I as shown in Figure 6-9. Hence, by adopting properly graded doping profile in the intrinsic area, the carrier current density in the p-i-n will be enhanced and the carrier uniformity can be improved. This will be used to improve the electrical characteristics of InGaN NSSP LEDs.

	Type I	Type II	Type III	
Description	p : 5 x 10^{17} /cm^3 upper-i : (n) 5 x 10^{16} /cm^3 middle-i : (n) 5 x 10^{16} /cm^3 lower-i : (n) 5 x 10^{16} /cm^3 n : 1 x 10^{18} /cm^3	p : 5 x 10^{17} /cm^3 upper-i : (n) 5 x 10^{16} /cm^3 middle-i : (n) 5 x 10^{16} /cm^3 lower-i : (n) 1 x 10^{17} /cm^3 n : 1 x 10^{18} /cm^3	p : 5 x 10^{17} /cm^3 upper-i : (n) 5 x 10^{16} /cm^3 middle-i : (n) 5 x 10^{16} /cm^3 lower-i : (n) 5 x 10^{17} /cm^3 n : 1 x 10^{18} /cm^3	
Simulated Structure				
Electron Current Density				High ↑ Low
Hole Current Density				High ↑ Low

Figure 6-6. Simulation for improving current uniformity in NSSP region with different graded doping profiles in intrinsic region.

	Type IV	Type V	Type VI	
Description	p : 5 x 10^{17} /cm^3 upper-i : (n) 5 x 10^{16} /cm^3 middle-i : (n) 5 x 10^{16} /cm^3 lower-i : (n) 5 x 10^{18} /cm^3 n : 1 x 10^{18} /cm^3	p : 5 x 10^{17} /cm^3 upper-i : (n) 5 x 10^{17} /cm^3 middle-i : (n) 5 x 10^{16} /cm^3 lower-i : (n) 5 x 10^{17} /cm^3 n : 1 x 10^{18} /cm^3	p : 5 x 10^{17} /cm^3 upper-i : (p) 1 x 10^{17} /cm^3 middle-i : (n) 5 x 10^{16} /cm^3 lower-i : (n) 5 x 10^{17} /cm^3 n : 1 x 10^{18} /cm^3	
Simulated Structure				
Electron Current Density				
Hole Current Density				
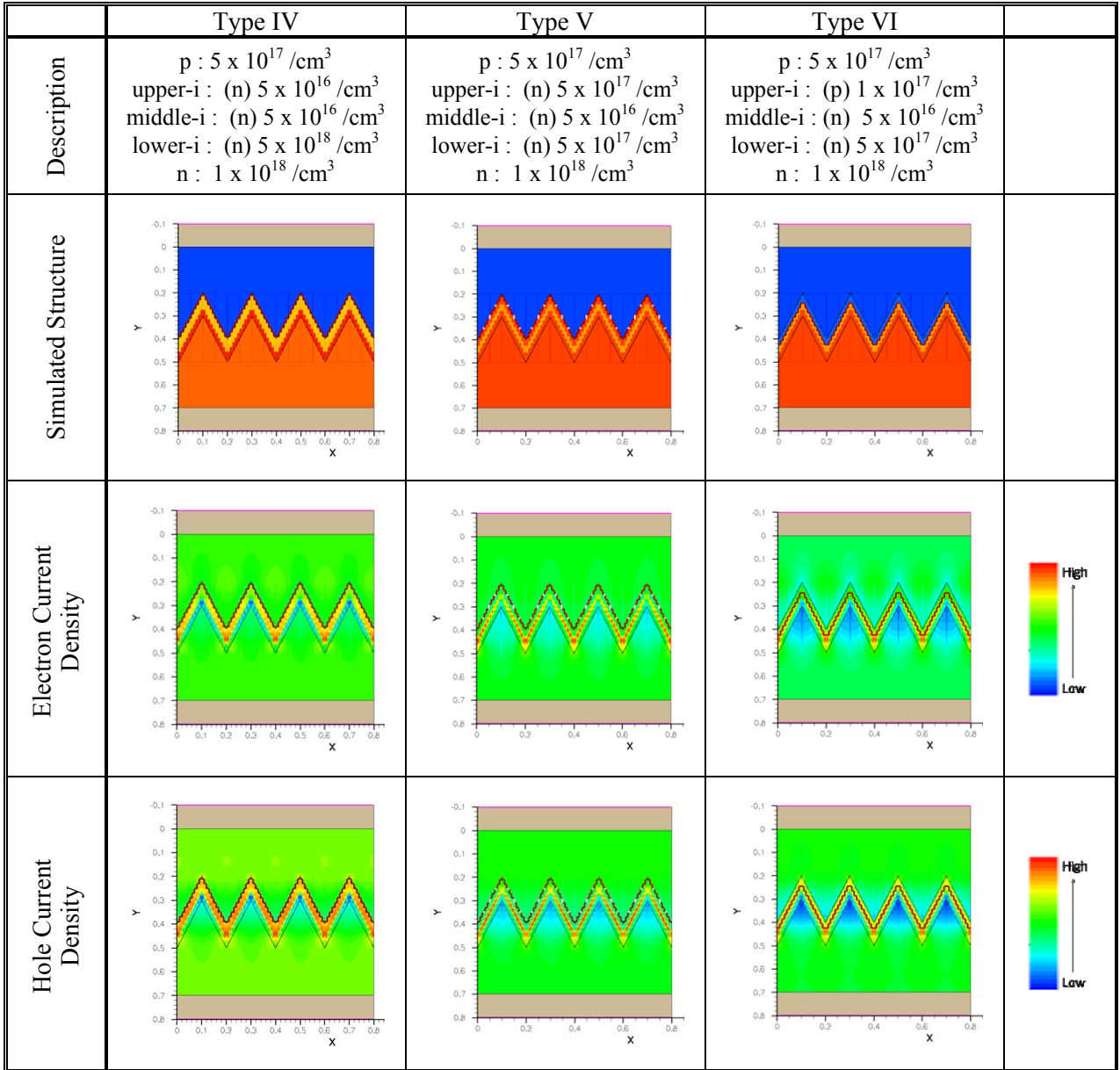
Figure 6-7. Simulation for improving current uniformity in NSSP region with different graded doping profiles in intrinsic region.

90
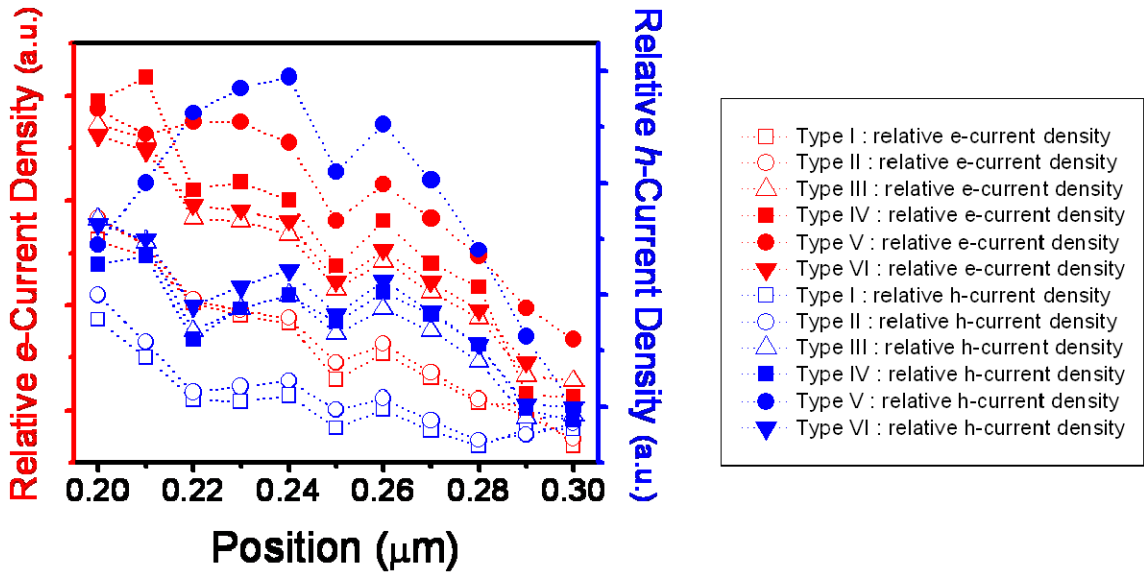
Figure 6-8. Summarized electron and hole current densities along the center of intrinsic region for different graded doping profiles.
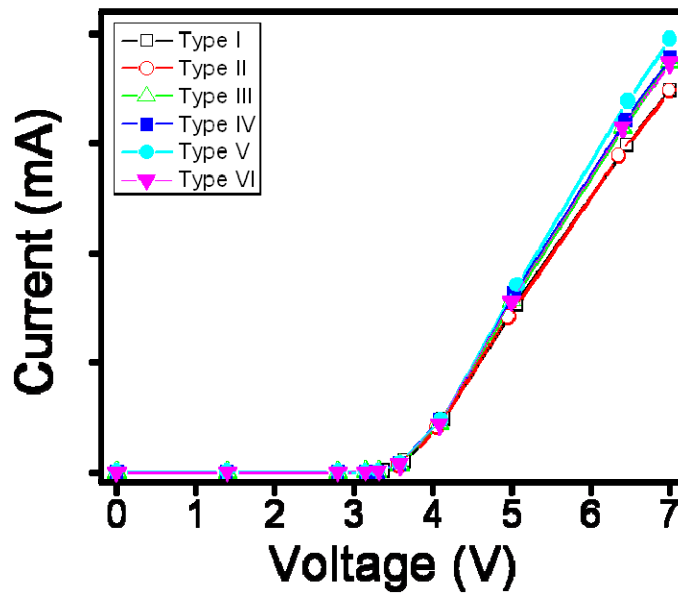
Figure 6-9. Simulated IV characteristics of different graded doping profiles in intrinsic region.

6.3   Summary

In the previous chapter, we demonstrated a green NSSP LED with a higher turn-on voltage compared to conventional planar *c*-plane LEDs. To investigate the root cause, we studied the NSSP structures using TCAD simulations. The doping profile was found to be critical for the current spreading across the NSSP active region. To improve the electrical property of NSSP LEDs, a graded doping profile was predicted to be useful. A p-i-n structure with n-type grading show improved current and hole current densities in the QW and lower the turn-on voltage.

CHAPTER 7

IMPROVING PHOTON EXTRACTION USING NANO-STRUCTURED GaN

As discussed in Chapter 1, total internal reflection (TIR) at the smooth light-emitting diode (LED) surface is a major limiting factor to LED extraction efficiency. Roughened or textured LED surfaces have proven to be effective in improving the extraction efficiency due to the reduction of TIR at the light emitting surface. Many of approaches to texturing the surface have been introduced such as the introduction of photonic crystal structures [37, 90-92] and photo-electrochemical (PEC) etching [38]. Most of these approaches are based on *ex situ* processes which require additional resources and costs. In this chapter, a novel and cost-effective approach to improving extraction efficiency of InGaN LEDs will be discussed. This method, the use of nano-structured GaN, is an *in situ* surface texturing process which can directly be integrated into LED epitaxy and provide a cost-effective alternative.

7.1 Nano-Structured InGaN/GaN Light Emitters

Previously, in Chapter 4, we discussed the use of an *in situ* silane treatment (ISST) and high temperature overgrowth (HTO) for the creation of nano-structures on a GaN surface. Both processes are *in situ* processes which can be performed in a standard III-nitride metal-organic chemical vapor deposition (MOCVD) system. The fact that surface texturing is possible without additional *ex situ* processes means that we can simplify the fabrication process and reduce total cost for LEDs. In the following, we will show the ISST process alone suffices to generate suitable surface texturing for extraction efficiency improvement in InGaN LEDs. The process is illustrated in Figure 7-1. Using an ISST process, randomly distributed nano-scale island-like structures with lateral dimensions of 100 – 200 nm are generated on a GaN surface.
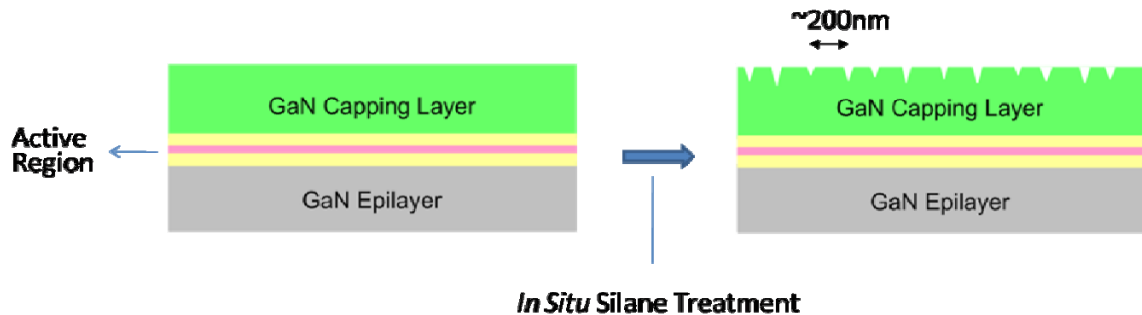
Figure 7-1. Surface texturing process using ISST.

7.1.1 Epitaxial Growth

To characterize the enhancement of photon extraction, two samples with complete LED structures were grown back-to-back on c-plane sapphire substrates under the same conditions. A 5-minute ISST process was added at the end of the epitaxial process for one sample while the other sample was left untreated. The active regions for both samples consisted of 3 pairs of InGaN/GaN multiple quantum wells (MQWs). In both samples, there were 150 nm of GaN overlayers on top of the active regions. The growth conditions of the as-grown samples are summarized in Table 7-1. Here, the ISST condition was slightly modified to allow better controllability of the surface morphology with a reduced silane (SiH_4) flow.

Layer	Growth Temp. (˚C)	Reactor Pressure (Torr)	TMG Flow (μmol/min)	TMI Flow (μmol/min)	NH_3 Flow (mmol/min)	SiH_4 Flow (sccm)	V/III Ratio	Thickness (nm)
UID GaN	1040	200	115	-	112	-	967	1550
InGaN	745	400	3.9	16.1	178	-	8901	3
GaN Barrier	745	400	14.4	-	178	-	12427	10
UID GaN Overlayer	1000	200	73	-	112	-	1524	150
ISST	1030	200	-	-	112	25	-	-

Table 7-1. Summary of growth conditions for ISST-treated InGaN LEDs.

7.1.1.1 Photoluminescence Characterization

Room temperature (RT; 300 K) photoluminescence (PL) measurements on both samples were performed at the same excitation intensity. The excitation was generated from a continuous-wave (CW) He-Cd laser at 325 nm wavelength with the estimated excitation intensity of 300 W/cm^2 at the sample surfaces. The comparison of the PL results for both ISST-treated and untreated samples is shown in Figure 7-2. The peak wavelengths were 456 nm and 458 nm for ISST-treated and untreated samples, respectively. The PL intensity of the ISST-treated sample was measured to be a factor of two compared to that of the untreated sample. This enhancement was attributed to the reduction of TIR at the sample surface due to surface texturing. It was further confirmed by the disappearance of interference fringes that were observed in the untreated sample. The fringes originated from multiple reflections between sapphire/GaN and GaN/air interfaces. Surface roughening considerably reduced the reflection at the GaN/air interface and suppressed the interference effect. The results agreed with previous results obtained on roughened nitrogen-polar GaN surfaces using PEC etching [38].
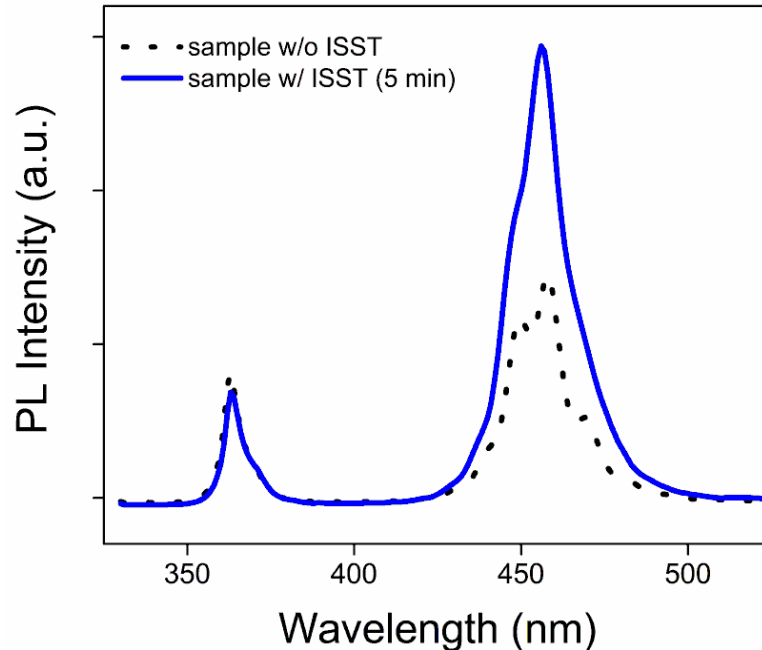
Figure 7-2. Room temperature photoluminescence spectrum comparison of MQWs without ISST and with 5-minute ISST.

7.1.2   LED Fabrication

One might think that improving the extraction efficiency using an ISST process is not feasible in making electrically injected LEDs due to the roughened surface. To this end, current injection LED devices were fabricated incorporating the ISST process as described in the previous subsection. Growth conditions for the LED structure with three pairs of InGaN/GaN MQWs were similar to those summarized in Table 7-1. The LED structure had a 180 nm of p-GaN grown at 1000 ˚C and the ISST process was performed immediately after the p-GaN growth. The ISST condition was modified slightly for a lower process temperature, the same as p-GaN growth temperature. Instead of using 5-minute ISST at 1030˚C, 6-minute ISST at 1000 ˚C was performed to achieve a textured

surface. The surface morphology is shown in Figure 7-3 as compared to the result from a higher-temperature ISST process. For LED fabrication, the same top-light-emitting structure and identical fabrication process as described in the previous chapter were used (Figure 7-4).
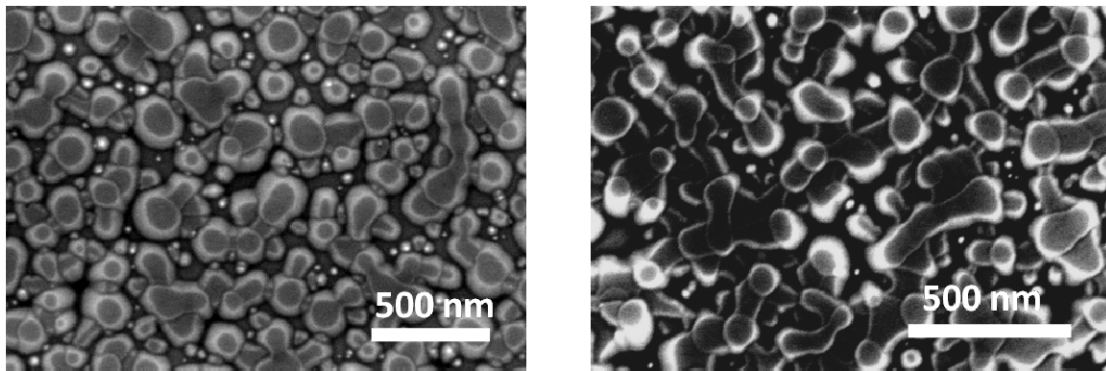
Figure 7-3. Surface morphology comparison: (left) 5 min ISST at 1030 ˚C and (right) 6 min ISST at 1000 ˚C.
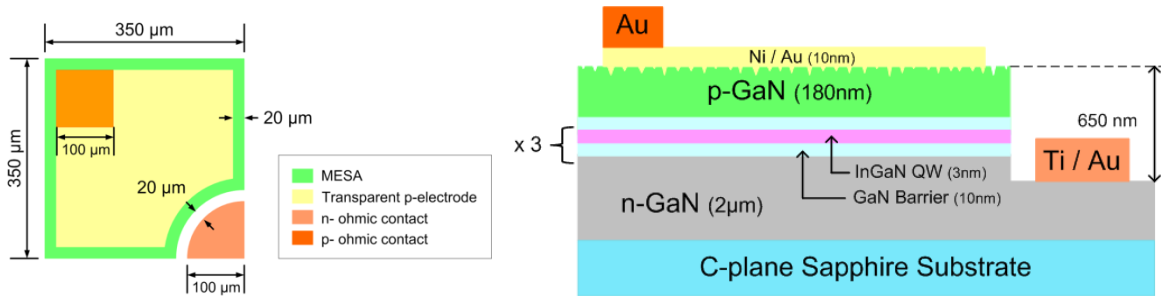
Figure 7-4. Device structure of nano-structured LEDs grown on *c*-plane sapphire substrate: (left) top view and (right) side view.

7.1.2.1 LED Characterization

The measured EL spectra are shown in Figure 7-5 under different CW injection. The peak wavelength was 425 nm. In contrast to the PL result of ISST-treated MQWs, fringes were recognized in the EL spectra. These fringes were attributed to the reflections from the interface between p-GaN and p-type transparent electrode as well as the interface between p-type transparent electrode and air. Both the I-V and L-I characteristics were shown in Figure 7-6. The turn-on voltage was measured to be 3.9 V at 20 mA. This high turn-on voltage was attributed partially to the high contact resistance at the textured surface. Further optimization of device structure and metal interface is still required. Due to the un-optimized electrical properties, direct comparison of the external quantum efficiency between the ISST-treated LED and the planar LED was not possible at this moment.
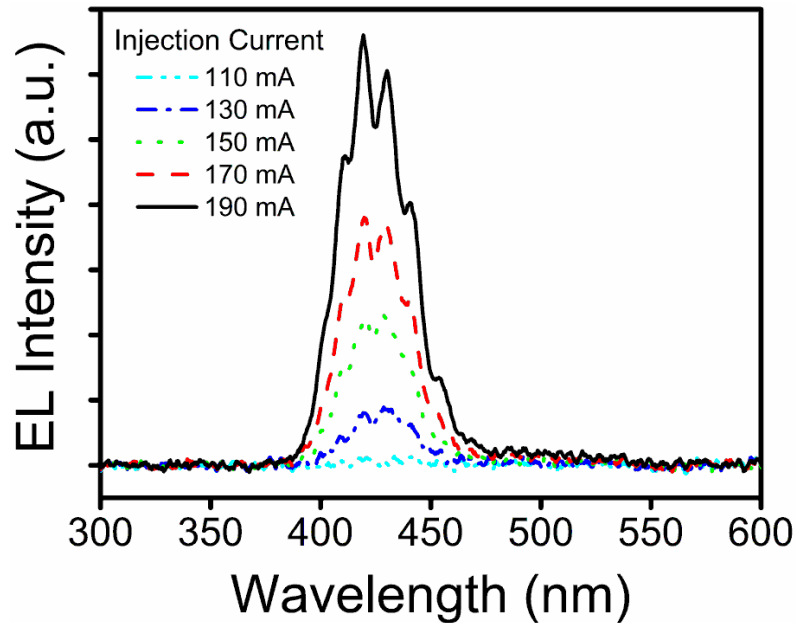
Figure 7-5. Electroluminescence spectra of nano-structured LED under different injection current.
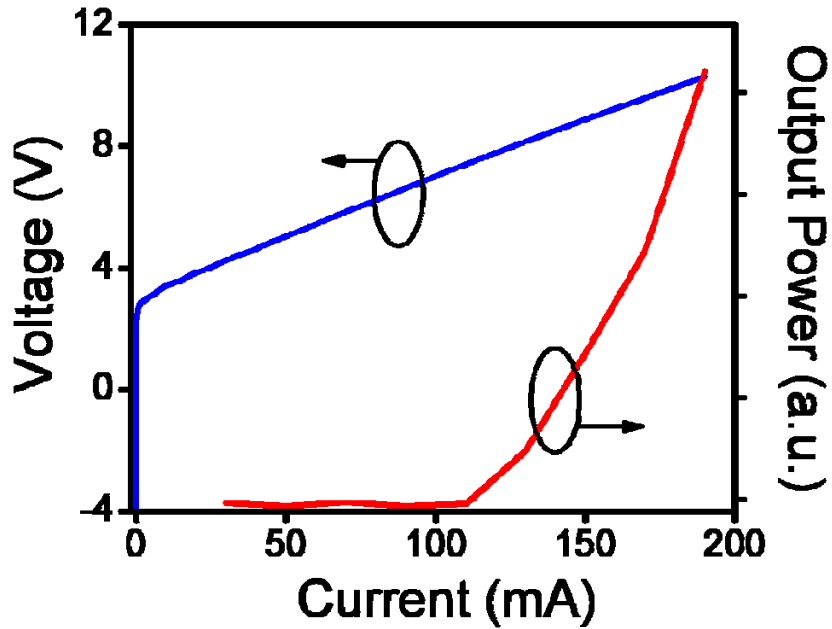
Figure 7-6. L-I and I-V curves of nano-structured LED.

7.2   Summary

In this Chapter, nano-structured GaN was employed to enhance extraction efficiency of InGaN LEDs. The ISST process was demonstrated as a possible cost-effective approach to improving extraction efficiency. The ISST was performed using a standard MOCVD tool and can be easily scaled up for manufacturing. From room temperature PL measurements, a factor of 2 improvements in light extraction was observed as compared to conventional LEDs. In addition, the feasibility of ISST process incorporated in a conventional LED process was demonstrated. A simple top-light-emitting structure was used and the fabricated LEDs were characterized by standard measurements. Electroluminescence spectra showed the interference fringes, possibly caused by the reflection at the p-GaN transparent electrode interface, in contrast to the

results from PL measurements. Further optimization of device structure and p-ohmic

contact is necessary to improve the electrical performance of nano-structured LEDs.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1   Research Summary

In this Thesis, we have developed and demonstrated that novel *in situ* nano-structured gallium nitride (GaN) processes in metal-organic chemical vapor deposition (MOCVD) are effective in improving the efficiencies of InGaN light-emitting diodes (LEDs). InGaN LEDs grown on *semi*-polar GaN templates were proven to exhibit higher internal quantum efficiency (IQE) and negligible quantum confined Stark effect (QCSE). The same *in situ* processes are also effective in reducing the defect density by an order of magnitude and increasing the photon extraction efficiency.

First, quasi-planar *semi*-polar InGaN quantum wells (QWs) were studied. {10-11} *semi*-polar GaN planes were generated using selective area epitaxy (SAE) on a *c*-plane GaN template followed by the growth of InGaN/GaN multiple quantum wells (MQWs). From PL measurements, the growth of MQWs on the *semi*-polar plane is stable within wide range of growth conditions. The excitation dependent PL also showed the reduced QCSE in comparison with that of polar InGaN/GaN MQWs grown on the (0001) plane,

which confirms the suppression of the internal electric field on the {10-11} *semi*-polar plane. Temperature dependent PL measurements reveal that the internal quantum efficiency of {10-11} MQWs is three times higher than that of the (0001) MQWs.

Next, we studied *in situ* processes that can effectively generate *semi*-polar GaN templates directly on *c*-plane substrates. These processes include *in situ* silane treatment (ISST) and high temperature overgrowth (HTO). The *in situ* processes developed in this Thesis are cost effective and suitable for mass-production because they require only standard MOCVD tools.

During ISST, silane (SiH_4) gas was introduced into the reactor under ammonia (NH_3) environment at above 1000°C. The ISST process can generate randomly distributed nano-scale cone structures with grain sizes up to 200nm. The surface morphology evolves with the treatment time, and the root-mean square (RMS) surface roughness becomes maximized after 5 minutes of ISST at a typical condition (40 sccm of diluted SiH_4 and 2.5 slm of NH_3 flow at 1030 °C). We have shown that SiH_4 is responsible for the surface morphological change. Although further analysis for the ISST mechanism is still required, our analytical and optical characterizations so far have favored the surface etching model instead of the deposition of a porous SiN_x nanomask. This etching model also agrees well with the optical properties of the ISST-treated surface. As the treatment time increases, stronger yellow band emission (YBE) was observed. It is widely accepted that this YBE originates from the gallium vacancies which can be formed at the surface during the GaN etching. As has been shown later, ISST is also an effective method for surface texturing to improve the photon extraction efficiency.

Sequential ISST and HTO processes can transform the inverted cone structures into sharp nano-structured *semi*-polar (NSSP) planes comprising of {10-11} and {11-22} planes. During HTO, growth rate anisotropy of GaN results in the nano-scale *semi*-polar plane formation. The NSSP GaN template can be used as a nano-scale *semi*-polar template for InGaN MQWs to improve the IQE. Similar to the quasi-planar *semi*-polar active region, the improved IQE on NSSP GaN is due to the suppressed internal electric field (IEF) on the *semi*-polar planes.

The complete InGaN/GaN LED structure was also grown on the NSSP GaN template. InGaN/GaN MQWs on NSSP planes were characterized by temperature- and excitation- dependent PL measurements as well as time resolved photoluminescence (TR PL) in comparison with *c*-plane MQWs. Room temperature PL showed that the peak intensity of NSSP MQWs is 3.3 times stronger than that of *c*-plane MQWs. This intensity enhancement was explained by surface roughening and surface grating effect. Excitation dependent PL measurements demonstrated that NSSP active region had a negligible QCSE, confirming the reduced IEF. Temperature dependent PL measurements were used to compare the IQEs of NSSP MQWs and *c*-plane MQWs, revealing a 30% higher IQE for NSSP MQWs in comparison to that of the *c*-plane MQWs. TR PL measurement showed that the difference in improvement of IQE is likely due to shortened *non*-radiative lifetime, generated by the ISST process. Further optimization of the ISST and HTO conditions is required to further improve the IQE of NSSP MQWs. Green/yellow NSSP LEDs were fabricated using a conventional top-emitting mesa structure. According to electroluminescence (EL) measurements, emission wavelengths with different current injections showed a negligible peak wavelength shift around 543 nm, due to the reduced

IEF in the *semi*-polar active region. Additionally, the linewidths of EL spectra were comparable to the state-of-the-art polar LEDs. However, the fabricated device showed a high turn-on voltage of 4.2 V at 20 mA. This is due to the combination of un-optimized growth conditions including HTO and p-GaN growth and un-optimized doping profiles. The latter has been verified by technology computer aided design (TCAD) simulations. Nevertheless, this demonstration was the first green *semi*-polar LEDs grown on a *c*-plane substrate that required no *ex situ* processing and re-growth.

In situ silane treatment was also demonstrated to be effective in improving the photon extraction efficiency. ISST-treated InGaN/GaN LED surfaces were compared to smooth surfaces. Room temperature PL measurements showed that the peak intensity of an ISST-treated sample becomes twice as strong as that of a planar sample. Interference fringes in the PL were eliminated in the ISST-treated sample. The increased peak intensity as well as the elimination of interference fringes confirms the improvement of extraction efficiency in the ISST-treated InGaN/GaN MQWs through surface texturing. ISST surface treated, electrically injected LEDs were also demonstrated, showing the feasibility of making electrical contact on ISST-treated surfaces. Unlike the PL results, interference fringes were observed from EL measurements, which was attributed to the reflection of the light from the p-Ohmic contact. The turn-on voltage was 3.9 V at 20 mA. Electrical properties can be improved by optimizing the device structure and p-type Ohmic contacts processing conditions.

8.2   Future Work

Further studies of NSSP InGaN LEDs should begin with a deeper understanding of the fundamental mechanism of the ISST process on the reduction of excessive materials defects. One potential analytical approach is the use of high-resolution transmission electron microscopy (HR TEM) and x-ray energy dispersive spectroscopy (XEDS). This method has been adopted in this research. However, the possible contamination of silicon atoms at the ISST interface due to silicon sample mount during the TEM sample preparation has prevented a proper data interpretation. We are currently investigating the use of the sapphire sample mount to circumvent this issue.

Because the NSSP GaN template consists of two different *semi*-polar planes, it is unknown whether the growth rate is uniform across the entire sample. Although the current device shows a comparable emission linewidth than that of the planar sample, it will be useful to study this at an atomic level, perhaps using high resolution TEM. In addition, first-principle theoretical modeling of the epitaxial growth on the NSSP surface can be important to understand the indium incorporation on the nano-structured surface. It has been shown that the indium incorporation depends on the crystal orientation of the planar substrate. To this end, the study of indium incorporation on the NSSP surface can help us achieve even longer wavelength (e.g. red) InGaN LEDs.

The current spreading in the NSSP InGaN LEDs also requires further theoretical and experimental studies. Preliminary simulation studies have been performed in this research. Doping profiles are found to be important in further optimization of the NSSP LED electrical characteristics. The dependence of device reliability on the uniformity of

the carrier concentration in the InGaN MQWs can also be important for practical applications.

In using the ISST process for the improvement of the photon extraction efficiency, the LED fabrication needs to be further optimized. It has been found that the p-ohmic contact on the rough surface can lead to high contact resistance, resulting in a high turn-on voltage. Strategies such as additional annealing should be experimentally verified. In addition, the flip-chip high-power InGaN LED structure is getting more popular today owing to its improved hole current spreading. We can also potentially apply the ISST process in the flip-chip structure. One potential strategy is to perform the ISST on a thin AlGaN sacrificial layer underneath the LED structure. Once the sapphire substrate is removed, photoelectrochemical etching can be used to remove the AlGaN layer, revealing a textured surface on the n-GaN surface.

APPENDICES

APPENDIX A: LED FABRICATION PROCESS

A.1 Step 1 : P-type Transparent Electrode Deposition

Sample Cleaning	DI water, Acetone, and then IPA spray cleaning. N_2 blow dry
Local Oxide Removal	HCl Cleaning : Dipping in HCl solution (HCl : H_2O = 1 : 1) : 5 min , w/ Agitation Rinse in flowing DI water
Dehydration Bake	Hotplate 130 °C, 3 min
Spin Coating	SPR 220 (3.0) 4500 rpm, 45 sec , Estimated thickness 1~2 um
Pre-Bake	Hotplate 115 °C, 90 sec
Alignment & Exposure Lamp Intensity WEC pressure WEC type WEC offset Exposure type Exposure time Alignment gap Hard contact wait time	Mask : LED2 P OHMIC 20 mW/cm^2 Pieces : 0.1 Contact 0 Hard 4.5 sec 30 um 2 sec
Post Exposure Bake (PEB)	Hotplate 115 °C, 90 sec
Development	AZ 300 MIF, 90 sec, w/ Agitation Rinse in flowing DI water N_2 blow dry
Plasma Descum (optional)	Pressure : 250 mTorr Power : 100 W Gas : O_2 Gas % : 17 % Time : 60 sec
Hard-bake (optional)	Not necessary but adopted to increase etch selectivity Hotplate 130 °C, 2 min
Local Oxide Removal Before Metal Deposition	Same as Local Oxide Removal Step
Metal Deposition (SJ20)	Ni (5 nm) / Au (5 nm) Deposition rate 2A/sec
Lift-off	Dipping in PRS-2000, 30 min on Hotplate (105 °C) Dipping in Acetone, 5min on Hotplate (105 °C) Acetone + IPA spray cleaning Rinse in flowing DI water
Piranha Etch (optional)	H_2SO_4(50ml) + H_2O_2(50ml) : 15min
Plasma Ash (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 300 sec
Annealing (RTA)	Temp. : 450 °C Ambient : N_2 Time : 10 min

A.2 Step 2 : Defining Mesa Structures

Sample Cleaning	DI water, Acetone, and then IPA spray cleaning. N_2 blow dry
Dehydration Bake	Hotplate 130 °C, 3 min
Spin Coating	SPR 220 (3.0) 4500 rpm, 45 sec , Estimated thickness 1~2 um
Pre-Bake	Hotplate 115 °C, 90 sec
Alignment & Exposure Lamp Intensity WEC pressure WEC type WEC offset Exposure type Exposure time Alignment gap Hard contact wait time	Mask : LED2 MESA 20 mW/cm^2 Pieces : 0.1 Contact 0 Hard 4.5 sec 30 um 2 sec
Post Exposure Bake (PEB)	Hotplate 115 °C, 90 sec
Development	AZ 300 MIF, 90 sec, w/ Agitation Rinse in flowing DI water N_2 blow dry
Plasma Descum (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 60 sec
Hard-bake (optional)	Not necessary but adopted to increase etch selectivity Hotplate 130 °C, 2 min
ICP Etching	LAM etching (Recipe : Pressure 2 mT, FWD RF PW 150 W, Cl$_2$ 25 sccm, Ar 5 sccm, TCP PW 300 W) Target height : 570 nm
PR Removal	Dipping in PRS-2000, 30 min on Hotplate (105 °C) Dipping in Acetone, 5min on Hotplate (105 °C) Acetone + IPA spray cleaning Rinse in flowing DI water
Piranha Etch (optional)	H_2SO_4(50ml) + H_2O_2(50ml) : 15min
Plasma Ash (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 300 sec
Annealing (RTA)	Temp. : 450 °C Ambient : N_2 Time : 10 min

A.3 Step 3 : P-type Ohmic Contact Deposition

Sample Cleaning	DI water, Acetone, and then IPA spray cleaning. N_2 blow dry
Dehydration Bake	Hotplate 130 °C, 3 min
Spin Coating	SPR 220 (3.0) 4500 rpm, 45 sec , Estimated thickness 1~2 um
Pre-Bake	Hotplate 115 °C, 90 sec
Alignment & Exposure Lamp Intensity WEC pressure WEC type WEC offset Exposure type Exposure time Alignment gap Hard contact wait time	Mask : LED2 P PAD 20 mW/cm^2 Pieces : 0.1 Contact 0 Hard 4.5 sec 30 um 2 sec
Post Exposure Bake (PEB)	Hotplate 115 °C, 90 sec
Development	AZ 300 MIF, 90 sec, w/ Agitation Rinse in flowing DI water N_2 blow dry
Plasma Descum (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 60 sec
Hard-bake (optional)	Not necessary but adopted to increase etch selectivity Hotplate 130 °C, 2 min
Metal Deposition (SJ20)	Au (310 nm) Deposition rate 10A/sec
Lift-off	Dipping in PRS-2000, 30 min on Hotplate (105 °C) Dipping in Acetone, 5min on Hotplate (105 °C) Acetone + IPA spray cleaning Rinse in flowing DI water
Piranha Etch (optional)	H_2SO_4(50ml) + H_2O_2(50ml) : 15min
Plasma Ash (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 300 sec

A.4 Step 4 : N-type Ohmic Contact Deposition

Sample Cleaning	DI water, Acetone, and then IPA spray cleaning. N_2 blow dry
Dehydration Bake	Hotplate 130 °C, 3 min
Spin Coating	SPR 220 (3.0) 4500 rpm, 45 sec , Estimated thickness 1~2 um
Pre-Bake	Hotplate 115 °C, 90 sec
Alignment & Exposure Lamp Intensity WEC pressure WEC type WEC offset Exposure type Exposure time Alignment gap Hard contact wait time	Mask : LED2 P PAD 20 mW/cm^2 Pieces : 0.1 Contact 0 Hard 4.5 sec 30 um 2 sec
Post Exposure Bake (PEB)	Hotplate 115 °C, 90 sec
Development	AZ 300 MIF, 90 sec, w/ Agitation Rinse in flowing DI water N_2 blow dry
Plasma Descum (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 60 sec
Hard-bake (optional)	Not necessary but adopted to increase etch selectivity Hotplate 130 °C, 2 min
Metal Deposition (SJ20)	Ti (20 nm) / Au (300 nm) Deposition rate : Ti – 5 A/sec, Au – 10 A/sec
Lift-off	Dipping in PRS-2000, 30 min on Hotplate (105 °C) Dipping in Acetone, 5min on Hotplate (105 °C) Acetone + IPA spray cleaning Rinse in flowing DI water
Piranha Etch (optional)	H_2SO_4(50ml) + H_2O_2(50ml) : 15min
Plasma Ash (optional)	Pressure : 250 mTorr Power : 150 W Gas : O_2 Gas % : 17 % Time : 300 sec

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