TIME-BASED ANALOG TO DIGITAL CONVERTERS

by

Shahrzad Naraghi

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2009

Doctoral Committee:

Associate Professor Michael Flynn, Chair
Professor Kensall D. Wise
Associate Professor Dennis M. Sylvester
Associate Professor Anna C. Gilbert
Assistant Professor David D. Wentzloff

ACKNOWLEDGEMENTS

This work was only made possible by support of many great people. First of all, I would like to thank my advisor, Professor Michael Flynn for all his support during these years. His expectations of me remained a constant source of inspiration for me throughout this project. His expert technical guidance was very helpful in making this work possible. I will always appreciate his having faith in me in times of frustration. I am also grateful to the rest of my committee members: Professor Kensall Wise, Professor Dennis Sylvester, Professor Anna Gilbert and Professor David Wentzloff. Their technical help and kind words of encouragement will always be appreciated.

I would also like to extend my appreciation to Matthew Courcy and Gabriele Manganaro from National semiconductor for their support.

Also, I would like to thank Mehrzad Malmirchegini and Professor Farrokh Marvasti for helping me in implementing the digital signal processing algorithms.

In addition I would like to express my gratitude to my great group members. I couldn't have finished this work if it weren't for their support. Mark Ferriss, who patiently listened to me and gave me solutions for my technical problems. He always encouraged me with his optimistic views. Jorge Pernillo, Andres Tamez, Ivan Bogue, Joshua Jaeyoung Kang always generously devoted their time to help me with the tools and lab

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF APPENDICES

ABSTRACT

TIME-BASED ANALOG TO DIGITAL CONVERTERS

by

Shahrzad Naraghi

Chair: Michael Flynn

Low-power, small analog-to-digital converters (ADCs) have numerous applications in areas ranging from power-aware wireless sensing nodes for environmental monitoring to biomedical monitoring devices in point-of-care (PoC) instruments. The work focuses on ultra-low-power, and highly integrated implementations of ADCs, in nanometer-scale complementary metal-oxide-semiconductor (CMOS) very large scale (VLSI) integrated circuit fabrication technologies. In particular, we explore time-based techniques for data conversion, which can potentially achieve significant reductions in power consumption while keeping silicon chip area small, compared to today's state-of-the-art ADC architectures.

Today, digital integrated circuits and digital signal processors (DSP) are taking advantage of technology scaling to achieve improvements power, speed, and cost. Meanwhile, as technology scaling reduces supply voltage and intrinsic transistor gain, analog circuit

designers face disadvantages. With these disadvantages of technology scaling, two new broad trends have emerged in ADC research. The first trend is the emergence of digitally-assisted analog design, which emphasizes the relaxation of analog domain precision and the recovering accuracy (and performance) in the digital domain. This approach is a good match to the capabilities of fine line technology and helps to reduce power consumption. The second trend is the representation of signals, and the processing of signals, in the time domain. Technology scaling and its focus on high-performance digital systems offers better time resolution by reducing the gate delay. Therefore, if we represent a signal as a period of time, rather than as a voltage, we can take advantage of technology scaling, and potentially reduce power consumption and die area.

This thesis focuses on pulse position modulation (PPM) ADCs, which incorporate time-domain processing and digitally assisted analog circuitry. This architecture reduces power consumption and area significantly, without sacrificing performance. The input signal is pulse position modulated and the analog information is carried in the form of timing intervals. Timing measurement accuracy presents a major challenge and we present various methods in which accuracy can be achieved using CMOS processes. This 'digital' approach is more power efficient compared with pure analog solutions, utilized for amplitude measurement of input signals.

CHAPTER 1

INTRODUCTION

1.1 Background & Motivation

Analog to digital converters (ADC) are key components in many electronic systems. Today's integrated circuits (ICs) are mostly mixed-signal (i.e., a combination of analog and digital) circuits, consisting of a digital signal processor (DSP) core which has input interfaces to the external analog signals through ADCs. The growth in hand-held and battery-operated electronic systems is pushing designers to search for ADC architectures which offer lower power consumption and are more cost-efficient. The starting point of the research presented in this thesis is to identify the limiting features of today's *conventional* technologies, and explore *alternative* architectures which address and potentially overcome these shortcomings.

Increasingly, many experiments and measurements require signal digitization of a large number of parallel signal channels for storage and analysis. Examples can be found in applications such as high energy physics, spectroscopy, medical imaging, radiation sensors, and environmental sensors [1-5]. Due to the large number of channels in these applications, power consumption and the die area of the ADC per channel should be as small as possible. This is a very fundamental problem and the scalability of these acquisition systems is a bottleneck for many instrumentation applications. One approach

1

to address the scalability of these systems is component sharing which helps further shrink the whole multi-channel ADC architecture. ADCs with sampling frequencies of tens of kHz to few tens of MHz, and medium resolution, are often used in these systems. The motivation of our research is the implementation of a multichannel ADC for a wireless sensor, as shown in Figure 1.1. The ADC is used in a sensor node which sends data to a central node where data is processed. Since the sensor is battery-operated, the ADC needs to be extremely power efficient.
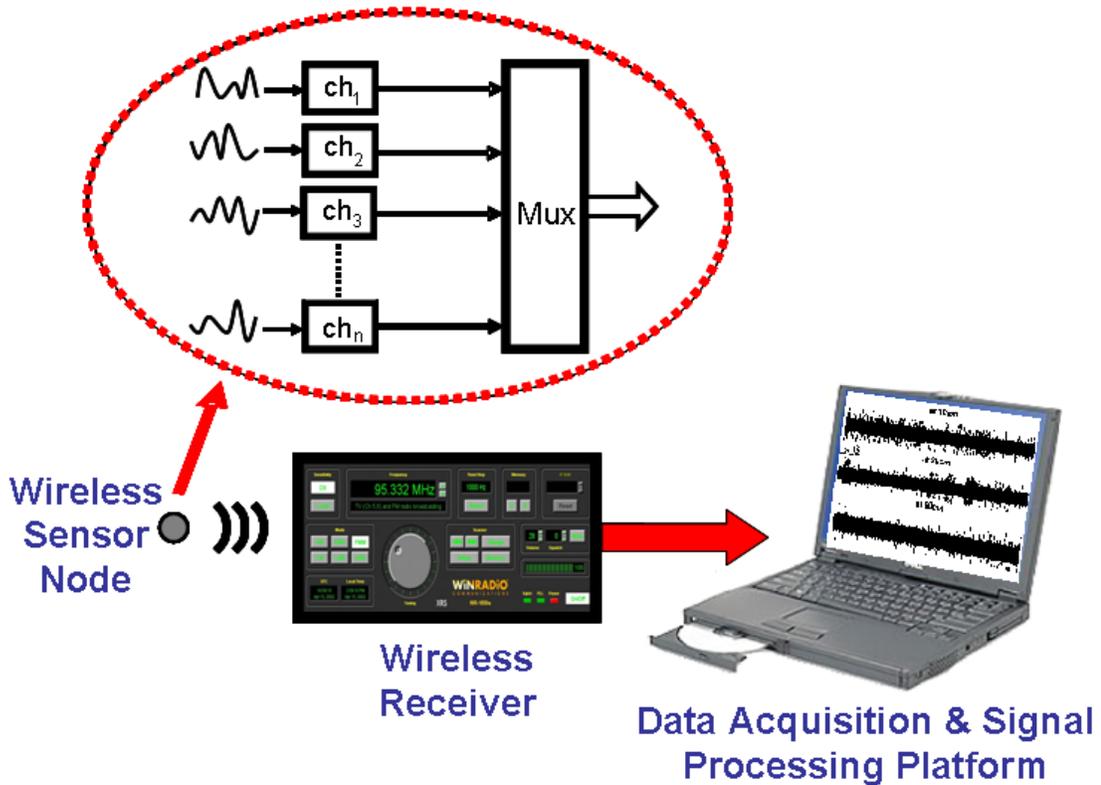
Figure 1.1 : Research Motivation

This thesis focuses on a Pulse Position Modulation (PPM) ADC architecture. PPM is generally a time-based architecture. We believe that this architecture can fulfill many of the requirements in the sensor applications mentioned above. The PPM ADC can meet the need for energy efficiency since it incorporates time-domain signal processing based on low power digital circuits. Signal processing can be performed in the digital domain and in the central node, helping to relax the analog circuit precision of the ADC which subsequently leads to less current consumption in the sensor node. Another benefit of the PPM architecture is the ability to share the building blocks between the channels, as we will discuss later, leading to a compact area and further power reductions.

1.2 ADC circuit energy trends

Power dissipation is one the most important concerns in ADCs used for battery operated devices. It is important to track the trends in ADC power efficiency during the past years. In an ADC survey, Murmann [6] has gathered ADC performance data from the International Solid State Circuit Conferene (ISSCC) and the VLSI Symposium on Circuits during the past eleven years. In this survey, power efficiency is defined as ADC total power (P) divided by sampling frequency (f_s). Figure 1.2 is the 3-D representation of power efficiency along with the published year. The data in this survey shows that the power dissipation of ADCs halves approximately every two years, over the past decade. This time duration corresponds to CMOS process scaling from $0.6\,\mu$m to 65nm.

From the data above we see improvement in ADC power efficiency. This occurred despite the obstacles in analog design associated with scaling. Technology scaling reduces the supply voltage and this limits the headroom voltage in the amplifier design and in cascode architectures. Reducing the supply voltage also reduces the signal

dynamic range. This reduces the signal-to-noise ratio in thermal-noise-limited ADCs, as thermal noise does not scale with technology. Furthermore, short-channel transistors suffer from lower output resistance and lower intrinsic gain. These issues significantly affect the choice of low power ADC architecture in advanced technologies.
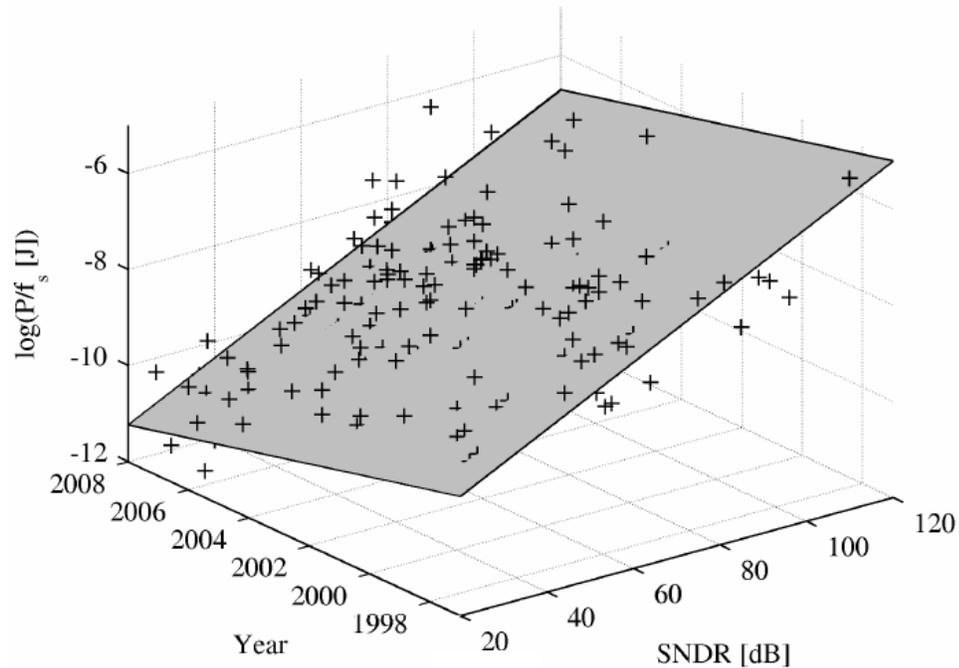
Figure 1.2 : Trends in ADC performance [6]

Looking at the ADC architectures shows that the power efficiency improvement is mostly due to the new design trends coming with scaling [6] as:

- Minimalistic design

- Digitally-assisted analog design

- Time domain analog processing

1.2.1 Minimalistic design

The goal of minimalistic design is to improve power efficiency by simplifying the analog subcircuits of the ADCs. As an example, the inherent inefficiency of op-amps has encouraged many ADC designers to remove this building block or to simplify it. An example of this approach is op-amp-less implementation of pipeline ADCs [7, 8] in which the op-amp is replaced with open-loop amplifiers. Another approach is to replace op-amps with comparators in switched capacitor circuits [9]. Pipeline ADCs based on comparator-based switch capacitor circuits have been published [10, 11]. Another recent example is the dynamic amplifier concept which uses a single transistor and charge conservation to amplify the residue in pipeline ADCs [12]. This simplification of the analog circuit block can sacrifice precision for performance [6] and therefore, it is very also attractive to consider digital techniques to recover accuracy in minimalistic designs.

1.2.2 Digitally-assisted analog design

The rationale behind digitally-assisted analog design is to move the accuracy burden from the realm of analog design to the digital domain. Relaxing the precision of the analog circuitry reduces power consumption significantly, while the correction of analog imperfections is implemented in the digital domain, allowing lower power and faster designs. One example of this approach is use of open-loop amplifiers in pipeline ADCs and correcting the nonlinearities caused by open-loop amplifiers in the digital domain [7, 8].

Technology scaling has reduced the energy per operation in CMOS logic circuits. The scaling of transistor feature size along with aggressive supply voltage reduction has led to a 65% reduction in energy per logic operation for each new technology node [13]. For

example, a purely digital circuit implemented in a 90nm CMOS process consumes approximately 65% the energy per operation of its identical counterpart in a 130nm CMOS process. Murmann *et. al* compares the energy efficiency of ADCs with that of a single NAND gate, to give a feel for how much logic can be used to "assist" a converter for calibration or error correction [6]. In this comparison, we take E_{NAND} as the energy a NAND gate consumes each time it is toggled. At low signal fidelity, E_{NAND} is 45 fJ in 90nm CMOS. The ADC energy consumption, E_{ADC}, is the amount of energy consumed in each conversion. Based on the ADCs reported in 2008, E_{ADC} and E_{NAND} are compared for different ADC resolutions as shown in table 1.1. The numbers [6] in table 1.1 show that in a low-resolution converter, it is unlikely that tens of thousand gates should be used for digital error correction. However, for ADCs with SNDR above 50dB, each analog conversion requires a significant amount of energy compared to the energy consumed by a digital processing, operation as shown in Table 1.1. This justifies the use of digital circuits to recover accuracy in analog circuits.

SNDR[dB]	E_{ADC}	E_{ADC}/E_{NAND}
30	21 nJ	4700
50	168 nJ	38000
70	1.35 μJ	300000
90	10.8 μJ	2,400,000

Table 1.1: E_{ADC} and E_{NAND} comparison [6]

1.2.3 Time domain analog signal processing

One way to overcome the challenge of low-voltage design is to process a signal in the time-domain [14]. Time resolution has been improved in nanometer-scale devices due to the reduction of gate delay, despite the reduction in supply voltage [15]. Hence, time-domain processing potentially offers a better solution compared to voltage-based methods, when implemented in deep sub-micron VLSI fabrication processes. This is discussed in detail in Chapter 3. According to a new paradigm in RF circuit design [15], in deep-submicron CMOS processes the time-domain resolution of digital signal edge transitions is superior to voltage resolution of analog signals. Employing this approach, digital circuits can be used to perform analog processing [14] while taking advantage of technology scaling to significantly reduce power consumption and area. One particular example of this trend is the design of all-digital phase-locked loops (PLL), in which the phase difference measurement is implemented with a time-to digital-converter (TDC). In these systems, the required loop filter of the PLL is simply a digital finite impulse response (FIR) digital filter [15]. Another design is a voltage-controlled oscillator (VCO)-based ADC, where the input signal changes the VCO frequency and the frequency is digitized with phase detectors [16].

1.3 Time-based ADC architectures

There are many different ADC architectures which quantize time or frequency instead of voltage or current. These architectures are explained in this section.

1.3.1 Slope and integrating ADC

Slope and integrating ADCs perform analog to digital conversion in time domain. A block diagram of a single slope ADC is shown in Figure 1.3. The sampled input voltage (V_s) is stored on a capacitor. Then, V_s is discharged by a constant current source and this generates a ramp voltage at the capacitor output. A counter is triggered by the start of the ramp (or the start of the discharge) and stops counting when the ramp voltage is zero or when the capacitor is completely discharged. The waveforms are shown in Figure 1.3. The input signal is proportional to the counter digital output [17]. The main advantages of this ADC architecture are as follows:

- Low complexity and simplicity

- Integral non-linearity (INL) depends on ramp linearity and not component matching

- Always monotonic

Low sampling speed is the main disadvantage of this ADC architecture. In order to have a high resolution ADC, the clock frequency must be high which leads to large power consumption. Some researchers have recently demonstrated high-speed slope based ADCs by replacing the counter with advanced time to digital conversion techniques [3, 4].

$$S = \frac{I_{ref}}{C}, T = \frac{V_s}{S}$$
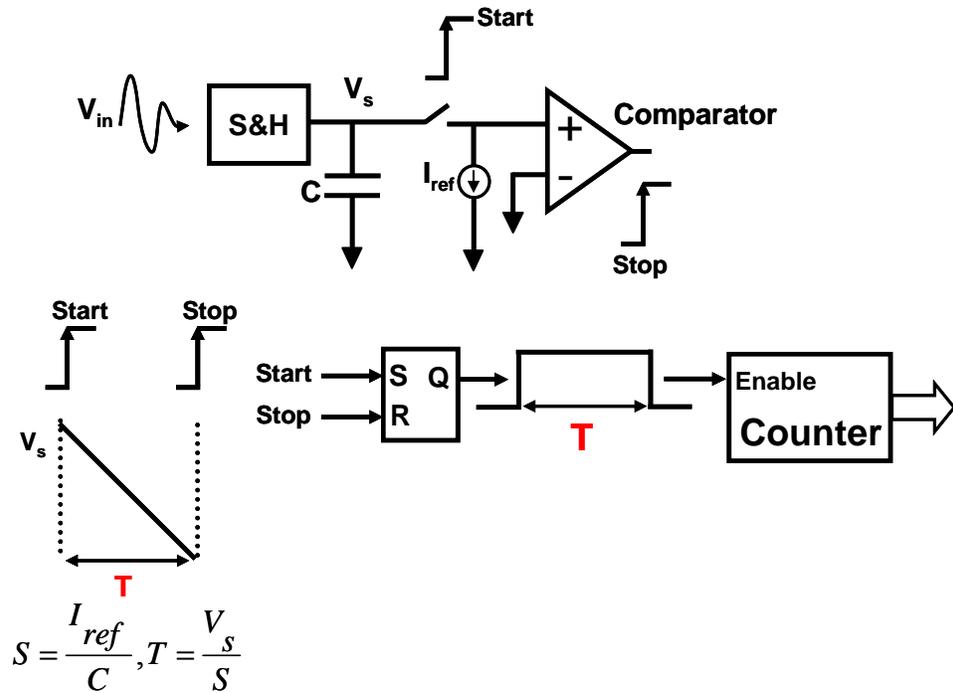
Figure 1.3 : Single slope ADC

1.3.2 Pulse width modulation (PWM) ADC

One of the oldest time-based ADC architectures is found in a 70-year-old patent [18]. A simplified block diagram of this ADC taken from [19] is shown in Figure 1.4. The input signal is first pulse-width-modulated and then quantized with a counter. Pulse width modulation is a technique to transfer amplitude domain signal information to the time domain. With this method, a simple counter or an advanced TDC can be used as the time quantizer. PWM generally creates signal distortion due to its nonlinear behavior. In order to avoid these nonlinearities, the modulation frequency must be at least 8 times larger than the signal bandwidth [20]. The pulse position modulation (PPM) ADC prototype in our research is an elaboration of this architecture.
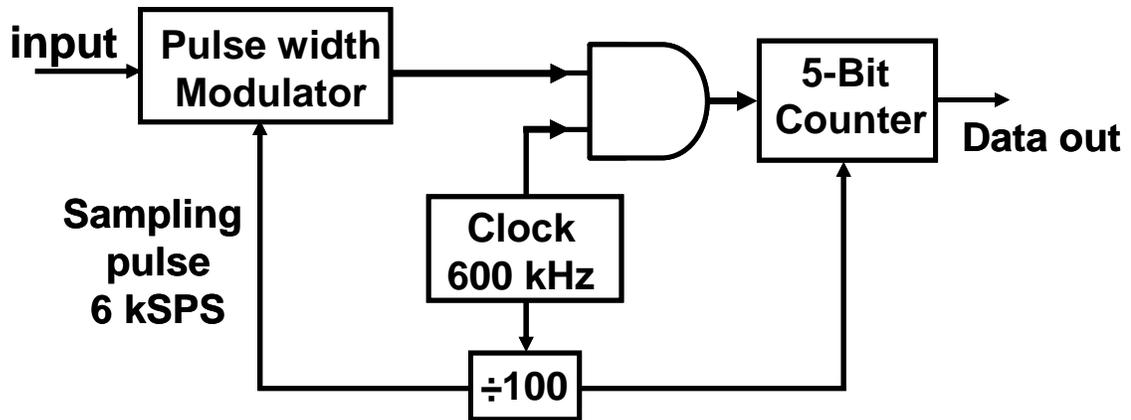
Figure 1.4 : PWM ADC [19]

1.3.3 Level-crossing or asynchronous ADC

Asynchronous ADCs [21-25], typically have different reference levels and multiple comparators. At the instant the signal passes a threshold level, a sample is captured and the ADC records and quantizes the time interval between these instants. This is shown in the waveforms of Figure 1.5. The output samples are non-uniformly spaced in time. One simple asynchronous ADC block is illustrated in Figure 1.5. Each comparator generates an output pulse when the input signal passes its corresponding threshold voltage. The comparator activity is not synchronous with any reference clock and it only depends on the input signal activity. Therefore, there must be a handshake protocol between these comparators (e.g. tokens in Figure 1.5) and a time recording block. An interesting characteristic of level-crossing or asynchronous ADCs is that the ADC power consumption is proportional to the signal activity. If the signal remains silent for a while, no threshold level is crossed, resulting in no digital power consumption. However, comparator offset and mismatch are concerns in this approach, similar to the design of flash ADCs.

10

input signal

Time measurement
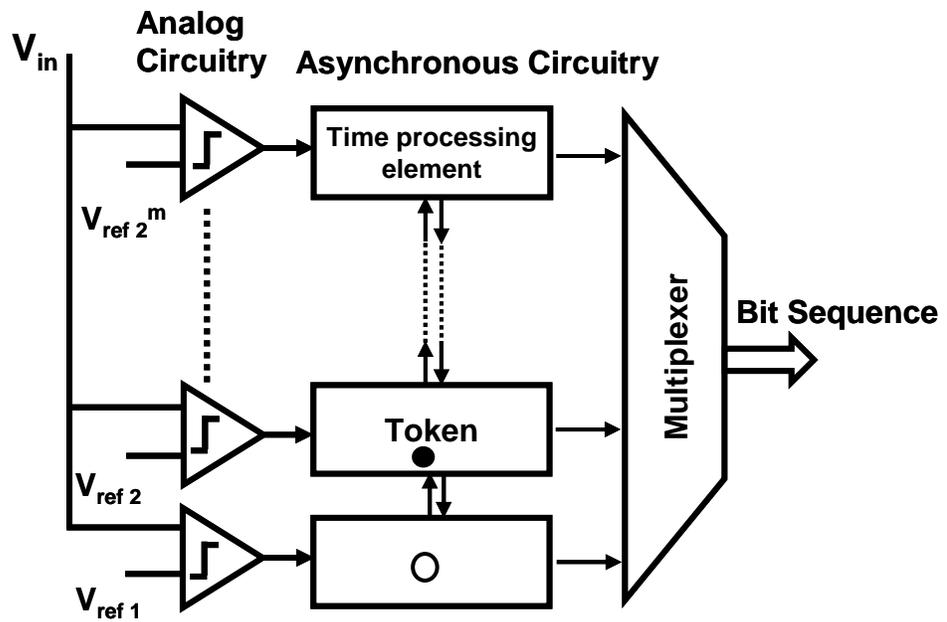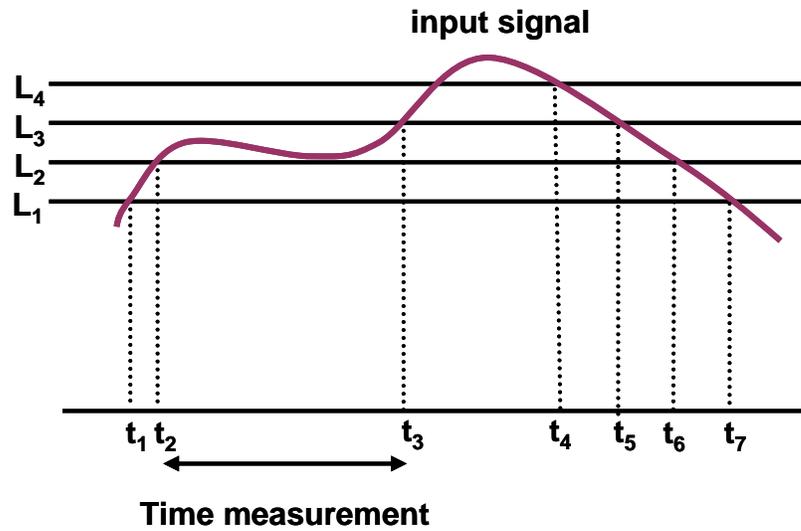
Figure 1.5 : Asynchronous ADC [22]

1.3.4 ADCs based on voltage-controlled delay cell

In this ADC architecture [26], the input signal voltage is first converted to a delay, using a voltage-controlled delay cell and then the delay time is digitized by a time-to-digital converter (TDC), as shown in Figure 1.6. In other words, the delay of the voltage-controlled cell is modulated in a linear way by the input voltage V_{in}. As we see in Figure 1.6, a signal edge (*start*) goes through a voltage-controlled delay cell. The output of this cell (*stop*) is generated after a certain delay (t_d). It is important to realize that t_d is linearly proportional to the input signal (V_{in}) and therefore the TDC output is proportional to V_{in}. Designing a linear voltage-controlled delay cell with a fairly large dynamic range is a challenging task.
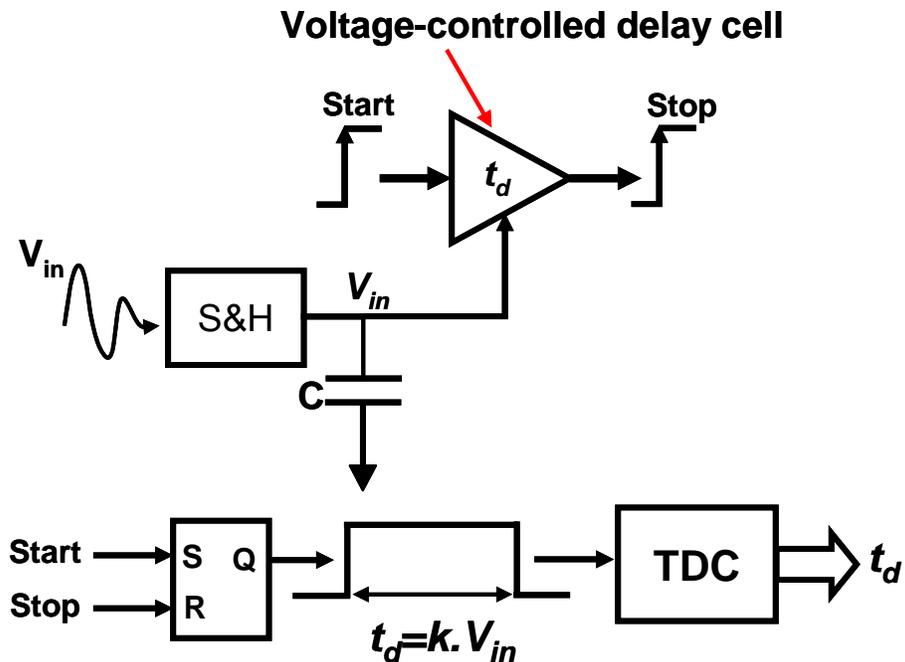
Figure 1.6 : TDC-based ADC with linear voltage-controlled delay cell

1.3.5 ADCs based on voltage-to-frequency conversion

In a voltage-to-frequency-conversion based ADC architecture, the input signal is converted to frequency (or phase) and then quantized by a frequency (phase) quantizer. The main challenge is the precision and linearity of the voltage-to-frequency conversion. Typically, this time-based ADC uses a voltage-controlled oscillator (VCO) as a voltage-to-frequency converter where the frequency is controlled by the analog input voltage (V_{in}) [27, 28]. During a limited amount of time, t_{sample}, the output of the VCO is fed to a counter which detects the rising edges of the VCO output and accordingly quantizes the frequency. The counter output is processed by a mapping table which stores the characteristics of the VCO. The resolution of the ADC is determined by the maximum and minimum VCO frequency and t_{sample} as:

$$\text{Resolution} = \log_2 \left(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}} \right), \qquad [1.1]$$

where, f_{sample} is the inverse of t_{smaple} and f_{max} and f_{min} are the maximum and minimum VCO frequency respectively.

In order to increase ADC speed and resolution, a multiphase VCO such as a ring VCO can be employed (see Figure 1.7). During the sampling period, the VCO converts the analog input voltage to phase. The output is coarsely quantized by a counter, counting rising and falling edges. The residual phase or coarse quantizer error is quantized by the phase detectors tapped to different stages of the ring oscillator. Assuming N_{cell} stages in the ring VCO, the resolution is modified to:

13

$$\text{Resolution} = \log_2 [(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}}) \cdot 2N_{cell}] \qquad [1.2]$$
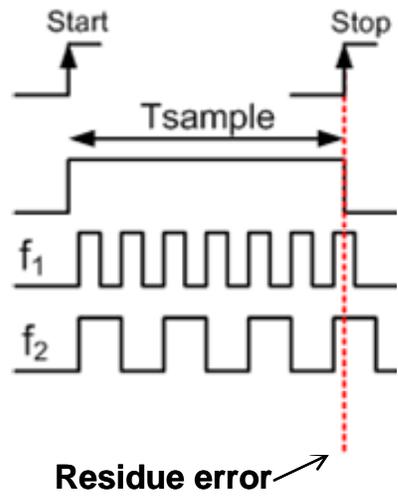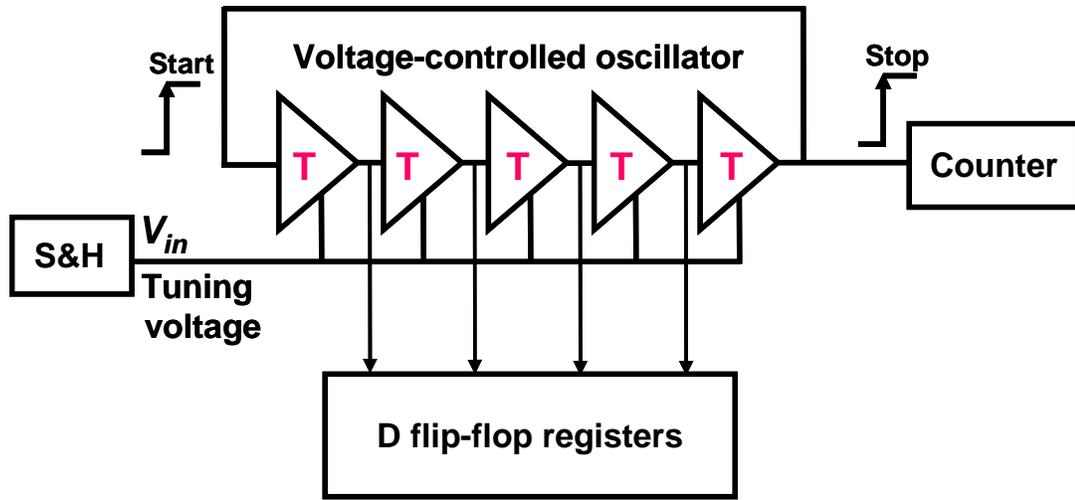
Figure 1.7 : VCO-based ADC

There are many challenges involved in implementing these architectures such as jitter, linearity of the VCO, and process, voltage-supply, and temperature (PVT) variations. The main advantage of this architecture is that the VCO acts as the voltage to frequency converter and quantizer at the same time. The VCO along with a pulse counter can work as a high-speed quantizer. A VCO also produces first-order noise shaping, because the phase of the output pulse is an integrated quantity of the input voltage [29-31]. Most VCOs suffer from a nonlinear relationship between the input voltage and output frequency. To improve linearity, the VCO can be configured with feedback as a 2nd order $\sum\Delta$-ADC as shown in Figure 1.8. High resolution and relatively fast $\sum\Delta$ADCs have been reported using this architecture [29, 30, 16].
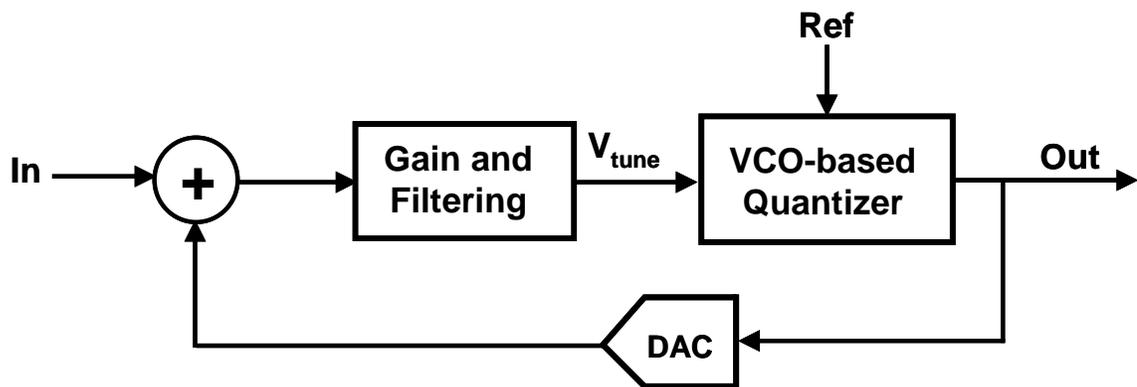
Figure 1.8 : VCO-based $\sum\Delta$ADC

CHAPTER 2

TIME-TO-DIGITAL CONVERTERS

This chapter reviews some common time-to-digital (TDC) circuit architectures. TDCs are important blocks in most time-based ADCs. The focus is on qualitative explanation, and more quantitative derivations are presented in Chapter 4.

2.1 Background

TDC systems have application in a large number of time measurement systems and subsequently have a variety of industrial and research applications. They are widely used in digital storage oscilloscopes, logic analyzers and high-energy particle physics experiments [32]. The simplest form of a TDC is a digital counter. However, to achieve a high resolution TDC, one needs to use a very high frequency counter for a wide dynamic range, and this is not necessarily energy efficient. The resolution of counter-based TDCs can be improved significantly by resolving the counter residual error with a high resolution fine TDC based on gate delay. These fine TDCs and various CMOS tapped delay line configurations are discussed in this chapter.

CMOS delay line methods [33] are very appealing since these require nothing more than a standard digital CMOS process. Since a logic buffer or inverter delay is used as the time unit in these architectures, very high resolution TDCs can be obtained and the

time resolution gets better with the advancement of the technology, despite the reduction in the voltage supply.

2.2 Digital delay line TDC

The principle of a TDC using digital delay lines is shown in Figure 2.1. Our purpose is to measure the time interval between two events indicated by the signal edges: *start* and *stop*. The earlier pulse, *start* propagates in a delay line which consists of a series of buffers. The buffer outputs are the inputs of a series of D flip-flops (see Figure 2.1). The rising edge of the second pulse, *stop*, latches the status of the delay line. The D flip-flop outputs form a thermometer code showing the distance between *start* and *stop* rising edges. The time resolution is limited to the smallest buffer delay obtained in the technology which is used to implement the delay line. The buffer elements are commonly implemented as voltage-controlled delay cells. A delay-locked loop (DLL) can be used to stabilize the buffer delay against process, temperature and power supply variations [34].
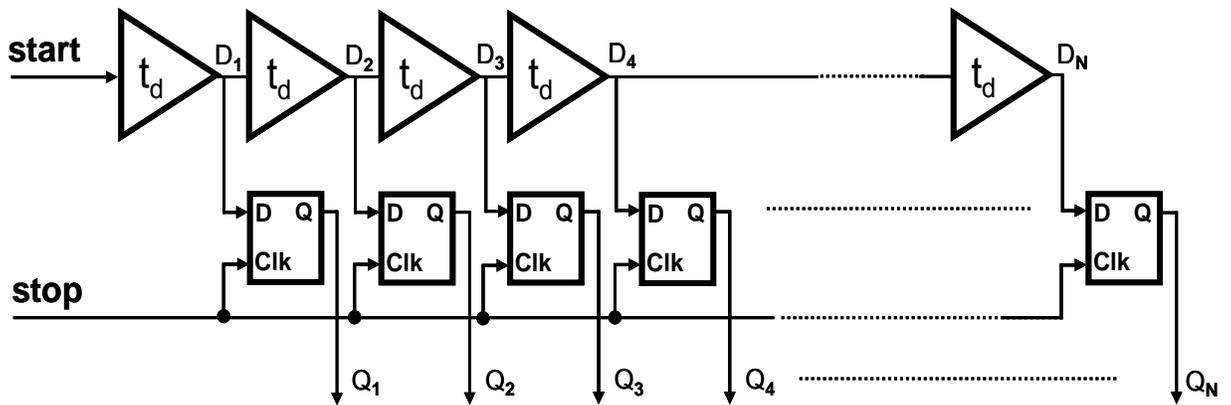
Figure 2.1 : Delay line TDC

Random variations of the delay elements, caused by the device mismatch, due to the process parameter variation, are a source of differential nonlinearity (DNL). This is accumulative as the signal propagates along the delay line. INL increases from the start of the delay line and goes back to zero at the end of the line since the last delay is matched to the DLL reference clock [35]. Therefore, the maximum INL occurs in the middle of the delay line and is proportional to the square root of delay line length or:

$$INL_{max} \propto \sqrt{n} \ .$$

[2.1]

Based on 2.1, having a long delay chain degrades the INL.

The setup time and metastability rate of the sampling D flip-flops can cause errors in the time measurement in the same way comparator metastability limits least significant bit (LSB) resolution of a typical flash ADC architecture. To ensure proper measurement along the delay line, the flip-flops should have a narrow metastability window. In fact, the flip-flop metastability window should be much smaller than the time unit delay of the delay chain or TDC LSB. Generally, sense-amplifier based flip-flops [36, 37] are used in high resolution delay line TDCs, since these can be designed to have a narrow metastability window.

2.3 Inverter-based delay line TDC

In the delay line TDC described above, the unit delay is limited to a buffer delay. Since the buffer is composed of two inverters, an inverter-based TDC can potentially double the buffer-based TDC resolution. An inverter-based TDC example [36] is

illustrated in Figure 2.2. Both *start* and $\overline{start}$ are propagated along the delay line. The polarities of the differential flip-flops are swapped in each stage since we have two signal edges traveling. In order to avoid any phase mismatch between *start* and $\overline{start}$, an edge aligner is used [36]. As we see in Figure 2.2, *start* is inverted in the lower chain as $\overline{start}$ and is sent to a latch along with *start*. The contention in the latch feedback causes the *start* rising (falling) edge to get aligned with $\overline{start}$ falling (rising) edge. The flip-flop outputs generate a thermometer code.
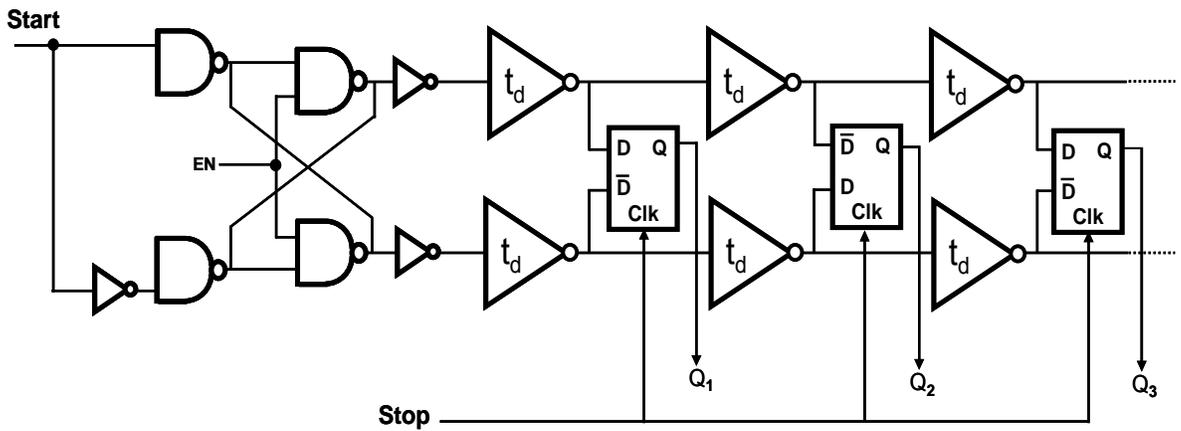
Figure 2.2 : Inverter-based delay line TDC

2.4 Vernier Oscillator TDC

The Vernier Oscillator time-to-digital conversion method is based on two startable oscillators running at two different frequencies [38-40]. The difference in the frequencies defines the time resolution. The oscillators are triggered by *start* and *stop* signals. Since the period of the *stop* oscillator is shorter, the phase of the *stop* oscillator

gradually catches up with phase of the *start* oscillator. The number of clock cycles it takes for the two oscillator phases to align is counted by a counter. The Vernier oscillator technique is illustrated in Figure 2.3. One of the oscillators is triggered by the earlier signal, *start*, with oscillation period of t_s and the other oscillator has a shorter period, t_f and is triggered by *stop*. As we see in Figure 2.3, T_{in} is the time interval between *start* and *stop*. After N cycles of t_f, the two rising edges of the oscillators will be aligned and $T_{in} = N \times (t_s - t_f)$.
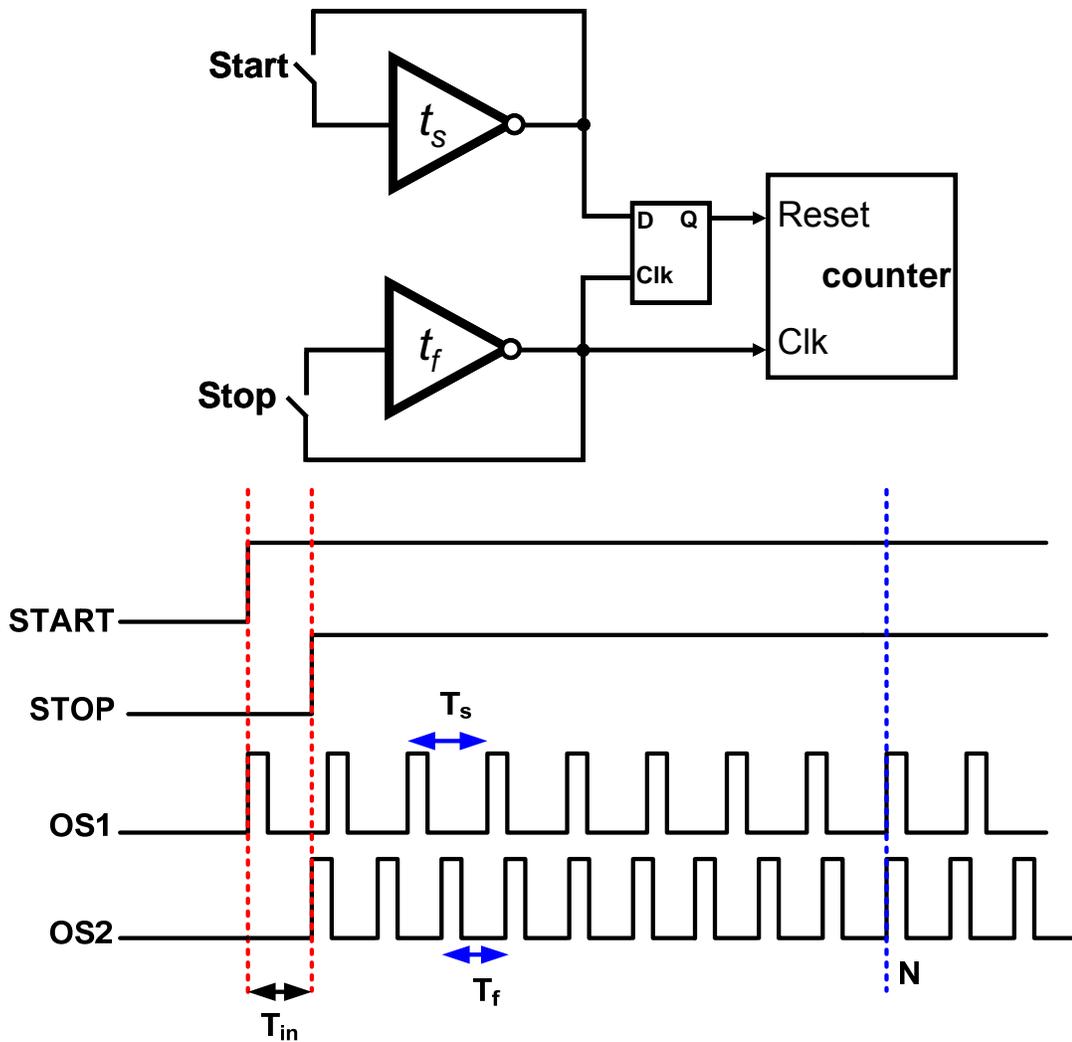
Figure 2.3 : Vernier oscillators

2.5 Vernier delay line TDC

The resolution achievable, in the digital delay lines we have shown, is limited to a gate delay (either buffer- or inverter-based), which is accordingly limited by the speed of the technology in use. A delay line consisting of two parallel elements, with different delays as a Vernier delay line, can be used to overcome this problem [38-42]. The basic configuration is shown in Figure 2.4. The goal is to measure the time interval between *start* and *stop*. There are two parallel delay chains. The delay of the buffer in the upper chain is t_1 and is slightly greater than the delay of the buffer in the lower chain t_2. The *start* and *stop* travel through the delay chains until they become aligned. The position '*n*' in the delay line at which *stop* catches up with the *start* signal, shows the time distance between *start* and *stop* as

$$d = n \cdot t_R \quad , \quad t_R = t_1 - t_2 \ , \qquad\qquad [2.2]$$

t_R is the time resolution of measurement and it can in theory be made very small, irrespective of the CMOS technology in use. In practice, a very small t_R requires a long delay chain which can suffer from a large INL, as stated earlier.
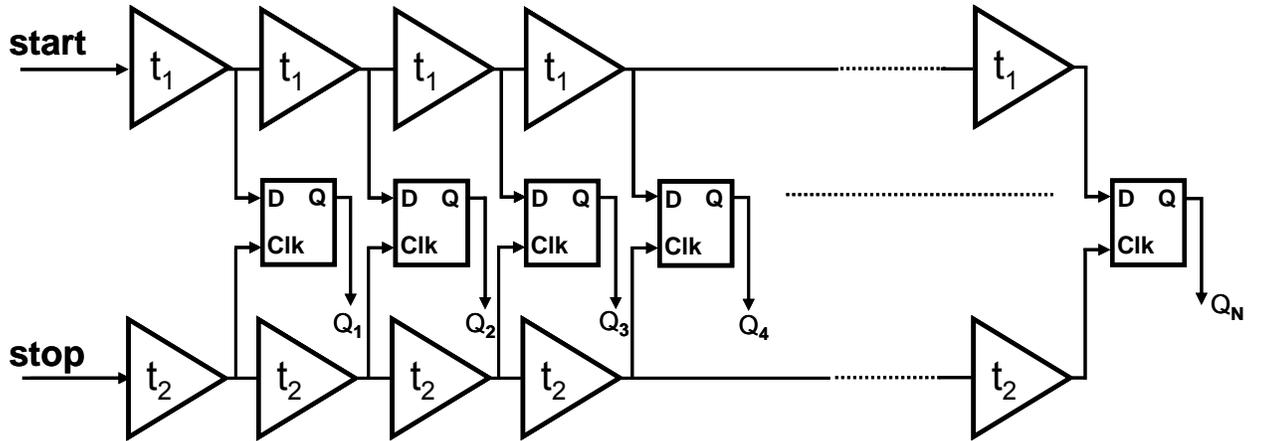
Figure 2.4 : Vernier delay line TDC

2.6 Hybrid TDC

The delay line TDCs discussed so far can be used to measure a short time interval with high resolution. To measure a long period of time, the delay line must be very long, which degrades INL, and therefore resolution, significantly. However in some applications, there is a need to simultaneously measure a wide time range with a high resolution. To obtain this goal, a counter is used as a coarse quantizer and a delay line TDC is employed as a fine quantizer resolving the residual error of the counter measurement [35, 43 and 44]. This is shown graphically in Figure 2.5. The time interval t_m is measured by a counter, which is clocked with a clock period t_c. For simplicity, we assume the starting point is synchronous with the clock. As we see in the example in Figure 2.5, counter measures t_m as $3.t_c$, however there is a residual error, t_d, of this coarse quantization. The error, t_d can be resolved by a delay line TDC to get finer resolution. This hybrid structure is used in our prototype PPM ADC and is discussed extensively in the next chapters.
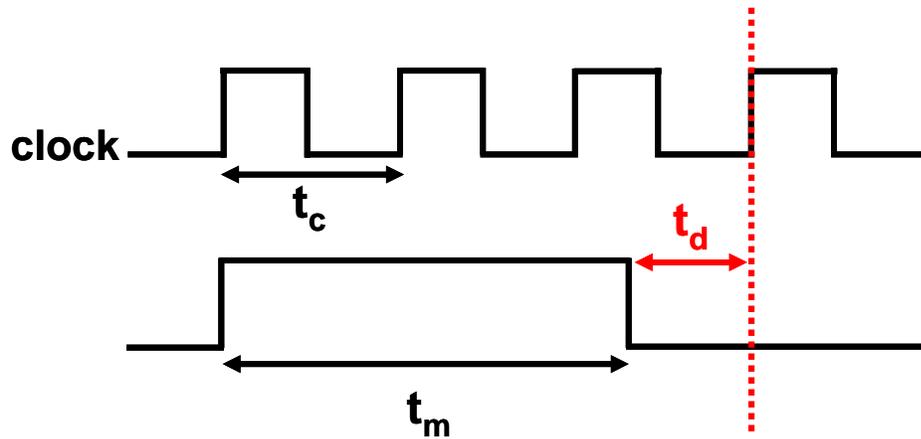
Figure 2.5 : Counter residue error.

The coarse time measurement using a counter is dependent on the clock frequency (f_c) and the fine time measurement is related to the gate delay. In implementing a two-step TDC, the gate delay and clock frequency must be related. In order to relate these two, the delay line TDC needs to be adjusted to the clock period (t_c). In other words, the delay line should be used to interpolate time fractions of one clock cycle. This can be done by including the delay chain in a closed control loop or a DLL shown in Figure 2.6 or by using online or offline calibration cycles in which the delay chain is calibrated with a clock reference -this approach is explained in detail in Chapter 4.
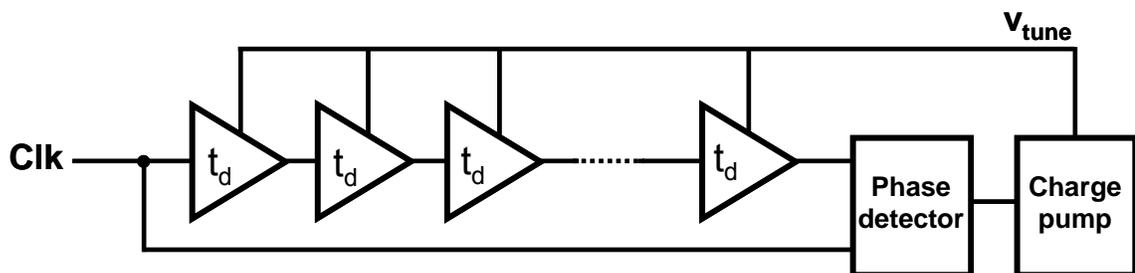
Figure 2.6 : Delay line TDC inside a DLL.

CHAPTER 3

TIME-DOMAIN AND VOLTAGE-DOMAIN ADC CIRCUITS

In this chapter, we compare power consumption of time-domain and voltage-domain ADC circuits. This study helps us to choose the more appropriate architecture before starting the design of an ADC. In particular, we look at the flash ADC architecture in the voltage domain and, its analog, operating in the time-domain and compare the minimum possible power consumptions in the thermal noise-limited regime.

3.1 Voltage-domain flash ADCs

In voltage-domain flash ADCs (see Figure 3.1), we need 2^B-1 comparators to achieve a conversion resolution of B bits. The voltage input is compared with different reference voltage levels and the outputs of the comparators collectively form a thermometer code. Assuming that f_s is the sampling frequency, the comparator conversion should be done no later than $1/2f_s$. In addition, each individual comparator must be able to resolve a fraction, α, of one LSB (i.e., $V_{ref}/2^B$) in the time duration less than $1/2f_s$. In order to simplify our analysis and relax the requirement of the voltage-domain flash ADC, we have assumed α=1. As we see in the next section, the equivalent assumption for time-based ADCs is to neglect the metastability requirment for the sense-amplifier-based flip-flops.
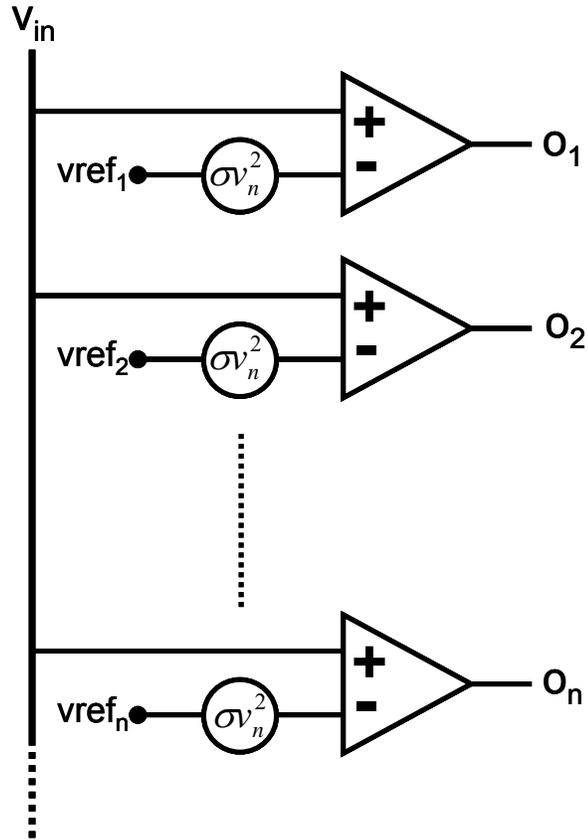
Figure 3.1 : Voltage-domain flash ADC

To further analyze this system, we assume that dynamic comparators (e.g., latch circuits) are used, as illustrated in Figure 3.2. The outputs of dynamic comparator are initially pre-charged to V_{DD} (i.e., during *clk*='0'). At the onset of the conversion (i.e., *clk*='1'), the regenerative latch pulls the output exponentially toward either zero or V_{DD} based on the difference between the input and the associated reference voltage at that comparator. The comparator delay, T_d, to resolve a single LSB, can be defined using the following equation

$$V_{DD} 2^{-B} \cdot e^{\frac{T_d}{\tau}} = V_{DD}.$$ [3.1]

The parameter τ, is the comparator regeneration time-constant and equal to C/g_m, where C is the output capacitive load, and g_m is the small signal transconductance of the comparator at the onset of the conversion (see Figure 3.2).
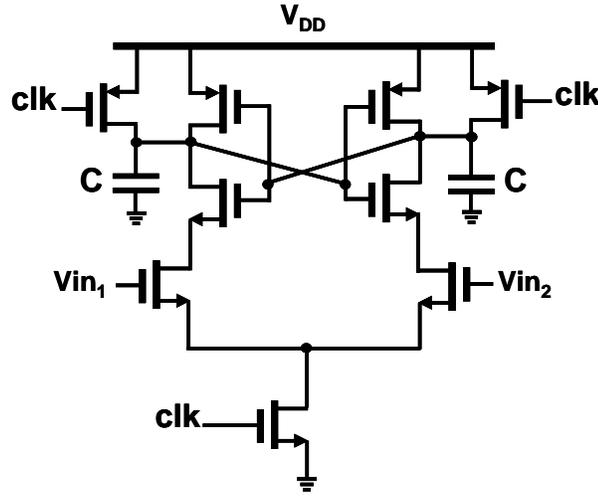
Figure 3.2 : Dynamic comparator

The comparator transconductance, g_m, and the overall DC current, I_D, have the following relationship [45]:

$$I_D = g_m \cdot V_{eff},$$ [3.2]

Where, V_{eff} is $\dfrac{V_{GS} - V_{th}}{2}$ in the square law model and is set to 80-100mV in sub-micron transistors for better efficiency [45]. By replacing τ with C/g_m, and g_m with I_D/V_{th} in 3.1, the minimum DC current, I_D, becomes

$$I_D = 2f_s \cdot B \cdot C \cdot \ln 2 \cdot V_{eff}.$$

[3.3]

It is important to realize that 3.3 is derived based on the speed specification of the flash structure. Nevertheless, thermal noise presents another constraint on this system. It has been previously shown that the input-referred noise of the dynamic comparator can be derived as [46]

$$\sigma_{vn}^2 = \kappa \frac{kT\gamma}{C},$$

[3.4]

where κ is architecture-dependant parameter and γ is process-dependant parameter related to thermal noise. In this analysis, we assume both κ and γ are '1' to simplify our calculations by considering the worst case possible.

It is widely accepted that in any noise-limited ADC, the minimum power consumption is achieved (no overdesign) when input-referred thermal noise is equal to quantization noise. This indicates that

$$\kappa \frac{kT\gamma}{C} = \frac{V_{DD}^2}{12 \cdot 2^{2B}}.$$

[3.5]

Hence, the minimum capacitance C can be calculated as

$$C = \kappa \cdot 12kT\gamma \cdot \frac{2^{2B}}{V_{DD}^2}.$$

[3.6]

Replacing C in equation 3.3 provides the minimum power consumption of the voltage-domain flash architecture, P_v as:

$$P_v = \left(2^B - 1\right) \cdot 24kT \cdot n \ln 2 \cdot f_s \cdot \frac{V_{eff}}{V_{DD}} \cdot 2^{2B}. \qquad [3.7]$$

The aforementioned analysis method was presented initially in [45]. Here, we adopt the same approach and derive the minimum power consumption of a time-domain flash ADC architecture.

3.2 Time-domain flash ADCs

For the purpose of analyzing time-domain flash ADCs, we consider the architecture illustrated Figure 3.3. As previously discussed in Section 2.2, the input signal edge travels through an active delay line and the comparator outputs form a thermometer code, similar to a voltage-domain flash ADC. The inverters are self-loaded and capacitors C_d represent the input capacitances of the next stage and the comparator input. Again, the conversion must be done in $1/2f_s$. The time resolution of TDC measurements is approximately one inverter delay, denoted by t_d.
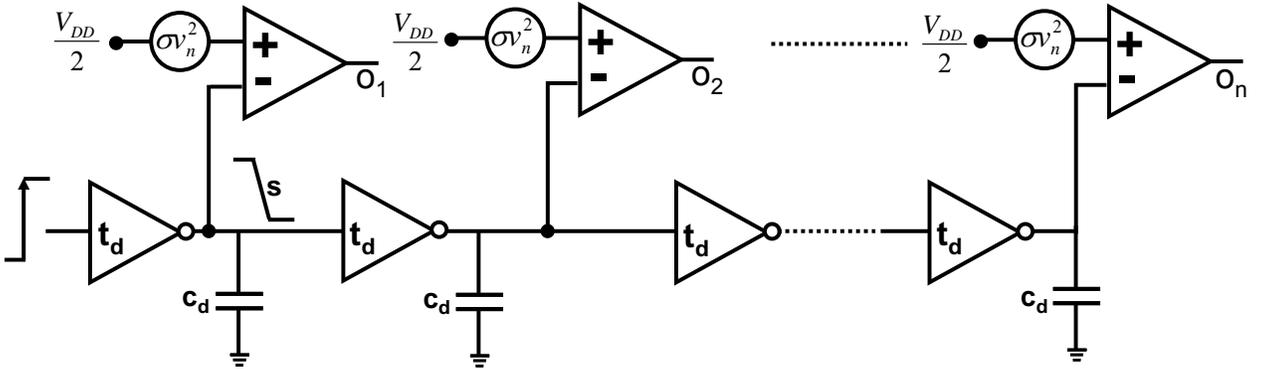
Figure 3.3 : Time-domain flash ADC

Since the conversion is done in the time domain and in a sequential way, the worst case conversion delay (full range input) occurs when the signal has to travel all the way to the end of the delay line. In this case, the conversion delay, $t_{conversion}$, is equal to

$$t_{conversion} = 2^B \cdot t_d + t_{comp} = \frac{1}{2f_s},$$ [3.8]

where t_{comp} is the comparator conversion time. In this time, the comparator resolves $V_{DD}/2$ which is the differential input voltage when we have one input tied to $V_{DD}/2$. It is important to realize that there is another constraint on the comparator speed, which is that the metastability window of the comparator must be smaller than the TDC resolution, t_d. For simplification, we have ignored this requirement as we did in the case of voltage-domain flash ADC.

Now, if we assume that dynamic comparators (Figure 3.2) are also used in this architecture, based on 3.1, we have:

$$t_{comp} = \tau \ln 2,$$ [3.9]

where τ is equal to C_c/g_m and C_c is the capacitive load of the dynamic comparator. Now, we rewrite 3.8 by replacing g_m using 3.2 so that

$$t_{conversion} = 2^B t_d + \frac{C_c V_{eff}}{I_D} \ln 2 = \frac{1}{2f_s}.$$ [3.10]

Deriving I_D from 3.10, we calculate the total comparator power consumption, P_{comp}, as:

$$P_{comp} = \left(2^B\right) \cdot \frac{C_c \cdot V_{eff} \cdot V_{DD} \cdot \ln 2}{\dfrac{1}{2f_s} - 2^B t_d} . \qquad\qquad [3.11]$$

Consequently, the total power consumption of the delay line (2^B inverters) and of the 2^B comparators, denoted by P_T, is equal to:

$$P_T = 2^B \cdot C_d \cdot V_{DD}^2 \cdot f_s + \left(2^B\right) \cdot \frac{C_c \cdot V_{eff} \cdot V_{DD} \cdot \ln 2}{\dfrac{1}{2f_s} - 2^B t_d} , \qquad\qquad [3.12]$$

where first term in the RHS of 3.12 describes the power consumed by the inverters of the delay line. This term is calculated based on the fact that for each input sample taken at f_s, the signal edge has to travel all the way to the end of the delay line and toggle all 2^B inverters. The second part in the RHS of 3.12 comes from 3.11 and represents the power consumed by the comparators.

At this point, we consider thermal noise to assess the minimum power consumption. Generally speaking, thermal noise manifests itself as jitter in time-domain circuits. Individual jitter sources originate from each inverter, and these can be considered independent. [47] calculates the total jitter noise at the inverter output, and by rearranging the formulas in [47] we can calculate the inverter jitter, σ^2_{jinv}, with the following equation:

$$\sigma^2_{jinv} = \left(\frac{8kT\gamma}{CV_{DD}(V_{DD} - V_{th})} + \frac{4kT}{CV_{DD}^2} \right) \cdot t_d^2 . \qquad\qquad [3.13]$$

Comparators also introduce additional jitter. The jitter variance caused by the dynamic comparator, σ^2_{jcomp}, can be approximated by the comparator input-referred noise power, σ^2_{ncomp}, divided by the square of the inverter slope, s, as:

$$\sigma^2_{jcomp} = \frac{\sigma^2_{ncomp}}{s^2} \, . \qquad [3.14]$$

Assuming that the inverter output goes from zero to $V_{DD}/2$ in t_d, s is

$$s = \frac{V_{DD}}{2t_d} \, . \qquad [3.15]$$

Using 3.4, we have,

$$\sigma^2_{jcomp} = \frac{kT}{C_c} \cdot \frac{4t_d^2}{V_{DD}^2} \, . \qquad [3.16]$$

The maximum jitter is at the end of the delay line, where we observe the aggregate jitter of all the previous inverter stages. Since the inverter and comparator noise can be considered uncorrelated, the total jitter noise in the last stage of the delay line, σt_{jtotal}, is

$$\sigma^2_{jtotal} = \sigma^2_{jcomp} + 2^B \cdot \sigma^2_{jinv} \, , \qquad [3.17]$$

or

$$\sigma^2_{jtotal} = \left(\frac{2^B \cdot 8kT\gamma}{C_d V_{DD}(V_{DD} - V_{th})} + \frac{2^B \cdot 4kT}{C_d V_{DD}^2} + \frac{4kT}{C_c V_{DD}^2} \right) \cdot t_d^2 \, . \qquad [3.18]$$

Similar to calculations for a voltage-domain flash ADC, the minimum power consumption is achieved when the time-domain quantization-noise power is equal to this maximum jitter power; hence

$$\sigma_{jtotal}^2 = \frac{t_d^2}{12} \ .$$

[3.19]

By combining 3.18 and 3.19, we get

$$\frac{\sigma_{jtotal}^2}{t_d^2} = \left(\frac{2^B \cdot 8kT\gamma}{V_{DD}(V_{DD} - V_{th})} + \frac{2^B \cdot 4kT}{V_{DD}^2} \right) \cdot \frac{1}{C_d} + \left(\frac{4kT}{V_{DD}^2} \right) \cdot \frac{1}{C_c} = \frac{1}{12} .$$

[3.20]

It is important to realize that in this analysis, we ignore the parasitic capacitance of wires and other similar non-idealities. Therefore we can estimate the input inverter capacitance, C_d, for the minimum achievable inverter delay, t_d, for each CMOS technology. The comparator capacitance, C_c, is subsequently computed based on the allowed amount of jitter, using 3.20. Having C_d and C_c, we can then examine the minimum total power from 3.12 at different sampling frequencies.

3.2 Comparison between time-domain and voltage-domain flash ADC

The minimum power consumption of time- and voltage-domain Flash ADCs structures (P_V and P_T, respectively) for three different technology nodes is compared and plotted here for f_s=10MHz (see Figure 3.4). This sampling frequency is chosen so that the time-domain flash ADC can be implemented in all three CMOS technology nodes. In other words, it should be low enough to be feasible in 0.35μm CMOS. As evident, in 0.35μm

CMOS, the voltage-domain flash ADC has lower power consumption in the conventional flash architecture resolution range (i.e, below 9 bits). When we move to 90nm CMOS technology, the power of voltage-domain flash ADC becomes larger than the power of time-domain flash ADC at approximately 8.5 bits of resolution. Moving to 45nm CMOS, this crossover happens at a lower resolution, around 7.5 bit. This comparison suggests that, in theory, time-based architectures are more efficient in advanced technologies with smaller gate lengths. This conclusion, can be a guidline as to when one should consider replacing voltage-domain circuits with time-based alternatives for each CMOS technology. Intutively, as the voltage supply is dropped, the voltage level detection gets more challenging in presence of amplitude noise (e.g., voltage and current thermal noise). However, when we tranfer the signal to time, the circuit works with the full supply voltage and hence is not affected by amplitude noise.

It is imperative to recognize that the preceding analysis is carried out for the noise-limited circuit conditions. A similar approach can be used for the mismatch-limited circuit condition. It should also be noted that, the sample-and-hold circuit in voltage-domain flash ADC is not included in the formulations describing the total power consumption. In the same way, the voltage-to-time conversion function is not included in the analysis of time-domain flash ADC architectures.
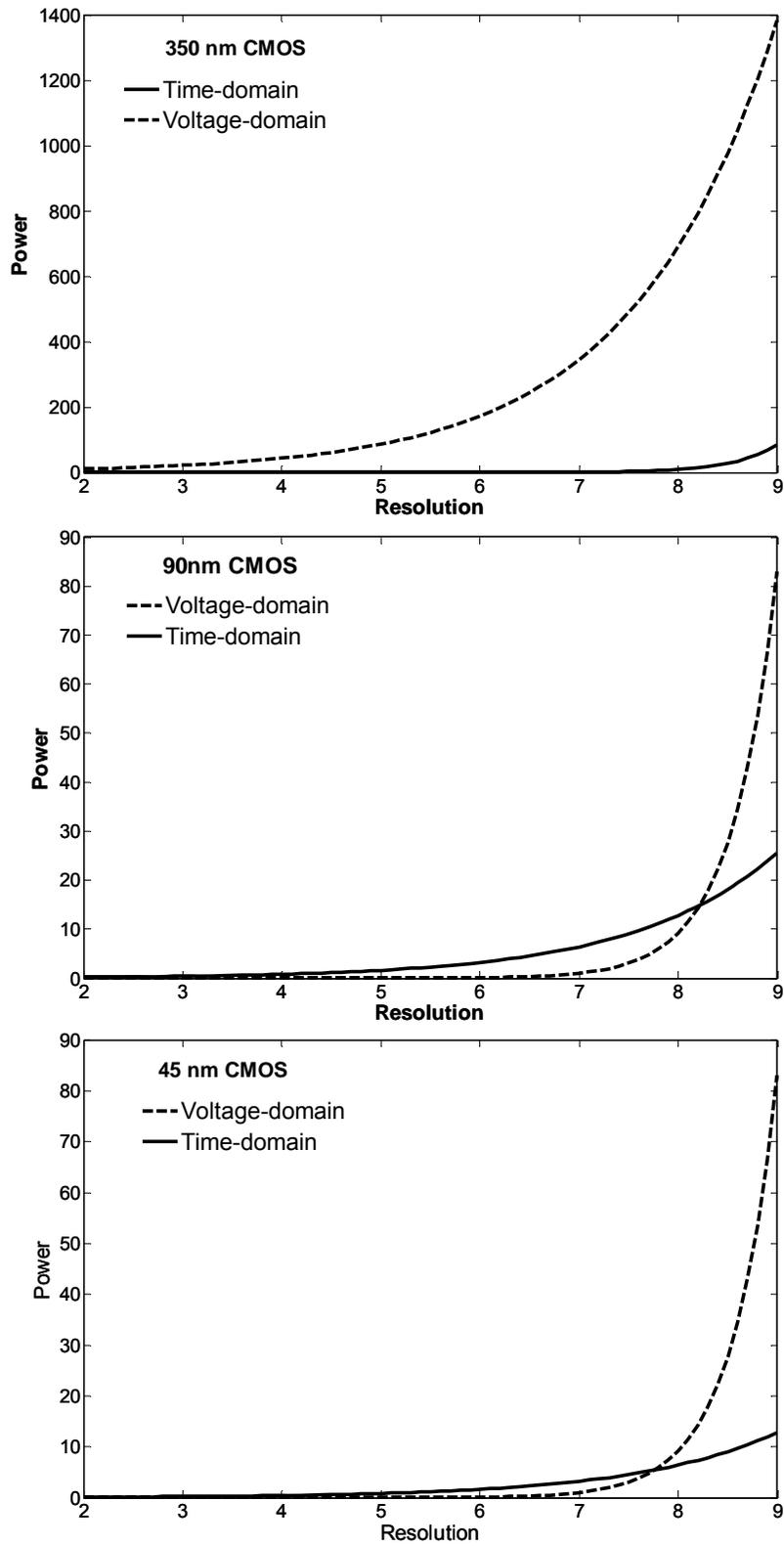
Figure 3.4 : Time-domain and voltage-domain minimum power comparison

CHAPTER 4

PULSE POSITION MODULATION ADC

This chapter introduces the concept of the pulse position modulation (PPM) ADC. First, the ADC operation is described and typical waveforms are presented. Next, the top level ADC architecture and the building blocks are discussed in detail. Finally, two prototypes are presented and the experimental results are discussed.

4.1 PPM ADC architecture

The concept of the PPM ADC is shown with the main waveforms in Figure 4.1. The input signal is continuously compared with a ramp voltage. At the time of the intersection between the input signal and the ramp, an output pulse is generated. The time interval between the ramp starting point and the instant the input signal crosses the ramp (i.e. $[t_1, t_2, t_3, …]$) in Figure 4.1 is measured by a time-to-digital converter. Assuming the ramp slope is constant, the time vector $[t_1, t_2, t_3, …]$ is proportional to the signal amplitude at the cross over points. If we sample the signal at the starting point of the ramp we would have the input signal amplitudes at $[s_1, s_2, s_3 …]$ uniformly. However, in a PPM ADC, measuring $[t_1, t_2, t_3, …]$ results in non-uniform samples of the signal given as time and amplitude pairs of $[(t_1,a_1), (t_2,a_2), (t_3,a_3), …]$.
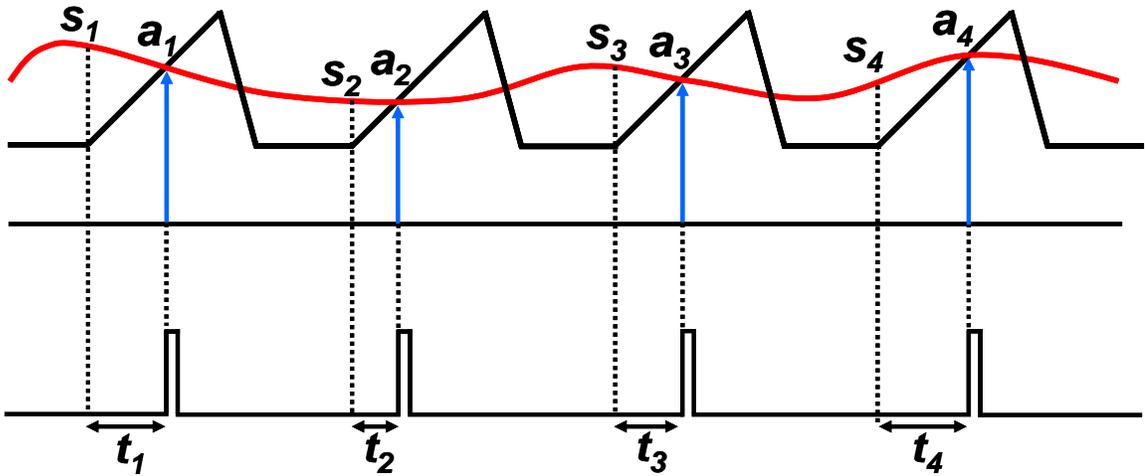
Figure 4.1 : PPM ADC typical waveforms

Due to the non-uniform sampling nature of the PPM ADC, we have harmonic distortion in the output frequency spectrum of the ADC as shown in Figure 4.2. This frequency spectrum is derived assuming the samples are uniform (uniform FFT).
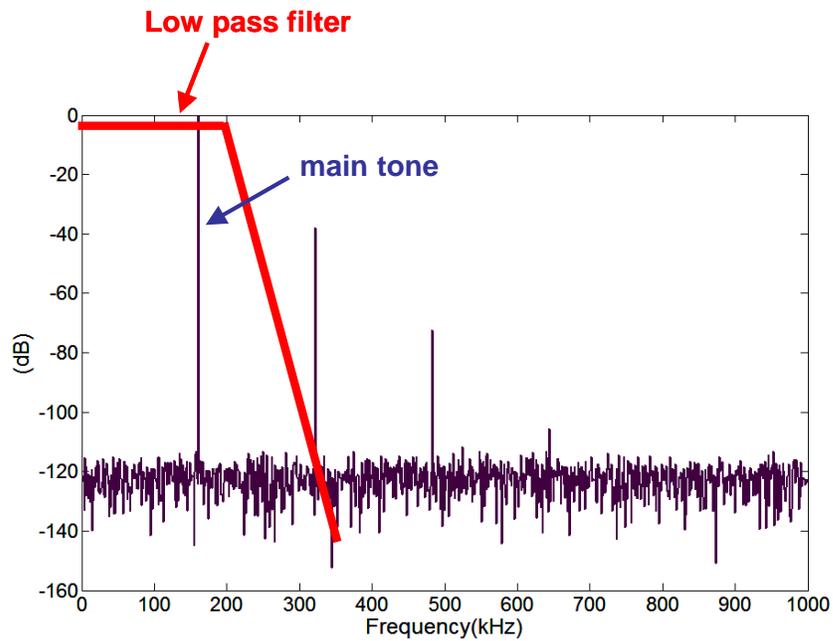
Figure 4.2 : PPM ADC frequency spectrum

Linear low pass filtering (in the digital domain) is a traditional way of reconstructing the original analog input signal in PPM ADCs (Figure 4.2) and for this an oversampling ratio of 8 or higher is generally required [20]. Another approach is to rely on a time-varying/nonlinear recovery technique so that we can sample the signal at a frequency close to the Nyquist rate [20]. This way we can sample higher input frequencies with lower power consumption, but at the cost of more complexity in digital post processing. The nonlinear recovery technique or reconstruction algorithm [48] is extensively discussed in Appendix A.

4.2 PPM ADC block diagram

The PPM ADC block diagram is depicted in Figure 4.3. The input signal is compared with a ramp voltage by a continuous time comparator and the comparator generates pulses shown in Figure 4.1. The time intervals [t_1, t_2, t_3, ...] are encoded by a TDC. Employing a TDC for quantization saves substantial power and area since the TDC consists of digital blocks such as inverters, flip-flops, and counters. These digital blocks consume power only during switching activity, i.e., dynamic power. In comparison, pre-amplifiers and comparators, used in conventional analog architectures, consume constant DC power during their operation.
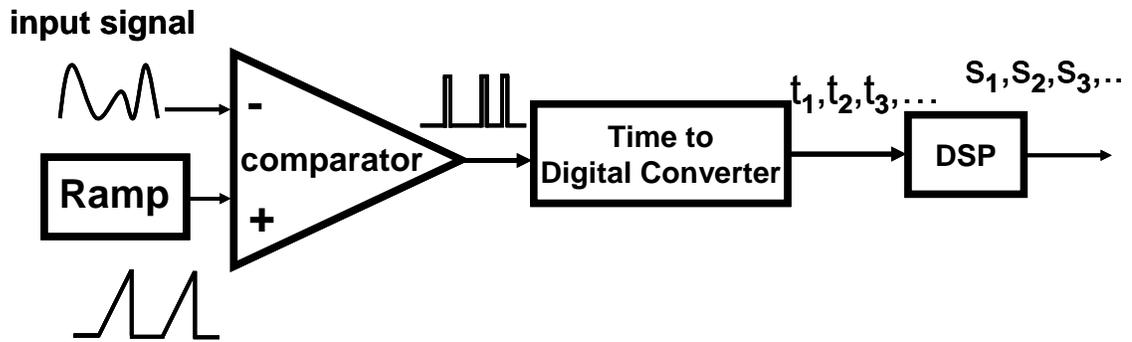
Figure 4.3 : PPM ADC block diagram

4.3 PPM ADC vs. slope ADC and synchronous ADC

The PPM ADC is a hybrid synchronous/asynchronous architecture. In an asynchronous ADC [21-25] there are different reference levels and comparators as shown in Figure 1.5. As the signal passes through different levels, the time between crossings is recorded. The outputs of these ADCs are a set of non-uniform samples. To reiterate, an interesting characteristic of the level-crossing or asynchronous ADCs is that the ADC power consumption is proportional to the signal activity. If the input signal remains silent for a while, no threshold level is crossed, resulting in no digital power consumption. A PPM ADC does not have this advantage; however, different reference levels and multiple comparators are not required since the ramp sweeps the entire input voltage range. In addition, the use of a single comparator eliminates, to a first order, considerations of comparator offset and mismatch. Also, the use of a clock-synchronous ramp signal removes the requirement for asynchronous digital protocols [21-25], reducing power consumption and area.

In a single-slope ADC, shown in Figure 1.3, the signal is uniformly sampled by a sample-and-hold block and the time it takes for the sampling capacitor to be discharged is measured. Accordingly, there are two linearity constraints in a single slope ADC; the

first is the sample-and-hold linearity and the second is the discharging current linearity. The current linearity requirement is the same as the ramp linearity in the PPM ADC; however, the sample-and-hold linearity is not critical in a PPM ADC, since the input signal is continuously compared with the ramp input. Instead, there are some limits on the response time of the continuous time comparator, which are easy to satisfy and will be explained in the next section. The single-slope ADC has traditionally been criticized for its low speed, despite its high resolution, since the time interval measurement accuracy limits the speed. However, using alternative TDC techniques, the single slope ADC's speed can improve significantly, e.g., [3, 4]. Furthermore, this research shows that single-slope ADCs are very promising for the future, due to their reliance on time measurement.

4.4 PPM ADC characterization

4.4.1 ADC resolution

Assuming the ramp slope is constant and the recovery technique works perfectly, the ADC resolution is defined by the TDC resolution. The voltage-to-time conversion accuracy of the PPM system is directly dependent on the linearity of the ramp generator. As a rule of thumb a ramp linearity of at least two bits more than the ADC resolution should be targeted. Supposing the ramp is linear from voltage A to voltage B, as shown in Figure 4.4(a), the input signal amplitude must be limited to the $[A, B]$ range. Assuming the ramp slope is s, the time input range to the TDC is $[B - A]/s$.

In order to guarantee convergence of the recovery algorithm techniques, which is discussed in detail in the appendix, the input time range must be less than $1/(4 \cdot f)$, where f is the ramp signal frequency. The input signal bandwidth is f/n, where n defines the oversampling ratio. As discussed previously, using a simple low-pass filter requires $n \geq 8$; however, if a nonlinear recovery technique is used, n can be reduced to 2 [48]. Assuming the TDC operates with t_b resolution (LSB in time), ideally we expect an N bit ADC where,

$$N = Log_2(\frac{B-A}{s.t_b}) \hspace{3cm} [4.1]$$
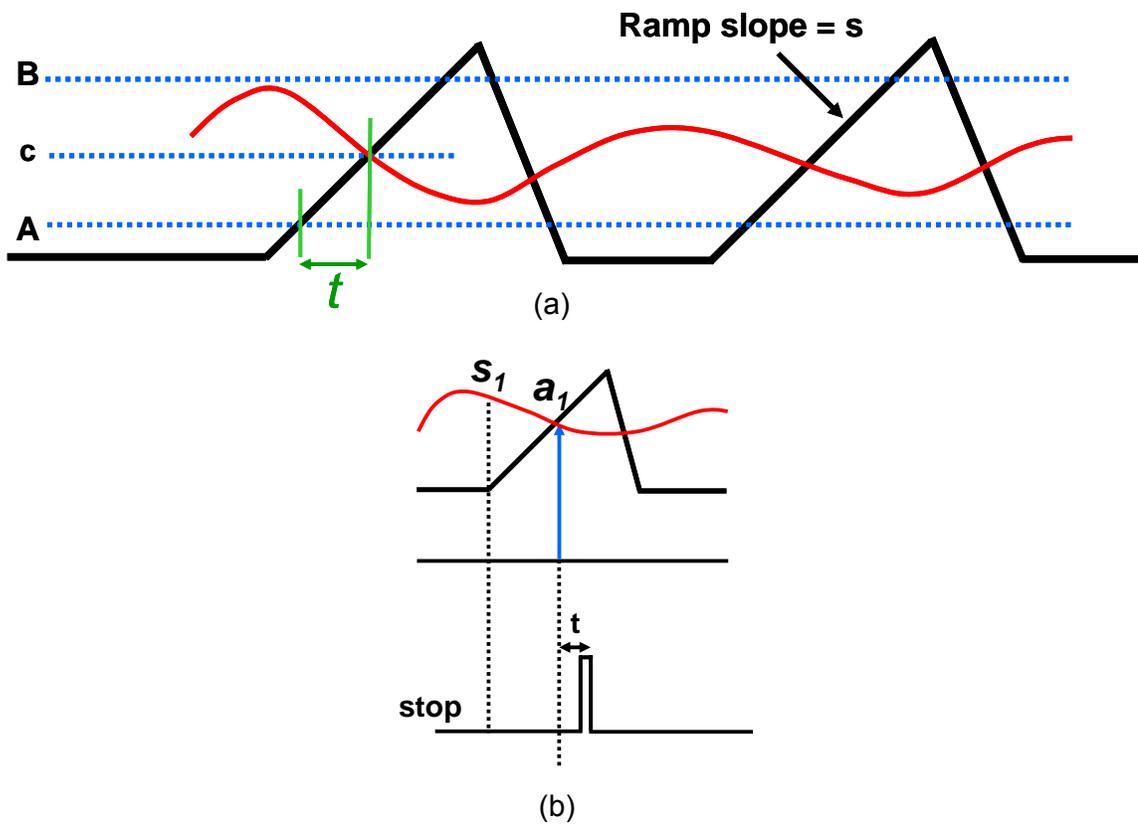
Figure 4.4 : (a) Input dynamic range and ramp linearity, and (b) comparator propagation delay

40

4.4.2 Comparator response time

The continuous time comparator generates a pulse at its output with a delay t, when the ramp and input intersect, as illustrated in Figure 4.4(b). This pulse is generated asynchronously somewhere in the input voltage range $[A, B]$. The comparator propagation delay, t, varies with the input signal level. This propagation delay variation must remain lower than the LSB t_b over the input range $[A, B]$ or $\Delta t \leq t_b$. This is a fundamental impediment found in this time-based ADC architecture. In other time-based ADCs such as single slope ADCs, this does not exist since the ramp and input signal intersection point always happens at a certain voltage (e.g. 0V). Since in single-slope ADC the comparison is always at the same voltage, the comparator propagation delay acts like an offset in the TDC measurement and it is not input signal amplitude dependent.

4.4.3 Jitter noise

Several sources of noise limit the performance of the PPM ADC. The noise generated in the ramp and comparator circuits causes time jitter and degrades the accuracy of the time measurement [49]. There are three primary jitter elements: tj_r, tjc_1, and tjc_2. The first jitter noise, tj_r is caused by the ramp and is

$$tj_r^{\ 2} = \frac{VN_{ramp}^{\ 2}}{s^2} \qquad [4.2]$$

VN_{ramp} is the total noise at the ramp generator output and s is the slope of the ramp. The other jitter elements, tjc_1 and tjc_2 are related to the comparator.

$$tjc_1^{\ 2} = \frac{VN_{comp}^{\ 2}}{s^2} \qquad [4.3]$$

41

VN_{comp} is the input referred noise of the comparator.

$$tjc_2{}^2 = \frac{Vout_{comp}{}^2}{sr^2} \qquad [4.4]$$

$Vout_{comp}$ is the total comparator output noise and sr is the slew rate at the last stage of the comparator.

The total time jitter (t_{jitter}), which appears in time measurement, is defined by the following equation, assuming that tj_r, tjc_1, and tjc_2 are uncorrelated:

$$t_{jitter}{}^2 = tj_r{}^2 + tjc_1{}^2 + tjc_2{}^2 \qquad [4.5]$$

Assuming that T is the input time dynamic range of the TDC or $[B - A]/s$, the TDC resolution (N) limited by signal to noise ratio is:

$$2^{2N} = \frac{T^2}{t_{jitter}{}^2} \qquad [4.6]$$

In the PPM ADC design, it is necessary to minimize tj_r and tjc_1 within the power budget. A compromise has to be made for the ramp slope (s); since increasing the ramp slope reduces jitter but limits the time input dynamic range (T). Jitter noise (tjc_2) is negligible with respect to the other sources, since the inverters at the comparator output have a large slew rate.

4.5 First ADC prototype

Two PPM ADC prototypes were designed and fabricated in this research. In this section, the first design is briefly discussed, accompanied with comments regarding drawbacks and conclusions derived from the chip's actual measurements.

4.5.1 Comparator and ramp circuits

The ramp generator and the continuous time comparator are shown in Figure 4.5. The ramp generator consists of a cascoded current source charging a constant capacitance under the control of digital switches. Since the input signal is compared with the ramp only during charging, there is no requirement to match charging and discharging rates and capacitor discharge is achieved simply with a switch to ground. A cascoded current source is chosen to achieve a fairly constant current during capacitor charging. Simulations indicate that a linearity of 11 bits is achieved over a 600mV ramp range. The linearity of the ramp is measured by looking at its maximum INL (INL_{max}), which is the maximum deviation of the ramp from an ideal linear ramp. If the ramp output range is $[A, B]$, then the linearity in terms of bit resolution, N, can be derived by the following equation [50]:

$$N = Log_2\left(\frac{B-A}{INL_{max}}\right).$$
[4.7]

The continuous time comparator consists of a PMOS input differential amplifier followed by another differential stage. The output of the second stage connects to a buffer stage to create a rail-to-rail digital signal.
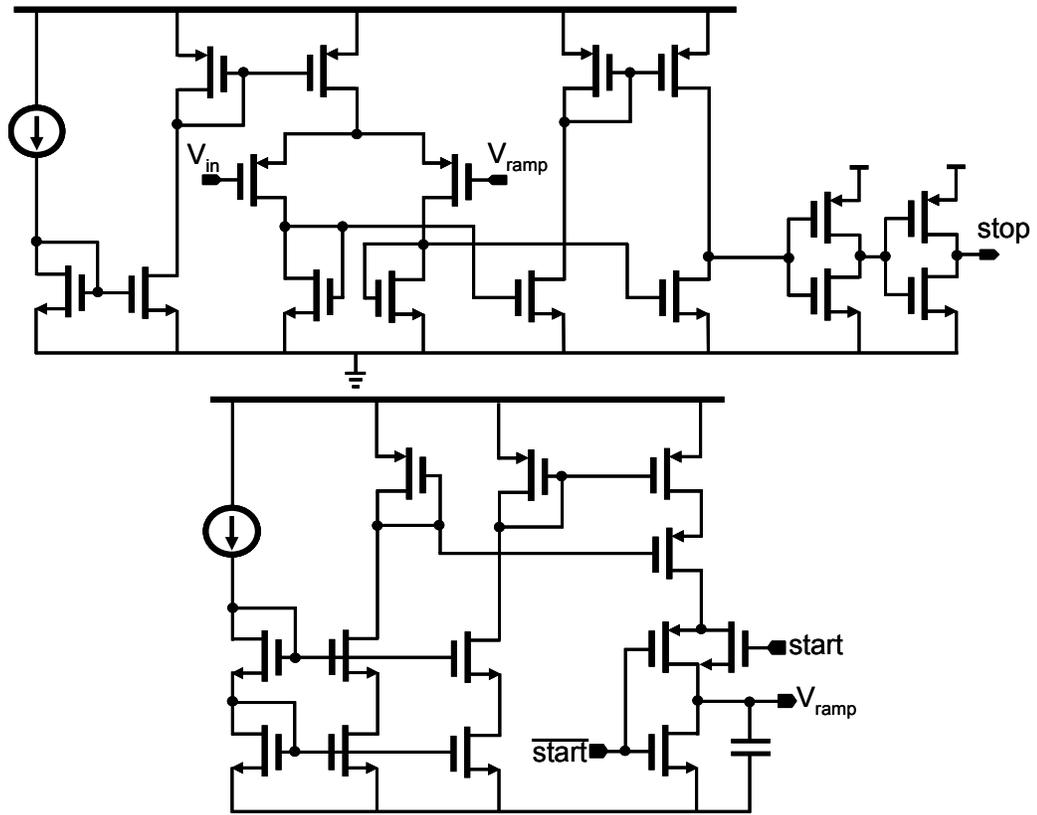
Figure 4.5 : Continuous time comparator and ramp generator

4.5.2 Time-to-digital converter structure

In order to understand the TDC building blocks of our first prototype ADC, one period of

the ramp signal is illustrated in Figure 4.6.
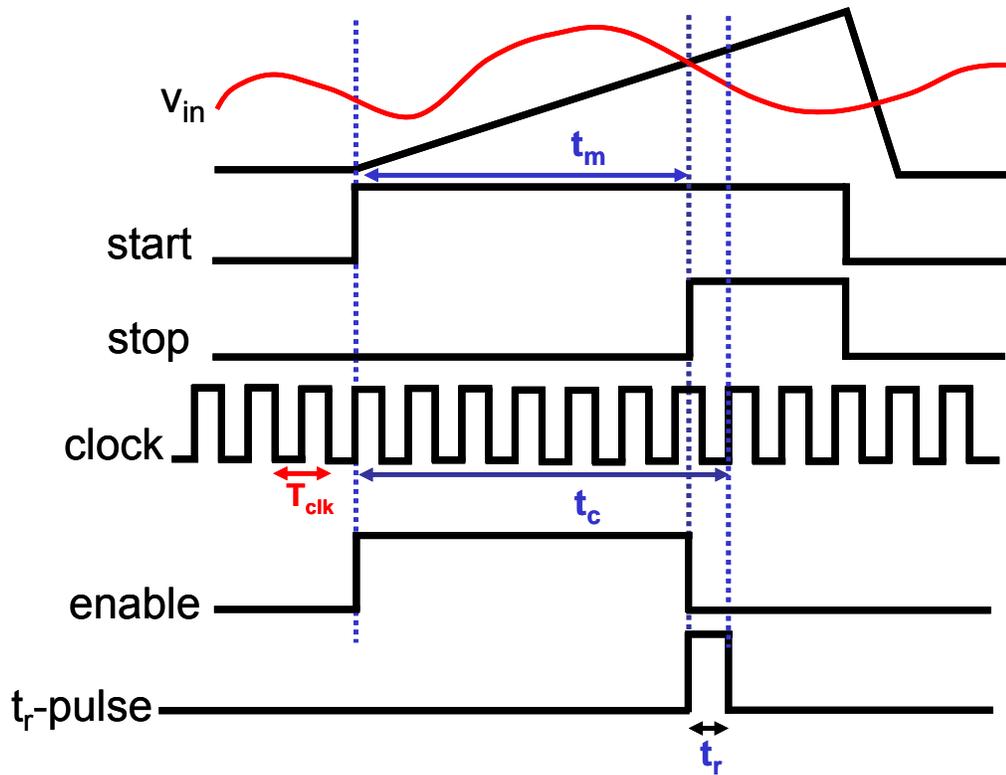
Figure 4.6 : One period of the ramp signal

Our goal is to measure the time interval, t_m, defined by the time difference between the start of the ramp to the crossover point of the ramp and the input signal. The *start* is a signal synchronized with the reference clock, while the *stop* is generated by the comparator. To measure t_m, the time interval between the *start* and *stop* rising edges simply needs to be measured.

In order to measure t_m with high resolution, a two-step hybrid TDC is used. To realize a two-step TDC, two more signals are generated, which are called t_r-*pulse* and *enable* as shown in Figure 4.6. The t_r-*pulse* signal is set by the *stop* signal and is reset by the arrival of the first reference clock (*clk*) rising edge right after the *stop* signal. The *enable* signal is set by the *start* signal and reset by the *stop*. A coarse time quantizer, formed using a counter is activated with *enable* and measures the number of reference clock

cycles while the *enable* is high (t_c in Figure 4.6). A fine TDC block implemented with a

delay line is required to measure, t_r, which is the time interval during which the t_r-*pulse* is

high and needs to be subtracted from t_c to obtain the correct time measurement ($t_m = t_c - t_r$).
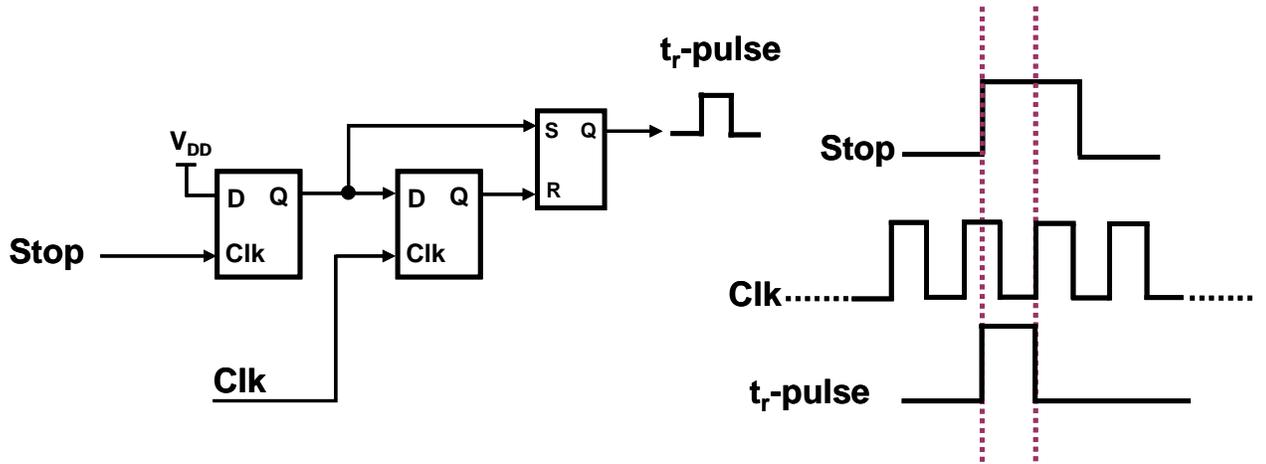
Figure 4.7 : Fine TDC pulse generation

The t_r-*pulse* with the time duration (t_r) can be generated through two flip-flops

and a latch as shown in Figure 4.7. The first flip-flop detects the rising edge of the *stop*

signal and sets the latch output, while the second flip-flop detects the immediate rising

edge of the *clk* and resets the latch.

The fine TDC is implemented with a delay chain of buffers. The delay line

divides the clock period, T_{clk}, into 46 equally sized slices. The outputs of these buffers

are connected to one terminal of gated dynamic NAND gates (see Figure 4.8). The

dynamic NAND gates are pre-charged with the global *reset* signal which is $\overline{start}$. When

the t_r-*pulse* propagates in the buffers, t_r-*pulse* and its delayed version start discharging the

dynamic gates. The dynamic gates are discharged up to the nth position in the delay line

(see Figure 4.8 waveforms). At the nth NAND gate, t_r-*pulse* and its delayed version do

46

not have overlap. Therefore, n is proportional to the duration of the t_r-*pulse*. The buffer delay of this system is tuned with the supply voltage *Vc*.

To relate the fine time and coarse time measurement, the delay line needs to be calibrated and each buffer delay needs to be a fraction of one reference clock period. In the first prototype, 5-bit resolutions were expected from the fine TDC, therefore the clock period must be divided by 32. During the calibration phase, one clock period, T_{clk}, is sent as t_r-*pulse* to the fine TDC, and the supply voltage (V_c) is tuned until a thermometer code of 32, at the output, is visible. Therefore, the average buffer delay is $T_{clk}/32$. A wide-OR dynamic logic gate is used as the thermometer-to-binary encoder as shown in Figure 4.9. The thermometer codes are indicated in the general form of O_n and O_m and they discharge the dynamic nodes D_0, D_1, etc. based on the encoding logic function.
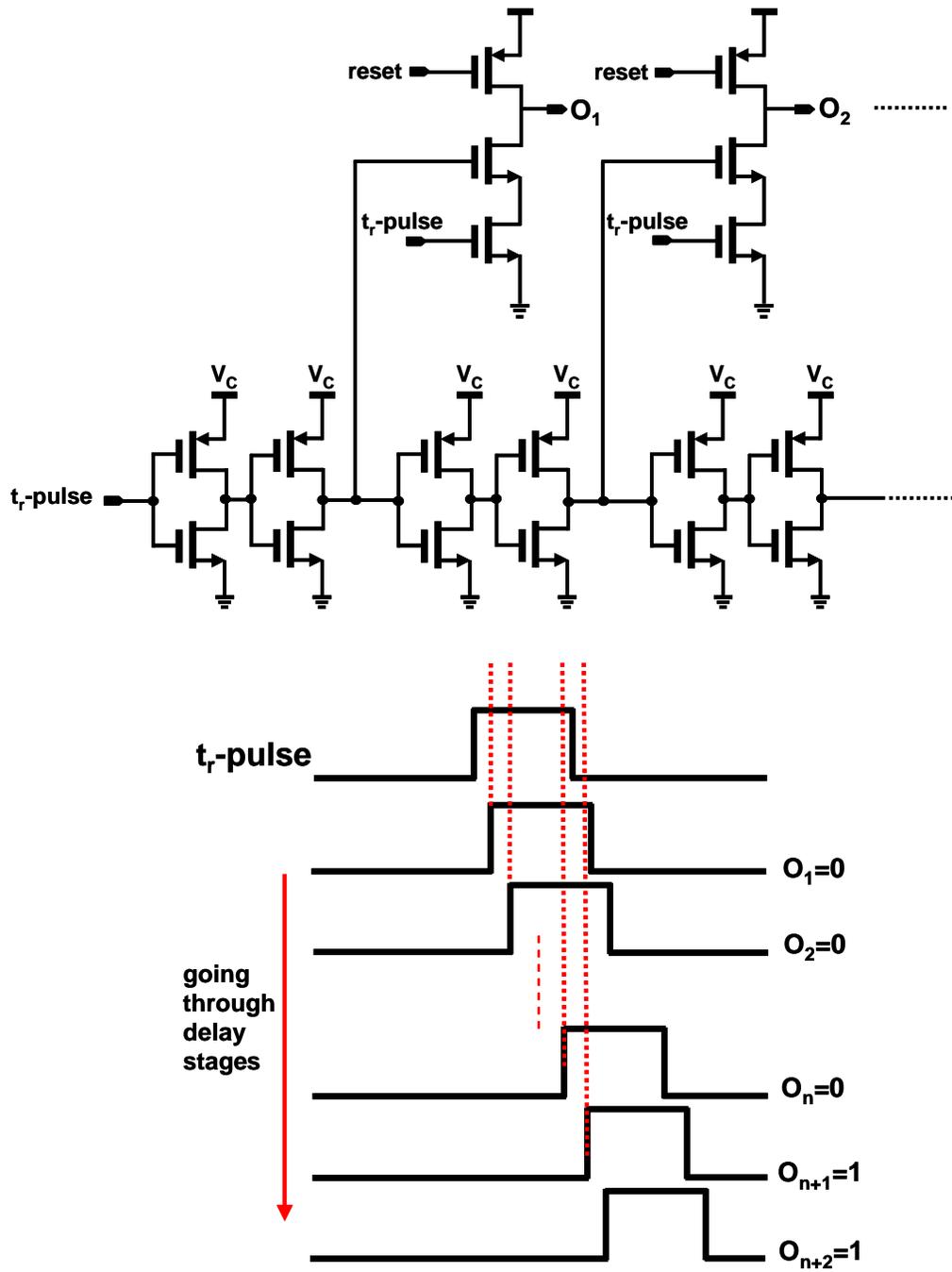
Figure 4.8 : Buffer chain and gated NAND gates for fine TDC
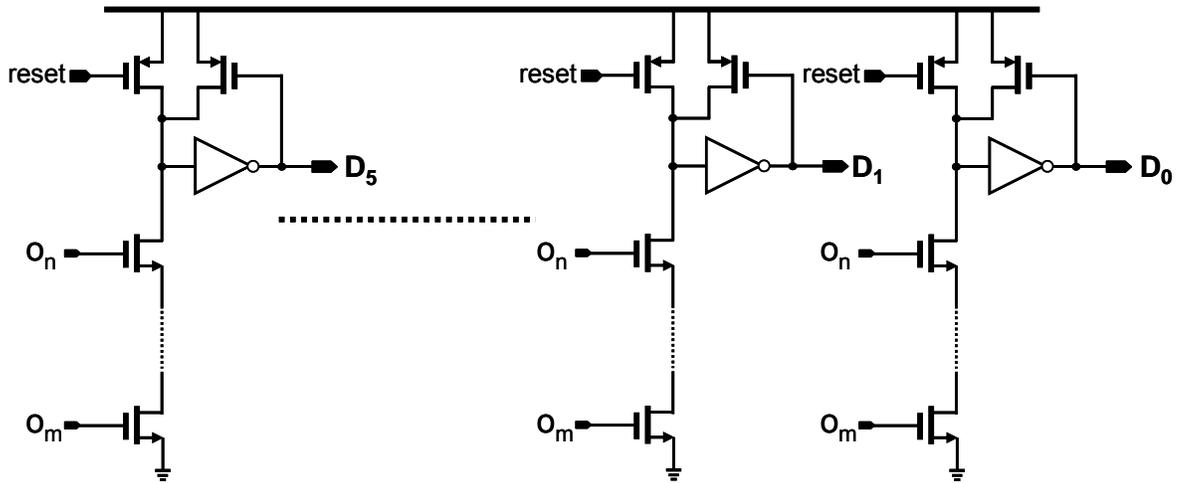
Figure 4.9 : Dynamic encoder

The clock frequency is $f_{clk} = 128MHz$ and accordingly $T_{clk} = 7.8125ns$. The input time range, $[B - A]/s$, to the TDC based on the ramp linearity specification and noise, is $250ns$. The counter is a 5-bit counter and works with the clock frequency of $128MHz$, covering the required 5 bits of time resolution. Since T_{clk} is divided by 32 in the buffer chain, the fine TDC provides 5 bits of additional resolution. Therefore, the overall ADC can resolve the signal to 10 bits, ideally, assuming perfect reconstruction. The resolution is calculated based on (4.1), so that $t_b = 7.8125ns/32 = 244ps$ and therefore, $N = 10$.

The length of the buffer is chosen to include 46 delay stages. There are two reasons why the buffer chain length is greater than 32 delay stages. First, this larger number (overdesign) gives us flexibilty in the chain length to enable possible calibration of the TDC delay to different values of t_b which is defined by ($2T_{clk}/length$). Such a design gives us the option of tunning to experimentally examine the effect of TDC resolution on

the overall performance. Second, additional delay stages are necessary at the tail of the buffer chain to ensure the detection of possible overflows during the ADC calibration.

4.5.3 TDC error correction

A potential error source exists in the fine TDC that we described in the previous subsection. If the immediate rising edge of the *clk*, after the *stop*, does not satisfy the setup time requirements of the second flip-flop in Figure 4.7, the *clk* edge will be missed. Instead, the second rising edge of the clock will be captured and a single clock period error in t_r measurement will appear. Repeating the fine measurement block with a delayed version of *clk* potentially avoids this error. The *clk* is delayed by two to three buffer delays as shown in Figure 4.10 and at the encoder output; the outputs of the two fine measurement blocks are compared. If the two encoder numbers differ within the range of 2-5, the above error does not occur, meaning that the flip-flop set up time is satisfied. However, if the first encoder reports a large number (close to the clock period) and the second encoder shows a small number, a clock missing has definitely occurred and the *stop* signal arrived directly prior to the next rising edge of the *clk*. Using this approach, the error can be caught and fixed in the post processing.
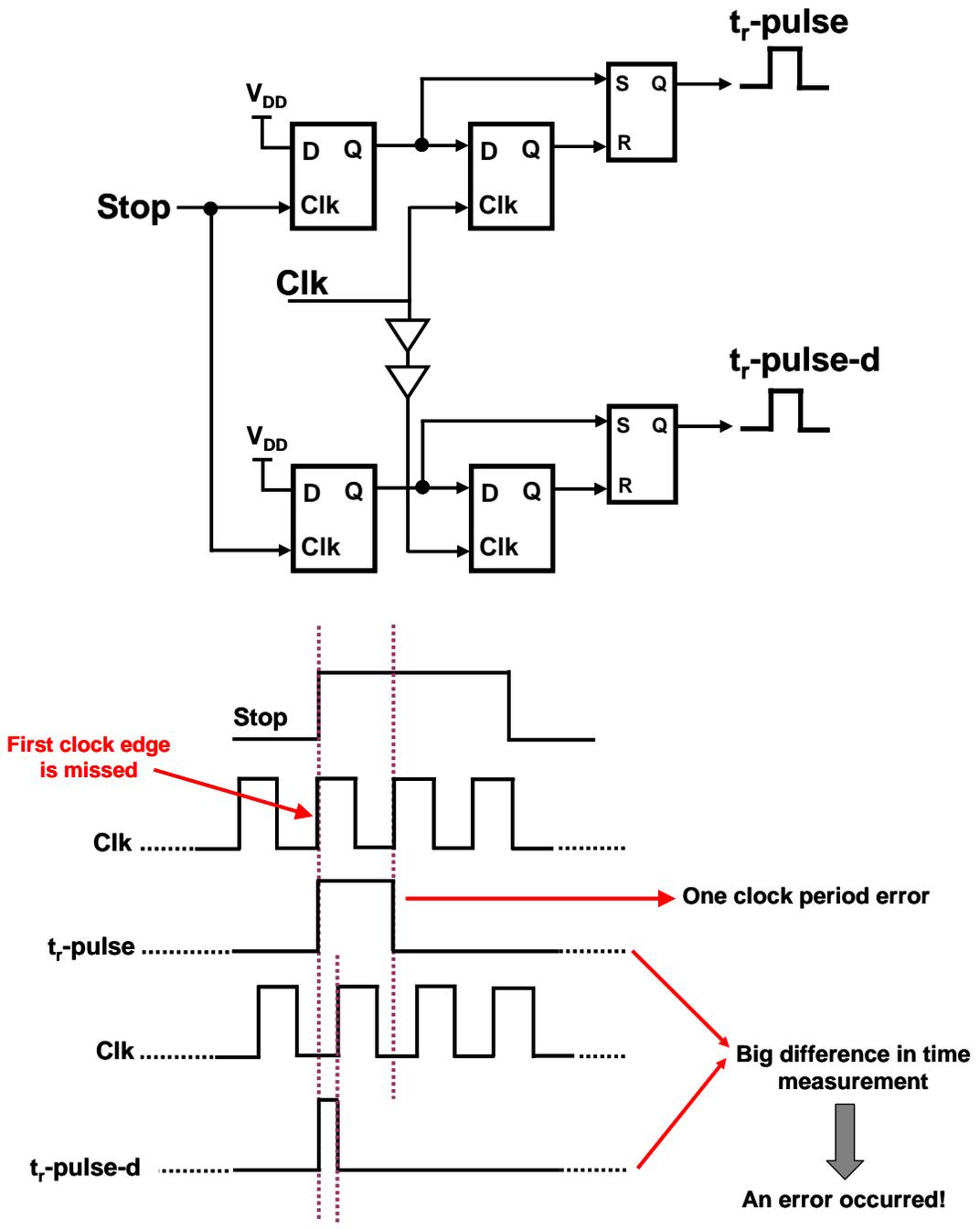
Figure 4.10 : Error correction technique

4.5.4 Chip measurement results

The first prototype was taped-out on ST 90nm digital CMOS in April 2007. The chip was tested in the Fall of 2007. The chip layout is shown in Figure 4.11. The analog circuits (ramp generator and comparator) operate from a 1V supply, while the digital circuits run from a 500mV supply. The total chip power consumption is 25μW at 1MHz sampling frequency.
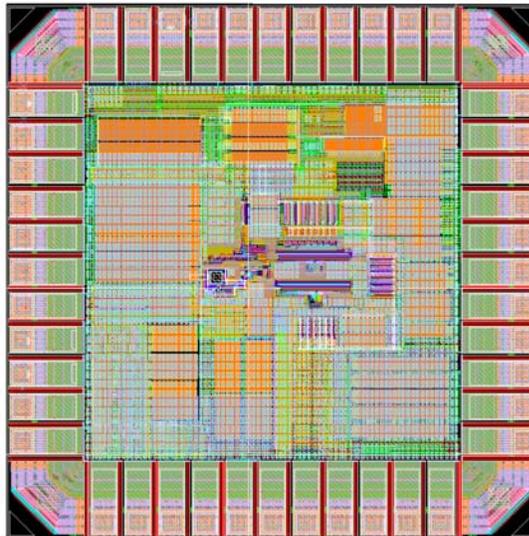
Figure 4.11 : First prototype layout

In the measurement results, wrong codes were randomly observed at the output of the encoder, the number 63 being the most common. Since the encoder is a wide dynamic OR gate, code 63 showed all the OR branches are activated. The possible explanations for this non-ideality are:

- Leakage of the encoder dynamic gate at this low speed $(f_s = 1MHz)$

- Sparkle and bubble codes at the thermometer output

- Leakage at the dynamic NAND gates tapped off the delay line

512 data points were obtained without a flawed code and after digital post processing 7.2 bit ENOB, was measured. The FFT plot for a single input tone at 140 kHz and sampling frequency (f_s) of 1MHz is shown in Figure 4.12.
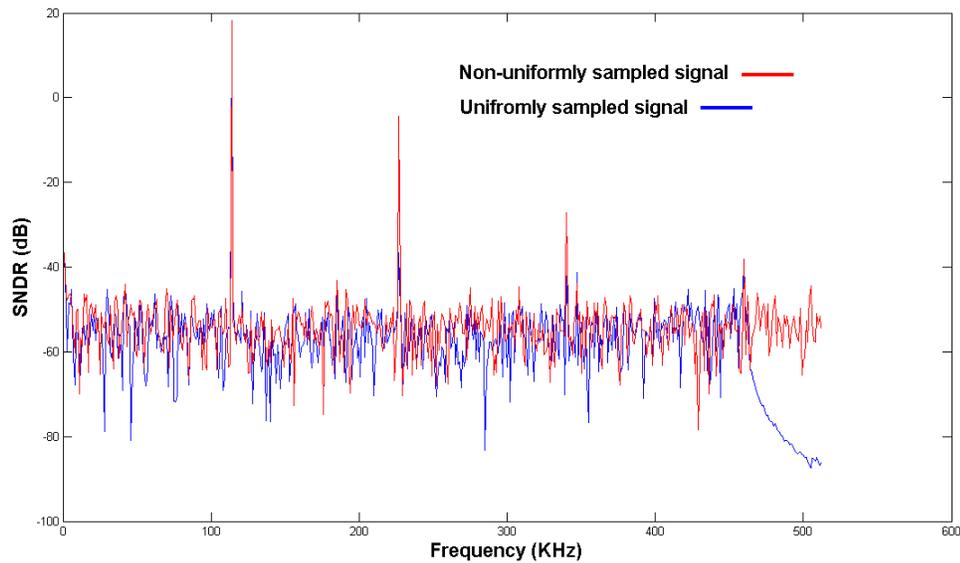
Figure 4.12 : The FFT plot of a single tone at 140 kHz and fs=1MHz

The other observation from the measurements was the high sensitivity of the system to supply voltage variations in the buffer delay chain. This caused difficulty in calibration, unreliability, and sensitivity to the noise in the DC power supplies. The measured drop in the ENOB can come from all the above error sources. In addition to that, there are other sources of error, which were not considered in the design of the first prototype. One is related to stitching coarse time and fine time measurements and this can cause error in the counter measurement. The *enable* signal, which activates the counter is reset with the

53

stop signal and as shown in Figure 4.13, there is a delay, t_d, between the *stop* rising edge and the *enable* falling edge. Since the *stop* signal happens at a random phase with respect to the reference clock, a *clk* rising edge can arrive at any time in the t_d time interval. Hence, the *clk* rising edge may or may not be counted by the counter depending where it happens in this time interval. This uncertainty can cause a substantial error (1 MSB) in the time measurement. In the second prototype, as we discuss in the following subsections, this issue is mitigated by properly stitching the counter measurement to the fine TDC measurement. It is also worth mentioning that since the *t_r-pulse* shrinks by traveling in the delay line TDC, for very small t_r, the pulse fades away. This is another source of error in the time measurement.
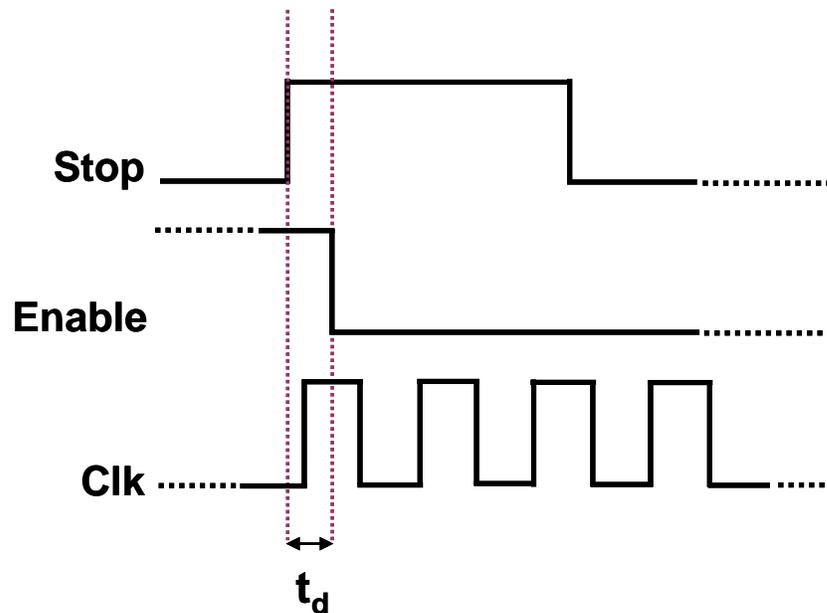
Figure 4.13 : Uncertainty in the counter measurement

4.6 Second design prototype

The design of the second prototype concentrated on new techniques to address the drawbacks of the first prototype.

4.6.1 Two-step TDC

First of all, this design does not utilize dynamic logic and the structure of the fine TDC is significantly changed compared to the previous design discussed in Section 4.5.2. A two-step TDC is still used; however, here a pulse equivalent to t_r or the counter residual error is not generated and instead, the time between the edges is measured. One cycle of the ramp is shown in Figure 4.14.
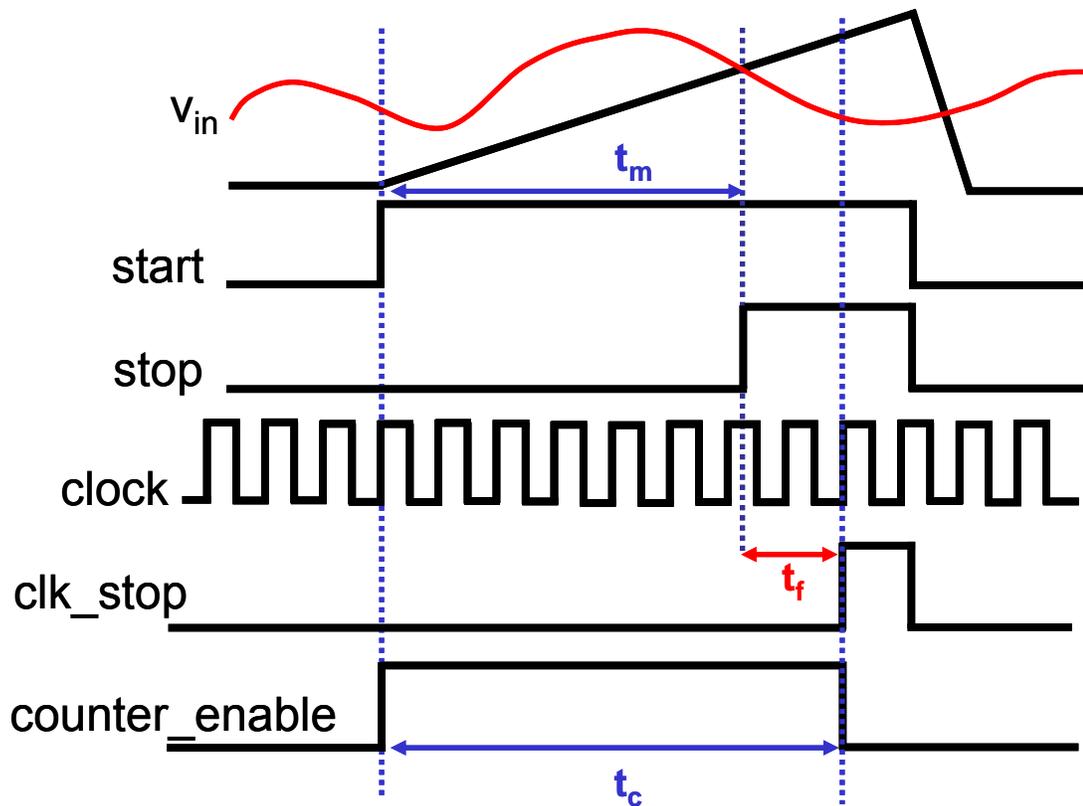
Figure 4.14 : Second prototype waveforms

In this TDC, the *start* and *stop* signals are utilized in the same way as in the first prototype, while two additional signals are generated on-chip to enhance the performance of the system, i.e., *clk_stop* and *counter_enable*. The signal *clk_stop* is set by the arrival of the second next rising edge of the *clock* after the *stop* signal. The second *clock* rising edge is selected due to metastability issues, which will be addressed later. The *counter_enable* signal is set by the *start* and reset by the *clk_stop*. A coarse time quantizer, formed using a counter, measures the number of reference clock cycles, while the *counter_enable* signal is high. The fine TDC measures the time t_f, defined as the time between the *stop* signal and *clk_stop*. The overall TDC output is $t_m = t_c - t_f$.

The overall PPM ADC block diagram with the described TDC is depicted in Figure 4.15. The two signals *counter_enable* and *clk_stop* are generated by the synchronizer block.
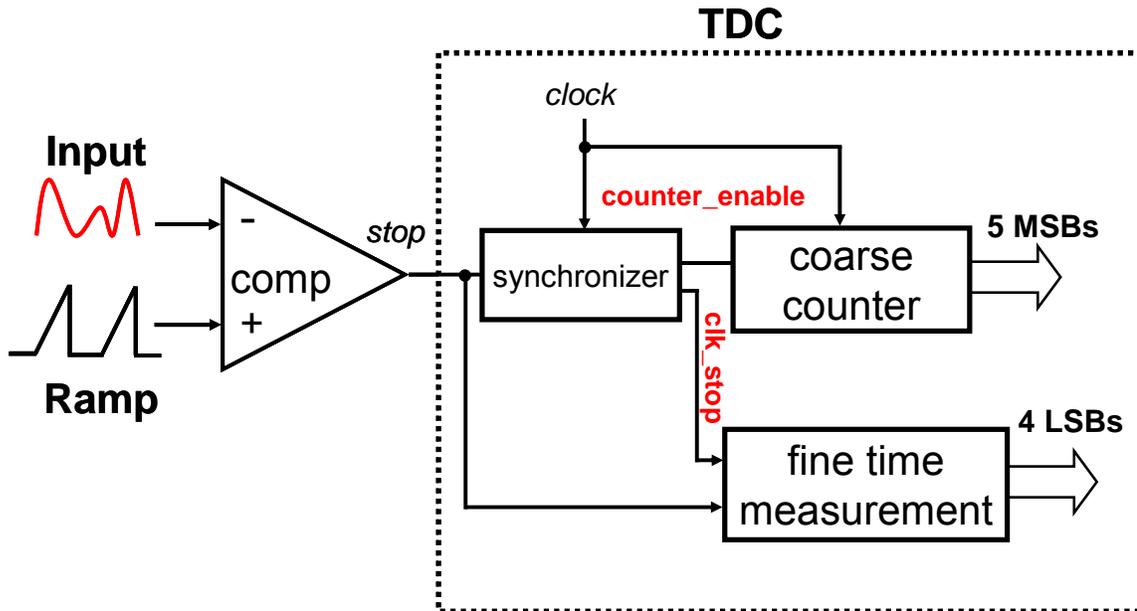
Figure 4.15 : PPM ADC block diagram

The synchronizer generates *counter_enable* and *clk_stop*. It is shown in Figure 4.16 and consists of three flip-flops in series. The first flip-flop detects the arrival of the *stop* signal while the second flip-flop catches the next rising edge of the *clock* right after the *stop* signal. The second next rising edge of *clock* after the *stop* signal is detected by the third flip-flop. The *stop* signal is an asynchronous signal, which arrives at an arbitrary time with respect to the reference clock. Consequently, it can lie within the metastability window of the second flip-flop. Waiting for another clock cycle in the third flip-flop reduces the chance of metastability significantly. This is a tradeoff between latency and accuracy, and at the expense of adding one clock period as an offset to the fine TDC block. The synchronizer also generates a *counter_enable* signal, which is synchronously set by *start* and asynchronously reset by *clk_stop*.
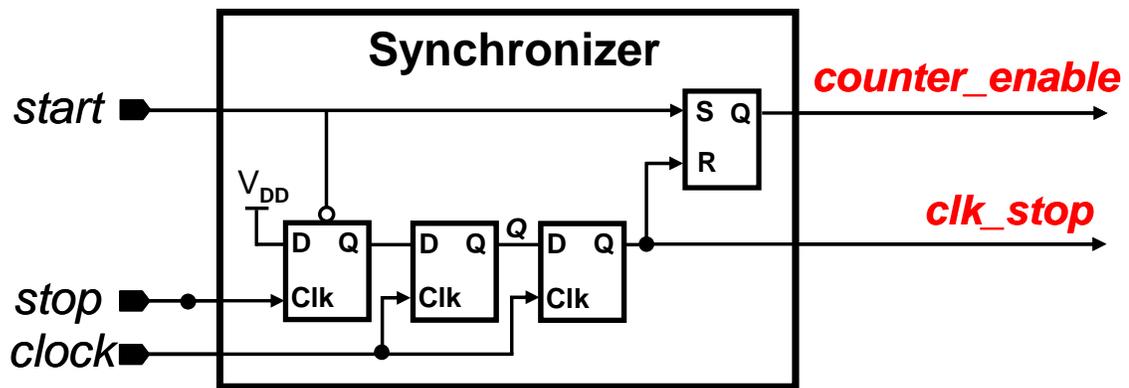
Figure 4.16 : Synchronizer block

Since the *counter_enable* is reset by the *clk_stop* signal, the coarse time measurement made by the counter is correctly stitched to the fine time measurement. In this way, the error demonstrated in Figure 4.13 will never occur. The stitching concept is illustrated

graphically in the waveforms of Figure 4.17 (a) and (b). One possible scenario is illustrated in 4.17(a) in which *stop* signal happens right before the *clock* rising edge. The second flip-flop output (*Q*) in the synchronizer block goes high with the next rising edge of *clock* after the *stop*. Therefore, the fine TDC measures one T_{clk}, which is essentially the TDC offset. In the second scenario as shown in 4.17(b), the *stop* signal happens right before the *clock* rising edge but due to metastability the output *Q* is set with the second next rising edge of *clock* and thus, the third next rising edge of the *clock* is sampled as *clk_stop*. The fine TDC measures $2T_{clk}$ and one T_{clk} error is expected in its measurement; however since *counter_enable* is reset by *clk_stop*, the counter has already counted an extra clock period and the error is canceled out. Based on this, the *counter_enable* is always reset after a certain delay with respect to *clk_stop*, denoted by t_{delay} in Figure 4.17. It is important to guarantee that t_{delay} provides enough time for the counter to count the clock edge prior to the *clk_stop* within all the PVT variations. By doing this, no uncertainty in the counter measurement and no MSB error in the TDC results are assured.

The *start* signal in this system is generated using the reference clock signal. The reference clock in our system is 128 MHz, and this is divided by 128 to generate the 1MHz *start* signal. As is shown in Figure 4.18, there is a delay between the *start* signal and the first reference clock rising edge after that. This delay is denoted as t_{d1} in Figure 4.18. There is also a delay between the *start* rising edge and the *counter_enable* rising edge, t_{d2} in Figure 4.18. In our design, ensuring that the duration $(t_{d1} - t_{d2})$ provides sufficient setup time for the counter to count the next *clock* edge after the *start* signal over all PVT variations is required. Giving enough margin to $(t_{d1} - t_{d2})$ guarantees that clock jitter does not introduce additional measurement uncertainty.

58
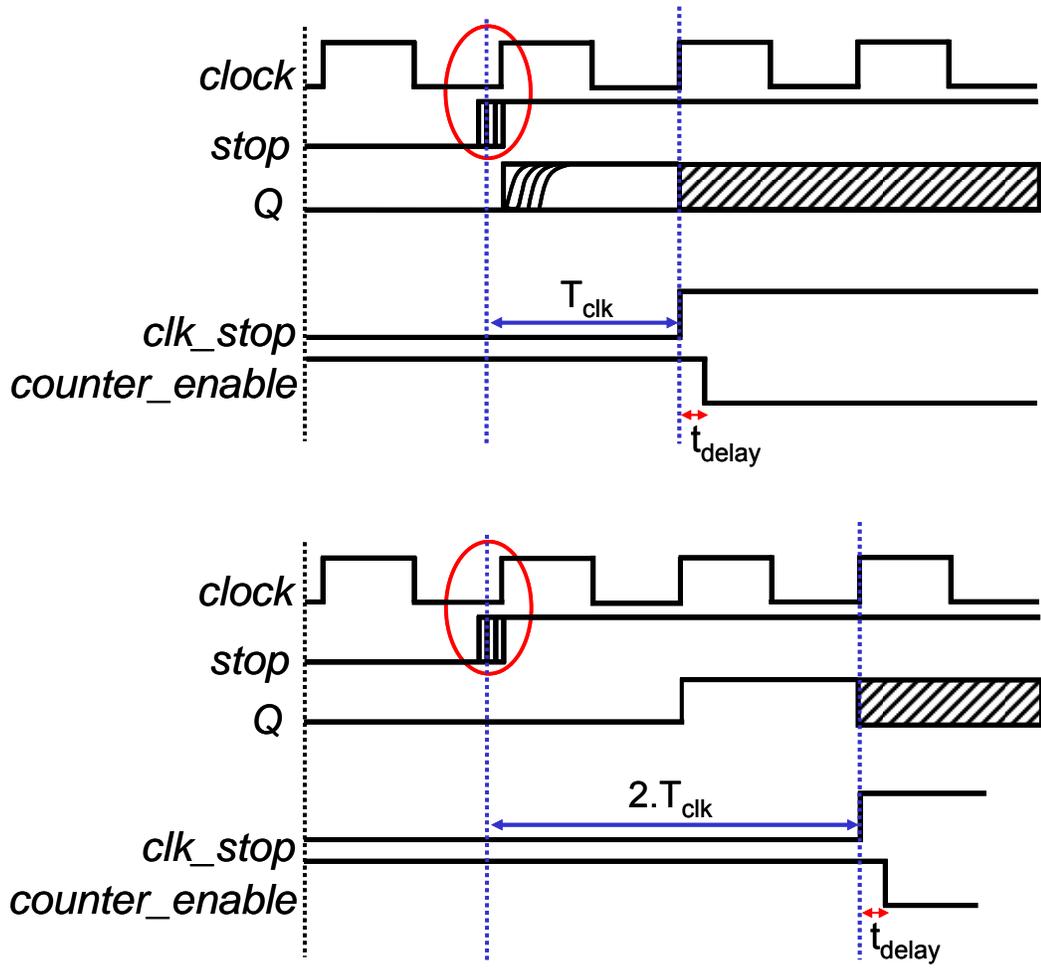
Figure 4.17 : Coarse and fine TDC stitching
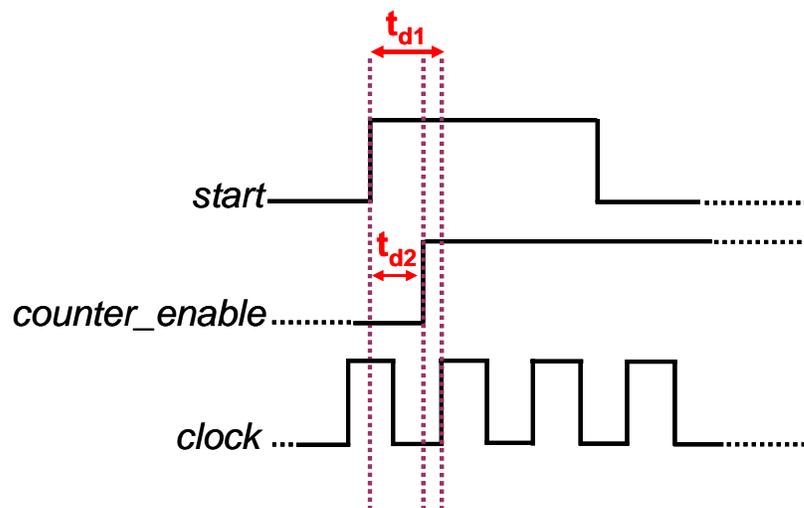
Figure 4.18 : Counter setup time

A fine sub-TDC measures the interval, t_f, from the *stop* rising edge to the *clk_stop* edge. A 32 element delay line shown in Figure 4.19 is tuned to generate the required 32 delay steps, covering two full periods of the reference clock. Two periods of delay are required since the synchronous *clk_stop* signal is the second next reference clock edge after the comparator *stop* signal. The asynchronous comparator output signal, i.e., *stop*, is the input to the delay line. The 32 flip-flops are all clocked by the *clk_stop* signal and sample delayed versions of the *stop* signal. Running the interpolating-delay-line off the *stop* edge, and not off the reference clock, saves power since the delay cells are only activated when there is a comparator transition. The outputs of these flip-flops form a thermometer code with a certain number of 1's indicating the distance in time from *stop* to *clk_stop*. As the 32 delay cells cover 2 reference clock periods, the fine TDC resolves 4 LSBs. The input TDC time dynamic range is 250ns and f_{clk}=128 MHz. The counter is a 5-bit counter operating at 128MHz, covering 5 bits of time resolution. Therefore, the two-step TDC can ideally resolve 9 bits. The complete TDC architecture is sketched in Figure 4.20.
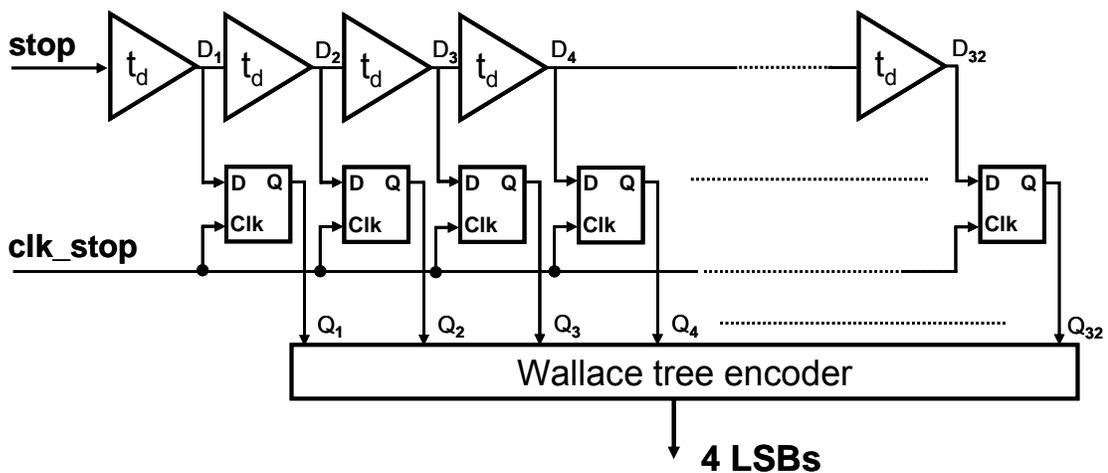
Figure 4.19 : Delay line TDC
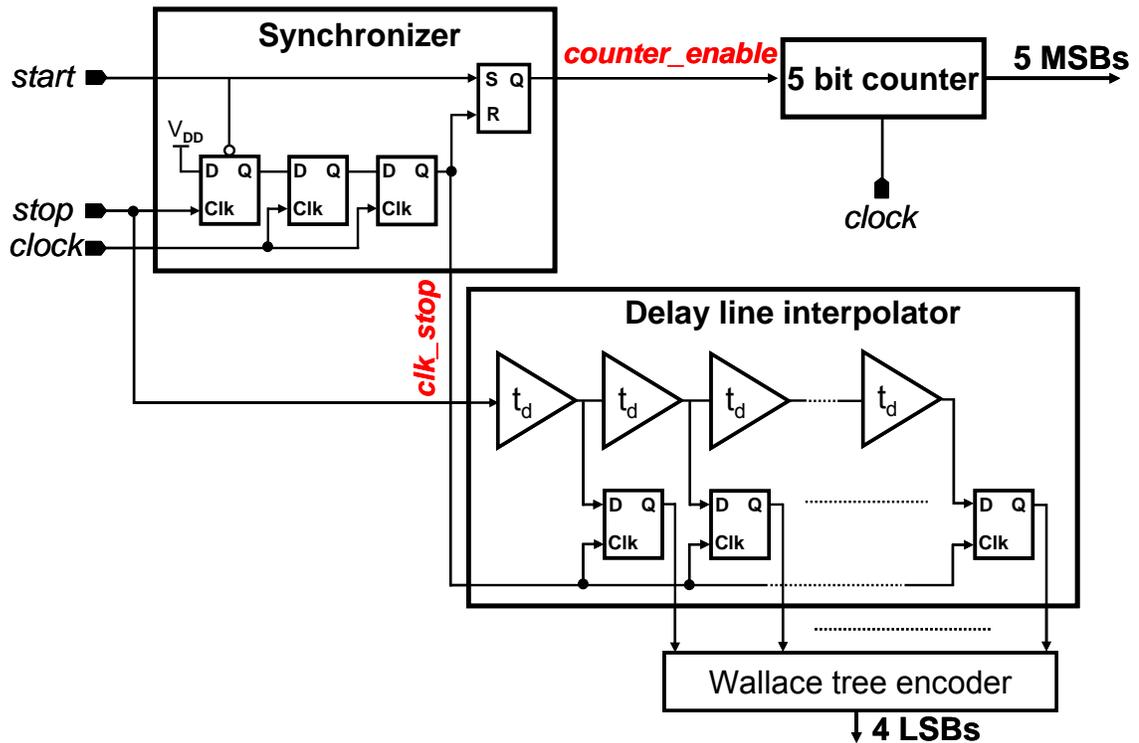
Figure 4.20 : Complete TDC architecture

4.6.2 Counter and delay line TDC resolution

In our design, the overall digital power consumption (approximately 50% of the power for the whole system) is dominated by the dynamic power consumption of the digital counter as well as the signal routing buffers. There is a fundamental tradeoff between this dynamic power and the ADC INL in our two-step TDC design. We can achieve more linearity by shortening the delay line and increasing the resolution of the counter. However, to do this, the counter should resolve more bits and hence consumes

more power. On the other hand, if we assign more resolution to the delay line, which makes it longer and more nonlinear we reduce the power consumption of the counter.

The reference clock in the system is divided by a binary number to generate the required clock for the ramp (1MHz in our system). The clock frequency also defines the counter time resolution. The input time range of the TDC is 250 ns, therefore the counter resolution is $\log_2(250ns/T_{clk})$. Therefore, the delay line TDC requires a resolution of $n = 9 - \log_2(250ns/T_{clk})$ for a 9 bit ADC. In this case, the length of the delay line TDC is 2^n. Based on 2.1, the INL in the line is proportional to $\sqrt{2^n}$. The maximum INL and the counter power are sketched in Figure 4.21. As shown, in order to limit the INL in our TDC to 0.5 LSB, and optimize the power, we choose a 5 bit resolution for the counter and 4 bit for the delay line TDC.
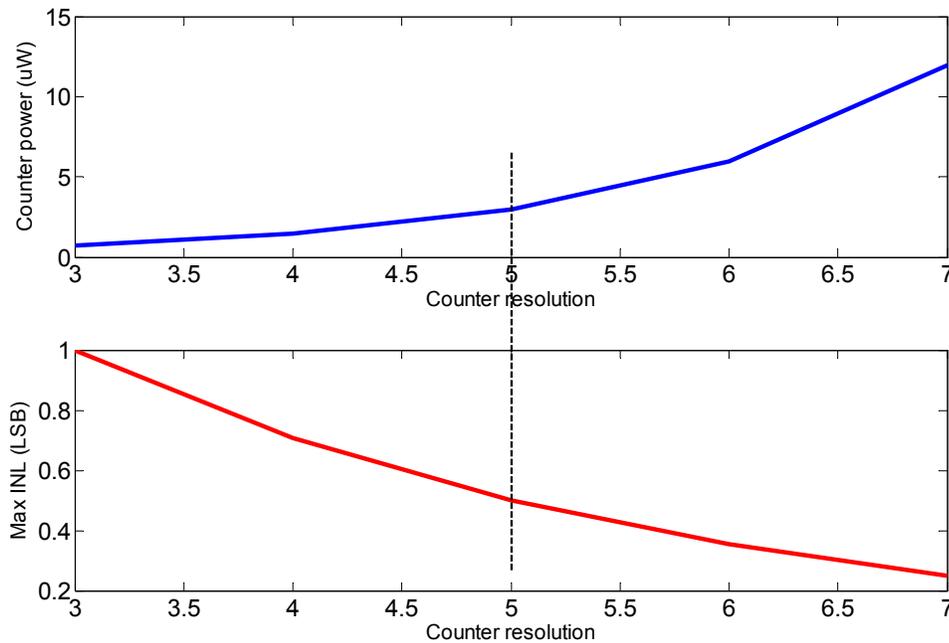
Figure 4.21 : Trade-off between counter power and delay line resolution

Sense amplifier-based flip-flops, shown in Figure 4.22, are used in the TDC. The rationale behind this is that they can be designed to have a very narrow metastability window. In this design, two design criteria, regarding these flip-flops, were considered. First, the input transistors (M1 and M2) are oversized to reduce the mismatch. Second, the metastability window of the sense-amplifier flip-flops is designed to be less than 2% of the delay line resolution, across PVT. Although the chance of metastability is reduced, it can still occur, causing large errors in the output thermometer code. This is similar to metastability in flash ADCs. A Wallace tree encoder [51] is used to encode the thermometer code and to suppress potential bubble and sparkle codes.
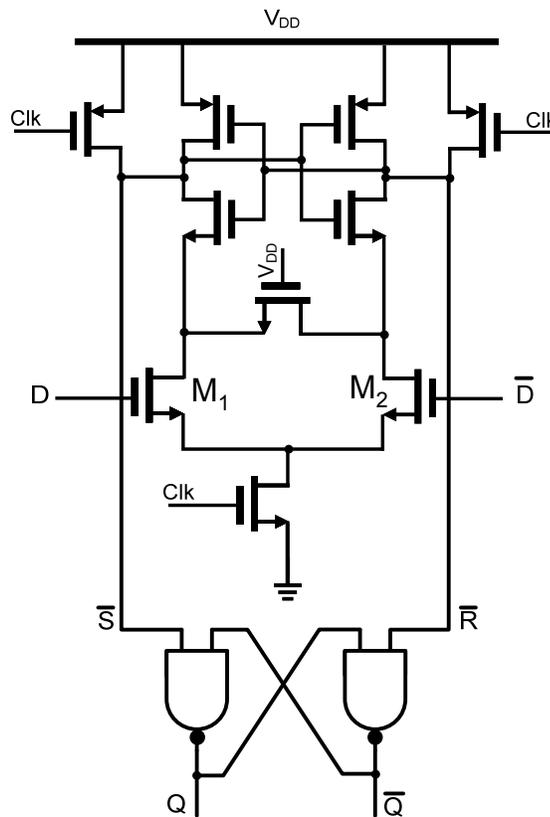
Figure 4.22 : Sense amplifier flip-flop

The delay line in this design is composed of 32 current-starved buffers where the gate voltage of the bottom devices is controlled by tuning voltage (V_c) (see Figure 4.23). The PMOS and NMOS transistors in the buffer stages are oversized to avoid mismatch. Based on Monte Carlo analysis, the maximum delay variation in buffers is 2% of the TDC LSB, due to mismatch. The delay buffers are calibrated during a calibration cycle in which a half clock rate is applied to the interpolator and the V_c is tuned to activate all 32-sampler flip-flop outputs. Realizing the delay versus V_c covers the full PVT range was ensured in the buffer design. Additional delay stages are added at the tail of the 32 buffer chain to detect possible buffer overflow errors.
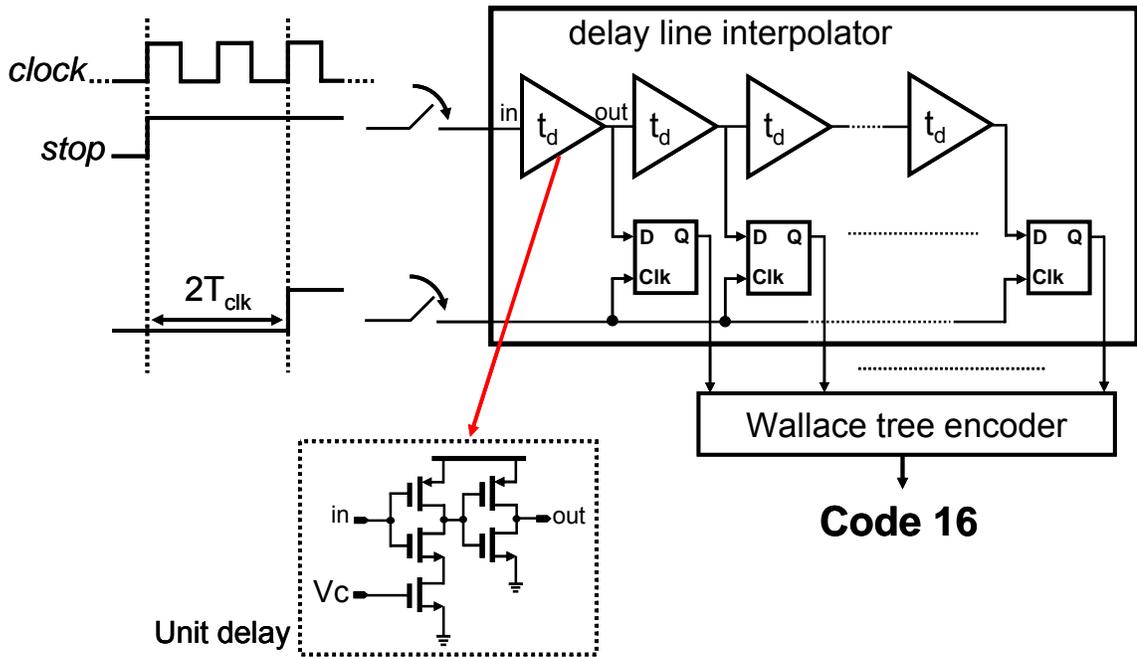
Figure 4.23 : Delay Line TDC calibration

The calibration cycle in this prototype is carried under off-chip control. Nevertheless, it is possible to make calibration automated and on-chip as shown in the diagram of Figure 4.24. The Wallace tree encoder output is compared with code 32 and controls an up/down counter, which subsequently controls a DAC. The counter increases the DAC output if the encoder output is less than code 32 and vice versa. This means that V_c needs to be boosted to reduce the buffer delay until 32 buffers exactly cover two clock periods. This automated calibration can be accomplished on-chip during ADC idle times, or it can continuously calibrate a replica of the delay line. A more precise calibration method uses a charge pump as in a DLL, as mentioned in chapter 2. However, this approach can be very power hungry for a single channel ADC but a good candidate for multichannel ADCs, as will be described in Chapter 5.
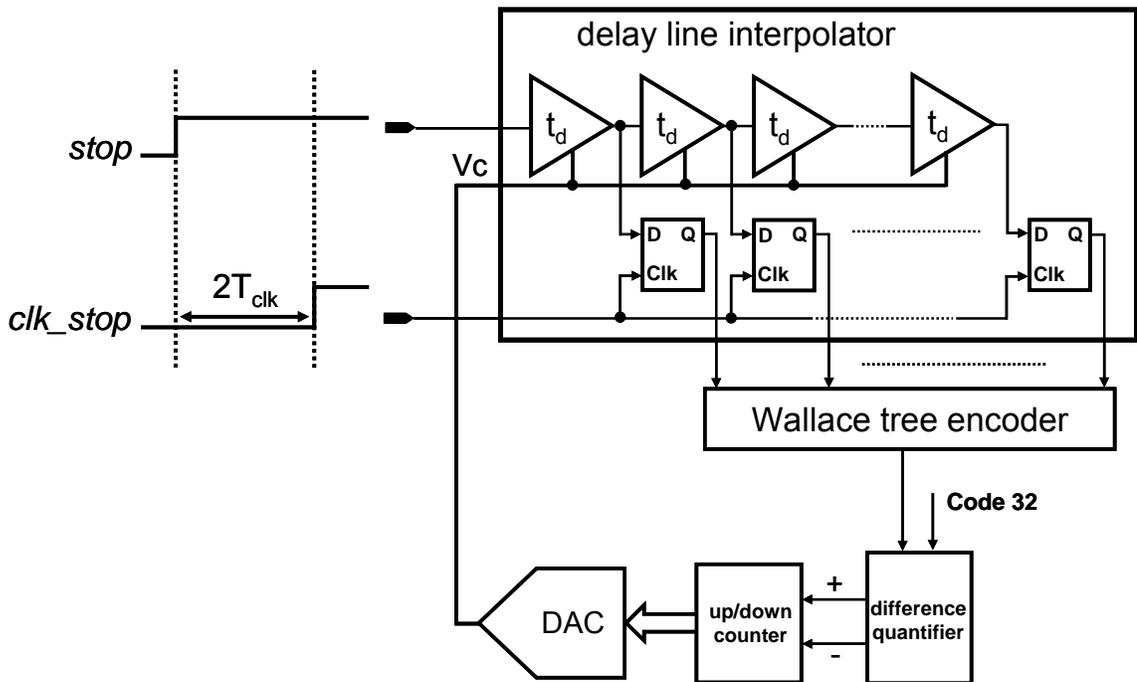
Figure 4.24 : Automation of delay line TDC calibration

4.6.3 Comparator and ramp generator

The ramp generator is shown in Figure 4.25 and is similar to the design in the first prototype. Some modifications were performed to reduce noise. Decoupling capacitors C_1 and C_2 are added to filter out the noise coming from bias transistors. Due to the low frequency operation of this ADC, flicker noise (1/f noise) is the dominant source of noise in the ramp generator circuit. Switching transistors M_1 and M_2 contribute little to the flicker noise [52]. The noise contribution of cascode transistor M_3 is negligible compared with that of M_4 and M_5. In our design, M_4 and M_5 are oversized and biased with low g_m. To achieve an almost 11 bit linear ramp with large dynamic range, transistors M_3 and M_4 must be biased with small VDS_{sat} to allow more headroom in the ramp output swing. This necessitates high g_m in M_4 and therefore increases its current noise and indicates a tradeoff between ramp voltage linearity and output noise.
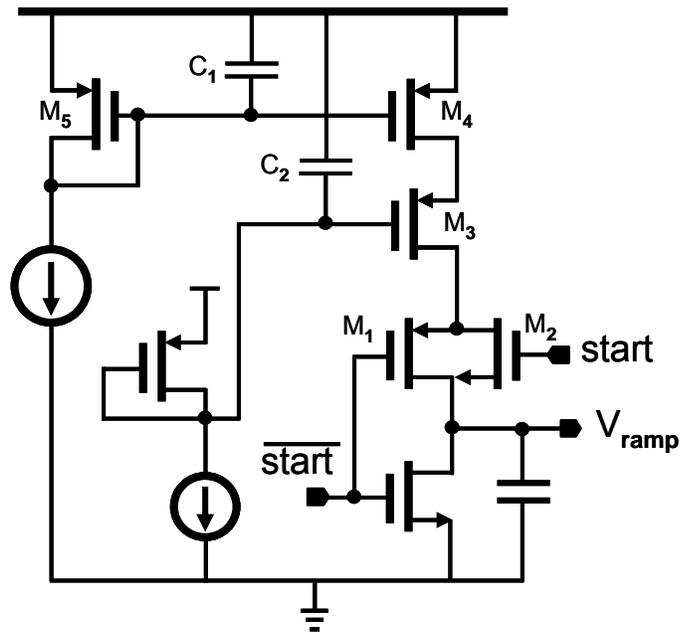
Figure 4.25 : Ramp generator circuit

The continuous time comparator shown in Figure 4.26 consists of a PMOS input differential amplifier followed by a common source stage. This architecture consumes less power than the one used in the first design prototype. The input transistors, M_1 and M_2, operate in the subthreshold region. In addition to saving power, this allows a larger input common mode range and therefore larger ramp dynamic range. Transistor M_2 and M_4 sizes were chosen such that the output impedance of the differential stage is dominated by M_4, which is relatively small. By this proper sizing, a wider bandwidth is achieved, and in addition, the bandwidth is not affected by the output resistance of M_2, which varies with the input common mode level. The propagation delay variation (shown in Figure 4.4(b)) in this design is kept at less than one LSB of time measurement.
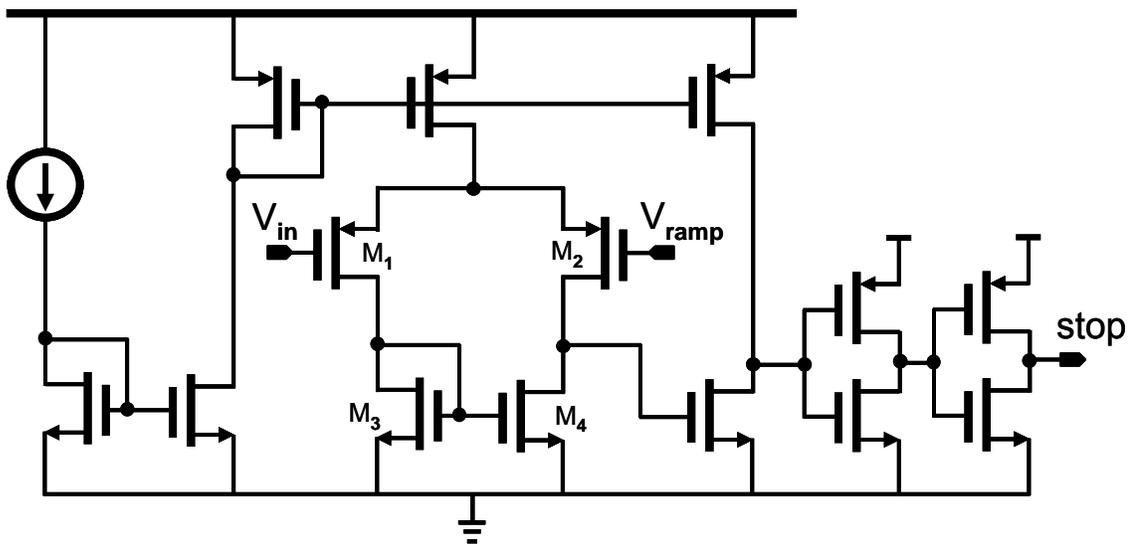
Figure 4.26 : Continuous time comparator circuit

4.6.4 Chip measurement results [53]

The prototype PPM ADC was implemented in ST 90nm digital CMOS and occupies an active area of $0.06mm^2$, and a total area of $1mm^2$ including pads. The layout of the prototype is shown in Figure 4.27. It is worth noting that even though many of the analog components have been removed, the area is still dominated by the area of the remaining analog blocks. The analog circuits operate with a 1V supply, while the digital blocks operate at near-threshold using a 400mV supply.

The TDC resolution is targeted for 9 bits, which is obtained with a 5-bit counter and 4-bit delay line TDC. The ramp frequency, which is the sampling frequency (f_s) in this ADC, is 1MHz. The input signal bandwidth is 300 kHz and therefore, the oversampling ratio is 1.7. The measured ENOB is 7.9 bits over the entire bandwidth. The measured power consumption of the entire system is 14µW (excluding digital post processing). The analog and digital blocks each consume 7 µW. The figure of merit $\left(\dfrac{power}{2 \times BW \times 2^{ENOB}} \right)$ is 98fJ per conversion-step.

Figure 4.27 : Chip die micrograph

The measured spectrum for a 40.25 kHz tone sampled at fs=1MHz is shown in Figure 4.28 (a). The FFT of the raw non-uniform data shows large harmonics due to non-uniform sampling. The spectrum of the same signal after the iterative algorithm is shown in Figure 4.28 (b), which illustrates how the artifacts are suppressed and the SNDR and SFDR are improved by creating uniform samples in post processing. The same plots are repeated in Figure 4.29 for a signal at 290.25 kHz closer to the end of the bandwidth. Measured DNL, INL, and SNDR versus f_{in} are illustrated in Figure 4.30. The maximum DNL is 1.2 LSB and the maximum INL is measured as 1.5 LSB. In another test, two tones at 100.25 kHz and 20.25 kHz are applied to the ADC to observe the effect of possible inter-modulation distortions. The results are shown in the plots of Figure 4.31. The top plot (a) is the raw data before the post processing. As evidenced in (b), the extra harmonics are suppressed and the inter-modulated products are below the noise floor.
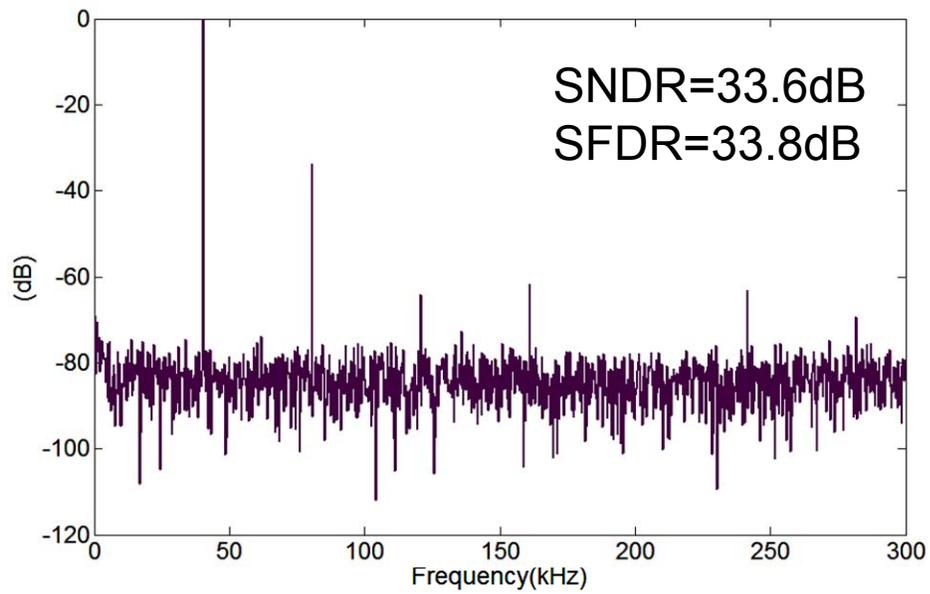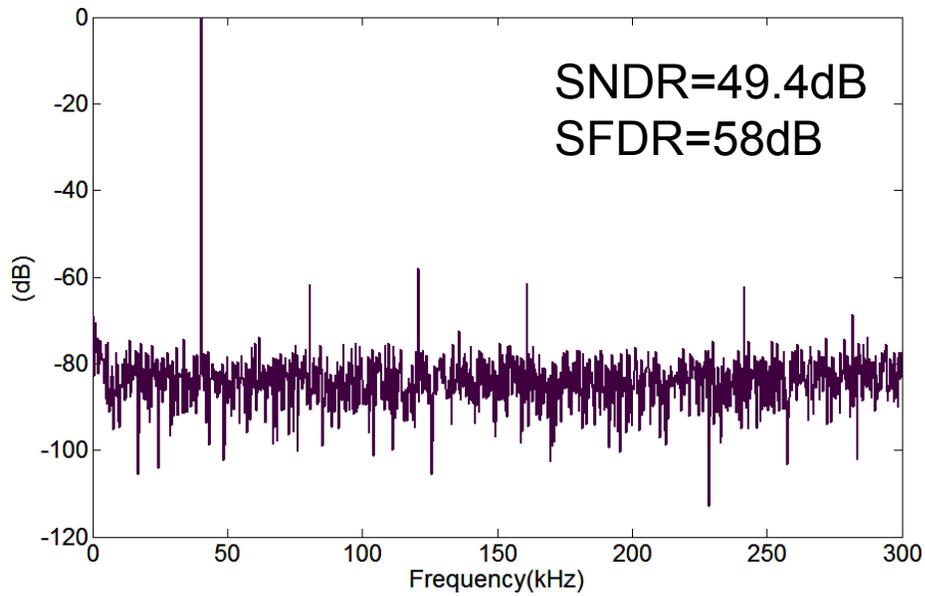
Figure 4.28 : Measured spectrum of a single tone at 40.25 kHz before post processing (a) and after post processing (b)
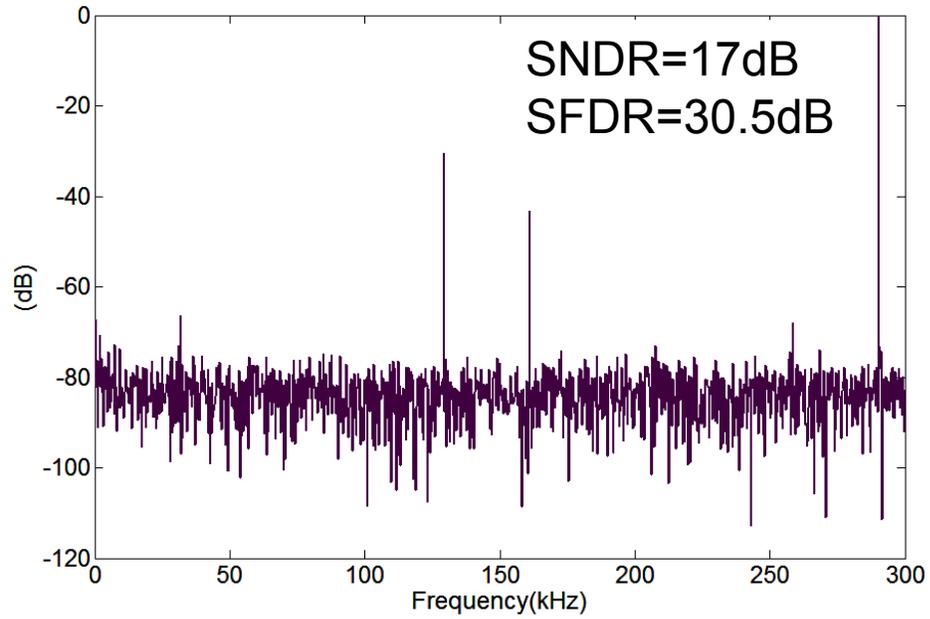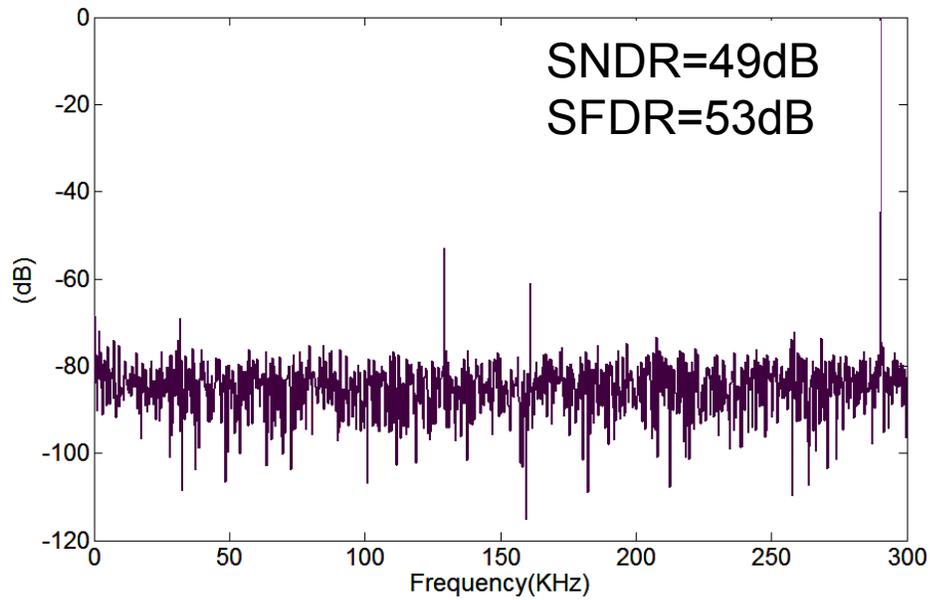
Figure 4.29 : Measured spectrum of a single tone at 290.25 kHz before post processing (a)and after post processing (b)
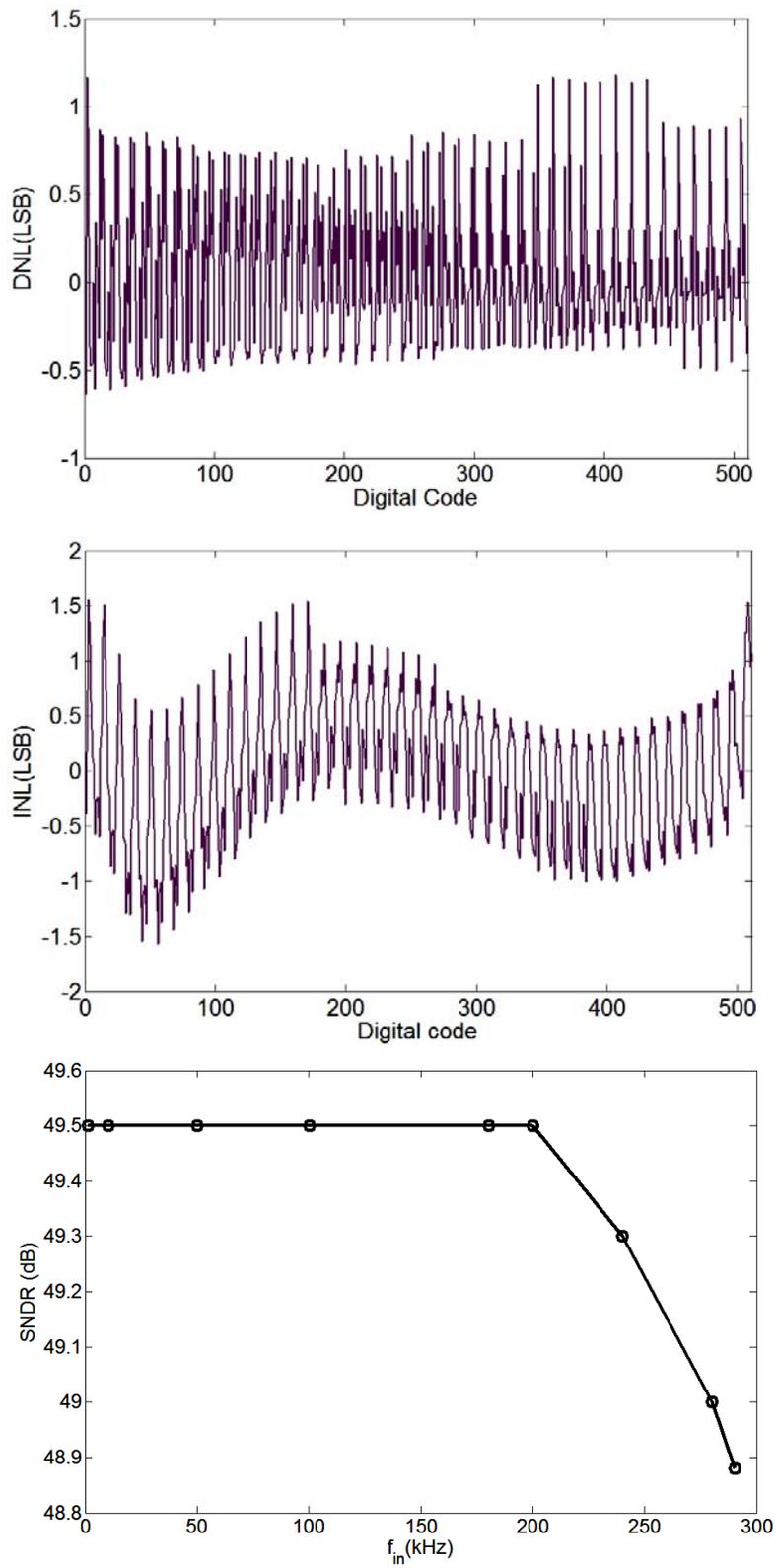
Figure 4.30 : Measured DNL, INL, and SNDR versus f_{in} at fs=1MHz
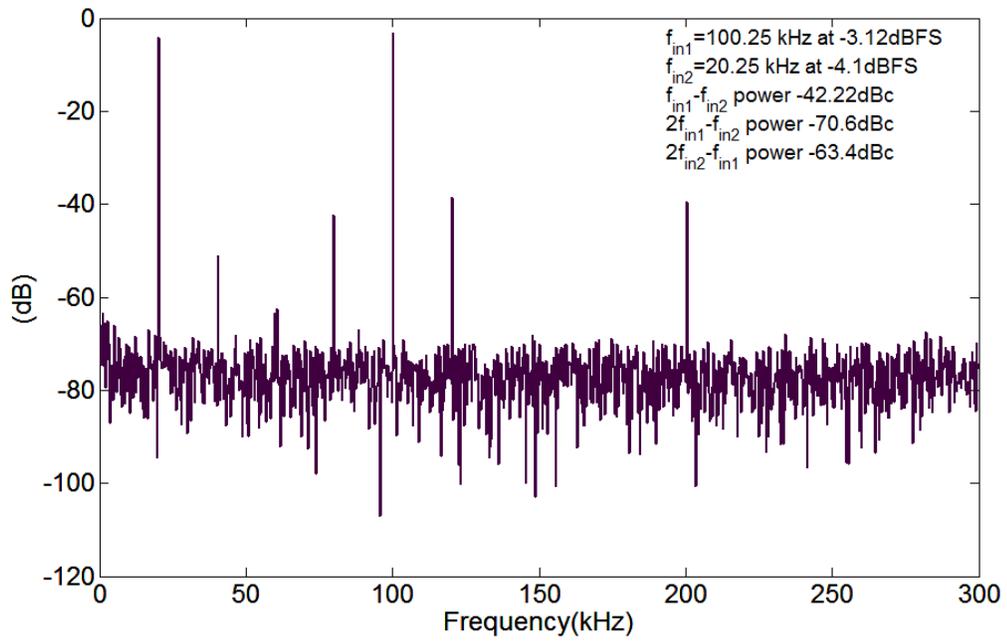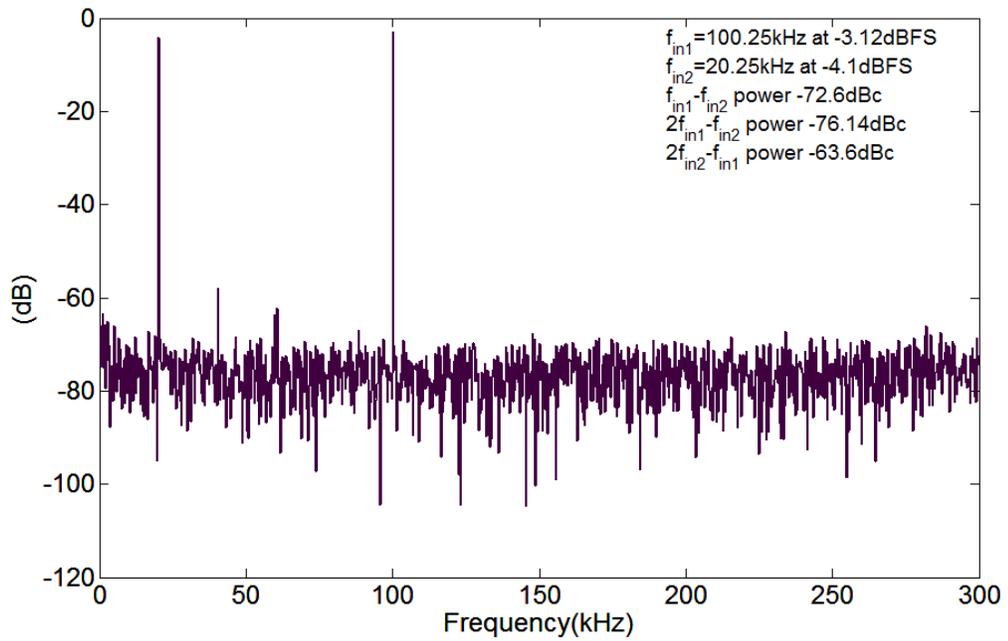
Figure 4.31 : Measured spectrum of two input tones (100.25/20.25 kHz) before post processing (a), after post processing (b)

A summary of the measured chip performance is given in table 4.1. The measurements exhibit 1 bit drop in the ENOB compared to ideal. Based on circuit simulation and prototype measurements, we believe that the distortion observed in the INL can originate from different sources. The major source of nonlinearity in this system is the nonlinearity of ramp slope in the voltage-to-time converter. The parasitic capacitances at the output of this block (see Fig. 4.25) are voltage-dependant and thus change the ramp slope as the output capacitor charges. Since most of the designed digital circuits, including the delay line TDC, work close to the subthreshold region of operation, they are very sensitive to the supply voltage level. Any supply noise (and fluctuation) in the system could become also a major source of error. A differential delay line TDC seems to be a more promising approach for future designs.

Sampling frequency	1 MHz
Input bandwidth	300 kHz
ENOB	7.9
DNL (max)	1.2 LSB
INL(max)	1.5 LSB
Digital voltage supply	400mV
Analog voltage supply	1 V
Digital power	7 μW
Analog power	7 μW
Area	0.06 mm2

Table 4.1: Chip performance summar

4.7 Impact of technology scaling on PPM ADC

In this section, we analyze the impact of technology scaling on the noise and total power consumption of the PPM ADC. For simplicity and without losing the generality of this approach, we assume that we use the same circuit blocks and architectures as we implement the system in more advanced technology nodes. In addition, we assume a scaling factor of α (where $\alpha < 1$) for the channel length, vertical and lateral dimentions and also for the supply voltage [13]. The original and "un-scaled" parameters associated with the original design in this section are I, V, C, g_m, and P, while I_s, V_s, C_s, g_{ms}, and P_s are design parameters after scaling with scaling factor α.

The analog blocks (i.e., ramp generator and comparator) and the digital blocks (i.e., counter, delay line and signal routing buffers), each contribute 50% to the total power consumption of the original design. The digital power consumption (mostly dynamic) is reduced by factor α^2 after scaling (without considering the leakage) [13]. Although it is straightforward to predict the power consumption of scaled digital blocks, it is more complicated to accurately estimate the power and characteristics of the scaled analog blocks. In order to consider the impact of scaling on the analog blocks of our ADC architecture, we need to examine the output voltage noise of the ramp generator as well as the input-referred noise of the comparator.

Since the supply voltage is reduced by α, the input signal dynamic range (see Figure 4.32) is scaled by α. Therefore, for the same ADC resolution, the voltage *LSB* is also reduced by α. As evident in Figure 4.32, the comparator input-refered voltage noise,

v_{cn} and the ramp generator output voltage noise, v_{rn}, collectively, degrade the precision of the comparision.
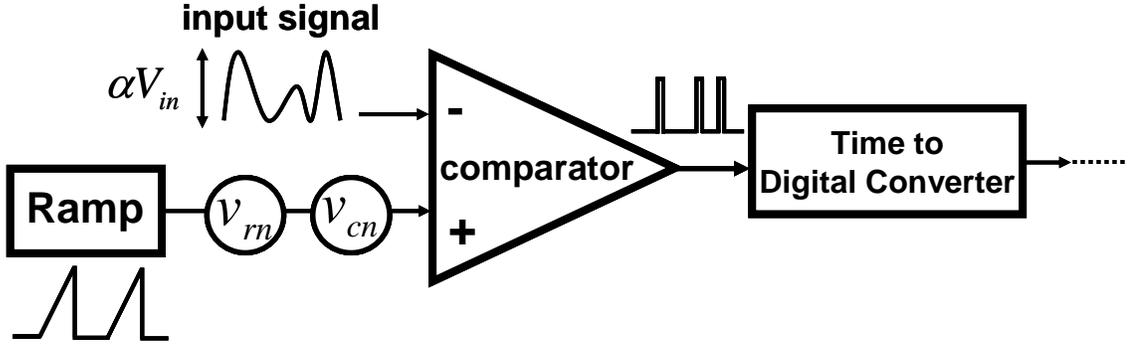
Figure 4.32 : Impact of scaling on voltage to time conversion

The total noise conributed by two independent noise sources v_{cn} and v_{rn} must be smaller than the voltage *LSB* such that their variances σ_{vcn}^2 and σ_{vrn}^2 respectively, should be smaller than LSB^2 or

$$\sigma_{vrn}^2 + \sigma_{vcn}^2 \leq LSB^2 .$$ [4.8]

Now, we assume that v_{cn} is dominated by the input PMOS transistors (M_1 and M_2) of Figure 4.26. Accordingly, σ_{vcn}^2 can be approximated by

$$\sigma_{vcn}^2 = \frac{4kT\gamma}{g_m} .$$ [4.9]

On the other hand, σ_{vrn}^2 can be described as a function in time,

$$\sigma_{vrn}^2(t) = \frac{kT}{C} + \frac{2kT\gamma \cdot g_m}{C^2} \cdot t ,$$ [4.10]

76

where the first term in the left-hand-side of 4.10 is the kT/C noise due to voltage switching on the ramp generator capacitor, C. The second term in the RHS of 4.10 originates from integrating the current noise and can be reperesented by a noisy voltage on C. Derivation of this term is complicated, however the complete analysis can be found in [47, 54, 55]. Now if we examine 4.10, we observe that the maximum voltage noise occurs at the end of the ramp and at time T_{ramp} such that

$$\sigma^2_{vrn} = \frac{kT}{C} + \frac{2kT\gamma \cdot g_m}{C^2} \cdot T_{ramp} \qquad [4.11]$$

By using 4.9 and 4.11 in 4.8 we have

$$\frac{kT}{C} + \frac{2kT\gamma \cdot g_m}{C^2} \cdot T_{ramp} + \frac{4kT\gamma}{g_m} \leq LSB^2. \qquad [4.12]$$

Now to consider scaling, we can state that LSB^2 is reduced to $\alpha^2 LSB^2$. Consequently, to keep the same precision requirement of 4.12 for the scaled system, the total noise on the left-hand-side of 4.12 should also be reduced by α^2. If we aim to reduce the noise contributed by comparator by α^2, based on (4.9), we should have

$$g_{ms} = \frac{g_m}{\alpha^2}, \qquad [4.13]$$

and by assuming that the input transistor overdrive voltage is kept constant for maximum transistor efficiency [6], the DC current should also be reduced by α^2 such that

$$I_s = \frac{I}{\alpha^2}. \qquad [4.14]$$

Therefore, the comparator total power consumption is scaled by $1/\alpha$ or

$$P_s = I_s \cdot V_s = \frac{I}{\alpha^2} \cdot \alpha V = \frac{P}{\alpha} \qquad [4.15]$$

It is important to realize that increasing g_m also increases the comparator speed and satisfies the bandwidth requirements of the system, which is discussed in detail in Section 4.4.2. This is due to the fact that the unity-gain bandwidth of the amplifier used in the comparator is proportional to g_m/C and hence scaling increases it by a factor of $1/\alpha^3$.

In our ADC architecture, we also scale the sampling frquency by $1/\alpha$ to achieve faster conversion. Therefore, we can deduce that the input time range (i.e., T_{ramp}) is reduced by α. This is possible since the counter is a digital circuit and its speed is increased by $1/\alpha$. In addition to that, the TDC buffer delay is also reduced by α since it is a function of the inverter delays.

To statisfy the noise requirements, kT/C of 4.12, should be reduced by α^2, and therefore we should have

$$C_s = \frac{C}{\alpha^2} . \qquad [4.16]$$

As we know, the voltage ramp signal in the ramp generator is governed by

$$\frac{I}{C} \cdot T_{ramp} = V_{ramp-swing} , \qquad [4.17]$$

where, $V_{ramp-swing}$ is the ramp voltage output swing. Since the voltage supply is scaled by α, to keep the same ramp lineraity, the ramp volatge swing ($V_{ramp-swing}$) should be scaled by α. As mentioned before, T_{ramp} is scaled by α, therefore in 4.17, the ratio I/C needs

to stay constant. This results in a similar current and power scaling as to 4.14 and 4.15, respectively.

If we replace all the scaling parameters into the term $(2kT\gamma g_m / C^2)T_{ramp}$ of 4.11, we observe that this term is reduced by factor α^3 which is less than the constraint of 4.12.

As we mentioned earlier, in our system, the digital and analog power consumptions are equal, and by assuming that this trend is kept with scaling, the total power is scaled by a factor of $0.5 \cdot (\frac{1}{\alpha} + \alpha^2)$. This is smaller than one (i.e., lower power) for $0.63 \le \alpha \le 1$.

This analysis shows that, the PPM ADC can be made faster without increase in the power consumption as we scale down the system by one generation (i.e., $\alpha = 0.7$). The ADC power consumption trend with technology scaling based on this analysis is plotted in Figure 4.33.
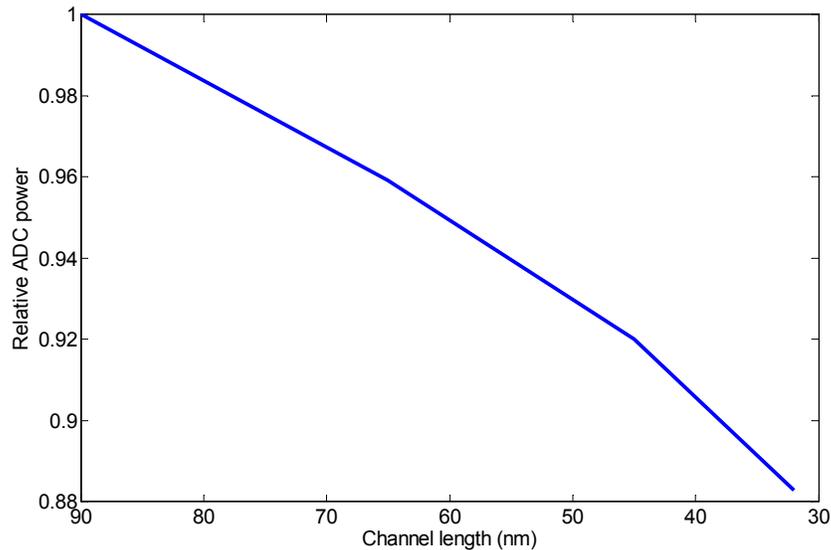
Figure 4.33 : ADC power trend with technology scaling

CHAPTER 5

CONCLUSION

This work has made several important contributions to the field of ultra-low power ADC design, in deep-submicron CMOS technologies. In particular we have:

1. Proposed a time-based and "digitally-friendly" ADC architecture

2. Developed analytical models, theory, and forumlations which describe the advantages of this architecture compared to conventional approaches

3. Implemented and testing two prototypes of the proposed ADC. A state-of-the art energy efficiency of 98fJ/conv.step was achieved.

By applying pulse-position-modulation to the input signal, we are able to replace voltage measurement with time measurement, and employ digital circuitry to significantly reduce the power consumption and required silicon area. The analog circuitry is therefore reduced to two simple building blocks, leading to less design complexity and lower power consumption. The design trade-off is in the digital post-processing complexity required to convert the non-uniform samples to uniform ones. But this trade-off is quite favorable given recent technological advancements in nanometer CMOS technologies.

The proposed ADC design techniques are envisioned for use in ultra-small sensing nodes as part of wireless sensing for environmental monitoring or for point-of-care diagnostics.

Figure 5.1 shows the Figure of merit $\dfrac{P}{2 \cdot BW.2^{B}}$ of ADCs published from 2006 to 2009 at ISSCC [6]. As we see, the PPM ADC figure of merit is comparable with the state of the art.
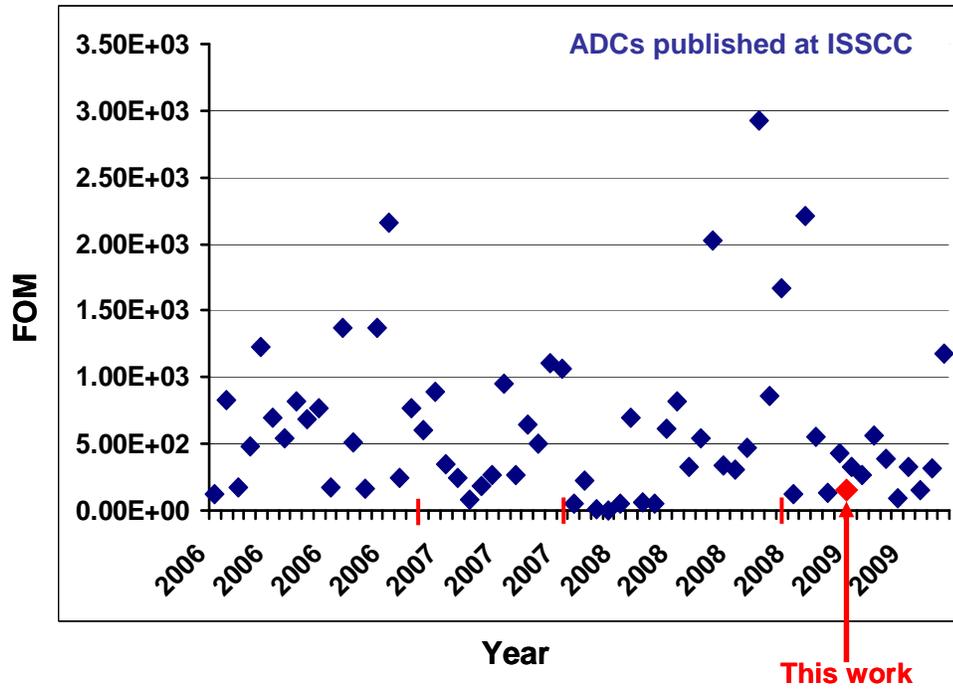
Figure 5.1 : Recent ADC's figure of merit

5.1 Suggestions for the future research

Time-based ADCs are promising for future research, due to their low power and small area. Exploiting these advantages, some future research areas are proposed.

5.1.1 PPM ADC in image sensors

Most analytical systems in biotechnology are based on optical methods such as fluorometry and luminometry. CMOS image sensors are the best candidate for the optical imaging systems required in these applications since these offer higher integration while providing an extremely low cost [56]. A recent trend in high-performance CMOS image sensors is the digital pixel sensor (DPS) architecture in which an ADC is assigned to and integrated within each pixel [56]. Dynamic range and pixel size are two of the main challenges in DPS imagers. An ADC architecture which can be shared between different pixels is desirable to reduce the pixel size and total chip power consumption. Modification of the time-based ADC architecture, developed during this PhD, is an attractive alternative approach in these imagers. The reasons are as follows:

Building blocks can be shared between ADCs, requiring just one comparator and set of registers per pixels as will be described later.

- Using a two-step TDC technique can improve the dynamic range.

- The precise TDC in the ADC block can also be used for TOF (time-of-flight) measurement in 3-D imagers.

5.1.2 Multichannel ADC

The PPM ADC is an attractive candidate for a multichannel data-conversion for use in neural recording and biomedical sensing. In some scan and recording applications, there is a need for more than 1000 ADC nodes to record the signal. The PPM ADC is a good candidate for this application. The potential multichannel architecture is illustrated in Figure 5.2. One counter and one delay line TDC are shared between all the channels. Each ADC consists of a comparator, a register fed by the counter and flip-flops series fed by the delay line TDC. The counter output goes to registers allocated to each ADC channel. The delay line TDC can be calibrated on line in a DLL (digital locked loop) and again shared between all the ADC's (Figure 5.2). ADC comparators generate output signals (similar to *stop* signal in the prototype PPM ADC). The comparator outputs sample the status of the delay line by the sampler flip-flops allocated to each channel. Since the number of channels is quite high, the additional power of a DLL loop is negligible and the accuracy of the measurement is kept constant despite temperature or supply voltage variation.

The ramp generator with buffer can be shared between several channels, without the need for individual sample and hold blocks, and this can dramatically reduce the silicon area and power consumption.
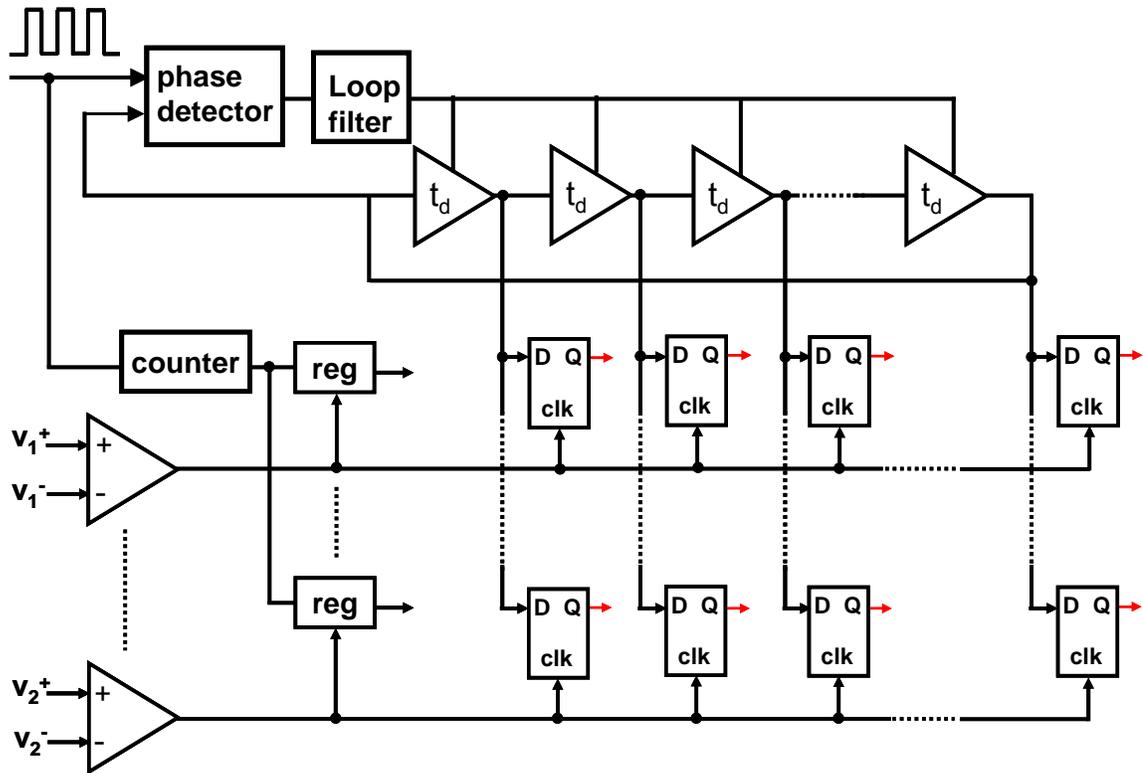
Figure 5.2 : Multichannel ADC

5.1.3 Redundancy in VTC-based ADC

Time-based ADCs using VTCs (voltage to time converters) are described in chapter 1. Since these VTC blocks are mostly digital circuits and consume little area and power, there is a possibility to have many VTCs and TDCs, with a poor precision in a redundant way, as shown in Figure 5.3. The final output is the average of the redundant measurements. This architecture can potentially reduce the power consumption of the ADCs with the same accuracy.
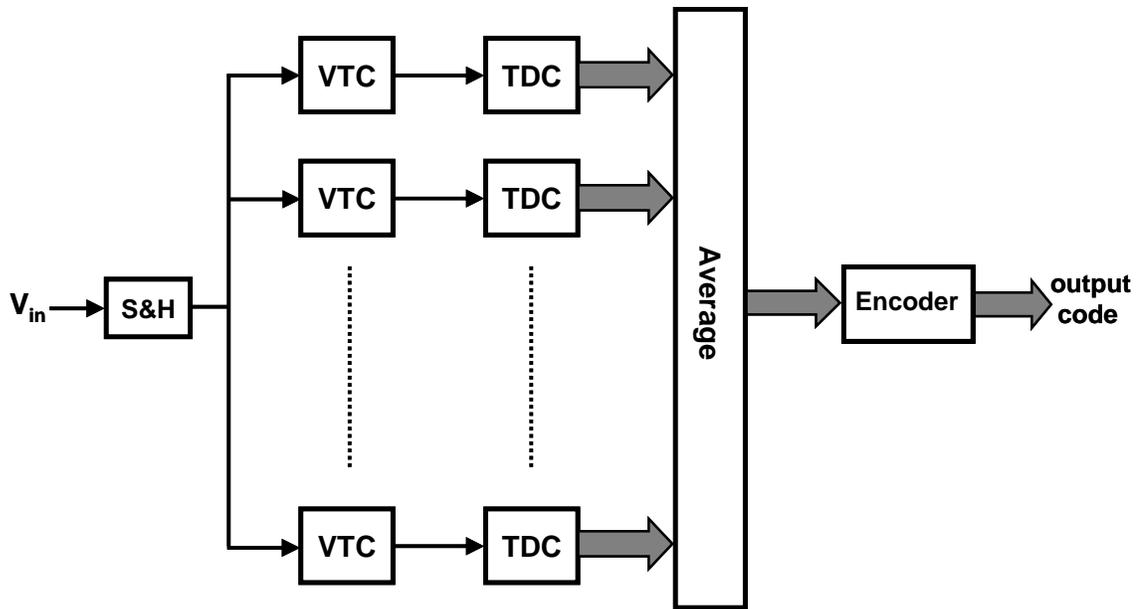
Figure 5.3 : Redundant time-based ADC

APPENDICES

APPENDIX A

ITERATIVE RECOVERY ALGORITHM

This section covers pertinent background information selected from [57] which are required to understand the iterative recovery algorithm used for converting non-uniform to uniform sampling. Next, the iterative recovery itself is explained.

A.1 Iterative algorithm

Iterative algorithms are recursive in nature, in which a new solution is computed as new data becomes available where the new value is obtained by updating the old value as opposed to computing the new result from scratch. An example of an iterative algorithm is the famous steepest descent method [57]. At each step the solution approaches closer to the final solution. In signal processing, iterative algorithms are used when there is not a closed-form solution for an equation but we can get an acceptable solution by some degree. In addition, iterative algorithms are flexible and adaptive which makes them very attractive to real time systems. Their main issue is convergence. We need to set some constrains and prove that the algorithm will converge to a unique solution either mathematically or empirically [57].

A.2 Contraction mapping

Contraction mapping is a powerful tool to prove convergence of an iterative algorithm and it is defined in this way:

Let T be a transfer function which maps space S into S. T is a contraction mapping if there is an α with $0 \leq \alpha < 1$ such that

$$\left\| T(x) - T(y) \right\| < \alpha \left\| x - y \right\| \quad \text{for all x,y} \qquad \text{(A.1)}$$

Now, if T is a contraction mapping on a convex set, there is a unique vector x such that $x=T(x)$, x is called the fixed point here and can be obtained through iteration of T (Proof in page 630 [57]). As an example, in order to find x in the equation $Ax=B$ instead of calculating the inverse of A, we can easily find it by iterating on a function T defined as:

$$T(x) = (I - A)x + B \qquad \text{(A.2)}$$

It is easy to show that $T(x)$ has contraction mapping property. It is worth mentioning that a lot of problems can be solved through this algorithm, for example LMS and neural networks and training algorithms.

A.3 Iteration by composition of mappings

Many signals that we deal with have some known properties. For example they are band limited or symmetric. However when we measure them, we loose some of these properties because of the nature of our measurement. It is desired to give back this property to the signal to some extent. The iterative methods usually work in this situation by finding the nearest signal that satisfies original properties by composition of mappings. There is a famous example for this - When we take samples from a band limited signal, we truncate the signal in time due to the finite number of samples; therefore it expands to infinity in frequency domain. This problem is called band limited reconstruction [58]. As we go through the iteration, we try to satisfy the first property (band limit) and then the second one (finite samples) and so forth, until the original signal is reconstructed through composition of these mappings.

We will describe this method completely here:

Let Φ be a linear manifold M in a Hilbert space, meaning that the linear combination of elements in M is again in M and let Φ' be its orthogonal complement. We define P as the orthogonal projection operator on to Φ. Then the projection of point f to Φ is a point g.

$$Pf = g \qquad\qquad (A.3)$$

It means that we find the signal in Φ that is nearest to f or the nearest signal that satisfies the constraints in the set Φ. Let Q be the orthogonal projector to Φ'.

$$Q = I - p \quad , \text{I: identity operator} \qquad (A.4)$$

Now we address the problem of alternate projection in this way. Φ_a and Φ_b are two Hilbert spaces with different properties. An element f is supposed to belong to Φ_b, but due to our measurement we have data g in Φ_a which is the projection of f to Φ_a. We want a way to compute f from g. We define P_b as the projection operator to Φ_b and Q_a as the projection to Φ_a'.

Now we define a transformation function as T ($f=T\,g$). Rather than trying to find T, we try to iterate the equation:

$$f^{[k+1]} = g + Q_a P_b f^{[k]}, \quad f^{[0]} = g; \qquad (A.5)$$

The Figure A.1 shows the geometric illustration of alternate projection which makes it easier to understand. In the first iteration, shown in Figure A.1(a), we project g to Φ_b with P_b operator. $P_b g$ is then projected to Φ_a' with Q_a. The result of this projection, h, is added with g and makes f_1. In the second iteration shown in Figure A.1 (b), f_1 is projected to Φ_b and then Φ_a', the result of this iterations is added to g and makes f_2.
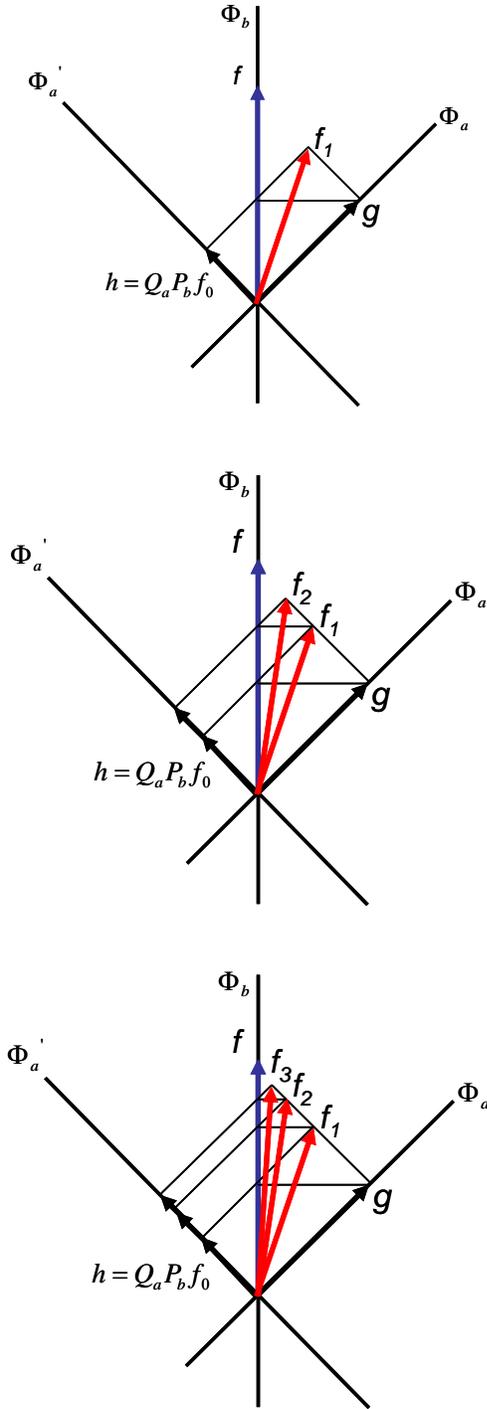
Figure A.1: Composite mapping, first iteration (a), second iteration (b) and third iteration (c)

As we can see in the third iteration (Figure A.1 (c)), in this process we get closer to f (the answer) as we iterate more.

As we already expected there must be some constraints on these operators for the equation to converge. Those constraints are defined this way:

1. f is uniquely defined if : $\Phi_b \cap \Phi_a^{'} = 0$

2. The inverse operator T has bounded inverse if and only if: $\| Q_a P_b \| < 1$

As mentioned before, one of the main applications of alternative projection is the problem of band limited reconstruction. Now, we show how the alternate or composition mapping technique works in order to reconstruct the original band limited signal. We define P_t as the projection function which truncates signal in time domain and P_b as the signal which limits the signal in frequency.

$$P_t(t) = 1 , \quad -T \leq t \leq T$$
$$P_t(t) = 0 , \quad \text{otherwise} \tag{A.6}$$

Then the reconstructed signal can be obtained through this iteration:

$$f^{[k+1]} = g + (1 - P_t(t)) F^{-1} \left[f^{[k]}(w) P_b(w) \right] \tag{A.7}$$

$$P_b f = \int_{-b}^{b} F(w)e^{jwt} \qquad \text{(A.8)}$$

PQ There is an elaboration on composition mapping technique called PQ Theorem proposed by Irwin W. Sandberg [59]. This theorem is sometimes called Sandberg theorem and concerns the solution of the equation $PQx = y$ through iteration. In this equation, P, Q and y are given and x needs to be determined. P is an orthogonal projector which takes elements in a space and maps them into a subspace. Band limiting operator is a good example for that. Also P could be simply an identity operator. Q typically represents a nonlinear operator and the problem is to recover signal x after it is distorted by the nonlinearity Q. As can be seen, this technique could have a lot of applications in circuit and system theory in which signals are easily distorted by non idealities.

Theorem: Let *PQ* is defined over space S and maps elements back to S. Let Q be such that there exist two positive constants k_1 and k_2 with the property that:

$$\text{Re}\langle Qx - Qy, x - y \rangle \geq k_1 \|x - y\|^2 \qquad \text{(A.9)}$$

$$\|PQx - PQy\|^2 \leq k_2 \|x - y\|^2 \qquad \text{(A.10)}$$

93

Then S contains exactly one element x such that $PQx = y$. In fact, $x = \lim_{n \longrightarrow \infty} x_n$

Where,

$$x_{n+1} = \left(\frac{k_1}{k_2}\right)(y - PQx_n) + x_n \qquad \text{(A.11)}$$

As it has been shown in the literature, Q could be companding operation or non uniform sampling, sample and hold distortion and some other operators.

A.4 Recovering the uniform samples from the non-uniform ones

Richard Wiley [60] has shown that Sandberg theorem can be applied to the reconstruction of band limited signals from non-equally spaced sample values. In this method we apply low pass filtering to the unequally spaced times. This is followed by resampling at the same unequally spaced times and again low pass filtering to obtain a correction signal. Repeated application of this process is shown to converge to the original signal. Wiley has re written the two requirements of the PQ theorem in another format as follows which are equivalent to the original ones mentioned above:

$$\int_{-\infty}^{\infty} (Qx - Qy)(x - y)\,dt \geq k_1 \int_{-\infty}^{\infty} (x - y)^2\,dt \qquad \text{(A.12)}$$

$$\int_{-\infty}^{\infty}(PQx-PQy)^2\,dt \le k_2 \int_{-\infty}^{\infty}(x-y)^2\,dt \tag{A.13}$$

Wiley has shown [60] that these requirements are satisfied for the case of interval average sampling defined as follows and therefore could be extended to impulsive sampling as ε approaches zero. However Marvasti [48] has directly proved that these conditions are true for the impulsive and sample and hold sampling. We define interval average sampling $S(t)$ as follows:

$$S(t)=\frac{1}{\varepsilon}, \quad \frac{-\varepsilon}{2}\le t \le \frac{\varepsilon}{2} \tag{A.14}$$
$$S(t)=0 \text{, otherwise}$$

Now the non-equally spaced interval average sample sequence is

$$Sx = \sum_{n=-\infty}^{\infty} \frac{s(t-t_n)}{\varepsilon} \int_{t_n-\varepsilon/2}^{t_n+\varepsilon/2} x(t)dt \tag{A.15}$$

The sequence $\{t_n\}$ must have the properties that:

$$(t_{n+1}-t_n)\ge d > 0 \tag{A.16}$$

$$\left|(t_n - \frac{n}{2f_s})\right| < \frac{L}{2f_s} \qquad (A.17)$$

As we can see in the above equations, there must be a minimum spacing between the sampling intervals and $2f_s$ is the average sampling rate of the non-uniform sampling. According to the definition by Duffin and Schaeffer [60], if $\{t_n\}$ be a sequence of non uniform samples with the density of $2f_s$ and $0 \le f_B \le f_s$ and $x(t)$ is bandlimited to f_B then,

$$A \le \frac{\sum_n \left|x(t_n)^2\right|}{\int_{-\infty}^{\infty} |x(t)|^2 dt} \le B \qquad (A.18)$$

Where A and B are two positive constants. Now we can show that based on Duffin definition and mean value theorem defined as follows, equation (A.12) and (A.13) are satisfied for average sampling.

$$\frac{1}{\varepsilon} \int_{t_n - \varepsilon/2}^{t_n + \varepsilon/2} x(t)dt = x(t_n^0) \qquad (A.19)$$

Equation A.12 can be re written as:

$$\int_{-\infty}^{\infty} (Sx - Sy)(x - y)dt = \sum_{n=-\infty}^{+\infty} \frac{1}{\varepsilon^2} \left[\int_{t_n - \varepsilon/2}^{t_n + \varepsilon/2} (x - y)du\right]^2 = \sum_{n=-\infty}^{+\infty} ((x(t_n^0) - y(t_n^0))^2 \qquad (A.20)$$

According to A.18 we have

$$\sum_{n=-\infty}^{+\infty}((x(t_n^{\,0})-y(t_n^{\,0}))^2 \geq A\int_{-\infty}^{\infty}(x-y)^2\,dt \qquad (A.21)$$

And therefore

$$\int_{-\infty}^{\infty}(Sx-Sy)(x-y)\,dt \geq A\int_{-\infty}^{\infty}(x-y)^2\,dt \qquad (A.22)$$

, which is the first condition of PQ theorem.

Since P is a band limiting operator according to Parseval theorem we have:

$$\int_{-\infty}^{\infty}(PSx-PSy)^2\,dt \leq \int_{-\infty}^{\infty}(Sx-Sy)^2\,dt = \frac{1}{\varepsilon}\sum_{n=-\infty}^{+\infty}((x(t_n^{\,0})-y(t_n^{\,0}))^2 \qquad (A.23)$$

According to A.18 we have:

$$\sum_{n=-\infty}^{+\infty}((x(t_n^{\,0})-y(t_n^{\,0}))^2 \leq B\int_{-\infty}^{\infty}(x-y)^2\,dt \qquad (A.24)$$

Therefore the second PQ condition is satisfied:

$$\int_{-\infty}^{\infty}(PSx - PSy)^2\,dt \le \frac{B}{\varepsilon}\int_{-\infty}^{\infty}(x-y)^2\,dt \qquad\qquad\qquad\text{(A.25)}$$

Now that we show the two requirements of Sandberg theorem is satisfied we can show that the iterative recovery procedure can be applied to the non uniform samples. All these equations are true if $\varepsilon \longrightarrow 0$ which implies impulsive sampling. However as mentioned before Marvasti has a direct proof for impulsive sampling in [48].

A.5 Iteration procedure for the non-uniform sampled signal

Now that we proved mathematically that requirements of Sandberg theorem are satisfied by the nonlinear operation of non uniform sampling, we can apply the iterative recovery technique to the sequence of non-uniformly sampled signals to recover the original signal. The procedure is defined as follows:

We have y as the distorted or non-uniformly sampled signal at hand so $y=Sx$, where x is the desired signal. Then we apply the low pass filtering operation on y to obtain $x_1=PS(x)$. Now we interpolate x_1 and resample it at the same unequally samples. It is important to pay attention to the fact that we need to know the amount of time deviation from the uniform sampling points in order to resample the signal. After that, we apply low pass filtering again to get $PS(x_1)$ and then we calculate x_2 and x_3 as:

$$x_2 = k(x_1 - PSx_1) + x_1 \qquad\qquad \text{(A.26)}$$

$$x_3 = k(x_1 - PSx_2) + x_2 \qquad\qquad \text{(A.27)}$$

We can continue this way until we don't see much improvement in SNR and that is the point that the algorithm converges, k is the ratio k_1/k_2 which can be taken as 1 in this process. There are some important points need to be considered in this algorithm. Although the sampling points are not uniform, they must have the Nyquist density ($2f_s$). Sampling instants are better to be taken such that $|t_k - KT| \leq T/4$. This is a sufficient condition to ensure a stable sampling set. If we relax this condition, there is no guarantee that the sampling set converges at the Nyquist rate. For $|t_k - KT| \leq T/2$, the iterative technique slowly converges and at the rates lower than Nyquist the iteration method diverges.

BIBLIOGRAPHY

[1]   M. S. Emery, et al., "A Multi-Channel ADC for Use in the PHENIX Detector," *IEEE Transactions On Nuclear Science*, vol. 44, no. 3, pp. 374-378, June 1997.

[2]   N. Nambiar, "A Current Mode Multi-channel Wilkinson ADC," *International conference on signals and electronic systems (ICSES)*, pp. 11-14, Sep. 2008.

[3]   E. Delagnes, D. Breton, F. Lugiez, and R. Rahmanifard, "A Low Power Multi-Channel Single Ramp ADC With Up to 3.2 GHz Virtual Clock," *IEEE Transactions On Nuclear Science*, vol. 54, no. 5, pp. 1735-1742, Oct 2007.

[4]   T. Fusayasu, "A Fast Integrating ADC Using Precise Time-to-Digital Conversion," *Nuclear Science Symposium Conference Record*, vol. 1, pp. 302-304, Oct. 2007.

[5]   O. B. Milgrome, S. A. Kleinfelder, M. E. Levi, "A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science," *IEEE Transactions On Nuclear Science*, vol. 39, no. 4, pp. 771-775, 1992.

[6]   B. Murmann, "A/D Converter Trends: Power Dissipation, Scaling and Digitally Assisted Architectures," *IEEE 2008 Custom Integrated Circuits Conference (CICC)*, pp. 105-112, Sep. 2008.

[7]   B. Murmann and B. E. Boser, "A 12-bit 75-MS/s Pipelined ADC using open-loop Residue Amplification," *IEEE Journal of Solid State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[8]   A. Nazemi, et al., "A 10.3 GS/s 6bit Time-Interleaved/Pipelined ADC Using Open-Loop amplifiers and Digital Calibration in 90nm CMOS, " *VLSI Symp. Dig. Tech. Papers*, pp. 18-19, June 2008.

[9]   H. Lee and C. G. Sodini, "Analog-to-Digital Converters: Digitizing the Analog World," *Proceedings of the IEEE*, pp. 323-334, Feb. 2008.

[10]   J. K. Fiorenza et al., "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2658-2668, Dec. 2006.

[11]   L. Brooks and H. S. Lee, "A Zero-Crossings-Based 8-bit 200 MS/s Pipelined ADC," *IEEE Journal of Solid State Circuits*, vol. 42, no. 12, pp. 2677-2687, Dec. 2007.

[12]   J. Hu, et al., "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Residue Amplification," *VLSI Symp. Dig. Tech. Papers*, pp. 216-217, June 2008.

[13] S. Borkar, "Design Challenges of Technology Scaling," *IEEE Micro*, vol.19, pp.23-29, Apr. 1999.

[14] M. H. Perrott, "Making Better Use of Time in Mixed-Signal Circuits," http://www-mtl.mit.edu/researchgroups/perrottgroup/Publications/Talks/better_timing_2007.pdf

[15] R.B. Staszewski, et al., "All-digital TX Frequency Synthesizer and Discrete-time Receiver for Bluetooth Radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no.12, Dec. 2004.

[16] M. Z. Straayer and M. H. Perrott, "A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based Quantizer and DEM circuit in 0.13μ CMOS," *VLSI Symp. Dig. Tech. Papers*, pp. 246-247, June 2007.

[17] Understanding Integrating ADCs, http://www.maximic.com.cn/pdfserv/en/an/AN1041.pdf

[18] A. H. Reeves, "Electrical Signaling System," patent, Feb. 3,1942.

[19] Analog Devices Data Conversion Handbook, http://analog.com/library/analogDialogue/archives/39-06/data_conversion_handbook.html

[20] F. Marvasti, *Nonuniform Sampling Theory and Practice*, Kluwer Academic Publisher, 1990.

[21] E. Allier, et al., "120nm Low Power Asynchronous ADC," *ISLPED'OS*, Aug. 2005

[22] F. Akopyan, R. Manohar, A. B. Apsel, "A Level-Crossing Flash Asynchronous Analog-to-Digital Converter," *Proceedings of the 12th IEEE International Symposium on Asynchronous Circuits and Systems(ASYNC'06)*.

[23] B. Schell and Y. Tsividis, "A clockless ADC/DSP/DAC System with Activity-Dependent Power Dissipation and No Aliasing," *ISSCC Dig. Tech. Papers*, pp. 550-551, Feb. 2008.

[24] N. Sayiner, H. V. Sorensen and T. R. Viswanathan "A Level-Crossing Sampling Scheme for A/D Conversion," *IEEE Transactions on Circuits and Systems II*, vol. 43, no. 4, pp. 335 – 339, Apr. 1996.

[25] E. Allier, et al., "A New Class of Asynchronous A/D Converters Based on Time Quantization," *Ninth International Symposium on Asynchronous Circuits and Systems (ASYNC)*, pp. 196 – 205, May 2003.

[26] H. Pekau, A. Yousif and J. W. Haslett, "A CMOS Integrated Linear Voltage-to-Pulse-Delay-Time Converter for Time-Based Analog-to-Digital Converters," *ISCAS 2006*, pp. 2373-2376.

[27] J. Kim and S. Cho, "A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage-Controlled Oscillator," *ISCAS 2006*, pp. 3934-3937.

[28] T. Watanabe, T. Mizuno and Y. Makino, "An All-Digital Analog-to-Digital Converter With 12-µV/LSB Using Moving-Average Filtering," *IEEE Journal of Solid State Circuits*, vol. 38, no. 1, pp. 120–125, Jan. 2003.

[29] A. Iwata, N. Sakimura, M. Nagata and T. Morie, "The Architecture of Delta Sigma Analog-to-Digital Converters Using a Voltage-Controlled Oscillator as a Multibit Quantizer," *IEEE Transactions on Circuits and Systems II*, vol. 46, no. 7, pp. 941-945, July 1999.

[30] R. Naiknaware, H. Tang and T. S. Fiez, "Time-Referenced Single-Path Multi-Bit ΣΔ ADC using a VCO-Based Quantizer," *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 7, pp. 596 – 602, July 2000.

[31] B. M. Helal, M. Z. Straayer, G. Y. Wei and M. H. Perrott, "A Low Jitter 1.6 GHz Multiplying DLL Utilizing a Scrambling Time-to-Digital Converter and Digital Correlation," *VLSI Symp. Dig. Tech. Papers*, pp. 302-303, Feb. 2007.

[32] B. K. Swann et al., "A 100-ps Time-Resolution CMOS Time-to-Digital Converter for Positron Emission Tomography Imaging Applications," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 11, pp. 1839-1852, Nov. 2004.

[33] T. E. Rahkonen and J. T. Kostamovaara, "The Use of Stabilized CMOS Delay Lines for the Digitization of Short Time Intervals," *IEEE Journal of Solid-State Circuits,* vol. 28, no. 8, pp. 887-894, Aug. 1993.

[34] J. Christiansen, "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops," *IEEE Journal of Solid-State Circuits,* vol. 31, no. 7, pp. 952-957, July 1996.

[35] J. P. Jansson, A. Mantyniemi and J. Kostamovaara, "A CMOS Time-to-Digital Converter with Better than 10ps Single-shot Precision," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 6, pp. 1286-1296, June 2006.

[36] R. B. Staszewski et al., "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Transactions on Circuits and Systems II*, vol. 53, no. 3, pp. 220 – 224, March 2006.

[37] S. Hanzler et al., "90nm 4.7ps-Resolution 0.7-LSB Single- Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization," *ISSCC Dig. Tech. Papers*, pp. 548-549, Feb. 2008.

[38] A.H. Cahn and G. W. Roberts, "A deep sub-micron timing measurement circuit using a single-stage Vernier delay line," *CICC*, pp.77-80, May 2002.

[39] P. Chen et al., "A PVT Insensitive Vernier-Based Time-to-Digital Converter With Extended Input Range and High Accuracy," *IEEE Transactions On Nuclear Science*, vol. 54, no. 2, pp. 294-302, April 2007.

[40] T. Xia et al., "Self-Refereed on-chip Jitter Measurement Circuit Using Vernier Oscillator," *IEEE computer society annual symposium on VLSI*, pp.218-223, May 2005.

[41] P. Dudek, S. Szczepnski and J. V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE Journal of Solid-State Circuits*, vol. 35, no.2, pp.240-247, Feb. 2000.

[42] V. Ramakrishnan and P. T. Balsara, "A Wide-Range, High-Resolution, Compact, CMOS Time to Digital Converter," *VLSID' 06*, Jan. 2006.

[43] C. Ljuslin et al, "An Integrated 16-channel CMOS Time to Digital Converter," *IEEE Transactions on Nuclear Science*, vol.41, no.4, August 1994.

[44] E. Raisanen-Ruotsalainen, T. Rahkonen and J. Kostamovaara, "An Integrated Time-to-Digital Converter with 30-ps Single-Shot Precision," *IEEE Journal of Solid-State Circuits,* vol.35, no. 10, pp. 1507-1510, Oct. 2000.

[45] T. Sundstrom et al, "Power Dissipation Bounds for High-Speed Nyquist Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems I,* vol.56, no. 3, pp. 509 – 518, March 2009.

[46] P. Nuzzo et al, "Noise Analysis of Regenerative comparators for reconfigurable ADC architecture," *IEEE Transactions on Circuits and Systems II*, vol.55, no. 6, pp. 1441-1454, July 2008.

[47] A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," *IEEE Journal of Solid-State Circuits,* vol.41, no. 8, pp. 1803-1816, Aug. 2006.

[48] F. Marvasti, M. Analoui and M. Gamshadzahi, "Recovery of signals from nonuniform samples using iterative methods," *IEEE Transactions on Signal Processing*, vol.39, issue 4, April 1991.

[49] H. Y. Yang and R. Sarpeshkar, "A Time-Based Energy-Efficient Analog-to- Digital Converter," *IEEE Journal of Solid-State Circuits*, vol. 40, no.8, Aug. 2005.

[50] F. Azaïs, et al., "A Low-Cost Adaptive Ramp Generator for Analog BIST Applications," *VLSI Test Symposium*, pp. 266–271, May 2001.

[51] F. Kaess et al., "New encoding scheme for high-speed flash ADC's," *ISCAS*, vol. 1, pp. 5–8, June 1997.

[52] E. A. M. Klumperink, et al., "Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing," *IEEE Journal of Solid State Circuits*, vol. 35, no. 7, pp. 994–1001, June 2006.

[53] S. Naraghi, M. Courcy, and M. P. Flynn, "A 9bit 14μW 0.06mm^2 Pulse Position Modulation ADC in 90nm digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 548-549, Feb. 2008.

[54] H. Tian, B. Fowler and A. El Gamal, "Analysis of Temporal Noise in CMOS Photodiode Active Pixel sensor," *IEEE Journal of Solid State Circuits*, vol. 36, no. 1, pp. 92–101, Jan 2001.

[55] A. Hassibi, EE 382V, integrated sensors, University of Texas

[56] A. El Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits and Device Magazine*, vol. 21, no. 3, pp. 6 – 20, May 2005.

[57] T. K. Moon and W. C. Stirling, "*Mathematical methods and algorithms for Signal Processing,*" Prentice Hall publisher.

[58] R. G. Wiley, "On an Iterative Technique for Recovery of Bandlimited Signals," *Proceedings of the IEEE*, vol. 66, no. 4, pp. 522 – 523, April 1978.

[59] I.W. Sandberg, "Notes on PQ Theorems," *IEEE Transactions on Circuit and Systems I*, vol. 41, no. 4, pp. 303-307, April 1994.

[60] R. Wiley, "Recovery of Bandlimited Signals from Unequally Spaced Samples," *IEEE Transactions on Communications*, vol. 26, no.1, pp.13-137, Jan. 1978.