Quantum point contact transistor with high gain and charge sensitivity

Ç. Kurdak,[a] L. Farina, and K. M. Lewis
Department of Physics, University of Michigan, Ann Arbor, Michigan 48109

(Received 9 November 2000; accepted for publication 6 December 2000)

We analyze the potential performance of quantum point contact (QPC) devices in charge detection applications. For the standard QPC structure we show that the charge sensitivity is strongly dependent on gate geometry and can be close to the quantum limit, and that the gain parameter is less than one under bias conditions where the charge sensitivity is optimized. We propose a novel QPC device consisting of two split gates for defining the QPC and a third gate which can be used to filter out hot electrons that are emitted from the QPC. We show that this proposed device can have a high gain and a charge sensitivity close to that of single electron transistors. The device can be realized using high quality GaAs/AlGaAs with a two-dimensional electron gas and standard nanofabrication techniques. Unlike single electron transistors, the gain of the proposed device does not depend on the charge configuration near the active region of the device. Therefore the device can be used as an electrometer without a feedback charged locked loop and multiple devices can easily be integrated. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1344584]

I. INTRODUCTION

A quantum point contact (QPC) is a three-terminal device consisting of a quasi-one-dimensional constriction with subband energy levels that can be controlled by split gates.[1] The physics of ballistic electron transport through such a constriction has been intensively studied.[2] The size of the constrictions can be close to the Fermi wavelength of electrons; therefore the wave-like nature of electrons plays an important role in the transport behavior of these devices. The transport properties are best described by the Landauer formalism.[3] In this description, for a smooth constriction, the conductance is given, in units of $2e^2/h$, by the number of occupied subbands. Even though QPCs have been used to control the coupling between two electron systems or to inject and detect ballistic electrons in many physics experiments for over a decade, they have not been used as transistors to measure charge or voltage on an external device until recently.[4,5]

In this article we investigate the potential performance of QPC devices in low-noise charge detection applications. There is indirect evidence from low-frequency noise measurements that QPC devices are charge sensitive enough to resolve small changes in electric fields caused by the motion of a single electron.[6–9] Low-frequency resistance fluctuations in QPCs arise from the changes in the remote ionized impurity configuration near the constriction and the effects are most pronounced near the pinch-off regime of the QPC.[8,9] In the next section we provide small signal analysis of a quantum point contact as a transistor. We find that the charge sensitivity of a QPC depends strongly on the gate geometry and with proper fabrication can be close to the quantum limit. The analysis also indicates that the voltage gain is less than one for low bias currents where the noise performance is optimized. We propose that by adding a third gate near the QPC we can turn the QPC into a hot electron transistor, which would have similar charge sensitivity but a voltage gain much larger than one. We predict the noise performance of this proposed QPC device to be comparable to that of a single electron transistor (SET) and superior to that of low noise semiconductor transistors, such as high electron mobility transistors.

Both SETs and QPC devices have very low gate capacitance (fF). However, there are many applications where low noise charge sensitive amplifiers are needed to measure the signals of a macroscopic device with large capacitance (pF-nF). The mismatch between the capacitance of the device under test and the input capacitance of the amplifier results in a suppression of the charge sensitivity of the amplifier given by the ratio of these two capacitances. In principle, this input capacitance problem can be solved if multiple SETs or QPC devices are operated in parallel. We will argue that, in comparison to SETs, it is much more practical to operate multiple QPC devices in parallel as the transconductance of a QPC does not depend on the charge configuration near the active region of the QPC. If we can achieve parallel operation of multiple QPC devices, such devices can be used as electrometers in a variety of applications where signals from large capacitance devices need to be measured.

II. QUANTUM POINT CONTACT AS A TRANSISTOR

A. Small signal analysis

Let us consider the usual QPC structure shown in Fig. 1(a), which consists of two split gates placed on a heterostructure with a two-dimensional electron gas (2DEG) near the top surface. In general the two split gates are electrically connected to each other. Such a QPC is very similar to a field effect transistor, and therefore the leads of the quasi-one-dimensional channel will be referred to as source and drain and the split gates will be referred to as the gate. When a sufficient gate voltage is applied, the electrons underneath

[a]Electronic mail: kurdak@umich.edu

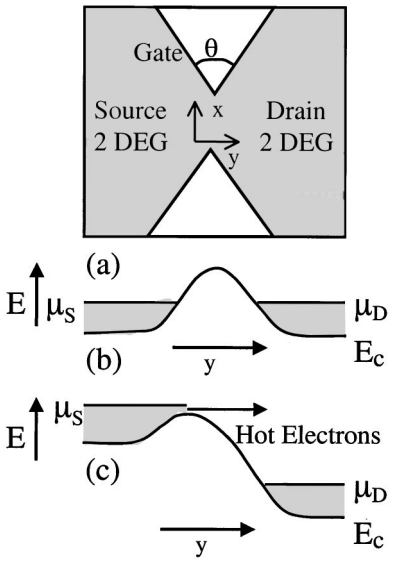

FIG. 1. (a) Schematic diagram of a quantum point contact consisting of two split gates placed on a heterostructure with a 2DEG, (b) energy band diagram when the device is pinched off under zero source–drain bias, and (c) energy band diagram when the source–drain is biased such that there is current injection from the source.

the split gates can be depleted leaving a quasi-one-dimensional channel in between the split gates. The width of the quasi-one-dimensional channel is shortest at the center of the point contact and smoothly increases with distance from the center. The width of the channel can be controlled by the gate voltage. For sufficiently large gate voltage the channel would be completely pinched off, in which case there would be an energy barrier between the source and the drain as shown in the cross section of the energy band diagram of the QPC in the direction of the channel [Fig. 1(b)]. Perpendicular to the channel there is a confinement potential which is nearly parabolic. E_1 and E_2 are the first and second quantized energy levels of this confinement potential. When the device is pinched off, the lowest one-dimensional energy level, E_1, is above the chemical potential of the leads and therefore the energy levels of the one-dimensional channel are unoccupied.

The current–voltage characteristics of a QPC in the pinched off regime were first studied by Kouwenhouven *et al.*[10] For drain–source voltages less than the threshold voltage the device current is found to be zero. At the threshold voltage the chemical potential of the source is aligned with the lowest energy level of the one-dimensional channel and for bias voltages larger than the threshold voltage the device turns on with a differential conductance less than $2e^2/h$. The energy band diagram of the device when current is flowing is shown in Fig. 1(c). Electrons are injected from the source to the drain at a rate that depends only on the relative position of E_1 with respect to the quasi-Fermi energy of the source, given by the Landauer description

$$I=\begin{cases} 0 & \text{for } \mu_S<E_1 \\ \dfrac{2e}{h}(\mu_S-E_1) & \text{for } \mu_S>E_1, \end{cases} \tag{1}$$

where I is the current through the channel, e is the electron charge, h is the Planck constant, and μ_S is the quasi-Fermi energy of the source. Here we assume that only the lowest energy subband contributes to current. The analysis can easily be generalized to the multichannel case.

In order to calculate the small signal parameters of the device we need to know the dependence of E_1 on gate, drain, and source voltages. Changing the gate, drain, and source voltages by the same amount is equivalent to shifting all the energy levels in the device, which leads to the constraint

$$-\frac{1}{e}\left(\frac{\partial E_1}{\partial V_G}+\frac{\partial E_1}{\partial V_D}+\frac{\partial E_1}{\partial V_S}\right)=1, \tag{2}$$

where V_G, V_D, and V_S are the gate, drain, and source voltages, respectively. The negative sign in front of the equation arises due to the negative charge of electrons. The three terms of this equation have the same sign and therefore are all less than one. The first term is particularly important, as it will appear both in the conductance and transconductance of the QPC:

$$\alpha=-\frac{1}{e}\left(\frac{\partial E_1}{\partial V_G}\right). \tag{3}$$

The parameter α, a positive number less than 1, describes the coupling of the gate to the one-dimensional channel. We will define a parameter β

$$\left(\frac{\partial E_1}{\partial V_D}\right)=\beta\left(\frac{\partial E_1}{\partial V_S}\right) \tag{4}$$

which is a positive number and describes the asymmetry of the QPC.

When the current through the constriction is small, we can assume that there is not a significant voltage drop between the source and the source contact, and therefore $\mu_S=-eV_S$. Now, using Eq. (1) we calculate all the small signal parameters of the QPC. The differential conductance g and the transconductance g_{tr} are given by the following expressions:

$$g=\frac{\partial I}{\partial V_S}=\frac{(\alpha+\beta)}{(1+\beta)}\frac{2e^2}{h}, \tag{5}$$

$$g_{\text{tr}}=\frac{\partial I}{\partial V_G}=\alpha\frac{2e^2}{h}. \tag{6}$$

As in other field effect transistors, the voltage gain parameter of a QPC device is given by the ratio $g/g_{\text{tr}}=(1+\beta)/(1+\beta/\alpha)$. Note that for all possible values of α and β the voltage gain parameter is less than one. However, if the current through the constriction is large the assumption of a small voltage drop between the source and source contact is no longer valid. Such a voltage drop would lead to a suppression of device conductance. In fact, in the extreme limit of high bias, when the electron velocities near the constriction reach saturation velocity, the differential conductance of the device would go to zero. In the saturation regime the noise performance of the device is far from optimized, even though the gain parameter can be larger than one.

B. Noise analysis

Noise measurements on QPC devices are performed at cryogenic temperatures and the devices are shown to exhibit shot noise near the pinch off regime.[11] However, noise measurements have not been performed at very high currents, for example, when the device is operated in the saturation regime. In this regime we expect significant additional thermal noise, resulting in degradation of the noise performance. In the noise analysis of the device, we will only consider low bias operation and ignore contributions to noise from thermal and quantum fluctuations. Real devices also exhibit low-frequency noise, such as $1/f$ or random telegraph noise, which are not of fundamental origin and will not be included in the following analysis.[6–9] Using the small signal parameters of the device, we can express the gate charge noise spectrum S_Q in terms of the current noise power spectrum, $S_1=2eI$,

$$S_Q=\frac{C_G^2}{g_{\mathrm{tr}}^2}S_I, \tag{7}$$

where C_G is the total gate capacitance. The gate is capacitively coupled to the source, the one-dimensional channel, and the drain. Therefore we can express gate capacitance as a sum of three capacitors, $C_G=C_{GS}+C_{GC}+C_{GD}$, where C_{GS}, C_{GC}, and C_{GD} are gate-to-source, gate-to-channel, and gate-to-drain capacitance, respectively. Even though S_Q determines the charge sensitivity of an electrometer, it is physically more meaningful to use energy sensitivity, E_N, as a figure of merit for noise performance of a QPC transistor;

$$E_N=\frac{S_Q}{2C_G}=\frac{1}{\gamma}\frac{C_{GC}}{g_{\mathrm{tr}}^2}eI, \tag{8}$$

where $\gamma=C_{GC}/C_G$. For a given current the total charge that is contributing to current is given by $eN_C=C_{GC}I/g_{\mathrm{tr}}$, where N_C is the total number of electrons in the channel that are contributing to current. When there is one sublevel contributing to device current, N_C is a small number that depends on bias conditions, device geometry, and density of electrons in the channel. If we rewrite the energy sensitivity in terms of N_C and use the expression for g_{tr} we get

$$E_N=\frac{\pi N_C}{\gamma\alpha}\hbar. \tag{9}$$

Note that the noise analysis presented here is physically meaningful only for N_C greater than one. For the case when N_C is less than one, quantum fluctuations must also be included in the noise analysis. In fact for any detector the energy sensitivity must be larger than $\hbar$ due to quantum fluctuations. For the QPC, both γ and α are less than one and the energy sensitivity is larger than the quantum limit of $\hbar$ by a prefactor that is dependent on the geometry of the QPC. Before discussing how to optimize the device geometry to minimize this prefactor, we should point out that the expected noise performance of a QPC electrometer is similar to that of single electron transistors[12–14] and superior to that of semiconductor field effect transistors.[15] This should not be surprising since, in both the QPC and SET, the dominant noise is shot noise, the transconductance of the devices is on the order of the quantum conductance, and the operation currents and the input capacitances are similarly small.

C. Optimization of geometry

The noise performance of a QPC device is strongly dependent on the geometry of the gate. In this section we will discuss the dependence of energy sensitivity on the width of the contact, w, the depth of the 2DEG, d, and the angle of the contact, θ, for the geometry shown in Fig. 1(a). We focus on how this dependence can be used to optimize the noise performance. E_N, as defined through Eq. (9), has a dependence on device geometry through N_C, γ, and α. γ is determined by the geometry of the 2DEG as well as the gate and will not be calculated in this article. However, the method for optimizing γ is straightforward, the capacitance between the gate and the 2DEG should be dominated by the capacitance between the gate and the channel. This can be accomplished by etching away all the 2DEG except for a channel surrounding the active region of the device.

The optimization of N_C and α is more subtle. The calculations for N_C and α can be obtained from a simple electrostatic model discussed by Davies *et al.*[16] In the calculation, the potential on the exposed surface is set to zero and the gates are negatively biased to V_G. This is a highly simplified but convenient model, which enables us to do analytical calculations. A more realistic model should include a proper treatment of donor and surface states in high fields. Nevertheless, the simplified model captures the main features of the confinement potential and is sufficiently accurate to allow us to see how the geometry affects the noise performance of the device. Furthermore, in this model the 2DEG is neglected, which is a reasonable assumption as we will only consider the device operation near the pinched-off regime, when the 2DEG is depleted. With these boundary conditions and assumptions, the potential for the geometry shown in Fig. 1(a), at $z=d$, is given by

$$\begin{aligned}\frac{\phi(x,y)}{V_G}=\frac{1}{\pi}\Bigg[&\arctan\left(\frac{d\sin(\theta)}{R_+ +(x+w/2)\cos(\theta)-y\sin(\theta)}\right)\\&+\arctan\left(\frac{d\sin(\theta)}{R_- +(x-w/2)\cos(\theta)-y\sin(\theta)}\right)\\&+\arctan\left(\frac{d\sin(\theta)}{R_+ +(x+w/2)\cos(\theta)+y\sin(\theta)}\right)\\&+\arctan\left(\frac{d\sin(\theta)}{R_- +(x-w/2)\cos(\theta)+y\sin(\theta)}\right)\Bigg],\end{aligned} \tag{10}$$

where $R_\pm=\sqrt{(x\pm w/2)^2+y^2+d^2}$.[16] A typical constriction in x and y due to this potential is shown in Fig. 2.

The first sublevel E_1 can be calculated by solving the Schrodinger's equation for this potential and the transconductance can be found from the dependence of E_1 on the gate voltage. For this particular model we Taylor expand the confinement potential around origin and neglect nonpara-

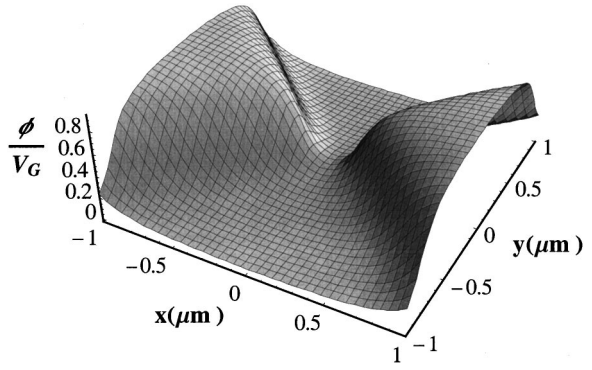

FIG. 2. The electrostatic potential at the depth of the 2DEG due to a voltage applied to the QPC gates for the structure shown in Fig. 1(a) with a gate angle $\theta=90°$, contact spacing $w=0.3$ μm, and 2DEG depth $d=0.1$ μm.

bolic terms in the calculation of E_1, as the additional corrections are well outside the precision of this approximation.We find that the transconductance, which is directly proportional to α, increases almost linearly with the gate angle (Fig. 3). Transconductance is also found to be increasing with decreasing ratio of width to depth, *w/d*, but, for a given *w/d*, is weakly dependent on these parameters individually. Due to this weak dependence we will only present results in terms of *w/d*.

The total number of electrons in the channel, N_C, contributing to current also appears in the calculation of energy sensitivity. N_C is proportional to the one-dimensional density of states, a bias energy dependent term, and the length of the one-dimensional channel, l_{1d}. The density of states and energy bias terms will depend on the source-to-drain voltage and the properties of the 2DEG, but l_{1d} is primarily affected by the gate geometry. The channel length defined here as the width at half maximum of the potential in *y* direction, increases with gate angle as shown in Fig. 3. We also find that l_{1d} increases with *w/d*.

The noise of the QPC device, which is best characterized by E_N, is proportional to l_{1d}/α for given bias conditions. From the minima in l_{1d}/α, plotted for different *w/d* in the inset of Fig. 3, we can calculate the optimum gate angle. The energy sensitivity improves as *w/d* decreases and the decreasing *w/d* has the additional effect of widening the curves, making the choice of angle less important. Therefore to achieve the best energy sensitivity, the widths of the point contacts should be fabricated as small as possible with respect to the two-dimensional electron gas depth, and with the angle determined to be optimum for a given *w/d*.

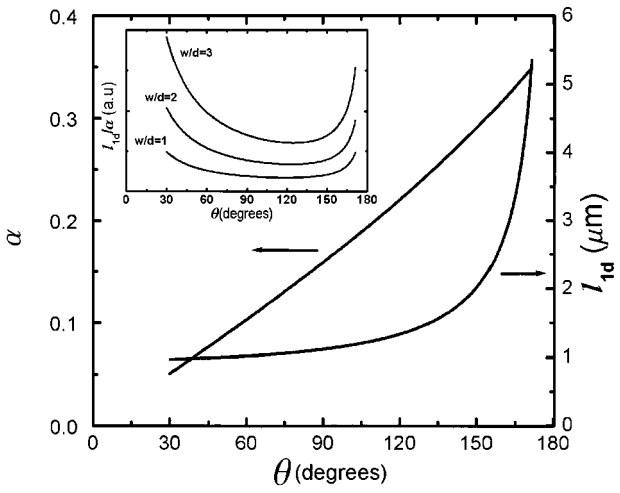

FIG. 3. Dependence of α and l_{1d} on gate angle, θ, for $w/d=3$. The inset shows l_{1d}/α vs α for different values of *w/d*.

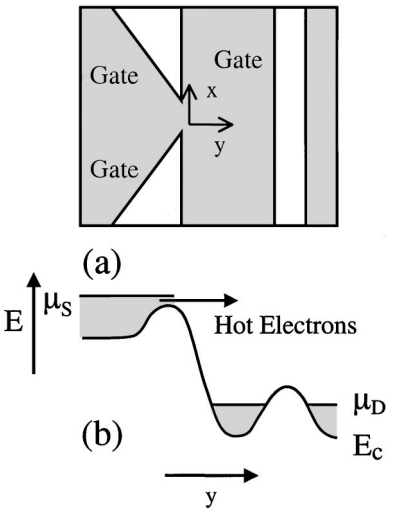

FIG. 4. (a) Schematic diagram of QPC with the addition of a third gate, which can used as an energy filter and (b) the energy band diagram when the device is operated as a hot electron transistor.

III. A HIGH GAIN QUANTUM POINT CONTACT TRANSISTOR

We have shown in the previous section that the QPC device in the usual geometry has good charge sensitivity but low gain. If it is operated in the saturation regime like other field effect transistors then the gain can be large but the additional thermal noise suppresses the charge sensitivity of the QPC. We propose a new QPC device with an additional gate, which has large gain without sacrificing the charge sensitivity. The schematic diagram of this proposed device is shown in Fig. 4(a). The existence of the third gate turns the device into a hot electron transistor.[17,18] For this transistor we will refer to the electron gases on the left of the QPC split gates, in between the split gates and the third gate, and on the right of the third gate as emitter, base, and collector, respectively. Now consider the situation discussed in the previous section where the split gate voltage is such that the QPC is pinched off and the emitter base voltage is large enough such that there will be current injected from the emitter. The emitter current is given by $I_E=(2e/h)(\mu_E-E_1)$, where I_E is the emitter current and μ_E is the chemical potential of the emitter. We will assume that the third gate is biased such that there is an energy barrier between the base and the collector as shown in Fig. 4(b). The barrier can be biased such that the probability of tunneling of cold electrons is negligibly small. However, if the distance between the QPC and the third gate is less than the scattering length,

an easy criteria to achieve in structures fabricated using high quality GaAs/AlGaAs heterostructures, most of the hot electrons injected from the QPC will reach the collector.[19] Under these conditions the collector current would not depend on collector voltage but would be strongly dependent on the split gate voltages, therefore suppressing collector conductance without affecting transconductance. Thus the device can have a gain parameter much larger than one. In the presence of such a filter the collector current noise would still be dominated by shot noise.[20] The energy sensitivity of the device would be suppressed by the collector efficiency, the ratio of collector current to emitter current. Note, however, the collector efficiency can be close to one, in which case the noise performance of such a QPC device would not be significantly degraded.

IV. CONCLUSIONS

In this article we show that QPC devices are promising candidates for low noise electrometer applications. To guide future experiments, we calculate small signal parameters for different gate dimensions and discuss how the gate geometry can be optimized to achieve the best noise performance. We also propose a new QPC device with an additional gate, which can have a high gain and a charge sensitivity close to that of the SET. For the electrometer applications it would be particularly interesting if multiple QPC devices are operated in parallel such that the total input capacitance of the electrometer is matched to that of the device under test. Since the sign of the transconductance of a QPC, unlike the SET, does not depend on the localized charges present near the active region of the device, multiple QPCs can, in principle, easily be operated in parallel. We believe QPC devices may find a wide range of applications in the future if the parallel operation of multiple QPCs is achieved.

ACKNOWLEDGMENTS

We thank A. G. Rojo for useful discussions. This work is partially supported by the Research Corporation and the Alfred P. Sloan Foundation.

[1] B. J. van Wees, H. van Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel, and C. T. Foxon, Phys. Rev. Lett. **60**, 848 (1988).
[2] H. van Houten, C. W. J. Beenakker, and B. J. van Wees, Semicond. Semimetals **35**, 9 (1992).
[3] S. Datta, *Electronic Transport in Mesoscopic Ssytems* (Cambridge University, Cambridge, UK, 1995).
[4] K. K. Ko, E. W. Berg, and S. W. Pang, J. Vac. Sci. Technol. B **14**, 3663 (1996).
[5] L. H. Chen, R. M. Westervelt, K. D. Maranowski, and A. C. Gossard (unpublished).
[6] Y. P. Li, D. C. Tsui, J. J. Heremans, J. A. Simmons, and G. W. Weimann, Appl. Phys. Lett. **57**, 774 (1990).
[7] C. Dekker, A. J. Sholten, F. Liefrink, R. Eppenga, H. van Houten, and C. T. Foxon, Phys. Rev. Lett. **66**, 2148 (1991).
[8] T. Sakamoto, Y. Nakamura, and K. Nakamura, Appl. Phys. Lett. **67**, 2220 (1995).
[9] Ç. Kurdak, C.-J. Chen, D. C. Tsui, S. Parihar, S. Lyon, and G. W. Weimann, Phys. Rev. B **56**, 9813 (1997).
[10] L. P. Kouwenhoven, B. J. van Wees, C. J. P. M. Hartmans, J. G. Williamson, H. van Houten, C. W. J. Beenakker, C. T. Foxon, and J. J. Harris, Phys. Rev. B **39**, 8040 (1989).
[11] M. Reznikov, M. Heiblum, H. Shtrikman, and D. Mahalu, Phys. Rev. Lett. **75**, 3340 (1995).
[12] K. K. Likharev, IBM J. Res. Dev. **32**, 144 (1988).
[13] A. N. Korotkov, Phys. Rev. B **49**, 10381 (1994).
[14] G. Zimmerli, T. M. Eiles, R. L. Kautz, and J. M. Martinis, Appl. Phys. Lett. **61**, 237 (1992).
[15] M. B. Das, IEEE Trans. Electron Devices **19**, 338 (1972).
[16] J. H. Davies, I. A. Larkin, and E. V. Sukhorukov, J. Appl. Phys. **77**, 4504 (1995).
[17] M. Heiblum, D. C. Thomas, C. M. Knoedler, and M. I. Nathan, Appl. Phys. Lett. **47**, 1105 (1985).
[18] A. Palevski, C. P. Umbach, and M. Heiblum, Appl. Phys. Lett. **55**, 1421 (1989).
[19] X. Ying, J. P. Lu, J. J. Heremans, M. B. Santos, M. Shayegan, S. A. Lyon, M. Littman, P. Gross, and H. Rabitz, Appl. Phys. Lett. **65**, 1154 (1994).
[20] R. E. Burgess, Br. J. Appl. Phys. **6**, 185 (1955).