

Nonalloyed and alloyed low-resistance ohmic contacts with good morphology for GaAs using a graded InGaAs cap layer

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Using a thin graded layer of InGaAs starting on GaAs and becoming InAs on the top, low-resistance alloyed and nonalloyed ohmic contacts have been achieved on n^+ -GaAs epilayers grown by molecular-beam epitaxy on a semi-insulating GaAs substrate. In addition, by a suitable choice of the multilayer ohmic metals and by an optimization of the alloying process, good surface morphology was obtained. The transmission-line model is used to extrapolate contact resistances from measurements on test patterns with multiple gap spacings varying from 1 to 10 μm . The nonalloyed contact resistance is found to be 0.025 $\Omega\text{ mm}$ for a GaAs layer doped to 1×10^{16} with a 500- \AA graded InGaAs layer. Alloying the contact at 475 $^\circ\text{C}$ for 60 s produces a contact resistance of 0.019 $\Omega\text{ mm}$. This represents a substantial improvement over the contact resistances obtained by just using an ungraded cap layer of InAs on GaAs. Assuming that the sheet resistance under the contact is the same as the sheet resistance in the top semiconductor layer (this is not strictly true), the nominal value of the specific contact resistance for the nonalloyed situation is $5.32 \times 10^{-7}\ \Omega\text{ cm}^2$, while for the alloyed case the specific contact resistance is $2.56 \times 10^{-7}\ \Omega\text{ cm}^2$. The metal scheme used for the contact is Ni/Ge/Au/Ti/Au.

The contact resistance between a semiconductor device and the contact is of utmost importance for successful operation of the device. Because of a high concentration of surface states, deposition of metals onto an n^+ -GaAs surface results in a Schottky barrier with a barrier height of approximately 0.8 eV. Charge transport through such barriers is dominated by thermionic field emission. For such a contact the contact resistance R_c is found to be around $10^6\ \Omega\text{ cm}^2$.¹ For acceptable device operation, this resistance must be brought down by orders of magnitude. For microwave and millimeter wave operation, the contact resistance should be very small in order to minimize the series resistance. Similarly, for devices like the resonant tunneling diode the resistance must be small enough as not to affect the negative differential resistance of the device. There are two ways of decreasing this contact resistance: either to increase the doping at the metal-semiconductor interface or to reduce the barrier height at the metal-semiconductor interface. With the ability of growing extremely thin epilayers, it has now become possible to use alternative materials to reduce the metal-semiconductor barrier so that the metal-semiconductor interface barrier is indeed reduced.

InAs is very attractive for good ohmic contacts² to III-V compounds because the surface Fermi level of metals is normally pinned above the conduction band of InAs, rather than near midgap. Utilizing this fact, ohmic contacts on GaAs with an InAs cap layer have been recently reported with typical nonalloyed contact resistance values of $10^{-6}\ \Omega\text{ cm}^2$.³ These results, although promising, are still modest. One of the primary reasons for this is the relatively large band-gap difference between InAs and GaAs, which pro-

duces a large conduction-band discontinuity and thus a barrier for charge transport. To improve this situation, in the present investigation results are presented for ohmic contact resistance on GaAs with a InAs top layer, but where the transition from GaAs to InAs is made gradually by a graded InGaAs layer. This design presents the advantage of producing a continuous conduction band between the GaAs and top InAs layer.

Besides the requirement of low resistance, for applications such as electron-beam lithography, surface morphology becomes an important issue. Generally, electron-beam lithography systems employ the method of four-corner registration,^{4,5} and the registration marks are usually detected by scanning with the electron beam and observing the backscattered electron signal. In certain situations alignment to the annealed ohmic contacts is critical. If the surface morphology is not smooth, the noise in the backscattered signal gets high enough in amplitude over the rough surface that registration of any pattern becomes practically impossible.

The samples investigated were grown on a semi-insulating GaAs substrate by molecular-beam epitaxy. An n^+ -GaAs 0.75- μm layer was grown at 610 $^\circ\text{C}$. Then a graded layer starting with GaAs and ending with InAs was grown with the growth temperature decreasing from 610 to 500 $^\circ\text{C}$. The thickness of the graded layer was 500 \AA .

The contact resistances are measured using the well-established transmission-line model (TLM).⁶ The transmission-line contact patterns were defined with standard photolithography and conventional wet chemical-etching techniques. The metal evaporation is carried out in an electron-beam evaporator at a pressure of $2\text{--}4 \times 10^{-7}$ Torr. The

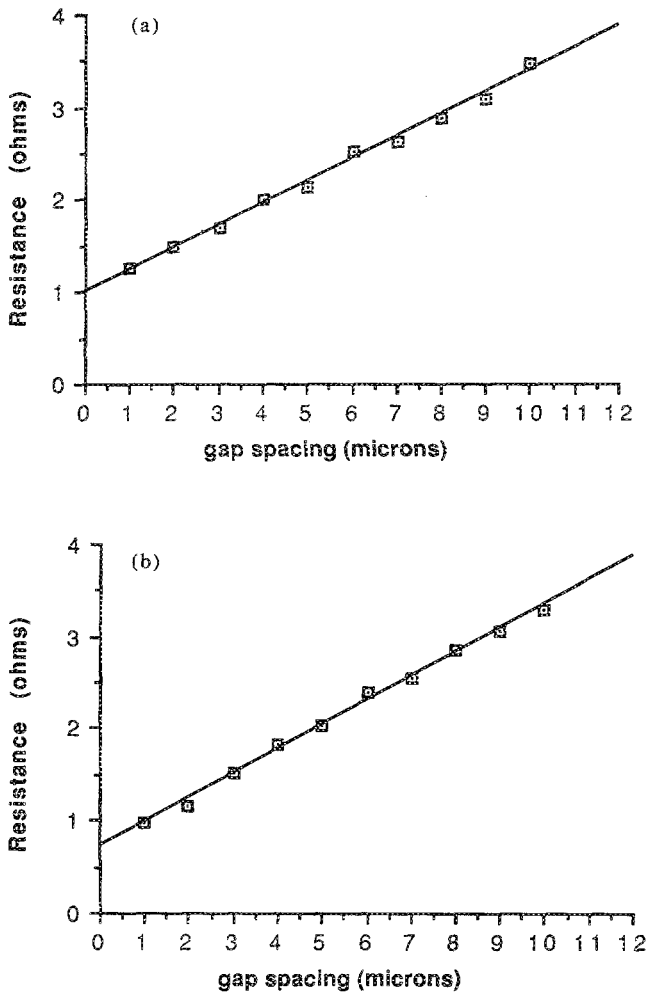


FIG. 1. TLM pattern measurement for the (a) nonalloyed ohmic contact and (b) the contact alloyed at 475 °C for 60 s.

evaporation rate is kept between 15 and 20 Å/s. Immediately prior to mounting the samples into the electron-beam evaporator, they were put in an asher and etched in oxygen plasma at a pressure of 0.25 mTorr for 36 s. The samples were then oxide etched in a 1:30 solution of $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ for 30 s. After the oxide etch the samples were cascade rinsed in deionized water and dried with dry nitrogen and quickly transferred to the electron-beam evaporator. This sequence of procedures is critical for getting good surface morphology on the annealed ohmics.

The metal layers used and the thicknesses from the sam-

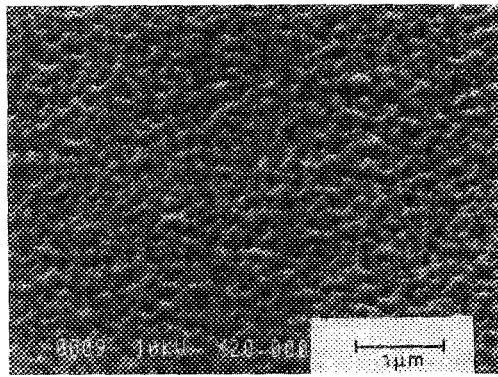
ple surface were as follows: Ni, 250 Å; Ge, 325 Å; Au, 650 Å; Ti, 100 Å; and Au, 1000 Å. These thicknesses have produced good ohmic contacts on n^+ -GaAs. After the metal evaporation the metal was lifted off and alloyed immediately. Annealing was done in an open-tube furnace with N_2 flowing through the tube at a rate of 3 l/s. The alloying procedure begins with a standby period in the load zone of the furnace. It is important to ensure that during the standby period the sample is well below the Au:Ge eutectic temperature. The samples are then transferred rapidly into the middle of the furnace where they remain for the actual annealing period. They are then rapidly withdrawn and allowed to cool.

Pads of length and width equal to 50 μm , separated by gap lengths varying from 1 to 10 μm were used. The resistance between two contacts, R_T , was measured at room temperature using the four-point probe arrangement. A constant current was forced between two probes while measuring the voltage with the other two to eliminate any error due to probe contact resistance. The contact resistance R_c was derived from a plot of R_T versus gap spacing. The method of least squares was used to fit a straight line to the experimental data, which were taken from all available test patterns on the sample. The intersection of the straight line with the abscissa gives the sum of two contact resistances. This resistance R_c includes the resistance of the contact metallization, the semiconductor layer underneath the contacts, and the actual specific contact resistivity for the metal-semiconductor interface. This resistance represents the contact resistance to be connected in series to parasitic region resistance in a real device. The slope of the straight line is proportional to the semiconductor sheet resistance R_{sh} between the contacts.

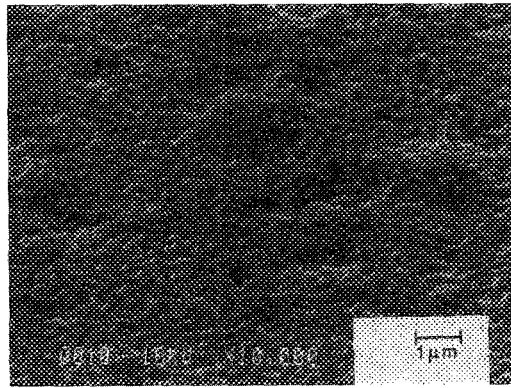
The results of the TLM measurement on the nonalloyed sample are shown in Fig. 1(a). To find the best alloying temperature the alloying time was fixed at 60 s and a temperature range from 400 to 500 °C was considered. The best contact resistance was found to be for an alloying temperature of 475 °C. The results of the TLM measurement for this anneal are shown in Fig. 1(b). Alloying the contact has a small effect on the sheet resistance. This observation confirms the fact that the alloying process does not typically produce significant dopant or composition redistribution resulting in dramatic changes in sheet resistance. A summary of the results is presented in Table I. The transfer resistance is the contact resistance normalized to 1 mm of contact width. Also shown in Table I is the nominal value of the specific contact resistance, ρ_c . This is included as a figure of

TABLE I. Summary of results obtained for the nonalloyed and alloyed contact resistances as a function of different anneal temperatures.

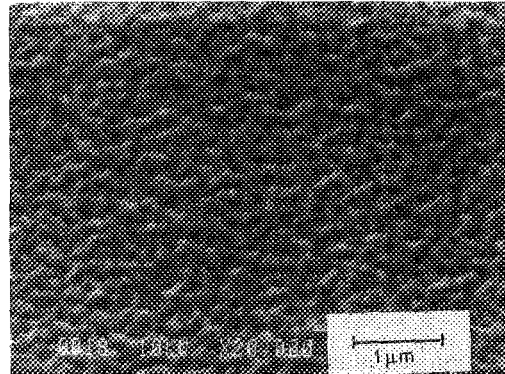
Time (s)	Temperature T (°C)	Transfer resistance R_t (Ω mm)	Transfer length L_T (μm)	Specific contact resistance ρ_c (Ω cm ²) $\times 10^{-7}$	Correlation coefficient R
	nonalloyed	0.025	2.11	5.32	0.994
60	450	0.023	1.71	4.01	0.996
60	475	0.019	1.40	2.56	0.995
60	500	0.024	1.72	4.08	0.996



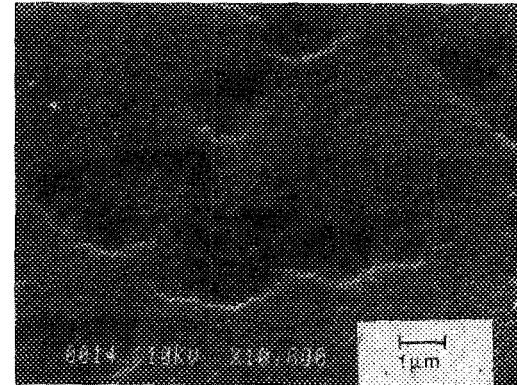
(a)



(c)



(b)



(d)

FIG. 2. Scanning electron micrograph of the surface morphology of (a) nonalloyed ohmic contact and (b) the contact alloyed at 450 °C for 60 s. Further increase in alloying temperature results in increasing roughness in surface morphology as shown in (c) contact alloyed at 475 °C for 60 s, and (d) contact alloyed at 500 °C for 60 s.

merit for comparison with results reported for conventional GaAs structures obtained in a similar manner. The specific contact resistance was calculated by assuming that the semiconductor sheet resistance underneath the contacts remains unchanged. It is clear, however, that the alloying procedure changes the semiconductor sheet resistance under contacts considerably, making this assumption inaccurate.

The morphology of the contacts is shown in Fig. 2. With increasing alloying temperatures the surface becomes increasingly rough, as expected. However, it can be noted that for the optimum alloying temperature the morphology is not very rough. Using the process discussed so far, 0.25- μm gates were successfully aligned to source-drain ohmic pads in our laboratory. Work is currently under way to further improve the morphology of the contacts by using a cap layer of silicon nitride or silicon dioxide, and a thinner InGaAs layer.

The results reported are perhaps not truly the optimum conditions for the contacts. A truly optimum condition will require a complete response surface experiment with parameters like the thickness of the cap layer, doping of the cap layer, growth conditions of the cap layer, and anneal conditions as variable parameters.

In conclusion, results have been presented that show a significant decrease in the nonalloyed and alloyed contact resistances of ohmic contacts on GaAs by incorporating a graded layer of InGaAs as a cap layer. Contact resistance of 0.025 and 0.019 $\Omega \text{ mm}$ have been obtained for the nonalloyed and alloyed contacts, respectively. By taking extreme care in the preparation and annealing of the samples, adequate morphology is obtained.

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