Molecular-beam epitaxial growth and characterization of silicon-doped AlGaAs and GaAs on (311)*A* GaAs substrates and their device applications

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The possibility of reliable and reproducible *p*-type doping of (311)*A* GaAs by Si during molecular-beam epitaxial growth and the application of such doping in the realization of high-performance electronic devices have been investigated. It is seen that *p*-type doping upto a free hole concentration of 4×10^{19} cm^{-3} can be obtained under conditions of low As_4 flux and high ($\geqslant$660 °C) growth temperatures. *n*-type doping up to a level of 1×10^{19} cm^{-3} is obtained at low ($\leqslant$500 °C) growth temperature and high As_4 flux. The *p*-type doping is extremely reproducible and the incorporation of Si atoms into electrically active As sites is at least 95%. The doping behavior has been studied and confirmed by Raman spectroscopy. *n-p-n* heterojunction bipolar transistors grown by all Si doping exhibit excellent current voltage characteristics and a common emitter current gain $\beta=240$. Doped channel *p*-type heterojunction field-effect transistors have transconductance $g_m=25$ mS/mm.

I. INTRODUCTION

III-V compound semiconductors have been traditionally grown on (100) substrates because of the wide range of growth conditions which results in good epitaxial layer quality and well-established device processing technology. However, fundamental material properties, growth mechanisms, surface kinetics, and impurity incorporation can be changed or improved by growing on crystal orientations other than (100).[1,2] From a technological point of view, the importance of high-index surfaces is reflected in various interesting material properties exhibited by the layers grown on non-(100) surfaces. For instance, the use of vicinal surfaces of (100) can dramatically improve the quality of epitaxial growth, such as in the case of GaAs on Si.[3] It has been predicted[2] and confirmed[4,5] that coherently strained (110) and (111) layers will possess a large built-in in-plane or out-of-plane piezoelectric field, which can lead to a new class of electronic and optoelectronic devices. Recent progress in epitaxial growth on patterned substrates indicates that such techniques will provide an additional degree of freedom in heterostructure band-gap engineering, which will find uses in device applications.[6,7] Patterned substrate epitaxy inevitably involves growth on high-index facets, which points to the necessity of understanding epitaxial growth on high-index surfaces in its own right.

High-index semiconductor surfaces present a unique opportunity to study impurity incorporation during epitaxial growth. In particular, silicon doping characteristics in III-V compounds have been known to depend on surface orientation. Although it is a common *n*-type dopant for (100) GaAs and AlGaAs, silicon shows strong amphoteric behavior in other orientations. Earlier work[8] has shown that Si acts as an acceptor in GaAs grown on $(n11)A$ substrates during molecular-beam epitaxy (MBE) when $n<3$, but behaves as a donor on $(n11)A$ for $n>5$ and $(n11)B$ for all values of n. There was also a report that Si doping type could be controlled during MBE by varying the growth temperature and V/III flux ratio.[7] Technologically, if the conductivity type of Si-doped GaAs or AlGaAs can be reproducibly chosen and controlled at high levels of doping ($>10^{18}$ cm^{-3}), it will be useful for many practical devices. The importance and usefulness of Si also arises from its small diffusion coefficient in most III-V compounds. We have, therefore, made a detailed investigation of the MBE growth and characteristics of Si-doped GaAs and AlGaAs on (311)*A* GaAs substrates and the device applications of these materials and heterostructures.

II. GROWTH PROCEDURE

GaAs substrates oriented within 0.5° of the (311) orientation were cut and polished with the *A* surface (Ga terminated) designated. Both Si-doped n^+ and Cr-doped semi-insulating substrates were used in this study. The substrates were prepared by standard solvent degreasing, followed by oxide etching in HCl:H_2O (1:1) and a rinse in de-ionized water. Etchants such as $5H_2SO_4$:$1H_2O_2$:$1H_2O$, which is commonly used for preparing (100) GaAs, is not used for (311) substrates, because it leads to surface roughness. In some cases, (100)-oriented wafers were mounted alongside (311)*A* wafers on standard mounting blocks for comparison.

Following standard thermal cleaning of the substrate under As_4 flux, a superlattice buffer layer consisting of 50 Å GaAs alternating with 50 Å AlGaAs was first grown. This superlattice was used to establish a better morphology during the subsequent growth. 0.2-μm-thick layers of GaAs were grown with different Si doping levels and/or

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under different growth conditions. Two series of epitaxial layers were grown. In the first the substrate temperature was held constant and the V/III flux ratio was varied; in the second the flux ratio was held constant and the growth temperature was varied. The substrate temperature was calibrated by observation of reflection high-energy electron diffraction (RHEED) patterns during InP and GaAs surface reconstructions. Molecular-beam equivalent pressure (BEP) was measured by a nude ion gauge at the same location as the substrate in growth position, and the beam flux ratio was calculated as[9]

$$R=\frac{J_{As_4}}{J_{Ga}}=\frac{P_{As_4}\eta_{Ga}}{P_{Ga}\eta_{As}}\left(\frac{T_{As_4}M_{Ga}}{T_{Ga}M_{As_4}}\right)^{1/2}, \quad (1)$$

where P is the measured BEP, η is the ionization efficiency relative to nitrogen, T is the cell temperature, and M is the mass. Experimentally, we assume the flux ratio to be unity when the surface reconstruction on (100) GaAs switches from As stabilized to Ga stabilized at a substrate temperature of 550 °C. The growth temperature was varied in the range 550–670 °C and the V/III flux ratio was varied between 1 and 5. The growth rate for GaAs is 0.7 μm/h. The growth was interupted between layers for changing the Si cell temperature, which was varied from 1150 to 1350 °C. In addition to the samples described above, thick reference samples were also grown on (100)- and (311)*A*-oriented substrates under various growth conditions for Hall measurement, secondary-ion mass spectrometry, and Raman spectroscopy measurements.

III. ELECTRICAL PROPERTIES

Carrier types and concentrations of the different films were measured by a capacitance-voltage (*C-V*) profiler using a solution of 0.1 M NaOH in de-ionized water as the electrolyte to etch the sample surface in successive steps under illumination. For the first group of Si-doped GaAs samples grown with fixed V/III ratio ~1.0 and different growth temperatures, the results are plotted in Fig. 1, together with data from the reference (100) samples. As reported earlier,[8] all Si-doped films with (311)*A* orientation exhibit *p*-type conductivity at all growth temperatures. Notice that as the growth temperature is increased from 550 to 670 °C, the *p*-type carrier concentrations in (311)*A* GaAs also increases to a maximum value of $p=2.1\times10^{19}$ cm^{-3}, which is higher than the *n*-type concentration achieved in (100) GaAs grown under identical conditions. This suggests that the Si doping efficiency in (311)*A* GaAs is greatly enhanced as the growth temperature increases.

The second group of Si-doped (311)*A* GaAs samples were grown at 650 °C under different As/Ga flux ratios. During growth, the Si cell temperature was held constant at 1350 °C. The BEP of As_4 increased from 25 up to 80, corresponding to a V/III flux ratio of 1.1 to 4.5. Two arsenic sources were employed for the higher As fluxes. Figure 2 shows the dependence of the measured carrier concentration on As/Ga flux ratios. At a specified growth temperature, Si doping in (311)*A* behaves quite differently from that observed in the first set of samples. The samples

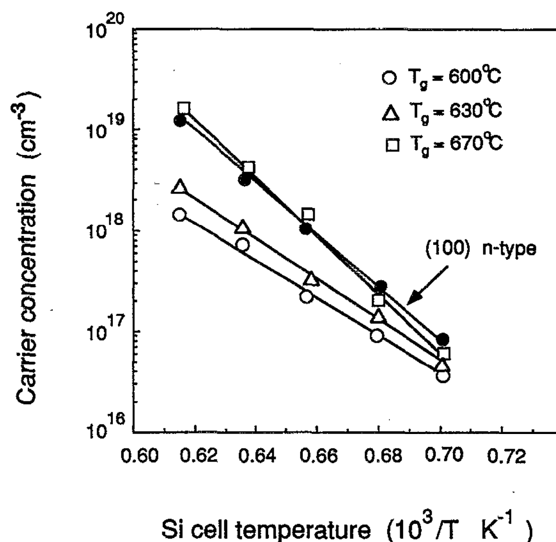


FIG. 1. Free-carrier concentration as a function of growth temperature. During growth the As/Ga flux ratio was kept constant and the Si cell temperature was varied. Note that the (311)*A* layers are *p* type while the (100) layers, which were grown during the same run, are *n* type.

exhibit *p*-type conductivity for low V/III ratio, but the degree of compensation increases as the V/III ratio increases. In fact, when the V/III ratio is ⩾3, Si behaves as a donor and the electron concentrations approach those measured in the (100) reference samples. This indicates that as the As flux is increased, more Si atoms are preferentially incorporated in Ga sites.

Si-doped $Al_{0.3}Ga_{0.7}As$ layers grown on a (311)*A* surface show similar behavior. The data obtained from measurements on Si-doped $Al_{0.3}Ga_{0.7}As$ samples are also plotted in Fig. 2. It is evident that both GaAs and AlGaAs show *p*-type conductivities at low V/IIII ratios (⩽1.5), but convert to *n* type when the V/III ratio exceeds 2.5. The (100) reference sample shows uniform *n*-type carrier concentration independent of the V/III ratios.

The amphoteric behavior of Si can be described by Teramoto's equation for the ratio of Si atoms incorporated

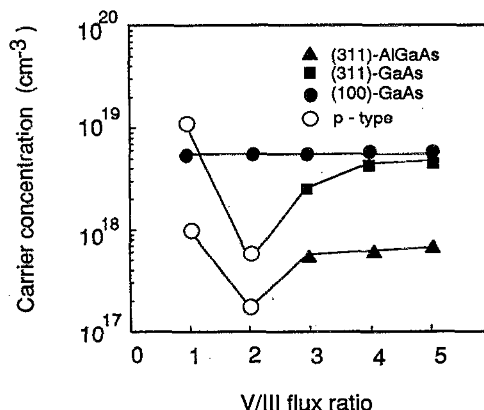


FIG. 2. Carrier type and concentration of Si-doped GaAs and AlGaAs grown on (311)*A* GaAs substrates as a function of V/III flux ratio.

on Ga sites to that on As sites (D_{Ga}/D_{As}) in GaAs,[10]

$$\ln \frac{[\mathrm{Si_{Ga}}]}{[\mathrm{Si_{As}}]} = \ln \frac{X_{As}}{X_{Ga}} + \frac{1.4\times 10^3}{T_s}. \quad (2)$$

For growth by MBE, Si_{Ga} (Si_{As}) is the number of silicon atoms substituting on the Ga (As) sublattice, X_{As} (X_{Ga}) is the number of As (Ga) vacancies on the growth surface, and T_s is the substrate temperature. It is clear that to enhance Si incorporation on As acceptor sites, low As/Ga flux ratios and high substrate temperatures are essential. From our experiments, it is seen that at growth temperatures above 660 °C and with a very small (~ 1) As/Ga flux ratio, Si predominantly incorporates at As sites. Free hole concentrations as high as 2.2×10^{19} cm^{-3} have been measured in GaAs. On the other hand, to achieve a high electron concentration with acceptable mobilities, the As/Ga flux ratio should be higher than 2.5, while maintaining the growth temperature below 500 °C.

To study the efficiency of p-type doping with Si, a 1.5-μm-thick film of Si-doped GaAs was grown on Cr-doped semi-insulating (311)A GaAs substrate at a temperature of 660 °C with $As_4/Ga \sim 1$. Hall measurements made on this film give $p=4.0\times 10^{18}$ cm^{-3} and $\mu = 100$ cm^2/(V s) at 300 K. The Si concentration in the film determined by secondary-ion mass spectrometry (SIMS) is [Si]$=4.2\times 10^{18}$ cm^{-3}. If we assume that all the Si atoms are electrically active, then the Si p-type doping efficiency is approximately $[p]/[\mathrm{Si}] > 95\%$, which clearly indicates that under appropriate growth conditions, Si predominantly incorporates into the As site.

IV. RAMAN SPECTROSCOPY

To effectively correlate transport properties in Si-doped GaAs films with MBE growth conditions, it is important to characterize the distribution of Si atoms among the As and Ga sublattice sites. Raman and infrared (IR) spectroscopy, probing local vibrational modes (LVM) in crystals,[11] are the most widely used techniques for this purpose. Because of various reasons, the former technique exhibits many advantages over IR spectroscopy in the case of thin-film structures. To confirm the explanation given for the Si doping mechanism in the previous section, we have performed and analyzed Raman spectra obtained from heavily Si-doped GaAs grown on (311)A by MBE under different conditions.

Two Si-doped GaAs samples (1 μm thick) were grown on n-type (311)A GaAs substrates. Sample A was grown at a substrate temperature of 670 °C with As/Ga flux ratio ~ 1, while the substrate temperature for sample B was 450 °C and the flux ratio was As/Ga >3.5. During each growth the Si cell temperature was kept constant at 1350 °C. Capacitance-voltage measurements were made on the samples to determine the conductivity types and free-carrier concentrations. Sample A exhibits p-type conductivity with $p=2.1\times 10^{19}$ cm^{-3}, while sample B is n type with $n=1.2\times 10^{19}$ cm^{-3}.

Raman data were obtained with a Dilor XY spectrometer. Spectra were recorded at room temperature in the

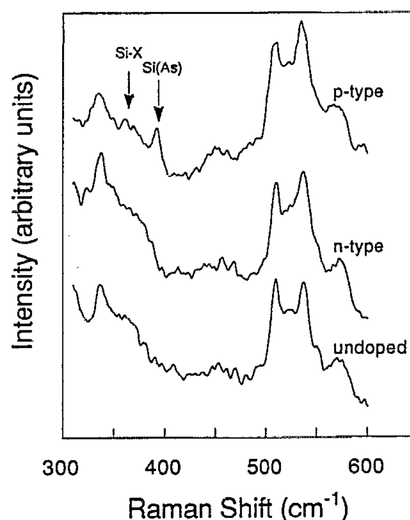


FIG. 3. Raman spectra of the p-type (top), n-type (middle), and undoped (bottom) (311) samples. The local vibrational modes of the p-type sample are labelled by arrows. The scattering configuration is $z(y,y)\bar{z}$ and the excitation wavelength is 4965 Å.

backscattering configuration with the incident and scattering light polarized either along the $x=(0\bar{1}1)$ or $y=(\bar{2}33)$ directions. The 4765 and 4965 Å lines of an Ar^+ laser were used as the excitation source. The penetration depth for such wavelengths is considerably smaller than the thicknesses of epitaxial layers. In (311) backscattering, both the LO (longitudinal optic) and TO (transverse optic) modes are allowed. In heavily doped GaAs, however, the LO phonon couples to electron (hole) plasmon giving rise to two coupled modes, L^+ and L^-. The Raman spectrum of the n-type film shows large energy shifts with a L^+ plasmon-like mode peak at ~ 1080 cm^{-1}. Its frequency corresponds to a free-electron concentration of $(1.2\pm 0.2)\times 10^{19}$ cm^{-3}, in very good agreement with the results of C-V measurements.

The low-frequency region of the spectra of the p-type (sample A), n-type (sample B), and undoped (sample C) samples are shown in Fig. 3. The weak peak at ~ 340 cm^{-1} and the structures between 450 and 600 cm^{-1} in all samples are due to second-order phonon scattering (small differences among the spectra are due to slight misalignments in the scattering geometry). Other than the intrinsic modes, the p-type sample shows additional features at 365 and 394 cm^{-1}, which are ascribed to Si-X and Si_{As} LVM, respectively. Si_{As} denotes the local vibration mode associated with a Si atom replacing As while Si-X is a controversial defect complex.[12] Murray *et al.*[12] found that the Si-X defect can be best explained as a nearest-neighbor double or triple acceptor Si_{As}-V_{Ga} pair, where V_{Ga} denotes a vacant Ga sublattice site. Of course, Si_{As} is a single acceptor. The fact that the n-type sample does not show features associated with acceptor sites indicates that levels of compensation are low for the specified films. The sample, however, does not show evidence of Si_{Ga} either. This is because such a line can only be observed in the immediate vicinity of the E_1 resonance at ~ 3 eV.[11]

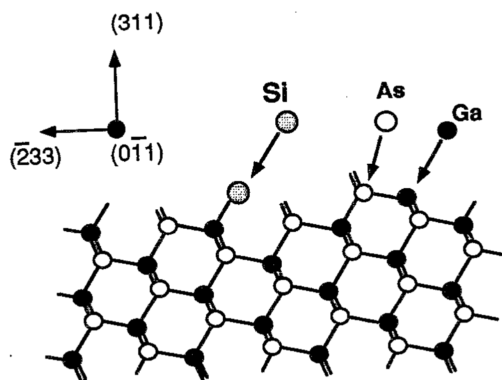


FIG. 4. Schematic of the atomic arrangement at an ideal (311)*A* GaAs surface.

The Si doping characteristics on the (311)*A* surface, as observed by electrical measurements and Raman spectroscopy, need to be discussed. The first important observation is that on the (311)*A* surface there is one single dangling-bond site and one double dangling-bond site in each surface unit cell (Fig. 4). Thus the Si doping properties can be expected to be similar to that on the (211)*A* surface,[13] which has twice as many single dangling-bond sites as double dangling-bond sites. On the (311)*A* surface, Si doping atoms on As acceptor sites can bond to surface Ga atoms by single bonds, or Si atoms on Ga donor sites can bond to surface As atoms by double bonds. The final incorporation of Si on donor or acceptor sites will depend not only on the relative strength of Si—As or Si—Ga bonds, but also on the competition the Si atom will encounter for a substitutional site from incoming As and Ga atoms. By anology with the situation on the (211)*A* surface,[13] it appears that, at low As-fluxes, molecular As_4 is a much less effective competitor of Si at single-bond acceptor sites. This is likely because the molecular As_4 must be broken up, the energy for which is less readily provided by forming only a single bond per atom as opposed to two bonds. These circumstances, together with the competition from plentiful Ga atoms at the double-bond donor sites, forming two strong Ga—As bonds, should effectively shift Si atoms to the acceptor sites on the As sublattice (as seen in sample A), even though the Si atom itself would bind more strongly on the donor sites. With increasing As/Ga flux ratios or decreasing growth temperatures, which results in a higher As sticking coefficient on GaAs surface, the balance should shift back in the direction of the energetically preferred Ga sites (as seen in sample B), leading to *n*-type doping.

V. DEVICE APPLICATIONS

A. Heterojunction bipolar transistors

Beryllium (Be) is frequently used as the *p*-type dopant during MBE of GaAs and other III-V compounds due to its favorable vapor pressure. It is therefore the dopant species of choice during the growth of the *p*-type base region in *n-p-n* heterojunction bipolar transistors (HBT). Heavy Be doping, however, leads to the increase of surface segregation[13] and diffusion[14] during growth and subsequently during device processing and operation. Growth techniques such as high-group-V overpressure during growth,[15,16] low substrate temperature,[16,17] and the addition of a small amount of In to the Be-doped layers[18] have met with some success. The use of other dopant species such as C (Ref. 19) or use of different substrate orientations[20] are also being investigated.

In the light of the results obtained from our Si-doping experiments with (311)*A* GaAs and AlGaAs, we have investigated the suitability of such doping in the growth of GaAs/AlGaAs HBTs by MBE. The objective is to utilize all-Si doping during the growth of the entire structure. The HBT layer structures and growth conditions are summarized in Table I. Two arsenic sources were used for rapid change of the V/III ratios during growth.

The carrier concentrations and doping type in the HBT structure described in Table I were measured by the *C-V* profiler and the results are shown in Fig. 5. It is important to note that a *p*-type concentration as high as 2.2×10^{19} cm^{-3} is achieved with Si doping in the GaAs base region under the specified growth conditions. This high level of doping is required for good high-frequency performance of the devices. The undoped GaAs collector region has a *p*-type concentration of 5×10^{16} cm^{-3}, which is typical on a (311)*A* GaAs surface.[8]

Transistors were fabricated with (5×10) μm^2 emitter areas. The active layers were accessed for contacting by wet etching. Electron-beam-evaporated Pt/Zn/Pt/Au was used for the base contact and GeAu/Ni/Ti/Au for the emitter and collector contacts. Device isolation was provided by mesa etching and surface passivation and crossover isolation were achieved by a plasma-enhanced

TABLE I. Layer sequence of the HBT device.

Layer	Composition	Thickness (μm)	Doping (cm^{-3})	Substrate temp. (°C)	V:III ratio	Remarks
I	GaAs	0.5	5×10^{18}, Si	450	4	collector contact
II	GaAs	0.3	undoped	630	1	collector
III	GaAs	0.12	2.2×10^{19}, Si	660	1	base
IV	$Al_xGa_{1-x}As$	0.03	5×10^{17}, Si	450	4	grading
V	$Al_{0.2}Ga_{0.8}As$	0.1	5×10^{17}, Si	450	4	emitter
VI	$Al_xGa_{1-x}As$	0.03	5×10^{17}, Si	450	4	grading
VII	$In_yGa_{1-y}As$	0.2	5×10^{18}, Si	450	4	graded emitter contact

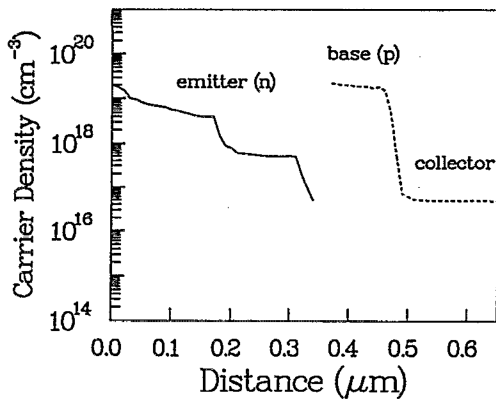
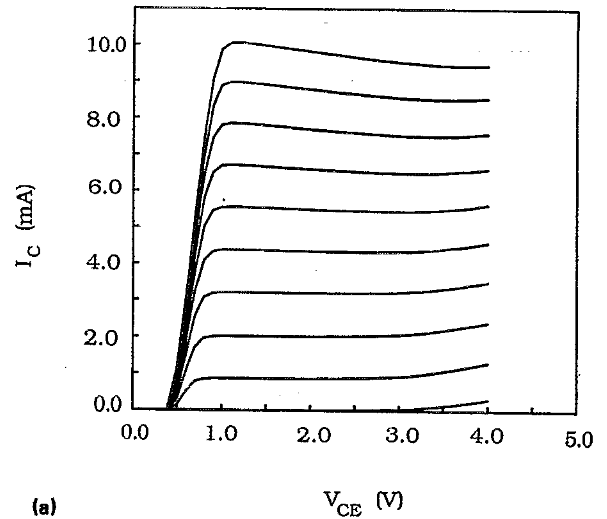


FIG. 5. Measured *C-V* profile of the carrier concentration and type of the Si-doped HBT structure.

chemical-vapor-deposited (PECVD) silicon nitride film. Figure 6(a) shows the typical common-emitter characteristics of a HBT with (5×10) μm^2 emitter size. The transistor has a current gain $h_{fe}=140$. The highest dc common-emitter current gain of 230 was measured in devices with the same structure but with a base doping of $p=4\times10^{18}$ cm^{-3}. This gain is uniform in the collector current density range of $(1\text{–}10)\times10^3$ A/cm^2. The emitter-base junction exhibits excellent rectifying current-voltage characteristics with sharp forward turn on and very small reverse leakage current ($\sim$6 nA at -5 V). The measured Gummel plot is shown in Fig. 6(b). The emitter-base and collector-base junctions are of very high quality with a collector current ideality factor of 1.04 and the base current ideality factor of 1.46.



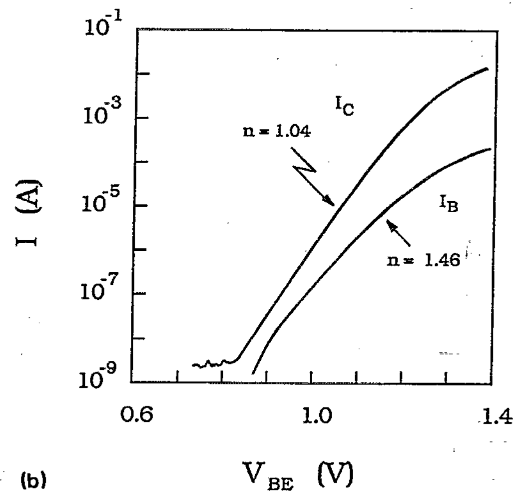


FIG. 6. (a) Common emitter characteristics of the HBT device [emitter area: (5×10) μm^2, $I_B=10$ μA/step], and (b) typical Gummel plot of the HBT.

B. Complementary heterostructure field-effect transistors

The unique orientation-dependent amphoteric behavior of Si in GaAs should find applications in other electronic devices as well. We have also realized *p*-type $Al_{0.2}Ga_{0.8}As/GaAs$ heterostructure field-effect transistors (HFET) over etched (311)*A* facets on (100)-oriented GaAs substrates by Si doping during MBE growth. Simultaneously, *n*-type HFETs were grown and fabricated on the (100) plane with the same structures and with the same level of Si doping, leading the way to the realization of complementary circuits by one-step epitaxial growth.

The substrates used for this experiment were undoped semi-insulating (100) GaAs. Patterning of ridges and grooves was done by conventional photolithography and wet-chemical etching. A solution of $NH_4OH:H_2O_2:H_2O$ (5:1:50) was used to etch angled facets approximately 5 μm deep in the $[0\bar{1}1]$ direction, yielding (311)*A* sidewalls.[7] The (311)*A* planes are preferred over the (111)*A* or (211)*A* planes since they make a smaller angle ($\sim$28°) with the (100) plane, which greatly facilitates planar processing during device fabrication. Immediately prior to loading into the MBE system, the substrates were cleaned in organic solvents, followed by a 1 min free etch in $NH_4OH:H_2O_2:H_2O$ (10:1:100) and a final rinse in deionized water.

The heterostructure of the Si-doped channel FET is shown schematically in Fig. 7. The entire structure was grown at a rate of 0.7 μm/h (for GaAs) at a temperature of 630 °C. After growing the 3000 Å $Al_{0.2}Ga_{0.8}As$ buffer layer with a V/III flux ratio of 1.5, growth was interrupted to lower the arsenic source temperature to adjust the V/III

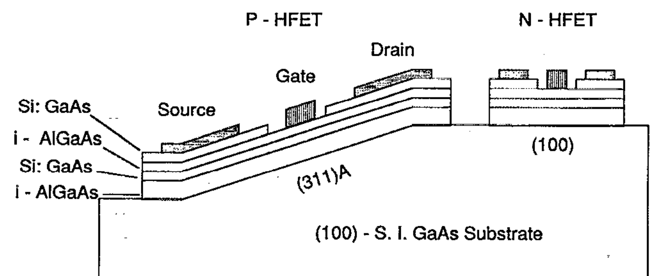
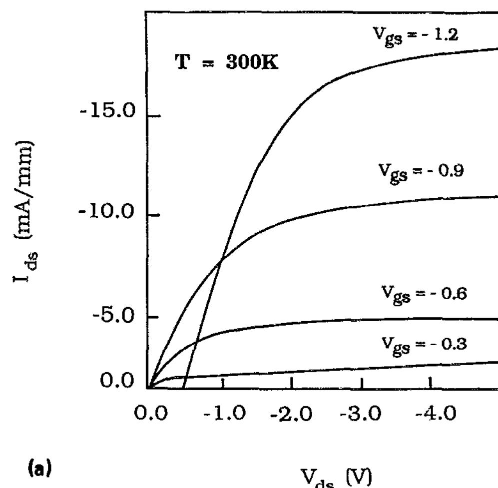


FIG. 7. Schematic of the AlGaAs/GaAs HFET structure on the etched (311)*A* facet.

flux ratio to 1 for the following 300-Å-thick Si-doped GaAs channel [Si doping level is approximately 7×10^{17} cm^{-3} as calibrated for the (100) plane]. The objective here is to create conditions on the $(311)A$ surfaces that are favorable for Si incorporation on As sites and thereby produce p-type doping. Remember that on this surface the As:Ga site density is in the ratio of 1:1. The relatively high substrate temperature and lower As flux help to create enough As vacancies for Si incorporation. After growth of the channel layer, the previous V/III ratio is restored and 300 Å of undoped $Al_{0.2}Ga_{0.8}As$ and 100 Å of Si-doped GaAs, with the same doping level as in the channel, were consecutively grown. On the control (100)-oriented GaAs substrate, the same level of Si doping and same growth conditions resulted in a channel sheet electron concentration of $n_s=2.0\times10^{12}$ cm^{-2} and a mobility of 1700 cm^2/V s at 300 K.

To fabricate the p-HFET on the $(311)A$ facets, device isolation was first done by wet-chemical mesa etching in H_3PO_4:H_2O_2:H_2O. Then the p-type drain and source ohmic contacts were formed by evaporation of Au/Zn/Ni/Au and lift-off techniques, followed by hot-plate alloying at 400 °C for 20 s. The source-drain separation is 5 μm and both approximately 10 μm long. Finally a 1.1×50 μm Ti/Au gate was formed without recessing. The n-type HFET on the (100) plane was processed separately using the same mask set.

Measurement of dc electrical characteristics of the p-HFET was done at 300 K. Figure 8(a) shows typical drain current versus drain-to-source voltage characteristics. Measured transfer characteristics (drain satuation current versus gate voltage and transconductance versus gate voltage) at room temperature is shown in Fig. 8(b). Maximum values of the transconductance are 23 mS/mm at 300 K. The low drain current and the relatively small temperature dependence of the transconductance may suggest that the Si doping on the $(311)A$ plane is partially compensated. The n-HFET fabricated on the (100) plane with a 1.1×50 μm^2 gate yields $g_m=250$ mS/mm at 300 K. For digital applications, such as complementary circuits, this is tolarable since the major concern is to make the transconductance of the two types of devices comparable. With optimized growth conditions, the compensation problem could be minimized. We also fabricated FET devices on the planar $(311)A$ substrate. A transconductance value of 26 mS/mm has been measured at 300 K with a 1.1×50 μm^2 gate, which is comparable to that obtained with the devices made on etched $(311)A$ facets.



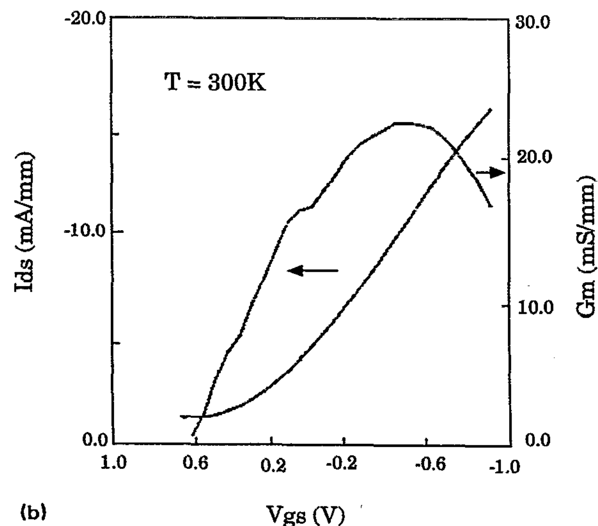


FIG. 8. (a) Room-temperature source-drain current-voltage characteristics of a p-HFET made on the etched $(311)A$ plane with gate length of 1 μm, and (b) transconductance and drain current of a p-HFET on $(311)A$ as a function of gate bias at room temperature.

VI. CONCLUSIONS

We have studied the MBE growth and properties of Si-doped GaAs and AlGaAs on $(311)A$ GaAs substrates. It is seen that Si is a truely amphoteric dopant in GaAs and AlGaAs with $(311)A$ orientation. The doping conductivity of Si in GaAs and AlGaAs can be controlled in a reproducible manner by varying MBE growth conditions. We find that at high growth temperatures ($\geqslant$660 °C) and low V/III flux ratios (~1), Si atoms predominantly incorporate on As sublattice sites and behave as uncompensated acceptors. High p-type doping of 2.1×10^{19} cm^{-3} has been obtained with Si doping in GaAs. On the other hand, a low growth temperature ($\leqslant$500 °C) and a high V/III flux ratio ($\geqslant$2.5) are necessary to make Si occupy Ga sublattice sites and act as a donor. Results obtained from Raman spectroscopy on these samples confirm these observations.

The controllable amphoteric doping property of Si in GaAs has been applied to the MBE growth of GaAs/AlGaAs HBTs with all-Si doping. The device shows excellent rectifying characteristics in both emitter and collector junctions, with ideal factors of 1.46 and 1.05 for emitter and collector, respectively. Typical transistors with emitter size of 5 μm^2 exhibit common current gain of 230. This gain is uniform in a large range of collector current density. We have also demonstrated complementary heterostructure FETs by one-step MBE growth on $(311)A$ GaAs facets created by chemical etching of (100) GaAs. The Si-doped p-type HFETs with 1 μm gate length made on the

(311)A facets have g_m=24 mS/mm, while the n-type HFETs with the same Si doping level show g_m=250 mS/mm. The technique suggests that, in principle, complementary circuits could be integrated on the same wafer by such one-step epitaxial growth.

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[1] T. Hayakawa, M. Kondo, T. Suyama, K. Takahashi, S. Yamamoto, and T. Hijikata, Jpn. J. Appl. Phys. **26**, L302 (1987).

[2] D. L. Smith, Solid State Commun. **57**, 919 (1986).

[3] R. Fischer, D. Neuwman, H. Zabel, H. Morkoc, C. Choi, and N. Otsuka, Appl. Phys. Lett. **48**, 1223 (1986).

[4] E. A. Caridi, T. Y. Chang, K. W. Gossen, and L. F. Eastman, Appl. Phys. Lett. **56**, 659 (1990).

[5] K. W. Gossen, E. A. Caridi, T. Y. Chang, J. B. Stark, and D. A. B. Miller, Appl. Phys. Lett. **56**, 715 (1990).

[6] E. Kapon, M. C. Tamargo, and D. M. Hwang, Appl. Phys. Lett. **50**, 347 (1987).

[7] H. P. Meier, R. F. Broom, P. W. Epperlein, E. van Gieson, C. Harder, H. Jaeckel, W. Walter, and D. J. Webb, J. Vac. Sci. Technol. B **6**, 692 (1988).

[8] W. I. Wang, E. E. Mendez, T. S. Kuan, and L. Esaki, Appl. Phys. Lett. **47**, 826 (1985).

[9] C. E. C. Wood, D. Desimone, K. Singer, and G. W. Wicks, J. Appl. Phys. **53**, 4230 (1982).

[10] I. Teramoto, J. Phys. Chem. Solids **33**, 2089 (1972).

[11] M. Ramsteiner, J. Wagner, H. Ennen, and M. Maier, Phys. Rev. B **38**, 10 669 (1988).

[12] R. Murray, R. C. Newman, M. J. L. Songster, R. B. Beall, J. J. Hanis, P. J. Wright, J. Wagner, and M. Ramsteiner, J. Appl. Phys. **66**, 2589 (1989).

[13] S. Subbanna, H. Kroemer, and J. Merz, J. Appl. Phys. **59**, 488 (1986).

[14] D. L. Miller and P. M. Asbeck, J. Appl. Phys. **57**, 1816 (1985).

[15] Y. C. Pao, T. Hierl, and T. Cooper, J. Appl. Phys. **60**, 201 (1986).

[16] Y. C. Pao, J. Franklin, and J. S. Harris, Jr., J. Cryst. Growth **95**, 301 (1989).

[17] D. C. Strait, A. K. Oki, D. K. Umemoto, J. R. Velebir, K. S. Stolt, F. M. Yamada, Y. S. Saito, M. F. Hafizi, S. Bui, and L. T. Tran, IEEE Electron Device Lett. **EDL-12**, 471 (1991).

[18] J. Livin, C. D. Chevallier, F. Alexandre, G. Leroux, J. Dangla, and D. Ankri, IEEE Electron Device Lett. **EDL-7**, 129 (1986).

[19] R. J. Malik, R. N. Nottenburg, E. F. Schubert, J. F. Walker, and R. W. Ryan, Appl. Phys. Lett. **53**, 2661 (1988).

[20] T. Tomioka, T. Fujii, H. Ishikawa, S. Sasa, A. Endoh, Y. Bamba, K. Ishii, and Y. Kataoka, Jpn. J. Appl. Phys. **29**, L716 (1990).