Improved quality GaN by growth on compliant silicon-on-insulator substrates using metalorganic chemical vapor deposition

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The use of compliant silicon-on-insulator (SOI) substrates instead of Si substrates is shown to improve the quality of epitaxial GaN layers by releasing the strain and absorbing the generated threading dislocations in the thin Si overlay of the SOI substrate. GaN layers have been grown on SOI substrates by low-pressure metalorganic chemical vapor deposition and various growth conditions and compared with GaN layers grown on Si substrates. Crystal uniformity, surface morphology, and number of threading dislocations of GaN layers grown on SOI substrates are improved compared to layers grown directly on Si substrates as evidenced by x-ray diffraction spectroscopy (XRD) and transmission electron microscopy. Full width at half maximum XRD values improved from 672 to 378 arcsec by growth on SOI instead of Si substrates. The GaN layers grown directly on Si substrates are highly resistive while all as-grown GaN layers on SOI substrates are unintentionally *n* type. For a 1–2 μm thick GaN layer grown on SOI, the electron mobility is typically in the order of 10^2 cm^2/V s with a background carrier concentration in the range of $1.5–5.0\times10^{17}$ cm^{-3}. © *1998 American Institute of Physics.* [S0021-8979(98)05607-2]

INTRODUCTION

GaN and related nitrides are promising materials for applications in UV/blue light emitters[1] and high-power, high-temperature electronic devices.[2] Although extensive efforts are made to achieve high-quality GaN materials,[3–6] the quality of epitaxially grown GaN layers is hindered by large lattice mismatch and a large difference in thermal expansion coefficients between GaN and the commonly used substrate sapphire.[7,8] The large lattice mismatch leads to high interfacial strain between the epilayer and the substrate, and, as a result, induces misfit and threading dislocations. Consequently, the structural and electrical properties of GaN layers cannot be fully optimized, and devices built on such layers cannot take full advantage of the intrinsic properties of III nitrides.

New, different epitaxial growth approaches are, therefore, desirable and the technique of growth on compliant silicon-on-insulator (SOI) substrates discussed in this paper offers such an alternative. Theoretical work[9,10] shows the possibility to grow thicker layers without degradation on thin compliant layers through stress absorption in the compliant substrate. Thick, lattice-mismatched InGaAs epitaxial layers have been grown on compliant GaAs substrates via molecular beam epitaxy (MBE).[11,12] Most recently, thick InGaP layers have been grown by metalorganic chemical vapor deposition (MOCVD) on twist-wafer-bonded GaAs compliant substrates without generation of threading dislocations.[13] Various types of ''soft'' buffers can be envisaged, but techniques which offer the potential of large wafer-size compatibility are obviously most attractive since they are best suited for device and circuit applications. The SOI approach investigated in this work offers exactly this possibility for GaN.[14] Recently, SiGe was grown by MBE on SOI substrates,[15] and GaN was grown, also by MBE, on a SiC–SOI heterostructure,[16,17] exploiting the advantages of this compliant substrate. The work presented in this paper reports very encouraging results for growth of GaN on SOI substrates without previous formation of SiC. Compared to the mismatched-growth using twist-wafer-bonded GaAs compliant substrates,[13] which requires extensive pregrowth processing and which has been demonstrated so far only on relatively small wafer pieces, the approach using SOI substrates would allow the direct use of commercially available, high-quality and large-size wafers which drastically simplifies the process. Moreover, the availability of high-quality SOI wafers should result in an overall improved yield. Also, if GaAs is to be used for compliant twist-wafer-bonded substrates, this material system would not withstand the typically required high growth temperatures of $>1000\,^{\circ}$C in MOCVD growth of GaN, which has been proven to date the best growth method for device quality GaN layers.[1,2] In addition, SOI wafers could be a more commercially viable technology due to their smaller cost than GaAs wafers of the same size.

The thin silicon overlay acts as the compliant buffer and SOI substrates enable large wafer-size processing. Epitaxy of GaN on SOI substrates offers the very attractive feature of the production of large-size GaN epitaxial wafers, as necessary for nitride-based device and circuit requirements. Moreover, incorporation of GaN devices into silicon-based integrated circuits could be envisaged, in order to perform more complex functions. By growth on SOI, the difficulty of growing GaN directly on silicon, which rises by the large differences in lattice constant, crystal structure, and thermal expansion coefficient, can be avoided.

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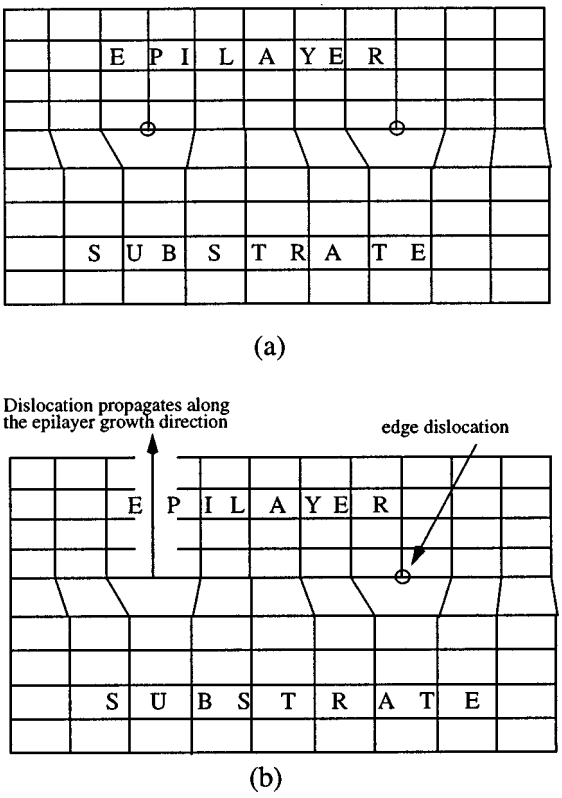

FIG. 1. (a) Schematic of ideal lattice-mismatched growth where the entire strain is relieved as edge dislocations; and (b) nonideal (realistic) case where the strain is relieved as edge and threading dislocations.

BASIC FEATURES OF THE COMPLIANT GROWTH APPROACH

Figure 1 shows a conceptual picture of the differences between ideal growth on mismatched substrates and the actual result obtained in practice with conventional growth approaches. Lattice-mismatched growth is in practice accompanied by strain relief through dislocations. These should ideally be edge dislocations located at the epilayer–substrate interface as shown in Fig. 1(a). If this is indeed the case, the layer grows as a free-standing unstrained layer, i.e., as the growth proceeds, the dislocations are confined in the first few monolayers and the layer on top has the lattice constant of ''bulk'' material resulting, therefore, in excellent epilayer quality. This ideal condition can only be realized if two conditions are satisfied: (i) the growth starts and continues completely layer by layer so that at any point of substrate coverage there is only a single island 1 ML high on the substrate; and (ii) the growth rate is slow enough that the grown layer is able to reach the minimum energy state. Unfortunately, those conditions are extremely difficult to implement in regular growth.

As Fig. 1(b) shows, in real growth several islands start nucleating simultaneously. Moreover, the large lattice mismatch produces strain energy accumulation at the site of edge dislocations and unstabilizes the chemical bonds resulting in atoms that cannot be stacked perfectly. When the edges of these islands eventually reach each other, there is a high probability that a threading dislocation instead of an edge dislocation develops. These dislocations may propagate through the epilayer, eventually degrading device performance on these layers.

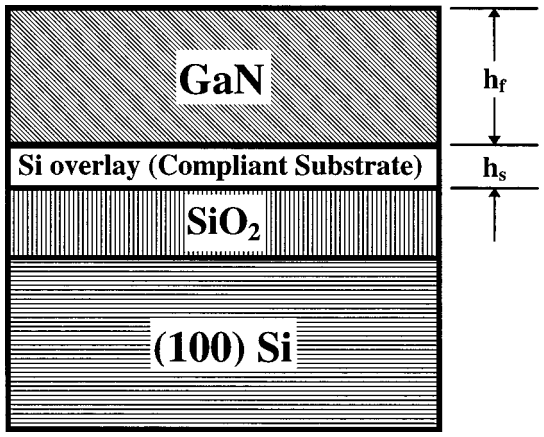

FIG. 2. Schematic diagram of the SOI substrate/GaN layer structure.

To overcome the problem outlined above we have explored the possibility of using the thin Si layer, which is bonded to a much thicker supporting Si substrate through a thin SiO_2 layer, thus forming the SOI structure, as the compliant substrate for GaN epitaxy (Fig. 2). The compliant substrate principle predicts that the strain in a lattice-mismatched epilayer can be reduced via partial accommodation of the total strain in a thin compliant overlay as contrasted with the rigidity of a thick Si or sapphire substrate. The biaxial elastic strains in substrate ϵ_s and epilayer ϵ_f prior to the formation of dislocations are partitioned as[9,10]

$$\epsilon_s = -\epsilon_m \frac{h_f}{h_s + h_f}, \quad \epsilon_f = \epsilon_m \frac{h_s}{h_s + h_f}, \tag{1}$$

where $\epsilon_m = (a_s - a_f)/a_f$ is the total strain due to lattice mismatch, h_s is the thickness of the substrate, and h_f is the thickness of the epitaxial layer. a_s and a_f denote the lattice constants of the substrate and the epilayer in the plane of interface, respectively.

In conventional epitaxial growth, the substrate is much thicker than the epilayer, thus, virtually all the strain resides in the grown layer. For example, if a 1 μm thick epilayer is grown on a 200 μm thick substrate, 99.5% of the total lattice-mismatch caused strain is distributed into the epilayer. In our approach with a compliant substrate, the substrate is much thinner than the epilayer and, thus, accommodates most of the total strain. If a film of the same thickness is grown on a much thinner substrate in the order of a few 100 Å or less, only a few percent of the strain is contained in the epitaxial which will, consequently, contain much fewer dislocations and will in general be of better quality.

Epitaxy on a compliant substrate can, consequently, reduce the threading dislocations when utilizing substrates that are largely lattice-mismatched with the epilayer. Figure 3 shows the physical implementation of the above-outlined principle when using a compliant buffer for growth of the epilayer. A very thin buffer layer is necessary so that the atom bonds are not as strong as in a bulk crystal. The bond energies in a compliant buffer at growth temperature are comparable to k_BT (e.g., $\leqslant 10k_BT$; k_B: Boltzmann con-

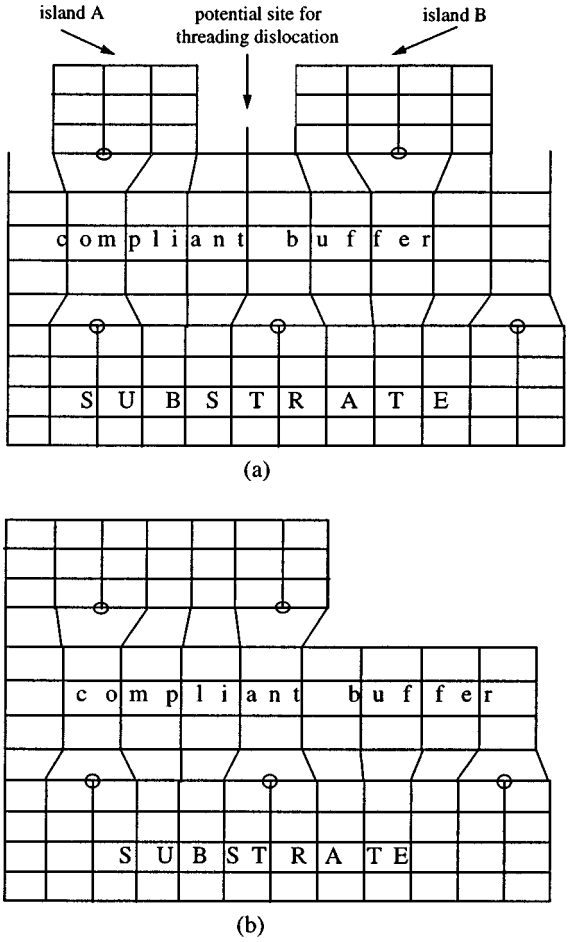

FIG. 3. (a) Schematic of two merging islands, A and B. If the islands remain in the positions shown, there is a high probably that a threading dislocation is formed; and (b) ideal configuration after island migration on the buffer creating only edge dislocations.

stant, T: temperature) so that the atoms and clusters of atoms may be able to move on the buffer. Figure 3(a) shows two islands, A and B, of the epilayer which are about to merge. At this point, there is a high probability that merging will produce threading dislocations. However, if the islands were able to ''float'' on the buffer to produce a registry as shown in Fig. 3(b), mostly edge dislocations will be produced. In conventional growth, this is difficult to achieve due to the very high energy barrier for this island migration process. However, a compliant buffer may become ''soft'' and allow the migration of the epilayer islands. The island merge allows reduction of the number of threading dislocations, and edge dislocations may be confined at the interface. The relatively high atomic migration rates in the compliant buffer region will allow the structure to come closer to the global minimum energy state where the dislocation network is periodic and entirely contained in the buffer. While the picture discussed above is not rigorous, it provides a physical description useful in selecting the growth parameters and choosing the compliant buffer.

GROWTH APPROACH AND PHYSICAL ANALYSIS OF GaN ON COMPLIANT SOI SUBSTRATES

The SOI substrates used in this work were fabricated by SOITEC via SIMOX (separation by implanted oxygen)

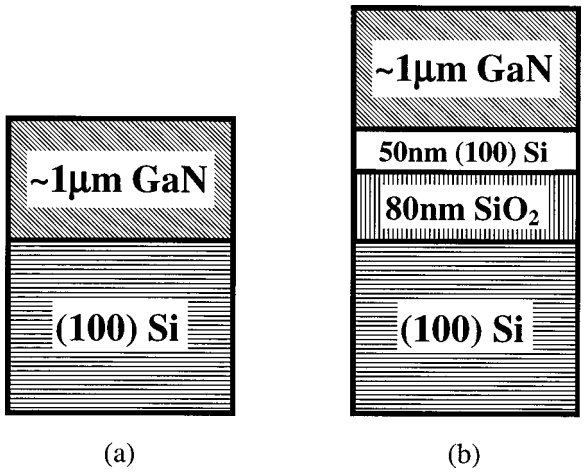

FIG. 4. Schematic cross section of grown structures to investigate growth on compliant substrates: (a) GaN growth on Si substrates, and (b) GaN growth on SOI substrates.

technology.[18] The thicknesses of the silicon overlay and SiO_2 buried layer were 52.8 ± 1.1 and 81.2 ± 4.4 nm, respectively, and the Si substrate was (100) oriented. GaN layers were grown on the SOI substrates in a modified EMCORE GS-3200 low-pressure (60 Torr) MOCVD system, using H_2 as the carrier gas (3000 sccm). Trimethylgallium (TMGa) and ammonia (NH_3) were used as Ga and N sources, using TMGa and NH_3 flow rates of 36 μmol/min and 2000 sccm, respectively, and the V/III ratio was 2500. Before loading into the reactor, the substrates were degreased in hot solvents. The substrates were then placed on a SiC-coated graphite susceptor, loaded into the horizontal quartz reactor, and annealed in an ambient of H_2 and NH_3 at a temperature of 1000–1050 °C for about 15 min. By identifying the N 1s peak, x-ray photoelectron spectroscopy (XPS) of the surface reveals, as explained below, that nitrogen was incorporated into the substrate surface during this process.

Typical structures investigated in this study are shown in Fig. 4. They include GaN layers grown on SOI as well as silicon (100) substrates for verifying the advantages gained by the compliant approach; the silicon wafers were subjected to the same surface preparation and have been placed side by side with SOI substrates in the reactor. After thermal annealing and cooling down of the reactor to 500 °C, the structures, consisting of a thin, ~250 Å thick GaN buffer followed by a ''bulk'' GaN layer, were grown. The latter was grown at high temperatures from 1 to 3 h depending on the desired layer thickness (0.7–2.0 μm). Growth of layers with thicknesses in this range on top of a compliant substrate allows fewer dislocations than growth on conventional substrates, even if there exists a large lattice mismatch. For example, for a 1 μm thick epilayer grown on a 500 Å thick substrate, only 5% of the strain reside in the epilayer. ''Bulk'' growth temperature has been varied between 700 and 1000 °C to evaluate its impact on the properties of the resulting GaN layers.

Secondary ion mass spectroscopy (SIMS) and XPS analysis were performed to understand the influence that the SOI substrate may have on the properties of the GaN layers. Figure 5 shows the SIMS analysis of GaN grown on SOI,

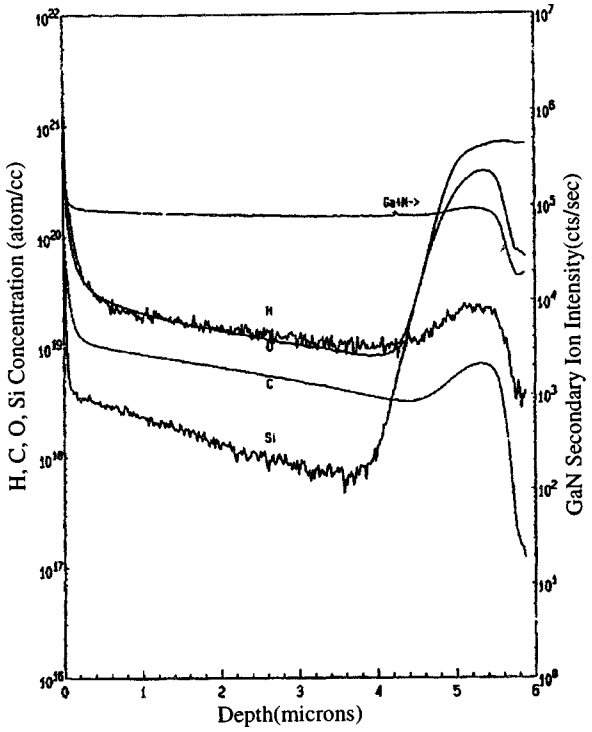

FIG. 5. SIMS analysis of a GaN layer grown on a SOI substrate. The profile of Ga and N is plotted in relative units (counts/second) relative to the right *y* axis, and the impurity concentrations are plotted in absolute values (atoms/cm^3) to the left *y* axis of the plot.

which reveals the presence of at least O, H, Si, and C impurities in the epilayer. Considering the structure of the SOI substrate, the profiles of Si and O are understandable. The concentration of both elements rises sharply with the probing depth reaching the substrate. The C concentration in the GaN epilayer is in the order of 10^{18}–10^{19} cm^{-3}. The source of C incorporated in the GaN epilayer is not clear at this point. It may come from the organometallic TMGa source, the graphite susceptor, or its SiC coating, both of which may release C atoms into the chamber during high-temperature growth.

The existence of C, O, and Si contaminants in the epitaxial layer can also be confirmed by XPS using a PHI 5400 ESCA system with an Al $K\alpha$ x-ray source ($E = 1486.6$ eV). A spectrum of a GaN epilayer grown on a SOI substrate is shown in Fig. 6. The XPS peaks at 19, 392, and 420 eV are identified as the Ga $3d$, $L_2M_{45}M_{45}$, and $L_3M_{45}M_{45}$ bonding of Ga, respectively. The contaminants C, O, and Si are identified with their signature peaks at 285 eV (C $1s$), 531 eV (O $1s$), 153 eV (Si $2P$), and 103 eV (Si $2S$).

Single-crystal x-ray diffraction (XRD) using the Cu $K\alpha$ double line was employed to investigate the crystal quality of the epitaxial GaN layers grown on SOI or Si substrates. The out-of-plane (θ–2θ) scans were carried out in reflection geometry with the scattering vector perpendicular to the plane of the layer. The spectra were obtained by a RIGAKU ''Rotaflex RU-200B'' system. The divergence slit and scatter slit were both 0.5°. The widths of the receiving slit and the monochromator receiving slit were 0.15 and 0.45 mm, respectively.

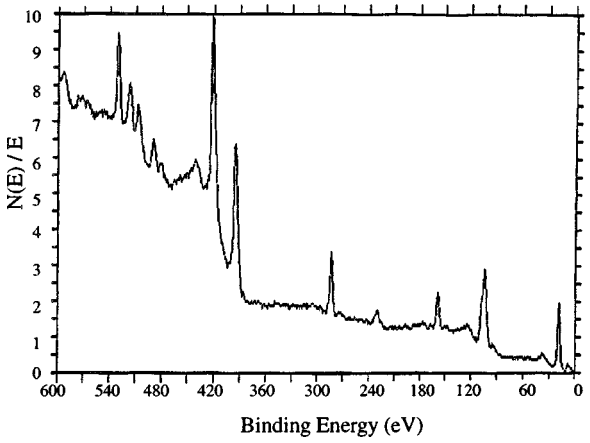

FIG. 6. XPS spectrum of a GaN layer grown on a SOI substrate.

STRUCTURAL AND ELECTRICAL PROPERTIES OF GaN GROWN ON COMPLIANT SOI SUBSTRATES

Figure 7 shows the XRD measurements of 0.75 μm thick GaN layers grown at 900 °C on (a) silicon and (b) SOI. Both samples show a peak at around 34.5° due to reflection from the (0002) plane of GaN. Scanning electron microscopy showed hexagonal hillocks on the surface of the GaN epil-

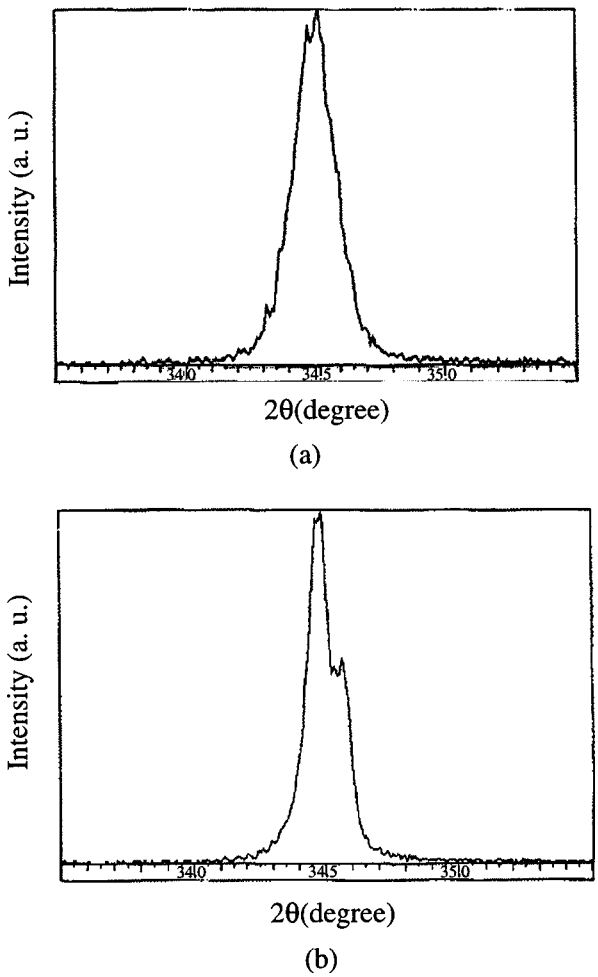

FIG. 7. X-ray spectrum for GaN grown at 900 °C in the same growth run on (a) a bulk silicon substrate and (b) a compliant SOI substrate.

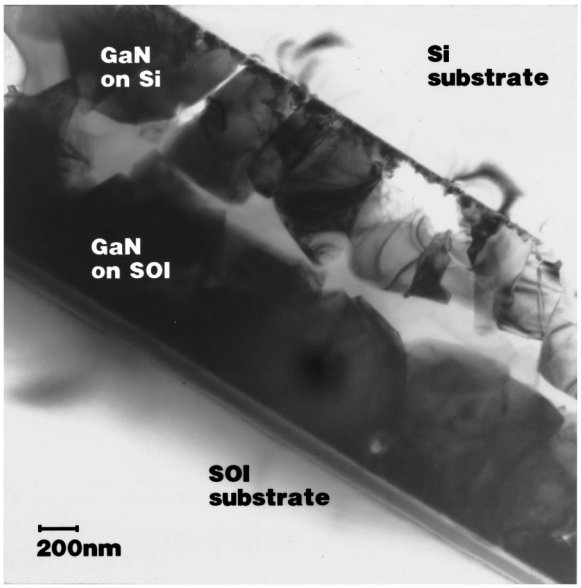

FIG. 8. TEM picture of the surface morphologies of GaN epilayers grown on bulk Si (layer in the upper part of the photograph) and compliant SOI substrates (layer in the lower part of the photograph). For comparison purposes, the two epilayer surfaces have been placed against each other.

ayers indicating wurtzitic GaN growth. This is consistent with reports[19] that GaN epitaxial layers would take wurtzitic structure if deposited on amorphous GaN buffers. The crystal quality of GaN on SOI is obviously better than that of GaN on Si as indicated by full width at half maximum (FWHM) values of 666 and 378 arcsec for GaN on Si and GaN on SOI, respectively.

The improvement in crystal quality can be further demonstrated by transmission electron microscopy (TEM). Figure 8 shows the TEM picture of a typical GaN epilayer region for growth on Si and SOI substrates. For comparison purposes, the two epilayer surfaces have been placed against each other. The GaN layer grown on SOI (layer in the lower part of the photograph) has a much better surface morphology than the GaN layer grown on Si (layer in the upper part of the photograph). The TEM pictures in Fig. 9 show further details of the grown layers and the SOI and silicon substrates. In the case of GaN grown on Si, there is a high concentration of threading dislocations. As a result, the epilayer consists of many small crystal grains of different size. In contrast, GaN grown on SOI shows a well-defined layer structure and manifests a much smaller number of threading dislocations. Overall, both XRD and TEM characterization support the fact that GaN epitaxy on SOI substrates provides the possibility of implementing the compliant substrate approach where strain caused by lattice mismatch can be effectively released and the crystal quality of the epilayer can be improved.

From the discussion above, the compliant substrate approach is based on the fact that the thin layer of the compliant substrate is more ''stretchable'' than the bulk layer and, thus, accommodates a large part of the strain caused by the lattice mismatch. At higher growth temperatures, the top thin silicon overlay and the buried SiO_2 layer of the SOI substrate should become more compliant and absorb most of the strain

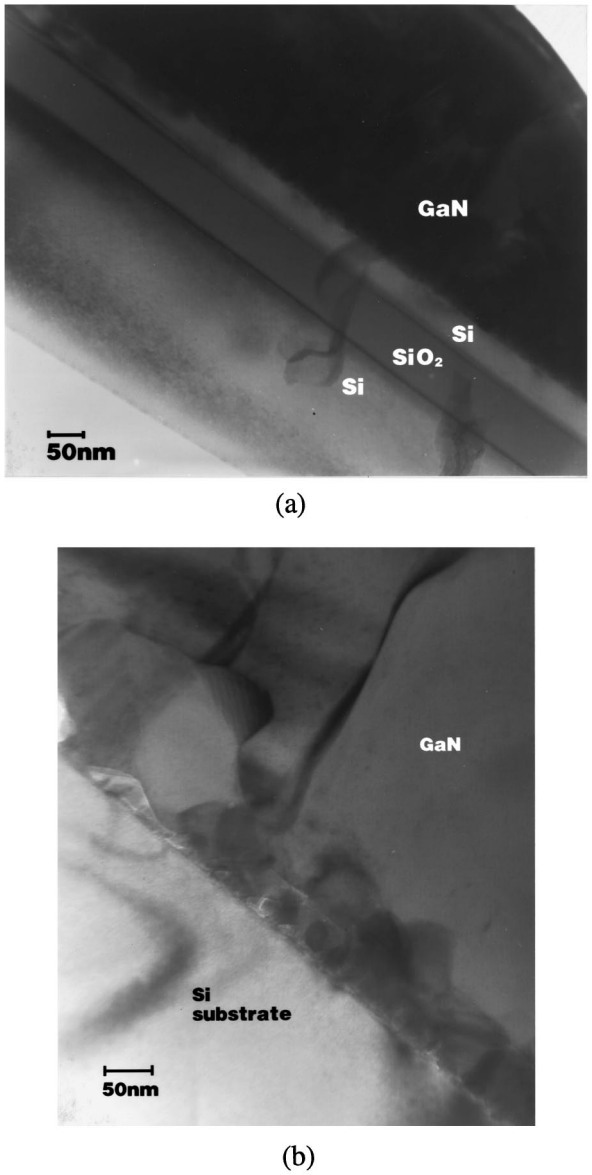

FIG. 9. TEM cross-sectional pictures of GaN epilayers grown on (a) compliant SOI and (b) bulk Si substrates.

resulting in improved GaN crystal quality. This effect can be demonstrated by XRD of GaN layers grown on SOI wafers at different temperatures (Fig. 10). The GaN layer grown at 700 °C has a large FWHM of 768 arcsec [Fig. 7(b)], while the FWHM of the GaN layer grown at 1000 °C is reduced by more than 50% to only 348 arcsec [Fig. 10(a)], which is also smaller than the 378 arcsec obtained at 900 °C [Fig. 7(b)], clearly demonstrating the trend of improved GaN quality with increased growth temperature.

The electrical transport properties of the GaN epilayers were evaluated at room temperature by van der Pauw–Hall measurements using In contacts. The GaN layers grown directly on Si substrates are highly resistive. The carrier mobility is probably too low for conventional Hall measurements. The low mobility can be due to the large number of threading dislocation dividing the GaN epilayer into small crystal islands and, thus, effective carrier transport is prohib-

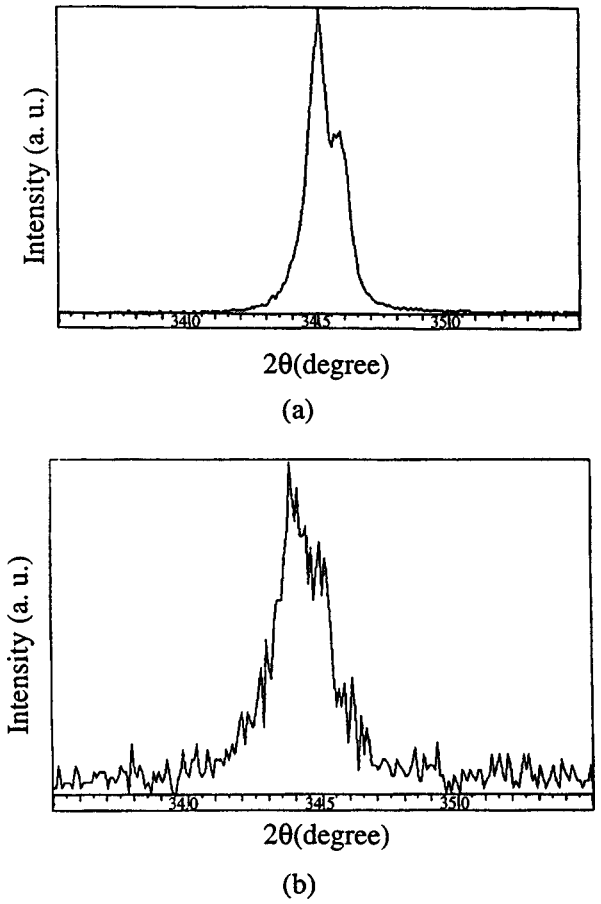

FIG. 10. XRD (0002) peak for GaN grown on compliant SOI substrates at (a) 1000 °C and (b) 700 °C growth temperature.

ited by the bad layer quality. However, mobility and carrier concentration of GaN layers grown on SOI can be readily measured. All the as-grown GaN layers are of *n*-type conductivity. Typically, for a 1–2 μm thick GaN layer grown on SOI, the electron mobility is in the order of 100 cm^2/V s with a background carrier concentration in the range of $1.5-5.0 \times 10^{17}$ cm^{-3}. Compared with the carrier concentration of the SOI substrate itself, which is almost two orders of magnitude lower (and which has an electron mobility in the same order of magnitude of the measured values for the GaN layer), an influence of the substrate on the Hall measurements can be excluded. A possible contribution of the SOI/GaN interface to the measured values can also be excluded, because GaN layers exhibit clearly larger electron mobilities as the film thickness is increased.

CONCLUSIONS

To improve the quality of epitaxially grown GaN, a compliant substrate approach has been employed so that the strain between the epilayer and the substrate can be released. GaN layers have been grown on SOI substrates by MOCVD. Compared with GaN grown on Si substrates, GaN layers grown on SOI show improved crystal uniformity, better surface morphology, and fewer threading dislocations, as demonstrated by XRD and TEM characterization. An increase in growth temperature results in a significant decrease of the FWHM value of the GaN (0002) XRD peak, indicating an improvement of the crystal quality of the epilayer. The background carrier concentration of the GaN layers grown on SOI is in the lower 10^{17} cm^{-3}, and the electron mobility is in the order of 100 cm^2/V s, providing reasonably good transport properties. SIMS and XPS analysis reveal the presence of C, O, and Si impurities in the GaN layers.

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