Nature and distribution of electrically active defects in Si-implanted and lamp-annealed GaAs

Sunanda Dhar,[a] Kwang S. Seo, and Pallab K. Bhattacharya
Solid State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan 48109

(Received 24 April 1985; accepted for publication 20 August 1985)

The nature and spatial distribution of deep levels arising from defects in device-quality, Si-implanted, and lamp-annealed liquid encapsulated Czochralski GaAs have been investigated. The best activation and mobility values are obtained for annealing times and temperatures of 3–5 s and 900–950 °C, respectively. Further improvements are obtained for a two-step annealing in which a second step at 840–850 °C for 15–40 s follows the main anneal step. From Hall measurements, average layer mobilities of 4000 cm^2/V s and activation of 55–65% are obtained for a Si^+ dose of 6.5×10^{12} cm^{-2} at 100 keV. Electrically active deep-level traps were studied by sensitive deep-level transient spectroscopy (DLTS) and optical DLTS techniques. A dominant 0.57-eV electron trap, which is also present in furnace-annealed GaAs, originates from implantation damage and is possibly related to V_{Ga}. Additional electron traps with activation energies of 0.35 and 0.40 eV are present only in lamp-annealed GaAs. Commonly observed hole traps have activation energies of 0.27–1.1 eV. The origins of these centers are discussed. Trap densities in single-step lamp-annealed samples are extremely low in comparison with furnace-annealed samples. Typical values of N_T/n are 10^{-2}–10^{-4}. Concentrations are even lower in samples undergoing two-step annealing. The spatial variation of trap density seems to be principally determined by the variation of defect density in the substrate. It is apparent that high-quality implanted and annealed GaAs can be obtained by the two-step lamp annealing procedure.

I. INTRODUCTION

Rapid thermal annealing (RTA) has emerged as a viable technique for dopant activation in ion-implanted semiconductors.[1,2] Unlike the more conventional furnace annealing method, in which the sample is heated (usually with a cap) at temperatures of 800–850 °C for ~20 min, during RTA the sample undergoes a pulsed temperature cycling at ~900 °C for 3–8 s. The annealing technique, with variations regarding the heat source, is now being extensively used in the fabrication of GaAs metal-semiconductor field-effect transistors (MESFET)[3,4] and more recently in the fabrication of GaAs-$Al_xGa_{1-x}As$ modulation-doped field-effect transistors (MODFET).[5,6] It has also been extended to other III-V semiconductors.

The recrystallization process is completed in the initial milliseconds of rapid thermal annealing and the remainder of the annealing time is utilized in improving the quality of the dislocation band underneath the recrystallized layer. It should be stressed that the structural quality of this region can be extremely important for device behavior, since unannealed defects in the interface region can lead to a large density of traps and to poor electrical characteristics. The nature and spatial distribution of electrically active defects in the active layer of lamp-annealed samples have not been studied in detail. We report here the results of a systematic study of traps present in Si-implanted and lamp-annealed GaAs. In particular, we have studied their spatial density variation in radial directions of GaAs wafers and have correlated these distributions with spatial profiles of bulk GaAs defects, electron mobility, and photoluminescence intensity. It is evident from this study that some of the dominant traps are damage related. By adopting a two-step annealing procedure in which an additional anneal is done at a lower temperature for a longer duration before or after the main pulse, considerable improvements are seen in activation, trap density, and photoluminescence intensity.

II. EXPERIMENT

A. Implantation and annealing

Polished wafers of 100-oriented undoped LEC GaAs were implanted with $^{29}Si^+$. Usually 5–10 μm of the polished surface was etched before direct implantation. For the samples reported here the implant dose and energy are 6.5×10^{12} cm^{-2} and 100 keV, respectively.

The implanted samples were annealed in a Heatpulse 210T Halogen lamp annealing station under flowing ultrapure nitrogen. Optimum annealing parameters were established after several initial experiments. The duration and temperatures of the anneals are in the ranges of 3–5 s and 900–950 °C, respectively. For the two-step annealing, an additional anneal at 850 °C for 15–40 s is done. This either preceeds or succeeds the main anneal pulse. Some anneals were also done at 850 °C for 30–45 s. A GaAs proximity cap was used during annealing.

B. Spatial uniformity

It has been our experience that low-temperature photoluminescence is a reasonably good index of the quality of the

[a] On leave from the Institute of Radio Physics and Electronics, University of Calcutta, 92, Acharya P. C. Ray Road, Calcutta 700 009, India.

 0021-8979/85/234216-05$02.40 © 1985 American Institute of Physics

material. We therefore measured the luminescence spectrum of lamp-annealed samples at 6 K and compared them with similar samples obtained from furnace-annealed GaAs. The luminescence was analyzed with a 1-m scanning spectrometer. The integrated PL intensity of the bound exciton and carbon-related transitions, which are the dominant features in the edge luminescence of ion-implanted GaAs, are comparable to or larger than those in similar furnace-annealed (850 °C, 20 min) samples.

Radial uniformity across 2-in.-diam implanted and lamp-annealed wafers were studied by low-temperature photoluminescence and Hall measurements. The spatial variations of mobility and activation in single- and two-step annealed samples are shown in Fig. 1. The activation values are calculated from the measured sheet-electron concentrations. Mobilities and activations are consistently higher for two-step annealing in which the low-temperature step follows the high-temperature main anneal step. The values of these parameters, obtained in our laboratories for samples implanted with 6.5×10^{12} Si^+ at 100 keV are among the highest reported and are comparable to the best furnace annealing data. In addition, the variation in mobility over a 2-in. wafer is within 5–10%. Mobility and activation profiles measured in our laboratory in a typical furnace-annealed sample are also shown in Fig. 1 for comparison. It should be mentioned that samples lamp-annealed at 850 °C only for periods of 15–40 s had poor mobility and PL intensity.

Figure 2 shows typical variations of integrated edge photoluminescence intensity over 2-in. wafers. Comparison is made between single- and two-step RTA and conventional furnace annealing. The improvement in the case of two-step annealing is evident. We generally find that the photoluminescence intensity variation closely follows the activation profile.

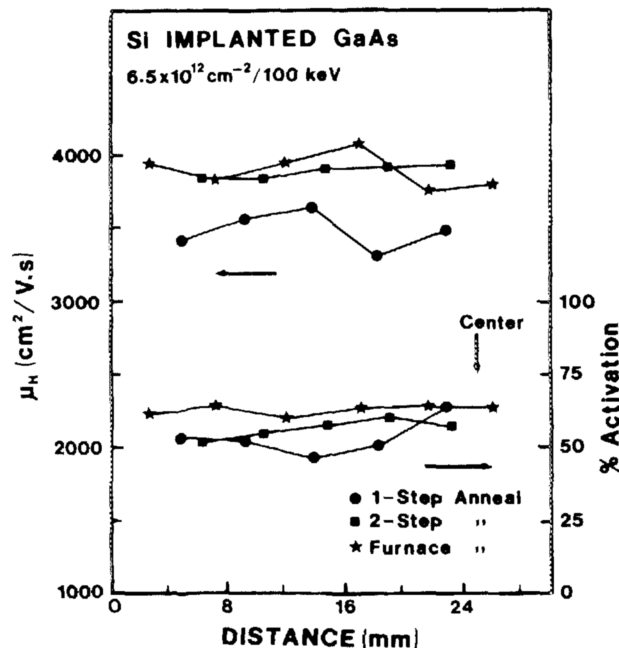

FIG. 1. Spatial profiles of Hall mobility and activation in furnace- and lamp-annealed Si-implanted GaAs.

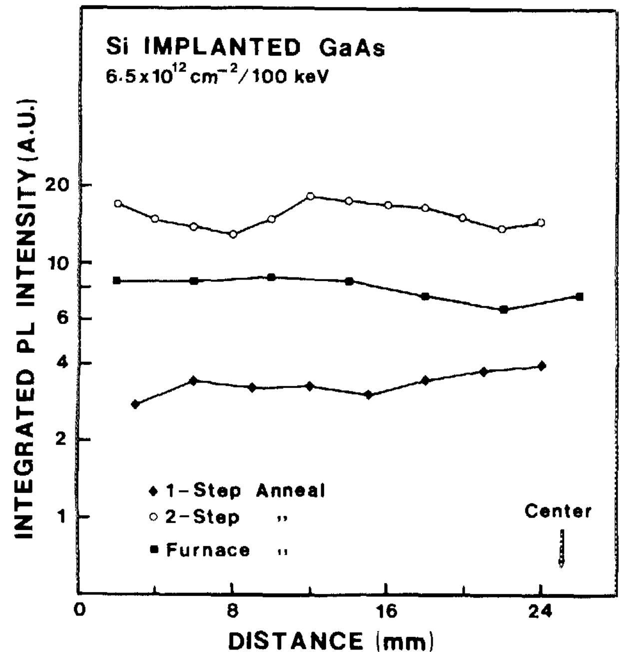

FIG. 2. Spatial variation of integrated photoluminescence intensity in furnace- and lamp-annealed GaAs.

C. Identification of deep-level defects

Measurements are made on Au Schottky barrier diodes deposited by vacuum evaporation on the implanted layers. The ohmic contact is made on the same surface by alloying

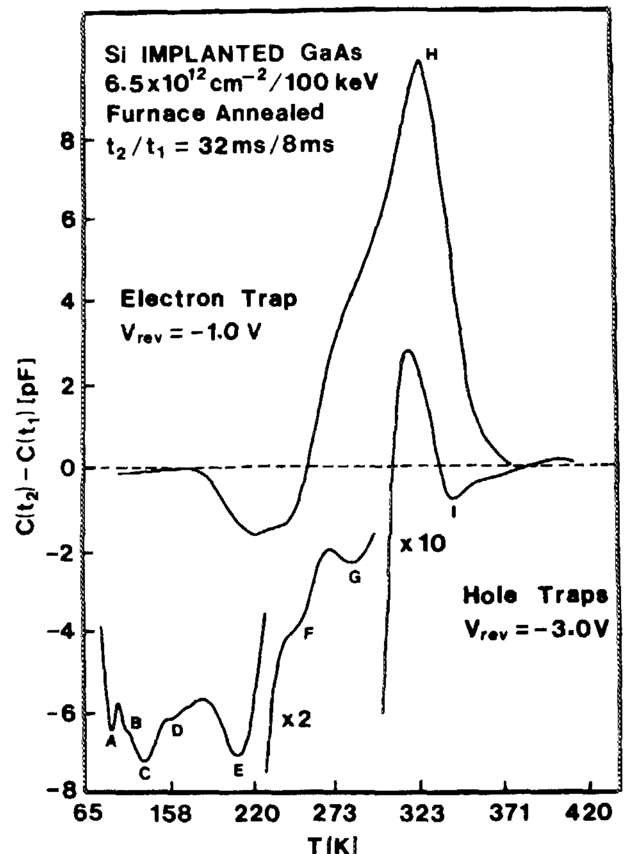

FIG. 3. Typical DLTS and ODLTS data obtained from measurements on Si-implanted and furnace annealed (850 °C, 20 min) GaAs.

TABLE I. Characteristics of electron and hole traps observed in Si-implanted and furnace-annealed GaAs.

Trap type	Trap label	Activation energy[a] ΔE_T (eV)	Capture cross section[b] σ_∞ (cm^{-2})	Possible origin
Electron traps	H	0.57	1.4×10^{-15}	Implantation damage
	J	0.82	2.0×10^{-14}	EL2, related to Ga vacancy
Hole traps	A	0.21	1.3×10^{-13}	Lattice damage
	B	0.27	7.0×10^{-12}	Possibly related to Ga vacancies
	C	0.25	6.0×10^{-15}	Possibly related to Ga vacancies
	D	0.47	9.6×10^{-10}	Possibly related to Ga vacancies
	E	0.43	5.0×10^{-15}	Cu impurity
	F	0.65	1.9×10^{-12}	Implantation damage
	G	0.72	2.4×10^{-12}	Native defects
	I	1.10	1.1×10^{-8}	Implantation damages

[a] Denotes average value over all samples measured.
[b] Determined from the emission rate prefactor.

Au-Ge/Ni. The device geometry is such that the contact-to-diode distance is small and it reduces series resistance effects. Deep level transient spectroscopy (DLTS) and optical DLTS (ODLTS) measurements were made to identify electron and hole traps which arise from defects in the material. Electron traps were studied by majority-carrier pulse filling in the DLTS scheme and hole traps were filled by pulsed intrinsic light excitation.

In order to form a basis for comparison, measurements were done on implanted samples activated by furnace annealing. Output from DLTS and ODLTS measurements on these samples are shown in Fig. 3. The positive- and negative-going peaks and shoulder indicate thermal emission from electron and hole traps, respectively. The data of Fig. 3 represent the commonly observed deep-level traps in Si-implanted and furnace annealed GaAs. We have recently made a detailed study of the origin of these centers,[7] from which we could conclude that some of these centers are process related. Others arise from existing substrate defects or damage created during implantation. The characteristics of these dominant traps are listed in Table I. The notable feature is that the density of most dominant traps are reasonably high, with N_T/n ranging from 10^{-1} to 1.0. The data obtained from DLTS and ODLTS measurements on single-step lamp-annealed samples are shown in Fig. 4. Electron traps K and L are new centers and they are occasionally observed in lamp-annealed samples only. Figure 5 depicts the Arrhenius plots of electron traps in lamp-annealed samples.

Concentration profiles of some commonly observed traps across a 2-in. single-step lamp-annealed wafer is shown in Fig. 6. It appears that some traps tend to follow the substrate defect profile[8] while for the others such a trend is not evident. It is also very clear that trap densities are drastically reduced. The concentration of observed traps are even lower in the two-step lamp annealed samples, which prevented accurate measurements.

III. DISCUSSION

The mobility and activation values obtained in the course of this study are comparable to the best values of these parameters reported by others.[3,9] The activation efficiency calculated from Hall data is slightly erroneous because of the depletion layer formation due to surface state pinning of the Fermi level.[10] It has also been observed[11] that Hall measurements yield a smaller activation efficiency than C-V profiling. The corrections for the surface depletion effect increases the activation efficiency in our lamp-annealed samples to 85–95%.

The commonly observed electron trap H is also observed in furnace-annealed GaAs. We have earlier related[7] this electron trap, having an activation energy of 0.57 eV, to implantation induced damage. Our present data in Fig. 6 shows that the concentration of this center follows the dislocation defect profile in the substrate. It is therefore thought

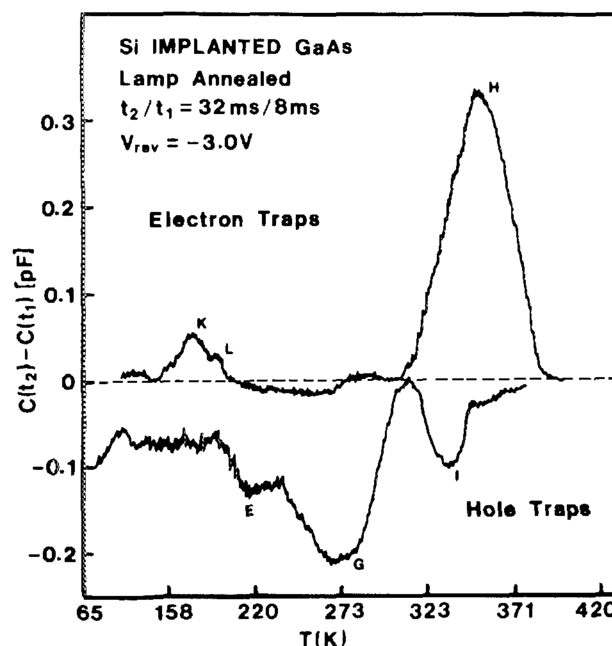

FIG. 4. DLTS and ODLTS data obtained from measurements on Si-implanted and lamp-annealed GaAs. The implant dose and energy are 6.5×10^{12} cm^{-2} and 100 keV, respectively. Single-step annealing was done at 900 °C for 5 s.

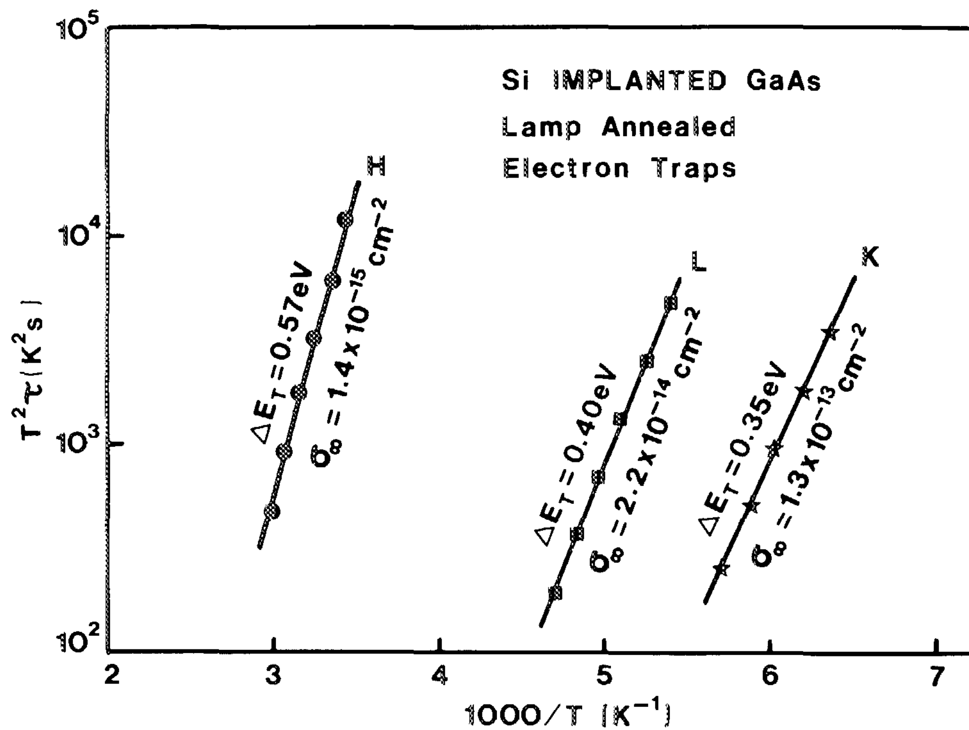

FIG. 5. Arrhenius plots of traps detected in single-step lamp-annealed GaAs. Trap H is a dominant center in both furnace- and lamp-annealed GaAs.

that implantation damage at or around substrate dislocations enhances the formation of electrically active defects after annealing. This segregation of imperfections around dislocations has been observed before.[12-14] It has been recently concluded by us[7] that the possible origins of the 0.72- and 1.1-eV hole traps are native defects and implant damages, respectively. The spatial distribution of the density of these traps, as seen in Fig. 6, probably reflects the segregation effects mentioned above. The 0.43-eV hole trap has characteristics which closely resemble those of Cu impurities in GaAs. Electron traps K and L have not been observed by us in furnace-annealed GaAs and without further evidence their origin cannot be ascertained. It is possible that they are created by the thermal impulse during RTA. Some of the commonly observed hole traps present in furnace-annealed GaAs are also present in lamp-annealed samples, but their concentrations are much lower.

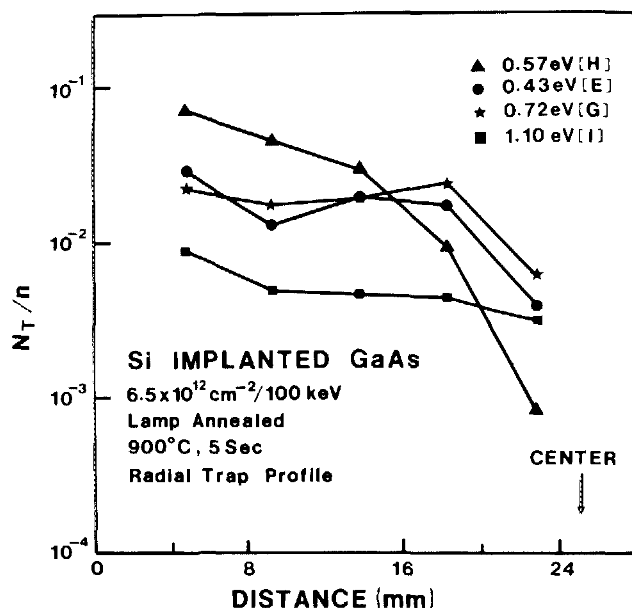

FIG. 6. Spatial variation of the density of commonly observed traps in Si-implanted and lamp-annealed GaAs.

The important revelation from this study is that trap densities are lower in lamp-annealed samples, compared to that in equivalent furnace annealed samples. In two-step annealed samples, trap densities are even lower. The improvement probably results from the reduction of defects in the dislocation band just beneath the active layer. Preliminary Raman spectroscopy measurements seem to indicate this. A more detailed study is in progress. It should be mentioned that reduced trap densities will minimize backgating effects and noise in GaAs MESFETs.

Another point which should be mentioned is the role of the substrate defects and damage defects on the final uniformity. We have observed that certain processing steps, such as etching prior to implantation to remove polishing and sawing damage, can greatly reduce the concentration of some of these traps and improve their uniformity.

IV. CONCLUSIONS

The nature and distribution of deep levels arising from defects and impurities in Si-implanted and halogen lamp-annealed GaAs have been investigated. Trap densities are lower in these samples, compared to that in similar furnace annealed samples, by about two orders of magnitude, though some new centers are identified. Densities are further reduced by using a two-step annealing procedure in which an additional anneal at 840–850 °C for 15–40 s is done after the main anneal step. Mobilities, activations, and uniformities,

with values among the best reported for Si-implanted GaAs, are obtained after such two-step lamp annealing.

ACKNOWLEDGMENTS

The authors wish to thank Dr. C. L. Ghosh of ITT-Gallium Arsenide Technology Center for providing the implanted wafers and for helpful discussions. The work is supported by the National Science Foundation under Grant ECS-8408743.

[1]T. O. Sedgwick, J. Electrochem. Soc. **130**, 484 (1983).
[2]J. Narayan and O. W. Holland, J. Appl. Phys. **56**, 2913 (1984).
[3]M. H. Badawi and J. Mun, Electron. Lett. **20**, 125 (1984).
[4]T. Ohuishi, Y. Yamaguchi, T. Inada, N. Yokoyama, and H. Nishi, IEEE Electron Device Lett. **EDL-5**, 403 (1984).
[5]Y. Kajikawa, K. Mizuguchi, T. Murotani, K. Fujikawa, and T. Sonoda, J. Vac. Sci. Technol. B **2**, 249 (1984).
[6]P. Pearah, T. Henderson, J. Klem, H. Morkoc, B. Nilsson, O. Wu, A. W. Swanson, and D. R. Ch'en, J. Appl. Phys. **56**, 1851 (1984).
[7]S. Dhar, P. K. Bhattacharya, F-Y. Juang, W. P. Hong, and R. A. Sadler, IEEE Trans. Electron Devices (to be published).
[8]D. E. Holmes, R. T. Chen, and J. Yang, Appl. Phys. Lett. **42**, 419 (1983).
[9]M. Kuzuhara, H. Kohzu, and Y. Takayama, IEDM. Dig. Tech. Papers, 170 (1982).
[10]A. Chandra, C. E. C. Wood, D. W. Woodard, and L. F. Eastman, Solid State Electron. **22**, 645 (1979).
[11]B. Tell, R. F. Leheny, A. S. H. Liao, T. J. Bridges, E. G. Burkhardt, T. Y. Chang, and E. D. Beebe, Appl. Phys. Lett. **44**, 438 (1984).
[12]K. Kitahara, K. Nakai, and S. Shibatoni, J. Electrochem. Soc. **129**, 880 (1982).
[13]H. C. Casey, J. Electrochem. Soc. **114**, 153 (1967).
[14]A. K. Chin, A. R. Von Neida, and R. Caruso, J. Electrochem. Soc. **129**, 2386 (1982).