Amorphous In-Ga-Zn-O Thin Film Transistor for Future Optoelectronics

by

Tze-Ching Fung

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Doctoral Committee:

Professor Jerzy Kanicki, Chair
Professor Kensall D. Wise
Associate Professor Cagliyan Kurdak
Associate Professor Jamie D. Phillips

To Dad, for teaching me the value of work.
To Mom, for encouraging me to complete the degree.
And to My Younger Brother, for sharing with me all the joy in life.

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Chapter 1

Introduction

1.1 Overview / Background

1.1.1 Current status and limitation of a-Si:H TFT backplane technology

The Hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) has long been the workhorse in the active-matrix liquid crystal display (AM-LCD) industry. As the most critical element of the entire AM-LCD, the active-matrix backplane commonly consists of a array of a-Si:H TFT pixel electrode circuits, which directly drive each individual liquid crystal cell pixel [1, 2]. This approach significantly reduces the pixel crosstalk and allows the LCD display to have a high resolution. Thanks to the growing need for large area displays for home entertainment and the full adoption of digital broadcasting, the active-matrix flat panel display (AM-FPD) industry experienced a strong growth during the past few years. It has taken over the dominate role in TV market from the old, bulky cathode ray tube (CRT) technology and is predicted to reach a 96% market penetration during year 2009 [3]. Although there are many different technologies available for AM-FPD, active-matrix liquid crystal display (AM-LCD) is by far the dominant one and is expected to occupy more than 70% of the entire AM-FPD market [3].

Just like the microelectronics industry pursues the miniaturization of transistors dic-

tated by Moore's law for lower production cost and enhanced functionality, scientists and engineers continuously investigates new material and processing technologies to fabricate TFT backplane over even larger substrate areas. Because of this unique technological road map, the TFT backplane has also frequently been called "macroelectronic" device [4]. During the past decades, the plasma enhanced chemical vapor deposition (PECVD) has been proven to be the ideal technique to deposit highly uniform a-Si:H thin film while keeping up the trend of substrate size scaling [5]. Today, the state-of-art Gen-8 facility is able to process glass substrate approximately 2160 × 2460 mm in size [6], which can produced up to six 52-inch flat panel TV screens from one single substrate!

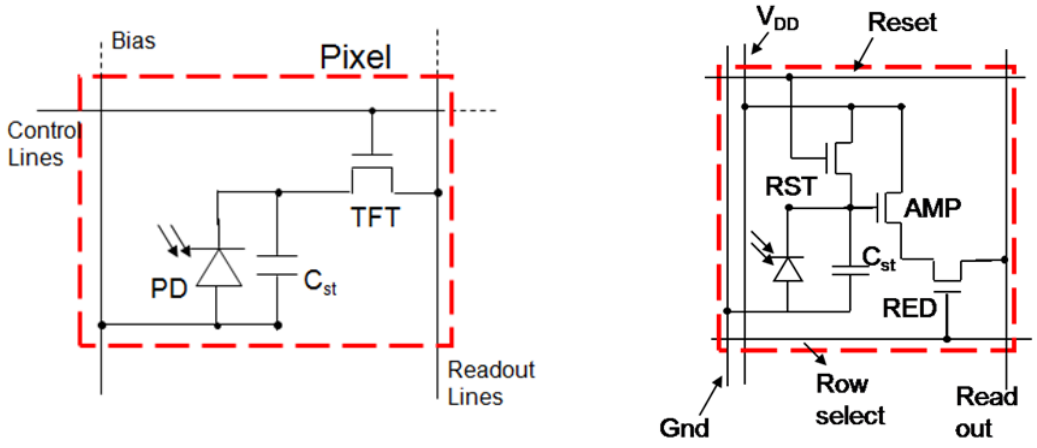
The typical PECVD a-Si:H TFT has field effect mobility (μ_{eff}) of 0.6 ~ 0.8cm^2/Vs, sub-threshold swing of 0.3 ~ 0.4V/dec, off-state drain current (I_{D_off}) below 10^{-13}A and on-to-off ratio about 10^7 [7]. These properties are suitable for liquid crystal cell switching but the μ_{eff} could become insufficient for the new requirements of next generation displays. For example, the future trend for AM-LCD is toward large area (e.g. 82-inch) with QFHD (3840×2160 pixels) resolutions [8, 9]. To suppress the display motion blur effect in QFHD, high frequency (120~240Hz or even higher) display driving circuits will be inevitable [10]. The driving scheme of the 120Hz (or higher) QFHD display only allows the pixel charging time to be less than 4μsec [9]. Conventional a-Si:H TFT backplane configuration doesn't work well in such short time and the pulse / clock signal can be distorted. To address this issue, proposed solutions are focused on reducing the gate bus-line RC propagation delay, such as adding gate planarization layer [11], adopting buried bus-line structure [12] or using low resistance Cu interconnection [13]. Nonetheless, the low μ_{eff} (< 1cm^2/Vs) of a-Si:H TFT itself can still fundamentally restrict the high frequency response of backplane. A TFT LCD pixel charging time (t_{charge}) is about five RC time constants ($t_{charge} \sim 5R_{on}C_{pix}$),

where C_{pix} is the pixel capacitance and R_{on} is the TFT channel resistance. R_{on} can be estimated as follows:

$$R_{on} \approx \frac{L}{W\mu_{eff}(V_{GS} - V_{th})C_{SiNx}}, \quad (1\text{-}1)$$

where W and L are channel width and length, respectively; V_{GS} and V_{th} are gate voltage and TFT threshold voltage, respectively; and C_{SiNx} is the gate insulator capacitance. For a typical a-Si:H TFT pixel, C_{pix} is ~0.5pF, and R_{on} is ~1.67MΩ (W/L=3, μ_{eff} ~ 0.6cm^2/Vs, (V_{GS}-V_{th})~10V and C_{SiNx} ~3.32×10^{-8} F/cm^2). This combination results in a t_{charge} of 4.2μsec. Thus, the t_{charge} required for a-Si:H TFT is too long, and driving large size, high rate/ resolution display with a-Si:H TFT backplane will be either impractical or complicated [9]. As indicated in (1-1), a high-mobility material is desired, since it can reduce R_{on} and t_{charge}.

The other emerging area in AM-FPD is the emissive display such as active-matrix organic light-emitting display (AM-OLED), where the organic light emitting diode (OLED) is directly integrated with the TFT pixel electrode circuit. AM-OLED avoids the need of backlight and the dynamic range of the AM-OLED brightness can be controlled at the pixel level, which is ideal for TV applications [14]. In addition, it can have an extremely high contrast ratio and delivers much better picture quality than the AM-LCD [15]. Despite all these attractive properties, AM-OLED actually poses more stringent requirement on TFT backplane. Unlike liquid crystal which only required external electrical field to change its phase, OLED takes significant amount of current to produce light. The μ_{eff} of a-Si:H TFT, unfortunately, is not high enough to drive a large area AM-OLED [16]. Because the TFT may constantly operate under high bias, a long term electrical instability is another concern [17] and can also make the pixel electrode circuit design more complicated (e.g. additional compensation circuits are needed) [18].



(a) (b)

Figure 1.1 Circuit schematics for (a) passive pixel sensor (PPS) and (b) active pixel sensor (APS). Both pixel circuits contain photodiode (PD) and storage capacitor (C_{st}). RED, AMP and RST represent read, amplifier and reset TFTs, respectively, in APS design.

1.1.2 a-Si:H TFT backplane in photo-imager

The application of a-Si:H TFT backplane is not limited to AM-FPD. By integrating the photodiode or radiation sensitive layer with the backplane, a-Si:H TFT can also be used for sensor signal readout [19]. One important example is the flat panel X-ray imager used for medical imaging [20-22]. Traditionally, a single TFT pixel electrode circuits is used to passively (no amplification) control the signal current transfer from sensor (Figure 1.1(a)). This restricts the sensor signal-to-noise ratio and also lengthens the imager response time. Recently, a more advanced approach, or so called "active pixel sensor (APS)" is proposed. By adding a transconductance amplifier stage in the a-Si:H TFT pixel electrode circuit, the APS is able to achieve a higher signal-to-noise ratio and a high operating speed [23]. Such circuit is expected to be more suitable for a low-noise, a high speed imaging like X-ray fluoroscopy [24].

As one of the key metrics for photo-imager performance, the sensor resolution can be

Applications	Technological Requirements on TFT Backplane	Enabling Material Properties
AM-LCD	Large area	Uniform amorphous phase
	High aperture ratio	Visible light transparency / High mobility
	Fast response	High mobility
AM-OLED	Good current driving capability	High mobility
	Good stability	Low defect and weak bonding density
Photo-imager	Large dynamic range	High mobility
	Small pixel size (high resolution)	High mobility

Table 1.1 Challenges of TFT backplanes for next generation optoelectronics.

more demanding than what is needed for display and it is directly dictated by the TFT backplane design. As shown in Figure 1.1(b), typical APS has three TFTs (read, amplifier and reset TFTs) in one single pixel [24]. In order to achieve desirable APS signal gain for signal readout, both amplifier and readout TFT can have a width-over-length ratio (W/L) of 150μm/25μm when using a-Si:H as the semiconductor material [23]. These transistors take a significant amount of pixel area (~50% for 250μm^2 pixel size) resulting in a low imager resolution (<200dpi) [25], which is considered as one drawback for a-Si:H TFT APS. To better understand the design constrain, we approximate the small signal current gain of AMP TFT (g_{m_AMP}) by its saturation region transconductance:

$$g_{m\_AMP} \cong \mu_{eff} C_{ox} \frac{W}{L}\left(V_{GS\_AMP} - V_{th}\right) , \tag{1-2}$$

where V_{GS_AMP} is the difference of AMP TFT gate and source voltage; V_{th} is the threshold voltage. Equation 1-2 suggests that the g_{m_AMP} is proportional to the product of μ_{eff} and W/L ratio. For a low mobility semiconductor like a-Si:H, designing a TFT with a large W/L ratio to achieve a high gain is necessary. Therefore, for a definite gate length, adopting TFT

Technology	Mobility (cm^2/Vs)	Visible Light Transparency	Large Area Uniformity	Comments
a-Si:H	<1	Poor	Good (Gen-8)	Low mobility, limited current driving capability
Poly-Si	~100	Poor	Poor (Gen-4)	Additional crystallization process required
ZnO	20~50	Good	Poor	Strong tendency to form poly phase
a-IGZO	3~12	Good	Good (Gen-8)	Balance between mobility and uniformity

Table 1.2 Comparison of different TFT technologies.

with higher mobility is one possible solution to achieve a smaller pixel area without sacrificing the APS performance. Table 1.1 summarizes the challenges of TFT backplanes for next generation optoelectronics and it is clear that a new high mobility semiconductor material yet with a uniform amorphous phase over a large area is highly desired.

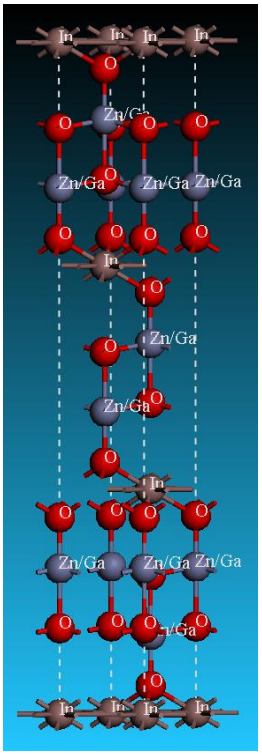
1.1.3 High performance amorphous In-Ga-Zn-O TFTs

Since 2004, there has been great interest in adapting TFT made of ionic amorphous oxide semiconductors (IAOS). Specifically, the ternary oxide system which consists of In_2O_3, Ga_2O_3 and ZnO has shown promising electrical performance for TFT active layer with a high μ_{eff} (3~12 cm^2/Vs), low I_{D_off} (<10^{-12}A) and expected good uniformity compatible with the state-of-the-art Gen-8 substrate size [26, 27].

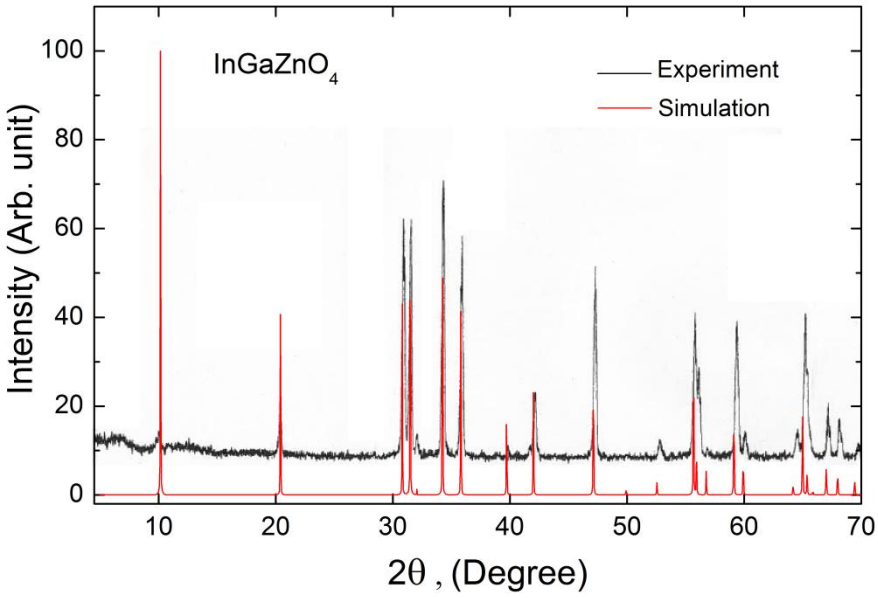
Table 1.2 compares amorphous In-Ga-Zn-O (a-IGZO) with other TFT technologies. It can be easily seen that a-IGZO TFT is currently the only technology which can achieve a desired balance between high mobility and large area uniformity. Although poly-crystalline silicon (poly-Si) TFT has μ_{eff} close to 100 cm^2/Vs, it required additional

re-crystallization steps such as excimer-laser annealing [28], metal seeding [29] or solid phase crystallization [30]. These add more complexity and costs to the process. Also the substrate area used by poly-Si TFT technology (Gen-4, 730 × 920 mm [15]) is about 4 generations behind what a-Si:H TFT can achieve (Gen-8) today. Mono-oxide semiconductor, ZnO, has been used as the active-layer in TFT channel. ZnO layer can be deposited by pulse laser deposition (PLD) [31], RF magnetron sputtering [32] or atomic layer deposition (ALD) [33] and the TFT μ_{eff} is around 20~50 cm^2/Vs. Despite its high mobility, due to its strong poly-crystalline nature even when deposited at room temperature [34], the grain boundary of such oxide semiconductor could affect device electrical properties, uniformity and stability over a large area.

Single-crystalline $InGaZnO_4$ (sc-IGZO) has a complex layered structure with alternating laminated layers of InO_2 and GaO(ZnO) [35, 36]. Figure 1.2(a) illustrates the crystal structure of $InGaZnO_4$. This structure was then inputted into the modeling software [37] to simulate the x-ray diffraction pattern of the $InGaZnO_4$. The result is highly consistent with the actual XRD rocking curves we obtained from a high quality $InGaZnO_4$ sputter target (Figure 1.2(b)). This also indicates that the structural model is closely representing the actual material. Orita *et al.* reported the first-principles molecular orbital (MO) calculations of $InGaZnO_4$ crystal structure by discrete-variational (DV)-$X\alpha$ method [36]. Figure 1.3 shows the calculated density-of-states (DOS) distribution for $InGaZnO_4$. The valence band is formed primarily by O 2*p* and Zn 3*d*-orbitals while the conduction band is formed by the *s* and *p* orbitals of the three metals, with some influence by the O *2p*-orbitals. The In 5*s* partial DOS shows a shoulder peak on the lower-energy side. Therefore, the conduction band minimum (CBM) of $InGaZnO_4$ is form by In 5*s* band only. Nomura *et al.* subsequently reported the calculation of a-IGZO electronic structure by the pseudopotential and



(a)



(b)

Figure 1.2 (a) (Color) Structure of the $InGaZnO_4$ crystal. The brown, blue and red balls represent In, Zn/Ga and O atoms, respectively. (b) (Color) XRD rocking curves of the $InGaZnO_4$. Black line: experimental result; red line: simulation result.

plane wave method at the local-density approximation (LDA) level [35]. This study also suggested that the CBM of a-IGZO is formed mainly by In ions (Figure 1.4).

Unlike ZnO, a-IGZO can have a uniform amorphous phase because multiple oxides (In_2O_3 & Ga_2O_3) are introduced to promote the glass phase formation [38] and the amorphous phase is thermally stable up to ~500˚C [39]. Several methods have been reported for a-IGZO deposition, including PLD [39, 40], RF [41] and DC [26] magnetron sputtering while the latter is the most attractive due to high rate deposition in comparison to other methods. Because of the unique electronic structure, a-IGZO is insensitive to bond angle variance of metal-oxide-metal chemical bonds induced by structural randomness. As illustrated in Figure 1.5(a), in conventional covalent bond semiconductors (such as Si), electrons are conducting through a highly directional sp^3 bonding. When these semiconductors are in amorphous state, distortions can occur in sp^3 bonding and will result in reduced carrier mobility. On the other hand, in IAOS (such as In-Ga-Zn-O), electrons are conducting through metal ion's *ns* orbital. Since *ns* orbital is symmetrical, the conducting path and carrier mobility can still be preserved even in amorphous phase. (Figure 1.5(b)) To ensure a high mobility in amorphous phase, a sufficient *ns* orbital overlap between metal ions is necessary. To satisfy this requirement, Hosono *et al.* proposed a working hypothesis which predicts the metal ion should be heavy post transition metal cations with electronic configuration of $(n-1)d^{10}ns^0$, where $n \geqq 5$ [42-44]. For example, the Hall mobility of the In-Ga-Zn-O system is primarily determined by the fraction of In_2O_3 content [42] in agreement with the Hosono working theory since In^{3+} has the largest ionic radius (n=5) among the metal cations.

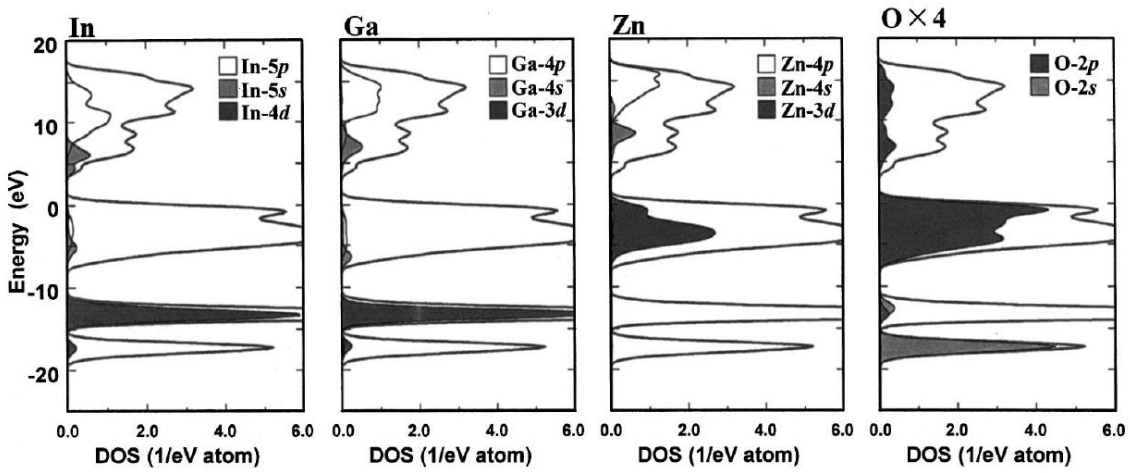


Figure 1.3 Partial density-of-states (DOS) curves for $InGaZnO_4$ crystal structures. The top of the valence band is located at zero energy and the total DOS is also shown in each figure as reference. (After Orita *et al.*, Ref. [36])

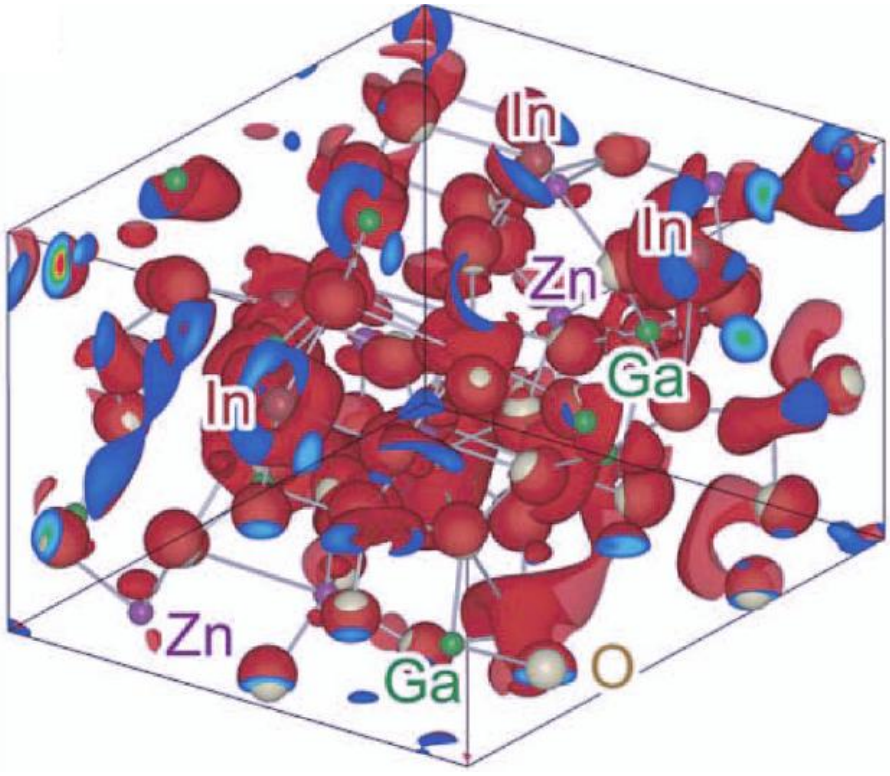


Figure 1.4 (Color) The red surfaces represent the conduction band minimum (CBM) wave function ($|\psi|^2$) in a-IGZO structure. The $|\psi|^2$ is composed of In 5*s* orbitals hybridized with O 2*p*. The blue-to-red planes show cross sections of the $|\psi|^2$ on the edge planes of the simulation cell. (After Nomura *et al.*, Ref. [35])

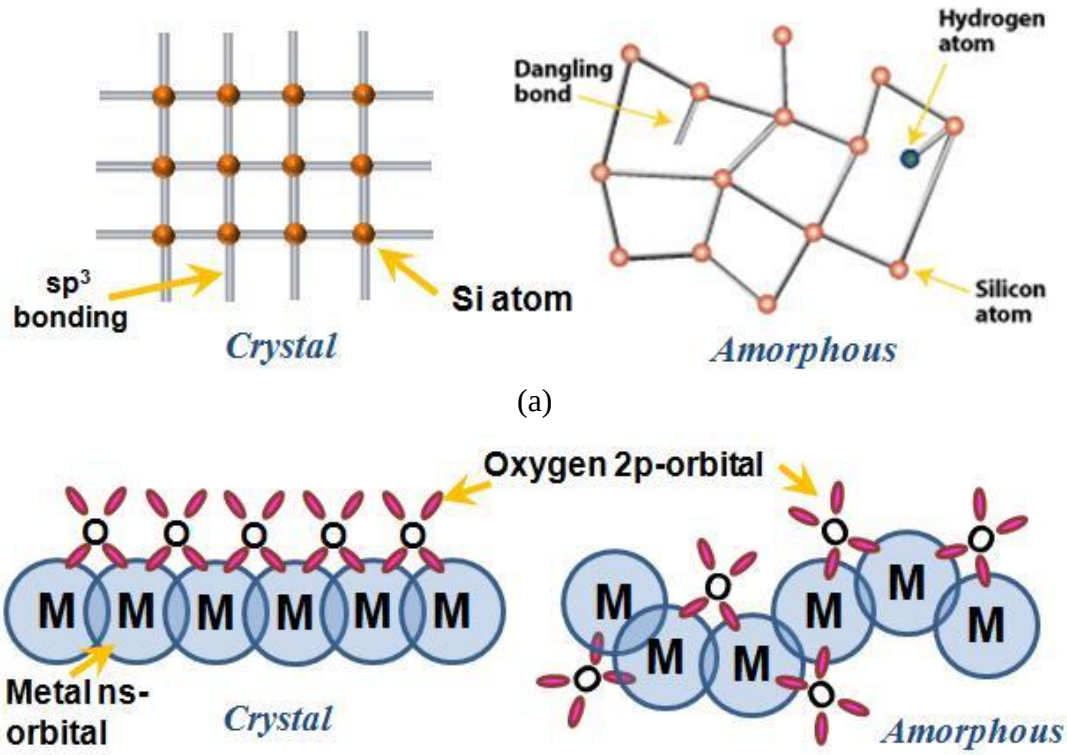


Figure 1.5 Schematic orbital drawing of electron conducting pathway (conduction band bottom) in (a) conventional covalent bond semiconductors (e.g. Si) and (b) ionic oxide semiconductors. (Adapted from [39])

For TFT to have a low I_{D_off} and high on-to-off ratio, it is important to control the semiconductor carrier concentration to a very low level. In IAOS, carrier generation can occur via oxygen vacancy formation. For examples, ZnO has been reported to have a very high carrier concentration in the as-deposited states [45]. It is usually because of the un-optimized deposition condition and the generation of excess oxygen vacancies in the thin-film. The incorporation of Ga^{3+} actually helps in suppressing the oxygen vacancies in a-IGZO thin-film since it has a stronger bonding to oxygen than Zn or In ions [39]. A comparative study between a-IZO and a-IGZO has also shown that a-IGZO is able to have five orders of magnitude larger reduction in carrier concentration than a-IZO when two

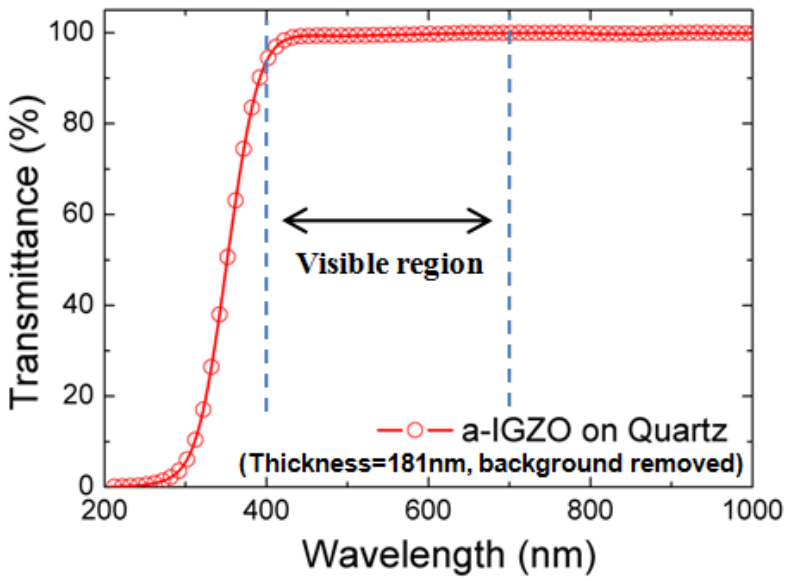


Figure 1.6 Absorption spectrum of the a-IGZO thin film.

thin-films are deposited under the same condition [42].

Finally, even though a-Si:H is widely used in TFT backplane, it absorbs visible photons and has a low visible light transmittance (<30%). This has been a major drawback for utilizing such material in optoelectronics and can even raise the concern of light induced instability [46]. On the other hand, similar to ZnO, a-IGZO has a wide bandgap (~3eV) and is highly transparent in visible light (with transmittance over 90% as illustrated in Figure 1.6 [47]). This property opens up to new application such as transparent electronics or see-through display. In addition, light may directly transmit through a-IGZO TFT. This capability can permit the display or sensor to operate in the direct transmission mode for improving pixel aperture ratio.

In conclusion, a-IGZO TFTs possesses unique physical properties and better electrical performance over traditional a-Si:H TFTs. The scope of this dissertation work is to study various aspects of the a-IGZO TFTs and hopefully, to shed light on potential application of such technology to future optoelectronics.

1.2 Dissertation Organization

This dissertation commences with the discussion on a-IGZO TFT fabrication and electrical properties in Chapter 2. Advanced electrical analyses are further introduced in Chapter 3. The source/drain (S/D) series resistance is extracted and studied. A new gate voltage dependent field-effect mobility model is also proposed and demonstrated. Considering many optoelectronic applications that may subject TFT to illumination, Chapter 4 discusses the photofield-effect in a-IGZO TFTs. Both wavelength and intensity dependent photo responses are presented. To provide physical explanation of the experimental observations, a mathematical analysis is also conducted. Chapter 5 and 6 discusses the two dimensional numerical simulation of the a-IGZO TFT. In order to accurately model the TFT electrical properties, a new density-of-states (DOS) model for a-IGZO thin film is proposed. The impacts of S/D series resistance and DOS properties are also discussed. Chapter 7 discusses the bias-temperature stress (BTS) induced a-IGZO TFT electrical instability. The stretched-exponential equation is proposed to model our experimental results that can be used for TFT life-time prediction. For the potential applications in imager, Chapter 8 studies the noise properties in a-IGZO TFT. The $1/f$ noise theories and the working principle of experimental setup are briefly reviewed. Finally, Chapter 9 concludes this dissertation work. Future research directions are also recommended.

Chapter 2

Electrical Properties of the a-IGZO TFTs

2.1 TFT Fabrication and Structure

Throughout the scope of this dissertation work, various a-IGZO TFT structures are used. For studying the fundamental electrical (Chapter 2, 3) and opto-electrical (Chapter 4) properties, the common gate TFT structure was chosen. Such structure is easy to fabricate and eliminates most of the processing induced variations. When studied the a-IGZO TFT electrical instability (Chapter 7), we utilized the defined gate TFT structure, because it is similar to the structure used in the actual display or imager backplane. The detail fabrication steps for all these structures are summarized in the following sections, which provides a good overview for readers who are interested in device fabrication.

2.1.1 Common gate, pulse-laser deposition (PLD) a-IGZO TFT

The common gate, inverted staggered amorphous a-IGZO TFTs serve as the most convenient test vehicle for studying the fundamental TFT electrical properties. Figure 2.1 highlights the process flow for making such TFT. We initially selected heavily doped (n^{++}) silicon wafer with 100nm thermal oxide layer as gate electrode and gate dielectric layer, respectively. A 40nm thick a-IGZO active layer was deposited on the substrate by pulse-

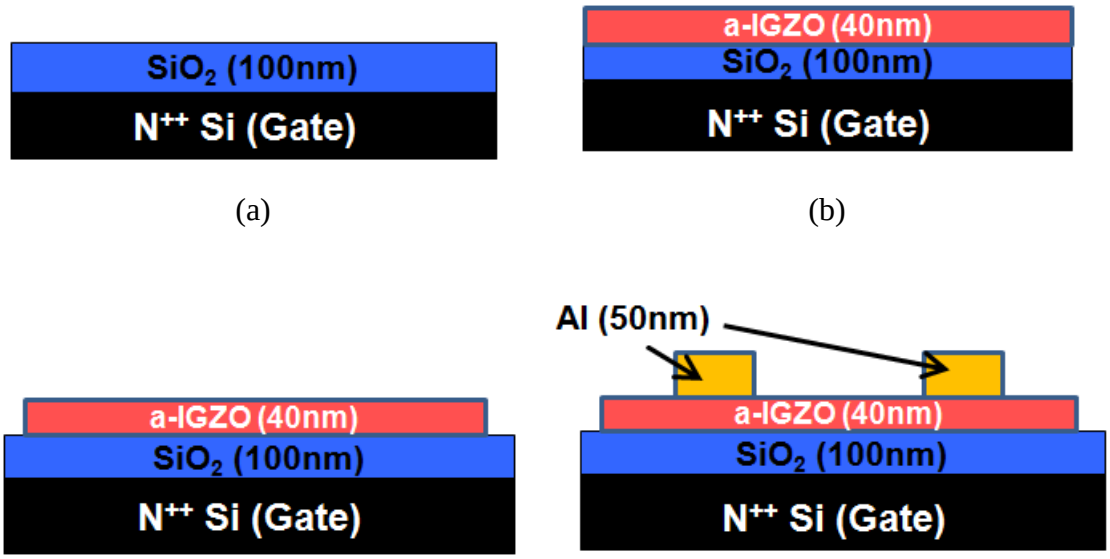


Figure 2.1 Process flow for making the common gate, inverted-staggered PLD a-IGZO TFT: (a) wafer cleaning, (b) deposit 40nm of a-IGZO thin-film by PLD, (c) macro-island formation by dilute HCl edge-dipping, (d) Al source/drain electrodes deposition.

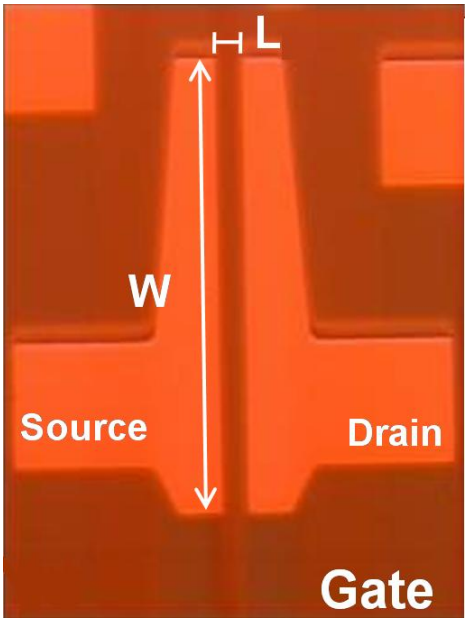


Figure 2.2 Top view of the common gate, inverted-staggered PLD a-IGZO TFT. W and L are TFT channel width and length, respectively.

laser deposition (PLD) from poly-crystalline $InGaZnO_4$ ceramic target [40]. The KrF excimer laser (λ=248nm) was used and the laser energy density was set at 2 J/cm^2 per pulse. The substrate was placed in an ultra-high vacuum system where the target-to-substrate distance is 3 cm and the deposition was done in an oxygen atmosphere (~ 8 Pa) without any intentional substrate heating. Before the source/drain (S/D) electrodes deposition, a macro-island was formed by edge-dipping/etching of the substrate in dilute HCl solution (0.1M). The 50nm thick aluminum (Al) S/D electrodes were deposited through fine pitch stencil mask openings by thermal evaporation. (It should be noticed that TFTs with 60nm thick of gold (Au) as S/D electrodes were also fabricated and exhibited a similar electrical properties.) Finally, the device was thermally annealed in air at 300˚C for 5 minutes. Figure 2.2 shows top view of such device used in this study.

2.1.2 Common gate, radio frequency (RF) sputter a-IGZO TFT

Although the previous TFT structure is easy to fabricate, the macro-island approach inevitably suffers from the loss of channel current confinement. In addition, when a positive gate bias is applied, the entire a-IGZO layer becomes highly conductive and can cause a significant amount of leakage current through gate if the dilute HCl edge etching cannot remove the a-IGZO completely. Therefore, to improve the TFT performance, an active island patterned at individual device level is necessary.

Figure 2.3 illustrates how such device structure was fabricated [48]. Similar to the process steps discussed in Section 2.1.1, a heavily P-doped (n^{++}) silicon wafer and a 100nm thermal SiO_2 layer was also used as a gate electrode and a gate insulator, respectively. A 20nm thick a-IGZO active layer was than deposited on the unheated substrate by RF magnetron sputtering from a poly-crystalline $InGaZnO_4$ target. The film was deposited in

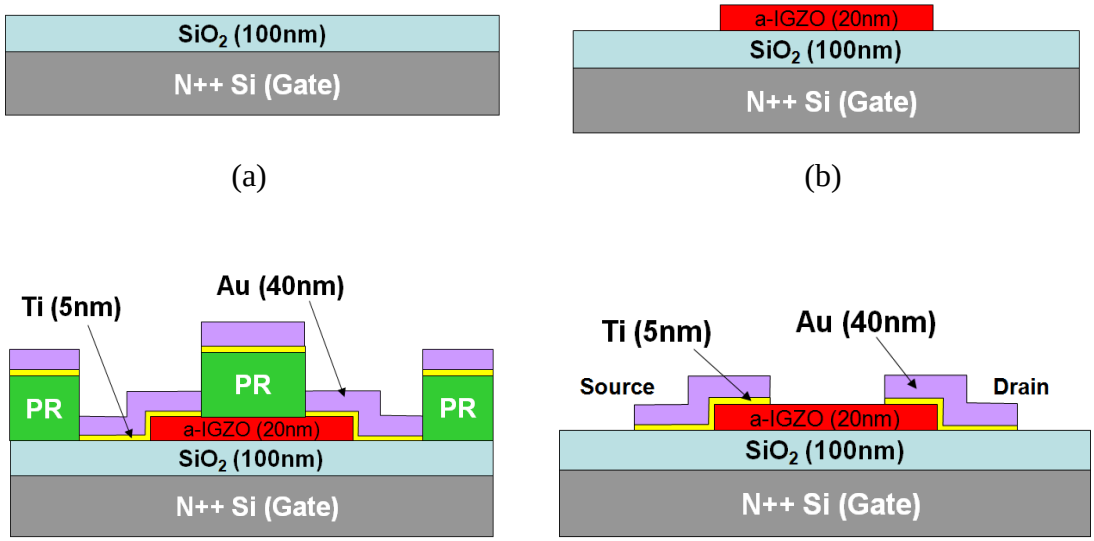


Figure 2.3 Process flow for making the common gate, inverted-staggered RF sputter a-IGZO TFT: (a) wafer cleaning, (b) depositing the a-IGZO layer (20nm) by RF magnetron sputtering and patterning the active island, (c) photoresist (PR) patterning and blanket deposition of Au/Ti stack layers (40/5 nm thick), (d) stripping off the photoresist.

the mixtures of Ar and O_2 gases under a total pressure of 0.5Pa with an O_2 partial pressure of 25mPa. The a-IGZO active island was patterned by a diluted HCl wet-etching process (Figure 2.3(b)) and then thermally annealed at 300˚C for 20min in air. Finally, the S/D electrodes were patterned by the lift-off technique: first, as shown in Figure 2.3(c), the photoresist is patterned by photolithography and followed by a blanket deposition of gold/titanium (Au/Ti) stacked layer (40/5 nm thick); then, the photoresist is stripped off and "lift-off" the unwanted Au/Ti material except S/D electrodes (Figure 2.3(d)).

2.1.3 Defined gate, radio frequency (RF) sputter a-IGZO TFT

To practically utilize a-IGZO TFTs in circuit application, the defined gate rather than common gate TFT should be adopted. The cross-sectional view of the defined gate, RF

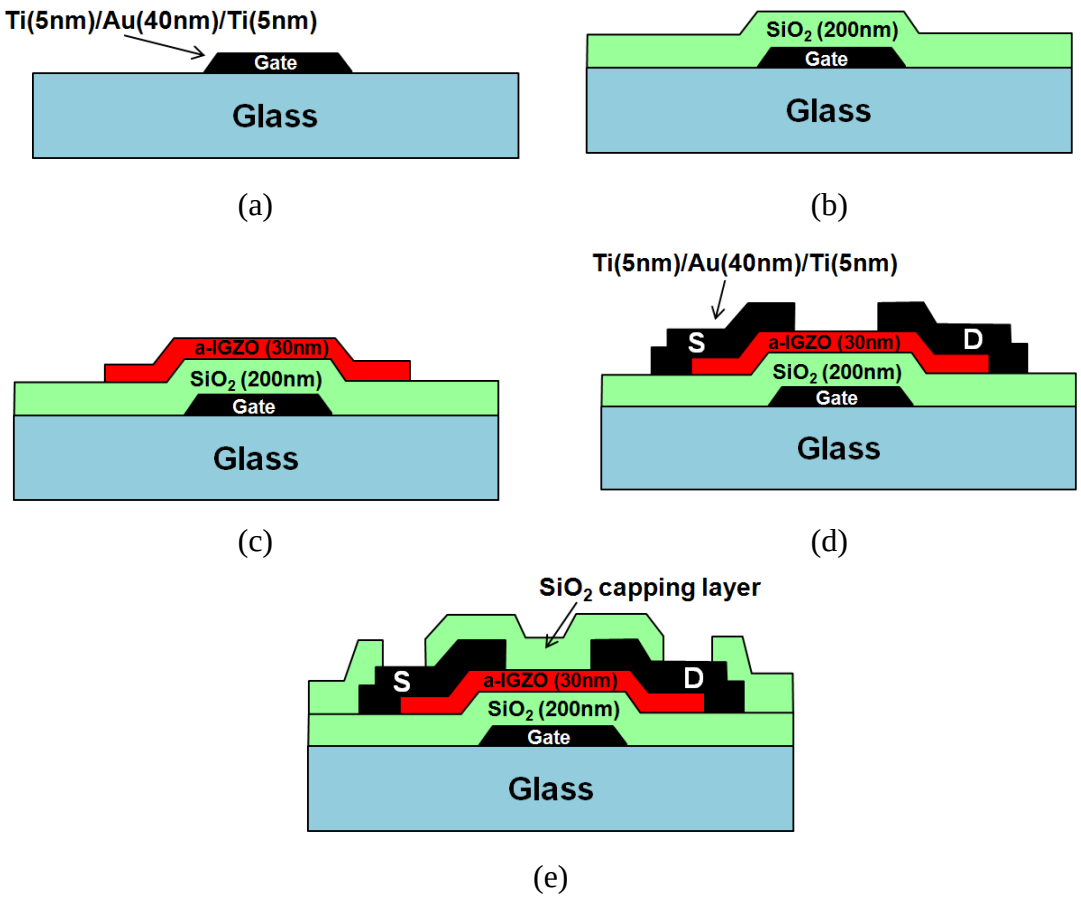


Figure 2.4 Process flow for making the define gate, inverted-staggered RF sputter a-IGZO TFT: (a) gate electrode definition, (b) gate insulator (200nm of SiO_2) deposition, (c) a-IGZO (30nm) deposition and active island patterning by wet etching, (d) S/D electrodes definition (lift-off), (e) capping layer (100nm of SiO_2) deposition. The contact holes are made by buffer HF etching.

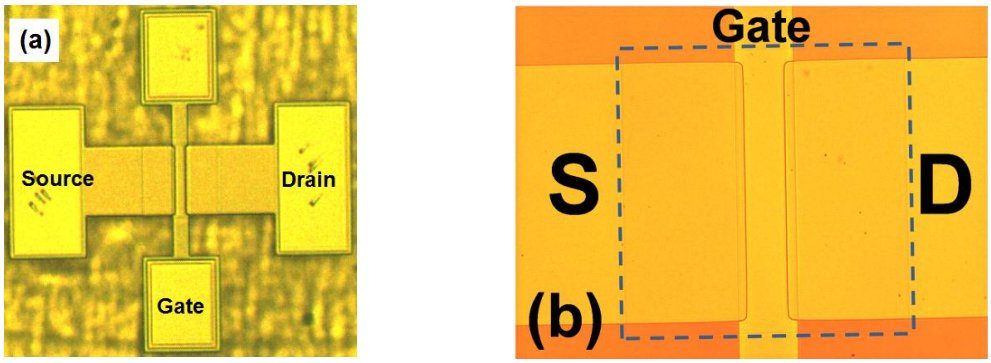


Figure 2.5 (a) Top view of the defined gate, RF sputter a-IGZO TFT. (b) A zoom-in view of the TFT channel area. The dash square indicates the region of a-IGZO active layer.

sputter a-IGZO TFT used in this study along with its process overview are portrayed in Figure 2.4. The detail processing steps were also discussed elsewhere [49]. The TFT has an inverted-staggered bottom-gate structure. The Ti (5nm)/Au (40nm)/Ti (5nm) stacking layers are used for gate and source/drain (S/D) electrodes. In addition, these metal electrodes are patterned by the lift-off technique. The SiO_2 gate insulator and a-IGZO active layer is about 200nm and 30nm thick, respectively. Both layers are deposited by RF magnetron sputtering. After the island formation and S/D electrodes definition, an additional sputter SiO_2 capping layer is added which serves as a protection layer for the TFT back channel. Finally, a thermal annealing step (200˚C, 1 hour in air) is applied. The die photo (top view) of the final RF sputter a-IGZO TFT is shown in Figure 2.5.

2.2 Basic TFT Electrical Properties

2.2.1 Common gate, PLD a-IGZO TFT electrical properties

Electrical measurements of the TFT were carried out with a probe station system located in a light tight box. The transistor electrical properties were measured by a PC controlled Agilent 4156C semiconductor parametric analyzer. The output characteristics of the common gate, PLD a-IGZO TFT (used Al S/D electrodes) under various gate to source voltages (V_{GS}) ranging from 4~20V are shown in Figure 2.6(a). During each measurement, the drain to source voltage (V_{DS}) was varied from 0~20V. A very clear distinction between linear and saturation region is obtained. This suggests that less than 20V of drain voltage (V_{DS}) is adequate for operating a-IGZO TFT active-matrix arrays. The TFT source/drain property is another important aspect for TFT evaluation. A non-ohmic source/drain contact, improper active layer thickness (too thick) and high bulk density-of-states (DOS) can all

cause TFT to have a non-linear drain current (I_D)/ V_{DS} behavior, also called "current crowding", at low V_{DS} [7, 50]. Figure 2.6(b) shows the output characteristics near the origin (V_{DS}=0~1V) and there is no current crowding observed in a-IGZO TFT. The absence of current crowding can be better appreciated by plotting the derivative of the output curves ($\delta I_D/\delta V_{DS}$) which is also shown in Figure 2.6(b). These properties are highly desirable for a-IGZO TFT to be used in active-matrix arrays.

Figure 2.7(a) illustrates the linear region (V_{DS}=0.1V) transfer characteristics of the common gate, PLD a-IGZO TFT. We extracted the threshold voltage (V_{th}) and field effect mobility (μ_{eff}) based on the standard MOSFET equation (with $V_{DS} << V_{GS}-V_{th}$):

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \cong \mu_{eff} C_{ox} \frac{W}{L}(V_{GS} - V_{th})V_{DS} \quad , \tag{2-1}$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are TFT channel width and length, respectively. The straight line in Figure 2.7(a) represents the best linear fit of (2-1) between 90% to 10% of the maximum I_D (at V_{GS}=12V) and the V_{th} and μ_{eff} are determined to be 1.92V and 7.3cm^2/Vs, respectively. It is worth to notice that the extracted μ_{eff} for a-IGZO TFT is much higher than the normal values reported for a-Si:H TFT. This experimentally justifies the unique metal ion's *ns* orbital conduction scheme in a-IGZO, which has been discussed in Section 1.1.3.

The subthreshold swing (S) was also extracted at the maximum slope point (V_{GS}=0V) from the subthreshold region data (Figure 2.7(b)), using the following equation:

$$S = \left(\frac{\delta \log(I_D)}{\delta V_{GS}}\right)^{-1} \quad . \tag{2-2}$$

The S for our PLD a-IGZO TFT is as low as 270mV/decade. Such value is compatible or even superior than a-Si:H TFT. This ensures a fast TFT response and also reduces the

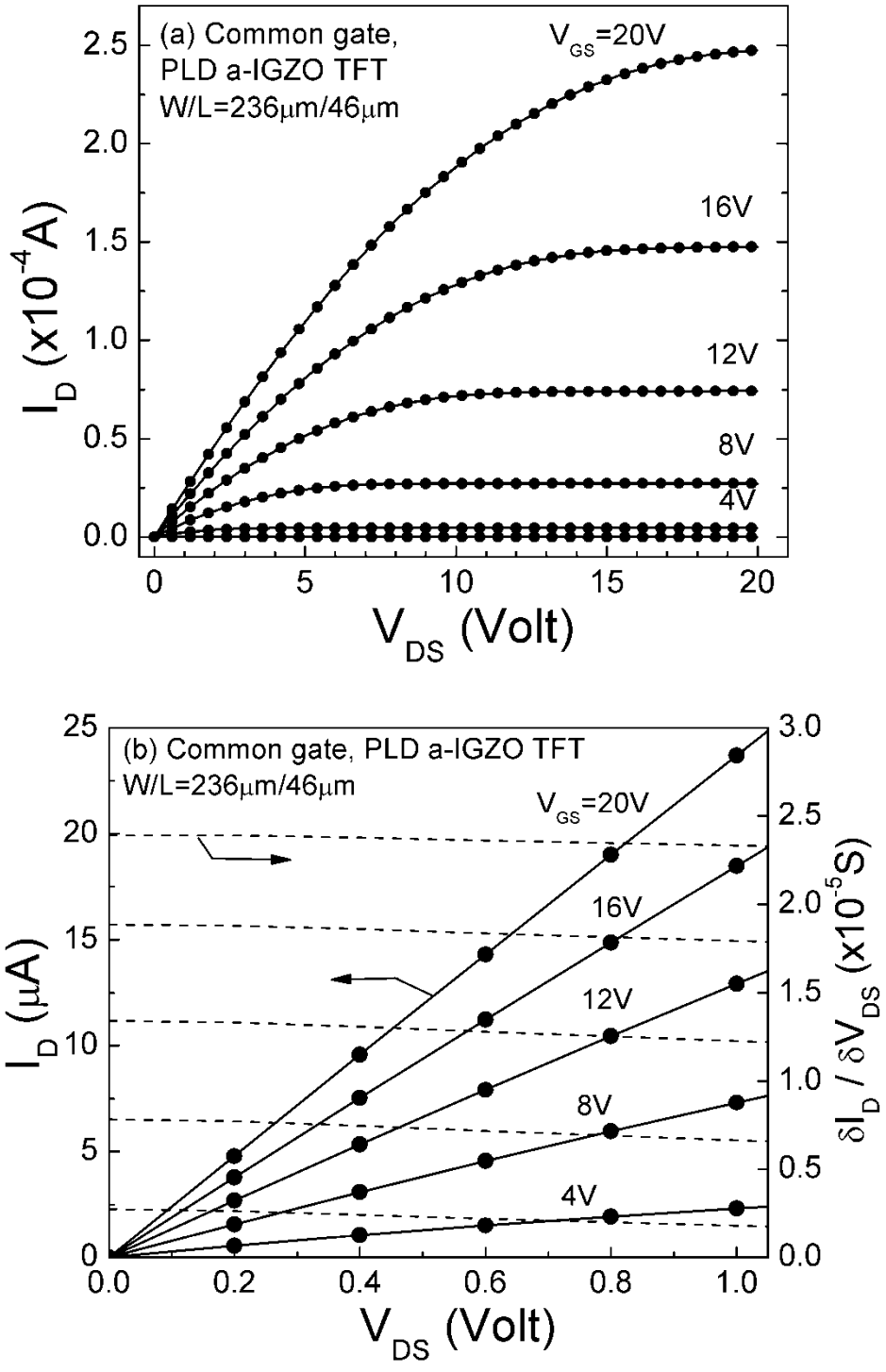


Figure 2.6 (a) Output characteristics of the common gate, PLD a-IGZO TFT (with Al S/D electrodes). (b) A zoom-in plot of the output characteristics (solid curves with symbols) near the origin (V_{DS}=0~1V); derivatives of I_D vs. V_{DS} characteristics ($\delta I_D / \delta V_{DS}$, dash curves) are also shown.

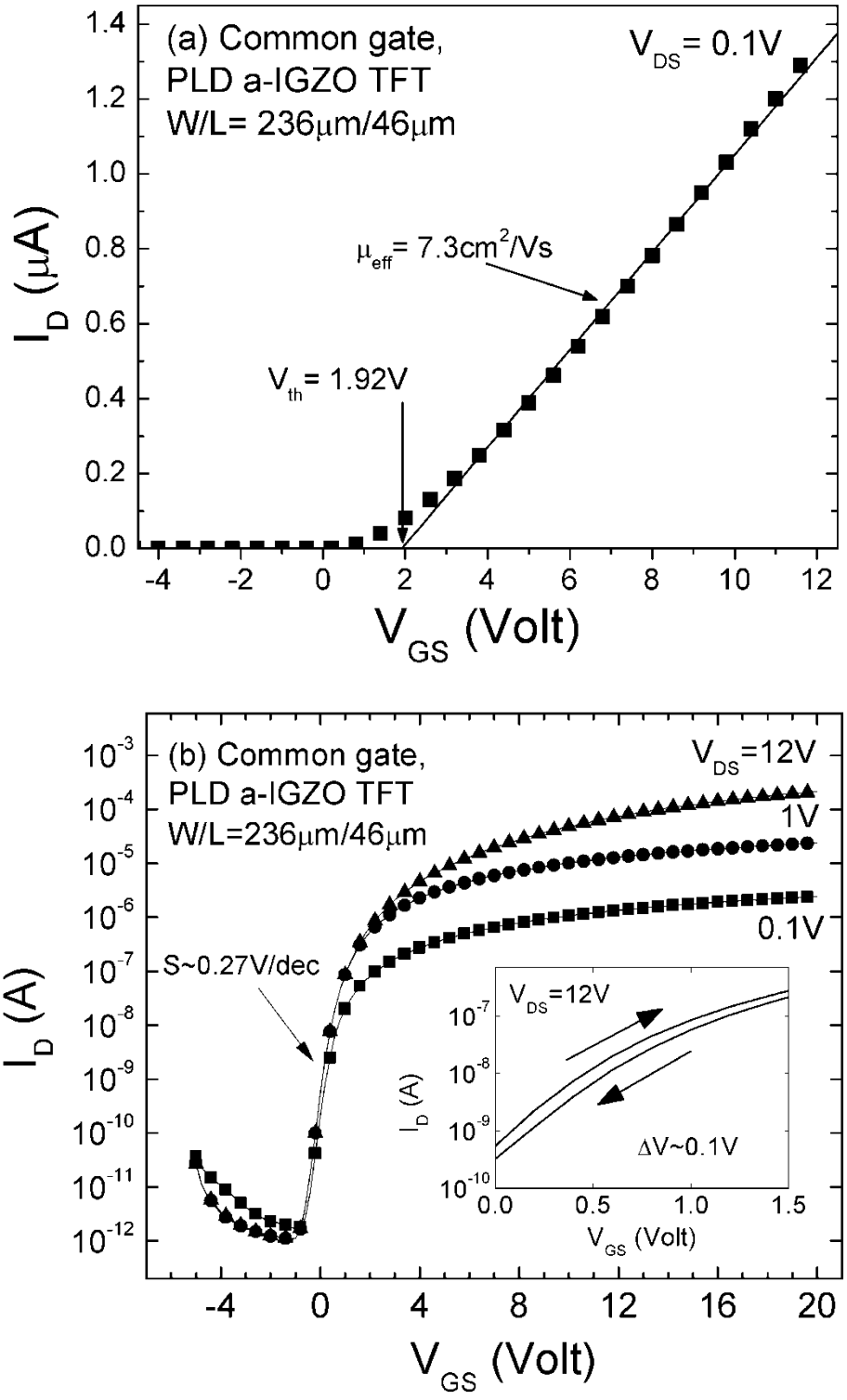


Figure 2.7 Transfer characteristics of common gate, PLD a-IGZO TFT in (a) linear plot and (b) semi-log plots. (Inset, b) The TFT hysteresis measured at V_{DS}=12V; ΔV is the shift in subthreshold properties.

voltage of the gate driving signal. The TFT off-state drain current (I_{D_off}) can be as low as 10^{-12}A. Although an increase in I_{D_off} is observed when a larger negative V_{GS} is applied (i.e. -1~ -5V), this shouldn't be associated with hole-current conduction. Rather, we believe it is due to the capacitance loading during measurement or the lack of confinement to channel current. The I_{D_off} (and also on/off current ratio) are expected to be further improved by incorporating active island in each individual transistor and this will be discussed in the next section.

2.2.2 Common gate, RF sputter a-IGZO TFT electrical properties

The electrical properties of common gate, RF sputter a-IGZO TFT were evaluated. Unlike the PLD a-IGZO TFT, this type of device has active island fabricated at individual TFT level and the detail processing steps were discussed in Section 2.1.2. The measured output and transfer properties are shown in Figure 2.8 and 2.9, respectively. The derivative of the output curves near origin [$\delta I_D/\delta V_{DS}$, Figure 2.8(b)] is highly linear without any local maximum or "hump" and it suggest the Ti (Au / Ti stacked layer is used for S/D electrodes) is making a good ohmic contact with a-IGZO.

Beside the evaluation on output curves, other key TFT parameters were also extracted from the transfer curves, following the same methodology depicted in previous section and these parameters were listed in Table 2.1 along with the parameters of PLD a-IGZO TFT. We found the RF sputter a-IGZO TFT can reach the μ_{eff} of 12.29 cm^2/Vs, which is about 68% higher than the value of PLD TFT. In addition, the S for RF sputter TFT (130 mV/decade) is only about half of the PLD TFT value. Based on these observations, we suspect the a-IGZO sputtering and/or subsequent post thermal annealing conditions are better optimized leading to improve a-IGZO film properties. (We also found that

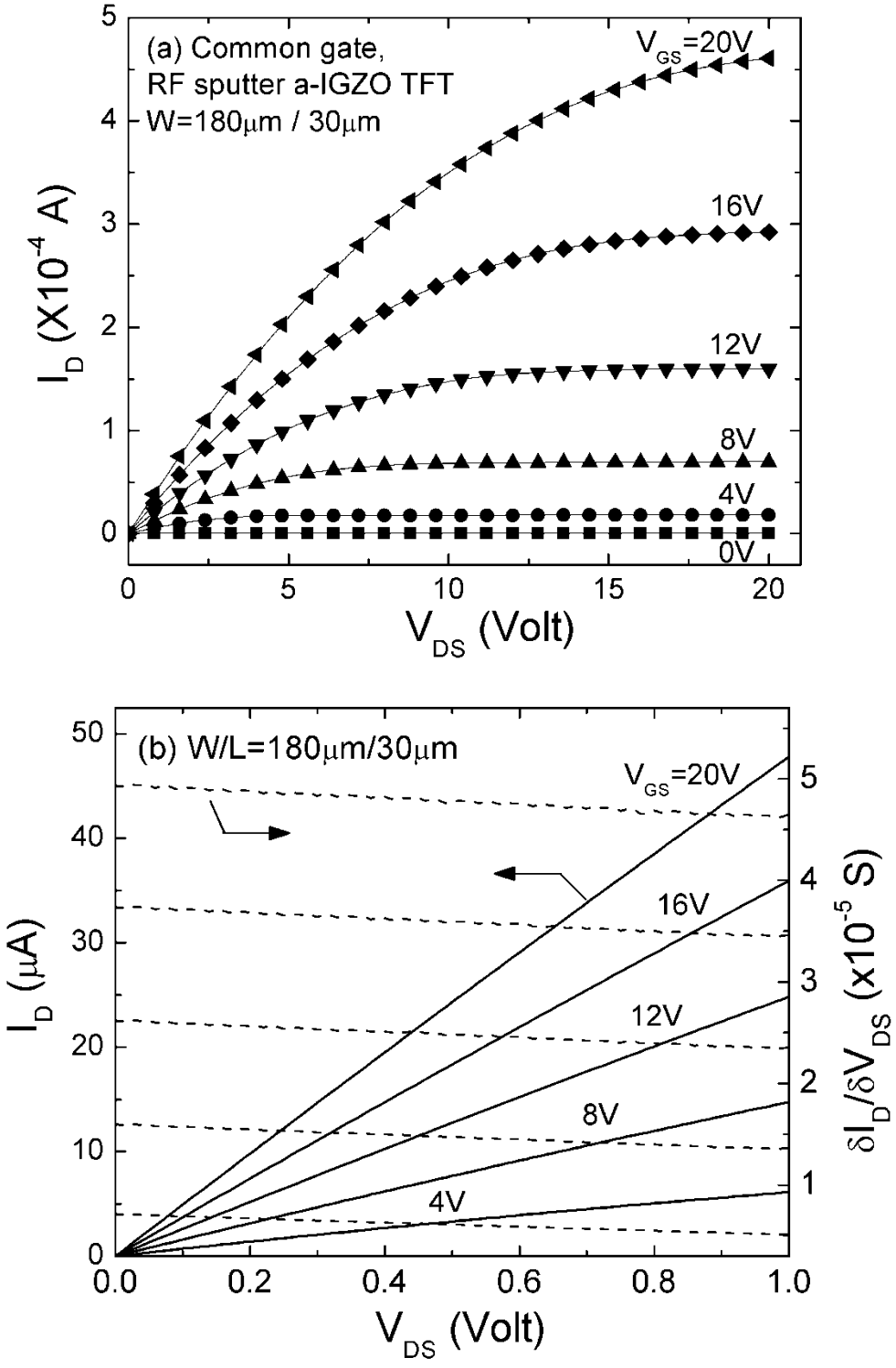


Figure 2.8 (a) Output characteristics of the common gate, RF sputter a-IGZO TFT. (b) A zoom-in plot of the output characteristics (solid curves) near the origin (V_{DS}=0~1V); derivatives of I_D vs. V_{DS} characteristics ($\delta I_D / \delta V_{DS}$, dash curves) are also shown.

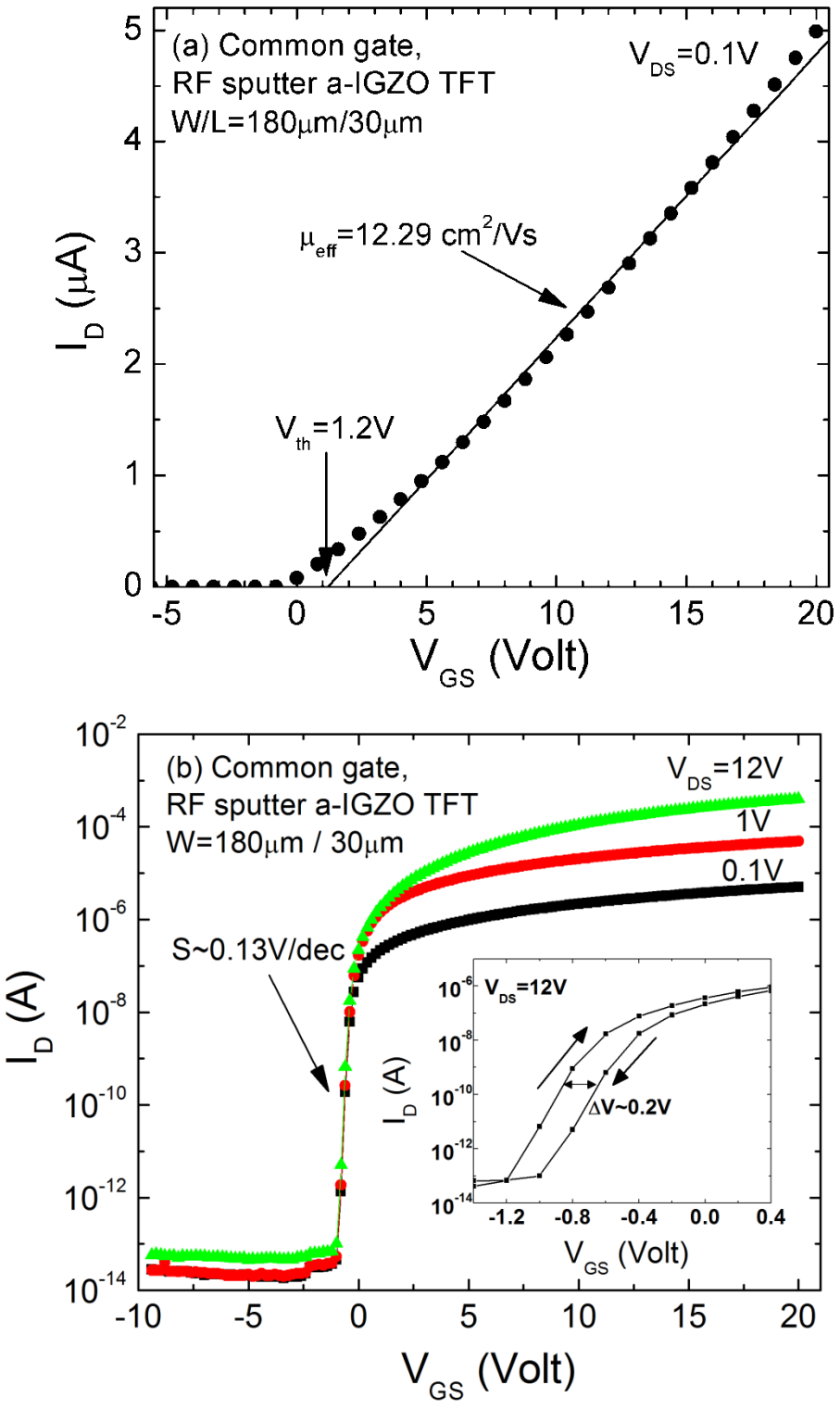


Figure 2.9 Transfer characteristics of common gate, RF sputter a-IGZO TFT in (a) linear plot and (b) semi-log plots. (Inset, b) The TFT hysteresis measured at V_{DS}=12V; ΔV is the shift in subthreshold properties.

Parameters	**μ_{eff} ***	**V_{th} ***	**S**	**I_{D_off}**	**ΔV**	**On/off ratio ****
Unit	cm^2/Vs	V	mV/decade	A	V	
PLD a-IGZO TFT (W/L=236μm/46μm, 50nm Al S/D Electrodes)						
Value	7.3	1.92	270	10^{-11}~10^{-12}	0.1	10^8
RF Sputter a-IGZO TFT (W/L=180μm/30μm, Au(40nm)/Ti(5nm) S/D Electrodes)						
Value	12.29	1.2	130	~10^{-14}	0.2	10^{10}

* Extracted by 90%-10% method.

** "On/off ratio" is the drain current ratio between on and off states.

Table 2.1 Typical electrical properties of common gate a-IGZO TFTs.

the thinner a-IGZO film thickness can reduce S/D series resistances, which will be discussed in Chapter 3.) All our a-IGZO TFTs (including defined gate device) have very small I/V hysteresis (ΔV<0.2V), which suggests that the gate oxide charges (e.g. mobile ions or oxide traps) are kept at a minimum level. The oxide charge density may be estimated by $Q_{ox}= C_{ox}\Delta V$ and for our devices, $Q_{ox}/q < 4.3\times10^{10}$ cm^{-2}.

The advantage of making TFT active island becomes more clear when the I_{D_off} and on/off drain current ratio between these two device structures are compared. Because the definition of the TFT active islands defines the current path to be located between their S/D electrodes, it suppresses the unwanted device current leakage. The I_{D_off} of RF sputter a-IGZO TFT can be as low as 10^{-14}A; that is two to three orders of magnitudes lower than PLD TFT (which only has macro-island) values. The low I_{D_off} in RF sputter TFT may also partially attribute to the low oxygen vacancy in a-IGZO film. However, it is unlikely due to the active layer thickness effect, because the a-IGZO layer in PLD TFT is only twice as thick as the layer in RF sputter TFT. Primarily because of the reduction in I_{D_off} , the on/off ratio of RF sputter a-IGZO TFT is also about two orders higher than the PLD TFT. We

didn't observe any dependence of I_{D_off} on V_{GS} and there is no appreciable increase in I_{D_off} with V_{GS} down to -20V (data not shown). The observed constant I_{D_off} (10^{-14}A) over a wide negative V_{GS} range implies the lack of hole-current conduction in TFT off region. It also supports the idea of a-IGZO being n-type semiconductor with electron as majority carrier and very low hole mobility.

2.2.3 Defined gate, RF sputter a-IGZO TFT electrical properties

The electrical properties of defined gate, RF sputter a-IGZO TFT are provided in this section. This device has a bottom gate, inverted staggered structure with individual gate electrode patterned. TFT cross-section and top views were provided in Figure 2.4 and 2.5, respectively. The output characteristics were first evaluated (Figure 2.10). Similar to the common gate a-IGZO TFTs, a 20V of gate and drain voltage is also sufficient to operate the defined gate TFT since Figure 2.10(a) shows a clear transition between linear and saturation regions. Because the defined gate TFT also uses the Ti as contact metal to the a-IGZO layer, the near origin I_D vs. V_{DS} curves (Figure 2.10(b)) are free from current crowding as expected.

Figure 2.11(a) illustrates the transfer characteristics of defined gate, RF sputter a-IGZO TFT. We extracted the V_{th} and μ_{eff} based on the standard MOSFET equation in both linear region (V_{DS}=0.1V) and saturation region (V_{DS}=20V). Readers can refer to (2-1) for the linear region equation, while the saturation region equation is written as follow:

$$\left(I_D\right)^{1/2} = \left[\mu_{eff} C_{ox}\left(\frac{W}{2L}\right)\right]^{1/2}\left(V_{GS} - V_{th}\right) \ , \tag{2-3}$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are TFT channel width and length, respectively. The straight lines in Figure 2.11(a) represent the best linear fits of

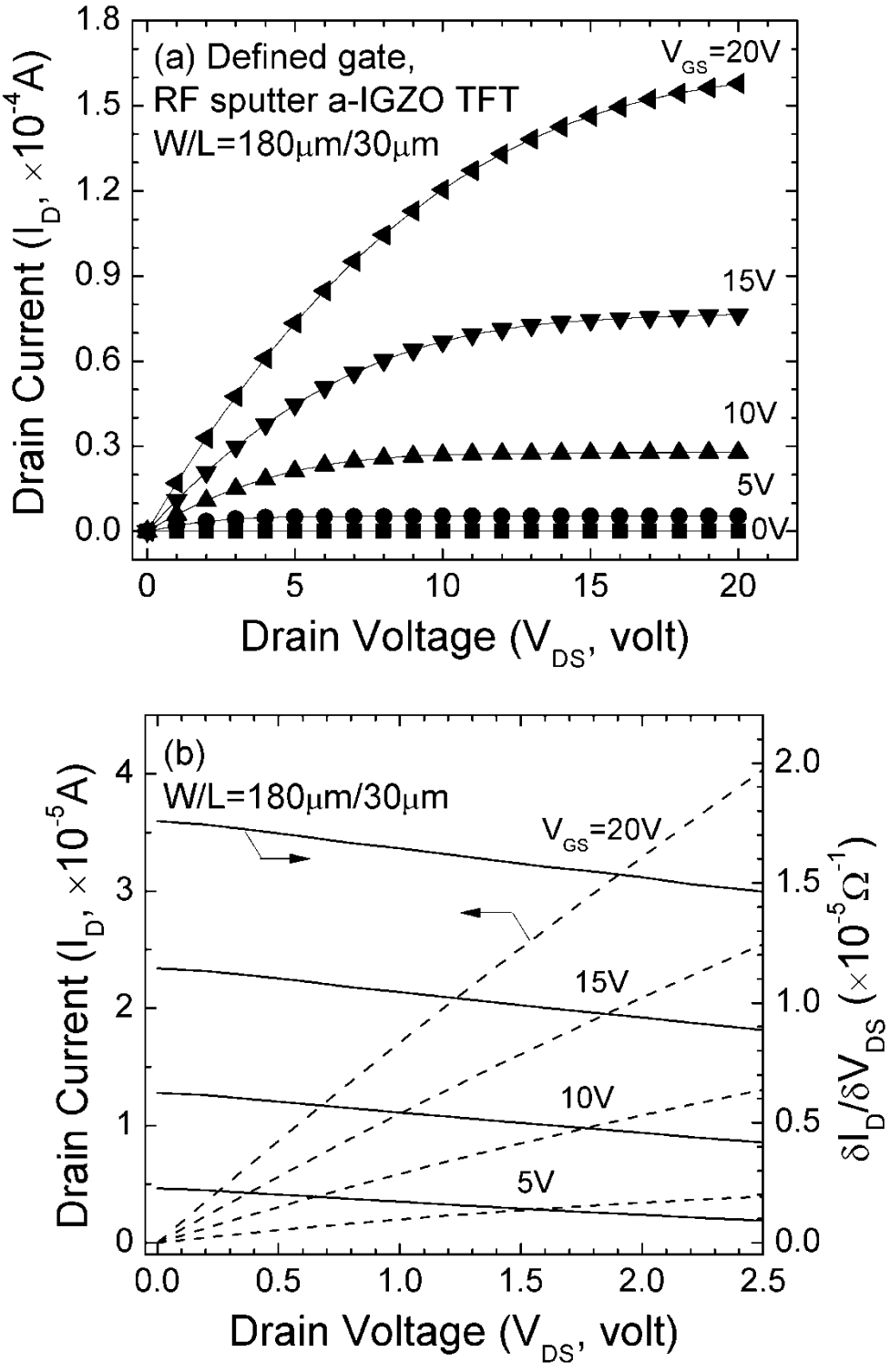


Figure 2.10 (a) Output characteristics of the defined gate, RF sputter a-IGZO TFT. (b) A zoom-in plot of the output characteristics (solid curves) near the origin (V_{DS}=0~2.5V); derivatives of I_D vs. V_{DS} characteristics ($\delta I_D / \delta V_{DS}$, dash curves) are also shown.

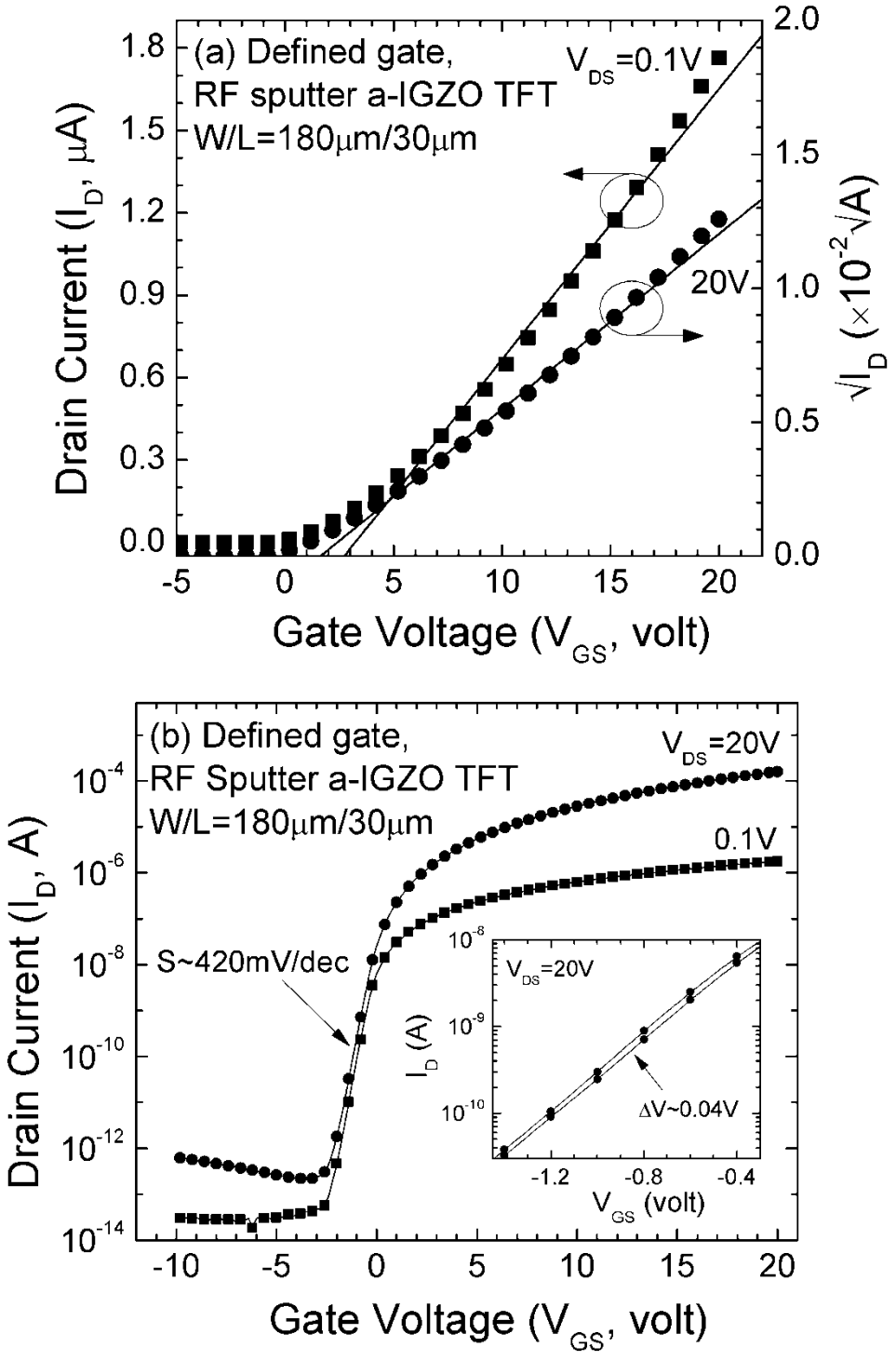


Figure 2.11 Transfer curves of defined gate, RF sputter a-IGZO TFT in (a) linear and (b) semi-log scales. (Inset, b) The TFT hysteresis measured at V_{DS}=20V; ΔV is the shift in sub-threshold properties. Symbol (•) and (■) represent the saturation (V_{DS}=20V) and linear (V_{DS}=0.1V) region properties, respectively.

Parameter	Unit	Value (region)	
μ_{eff}*	cm^2/Vs	Linear	9.51
		Saturation	8.3
V_{th}*	V	Linear	3.23
		Saturation	1.63
S	mV/decade	420	
I_{D_off}	A	$< 10^{-12}$	
ΔV	V	0.04	
On/off ratio**		$\sim 10^8$	

* Extracted by 90% - 10% method.

** "On/off" ratio is the drain current ratio between on and off states.

Table 2.2 Electrical properties of defined gate, RF sputter a-IGZO TFT.

(2-1) and (2-3) between 90% to 10% of the maximum I_D (or $(I_D)^{1/2}$) at V_{GS} = 20V. It should be noticed that there is a deviation from ideal MOSFET (linear) behavior at higher V_{GS}. Section 3.2 will discuss this non-ideal effect in more detail. The S was also extracted at the maximum slope point (V_{GS}= -1.4V) from the sub-threshold region data (Figure 2.11(b)), using (2-2). The S for the defined gate, RF sputter a-IGZO TFT is around 420 mV/decade. In case of the a-Si:H TFT, the subthreshold swing can be associated with the density of deep bulk states (N_{BS}) and interface states (N_{SS}) at the interface between gate insulator and semiconductor layers by the following formula [51]:

$$S = \frac{kT}{q\log(e)}\left[1+\frac{qd_{ins}}{\varepsilon_{ins}}\left(\sqrt{\varepsilon_{semi}\,N_{BS}}+qN_{SS}\right)\right], \qquad (2\text{-}4)$$

where k, T, and q are the usual physical parameters; ε_{ins} (= $n_{ins}\varepsilon_0$) and ε_{semi} (= $n_{semi}\varepsilon_0$) are permittivity in gate insulator and semiconductor, respectively; d_{ins} is the effective thickness

of the insulator; ε_0 is the permittivity in vacuum; and n_{ins} and n_{semi} are dielectric constants for gate insulator and semiconductor, respectively. If we assume the similar situation also occur in a-IGZO TFT, the bulk states of the a-IGZO active layer can be approximately estimated by considering a sole contribution from bulk states in (2-4) (set N_{SS}=0). With the S of 420mV/decade and the dielectric constant for a-IGZO (n_{semi}) of 10, we calculated the N_{BS} to be around 7.7×10^{16} $eV^{-1}cm^{-3}$. This value is consistent with the density extracted by SPICE modeling [52] and from a-IGZO TFT made by pulse-laser deposition (PLD) (to be discussed in Chapter 4) [53].

Table 2.2 summarizes all key TFT properties. Although the average μ_{eff} (8~9 cm^2/Vs) for the defined gate, RF sputter a-IGZO TFT is not as good as its common gate counterpart, the performance is still superior than typical a-Si:H TFT value (~0.8cm^2/Vs). The S (420 mV/decade) is also larger than the values we measured from common gate TFTs (100~300 mV/dev), which use thermal oxide as gate insulator. It is known that, if SiO_2/a-IGZO interface traps are present, the variation of TFT surface potential with gate voltage becomes slower, and this effect results in a higher S. We can estimate the maximum interface defect states density ($N_{SS}^{\max}$) from S by assuming N_{BS}=0 in (2-4):

$$N_{SS}^{\max} = \left(\frac{S \log(e)}{kT/q} - 1 \right) \frac{C_{ox}}{q^2}. \qquad (2\text{-}5)$$

The $N_{SS}^{\max}$ values for RF sputter common gate and defined gate TFTs are 2.5×10^{11} $eV^{-1}cm^{-2}$ and 6.5×10^{11} $eV^{-1}cm^{-2}$, respectively. Therefore, we suspect the sputter SiO_2 used in the defined gate, RF sputter TFT may contain excess interfacial defects and its quality should be further optimized to improve device properties.

We also measured the defined gate, RF sputter TFT I_{D_off} down to V_{GS}= -10V. The I_{D_off}

is independent of V_{GS} but is proportional to V_{DS}. During drain current measurement, the V_{DS} was changed from 0.1V to 20V, and a 1.5 orders of magnitude increase in I_{D_off} was observed (Figure 2.11(b)). There is also a small negative shift (~0.2V) in TFT subthreshold transfer curves between V_{DS}=0.1V and 20V (Figure 2.11(b)), which is associated with the increase of I_{D_off}. Nonetheless, all I_{D_off} values are below 10^{-12}A, which is suitable for circuit operation. Moreover, TFT on/off ratio is maintained at 10^{8} for both linear and saturation region. This indicates the film resistivity of a-IGZO is well under controlled during deposition [41].

Chapter 3

Advanced Analysis of the a-IGZO TFT Electrical Properties

3.1 a-IGZO TFT Source/Drain Series Resistances

3.1.1 Transmission line analysis of a-IGZO TFT

A thorough analysis on a-IGZO TFT should also include the extraction of channel length bias and TFT source/drain (S/D) series resistances. In this dissertation, the term "channel length (L)" is defined as the physical distance between the inner edges of S/D electrodes, as illustrated in Figure 2.2. This definition complies with the common expectation from the device design point of view but may fail to capture the actual scheme of device operation. The actual channel current cannot be collected by S/D contacts at the inner edges, but its path needs to extend a distance under the S/D electrodes, which usually recognized as channel length bias (ΔL). Associated with the channel length bias, the S/D series resistance is another important factor that affects TFT operation. The simplest thought on the origin of S/D series resistance may just be the non-negligible contact resistance at the metal/semiconductor interface. However, in the case of inverted-staggered TFT, because the electron need to traverse through the bulk semiconductor layer from the accumulation channel, the total series resistance (R_0) is actually the combination of contact

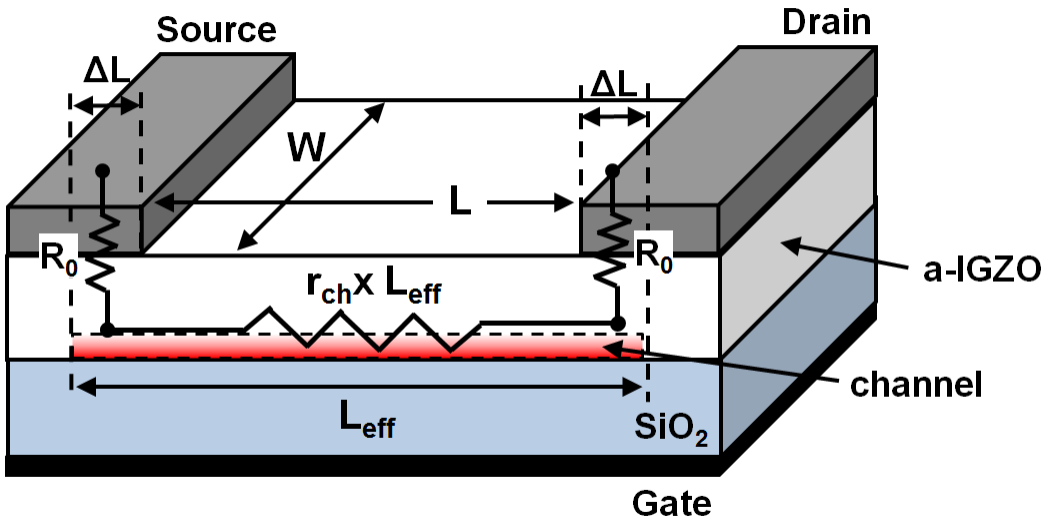


Figure 3.1 Physical origin of the resistance components in equation (3-1).

resistance and bulk semiconductor (e.g. the a-IGZO) resistance under the S/D electrodes [54].

Contributions from these two factors are integral parts of the measured TFT I-V properties and can't be separated from the output or transfer characteristics collected from a single transistor with a given L. Instead, both parameters can be extracted by the transmission line method (TLM) (also known as channel-resistance or current-voltage method). The development of such method can be traced back to late 70's, when Terada-Muta [55] and Chern *et al.* [56] proposed to extract the MOSFET effective channel length by measuring the channel resistance for a set of devices with different channel lengths. Kanicki *et al.* later on adopted this methodology and successfully implemented it in a-Si:H TFT analysis [7].

TLM theory assumes the total TFT on-resistance (R_T) measured at a low drain-source voltage can be broken down into the sum of S/D series resistances (R_0) and intrinsic TFT

channel resistance (Figure 3.1):

$$R_T \equiv \frac{V_{DS}}{I_D} = 2R_0 + r_{ch} \cdot L_{eff} \quad . \tag{3-1}$$

The r_{ch} is the channel resistance per unit length (Ω/μm) and can be written as:

$$r_{ch} = \frac{1}{\mu_{TLM} C_{ox} W \left(V_{GS} - V_{th\_TLM}\right)} \quad , \tag{3-2}$$

where μ_{TLM} and V_{th_TLM} are filed-effect mobility and threshold voltage associated with the intrinsic TFT (with no S/D series resistances). They are assumed to be constant, channel length (L) independent. (In fact, the theory also assumes that μ_{TLM} does not change with V_{GS}, an assumption which will be examined later in next section.) L_{eff} is the effective channel length, which takes the channel length bias (ΔL) into consideration:

$$L_{eff} = L + 2\,\Delta L \,. \tag{3-3}$$

Substituting (3-2) and (3-3) into (3-1), the R_T can be expressed as:

$$R_T \equiv \frac{V_{DS}}{I_D} = 2R_0 + \frac{L + 2\,\Delta L}{\mu_{TLM} C_{ox} W \left(V_{GS} - V_{th\_TLM}\right)} \quad . \tag{3-4}$$

It should be notice that for (3-4) to be valid, a low drain-source voltage (V_{GS}-V_{th} >> V_{DS}) must be applied during TFT linear region drain current measurements. In this study, a V_{DS} of 0.1V is used to comply with this requirement. In addition, because of the low drain bias, the space-charge-limited currents (SCLC) effect can be neglected [57].

Figure 3.2 illustrates how to use TLM to extract S/D series resistances (R_0) and channel length bias (ΔL). Linear region R_T data were first measured from a set of common gate PLD a-IGZO TFTs (Al S/D electrodes) and then they were plotted as a function of TFT channel length (L) for different gate voltage (V_{GS}=3~5V). All L values used in the extraction are determined by high resolution optical microscope. Therefore, the actual physical distances between source and drain electrodes are considered and any errors that might

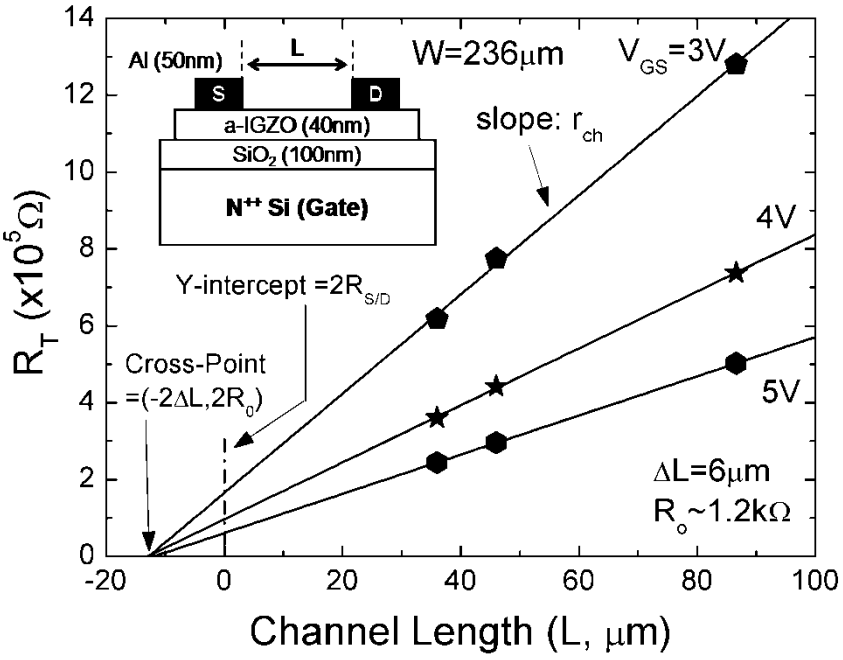


Figure 3.2 Illustration of the transmission line method (TLM). Symbol: experimental data, solid line: linear fit to the TLM model (3-4) or $R_{S/D}$ model (3-5). (Inset) Cross sectional view of the common gate, PLD a-IGZO TFT used in analysis.

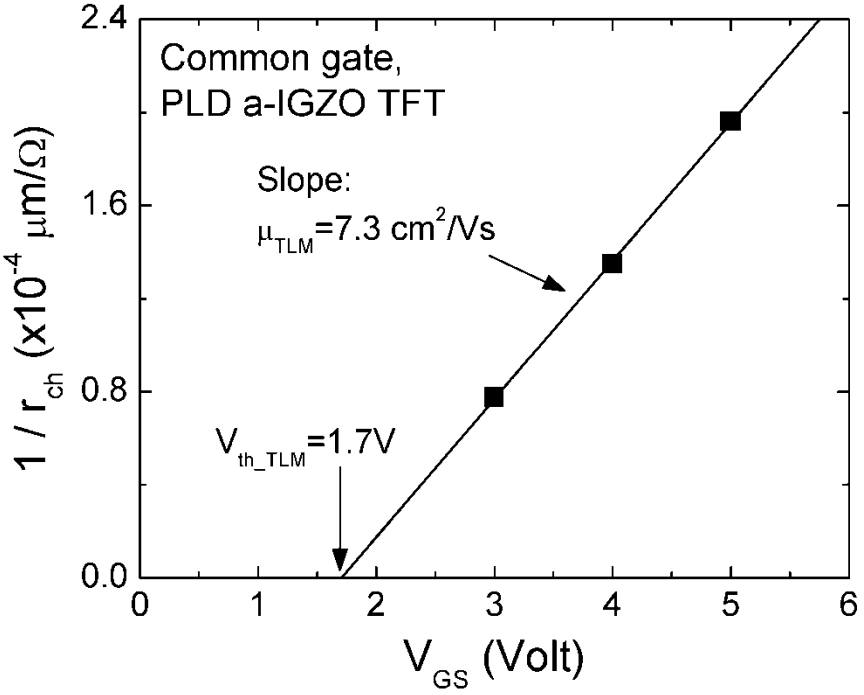


Figure 3.3 The evolution of $1/r_{ch}$ with TFT gate voltage (V_{GS}). The r_{ch} data are extracted from TLM analysis (Figure 3.2). Symbol: experimental data, solid line: linear fit to (3-2).

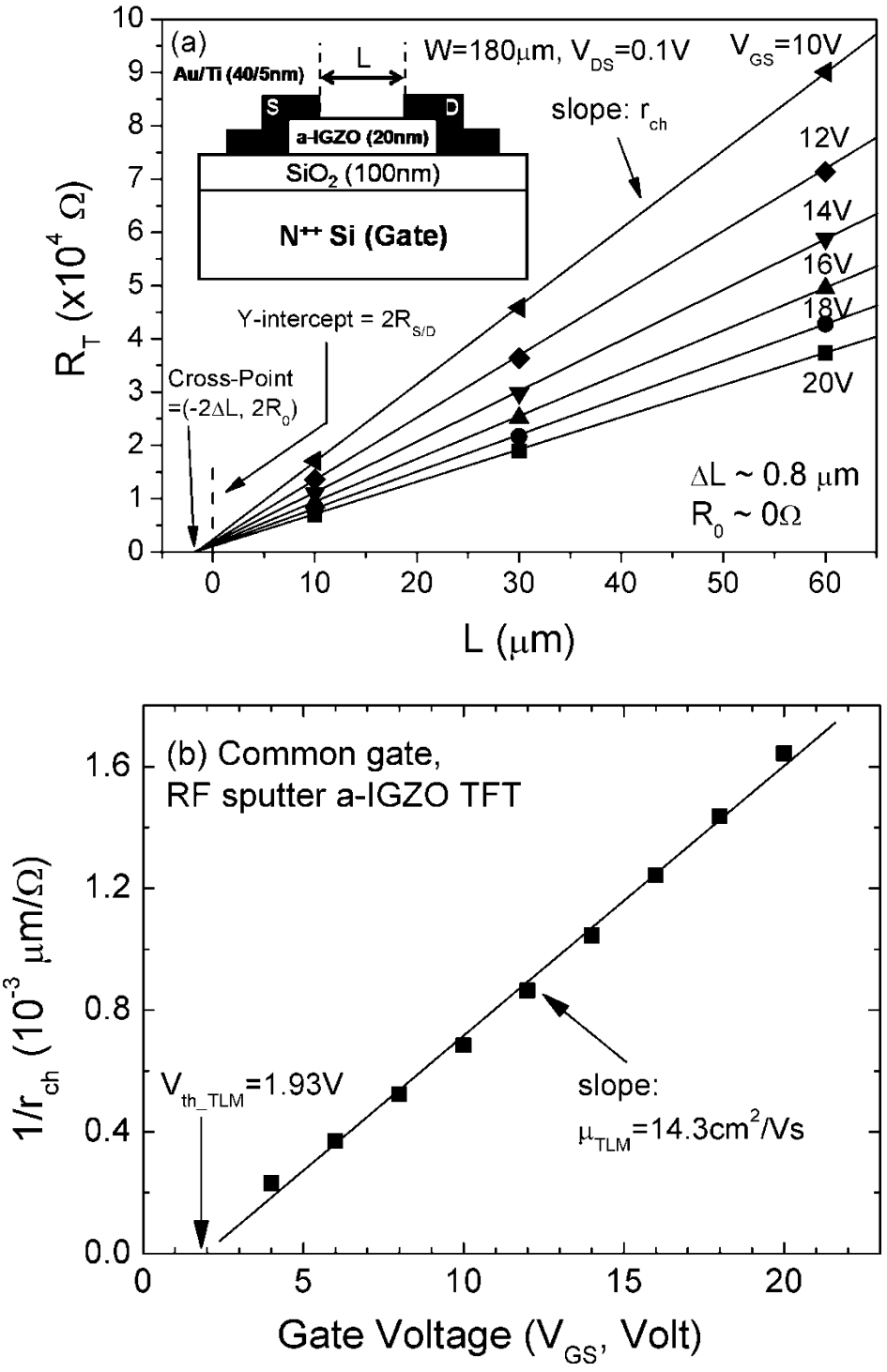


Figure 3.4 (a) TLM analysis of common gate, RF sputter a-IGZO TFTs. Symbol: experimental data, solid line: linear fit to the (3-4) or (3-5). (b) The evolution of $1/r_{ch}$ with V_{GS}. Symbol: experimental data, solid line: linear fit to (3-2). (Inset, a) The cross sectional view of the common gate, RF sputter a-IGZO TFT.

cause by the photolithography are excluded in the analysis. R_0 (~1.2kΩ) and ΔL (6μm) can be extracted from the cross-point which is extrapolated from multiple linear fits of (3-4) for different V_{GS}. The low R_0 indicates the S/D metal (Al) is forming a low resistance ohmic-like contact with a-IGZO. In comparison, R_0 of the a-Si:H TFT is usually on the order of 10^5~10^6Ω [54, 58, 59] If we assume the channel current is flowing through S/D electrodes in the specific area defined by W and ΔL (Figure 3.1). The R_0 might also be equally represented in the unit of specific contact resistance as 0.017Ω-cm^2. Nonetheless, this value consists of the contact and bulk semiconductor resistance and actual contact resistance should be lower than this value. For our a-IGZO TFT, the cross-point locates in the second (II) quadrant where $\Delta L > 0$. This is equivalent to say "$L_{eff} > L$", which experimentally supports the idea that the TFT channel current extends under S/D electrodes. Readers should not confuse this results with what is commonly found in MOSFET: because of the lateral implant straggle and the lateral source-drain diffusion in the fabrication process, the $L_{eff} < L_g$ (gate length) with MOSFET TLM cross-point usually locates in the first (I) quadrant of R_T vs. L_g plot [56].

The μ_{TLM} and V_{th_TLM} can also be extracted from r_{ch}, which is the slope of linear fit to (3-4) during TLM analysis. As shown in Figure 3.3, for common gate PLD a-IGZO TFTs, the μ_{TLM} and V_{th_TLM} are 7.3cm^2/Vs and 1.7V, respectively. These values are consistent with the basic electrical properties that have been discussed in Chapter 2.

We also made a similar analysis on common gate, RF sputter a-IGZO TFTs (Figure 3.4) [60]. The cross-point was extrapolated from data measured for V_{GS} ranging from 10~20V. For even lower V_{GS}, due to additional V_{GS} dependence of R_0 and ΔL, we observed a shift on the cross-point. Compare to PLD a-IGZO TFTs (Al S/D electrodes), much smaller parasitic values were extracted for RF sputter a-IGZO TFTs (Au/Ti S/D electrodes) with the

ΔL about 0.8μm and R_0 virtually undetectable. We suspect this improvement can be due to the reduction in a-IGZO thickness and/or better contact quality of the a-IGZO/Ti than a-IGZO/Al. The μ_{TLM} and V_{th_TLM} were further extracted to be 14.3cm^2/Vs and 1.93V, respectively (Figure 3.4(b)). The V_{th_TLM} is slight higher than V_{th} extracted from regular 90%-10% method (1.2V). This might not be consistent with the common expectation: the V_{th_TLM} supposes to be closer to the intrinsic threshold voltage, which tends to be over-estimated when S/D series resistance is not excluded. Such discrepancy might be explained by the following: (1) threshold voltages extracted by TLM and 90%-10% methods are based on different voltage ranges. TLM includes data points measured for a larger V_{GS}; (2) V_{th_TLM} is a weighting average of threshold voltages from multiple TFTs, not from single TFT. So a larger V_{th_TLM} may simply be due to sampling TFT that has threshold voltage slightly higher than others. To give a more consistent result, we expect a larger TFT sampling size will be necessary.

3.1.2 Gate voltage dependent series resistance ($R_{S/D}$)

In previous section, we have implicitly assumed the channel length bias and series resistance are V_{GS} independent and extracted them as ΔL and R_0, respectively. This assumption is in fact not accurate because the bulk a-IGZO resistivity is controlled by the gate bias. A more precise model should consider the gate voltage dependent S/D series resistance ($R_{S/D}$). Figure 3.5(a) is a closer look at the current flow near the source side where the channel current distributes itself within an active region while redirecting its flow "upward" toward the source electrode. This process is closely correlated with the bulk a-IGZO resistivity and in turn, the V_{GS}. Intuitively, the length (L_T, which is also called transfer length) that is required for current to transfer from channel to S/D electrodes

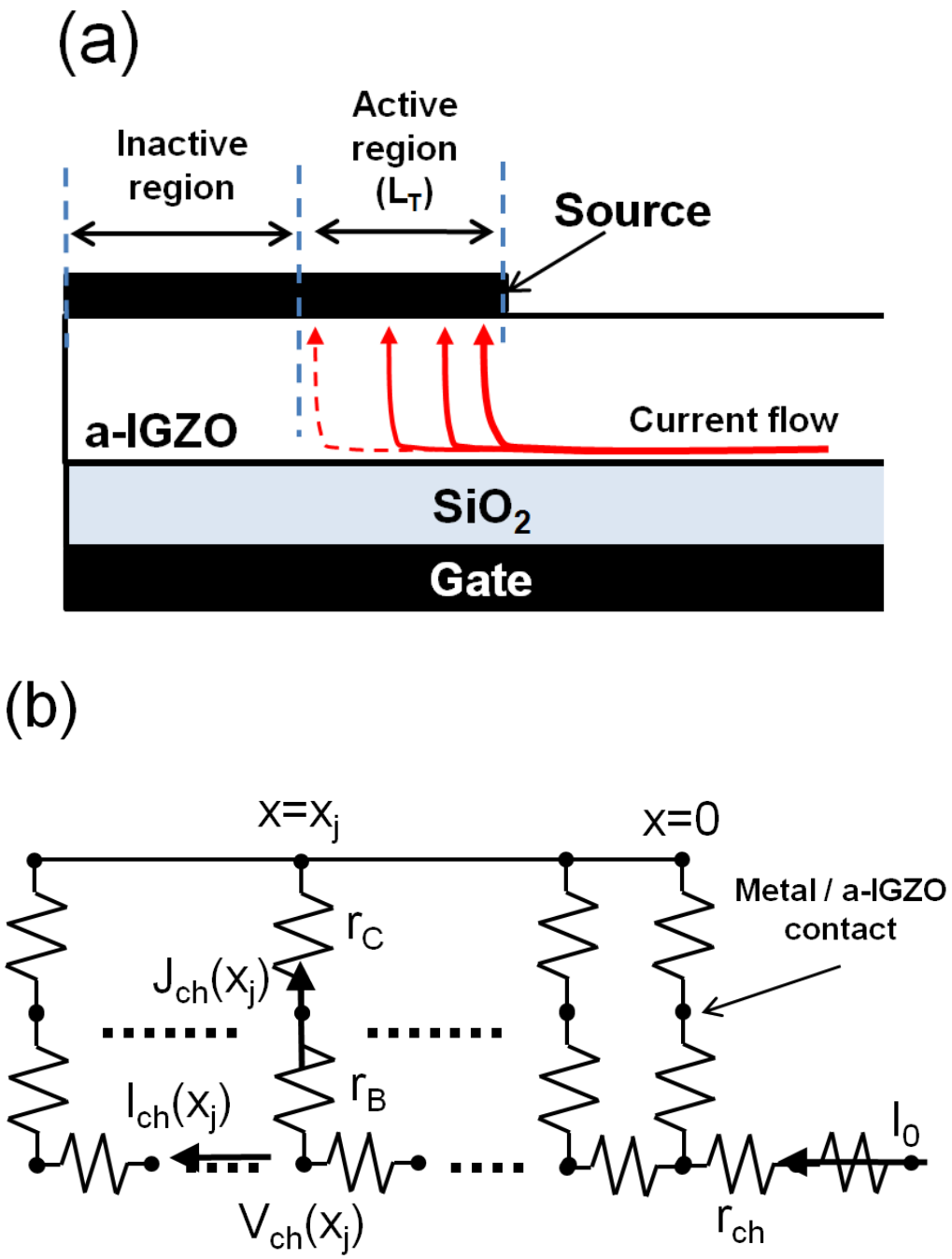


Figure 3.5 (a) Graphical representation of the transfer length (L_T) (adapted from [59]). (b) Equivalent circuit near the a-IGZO TFT source electrode (adapted from [54]). A distributed resistance network is chosen to model the current distribution under source electrode. I_0 is the total current. $I_{ch}(x)$ and $J_{ch}(x)$ are the horizontal current (unit: A) and the vertical current density (unit: A/cm^2) at position x, respectively. The origin of X-direction is set at the inner edge of source electrode.

should decrease with increasing V_{GS}. Because the L_T is an integral part of $R_{S/D}$, to derive the new model, the total TFT on–resistance (R_T) should be re-written as the sum of $R_{S/D}$ and intrinsic TFT channel resistance with length L (not L_{eff} as in (3-1)):

$$R_T = \frac{V_{DS}}{I_D} = 2R_{S/D} + r_{ch} \cdot L \quad . \tag{3-5}$$

Figure 3.5(b) shows the distributed circuit model used to derive the mathematical formula for analysis. The change of the horizontal channel current (I_{ch}) at position *x* under source electrode can be expressed as [54, 57]:

$$\frac{\delta I_{ch}(x)}{\delta x} = -W J_{ch}(x) \tag{3-6}$$

with

$$J_{ch}(x) = V_{ch}(x) \Big/ r_{Ceff} \tag{3-7}$$

and

$$r_{Ceff} \equiv r_B + r_C \quad . \tag{3-8}$$

In the above equations, W is the channel width; $J_{ch}(x)$ is the vertical current density at position *x*; $V_{ch}(x)$ is the voltage in the channel at position *x*; r_{Ceff} is the effective contact resistance and r_B and r_C are the vertical bulk and contact resistivity (unit: Ω-cm^2), respectively.

The change of $V_{ch}(x)$ along x direction can also be expressed as:

$$\frac{\delta V_{ch}(x)}{\delta x} = -I_{ch}(x) \cdot r_{ch} \quad , \tag{3-9}$$

where r_{ch} is the channel resistance per unit length and have been defined in (3-2). By differentiating (3-9) we have

$$\frac{\delta^2 V_{ch}(x)}{\delta x^2} = -r_{ch} \frac{\delta I_{ch}(x)}{\delta x} \tag{3-10}$$

and by combining (3-6) , (3-7) and (3-10), we then can have

$$\frac{\delta^2 V_{ch}(x)}{\delta x^2} = \frac{r_{ch} \cdot W}{r_{Ceff}} V_{ch}(x) = \frac{1}{L_T^2} V_{ch}(x) \quad . \tag{3-11}$$

The transfer length, L_T, is defined as

$$L_T^2 \equiv \frac{r_{Ceff}}{W \cdot r_{ch}} \quad . \tag{3-12}$$

The boundary conditions for differential equation (3-11) are

$$\left.\frac{\delta V_{ch}(x)}{\delta x}\right|_{x=0} = -I_0 r_{ch} \tag{3-13}$$

and

$$\left.\frac{\delta V_{ch}(x)}{\delta x}\right|_{x=d} = 0 \quad . \tag{3-14}$$

where I_0 is the total TFT drain-to-source current and position x=d is the end of a-IGZO layer defined by macro or active island. Equation (3-11) can be solved analytically:

$$V_{ch}(x) = I_0 r_{ch} L_T \frac{\cosh[(x-d)/L_T]}{\sinh(d/L_T)} \quad . \tag{3-15}$$

The V_{GS} dependent S/D series resistance $R_{S/D}$ (unit: Ω) can then be expressed as

$$R_{S/D} = \frac{V_{ch}(x=0)}{I_0} = r_{ch} L_T \coth\left(\frac{d}{L_T}\right) \quad . \tag{3-16}$$

Experimentally, $R_{S/D}$ and r_{ch} can be extracted from the *y*-intercepts and slopes of linear fits to (3-5), respectively (as in Figure 3.2, the linear fits to (3-5) are actually the same as fits to (3-4) used in TLM). In addition, for our a-IGZO TFT, the condition $(d/L_T)>>1$ holds and the $\coth(d/L_T)$ term in (3-16) can be simplified as unity. Therefore, the transfer length can be calculated directly from the ratio of $R_{S/D}$ and r_{ch}:

$$L_T = \frac{R_{S/D}}{r_{ch}} \tag{3-17}$$

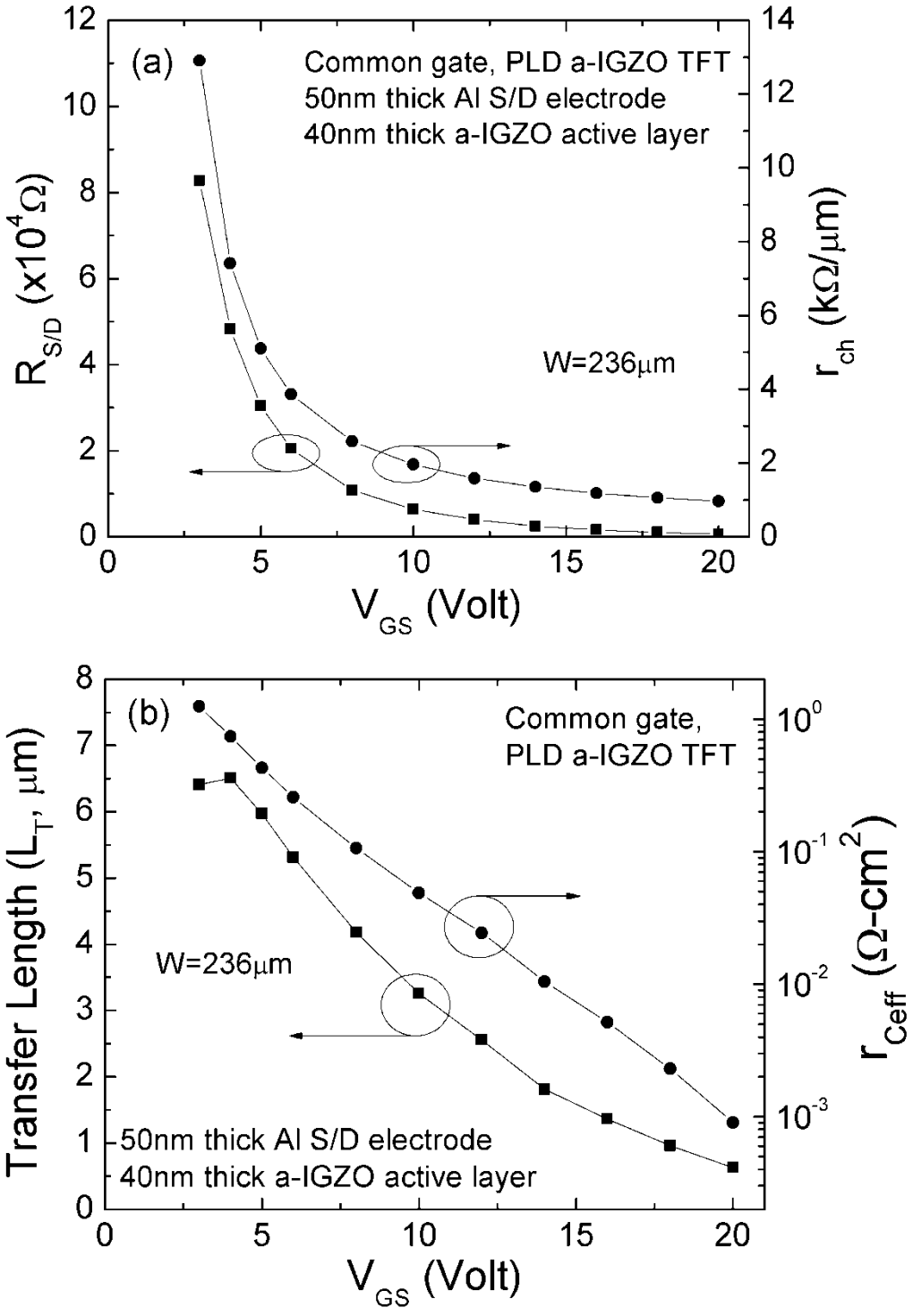


Figure 3.6 (a) Common gate, PLD a-IGZO TFT S/D series resistance ($R_{S/D}$) and channel resistance per unit length (r_{ch}) as a function of V_{GS}. (b) Calculated transfer length (L_T) and effective contact resistance (r_{Ceff}) as a function of V_{GS}. Equations (3-17) and (3-18) are used for calculation.

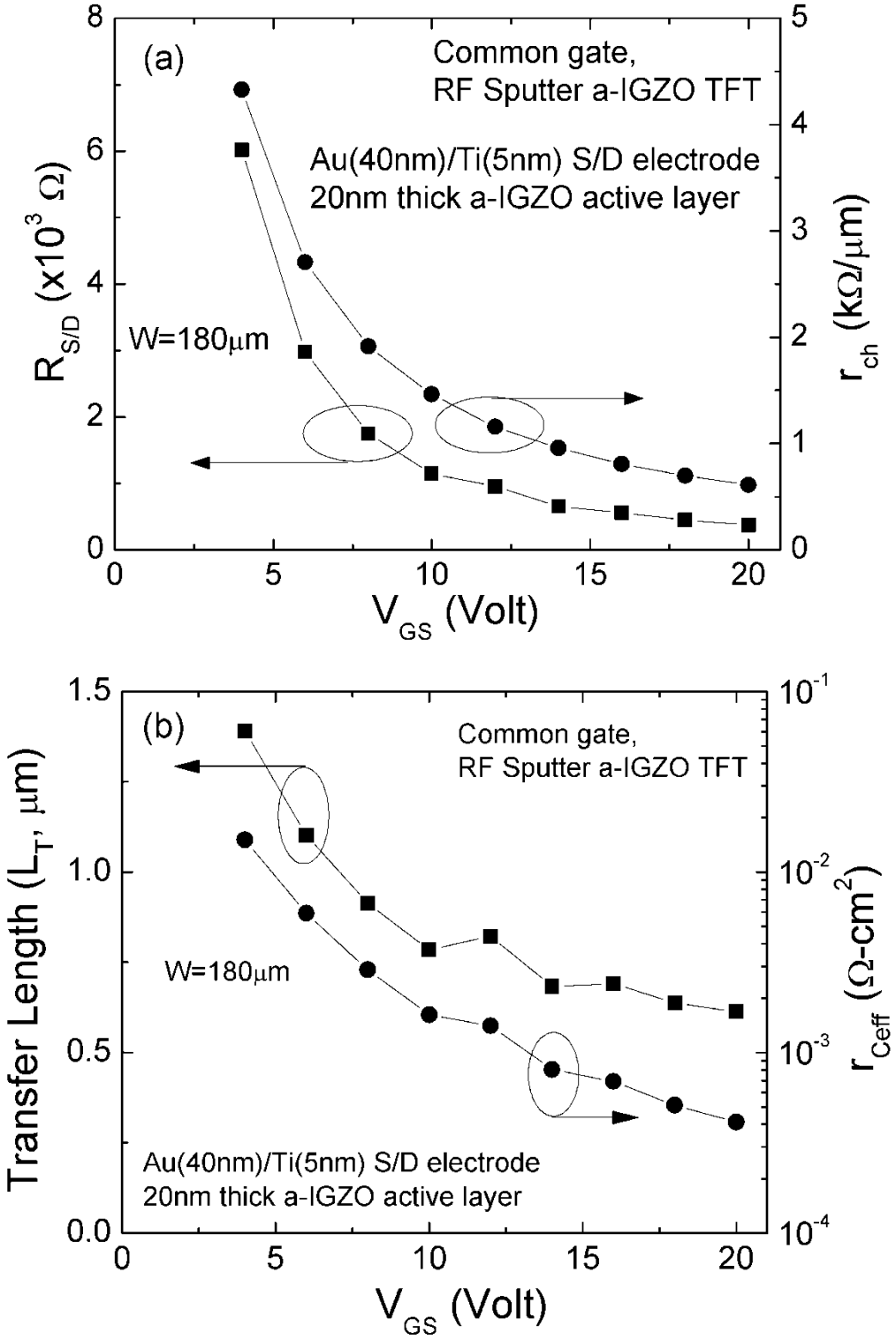


Figure 3.7 (a) Common gate, RF sputter a-IGZO TFT $R_{S/D}$ and r_{ch} as a function of V_{GS}. (b) Calculated L_T and r_{Ceff} as a function of V_{GS}. Equations (3-17) and (3-18) are used for calculation.

and from (3-12) the effective contact resistance (unit: Ω-cm^2) can be determined as:

$$r_{Ceff} = \frac{W(R_{S/D})^2}{r_{ch}} \quad . \tag{3-18}$$

$R_{S/D}$, r_{ch}, L_T and r_{Ceff} were all extracted or calculated based on data collected for both common gate PLD and common gate RF sputter a-IGZO TFTs. Their values are plotted as a function of V_{GS} as shown in Figure 3.6 and 3.7. $R_{S/D}$ and L_T are both decreasing with increasing V_{GS}. This means by applying a higher V_{GS} bias, the bulk a-IGZO becomes more conductive and the channel current requires less active region (Figure 3.5(a)) to transfer itself from the a-IGZO/SiO_2 interface to S/D electrodes. The transfer length L_T of RF sputter TFT is 1.4~0.6µm and for PLD TFT, it is 6.5~0.6µm. For low V_{GS} (e.g. V_{GS}=5V), the current in PLD TFT is much less confined with L_T more than five times higher than the L_T of RF sputter TFT. Similarly, r_{Ceff} of PLD TFT (~0.5 Ω-cm^2) is also much higher than the value of RF sputter TFT (~0.008 Ω-cm^2) for low V_{GS} (5V). From (3-8), we know the r_{Ceff} is the combination of r_B and r_C. Since r_C is largely determined by the metal/a-IGZO interface property, only r_B is a strong function of V_{GS}. The r_C may be approximated by the r_{Ceff} value for high V_{GS} (i.e. V_{GS}=20V) and from Figure 3.6(b) and 3.7(b), both TFTs have $r_C < 10^{-3}$ Ω-cm^2. (For reference, r_C of top gate a-Si:H TFTs is 0.18 Ω-cm^2. The TFT uses phosphorous-treated ITO as S/D electrodes [54].) This suggests the contact quality of the a-IGZO/Al is comparable to a-IGZO/Ti. We were not able to draw this conclusion from the TLM analysis alone. In addition, since the a-IGZO layer in PLD TFT is twice as thick as in RF sputter TFT, the large L_T (and also r_{Ceff}) in PLD TFT can be primarily associated with a high bulk a-IGZO resistivity (r_B). Consequently, the reduction in the thickness of active layer is expected to significantly improve the a-IGZO TFT S/D electrical properties.

3.2 Field-Effect Mobility of the a-IGZO TFT

3.2.1 Mathematical model for gate-voltage dependent filed-effect mobility

Perhaps the most attracting properties of the a-IGZO TFT we have discussed so far are its high mobility. Compare to a-Si:H TFT (with μ_{eff} ~ 0.8cm^2/Vs) there is more than an order of magnitude improvement in μ_{eff} for a-IGZO TFT. In fact, the μ_{eff} extracted by (2-1) or (2-3) can be considered as average value. Further analysis of the linear region transfer data [e.g. Figure 2.11(a)] reveals a non-linear I_D/V_{GS} behavior observed at the higher V_{GS}: the actual I_D seems to be higher than expected value for a given V_{GS}. In other words, the apparent field-effect mobility is dependent on V_{GS}. This can be better illustrated by defining the incremental field-effect mobility (μ_{inc}) with the following relation:

$$\mu_{inc} = \left(\frac{\delta I_D}{\delta V_{GS}} \right) \left[\frac{L}{(WC_{ox}V_{DS})} \right] \tag{3-19}$$

and plots it as a function of V_{GS}. It should be noticed that for a small V_{DS} ($V_{DS} << V_{GS}-V_{th}$), (3-19) is approximately equal to the definition proposed by Hoffman in his earlier work [61]. Figure 3.8 shows the μ_{inc} of defined gate, RF sputter a-IGZO TFT. The TFT structure and original I/V properties have been discussed in Section 2.1.3 and 2.2.3, respectively. The extracted μ_{inc} is proportional to the V_{GS} and reaches a maximum value of 12.6 cm^2/Vs within our measurement range, but μ_{inc} does not saturate. Such behavior has also been seen in other oxide semiconductor TFTs [62, 63]. It is believed that portion of the induced channel charges are trapped in band tail states (or deep states) and cannot contribute to the I_D. As V_{GS} increased, more free carriers are able to contribute to the I_D and this makes μ_{inc} increase toward the intrinsic band mobility (In Chapter 5, intrinsic band mobility of 15cm^2/Vs was used in the numerical simulation of RF sputter a-IGZO TFT with thermal

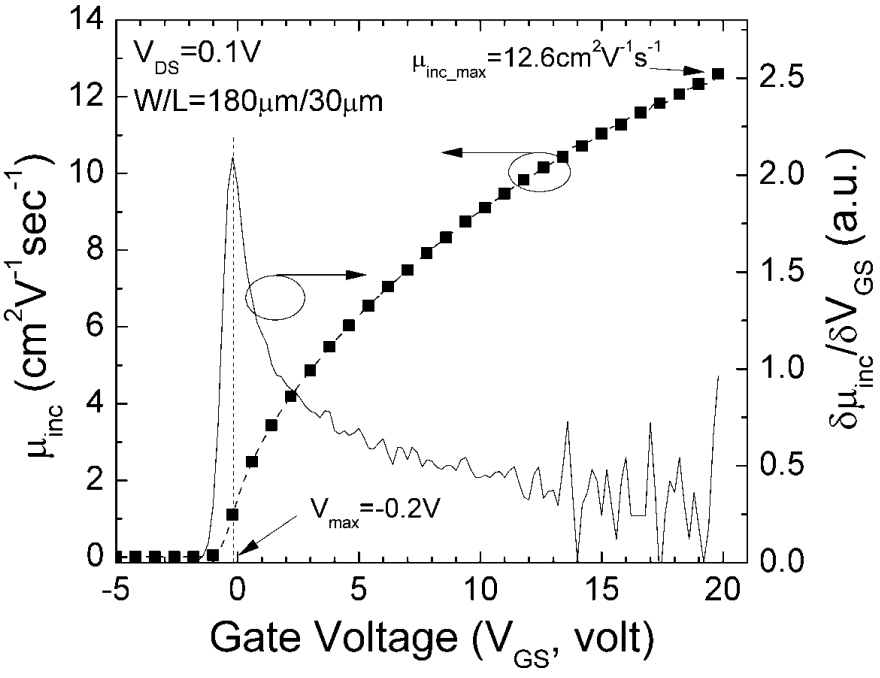


Figure 3.8 Symbol(■): Incremental field-effect mobility (μ_{inc}) of the defined gate, RF sputter a-IGZO TFT extracted by using (3-19). The differentiation of μ_{inc} ($\delta\mu_{inc}/\delta V_{GS}$, solid line) is also shown. V_{max} represents the V_{GS} with maximum $\delta\mu_{inc}/\delta V_{GS}$.

SiO_2 as gate insulator). Therefore, to better model the a-IGZO TFT I/V properties, the gate voltage dependent field-effect mobility ($\mu_{eff}(V_{GS})$) is introduced into the standard MOS-FET equation (2-1):

$$I_D = \mu_{eff}(V_{GS})C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{th})V_{DS} \tag{3-20}$$

and $\mu_{eff}(V_{GS})$ is described as

$$\mu_{eff}(V_{GS}) = \mu_0\left[\frac{(V_{GS}-V_{th})}{V_C}\right]^{\alpha} \tag{3-21}$$

where μ_0 is the intrinsic band mobility, V_C is the material dependent critical voltage and α is the power coefficient which describe the dependence of $\mu_{eff}(V_{GS})$ on effective gate voltage (V_{GS}-V_{th}). As a comparison, in ideal case, α=0 and $\mu_{eff}(V_{GS})= \mu_{eff} = \mu_0$. For the ease of parameter extraction, (3-21) is further simplified as:

$$\mu_{eff}(V_{GS}) = K(V_{GS} - V_{th})^{\alpha} \tag{3-22}$$

where $K = \mu_0 (1/V_C)^{\alpha}$ is a material dependent parameter. It should be noticed that the K has the unit of $cm^2/V^{\alpha+1}s$. By substituting (3-22) into (3-20), new I_D equation can be written as

$$I_D = K\, C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^{\gamma} V_{DS} \tag{3-23}$$

where $\gamma \equiv \alpha + 1$. (3-24)

From (3-22) and (3-24), we can also derive:

$$\mu_{eff}(V_{GS}) = K(V_{GS} - V_{th})^{\gamma - 1} \tag{3-25}$$

and from (3-19) and (3-23), incremental field-effect mobility can be described as

$$\mu_{inc} = K\gamma(V_{GS} - V_{th})^{\gamma - 1}. \tag{3-26}$$

3.2.2 Parameter extraction: simultaneous method

Special care should be made to properly extract the V_{th}, γ and K. Directly performed a non-linear fitting of the entire transfer data to (3-23) is not an ideal approach because this can introduce unwanted subthreshold region data into the fitting algorithm which causes error. In this study, we propose two different methodologies which are suitable for device parameter extraction. The first method (method #1 or simultaneous method) is adapted from what was developed for a-Si:H TFT [64]. The determination of threshold voltage is based on (3-23). By varying V_{th}, we find the least-square linear fit to the logarithm of drain current ratio:

$$\log\left(\frac{I_D}{I_0}\right) = \gamma \log\left(\frac{V_{GS} - V_{th}}{V_0 - V_{th}}\right) \tag{3-27}$$

where the reference drain current, $I_0 = I_D(V_{GS} = V_0)$, is chosen to be much larger than the

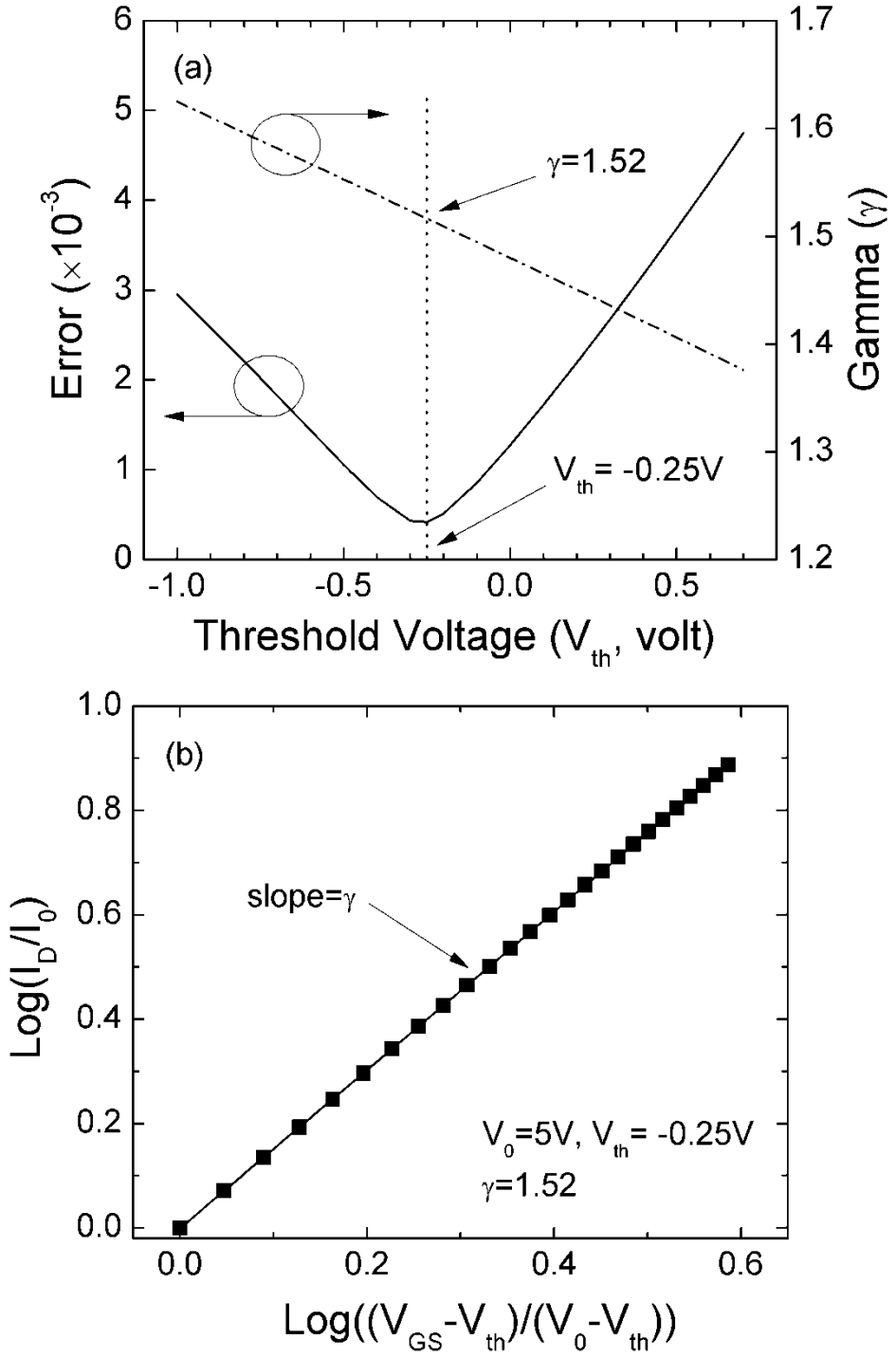


Figure 3.9 (a) Variation in γ of the experimental I-V data (collected from defined gate, RF sputter a-IGZO TFT) in above threshold region as a function of V_{th}. A reference gate voltage V_0 of 5V is used for parameter extraction. Also shown is the RMS error of the least-square fit to the log of drain current ratio ($Log(I_D/I_0)$). (b) Example of the actual linear fitting plot to (3-27) at V_{th} with minimum error (-0.25V).

subthreshold current. In this study, V_0=5V with I_0= 2.29×10^{-7}A were chosen. Figure 3.9(a) shows the RMS error and corresponding γ of the linear fit to (3-27) as a function of V_{th}. The V_{th} and γ are determined simultaneously by the best linear fit with minimum error. As indicated in Figure 3.9(b), V_{th} and γ are -0.25V and 1.52, respectively. K (=1.76) is finally extracted by performing a best non-linear fit of above threshold transfer data to (3-23). If μ_0=15cm^2/Vs is used, the V_C and α can also be calculated as 61.6V and 0.52, respectively.

3.2.3 Parameter extraction: two-steps method

Although the first method (method #1) can accurately extract V_{th} and γ simultaneously, the procedure is rather complicated and not straight forward. Our second approaches (method #2) extract V_{th}, γ and K separately in a two steps process. A similar method has also been used to extract the threshold voltage of the a-Si:H TFT [5]. The V_{th} is first defined as the V_{GS} value at which maximum $\delta\mu_{inc}/\delta V_{GS}$ occurs (V_{max}=V_{th}= -0.2V, as illustrated in Figure 3.8). The "change" of μ_{inc} vs. V_{GS} has two opposite behaviors between sub- and above threshold regions: in subthreshold region, μ_{inc} increases exponentially with V_{GS} and the $\delta\mu_{inc}/\delta V_{GS}$ is increasing with V_{GS}. However, in above threshold region, $\delta\mu_{inc}/\delta V_{GS}$ is decreasing with V_{GS}, and μ_{inc} will eventually saturate at certain value (e.g. intrinsic band mobility, μ_0). Consequently, the maximum $\delta\mu_{inc}/\delta V_{GS}$ point represents the transition between these two regions, where V_{th} is located. The authors believe such phenomenon is fundamentally due to the difference in a-IGZO deep gap and band tail density-of-states (DOS) properties. The γ-1 (or α) and K are then extracted from the linear fit of the log-log plot of (3-26):

$$\log(\mu_{inc}) = \log(K\gamma) + (\gamma - 1)\log(V_{GS} - V_{th}) \tag{3-28}$$

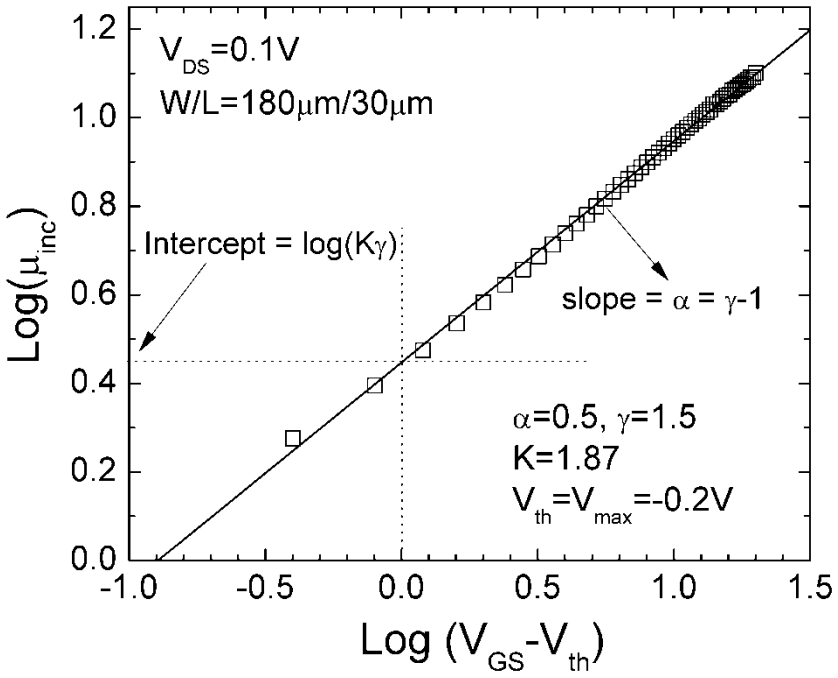


Figure 3.10 The log-log plot of the incremental field-effect mobility (μ_{inc}) as a function of the effective gate voltage (V_{GS}-V_{th}). Data are collected from defined gate, RF sputter a-IGZO TFT. The V_{th} is extracted from V_{max} in Figure 3.8. Solid line is the linear fit to the experimental data (symbol: □).

as shown in Figure 3.10. In summary, the V_{th}, γ and K extracted by method #2 are -0.2V, 1.5 and 1.87, respectively. In addition, the associated V_C and α are 64.3V and 0.5, respectively (with μ_0=15cm^2/Vs).

Figure 3.11 shows the results obtained from various models/methodologies discussed in this study. The table in Figure 3.11(a) summarized the extracted parameters by using different methods. The μ_{inc} and I_D are calculated by substituting corresponding parameters into (3-26) and (3-23), respectively. Results obtained from method #1 and #2 are consistent with each other and they are fairly closed to the experimental data. RMS errors for I_D calculated by different methods are also provided in Figure 3.11(b) and method #1 has the lowest error. Therefore, method #2 is recommended as the best method for routine

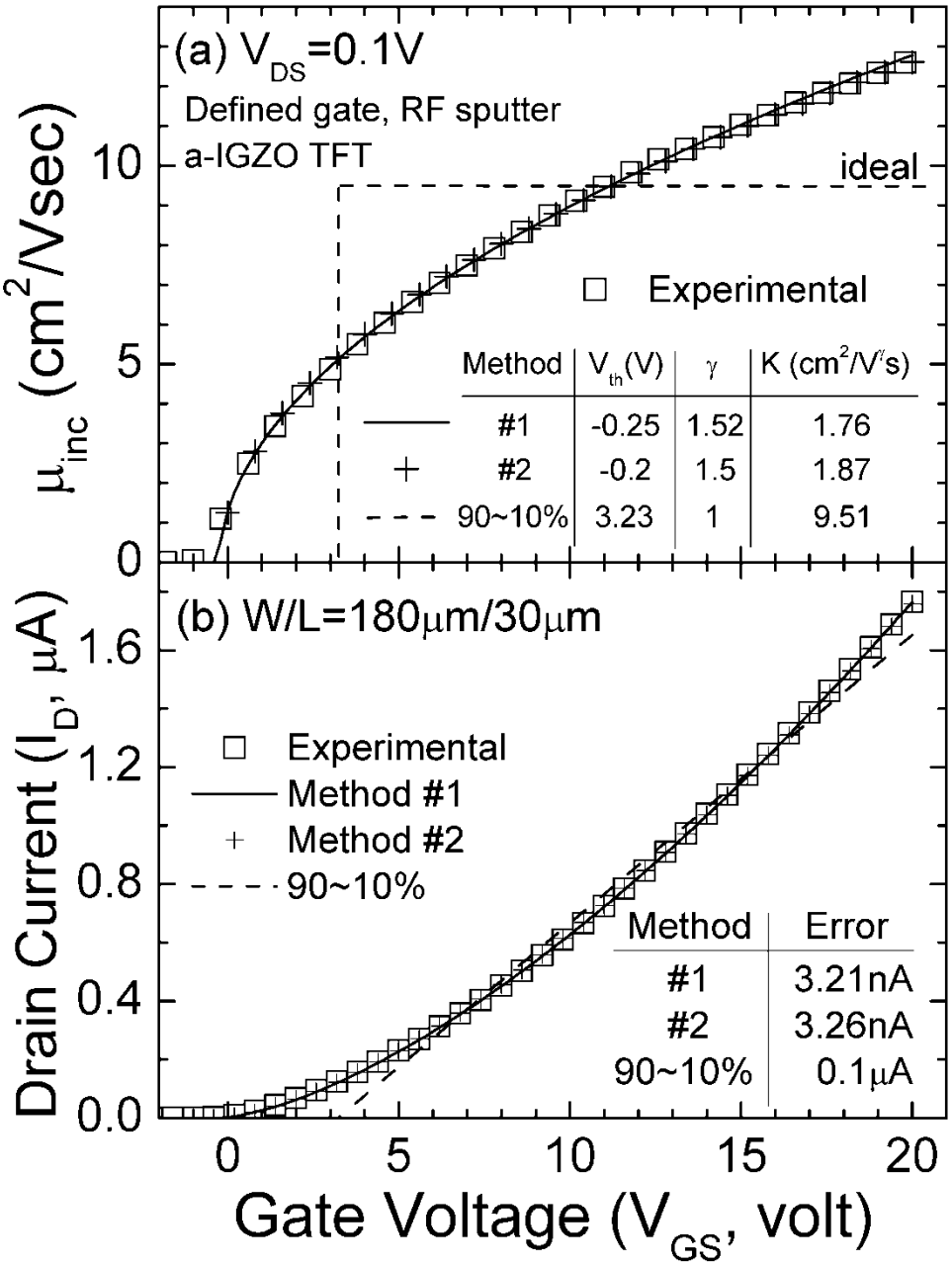


Figure 3.11 The calculation of (a) μ_{inc} and (b) I_D based on different models/extraction methods used in this study. Method #1 (solid line) is conducted in Figure 3.9. Method #2 (+) is illustrated in Figure 3.10. The 90%~10% method (dash line) is conducted based on the standard MOSFET equation (2-1). Symbol (□): experimental data measured from defined gate, RF sputter a-IGZO TFT.

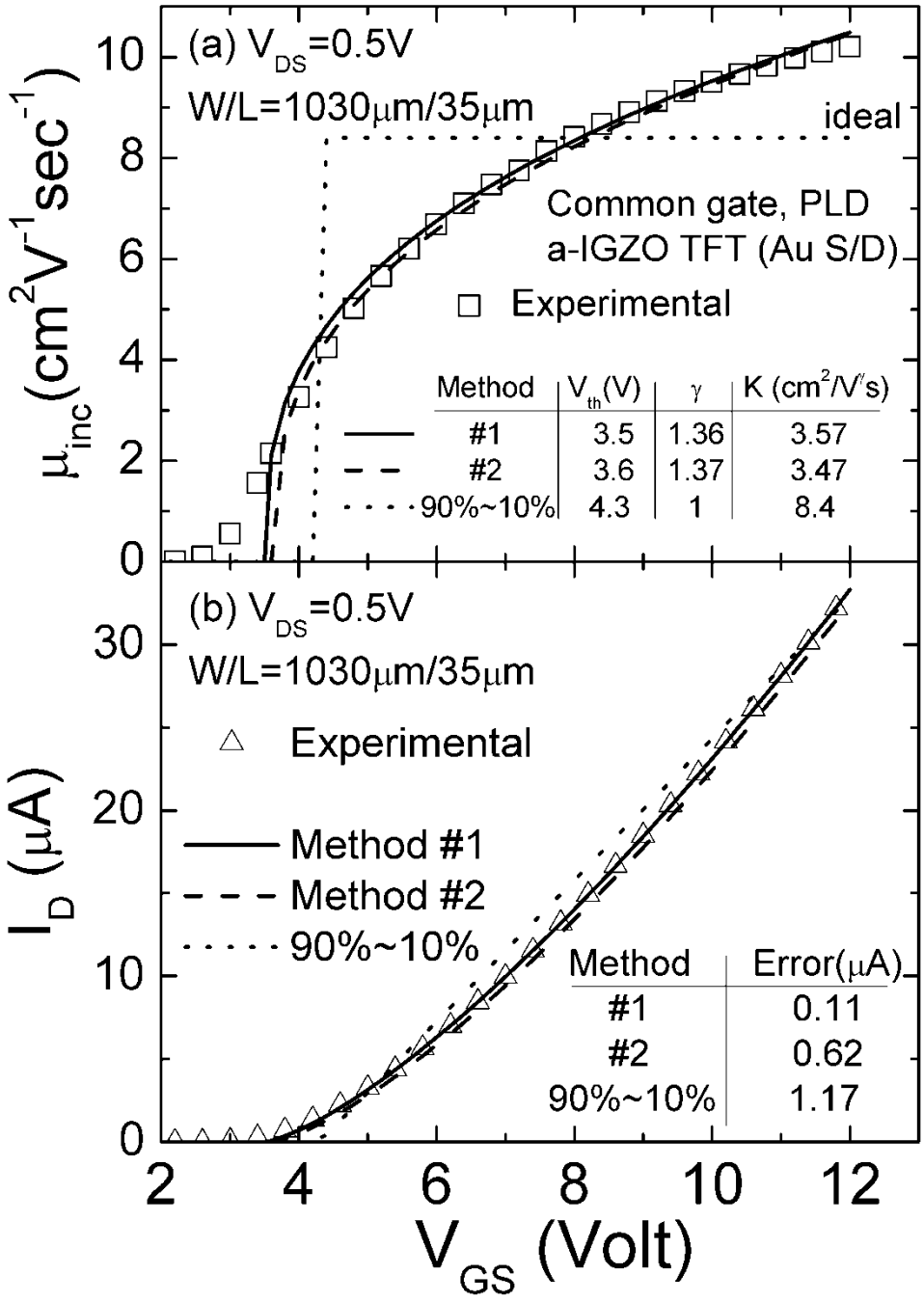


Figure 3.12 (a) μ_{inc} and (b) I_D of common gate, PLD a-IGZO TFT with gold (Au) S/D electrodes [47]. Both experimental and simulated data are shown. Method #1 (solid line) and method #2 (dash line) were discussed in Section 3.2.2 and 3.2.3, respectively. The 90%~ 10% method (dot line) is conducted based on the standard MOSFET equation (2-1). Symbol (□ and Δ): experimental data.

parameter extraction. Method #1 can be used as backup when the verification on accuracy is necessary. We also applied the same methodology to common gate PLD a-IGZO TFT (with Au S/D electrodes [47]) and achieved very close fit to the experimental data (Figure 3.12). It is clear that the (3-22) is suitable for describing gate voltage dependent field-effect mobility, $\mu_{eff}(V_{GS})$, which is essential to accurately model the a-IGZO TFT I/V properties.

The extracted $\gamma = \alpha+1$ for our RF sputter a-IGZO TFT is slightly higher than the value of the a-IGZO TFT fabricated from pulse-laser deposition (PLD) (γ=1.37, Figure 3.12) material and of coplanar homo-junction a-IGZO TFT with the chemical vapor deposition (CVD) SiO_2 gate insulator (γ=1.13) [65]. This suggests that γ is affected not only by the deposition method of IGZO but also by the gate insulator, fabrication processes, and device structures. The significance of γ may physically link to the conduction band tail states. Kishida *et al.* showed that the movement of TFT surface band bending with gate voltage changes when the electrons are trapped in the band-tail states and the γ can be expressed as [66]:

$$\gamma = 2\left(\frac{T_G}{T}\right) - 1 \tag{3-29}$$

where T is the temperature and T_G is the characteristic temperature of the amorphous semiconductor density-of-states (DOS) distribution around the position of the Fermi level. The equation is valid for $T < T_G$. For a-Si:H, T_G commonly represents the characteristic temperature of the conduction-band-tail-states and a high density of such states causes the non-ideal condition of $\gamma > 1$. Suppose the same idea also held for a-IGZO TFT (one possible origin of the conduction-band-tail-state in a-IGZO is the variation of In-O-metal bond angles [35, 67]), we extracted the T_G for our a-IGZO TFT to be ~371K (or kT_G ~32 meV). It should be noticed that the actual T_G for a-IGZO conduction-band-tail-states might have

an even lower value, due to the limitation of room temperature measurement. Nonetheless, the authors suppose that the extracted T_G is still proportional to the density of conduction-band-tail-states, i.e. a higher γ can correspond to an increase in T_G and vice versa.

3.2.4 The effect of $\mu_{eff}(V_{GS})$ on transmission line analysis

In Section 3.1.1, the transmission line analysis (TLM) model is based on constant field-effect mobility (μ_{TLM}). To discuss the effect of $\mu_{eff}(V_{GS})$ on TLM, we substitute the $\mu_{eff}(V_{GS})$ (i.e. equation 3-22) for μ_{TLM} in (3-2) and (3-4). Thus, we have the TFT channel resistance per unit length (r_{ch_γ}) with $\mu_{eff}(V_{GS})$ considered:

$$r_{ch\_\gamma} = \frac{1}{KC_{ox}W\left(V_{GS} - V_{th}\right)^{\gamma}} \tag{3-30}$$

and the total TFT on-resistance (R_T) becomes

$$R_T \equiv \frac{V_{DS}}{I_D} = 2R_0 + r_{ch\_\gamma} \cdot (L + 2\Delta L) = 2R_0 + \frac{L + 2\Delta L}{KC_{ox}W\left(V_{GS} - V_{th}\right)^{\gamma}}. \tag{3-31}$$

Equation 3-31 implies that the $\mu_{eff}(V_{GS})$ has no direct impact on the results of the S/D series resistance (R_0) and channel length bias (ΔL). Even when the $\mu_{eff}(V_{GS})$ is considered, the R_0 and ΔL can still be extracted from the R_T data, following the same methodology as indicated in Figure 3.2 or Figure 3.4(a). However, because the $1/r_{ch\_\gamma}$ is no longer a linear function of V_{GS} (for example, in Figure 3.4(b), a non-linear dependence of $1/r_{ch}$ on V_{GS} is observed), the extraction scheme for field-effect mobility and threshold voltage needs to be modified. Experimentally, it will be convenient if the $1/r_{ch\_\gamma}$ data can be converted into incremental field-effect mobility (μ_{inc}). The μ_{inc} and r_{ch_γ} have a mathematical relation as follows:

$$\mu_{inc} = K\gamma\left(V_{GS} - V_{th}\right)^{\gamma-1} = \left[\frac{\delta\left(1/r_{ch\_\gamma}\right)}{\delta V_{GS}}\right]\left(\frac{1}{WC_{ox}}\right). \tag{3-32}$$

Therefore, we may extract the $\mu_{eff}(V_{GS})$ and V_{th} from TLM analysis: first, the μ_{inc} vs. V_{GS} data are calculated by taking the derivative of the $1/r_{ch\_y}$ with respect to V_{GS}; then, with the μ_{inc} data, the methodologies depicted in Section 3.2.3 can be followed directly. It should be noticed that the data points of μ_{inc} need to be sufficient for parameter extraction and the V_{GS} interval in TLM analysis should be kept as small as possible (i.e. 0.2V or lower).

Chapter 4

Photofield-Effect Study of the a-IGZO TFTs

4.1 Introduction

Conventional active-matrix (AM) flat panel displays (FPDs) are based on amorphous or polycrystalline silicon thin-film transistor (TFT) technology. The advantage of hydrogenated amorphous silicon (a-Si:H) thin film is being able to be deposited uniformly on to the glass substrate over a large area by plasma enhanced chemical vapor deposition (PECVD) method [5]. Nonetheless, the main limitations of the a-Si:H are: electrical instability and a low (usually < 1 cm^2/Vs) field-effect mobility (μ_{eff}), which can lead to reduction of the pixel aperture ratio and driving ability for some demanding display applications [15]. Although poly-crystalline silicon TFT has a larger mobility (~100 cm^2/Vs), due to the need of re-crystallization (such as excimer-laser annealing, ELA [68]), its electrical properties uniformity over a large area is not always acceptable for a high yield low cost manufacturing and a high resolution display applications [15].

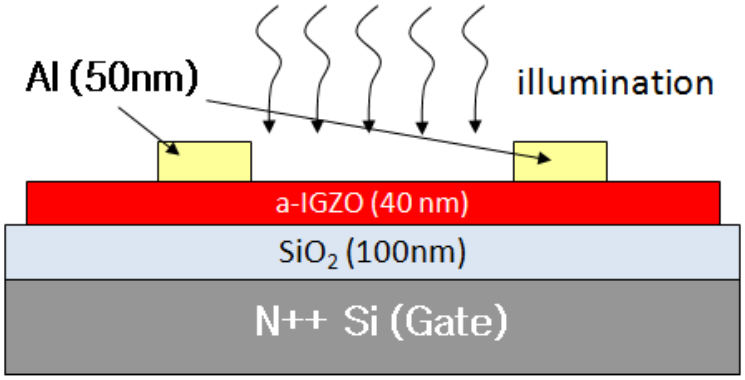
Because the next generation AM-FPDs [9] and flat panel photo-imagers [69] will pose a more stringent requirements, which cannot be handled by existing a-Si:H or poly-Si TFT backplane technology, such as a low temperature deposition over a large area, reduced pixel size (resolution), a large dynamic range and a high operational speed, there is an

increasing demand among others for a new semiconductor material to overcome the above mentioned limitations. In Chapter 2 and 3, we have seen that the TFT made from amorphous In-Ga-Zn-O (a-IGZO) can easily have a high μ_{eff}, a very low sub-threshold swing (S < 420mV/dec) and well controlled off-current (<10^{-12}A). In addition, the device processing is at low temperature and is compatible to large area (sputtering). These properties are highly desirable for next generation optoelectronics. In fact, by the time this dissertation is written, a-IGZO TFT has been successfully implemented in applications such as active-matrix organic light-emitting display (AM-OLED) [26], active-matrix liquid crystal display (AM-LCD) [27], electronic paper [70] and transparent electronics [39, 49]. Many of these proposed uses of the a-IGZO TFT will involve a possible exposure of device to backlight or ambient light during operation. However, there is only very limited work done in this important area. In this chapter, we investigate the light wavelength and intensity dependent photo-responses (photofield-effect) in a-IGZO TFTs. We also present, for the first time, the photofield-effect analysis of the a-IGZO TFT under UV monochromatic photo illumination that was used for the extraction of the a-IGZO density-of-states (DOS).

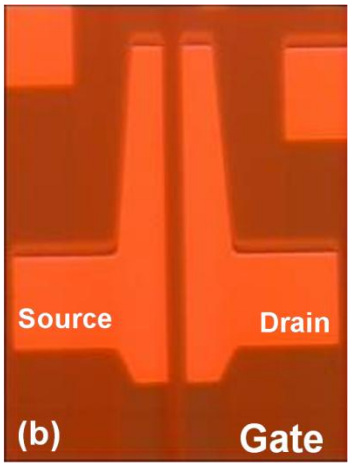
4.2 Experimental

4.2.1 Common gate, inverted-staggered a-IGZO TFT

Figure 4.1 shows the cross-section and top view of the common gate, inverted staggered, pulse-laser deposition (PLD) a-IGZO TFT used in this study. The detail process flow has been discussed in Section 2.1.1. The 50nm thick aluminum (Al) source/drain



(a)



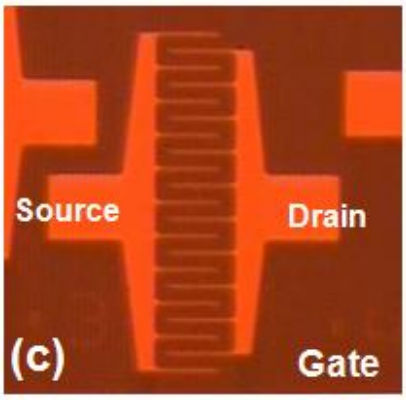


Figure 4.1 (a) Cross-sectional view of the common gate, PLD a-IGZO TFT device used in photo field effect study. (b) and (c) are die photos of regular and finger type (interdigitated) TFTs, respectively.

electrodes were deposited through stencil mask openings by thermal evaporation. In addition, the device was thermally annealed in air at 300^0C for 5 minutes. We also deposited a-IGZO thin film directly onto quartz substrate to measure its optical properties. The absorption spectrum of the a-IGZO thin-film was collected by a Cary 5E UV-VIS spectrometer using polarized light [71]. Quartz substrates were used to minimize the background interference during transmittance measurement.

Experiment Type	Wavelength (λ)	Photon Flux / Light Intensity (Irradiance)
Wavelength Dependent	660nm ~ 365nm	1×10^{13} photons/cm^{2}s
Intensity Dependent	420 nm	Dark ~ 10 μW/cm^2

Table 4.1 Experimental conditions for photofield-effect study.

4.2.2 Experimental conditions and setup

Electrical measurement of the a-IGZO TFT were carried out with a probe station system located in a light tight box. The transistor electrical properties were measured by a PC controlled Agilent 4156 semiconductor parametric analyzer. During photofield-effect measurement, photo excitation was provided by a Hg-Xe lamp in combination with narrow band filters and an optical fiber. The monochromic light passed through a fiber cable and probe station microscope, which is used to focus the illumination on the a-IGZO TFT channel. Figure 4.2 shows the schematic of experimental setup used in this study. All measurements were done at room temperature in ambient air. Table 4.1 further lists the details of experimental conditions. It should be noticed that before each measurement the light intensity was calibrated by Oriel 70260 radiant power meter with the photodiode sensor attached. Each measurement step takes about 10 mins to achieve a steady state under illumination. Both regular and finger (interdigitated) types of TFTs were measured under illumination and show very similar photo-responses.

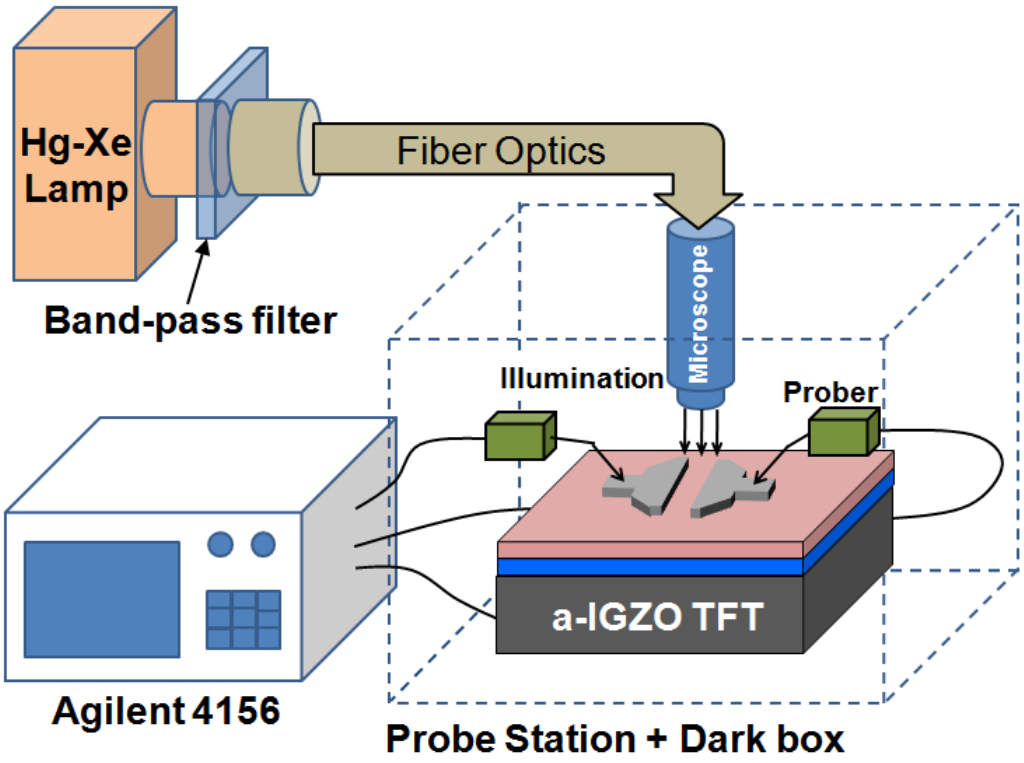


Figure 4.2 The schematic of experimental setup used in photofield-effect study.

4.3 Optical Properties of a-IGZO Thin-Film

Figure 4.3 shows the optical absorption spectrum of the PLD a-IGZO thin films (thickness=181nm). The absorption coefficient (α) of a-Si:H collected from other group [72] is also shown as a reference. The α of the a-IGZO is at least an order of magnitude lower than it's a-Si:H counterpart within the investigated photon energy range. For example, for visible light (1.8~3.1eV), the α of a-Si:H is ranging from 3000 to ~5×10^5 cm^{-1} while α of the a-IGZO is well below $10^3 cm^{-1}$ except the near UV region (~3.1eV). We assumed parabolic densities of band states within a-IGZO and extracted the optical energy band gap (E_g, also called Tauc gap) by applying the Tauc method [73]:

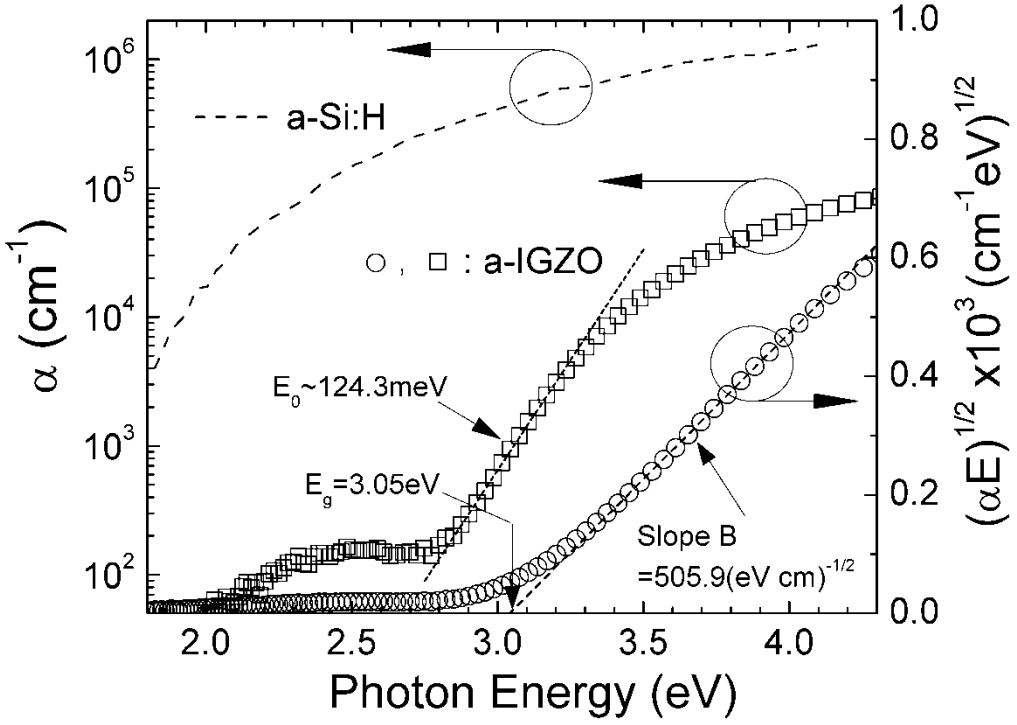


Figure 4.3 Optical absorption spectrum of PLD a-IGZO (○, □) [74] and a-Si:H (dash line) [72] thin film.

$$(\hbar\omega\alpha)^{1/2} = B(\hbar\omega - E_g) \tag{4-1}$$

where $\hbar\omega$ is the photon energy (E) and α is the absorption coefficient. The Tauc gap (E_g) was determined to be ~3.05 eV (and B=505.9 $(eV\text{-}cm)^{-1/2}$) as shown in Figure 4.3. The result suggests that a high visible light transparency of the a-IGZO is due to its wide optical band-gap. We also observed the exponential optical energy dependence of the absorption coefficient in the vicinity of E_g which can be described by [72]:

$$\alpha \propto \exp\left(\frac{E}{E_0}\right) \tag{4-2}$$

where E is the photon energy and E_o is the characteristic slope also frequently called Urbach energy. The Urbach energy is determined to be around 124 meV as indicated in Fig-

ure 4.3. In amorphous semiconductors, the Urbach energy is related to the joint density-of-states determined by both conduction and valence band tail states. Because the valence-band-tail state can be broader (or shallower) than conduction-band-tail state, they can dominate the optical absorption [75] and Urbach energy could be used to represent the valence-band-tail slope value. Such approximation had been commonly used in a-Si:H thin-film; and conduction-band-tail slope is usually about half of the valence-band-tail slope [76]. If we assume a similar situation to occur in a-IGZO, the valence-band-tail slope is approximately 124 meV and corresponding conduction-band-tail slope will be around 62 meV. However, this conduction-band-tail slope value (62 meV) appears to be much higher than other values extracted from TFT electrical properties. For example, in the study of V_{GS} dependent μ_{eff} (i.e. (3-29)), the kT_G is ~32meV; and in numerical simulation (Chapter 5), the conduction-band-tail slope (E_a) is determined to be 13meV. This suggests the conduction-band-tail slope in a-IGZO maybe much smaller than half of its valence-band-tail slope and this value still needs to be confirmed by other experimental methods.

4.4 Dark a-IGZO TFT Electrical Properties

Figure 4.4(b) illustrates the saturation region (V_{DS}=12V) transfer characteristics of the a-IGZO TFT (W/L= 236μm/46μm). We extracted the threshold voltage (V_{th}) and field effect mobility (μ_{eff}) based on the standard MOSFET equation (i.e. (2-3)). The best linear fit between 90% to 10% of the maximum I_D (at V_{GS}=12V) was found and the V_{th} and μ_{eff} can be determined. The subthreshold swing (S) was also extracted from the subthreshold

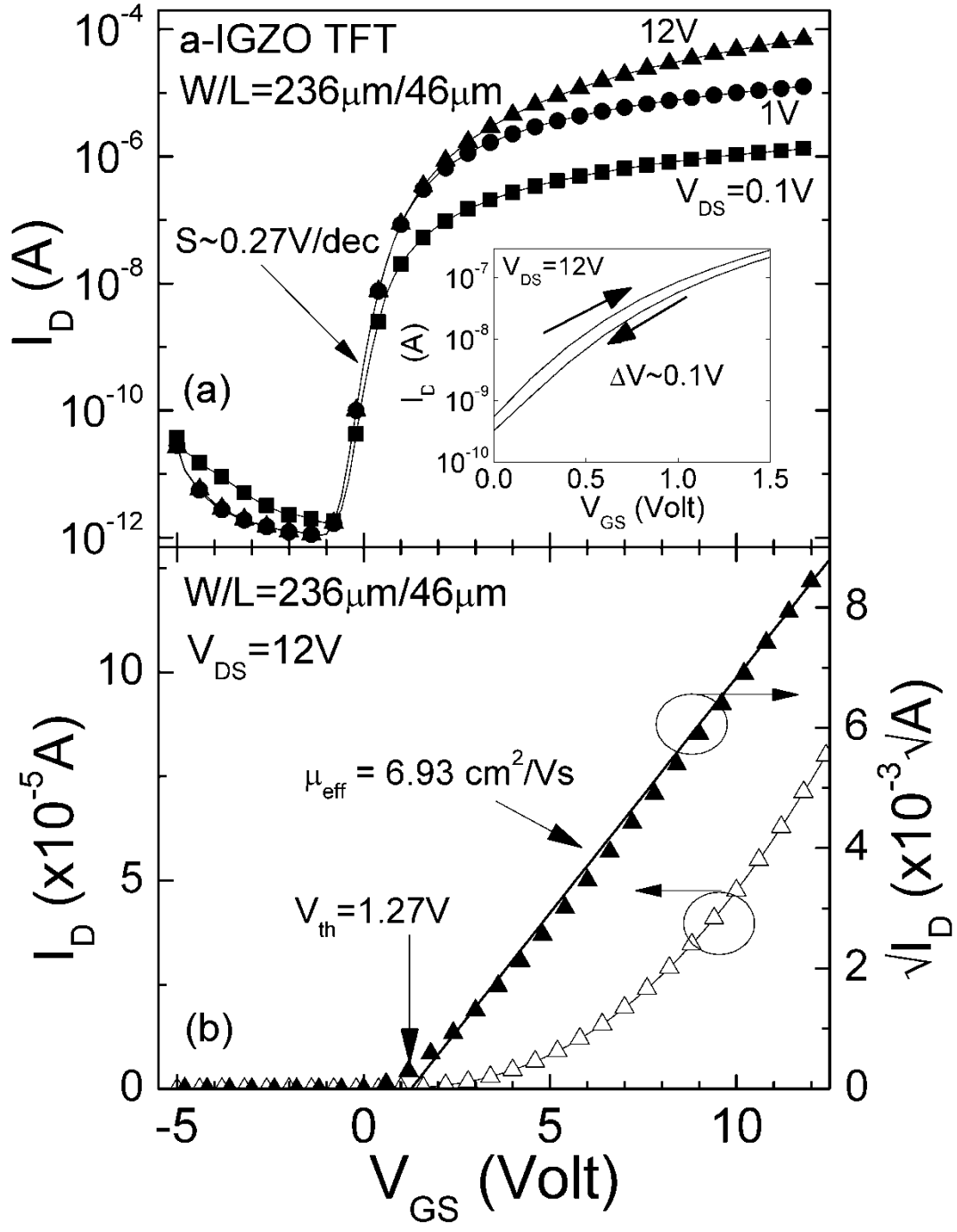


Figure 4.4 Transfer characteristic of PLD a-IGZO TFT in (a) semi-log plot and (b) linear plot. (Inset, a) The TFT hysteresis measured at V_{DS}=12V; ΔV is the shift (hysteresis) in sub-threshold properties.

TFT		μ_{eff} (cm^2/Vs)	V_{th} (V)	S (V/dec)	I_{D_off}* (A)	ΔV (V)	On/off ratio*
Type	**Size (W/L)**						
Regular Fig. 4.1(b)	236μm/46μm	6.93	1.27	0.27	10^{-12}	0.1	10^8
	1040μm/35μm	3.2	2.8	0.28	$<10^{-12}$	0.12	$>10^8$
Finger Fig. 4.1(c)	2811μm/25.6μm	3.48	2.57	0.28	$<10^{-12}$	0.11	$>10^8$

* I_{D_off} is the off-state drain-current and "on/off ratio" is the drain current ratio between on and off states.

Table 4.2 Key electrical properties of PLD a-IGZO TFTs with 50nm Al S/D electrodes used in this study.

region data (Figure 4.4(a)), using the (2-2). Table 4.2 summarizes all key electrical properties for a-IGZO TFTs with the Al S/D electrodes used in this study. It should be noticed that higher μ_{eff} is observed for TFT with smaller W. Since these devices have only macro-island patterned, channel current is not very well defined and could leak out near the channel edge. This phenomenon can cause an overestimation of μ_{eff} since the edge current could occupy significant portion of total drain current that is measured for TFT with smaller W. Even though the a-IGZO TFTs have channel width dependence, the author would like to comment that such non-ideal effect has no direct impact on photofield-effect analysis described in this chapter.

4.5 a-IGZO TFT Electrical Properties under Illumination

4.5.1 Wavelength dependent a-IGZO TFT photo-response

The response of the PLD a-IGZO TFT to monochromatic illumination was studied by measuring the TFT transfer characteristic for various light wavelengths with a constant photon flux (1×10^{13} photons/cm^{2}s). Figure 4.5 shows the a-IGZO TFT transfer characteristic in the dark and under illumination. We observed clearly a shift in TFT I_D-V_{GS} characteristics under illumination. Furthermore, a "threshold" wavelength exists when TFTs are illuminated: little or no shift occurs in TFT properties under illumination with λ>420nm (2.95eV) while a much larger change takes place when λ<420nm.

As shown in Figure 4.5(a), the I_{D_off} of TFT under illumination increases significantly as the wavelength getting closer to UV region. Compared to the original dark condition, about three orders of magnitude increase occurs when we illuminated the device at λ=365nm (3.4eV). In contrast with I_{D_off}, the I_{D_on} (drain current at V_{DS}=V_{GS}=12V) is rather constant. A negative shift in sub-threshold properties is also observed and the voltage shift about -7 volt was recorded for λ=365nm. Finally, the off-to-on switching in I_D becomes less steep when we illuminate the TFT at shorter wavelength. As consequence, the TFT subthreshold swing increases. Similar to the sub-threshold properties, in on-region, a negative shift of V_{th} (Figure 4.5(b)) is also observed. The threshold voltage shift (ΔV_{th}=$V_{th\_under\ illumination}$-$V_{th\_in\ dark}$) was determined to be about -6V under illumination at λ=365nm. The slope of $\sqrt{I_D}$-V_{GS} shows almost no change within the wavelength range used in this study (Figure 4.5(b)). This suggests the field-effect mobility (μ_{eff}) is not affected by illumination. We further summarize the result by plotting various TFT parameters as a function of incident photon energy as shown in Figure 4.6. After illumination, the I_{D_off}

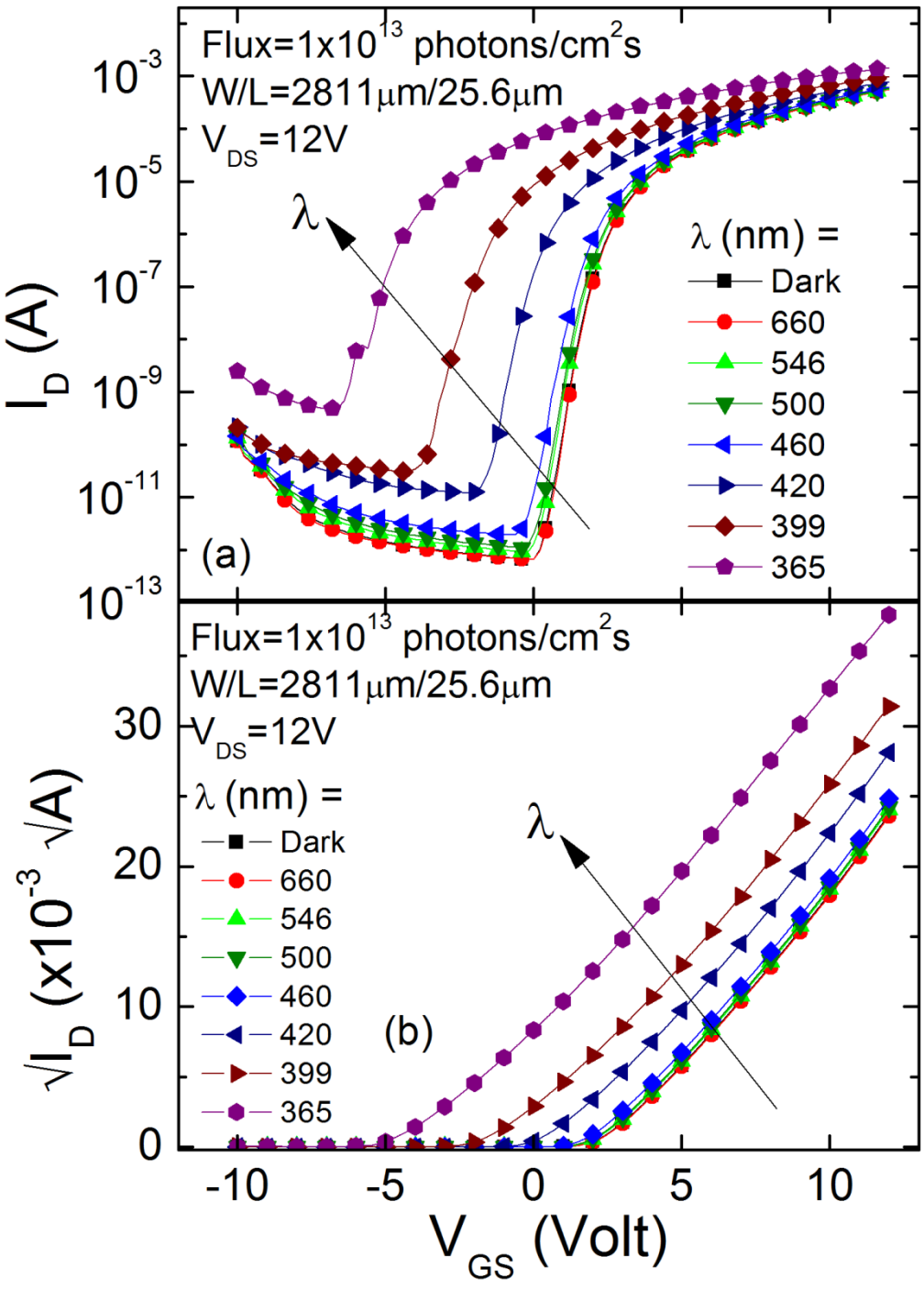


Figure 4.5 (Color) PLD a-IGZO TFT transfer characteristics for constant photon flux with the varying illumination wavelengths. ((a): semi-log plot, (b): linear plot)

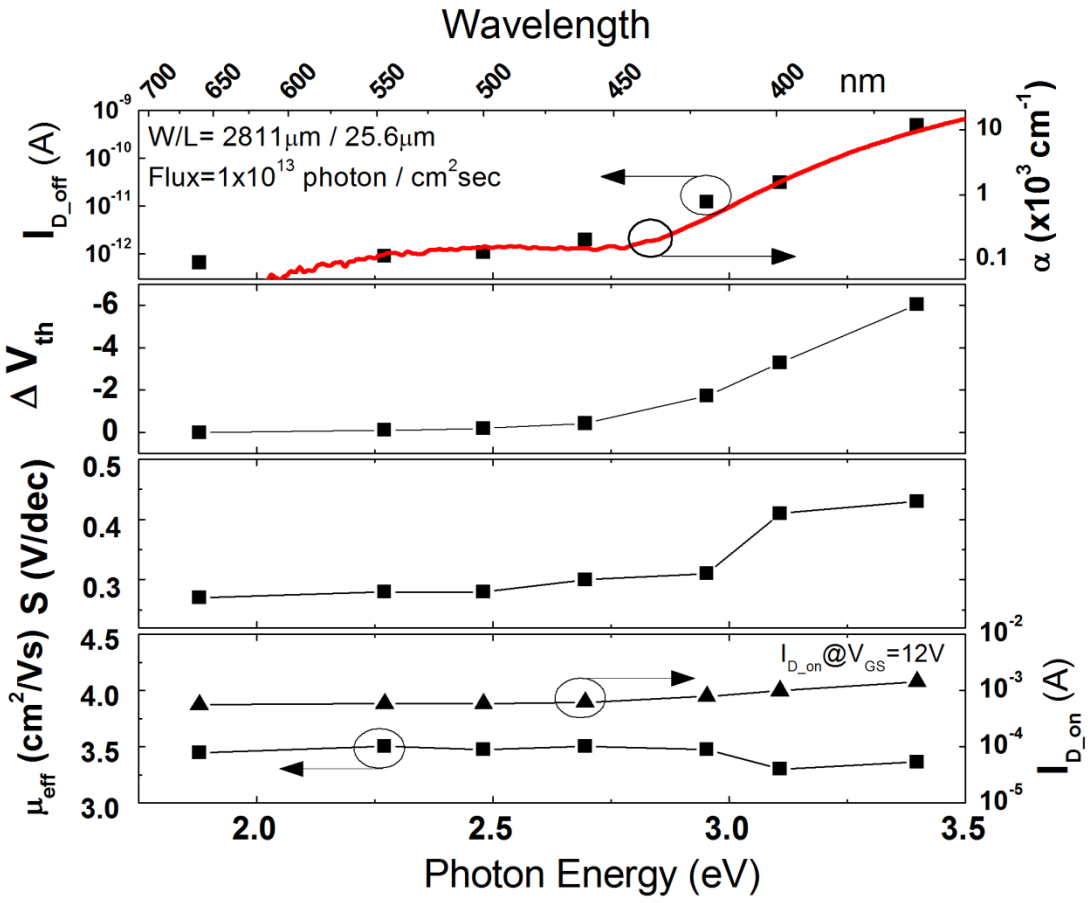


Figure 4.6 (Color) Dependence of PLD a-IGZO TFT minimum off-state drain current (I_{D_off}), on-state drain current (I_{D_on}), threshold voltage shift (ΔV_{th}), sub-threshold swing (S), and field-effect mobility (μ_{eff}) on incident photon energy (or equivalent wavelength). Red curve: absorption spectrum of the a-IGZO.

quickly reduces to its dark state value but the V_{th} shift remains. We can bring the device back to its original pre-illumination state by a 100^0C thermal treatment for 3 minutes. With no applied heat, the device will regain its pre-illumination properties after a much longer period of time. This effect is somewhat analogous to the persistent photoconductivity in a-Si:H: a brief exposure to illumination causes an increase in the a-Si:H conductivity which persists almost indefinitely at room temperature [77].

In order to elucidate the physical origin of the change in TFT electrical properties, the

a-IGZO absorption spectrum (red solid curve) is overlapped with the variation of the I_{D_off} data in Figure 4.6. It can be concluded that the light with energy less than 3.0 eV (visible region) is only weakly absorbed and has a negligible effect on the TFT transfer characteristics, while light with energy larger than 3.0 eV is strongly absorbed and is expected to generate a large density of electron-hole pairs that are separated in the device channel by electrical field. During illumination, the threshold voltage (V_{th}) shifts to more negative V_{GS} values with the increasing photo energy. We speculate that the positive charges are trapped (one possibility is hole trapping) within the channel or/and at the SiO_2 / a-IGZO interface and are responsible for the ΔV_{th}. Also, the photogenerated electrons could appear to be more mobile than holes in TFT channel region. The other possible mechanism responsible for ΔV_{th} may be the photo-induced oxygen vacancy creation [78]. The exact nature of the traps is under present investigation.

4.5.2 Intensity dependent a-IGZO TFT photo-response

To study the a-IGZO TFT response under different illumination intensity, we applied a UV monochromatic light (λ=420nm) to uniformly illuminate the TFT channel area directly through probe station microscope. The wavelength was chosen to match the absorption properties of the a-IGZO. At λ=420nm, our sample has absorption coefficient $\alpha \approx 714 cm^{-1}$, which corresponds to an optical penetration depth ($\delta=1/\alpha$) of 14μm. Since δ is much larger than the thickness of the channel a-IGZO layer (40nm), the illumination is thought to be uniformly absorbed throughout the thickness during measurement. Figure 4.7 shows the TFT transfer characteristics measured under dark and with different irradiance levels (I) up to $10 \mu W/cm^2$. We further extracted TFT parameters for each individual level and plot them as a function of light intensity (Figure 4.8). I_{D_off} was found to increase with the

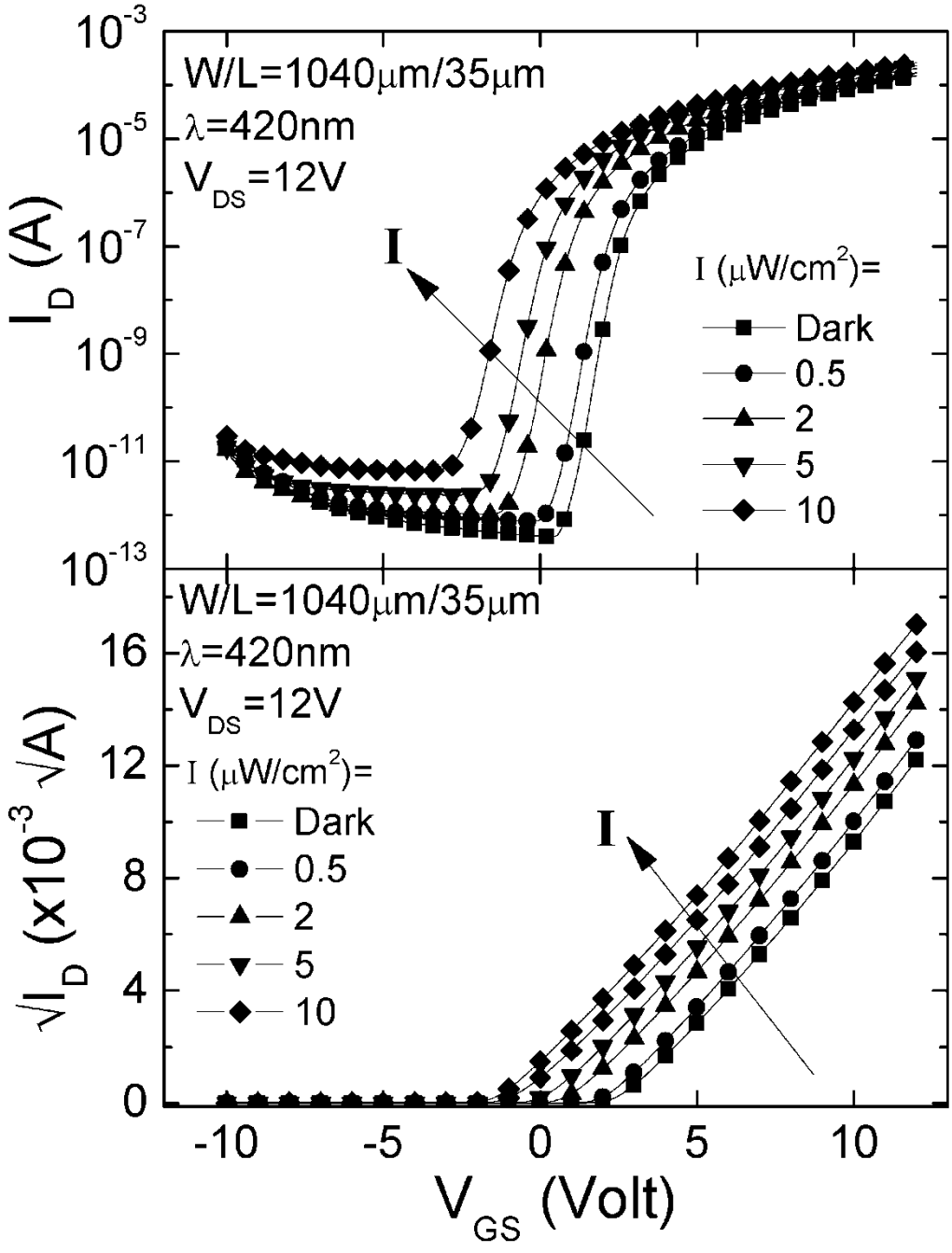


Figure 4.7 PLD a-IGZO TFT transfer characteristics for dark and different irradiance levels (I) in (a): semi-log plot and (b) linear plot. UV illumination wavelength (λ): 420nm.

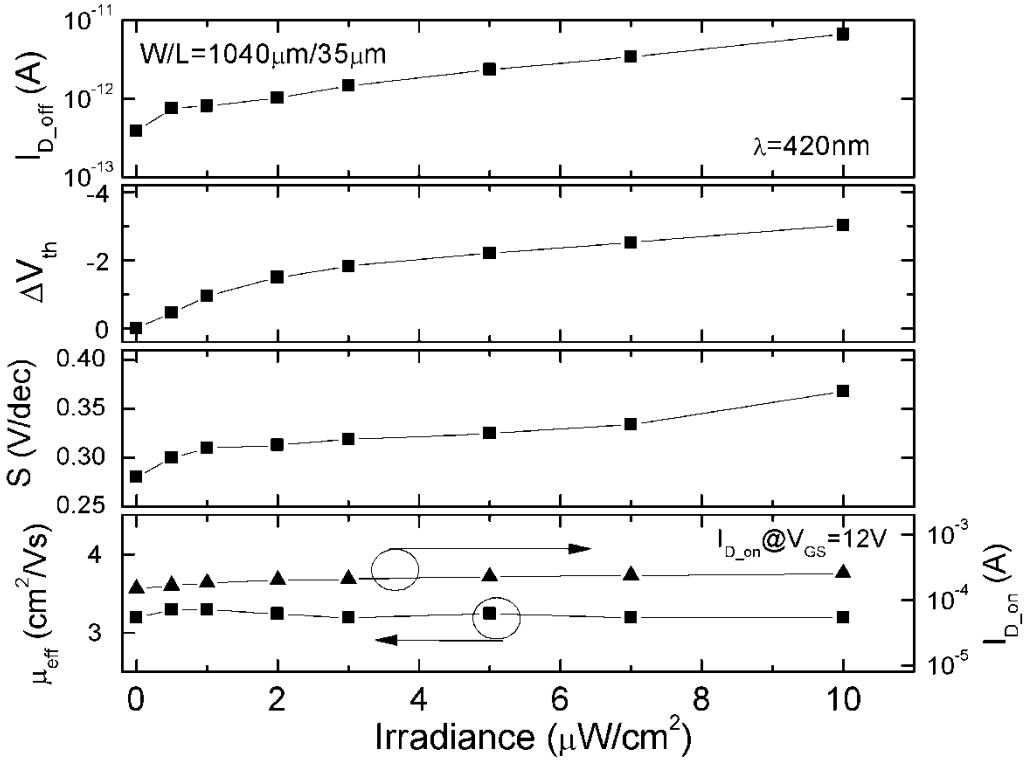


Figure 4.8 Dependence of PLD a-IGZO TFT off state drain current (I_{D_off}), on-state drain current (I_{D_on}), threshold voltage shift (ΔV_{th}), subthreshold swing (S), and field-effect mobility (μ_{eff}) on irradiance level. UV illumination wavelength (λ): 420nm.

illumination intensity, along with a negative shift of threshold voltage (ΔV_{th}). The sub-threshold swing rises from 0.28 to 0.37 V/dec at I=10μW/cm^2. This is primarily due to the increase of I_{D_off} as can clearly be seen when threshold voltage shift is used to normalize transfer curves (Figure 4.9). The μ_{eff} almost remains unchanged during the illumination process. This result indicates a strong UV photon absorption in a-IGZO layer and electron-hole pairs generated by photo-excitation cause the bulk conductivity to increase. The observed negative ΔV_{th} is similar to what has been discussed in previous section. We speculate that the photo-generated charge trapping is also occurring in this experiment. This can be further supported by the fact that all the TFT transfer curves share the same threshold voltage normalized turn-on voltage (about -2V) as illustrated in Figure 4.9.

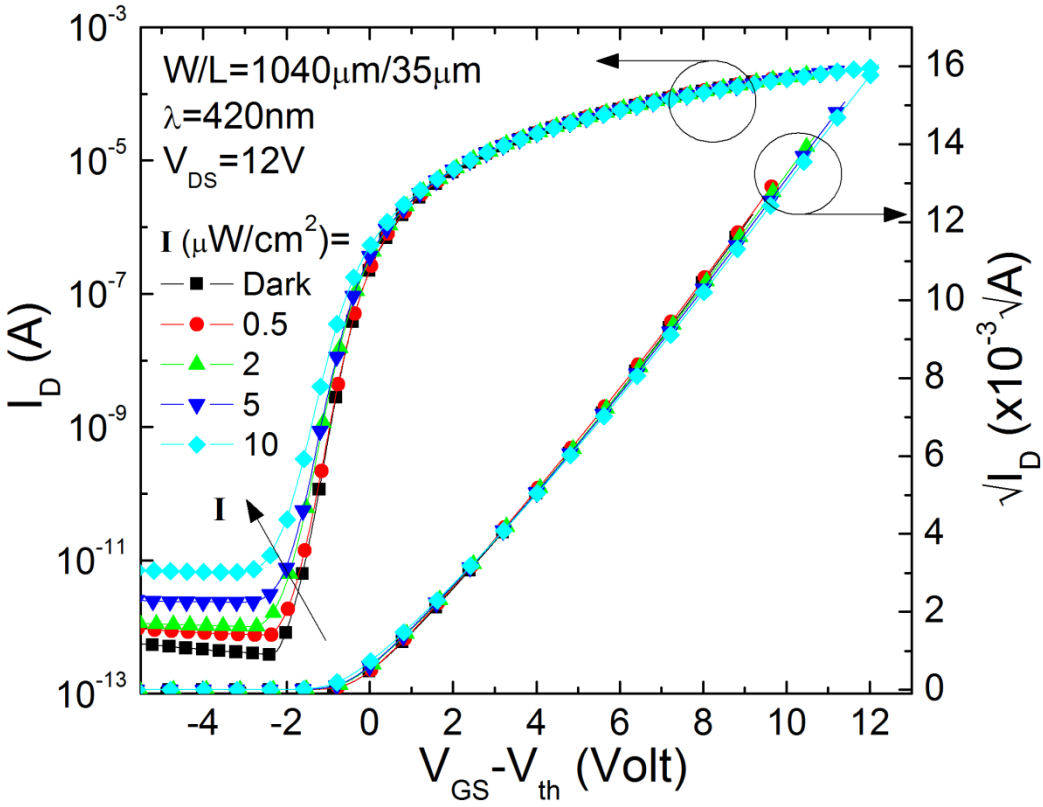


Figure 4.9 (Color) Threshold voltage normalized (I_D is plotted as a function of effective gate voltage, V_{GS}-V_{th}) PLD a-IGZO TFT transfer properties for dark and different irradiance levels (I).

It should be noticed that the UV illumination induced V_{th} shift is unique to a-IGZO TFT; it was not observed in a-Si:H TFT under UV illumination [78].

4.6 Photofield-Effect Analysis [79]

The photofield-effect theory was originally developed by Schropp *et al.* and later used to explain the photoconductivity under a controlled gate bias in a-Si:H TFT [80-83]. It was also successfully used to analyze the electrical properties under illumination in organic polymer TFT [84]. The analysis begins with the definition of photo-current (I_{ph}) as the

difference between TFT drain current under illumination and dark:

$$I_{ph} = I_{D\_ill} - I_{D\_dark} \ . \tag{4-3}$$

I_{ph} can then be extracted from the threshold voltage normalized a-IGZO TFT transfer properties (Figure 4.9). As illustrated in Figure 4.10, the I_{ph} has power-law dependence (γ) with the irradiance level (I):

$$I_{ph} \propto I^{\gamma} \ . \tag{4-4}$$

Because the I_{ph} is sensitive to the space charge distribution and surface band bending, γ is not a constant but a function of V_{GS}-V_{th} [81, 85, 86]. Dash lines in Figure 4.10 are linear fits for γ and they can be further described by an analytical theory. The theory assumes a symmetrical overlap of the acceptor (N_A=N_f+mE) and donor (N_D=N_f − mE) states around mid-gap, where E is energy, N_f is a constant and m is the linear characteristic energy slope (Figure 4.12). Thus, the total density-of-states (DOS) around mid-gap (N_D+N_A =2N_f) is a constant. The dependence of γ on V_{GS}-V_{th} is given by following formulas:

$$\gamma = \gamma_0 \left(1 - \frac{(V_{GS} - V_{th}) - V_{FB}^{'}}{(V_{GC}^{'} - V_{FB}^{'})} \right), \ for \ \ (V_{GS} - V_{th}) > V_{FB}^{'} \tag{4-5a}$$

and

$$\gamma = \gamma_0 \ , \ for \ \ (V_{GS} - V_{th}) < V_{FB}^{'} \ . \tag{4-5b}$$

In above equations, V_{FB}'=V_{FB} − V_{th_dark} and V_{GC}'=V_{GC} − V_{th_dark}. γ_0 is a material dependent constant. V_{FB} and V_{th_dark} are flat band voltage and dark threshold voltage, respectively. V_{GC} is also called critical voltage and is defined as:

$$V_{GC} = \frac{d_{ins}}{n_{ins}} \left(\frac{n_{semi}}{\varepsilon_0} \right)^{1/2} \frac{(2N_f)^{3/2}}{m} \tag{4-6}$$

where d_{ins} is the gate insulator thickness (=100nm), n_{ins} and n_{semi} are dielectric constants for

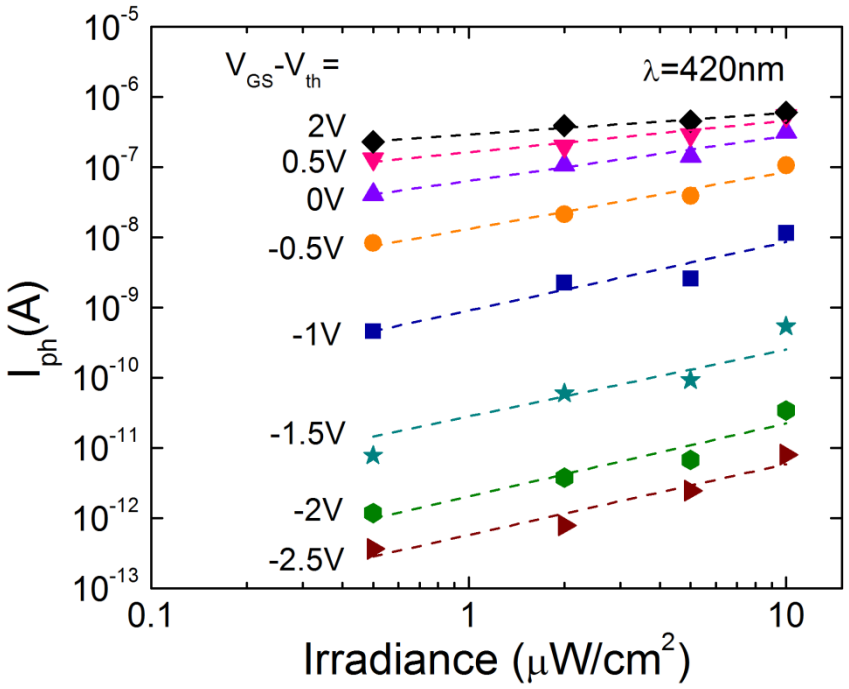


Figure 4.10 (Color) Dependence of photocurrent (I_{ph}) on irradiance at various V_{GS}-V_{th} voltages. Dash lines are linear fits for power-law dependence coefficients gamma (γ).

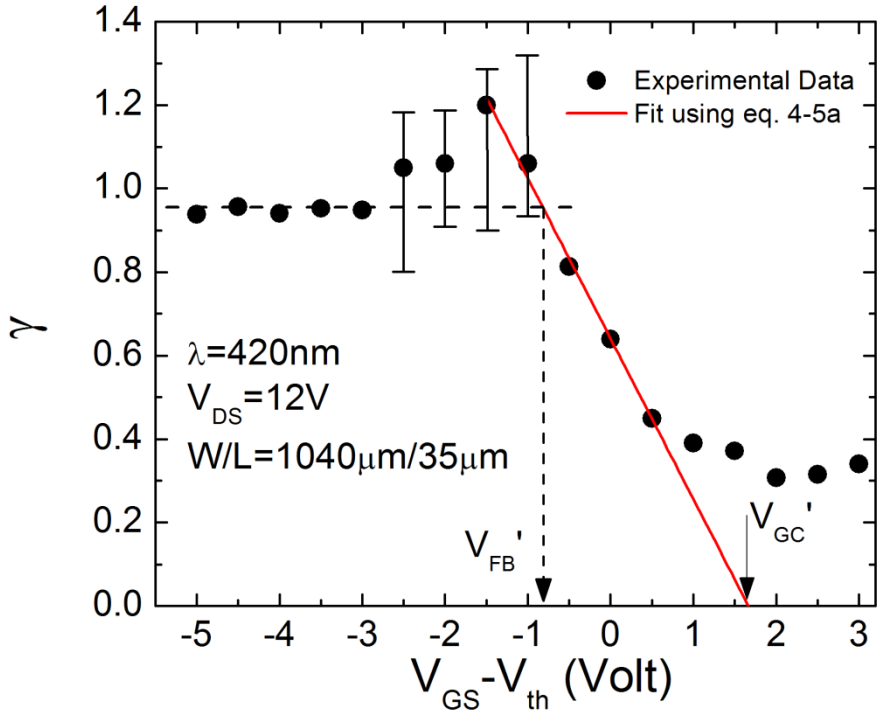
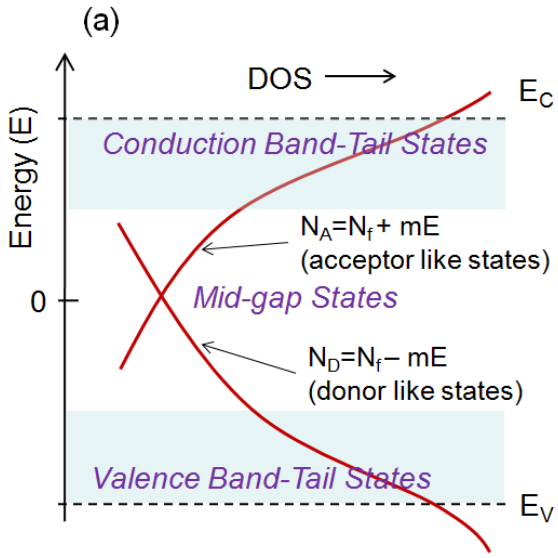


Figure 4.11 (Color) Gamma factor (γ) of PLD a-IGZO TFT versus V_{GS}-V_{th} at a wavelength of 420nm.

gate insulator (3.9 for SiO_2) and a-IGZO (=10), respectively; and ε_0 is permittivity in vacuum. To understand the physical origin of γ, we shall distinguish between three regions of V_{GS}: namely the region where V_{GS} is small or negative (TFT off-region), the region where V_{GS} is fairly large (saturation region), and the intermediate region. In TFT off-region, the band bending is close to its flat-band condition and γ mainly depends on the photocurrent due to the bulk region of semiconductor. Therefore, $\gamma \sim \gamma_0$ tends to be independent of V_{GS}. The electron–hole recombination is mainly monomolecular via recombination centers near mid-gap. Ideally, the γ_0 should be unity. Because of the continuous DOS near mid-gap, the measured γ_0 is usually lower than unity as the quasi-Fermi level sweeps through these states [81]. At a certain gate voltage (i.e. $V_{FB} < V_{GS} < V_{GC}$), the surface band banding begins. This effect opposes the raise of the quasi-Fermi level towards conduction band edge and as (4-5a) describes, γ values will appear to be lower. Under an even larger V_{GS}, because the space charge is now closer to the TFT channel surface, the surface band bending decreases. Eventually, the intensity dependence is diminished since the bands near the gate flatten almost as rapidly as quasi-Fermi level rises [85]. In our study, the γ of a-IGZO TFT saturates to a lower level of ~0.3 under high gate voltage.

Figure 4.11 shows the γ extracted from Figure 4.10 as a function of V_{GS}-V_{th} and the experimental data closely follow the analytical model (equation (4-5)). The γ_0 is extracted to be near 1.0 which indicates that a-IGZO TFT is efficiently converting the UV illumination to photocurrent in off-region. We then extracted the critical voltage (V_{GC}) and flat-band voltage (V_{FB}) to be 4.44V and 1.99V, respectively. In order to determine the mid-gap DOS characteristic slope *m*, we first determined the total mid-gap DOS, $2N_f$. In Section 2.2.3, we have discussed that the bulk DOS of a-IGZO can be estimated from TFT subthreshold swing. By assuming a sole contribution from bulk states in (2-4) [setting the



(b) DOS Extraction Results

Material	$2N_f$ ($cm^{-3}eV^{-1}$)	m ($cm^{-3}eV^{-2}$)
a-Si:H	10^{18}	2×10^{18}
a-IGZO	10^{17}	7.8×10^{16}

Figure 4.12 (a) Schematic of the simplified mid-gap DOS model used in photofield-effect analysis. (b) Extracted DOS parameters for a-Si:H [82] and a-IGZO (this study).

surface states (i.e. N_{SS}) equal to zero], we have

$$2N_f = \left(\frac{S\log(e)}{kT/q}-1\right)^2\left(\frac{n_{ins}}{n_{semi}}\right)\frac{n_{ins}\varepsilon_0}{(q\cdot d_{ins})^2} \tag{4-7}$$

where S is the TFT subthreshold swing. The $2N_f$ for our a-IGZO TFT is estimated to be ~10^{17} $cm^{-3}eV^{-1}$ (Figure 4.12(b)) which is consistent with the value (< 4×10^{17} $cm^{-3}eV^{-1}$) extracted using SPICE modeling [52]. By substituting all the parameters into (4-6), *m* is calculated to be 7.76×10^{16} $cm^{-3}eV^{-2}$. The extracted a-IGZO TFT mid-gap DOS is more than a order lower than the previously reported values for a-Si:H TFT [82]. This finding is supporting a good switching property of the a-IGZO TFTs that was experimentally observed by different laboratories across world.

Finally, we may estimate the electron lifetime (τ_n) by assuming the recombination process in a-IGZO is governed by the amount of donor-like states contained by both electron and hole quasi-Fermi levels (N_r). Under the TFT flat-band condition, τ_n can be written

as [81]

$$\tau_n = \frac{1}{N_r v_{th} \sigma_r} \approx \frac{1}{(2N_f \cdot \Delta E_f) v_{th} \sigma_r}, \quad (4\text{-}8)$$

where $2\Delta E_f$ is the energy separation between the two quasi-Fermi levels, v_{th} is the electron thermal velocity (~10^7 cm/sec at 300K), and σ_r is the coulombic cross-section for electron capture. Equation 4-8 implies that τ_n decreases with the increasing numbers of recombination centers $N_r \sim 2N_f \cdot \Delta E_f$. The energy separation ΔE_f can be calculated from the TFT drain current ratio under off region [81]

$$\Delta E_f = kT \cdot \ln\left(\frac{I_{D\_ill}}{I_{D\_dark}}\right); \quad (4\text{-}9)$$

and in this study, the ΔE_f is ~67.4meV at I=10μW/cm^2. Without further justification, we adopt a typical value of $\sigma_r \sim 10^{-17}$cm^2 and estimates the $\tau_n \sim 1.5\times10^{-6}$ sec for our a-IGZO TFTs. This estimated value is slightly longer than the carrier lifetime reported for a-Si:H TFT (~1.4μsec [87]) and the carrier lifetime in Au-diffused Si *pn*-junction device (0.25~0.75μsec [88]).

Chapter 5

Two Dimensional

Numerical Simulation of the a-IGZO TFT

5.1 A Brief Review of Earlier Works

During the past few years, there has been an increased interest in adapting amorphous In-Ga-Zn-O (a-IGZO) thin-film transistor (TFT) as next generation TFT technology for flat-panel displays [26, 27] or photo-imagers [53, 79]. Unlike covalent bond semiconductors (e.g. Si), the conduction-band of In-Ga-Zn-O primarily depends on the overlap of heavy metal ion *ns* orbitals, which appears to be insensitive to the crystal distortion in amorphous phase, leading to a higher mobility materials [39, 40, 42, 44]. Today, a-IGZO used in TFTs is deposited by pulse laser deposition (PLD) or magnetron sputtering. Such device has a field-effect mobility ranging from 8 to 20 cm^2/Vs, sub-threshold swing below 200 mV/dec, threshold voltage (V_{th}) around 0V and off-current below 1pA [48, 89-91].

To understand the device physics and the TFT operation principles, the numerical simulation is an indispensable tool. However, despite the remarkable advances in device fabrication there were only limited numbers of publications related to the numerical simulation of the a-IGZO TFT [67, 92]. The mid-gap density-of-state (DOS) models proposed for simulating a-IGZO electrical properties were fundamentally inherited from hy-

drogenated amorphous silicon (a-Si:H) with two components: the acceptor-like conduction band-tail states (g_{CBa}) and acceptor-like deep-gap states (g_{Da}) [57]. In the earlier work, g_{CBa} and g_{Da} were considered to have the exponential and Gaussian distribution, respectively [67]. After optimizing the numerical fit to current-voltage (I/V) characteristics of the a-IGZO TFT, the characteristic energy slope (E_a) of g_{CBa} was determined to be 80 meV for the enhancement mode device, while g_{Da} was observed to be very "flat", without a clear peak structure [67]. On the other hand, to simulate the electrical properties of the so called depletion mode TFT (negative threshold voltage), a shallower (E_a = 140 meV) g_{CBa} and a larger g_{Da} were used [67, 90]. In addition, the band mobility used for depletion mode TFT simulation was set to a higher value; a possible generation of oxygen vacancy and an increase in carrier mobility (which is proportional to the carrier concentration) were given as justification for this choice. The subsequent work proposed a simplified model by replacing the Gaussian distribution with the exponential distribution for g_{Da} [92]. Model parameters were than extracted from the optical response of capacitance-voltage (C-V) characteristics of the a-IGZO TFT, and the characteristic energy slopes of g_{CBa} and g_{Da} determined by this method were 125 meV and 1.4eV, respectively [92]. Although two different mathematical formula were used to describe g_{Da} , both works project a low g_{Da} concentration ~3×10^{16} $cm^{-3}eV^{-1}$ near the a-IGZO mid-gap ($E_C - E \sim 1.5eV$). In Chapter 4, the photofield-effect study conducted on a-IGZO TFT also reveals a similar result, which suggested that the a-IGZO mid-gap DOS can be described by a linear distribution and its value is an order lower than one reported for a-Si:H TFT [53].

Even though the numerical simulation can achieve adequate fit to the experimental I/V characteristics, our physical understanding of several a-IGZO properties is still rather poor. For example, so far the E_a has been treated as a fitting parameter without any physical

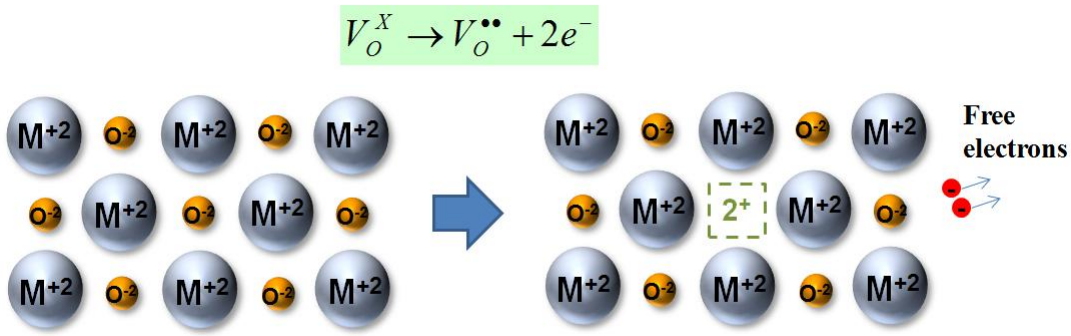


Figure 5.1 Schematic representation of the oxygen vacancy. Left: the ideal oxide (MO). Right: the oxide MO with an oxygen vacancy. M^{+2} and O^{-2} represent the metal cation and oxygen anion, respectively.

justification. It is well known that the broadened band-tail states are originated from the long range structural disorder of amorphous semiconductors [75] and the In-O-metal bond angles variation was suggested to be the physical origin of the conduction band-tail states in a-IGZO [35, 67]. Since the electron wave function is thought to experience minimum disturbance throughout the compound and the band conduction is still possible in a-IGZO [39], one would expect a much abrupt and sharper band-edge for a-IGZO with E_a smaller or at least compatible to value obtained for a-Si:H (E_a for a-Si:H is ~25meV).

The need to define different band mobility for various types of a-IGZO TFTs also makes the simulation process very complex and, from device physics' point of view, un-realistic. It is known that due to the existence of band-tail states, only portion of the total induced charges can participate in electrical conduction [93]. As a result, TFT field-effect mobility is proportional to the total induced charge concentration (or gate voltage), and such effect has been study in a-Si:H TFT with the numerical simulation [94]. The band mobility used in numerical simulation should be kept as a constant unless the material structure is suspected to be seriously modified during device operation.

Finally, the nature of oxygen vacancy (OV) states should be carefully reviewed (i.e. donor-like or acceptor-like states should be considered). To maintain the electro-neutrality of compound, the oxygen vacancy (OV) states are "positively charged" rather than neutral when they are not filled by electrons (Figure 5.1). It is clearer when the defect equation for an OV is written in Kröger-Vink notation as: $V_O^X \rightarrow V_O^{\bullet\bullet} + 2e^{'}$ [95]. The above equation describes an OV acting as a donor and becomes doubly charged. Symbol *V* stands for the vacancy, subscript *O* represents the oxygen atom site while the superscript *X*, " • ," and " ' , " represent neutral, positive or negative charge states, respectively.

To address all these issues, in this chapter, we report an improved modeling approach for radio frequency (RF) sputter a-IGZO TFTs. Section 5.2 presents the detail device structure and mathematical DOS models used in two-dimensional (2-D) numerical simulation. The simulation results are summarized in Section 5.3. The impact of DOS, source/drain (S/D) contact resistance, and OV states on TFT electrical properties will be discussed in Chapter 6.

5.2 Two Dimensional (2D) Numerical Simulation [96]

5.2.1 a-IGZO TFT structure used in simulation

A 2D inverted-staggered a-IGZO TFT structure used for numerical simulation is shown in Figure 5.2 and the inset of Figure 5.4(c), and it is designed to match with actual TFT used in this study. (Key processing steps are provided in Section 2.1.2. It should be noticed that there is no passivation layer in the device used in this study.) The structure consists of a 20nm thick a-IGZO active layer and a 100nm thick thermal SiO_2 gate insulator layer.

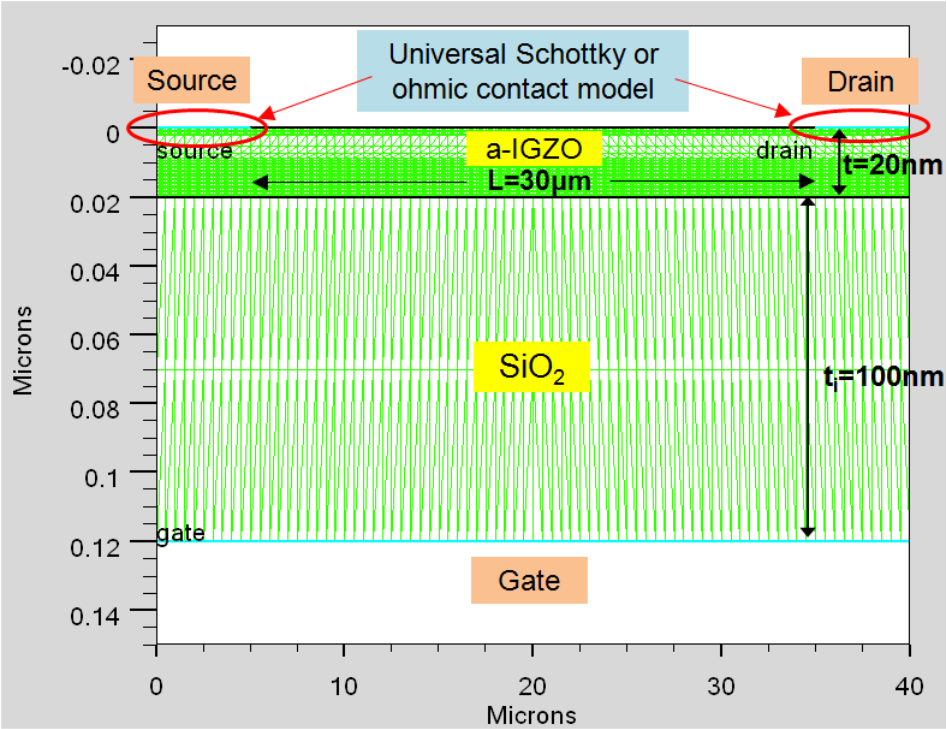


Figure 5.2 (Color) The cross section of inverted-staggered a-IGZO TFT structure used in the numerical simulation. Mesh/grid points are also shown in this figure.

During the 2D simulation, the program only calculates the distribution of physical properties along the channel length (L) direction. An ideal, uniform distribution is assumed along the channel width (W) direction. The TFT (L) and (W) are 30µm and 180µm, respectively. To model the unpassivated a-IGZO TFT, the homogeneous Neumann boundary condition [97] is applied to the back-channel surface of the a-IGZO layer. Such boundary condition prevents carriers from flowing outside of the back-channel surface and ensures the current only flows in/out of device through source/drain contacts during simulation. Note that both front and back-channel surfaces of the a-IGZO layer are assumed to be ideal and no interface states are included. The post-thermal annealing step during TFT fabrication is considered to improve the interface quality. This can be further justified by the very low subthreshold swing (S=0.13V/dec) and hysteresis ($\Delta V < 0.2V$) observed in TFT output

properties. Therefore, the contribution from interface states is thought to be minor in this investigation. To facilitate the discussion of quantities with the different geometrical directions of interest, *X*-direction is defined as the channel length direction and *Y*-direction is set to be perpendicular to the TFT surface. In addition, since the degenerate conduction might occur in a-IGZO TFT [38, 43], the Fermi-Dirac statistics is used in numerical simulation.

5.2.2 Source/drain contacts, electronic affinity and band mobility of the a-IGZO

Contacts between source/drain (S/D) electrodes and a-IGZO layer were either assigned as ohmic or Schottky in nature in this work (Figure 5.2). In ohmic contact model, the ideal Dirichlet boundary condition was used [97] and an additional heavily n-type doped (n^+) layer was added at the metal contact/a-IGZO interface. For Schottky model, S/D metal work function (Ti, Φ_{Ti}=4.33eV) and electron affinity of a-IGZO ($\chi_{a\text{-}IGZO}$) were included in calculation. Both thermionic emission and tunneling current were considered [97]. Throughout Chapter 5 and 6, unless otherwise specified, the Schottky contact model is used as default in numerical simulation. Because the $\chi_{a\text{-}IGZO}$ value is not available yet in literature by the time this thesis is written, we estimate the $\chi_{a\text{-}IGZO}$ from a simple linear relation between electron affinities of its three elementary compounds (χ with the compound name indicates as a subscript),

$$\chi_{a-IGZO} = a\left(\chi_{In_2O_3}\right) + b\left(\chi_{Ga_2O_3}\right) + c\left(\chi_{ZnO}\right), \tag{5-1}$$

where a, b and c are molar percentage (% mol); $\chi_{In_2O_3}$, $\chi_{Ga_2O_3}$ and χ_{ZnO} are 4.45eV [98], 3.19eV [99, 100] and 4.5eV [101], respectively. In addition, to maintain a total of 100% molar percentage, a + b + c = 1. For a-IGZO with atomic ratio of In : Ga : Zn = 1 : 1 : 1 (thus

a : b : c =1 : 1 : 2. a, b and c are 0.25, 0.25 and 0.5, respectively), the $\chi_{a\text{-}IGZO}$ was calculated to be 4.16eV. For comparison, Jeon *et al.* [92] adopted the Schottky barrier height of 0.36eV ($\Phi_b=\Phi_{Mo}-\chi_{a\text{-}IGZO}$) between the a-IGZO and molybdenum electrodes (Mo, Φ_{Mo}=4.6eV) in numerical simulation. Based on our calculation, the Φ_b of Mo/ a-IGZO is 0.44eV, which is very close to their value.

We set the electron band mobility (μ_n=15 cm^2/Vs) to be the maximum mobility calculated from TFT transconductance [$\mu_{inc\text{-}MAX}$, cf. equation (6-3)]. The μ_n is compatible with the Hall mobility (μ_{Hall}) extracted from Hall-effect measurements where μ_{Hall}=17 cm^2/Vs at free carrier concentration of 7.8×10^{19} cm^{-3}. As a comparison, these mobility values are slightly higher than the Hall mobility (~12 cm^2/Vs) reported for a-IGZO deposited by PLD [40]. The difference is thought to be due to the higher Indium composition ratio (X-ray fluorescence measurement showed the composition of In:Ga:Zn=1:1:0.7 in atomic ratio for a film deposited by sputtering with an In:Ga:Zn=1:1:1 target.) and/or lower trap density of the RF sputter a-IGZO thin film. Primarily due to its strong intrinsic *n*-type nature, by the time this paper is written, *p*-type conduction of a-IGZO has not yet been reported. Most metal oxides have a strong localization behavior of positive hole at valence-band edge to a single oxygen atom that prevent hole from freely moving within the crystal lattice [102]. As a result, the substitutional doping only yields a deep acceptor level (rather than a shallow one) causing the difficulty in achieving *p*-type conduction, and the hole mobility is much lower than electron mobility. We believe that a similar situation also exists in a-IGZO [Note: Although a high mobility p-type conduction has been reported, it only exists in metal oxides with cations that can potentially promote an extended valence-band structure (e.g. Cu^+, Ag^+ or Au^+) [103]]. Therefore, to properly determine the hole mobility (μ_p), we refer to the existing knowledge on ZnO, which is considered to have

properties similar to those of a-IGZO. In this study, the hole band mobility (μ_p) is chosen to be 0.1 cm^2/Vs, which is close to the values reported for p-type ZnO prepared by PLD (0.05~0.4 cm^2/Vs) [104, 105]. Higher μ_p values (up to 2 cm^2/Vs) were also tried in simulations but we observed no appreciable discrepancy in the results (data not shown). This suggests the electron conduction is the dominated mechanism in our a-IGZO TFT simulation.

5.2.3 a-IGZO TFT density-of-states (DOS) model

We also developed DOS model for a-IGZO based on several published results. Takagi *et al*. [40] extracted the a-IGZO conduction band effective mass (m_c) to be ~0.34 m_e (m_e is the mass of free electron) by combining the free carrier absorption spectrum with the results of the Hall effect measurement. We further calculated the effective conduction band DOS (N_c) to be $5\times10^{18}cm^{-3}$ at room temperature (300K) using

$$N_C = 2\left(\frac{2\pi m_c kT}{h^2}\right)^{3/2}, \tag{5-2}$$

where kT=26meV and h is the Planck constant [106].

The increasing structural disorder within amorphous material can induce electron scattering and eventually localized wave-functions. Such phenomenon can be approximately represented as localized tail states within band gap, near the band edges [57, 75]. In a-IGZO, the conduction band-tail states (g_{CBa}) are thought to be originated from the disorder of metal ion *s*-bands [107] (i.e. In-O-metal bond angles variation [67]). Nomura *et al.*[108] proposed that the tail-like structures observed in the a-IGZO absorption spectra should originate from sub-gap DOS near valence band maximum (VBM) by comparing it with the hard X-ray photoelectron spectroscopy (HX-PES) spectra. Kamiya *et al.* [109]

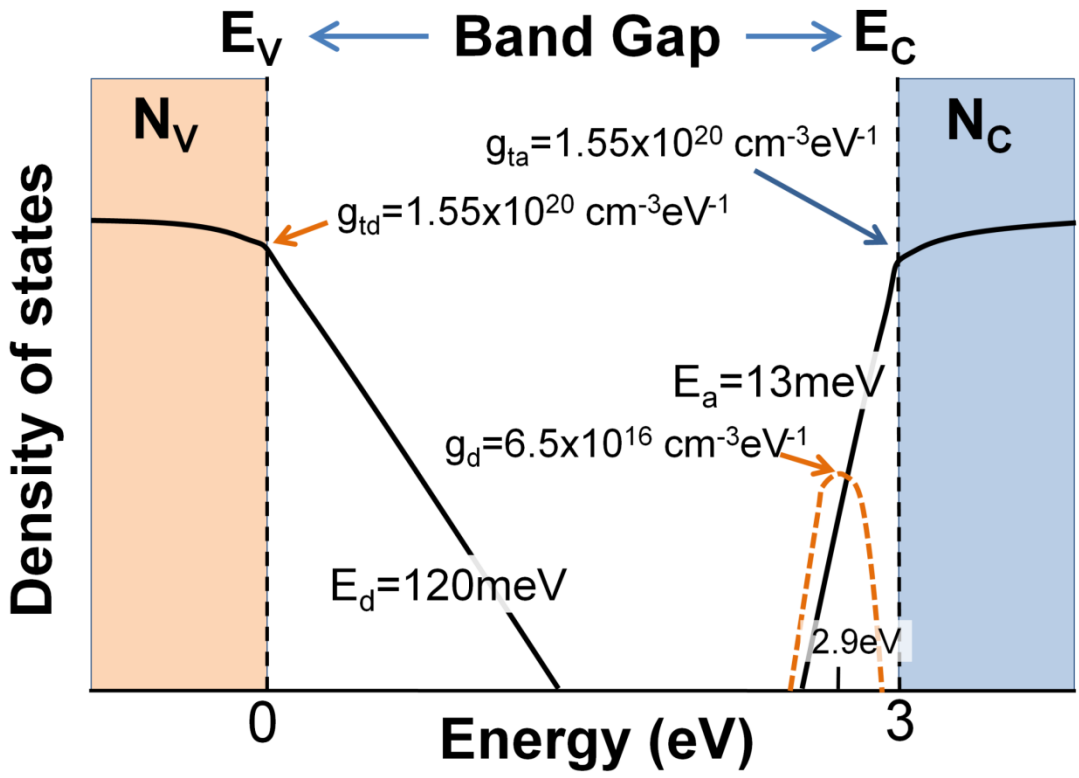


Figure 5.3 (Color) Proposed DOS model for a-IGZO. E_C and E_V are conduction and valence band-edge energies, respectively. Solid curves within band-gap represent the exponentially distributed band tail states (g_{CBa}, g_{VBd}), while the dash curve near the conduction band edge represents the Gaussian-distributed donor-like OV states (g_{Gd}).

speculated that these valence band-tail states (g_{VBd}) formed because the disordered atomic configuration in a-IGZO breaks the coherent hybridization of oxygen 2*p* orbitals that mainly form valence band in oxides. In this study, band tail states of the a-IGZO are represented as a function of energy (E) by following expressions (Figure 5.3):

$$g_{CBa} = g_{ta} \exp\left[\left(E - E_C\right)/E_a\right], \tag{5-3}$$

$$g_{VBd} = g_{td} \exp\left[\left(E_V - E\right)/E_d\right], \tag{5-4}$$

where E_C and E_V are conduction and valence band edge energy, g_{ta} and g_{td} are density of acceptor- and donor-like states at $E=E_C$ and $E=E_V$, respectively, and E_a and E_d are cha-

racteristic slopes of conduction and valence band tail states, respectively. To determine the proper range for g_{ta} , we considered the fact that the DOS has a continuous distribution from tail states to extended states (i.e. states located above E_C or below E_V in Figure 5.3). Therefore, it is reasonable for N_C (or N_V) and g_{ta} (or g_{td}) to have a proportional relation. Since N_C of the a-IGZO (~5×10^{18}cm^{-3}) is about an order smaller than a-Si:H (N_C for a-Si:H is ~ 3×10^{19} cm^{-3}), we assumed g_{ta} of the a-IGZO to be around 10^{20} cm^{-3}eV^{-1} (g_{ta} for a-Si:H is 10^{21} cm^{-3}eV^{-1}) [57]. It should be noticed that the range of g_{ta} and g_{td} determined by this method is consistent with those extracted from X-ray photoelectron spectroscopy expe-riments (~5×10^{19}cm^{-3}) [108]. The band gap (E_g) and valence-band-tail slope (E_d) were further extracted from optical absorption measurements (Ref: Section 4.3 and [74]). For simplicity, the deep-gap states of a-IGZO were not considered in this study. This is justified by a very low deep-gap state concentration of the a-IGZO (conclusion of Section 4.6 and Ref. [53]) and a good numerical fits to the experimental data using proposed DOS model. Although numerically, adding the acceptor-like deep-gap states can cause a positive shift in TFT transfer properties, we didn't observe a need to do so in this work. In addition, the deep-gap properties of a-IGZO are still not well understood and we don't feel competent to provide the physical justification for considering such states in simulation.

Oxygen vacancy (OV) can also alter the electrical properties of oxide semiconductors. It has been pointed out in the previous section, OV can act like a donor and is double po-sitively charged when fully ionized ($V_O^X \rightarrow V_O^{\bullet\bullet} + 2e^{'}$). Not only could these vacancies exist in the as-deposited film, but as what has been proposed recently [110], the trace O-H bonds in a-IGZO thin film could react with each other and cause additional OV, such as, $M-OH+M-OH \rightarrow V_O^{\bullet\bullet} + M-O-M + H_2O\uparrow + 2e^{'}$, where M is the metal cation.

Although this defect reaction is more complex, the charge state of OV remains the same (+2), and this implies that they can all be modeled as donor-like states.

The energy distribution of OV states is also important. OV states with different degrees of structural relaxation around the vacancy have been simulated by first-principle calculation and found to have different energy levels [111, 112]. Local density approximation (LDA) calculation of the a-IGZO has also shown that the energy level of OV states is located near the conduction band minimum (CBM) for a highly relaxed atomic structure that can be realized by post thermal annealing or proper film growth process. On the other hand, if there is no structural relaxation involved, the spatially localized OV state has an energy level closer to mid-gap or even valence band minimum (VBM) [112]. However, since the LDA severely underestimated the band-gap energy, the study is only qualitative and the exact energy level of OV state required further study.

The RF sputter a-IGZO film used in this work was first deposited on an unheated substrate in the O_2/Ar atmosphere (total pressure of 0.5Pa) with O_2/Ar gas pressure ratio of ~5%, followed by a post-annealing of 300^0C for 20 minutes in air. Because our a-IGZO has been through a thermal annealing process, we assumed the near-CBM OV states are dominant in this study, and we use a Gaussian-distributed donor-like state to model the OV in a-IGZO:

$$g_{Gd} = g_d \exp\left(\frac{-(E-\lambda)^2}{\sigma^2}\right), \tag{5-5}$$

where g_d, λ and σ are peak value, mean energy and standard deviation of states, respectively. The OV states were placed near CBM with λ=2.9eV as a default, but the impact of different energy levels on TFT electrical properties was also investigated. In addition, the energy level of OV states is assumed to be unchanged after the states are filled with the

electrons. It should be noticed that although the numerical simulation can directly assign the doping to the a-IGZO, it is not possible to simulate the complex carrier trapping behavior of OV states by this approach. To sum up, the schematic of the proposed a-IGZO DOS model is illustrated in Figure 5.3. During simulation, the DOS equations are model with discrete energy levels [97]. Even though a large number of energy levels can promise a better accuracy, it can also increase the calculation time significantly. In this study, we optimized the setting to 128 and 64 levels for acceptor and donor-like states, respectively (or Acc./Don.=128/64 levels). Compared to this optimized setting, simulation with larger number of energy levels (e.g. Acc./Don.=1000/500 levels) show a marginal difference in drain current (~40nA) which only occurs in TFT on-region.

5.3 Simulation Results and Discussion

The experimental data were measured for the a-IGZO TFT with a common gate, inverted-staggered structure. Readers who are interested in the TFT fabrication should refer to Section 2.1.2. All the parameters extracted from experimental data used in this numerical simulation are listed in Table 5.1. The listed threshold voltage (V_{th}) and field effect mobility (μ_{eff}) and subthreshold swing (S) were all extracted by methods depicted in Section 2.2.1. A nonlinearity of I_D vs. V_{GS}, which is associated with g_{CBa}, was observed and will be discussed in Chapter 6.

Highly accurate output (RMS error < 8μA), transfer (< 26nA) and sub-threshold (<17nA) a-IGZO TFT experimental characteristics were reproduced by our model (Figure 5.4). Simulation results based on the source/drain ohmic contact models are also shown in Figure 5.4. Ohmic contact model only gives a slightly higher drain current (for example,

Symbol	Value	Unit	Description
N_c	5×10^{18}	cm^{-3}	Effective conduction band DOS
N_v	5×10^{18}	cm^{-3}	Effective valence band DOS
g_{ta}	1.55×10^{20}	$cm^{-3}eV^{-1}$	Density of tail states at $E=E_c$
g_{td}	1.55×10^{20}	$cm^{-3}eV^{-1}$	Density of tail states at $E=E_v$
E_a	13	meV	Conduction-band-tail slope
E_d	120	meV	Valence-band-tail slope
E_g	3.05	eV	Band gap
χ	4.16	eV	Electronic affinity
ε	10		Permittivity
μ_n	15	cm^2/Vs	Band mobility (electron)
μ_p	0.1	cm^2/Vs	Band mobility (hole)
m_c	0.34	m_e	Conduction band effective mass
g_d	6.5×10^{16}	$cm^{-3}eV^{-1}$	Peak of OV states
λ	2.9	eV	Mean energy of OV states
σ	0.1	eV	Standard deviation of OV states
a-IGZO TFT Properties			
μ_{eff}	12.4	cm^2/Vs	Field effect mobility
V_{th}	1.15	V	Threshold voltage
S	0.13	V/dec	Sub-threshold swing
I_{off}	$<10^{-14}$	A	Off current
	10^{10}		On/off current ratio

Table 5.1 Key simulation parameters and properties of common gate, inverted-staggered a-IGZO TFT.

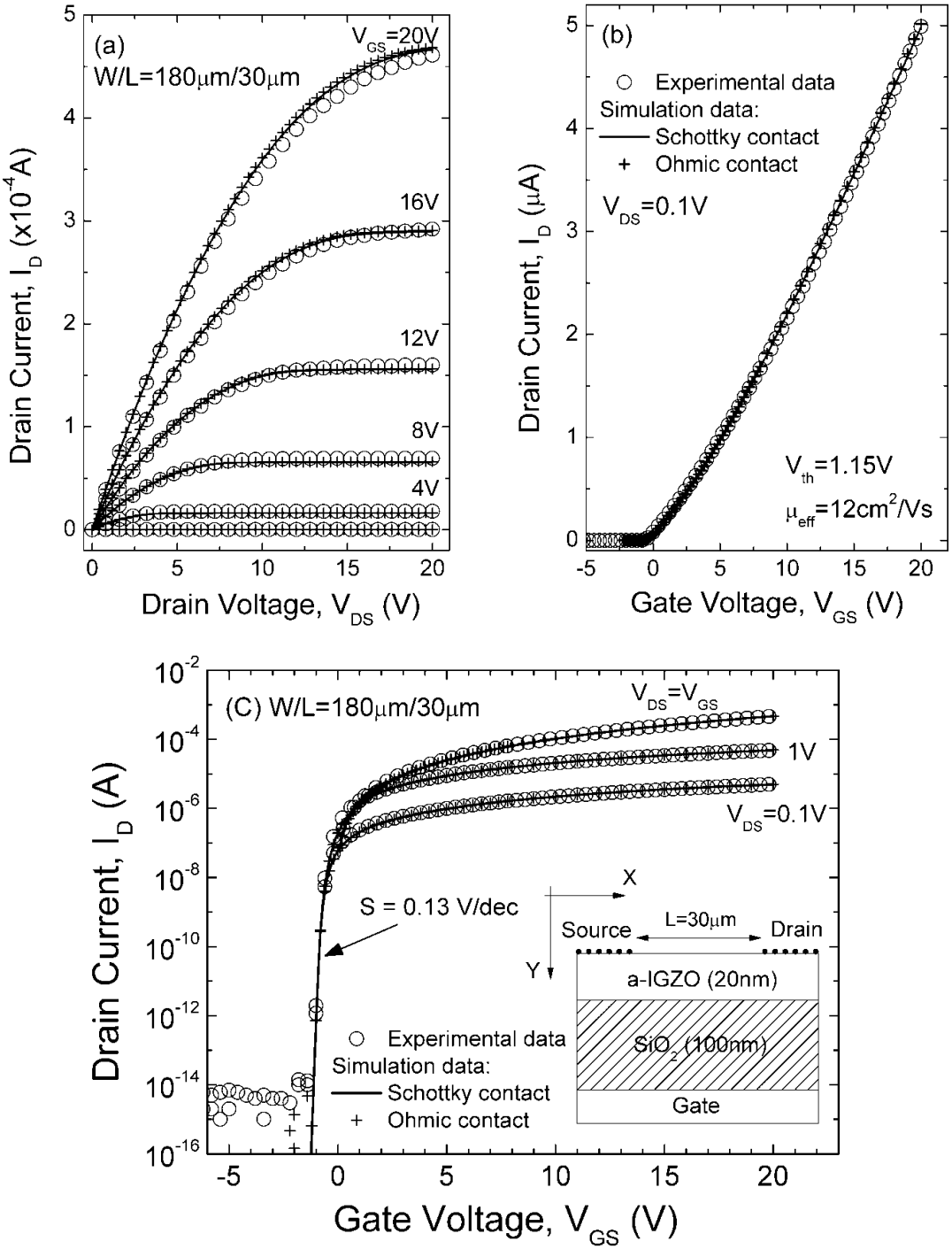


Figure 5.4 a-IGZO TFT: (a) output and [(b) and (c)] transfer characteristics (W/L= 180/30μm). Both experimental (○) and simulation data (solid line: Schottky contact; +: Ohmic contact) are shown. Extracted threshold voltage (V_{th}), field-effect mobility (μ_{eff}), and subthreshold swing (S) are also indicated. Inset of (c): the 2D TFT structure used in simulation. This structure is further decomposed into smaller mesh structures for a finite element analysis.

less than 1% increase under linear region) in comparison to Schottky (Ti) contact model. This suggests that the Schottky barrier height ($\Phi_b=\Phi_{Ti}-\chi_{a\text{-}IGZO}$ = 0.17eV) for Ti S/D metal is small, and Ti is forming ohmic-like contact with the a-IGZO layer.

To better understand the a-IGZO TFT operation, the cross sectional view of simulated drain current flow (vector plot) near the drain electrode, when a-IGZO TFT is operated under a linear region (V_{DS}=0.1V, V_{GS}=20V), is illustrated in Figure 5.5. The free electron concentration (n) is also shown as a contour plot. The results reveal a high concentration of free electrons ($n>10^{19}cm^{-3}$) accumulated near the gate insulator/a-IGZO interface; this "channel layer" carries the majority of the drain current. In addition, the channel current flow extends about 0.7μm below the drain electrode, which is approximately similar to the transfer length (L_T ~ 0.5μm) extracted from the analysis of gate voltage dependent series resistance (Section 3.1.2). The dependences of n and current density (J) on V_{GS} were also studied. Figure 5.6(a) and (b) show simulated distribution of n and the x-component of the current density (J_X) at the center of the a-IGZO TFT structure. When the TFT is operated in on-region ($V_{GS}>V_{th}$), a non-negligible amount of electrons accumulate near the back channel ($n\sim10^{17}cm^{-3}$) that corresponds to about 0.1μA/(μm)^2 of drain current. Hence the back channel current can contribute a major portion of total channel current at a low V_{GS} condition. Therefore, it is important / critical to passivate back channel in a-IGZO TFTs. It should be notice that the *Y*-component of the current density (J_Y) is essentially zero compare to J_X. Therefore, the current is flowing uniformly along the channel length direction at the center of the device. In fact, the 20nm thick a-IGZO layer is very thin, so the Fermi-level (E_F) of the entire film is moving toward the conduction band (E_C) in subthreshold region (Figure 5.6(c)). Hence, the conventional assumption of back channel as "bulk" with E_F position being same as it is under thermal equilibrium is not valid here. In the on-region,

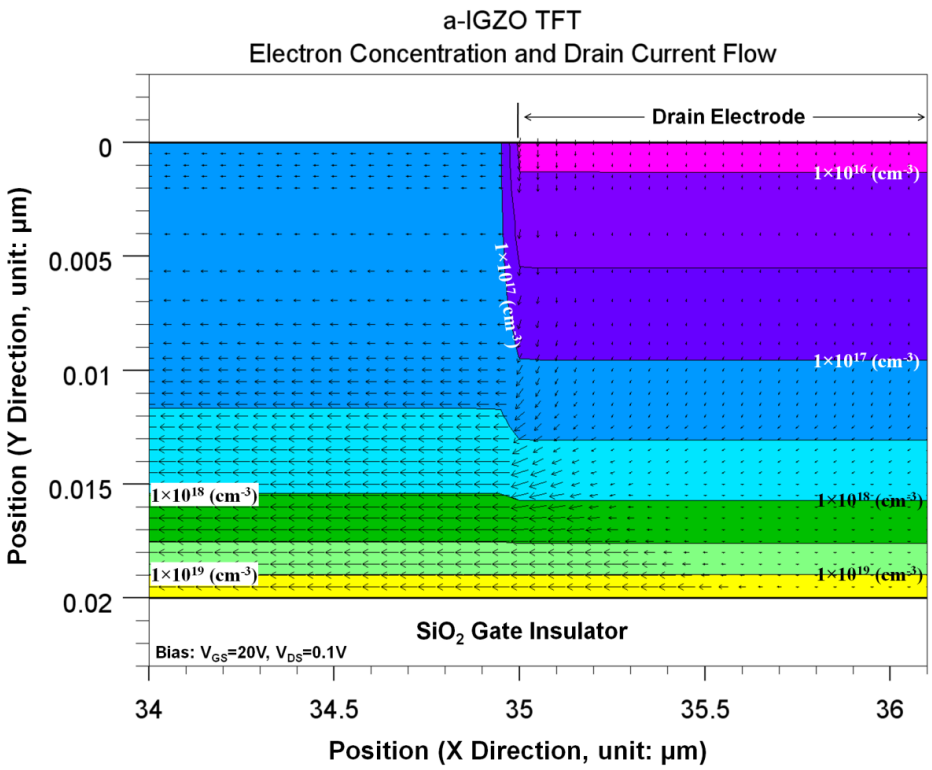


Figure 5.5 (Color) A zoom-in view of the simulated TFT structure near the drain electrode. The contour distribution of free electron concentration within a-IGZO layer is shown. The *X*-direction is parallel to the TFT channel length direction, while the *Y*-direction is perpendicular to the device surface. The arrow represents the vector data for current density at each mesh grid point, and the length of the arrow is proportional to the magnitude of the current density. (Bias condition: V_{GS}=20V and V_{DS}=0.1V.)

the E_F of back channel is approximately pinned at 0.1eV below E_C, and the band bending starts to occur near the a-IGZO/SiO_2 interface (front channel) as V_{GS} increased. The degree of band bending increases with the V_{GS} and the E_F can move into the E_C under a high V_{GS} condition (i.e. $E_C - E_F < 0$V at V_{GS}=20V). This suggests that a high electron concentration channel layer in a-IGZO illustrated in Figure 5.5 is in its degenerate state, which is an important factor to achieve a high-performance TFT. Our simulation results also provide the physical insight of the sensitive dependence of the a-IGZO TFT I/V properties on back channel conditions reported by other groups [113, 114].

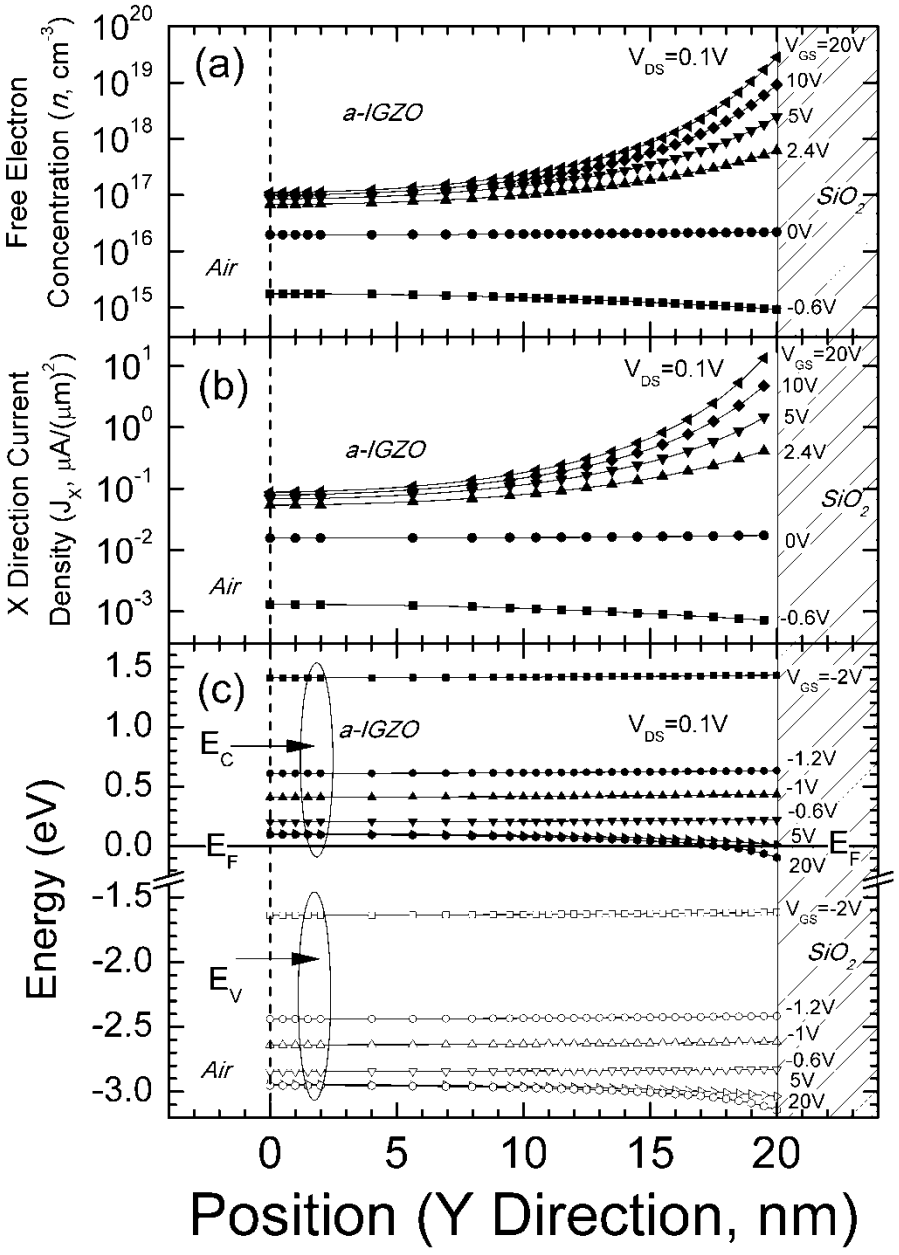


Figure 5.6 Simulated distribution of (a) free electron density (n) and (b) *X*-direction current density (J_x) at the center of the a-IGZO TFT structure. Gate voltage was changed from -0.6 up to 20 V. The film thickness of a-IGZO is 20nm. Position *Y*=0 represents the back channel surface while *Y*=20 nm represents the interface between a-IGZO and SiO_2 gate insulator. (c) Simulated energy band bending diagram at the center of TFT structure. The electron quasi Fermi-level (E_F) were used as reference energy level for all simulation results (energy = 0 eV). The gate voltage was changed from -2 up to 20 V. Closed symbols: conduction band edge energy (E_C); open symbols: valence band edge energy (E_V).

Chapter 6

Impact of Defect States and Contact Resistances on a-IGZO TFT Electrical Properties

6.1 The Impact of Conduction Band-Tail Slope (E_a)

As one of the important factors that determine the TFT electrical properties, the conduction band-tail states (g_{CBa}) originate from the In-O-metal bond angles variation in a-IGZO [67]; and the lower conduction band tail slope (E_a) values are associated with a-IGZO film having an enhanced short-range order or vice versa. In this section, we study the impact of E_a on a-IGZO TFT performance by utilizing the 2D numerical simulation model developed in Chapter 5. Multiple TFT transfer characteristics are simulated for different E_a ranging from 13 to 35meV. All other simulation parameters (including oxygen vacancy parameters: g_d, λ and σ) are kept constant as their default values listed in Table 5.1. The simulated linear region I/V data (V_{DS}=0.1V) for various E_a values are shown in Figure 6.1. The simulation indicates that a higher E_a could induce a significant decrease in TFT drain current/field-effect mobility and a positive shift in V_{th} extracted by ideal MOSFET model (Figure 6.3(b)). To clarify its physical origin, the band-bending near the a-IGZO/SiO_2 interface for different E_a was first investigated. The Fermi-level position relative to the conduction band-edge (E_C-E_F) is plotted as a function of V_{GS} (Figure 6.2(a)).

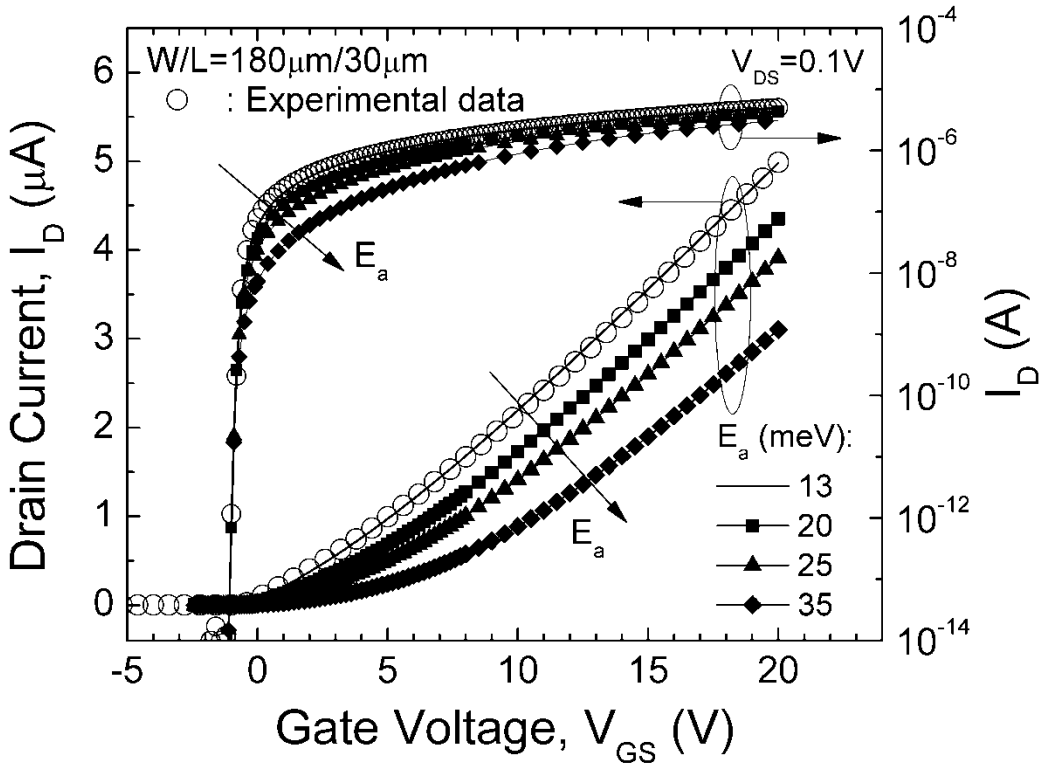


Figure 6.1 Simulated a-IGZO TFT linear region transfer curves for both linear and semi-logarithm scales for various E_a values are shown. The experimental data (symbol: ○) are also shown.

Clearly, the movement of E_F toward E_C is smaller for TFT with a higher E_a and it will take a higher V_{GS} to reach the same amount of the E_C-E_F. Such effect is directly related to the increase in g_{CBa}. As a result, the maximum achievable band-bending decreases, which lowers free electron concentration in the conducting channel and reduces the drain current.

Beside the reduction of I_D, the observed non-linearity of I_D-V_{GS} was also investigated. In Section 3.2, the gate voltage dependent filed-effect mobility (μ_{eff} (V_{GS})) has been adopted to describe the non-linear a-IGZO TFT I/V behaviors:

$$\mu_{eff}(V_{GS}) = K(V_{GS} - V_{th})^{\alpha} \quad . \tag{6-1}$$

In the above equation, α is the exponent to account for voltage dependence and K is a

material dependent constant. It is believed that, for a-IGZO TFT, portion of the total induced channel charges (electrons) are trapped in band tail states and cannot contribute to the I_D. As V_{GS} increased, more free electrons are able to contribute to the I_D and this makes μ_{eff} to increases with V_{GS} with a non-ideal condition of $\alpha > 0$ (or $\gamma > 1$). By introducing equation (6-1) into the standard MOSFET model, the non-linear drain current equation can be derived,

$$I_D = KC_{ox}\frac{W}{L}(V_{GS} - V_{th})^{\gamma} V_{DS}, \tag{6-2}$$

where $\gamma \equiv \alpha + 1$. As a comparison, in ideal case (i.e. there is no band tail state and all the induced electrons are able to participate in drain current conduction), $\alpha = 0$ (or $\gamma = 1$) and μ_{eff} (or K) is equal to the electron band mobility (μ_n). The gamma factor (γ) can be extracted from the field-effect mobility calculated from TFT transconductance (e.g. incremental field-effect mobility or μ_{inc}) using following mathematical relation:

$$\mu_{inc} = \left(\frac{\delta I_D}{\delta V_{GS}}\right)\frac{L}{WC_{ox}V_{DS}} = K\gamma(V_{GS} - V_{th})^{\gamma-1}. \tag{6-3}$$

The complete derivation of (6-3) has been provided in Section 3.2. We followed a two step process, as depicted in Section 3.2.3, for parameter extraction: the V_{th} is first determined as the V_{GS} value at which maximum $\delta\mu_{inc}/\delta V_{GS}$ occurs (i.e. $V_{th}=V_{max}$); then K and γ are extracted from the best linear fit of $\log(\mu_{inc})$ vs. $\log(V_{GS}-V_{th})$ plot based on (6-3) (data not shown). As illustrated in Figure 6.2(b), the field-effect mobility is actually a function of V_{GS}. It increases with V_{GS} and for the case of E_a=13meV, approaches the band-mobility ($15cm^2/Vs$) when V_{GS}=20V. The dependence of μ_{inc} on E_a is also included in Figure 6.2(b), and a significant decrease in μ_{inc} is observed for higher E_a. It is consistent with the μ_{eff} values extracted from the ideal MOSFET model (data not shown): compared with the

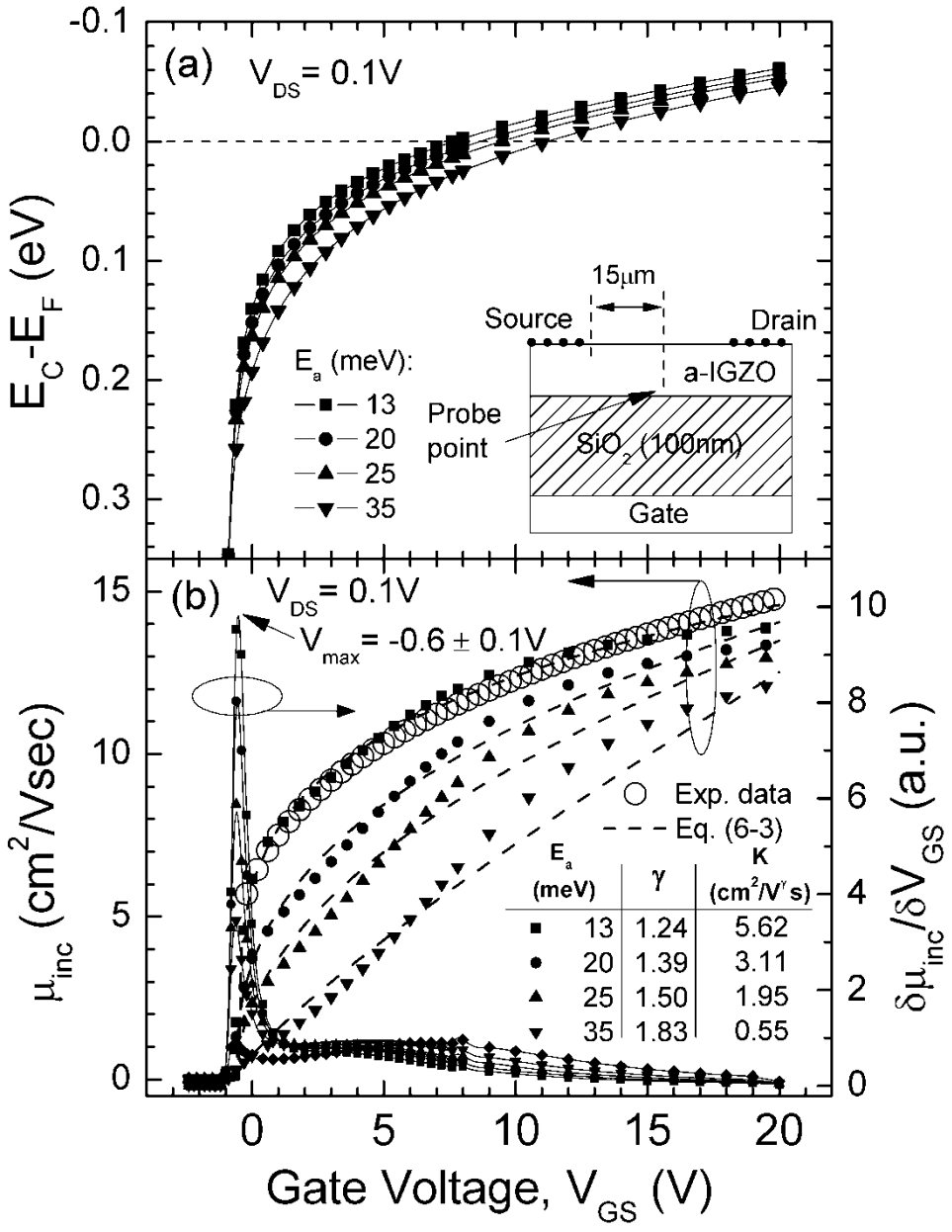


Figure 6.2 (a) Simulated a-IGZO Fermi-level position vs. gate voltage (V_{GS}). The Fermi-level position is represented as $E_C - E_F$, where E_C and E_F are energies for conduction band-edge and Fermi level, respectively. The inset indicates the probe point for this data and it is located at the center of the TFT, near (0.5nm away from) the a-IGZO/SiO_2 interface. The slight off-set is to avoid the calculation discontinuity which might occur at the interface. (b) The μ_{inc} and $\delta\mu_{inc}/\delta V_{GS}$ extracted from simulated a-IGZO TFT transfer characteristics for various E_a values. The experimental data (symbol: ○) are also shown. Dash lines are the model fitting curves based on (6-3), and the parameters used in the model are illustrated in the inset.

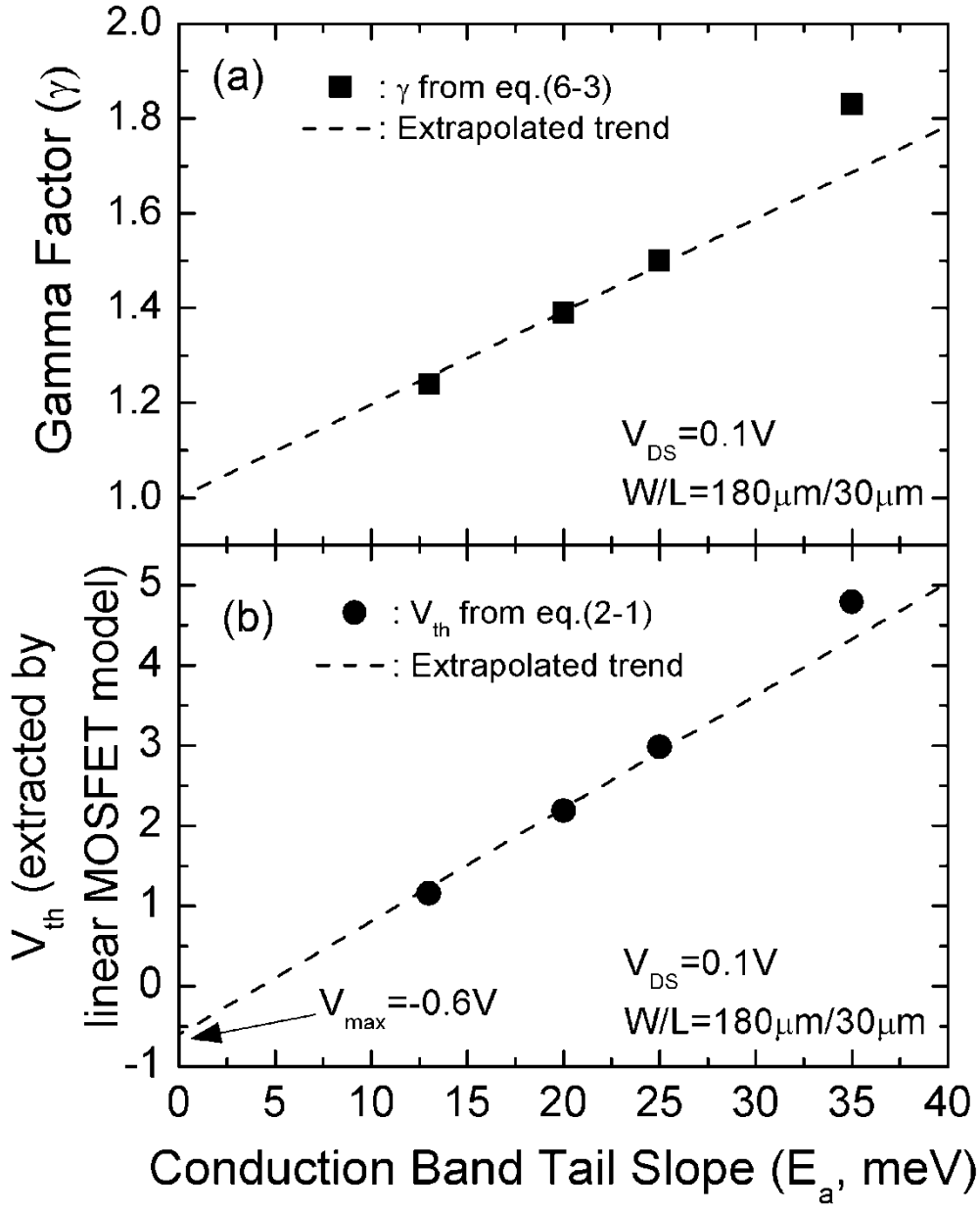


Figure 6.3 Simulated evolution of (a) gamma factor (γ) and (b) threshold voltage (V_{th}) as a function of conduction band-tail slope (E_a). The V_{th} is extracted by the ideal MOSFET model (2-1). Dash lines are extrapolated trends which indicate the limits when E_a= 0meV.

μ_{eff} =12.4cm^2/Vs at E_a=13eV, there is about 26% reduction in μ_{eff} (9.1cm^2/Vs) at E_a=35eV. Figure 6.3(a) illustrates the γ factors as a function of E_a. Although the simple power law dependence of (6-1) is not able to accurately model the complex V_{GS} dependence of μ_{inc} for higher E_a (i.e. 35meV), it still shows that the higher γ-values (e.g. γ=1.83 when E_a=35meV) are obtained as compared to the one extracted for lower E_a (e.g. γ=1.24 when E_a=13meV). This suggests that the degree of I_D-V_{GS} non-linearity increases with E_a. Consequently, the filed-effect mobility has a stronger dependence on V_{GS}; and as shown in Figure 6.3(b), there is a positive shift in V_{th} extracted by ideal MOSFET model. For example, the V_{th} extracted from (2-1) significantly shifts from 1.15V (for E_a=13meV) to 4.79V when E_a= 35meV. On the other hand, the V_{th} extracted from V_{max} in Figure 6.2(b) is fairly constant (~ -0.6V) for all E_a values (13meV~ 35meV). This gate voltage (-0.6V) correlates to E_C-E_F of 0.22 to 0.26eV where the E_C-E_F vs. V_{GS} starts to have a strong dependence on E_a (Figure 6.2(a)). (In Figure 6.5, the corresponding total ionized acceptor-like states ($n^-_{acceptor}$) range from 10^{15} to 10^{16} cm^{-3}.) Therefore, in this simulation the V_{max} is able to consistently be associated with the V_{th} point at which E_F is reaching the raising edge of conduction band-tail states in spite of the increasing non-linearity in I-V characteristics. This condition cannot be observed when V_{th} is extracted from the ideal MOSFET model (i.e. (2-1)). From Figure 6.3, we might extrapolate the limits of γ and V_{th} at E_a=0meV. The γ clearly approaches the ideal unity when E_a=0meV, which implies a perfectly linear I_D-V_{GS} relation. Thus, as expected, the V_{th} extracted by MOSFET model will converge to V_{max} of -0.6V at E_a=0meV.

Figure 6.4 provides an overview of the space charge distribution near the a-IGZO/SiO_2 interface during TFT operation. Total available donor-like and acceptor-like states are both

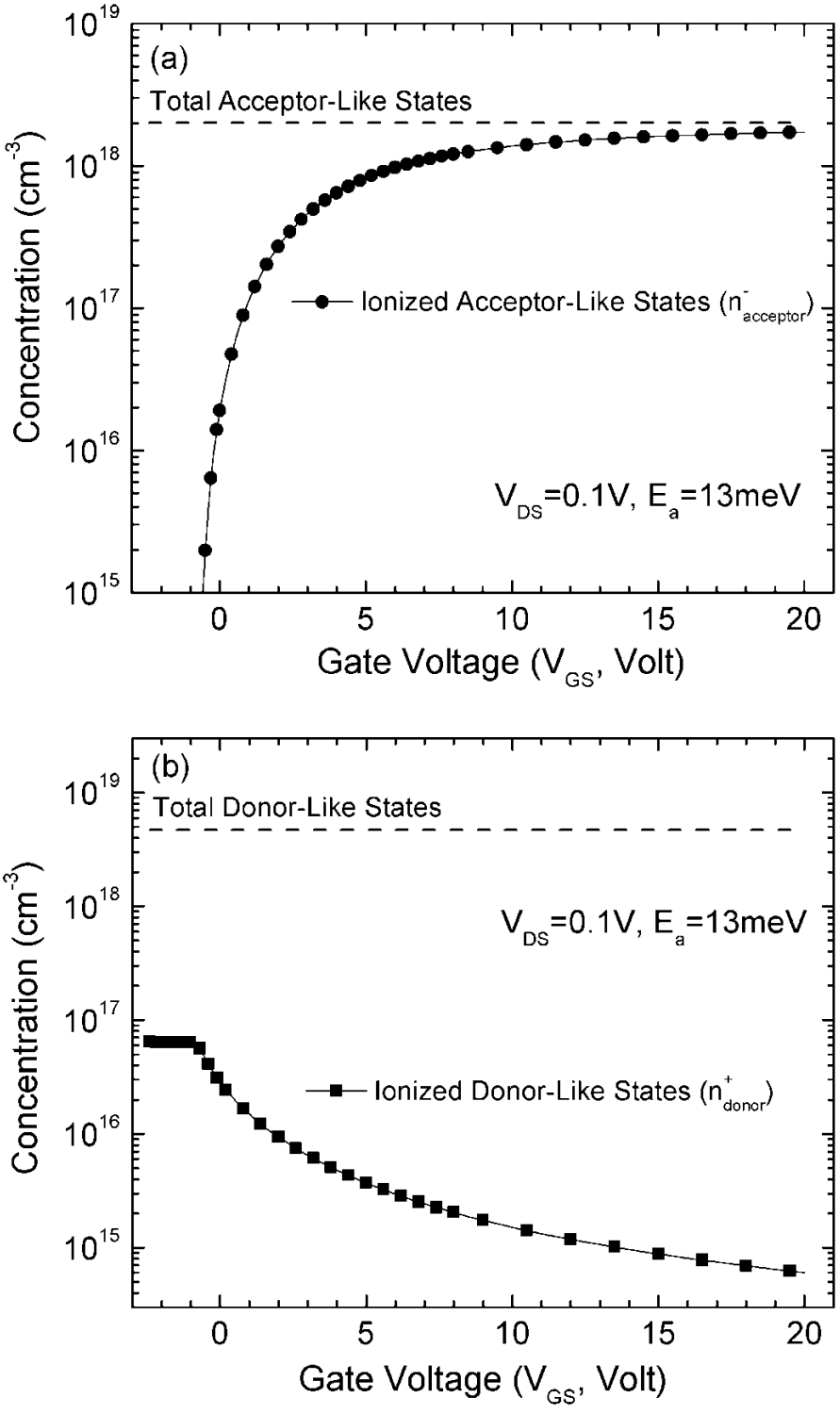


Figure 6.4 Simulated evolution of ionized (a) acceptor-like and (b) donor-like states as a function of V_{GS}. The simulation is done with E_a=13meV. Dash lines indicate the total concentration for both types of states.

constant in the simulation. When a higher V_{GS} is applied, the Fermi-level moves closer to the conduction band (Figure 6.2(a)). Because more electrons are now trapped by the band-tail states (g_{CBa}), ionized acceptor-like states ($n^-_{acceptor}$) increase (i.e. higher concentration of negative space charges). Meanwhile, the electrons can also fill the oxygen vacancy states (g_{Gd}) and cause a reduction in the ionized donor-like states (n^+_{donor}; i.e. lower concentration of positive space charges). In should be notice that during the simulation, both ionized states are lower than their total concentrations, which further confirmed the validity of our results. Figure 6.5 analyzes the concentration of free electrons (*n*), ionized donor-like states (n^+_{donor}), and ionized acceptor-like states ($n^-_{acceptor}$), and plots them as a function of Fermi-level position ($E_C - E_F$). To avoid confusion, it should be reminded that the E_a can affect the gate voltage dependence of E_C-E_F (Figure 6.2(a)), and one should not expect the same E_C-E_F value to be achieved under the same V_{GS} for different cases. It should also be noticed that n^+_{donor} is primarily contributed by the ionized oxygen vacancy (OV) states: when $E_C - E_F > 0.3$eV, all the OV states are ionized but start to be filled / passivated by electrons when E_C-$E_F < 0.3$eV. Since n^+_{donor} is one to two orders of magnitudes lower than *n* and $n^-_{acceptor}$ in most E_C-E_F range of interest, we only focus on *n* and $n^-_{acceptor}$ in the following discussion. Our default model has an E_a of 13meV. Such sharp distribution of conduction band-tail states (g_{CBa}) allows for *n* to be the dominated contribution to the total gate induced carriers. For instance, when V_{GS}=20V, $E_C - E_F \sim -0.06$eV and the ratio $n/n^-_{acceptor}$ can be as high as ~10. Also, as expected, E_a=13meV is lower than common a-Si:H value (~25meV), and agree fairly well with the Kamiya *et al.* and Nomura *et al.* (6~20meV) in their original

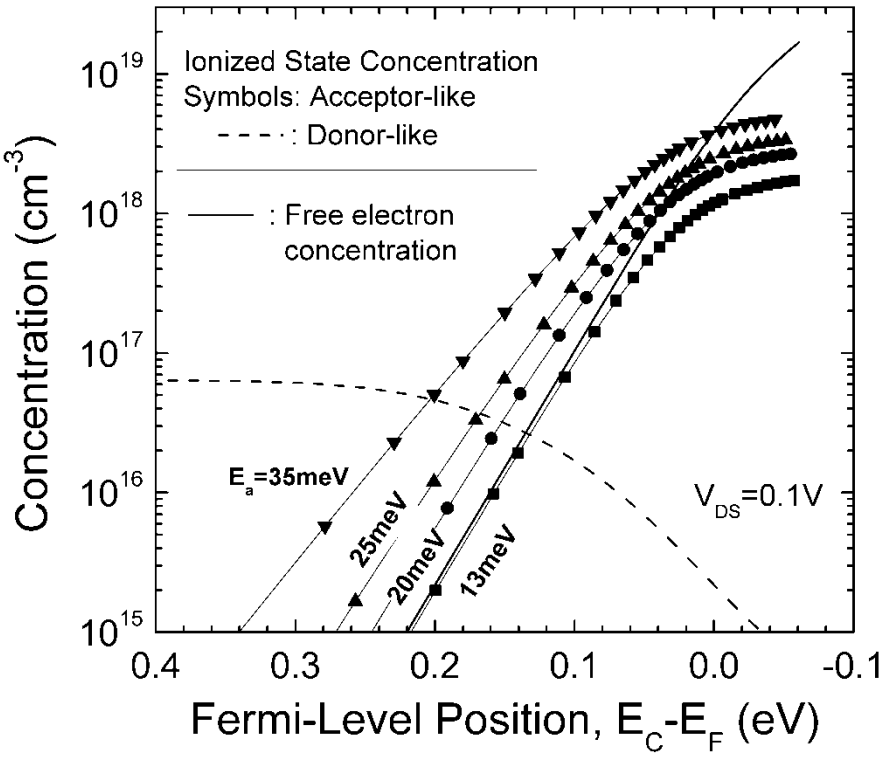


Figure 6.5 Simulated free electron concentration (n), ionized acceptor-like states ($n^-_{acceptor}$) and ionized donor-like states (n^+_{donor}) as a function of E_C-E_F. All the concentration data are integrated values over all energy levels within the band-gap. The symbols represent $n^-_{acceptor}$ for various E_a values, while the solid and dash lines are n and n^+_{donor}, respectively. Since the data for n and n^+_{donor} are the same for different E_a, only one data line is shown. The probe point is the same as indicated in the inset of Figure 6.2(a).

works [115, 116]. However, for the TFT with a higher E_a (20~35meV), most of the accumulated electrons are trapped by the conduction band-tail states. This trapping process decreases the ratio of $n/n^-_{acceptor}$ (< 1 for most of the $E_C - E_F$ values), and it will take a larger surface band-bending (i.e. $E_C - E_F < 0.05$eV), and V_{GS} for this ratio to be larger than unity. The phenomenon causing by this effect are twofold: First, since the concentration of n is lower, the maximum achievable μ_{inc} decreases. Secondly, an increasing degree of non-linearity in drain current (i.e. γ) is expected as experimentally observed.

6.2 The Impact of Source/Drain Contact Resistance (r_c)

To investigate the impact of source/drain contact resistance, additional contact resistivity (r_c) is added to the simulation code. Multiple TFT transfer properties are simulated with r_c values varied from 0~0.27Ω-cm^2 in a logarithmic increment (the Schottky contact model is still used). A perceivable decrease in simulated a-IGZO TFT linear region drain current (> 3%) only exist when $r_c > 2.7\times10^{-3}$ Ω-cm^2 (Figure 6.6(a)). This implies that r_c for the actual TFT could be in the ~10^{-4} Ω-cm^2 range. This is consistent with the result obtained from Section 3.1.2, suggesting that the contact resistance can be as low as ~4×10^{-4} Ω-cm^2.

Table 6.1 lists the key TFT properties. For $r_c \leq 2.7\times10^{-3}$ Ω-cm^2, both ideal MOSFET model and $\mu_{eff}(V_{GS})$ model give the consistent results with V_{th} ~1.1V, μ_{eff} ~12cm^2/Vs and γ ~1.24. However, with $r_c > 2.7\times10^{-3}$ Ω-cm^2, we found a significant decrease in V_{th} and μ_{eff}. (Note: the $\mu_{eff}(V_{GS})$ model is not valid for $r_c > 2.7\times10^{-3}$ Ω-cm^2.) In practice, the decrease of μ_{eff} might be misinterpreted as a result of increasing E_a; and a feature which can be used to differentiate between g_{CBa} and r_c induced μ_{eff} reduction could be very helpful. This task would be more easily accomplished by inspecting the μ_{inc} versus V_{GS} plots (Figure 6.6(b)). Due to the change in I_D-V_{GS} slope, the μ_{inc} for TFT with excess r_c decreases at high V_{GS}; such effect yields a unique "maximum" hump in the μ_{inc} versus V_{GS} plot. We can inspect this effect more closely by separating V_{GS} into three different regions (Figure 6.7). At low V_{GS} (region I), the channel resistance (R_{ch}) is much larger than S/D series resistance ($2R_o$). The I_D is solely determined by the R_{ch}; and both I_D and $\delta I_d/\delta V_{GS}$ are increasing with V_{GS}. Since the R_{ch} is inversely proportional to the V_{GS}, continuously increasing V_{GS} will eventually reach a point where $2R_o$ is comparable with R_{ch} (i.e. ~1% or higher). In this region (II), I_D is function of the resistance $2R_o+R_{ch}$. Further reduction of R_{ch} can still increase I_D,

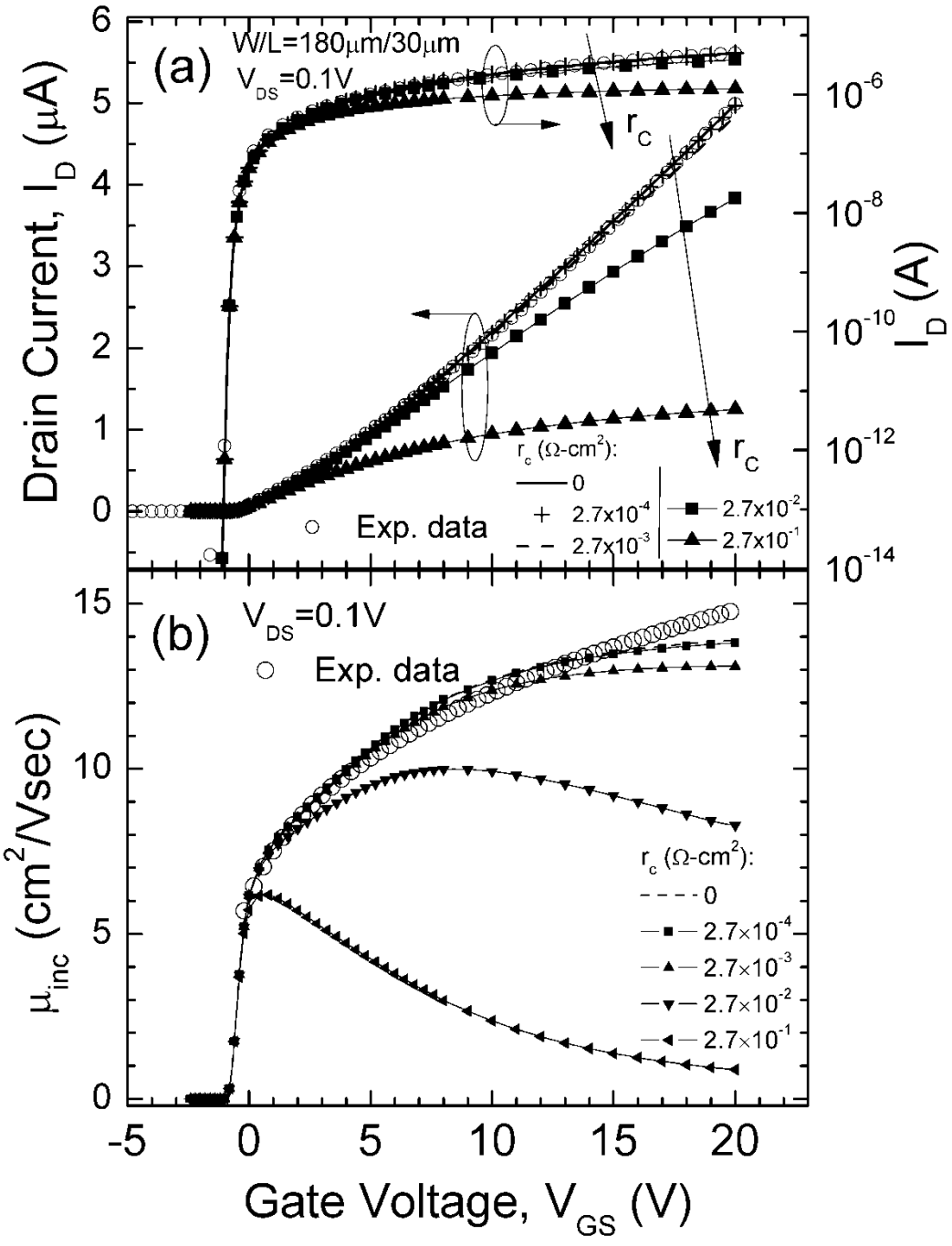


Figure 6.6 Simulated a-IGZO TFT (a) linear region transfer curves and (b) μ_{inc} extracted from TFT transfer characteristics for various r_c values. The experimental data (symbol: ○) are also shown.

r_c (Ω-cm^2)	MOSFET Model eq.(2-1)		μ_{eff} (V_{GS}) Model eq.(6-3)		
	V_{th} (V)	μ_{eff} (cm^2/Vs)	V_{max} (V)	K (cm^2/V$^\gamma$s)	γ
0	1.15	12.4	-0.6	5.62	1.24
2.7×10^{-4}	1.11	12.3	-0.6	5.57	1.24
2.7×10^{-3}	1.08	12.1	-0.6	5.69	1.23
2.7×10^{-2}	0.27	9.6	Not extracted**		
2.7×10^{-1}	-2.9*	3.6*			

* I_D-V_{GS} curve is highly non-linear.
** r_c is too large for proper parameter extraction.

Table 6.1 Simulated a-IGZO TFT electrical properties for various r_c values.

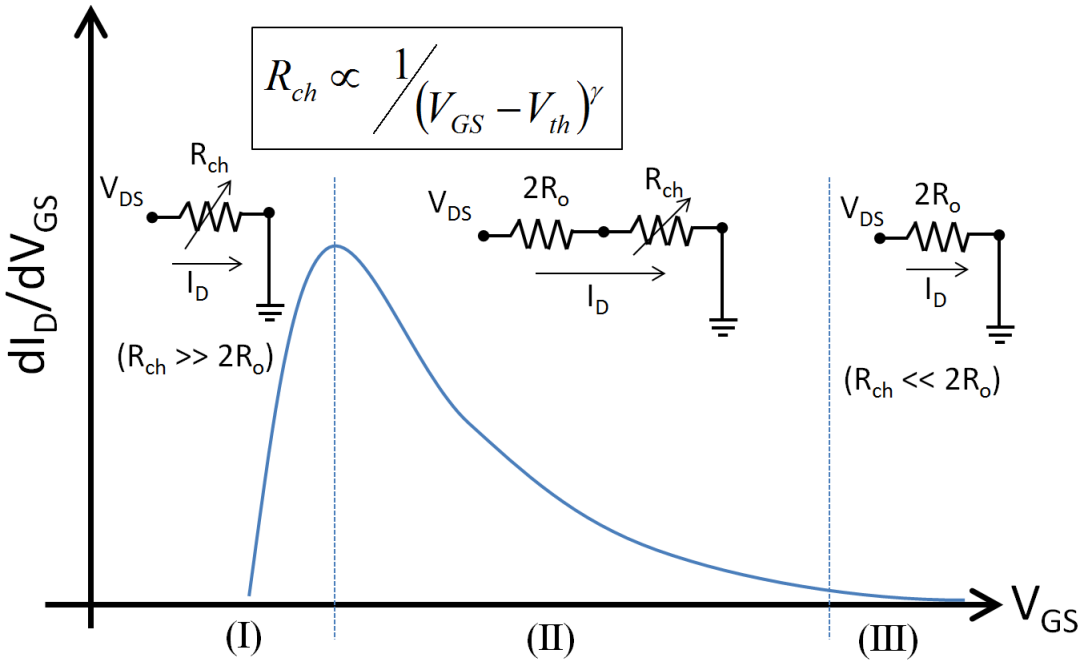


Figure 6.7 Illustration of the S/D contact resistance effect. The drain voltage (V_{DS}) is a constant. R_o and R_{ch} are the S/D series resistance and TFT channel resistance, respectively.

but it is less effective, because there is more voltage drop on the $2R_o$ (i.e. $\delta I_d/\delta V_{GS}$ decreases). In other words, the V_{GS} is losing the control over I_D. Finally, under a very high V_{GS} (region III), $R_{ch} << 2R_o$, the $I_D \sim V_{DS}/(2R_o)$ and $\delta I_d/\delta V_{GS}$ approaches zero. The existence of μ_{inc} maximum is an unique feature for TFT having larger r_c (but not for TFT having high E_a) and might be used for diagnostic purposes of the TFT S/D contact quality.

6.3 The Impact of Oxygen Vacancy (OV) States

Figure 6.8 shows the simulation result for different OV states peak values (g_d) ranging from 6.5×10^{16} to 5×10^{17} $cm^{-3}eV^{-1}$. (Note: All other simulation parameters (including E_a) are kept constant as their default values listed in Table 5.1.) We found that an increasing g_d can cause a negative shift in TFT transfer characteristic ($\Delta V_{th}\sim$ -0.8V), and this trend agreed very well with what have been reported for PLD a-IGZO TFT [67]. Accompanied with a negative shift, both sub-threshold swing (S) and TFT off-current increase (Figure 6.8(b)). In other words, the a-IGZO loses its semiconducting property and behaves more like a conductor with increasing g_d. At $g_d = 5\times10^{17}$ $cm^{-3}eV^{-1}$, the simulated TFT transfer curve shows very little switching behavior with a on/off ratio ~1.5 orders. The simulation also suggests such effect to be very sensitive to the g_d value, e.g., an approximately eight times increase in g_d can cause a reduction in on/off ratio by more than seven orders of magnitude. The evolutions of key TFT properties as a function of g_d are illustrated in Figure 6.9. It should be noticed that even though the TFT V_{th}, S and on/off ratio show large shifts, the μ_{eff} values extracted from the on-region data do not change much with g_d and are ~12.4cm^2/Vs.

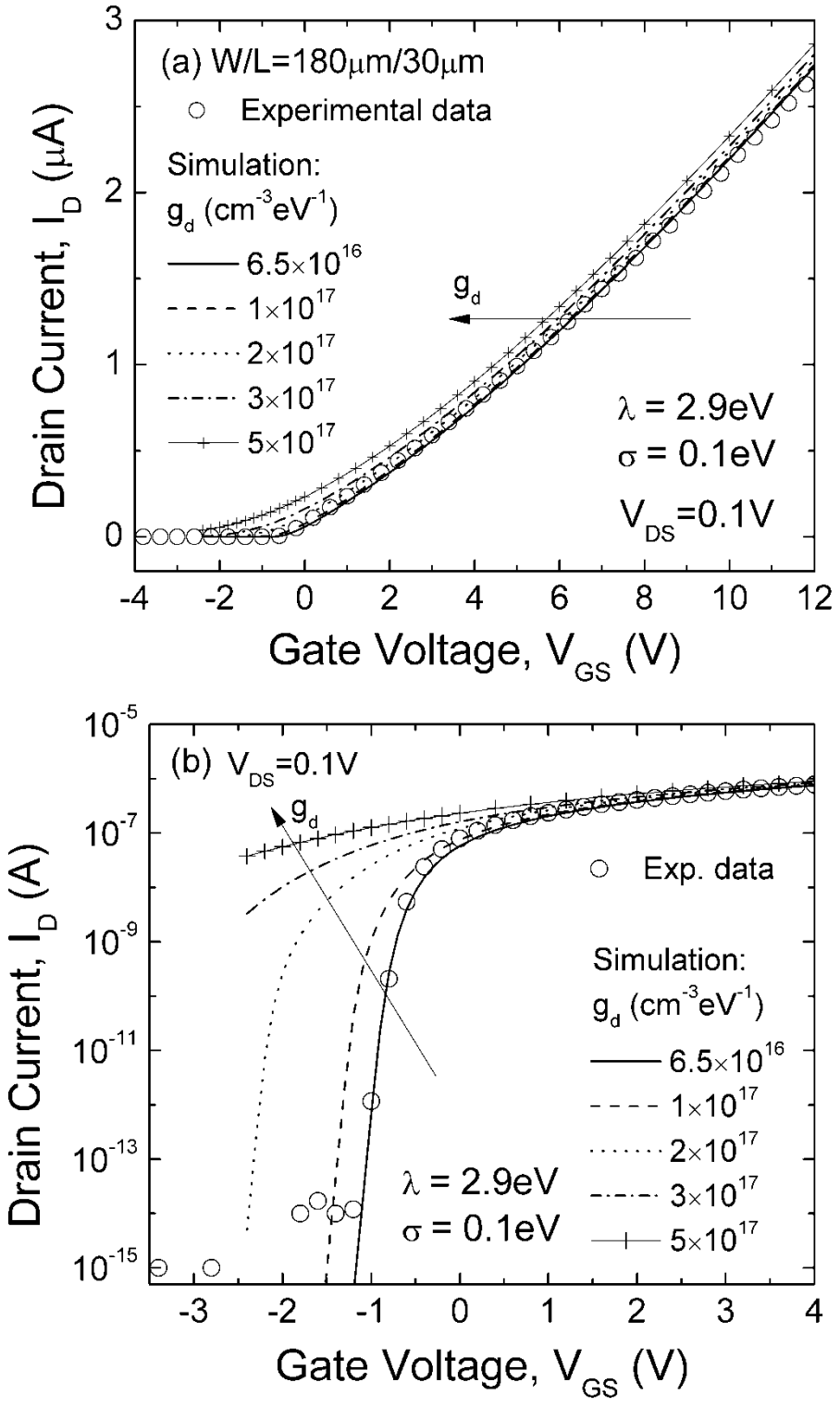


Figure 6.8 a-IGZO TFT simulated linear region I_D-V_{GS} curves in (a) linear scale and (b) semi-logarithm scale for various OV states peak value (g_d). Real experimental data (○) are also shown as reference.

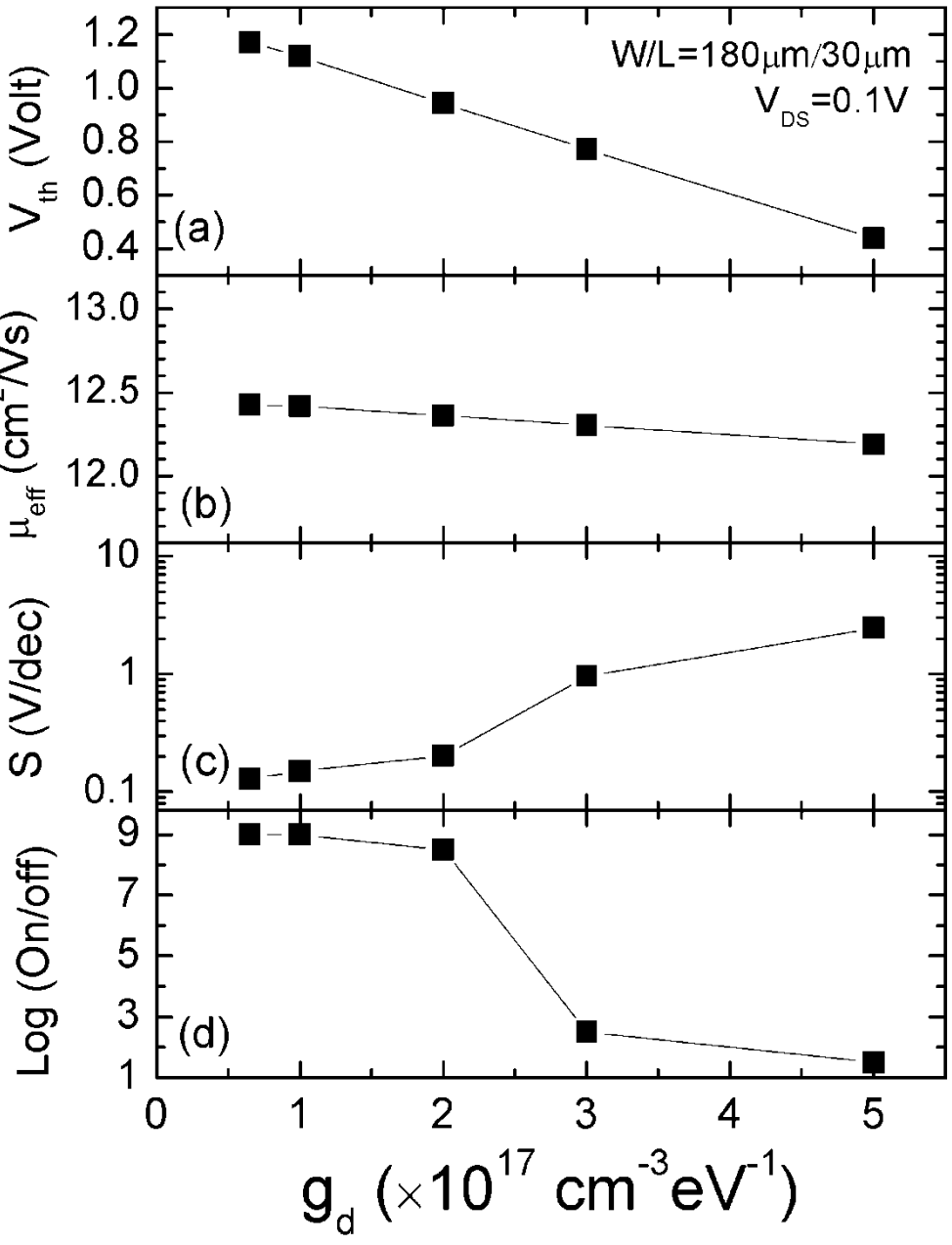


Figure 6.9 Simulated TFT (a) V_{th}, (b) μ_{eff}, (c) S and (d) on/off ratio as a function of g_d. These parameters are extracted from the data illustrated in Figure 6.8. V_{th} and μ_{eff} are extracted based on standard MOSFET model (2-1). S is calculated based on (2-2).

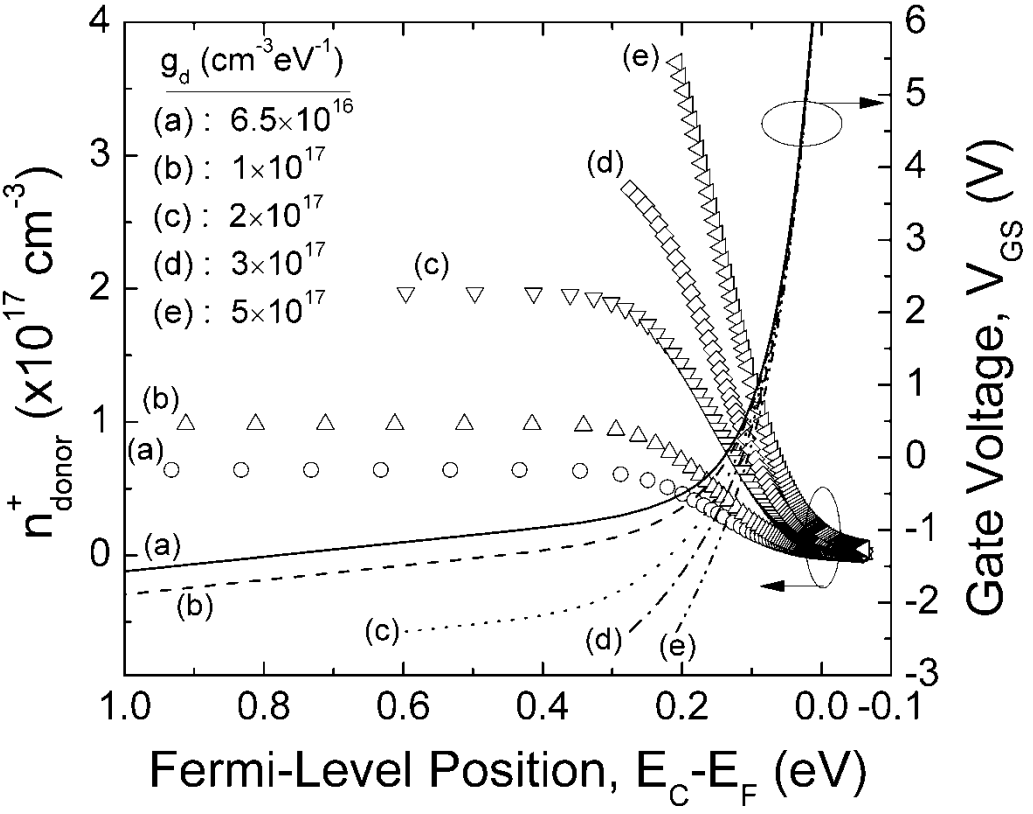


Figure 6.10 Simulated ionized donor-like states concentration (n^+_{donor}) and gate voltage (V_{GS}) as a function of Fermi-level position ($E_C - E_V$) for various OV states peak value (g_d) . The probe point is the same as indicated in the inset of Figure 6.2(a).

Figure 6.10 illustrates the n^+_{donor} and V_{GS} as a function of $E_C - E_F$. Per discussion in the previous section, n^+_{donor} is thought to be primarily associated with the ionized OV states (g_{Gd}). For the default condition ($g_d = 6.5\times10^{16}$ $cm^{-3}eV^{-1}$), all the g_{Gd} states are ionized in sub-threshold and off-regions (i.e. n^+_{donor} is a constant ~6×10^{16} cm^{-3} for $E_C - E_F > 0.3$eV). When g_d increases, the positive charged n^+_{donor} also increases, and to maintain the charge neutrality within the a-IGZO, E_F need to move closer to E_C to induce a larger density of electrons. For example, for V_{GS}= -1.5V, the $E_C - E_F$ moves from 0.93eV ($g_d = 6.5\times10^{16}$

$cm^{-3}eV^{-1}$) to 0.16eV when $g_d = 5\times10^{17}$ $cm^{-3}eV^{-1}$. In fact, the g_{Gd} states are only partially ionized for $g_d > 3\times10^{17}$ $cm^{-3}eV^{-1}$, this is because the Fermi-level is located within the energy range of g_{Gd} states for these conditions. The above mentioned mechanism is similar to doping despite of the lack of involvement of actual dopants. Furthermore, we believed such effect is consistent with the "intrinsic doping" concept proposed by other group [41, 89, 90].

Since the mean energy (λ) of OV states within bandgap can change if structural relaxation occurs [111], such effect was also investigated. Figure 6.11 illustrates the effect of g_{Gd} states located at seven different energy levels within bandgap (λ=2.9, 2.8, 2.7, 2.6, 2.5, 1.5 and 0.1eV). As shown in Figure 6.11(a), the TFT V_{th} (~1.15V) and μ_{eff} (~12.4cm^2/Vs) stay constant for various λ. Although the impacts of λ on on-region TFT I/V properties are minimum (note: it is thought to be due to a lower g_{Gd} concentration compared to g_{CBa} concentration.), the subthreshold properties do depend on λ (Figure 6.11(b)). By changing the λ from 2.9 to 1.5eV, there is about +0.6V of shift in transfer characteristics. In addition, an increase (or more accurately, "distortion") in subthreshold swing/region was observed during the transition phase. From the previous simulation, we know that the Fermi-level is approximately moving from 0.9eV below E_C toward E_C during the TFT operation. Before the E_F overlaps with the energy range of g_{Gd} states, they are all fully ionized, and when E_F moving across the g_{Gd} states ($E_C - E_F < 0.3$eV), these states starts to be filled by electrons, and therefore, n^+_{donor}decreases. In the default model, the decrease of n^+_{donor} primarily occurs in on-region (Figures 6.10 and 6.12). However, the situation changes when λ is located closer to the mid-gap. As shown in Figure 6.12, the decrease of n^+_{donor} occurs at a much higher value of E_C-E_F (0.4~0.7eV) for λ=2.8~2.5eV. These range overlaps with the

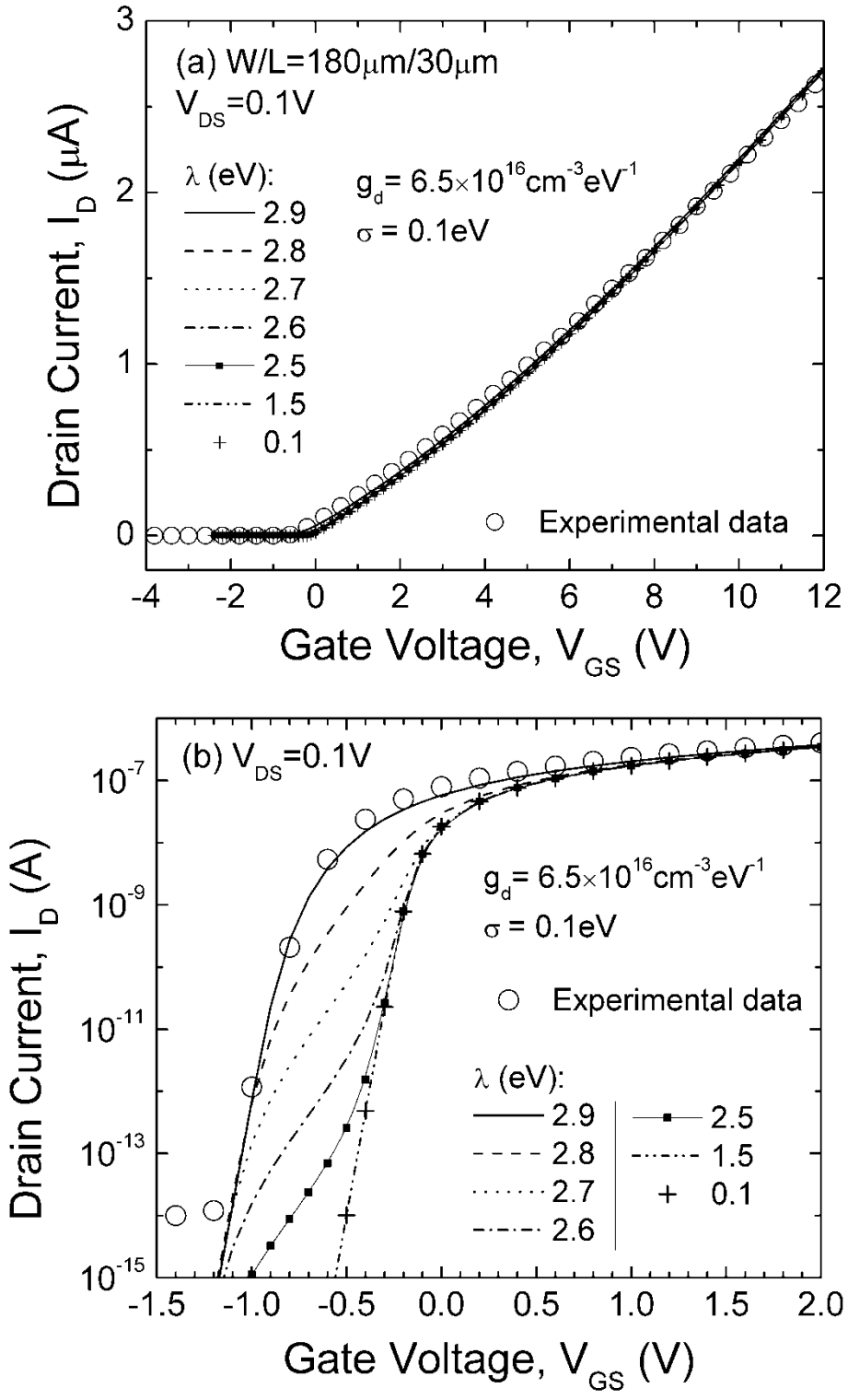


Figure 6.11 a-IGZO TFT simulated linear region I_D-V_{GS} curves in (a) linear scale and (b) semi-logarithm scale for various OV states mean energy (λ). Real experimental data (○) are also shown as reference.

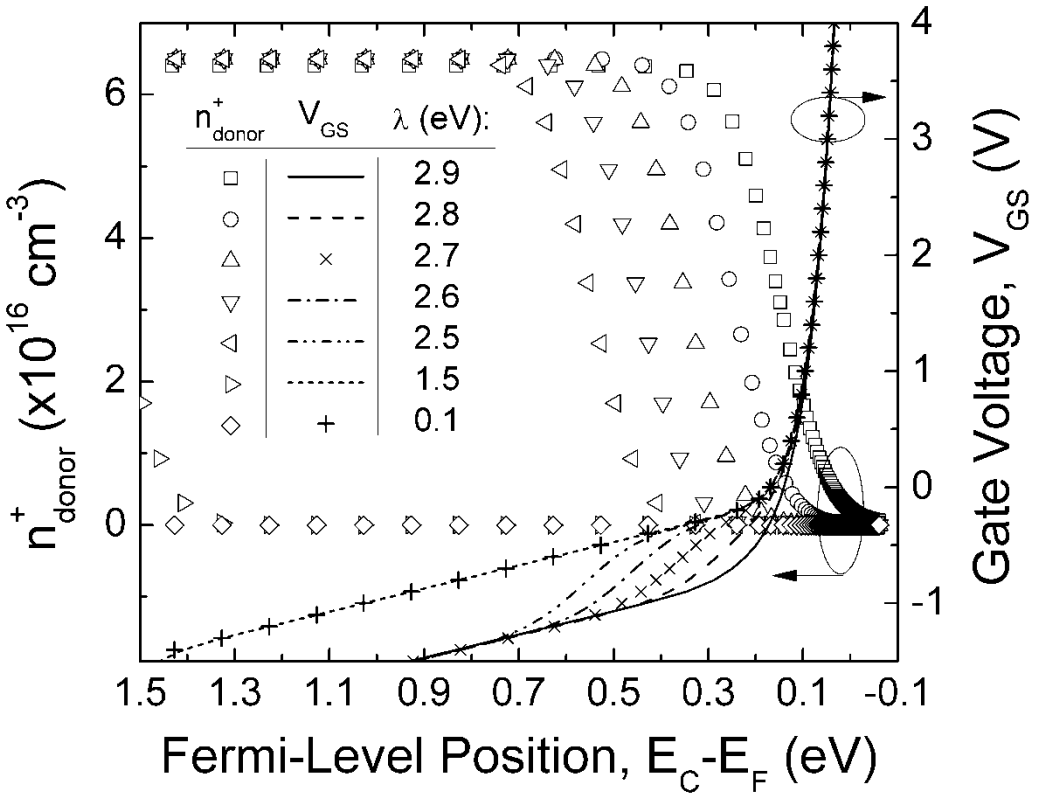


Figure 6.12 Simulated ionized donor-like states concentration (n^{+}_{donor}) and gate voltage (V_{GS}) as a function of Fermi-level position ($E_C - E_V$) for various OV states mean energy (λ). The probe point is the same as indicated in the inset of Figure 6.2(a).

subthreshold region and causes the observed degradation in simulated subthreshold swing properties. When λ is located at the mid-gap (1.5eV) or even closer to VBM (0.1eV), the g_{Gd} states are well below the initial Fermi-level position. As a result, instead of fully ionized, g_{Gd} states with λ<1.5eV are mostly or fully filled / passivated by electrons (i.e. $n^{+}_{donor} << 10^{16}$ cm^{-3}, Figure 6.12). This allows the Fermi-level to move closer toward mid-gap and induces the positive shift (+V_{GS} direction) observed in the transfer characteristics. In addition, since E_F is not within the energy range of g_{Gd} states, the subthreshold swing is not affected. It should be noticed that the g_{Gd} represents the electronically effective

density, and the actual OV density (D_{ov}) should be written as $D_{ov}=g_{Gd}/Z_{ov}$, where Z_{ov} is the charge state of OV. For instance, as suggested by the first-principle calculation, Z_{ov} are +2 and +1 when the OV states are near CBM and mid-gap, respectively [111]. Finally, our observations also agree well with the conclusions draw from the first-principle calculation on a-IGZO [112], which suggests that the energy locations of OV states should be properly controlled (e.g. thermal annealing) to achieve a high performance a-IGZO TFT.

Chapter 7

a-IGZO TFT Electrical Instability

7.1 Introduction

To ensure a robust product based on a-IGZO TFTs, it is essential to evaluate their electrical stability. The long-term constant current-temperature stress (CTS) study has shown that the a-IGZO TFT has a stable electrical properties with a threshold voltage shift (ΔV_{th}) much smaller (0.2V) than the ΔV_{th} for a-Si:H TFT (>1.8V) under the same active matrix organic light emitting display (AM-OLED) testing condition (3μA, 60^0C, 20 hours) [117]. The proper passivation layer for the back channel was also found to play an important role in improving the TFT CTS reliability [26]. Recent studies further extended investigation of the a-IGZO stability into the bias-temperature stress (BTS) measurements. A positive shift in TFT V_{th} was observed under a positive (gate bias) BTS while the V_{th} shifted to negative values for negative BTS [118]. Furthermore, a simple power law relation is able to fit the stress time trend of measured ΔV_{th} [119]. A great reduction (~75%) in BTS induced degradation was found when additional post annealing step during fabrication is performed. Although the nature of this reduction is not clear, the defect states located in bulk active layer or near the interface are suspected to be its origin [118].

Despite all the progress in a-IGZO TFTs so far, our knowledge on its electrical stability

is very limited and should be addressed more in-depth. This chapter discusses the BTS induced electrical instability of defined gate, RF sputter a-IGZO TFTs. Proper simulation model is also proposed to describe experimental data.

7.2 Experimental

7.2.1 Bias-temperature stress (BTS) measurement

The cross-sectional view of the defined gate, RF sputter a-IGZO TFT used in this study is shown in Figure 7.1(a). The detail processing steps have been discussed in Section 2.1.3. The TFT has an inverted-staggered bottom-gate structure. The Ti/Au/Ti stacking layers are used for gate and source/drain (S/D) electrodes. The SiO_2 gate insulator and a-IGZO active layer is about 200nm and 30nm thick, respectively.

A series of BTS experiments were conducted for steady-state conditions by using a semiconductor parametric analyzer (Agilent 4156C) and a light-tight probe station. During the BTS, a predetermined stress voltage (V_{G_stress}) is applied to the gate electrode and to ensure a uniform electrical field distribution along the SiO_2/a-IGZO interface, the drain terminal of the TFT is short to its source terminal (V_{DS}=0V, Figure 7.1(c)). Measurements were also performed under different stress temperatures (T_{STR}) ranging from 50^0C~80^0C. For even lower temperature, the ΔV_{th} is too small (few 10mV) to make a reliable analysis within the BTS time range (10Ks) chosen in this study. It should be noticed that all the BTS induced electrical instability can be fully recover after a thermal annealing step (2 hour, 200^0C, as illustrated in Figure 7.5). Each series of BTS experiment is performed on the same TFT and to ensure consistent initial TFT properties, the thermal annealing is applied before each new BTS experiment is conducted.

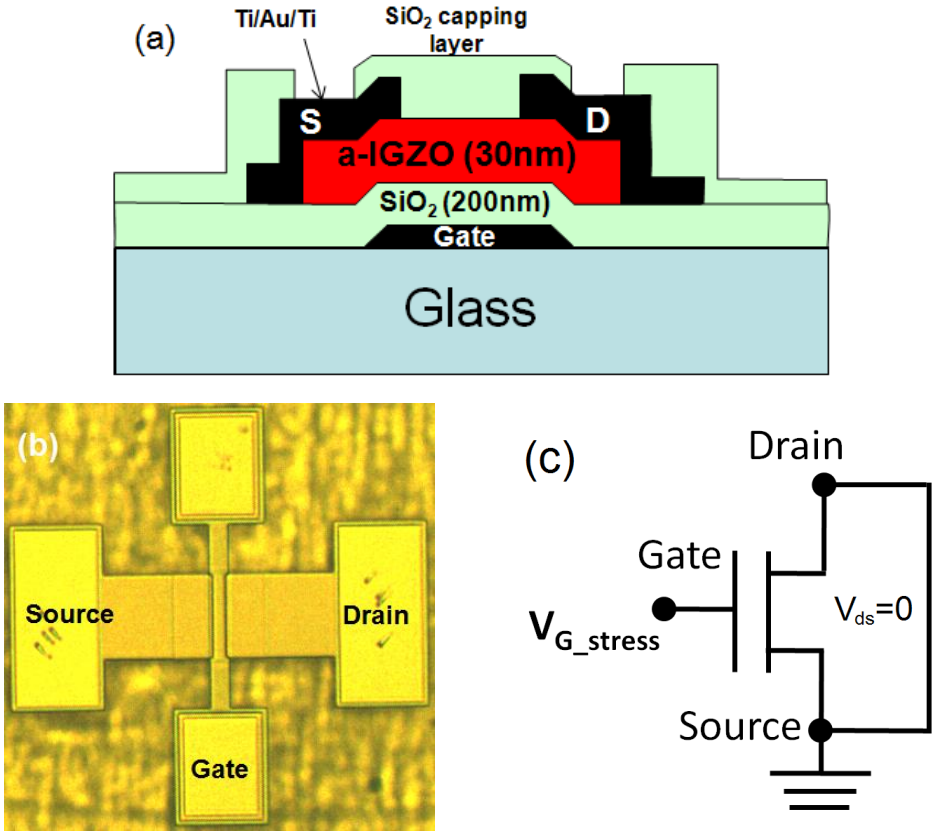


Figure 7.1 (a) Cross-sectional and (b) top view of the RF sputter a-IGZO TFT device used in this study. (c) The schematic of the circuit setup used for steady state BTS experiments.

7.2.2 Methodology for parameter extraction

We monitored the evolution of device degradation by interrupting the BTS at predetermined time steps and measuring the TFT transfer properties. During BTS measurement, the V_{th} of TFT is continuously changing. Since the V_{GS} range for the transfer property measurement is fixed, the maximum achievable drain current ($I_{D\text{-}MAX}$) is varying during different BTS time steps. This causes the conventional 90%~10% method (Section 2.2.3), which relies on $I_{D\text{-}MAX}$ to determine the analyzing data range, to be unsuitable due to the unequal data range among data collected at different times. In order to ensure a consistent comparison of extracted parameters between different BTS time steps, a fixed data range

should be defined. In this study, all the TFT V_{th} and μ_{eff} were extracted from the linear fit of the saturation region transfer curves between $(I_D)^{1/2}$=0.01~0.001 $A^{1/2}$ to the standard saturation region MOSFET equation (2-3), as illustrated in Figure 7.2. A V_{DS} of 20V rather than V_{DS}=V_{GS} was chosen because the first condition allows the TFT subthreshold region properties to be precisely measured. The ΔV_{th} is calculated as the difference between threshold voltages extracted at each stressing time step and the initial values of each BTS experiment ($V_{th\_initial}$). Subthreshold swing (S) is extracted from transfer characteristic in subthreshold region, using (2-2). In addition, to better characterize the change in subthreshold region, the parameter ΔV_T is defined as the transfer properties shift at I_D=10^{-9}A.

7.3 DC-BTS Electrical Instability of a-IGZO TFT [120]

Figure 7.2(a) shows the typical results we observed during the positive BTS experiments. The linear plots show a positive shift in TFT I-V properties and are consistent with the trend of ΔV_{th} extracted. The negative BTS experiment is also performed at 80^0C with V_{G_stress} = -20V (Figure 7.2(b)). A uniform negative shift is observed in both on and subthreshold regions. Key parameters such as ΔV_{th}, ΔV_T, μ_{eff} and S are extracted and plotted as a function of stress time (t_{stress}) in Figure 7.3. The result indicates that during the circuit operation, both positive and negative clock cycles can cause change in a-IGZO TFT electrical properties. Circuit designer should optimized the circuit driving scheme to ensure the product lifetime.

The BTS induced ΔV_{th} is the primary a-IGZO TFT instability. It should be noticed that a slight change in μ_{eff} and S is also observed [Figure 7.3(c) & (d)]. Many previous studies in amorphous semiconductor TFTs (e.g. a-Si:H TFT) have concluded that two main

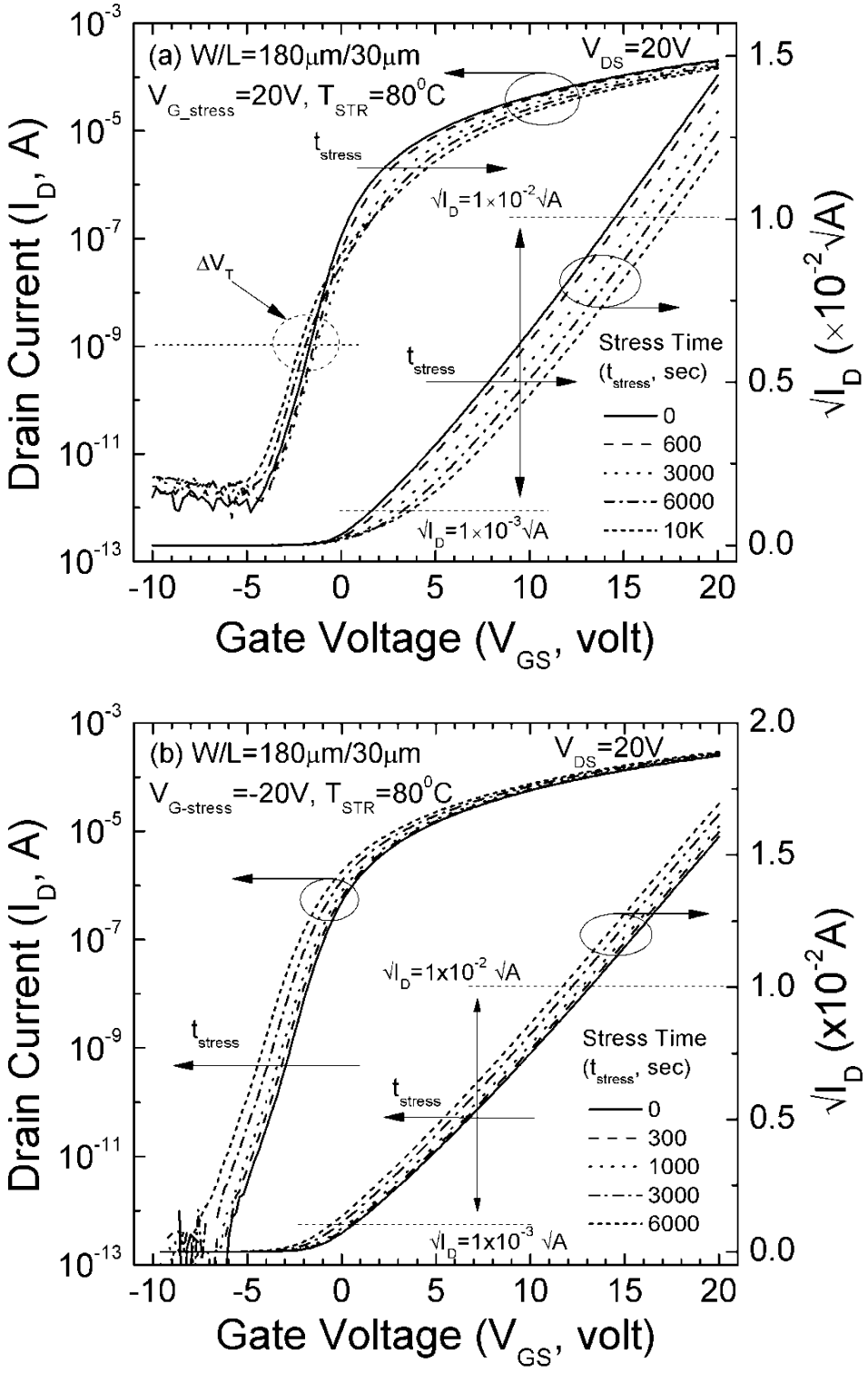


Figure 7.2 The evolution of RF sputter a-IGZO TFT transfer characteristics for (a) positive BTS (V_{G_stress}= 20V) and (b) negative BTS (V_{G_stress}= -20V). For both experiments, the stress temperature, T_{STR}, is 80^0C.

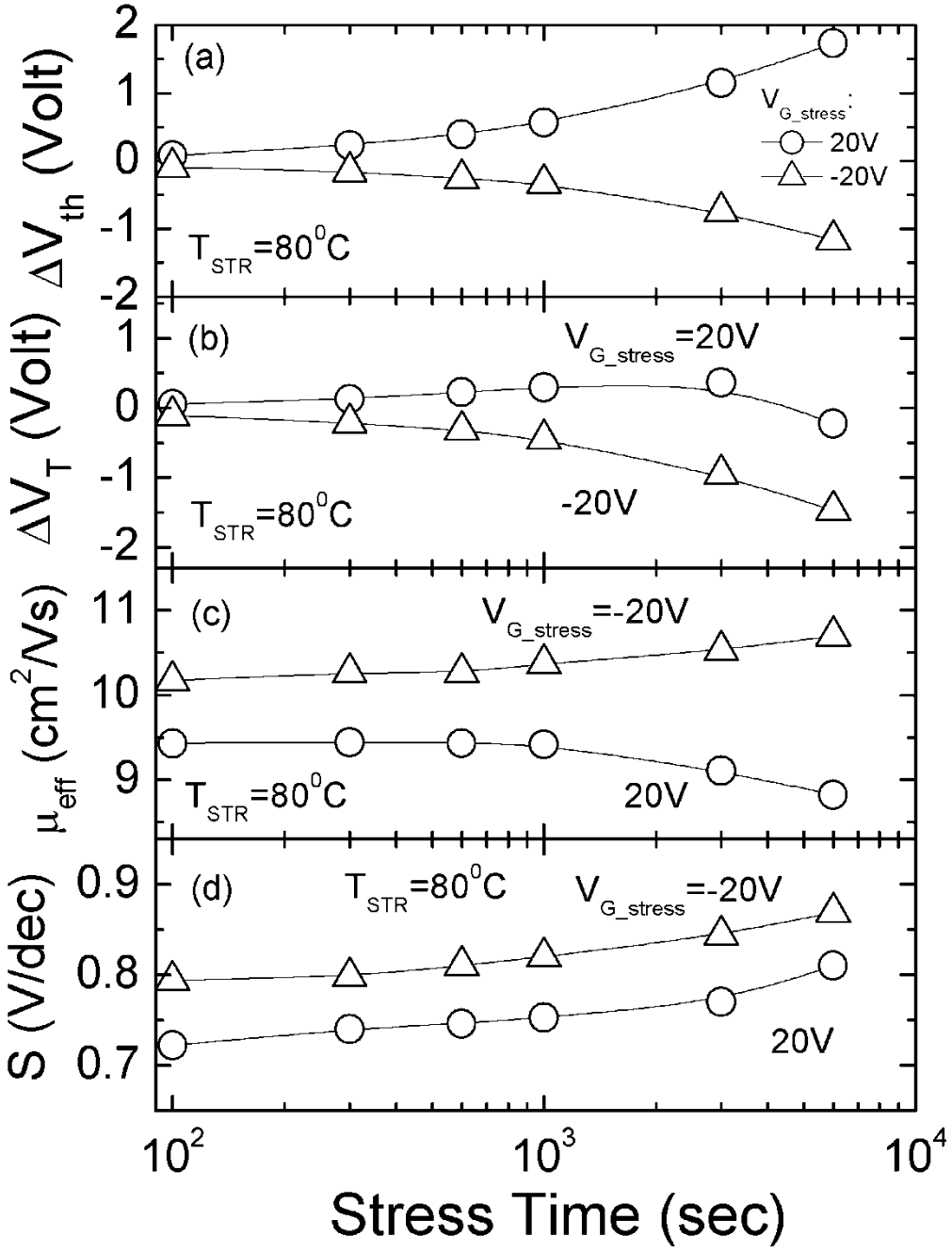


Figure 7.3 (a) ΔV_{th}, (b) ΔV_T, (c) μ_{eff} and (d) S as a function of stress time (t_{stress}) for both positive (V_{G_stress}=20V) and negative (-20V) BTS. Symbols represent the experimental data and lines are for aid of eye.

mechanisms can explain the electrical instability [121-124]. One is the carrier trapping in the gate insulator [121, 122] and the other is point defect creation which will increase the density of deep-gap (bulk) states at or near the semiconductor/gate insulator interface [123, 124]. In a-Si:H TFT, deep-gap states are originated from Si-Si weak and Si-dangling bonds. Biasing the TFT can cause the amorphous Si network to be unstable and the network can rearrange to break the Si-Si bonds [125]. However, in a-IGZO, instead of the sp^3 orbitals, carriers are conducting through metal ion's *ns*-orbitals with sufficient inter ions overlap [39]. Such mechanism permits a-IGZO to have a high immunity to dangling bond creation and maintains a low density of deep-gap states [107]. In Chapter 2 and 3, we have seen that the a-IGZO bulk states and band-tail states properties can be probed by the TFT subthreshold swing and I_D-V_{GS} non-linearity. Figure 7.4 illustrates the time evolution of bulk state density (N_{BS}) and characteristic temperature of the conduction band tail states (T_G) extracted by using (2-4) and (3-29), respectively. The increases of N_{BS} for both BTS polarities are less than 30% by the end of BTS experiments. The variation of kT_G is very small and is fairly closed to ~34meV. This indicates the conduction band-tail states weren't affected by the BTS. As a comparison, by the end of the experiments, ΔV_{th} is about 1.5 ~ 2V for both BTS polarity. This corresponds to a relative change of >100%. Therefore, our experimental results support the previously proposed theory and ΔV_{th} can be attributed mainly to charge trapping with some minor contribution from defects creation.

The analysis of ΔV_T (Figure 7.3(b)) highlights the difference between positive and negative BTS under longer stress time. Despite the positive shift in on-region, the subthreshold properties (ΔV_T) for positive BTS are actually starting to shift negatively for t_{stress} > 3000 secs, which can also be seen in the semi-log plot in Figure 7.2(a). This was accompanied by an increase (about two times) in the TFT off-current (I_{D_off}). On the other

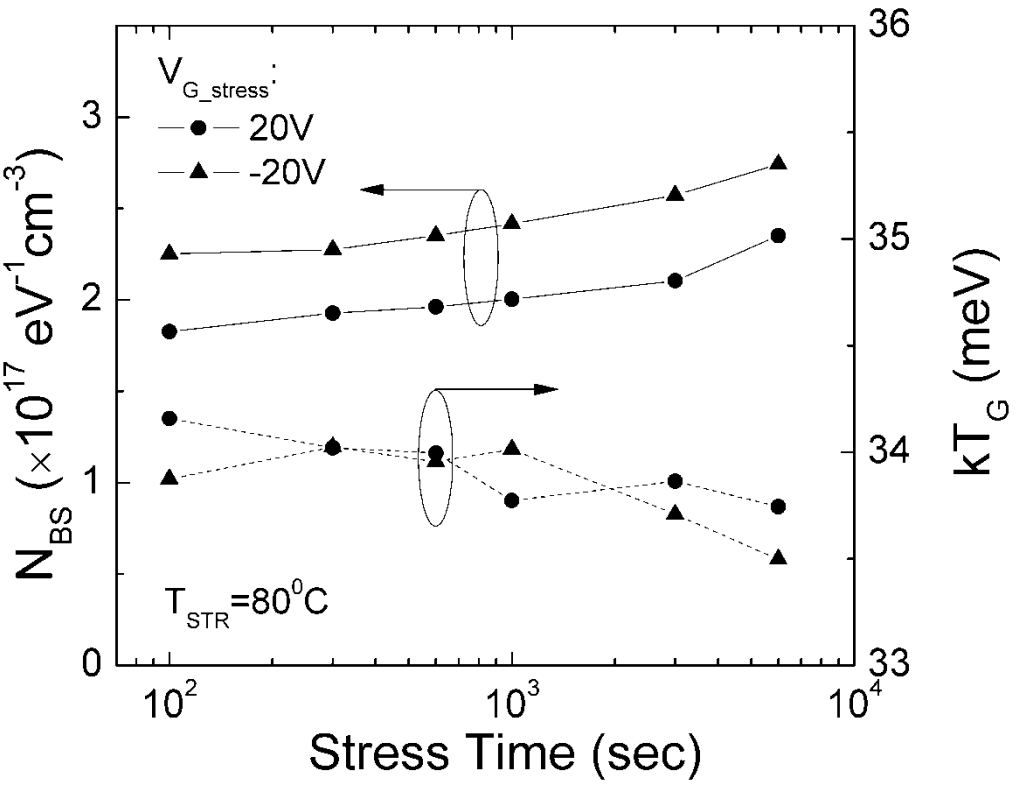


Figure 7.4 Density of bulk-states (N_{BS}) and characteristic temperature of conduction band tail states (T_G) as a function of stress time (t_{stress}) for both positive (V_{G_stress}=20V) and negative (-20V) BTS.

hand, negative BTS shows a consistent negative shift in both regions. The increase of I_{D_off} can be much larger under a severe positive BTS condition with V_{G_stress}=27V, 40Ksecs and T_{STR} of 80^0C as depicted in Figure 7.5. The increased I_{D_off} can be associated with the decrease in a-IGZO film resistivity. It is a reversible process even under the severe BTS and the TFT can recover to its initial state after the thermal annealing step discussed in Section 7.2.1. Since the increase in either bulk-states or conduction band-tail states should cause the positive shift in TFT I/V properties [57], such negative ΔV_T shift observed for prolong positive BTS should be associated with other secondary effect, e.g. certain defect creation mechanism that only exists in metal oxide semiconductors. Many previous works of

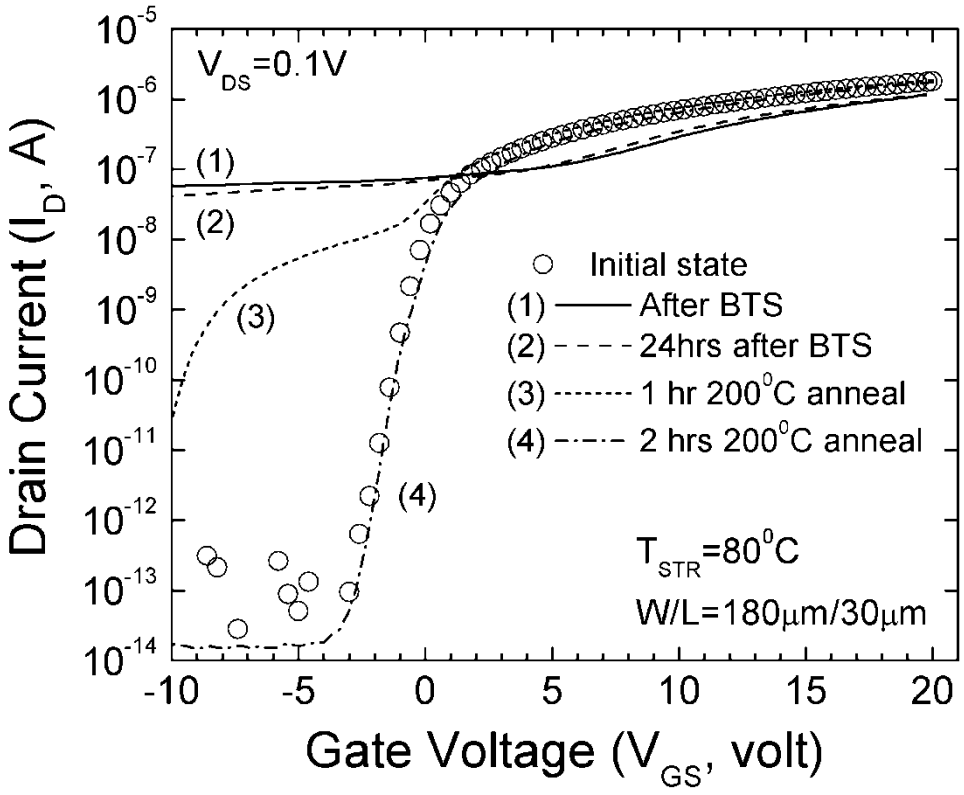


Figure 7.5 Recovery of the a-IGZO TFT electrical instability after thermal annealing. (1) TFT transfer properties after severe BTS condition (V_{G_stress}=27V, T_{STR}=80^{0}C, 40 Ksecs); (2) 24hr of storage under room temperature after BTS; (3) after 1 hours and (4) 2 hours of thermal annealing (200^{0}C) in air.

a-IGZO TFT have shown that the oxygen vacancy in a-IGZO can cause a decrease in film resistivity [41, 90] and a negative shift in TFT sub-threshold properties [110]. These reported phenomena are very similar to the a-IGZO I/V properties we observed after prolong positive BTS. Despite that the exact physical origin is still unclear; the authors suggest the meta-stable oxygen vacancies could be induced near the semiconductor/gate insulator interface by prolong positive BTS in this case. The induced oxygen vacancies then cause an increase in a-IGZO TFT I_{D_off} and the negative shifts in TFT subthreshold I/V properties (ΔV_T).

7.4 Stretched-Exponential Model

To better understand the physics behind the BTS induced ΔV_{th} in RF sputter a-IGZO TFT. We performed a detail numerical analysis based on the stretched-exponential model. The model, which was originally developed for active matrix flat panel display (AM-FPD) based on charge injection/ trapping concept [121, 126], describes the TFT ΔV_{th} by the following equation:

$$\left|\Delta V_{th}\right| = \left|\Delta V_0\right|^{\alpha}\left\{1-\exp\left[-\left(\frac{t_{stress}}{\tau}\right)^{\beta}\right]\right\} \tag{7-1}$$

where

$$\Delta V_0 = V_{G\_stress} - V_{th\_initi} \tag{7-2}$$

and

$$\tau = \tau_0 \exp\left(\frac{E_\tau}{kT_{STR}}\right). \tag{7-3}$$

In the above equations, ΔV_0 is the effective voltage drop across the gate insulator (or also called effective stress voltage); $V_{th\_initial}$ is the initial threshold voltage; α is the exponent for ΔV_0 dependence and β is the stretched exponential exponent. The τ in (7-1) represents the characteristic trapping time of carriers and E_τ is the average effective energy barrier that carriers in conducting channel needed to overcome before they can enter the insulator or near interface region, with τ_0 being the thermal pre-factor for emission over barrier. For a very short stress time ($t_{stress} << \tau$) Equation (7-1) can be further shortening as

$$\left|\Delta V_{th}\right| \cong \left|\Delta V_0\right|^{\alpha} \tau^{-\beta} t_{stre}^{\beta}. \tag{7-4}$$

Equation (7-4) relates ΔV_{th} to straightforward power law dependence (β) of t_{stress} and has

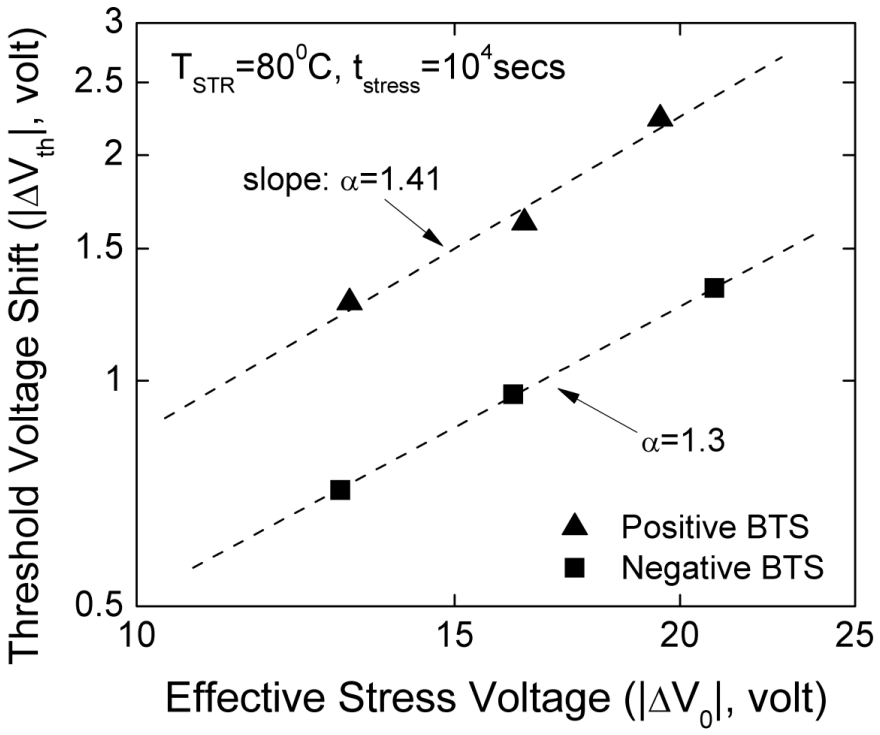


Figure 7.6 ΔV_{th} as a function of effective stress voltage (ΔV_0) for positive (symbol: ▲) and negative (■) BTS. Dash lines are the linear fits to the experimental data.

been applied to model BTS data [119]. On the other hand, for infinite stress time ($t_{stress} \rightarrow \infty$), (7-1) will give a saturated behavior with $\Delta V_{th} \rightarrow (\Delta V_0)^{\alpha}$.

To demonstrate the validity of using stretch-exponential model to simulate the BTS results. We further repeated the BTS tests under different V_{G_stress} (14 ~20V for positive BTS, -12 ~ -20V for negative BTS) and temperatures ($T_{STR}=50^0C \sim 80^0C$ for both BTS polarities). The α is first extracted from the $\log(|\Delta V_{th}|)$ vs. $\log(|\Delta V_0|)$ plots as depicted in Figure 7.6. The extracted α for positive BTS (=1.41) is larger than the one extracted for negative BTS (=1.3); this result suggests that the ΔV_{th} for positive BTS is more sensitive to V_{G_stress}. Figure 7.7 and 7.8 show the evolution of ΔV_{th} as a function of stress time (t_{stress}) under different positive and negative BTS conditions, respectively. The dash lines in these two figures are the numerical fits to (7-1). The characteristic trapping time, τ, is treated

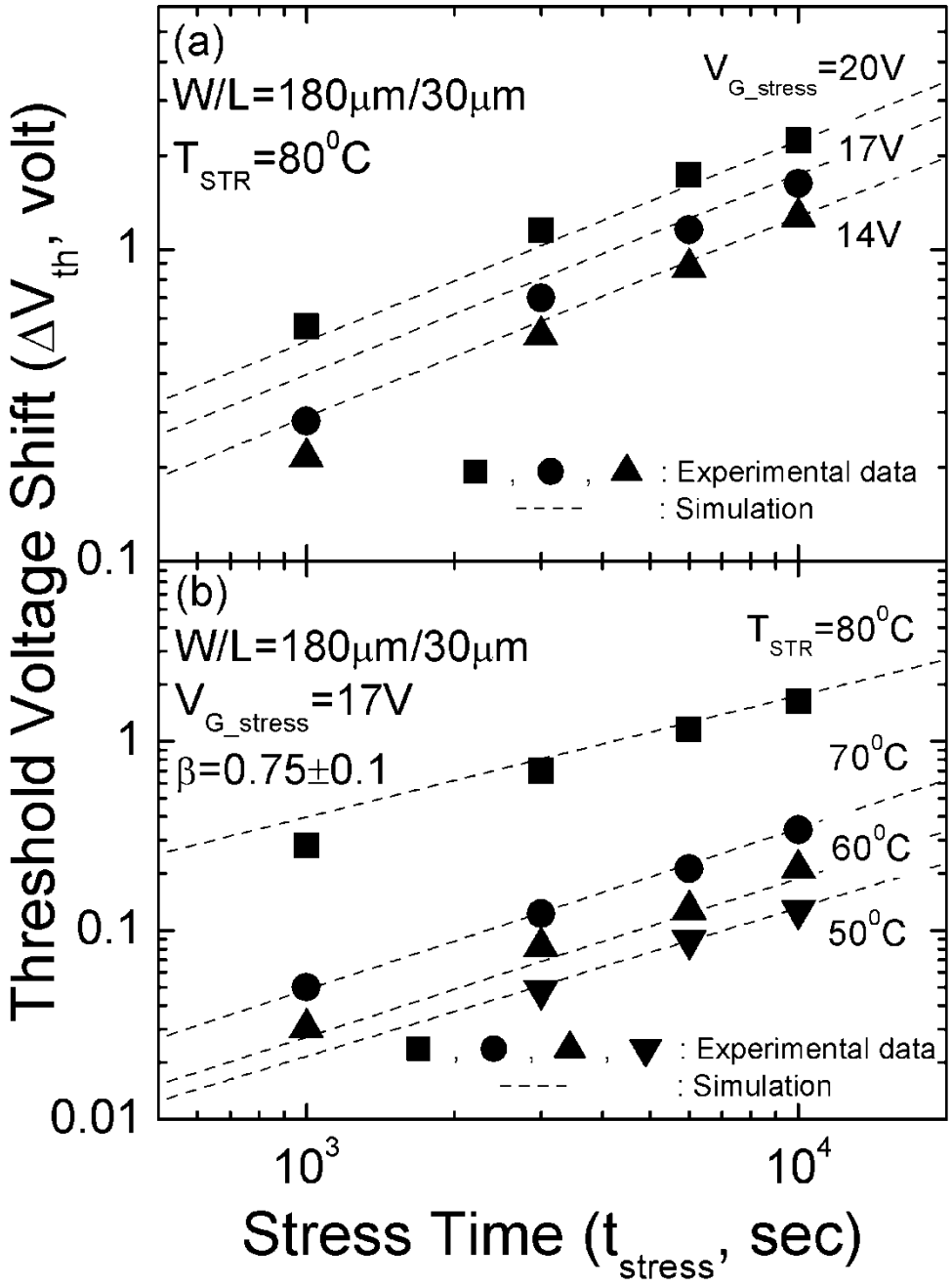


Figure 7.7 ΔV_{th} vs. stress time (t_{stress}) for various (a) positive stress voltages (V_{G_stress}=20V, 17V and 14V, T_{STR}=80^{0}C) and (b) temperature (T_{STR}=50^{0}C~80^{0}C, V_{G_stress}=17V). Symbols represent the experimental data while dashed lines are the simulation fits to stretched-exponential model (7-1).

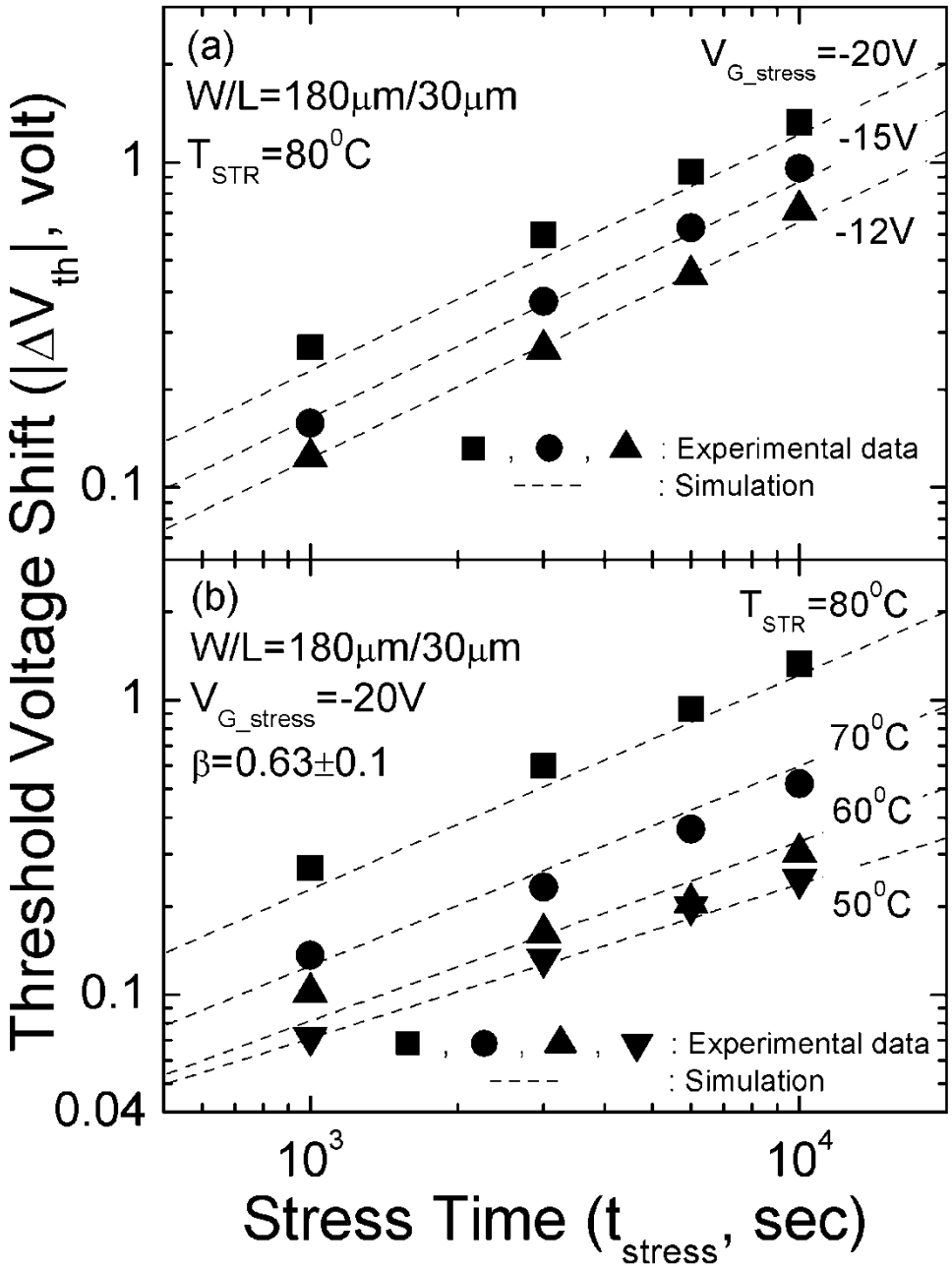


Figure 7.8 ΔV_{th} vs. stress time (t_{stress}) for various (a) negative stress voltages (V_{G_stress}= -20V, -15V and -12V, T_{STR}=80^{0}C) and (b) temperature (T_{STR}=50^{0}C~80^{0}C, V_{G_stress}= -20V). Symbols represent the experimental data while dashed lines are the simulation fits to stretched-exponential model (7-1).

as fitting parameter and plotted as a function of $1/kT_{STR}$ in Figure 7.9. Simulation errors were observed for data points with short stress time ($<10^3$ secs); this is because the ΔV_{th} for these data points are very close to the measurement resolution (~0.2V) set in this study. Despite the errors, the stretched-exponential model is able to universally reproduce the trend of experimental data, regardless of magnitude of the stress voltage, BTS polarity or stress temperature. This implies that the carrier injection from conducting channel and the subsequent charge trapping plays an important role in the a-IGZO TFT BTS instability. Such conclusion is also consistent with the discussion in previous section.

To determine the exact ΔV_{th} dependence on stress temperature, we extract the E_τ and τ_0 by applying (7-3) to the τ vs. $1/kT_{STR}$ plots (Figure 7.9). Table 7.1 summarizes all the parameters used in the stretched-exponential model. The extracted E_τ for positive BTS (0.78eV) is smaller than the value of negative BTS (1.637eV). This suggests that the electrons are experienced a lower energy barrier than holes do during the charge injection process near the a-IGZO/SiO_2 interface. Electron injection is very efficient and can quickly fill out the available states which in-turn increases the chance for re-emitting these filled states. As a result, the characteristic trapping time (τ) for positive BTS ΔV_{th} to reach the saturation point is lower than the values of negative BTS. It should be noticed that there is an exponential dependence of τ_0 on the y-axis intercept of the linear fit of data in Figure 7.9. Therefore, the extracted τ_0 can be very sensitive to the y-axis intercept and error can occur in our extraction due to the limited number of data points. More temperature dependence BTS data will be necessary to accurately determine the τ_0.

Although the stretched-exponential model predicted $\Delta V_{th} \rightarrow (\Delta V_0)^\alpha$ for long stress time, we didn't observed a strong saturated behavior with ΔV_{th}, since the BTS only performed for t_{stress} upto 10Ks in our experiments (e.g. limited stress time). This can be justified by

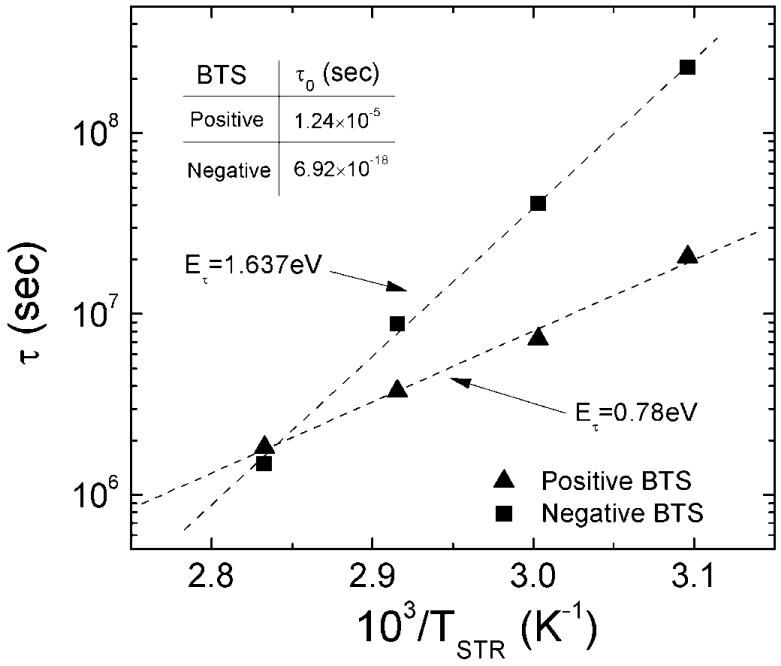


Figure 7.9 The characteristic trapping time τ for positive (symbol: ▲) and negative (■) BTS as a function of $1/T_{STR}$. (T_{STR} range: 50^0C~ 80^0C). Dash line: numerical fit to (7-3).

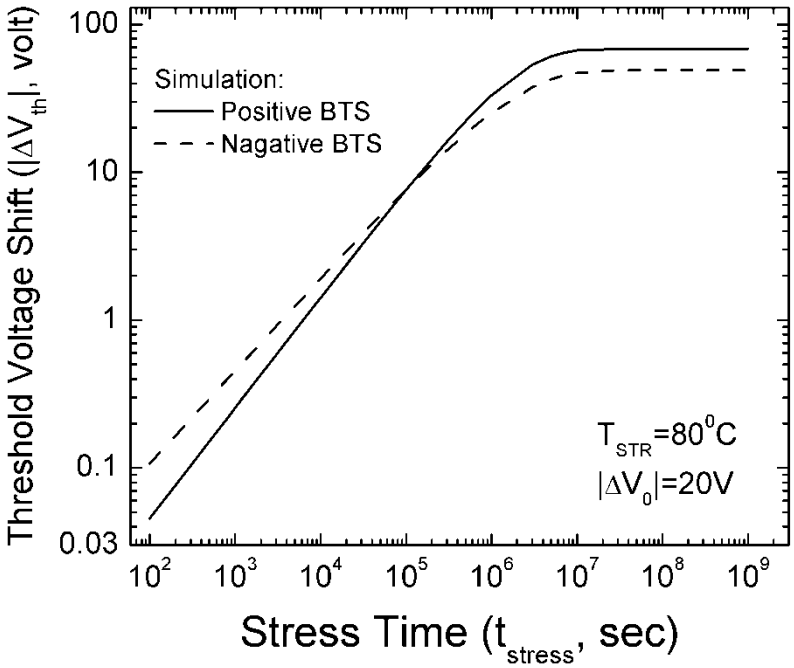


Figure 7.10 Simulated ΔV_{th} vs. stress time (t_{stress}) for (solid line) positive and (dash line) negative BTS. Parameters in Table 7.1 are used in simulation. For both stress polarities, T_{STR} and $|\Delta V_0|$ are 80^0C and 20V, respectively.

Model Parameters	Positive BTS	Negative BTS
α	1.41	1.30
β	0.75	0.63
τ_0 (sec)	1.24×10^{-5}	6.92×10^{-18}
E_τ (eV)	0.78	1.637

Table 7.1 Fitting parameters for stretched-exponential model used in this study.

simulating the ΔV_{th} over a longer stress time (upto 10^9 sec). Figure 7.10 shows that for positive BTS, model (7-1) predicts a saturation of ΔV_{th} at $t_{stress} > 9\times10^6$ secs. For negative BTS, the saturation occurs a bit longer at $t_{stress} > 7\times10^7$ secs. The β listed in Table 7.1 is close (< 8% difference) to the average value extracted from the $\log(\Delta V_{th})$ vs. $\log(t_{stress})$ plot based on (7-4) (for example, in positive BTS, $\beta \sim 0.76$; in negative BTS, $\beta \sim 0.7$). This also suggests that the short stressing time assumption ($t_{stress} << \tau$) is generally valid in this study. A small variation (~ 0.1 for both BTS polarities) is observed for β extracted from positive and negative BTS data under different T_{STR} with the average β of 0.75 and 0.63, respectively. In summary, our proposed analytical equation can not only serve as a universal model for describing the RF sputter a-IGZO TFT BTS instability but also provide valuable insights on the actual physical mechanism governing the observed instability.

Chapter 8

Electronic Noise in a-IGZO TFTs

8.1 Common Low Frequency Noise Sources in TFTs

In this chapter, we investigate the noise properties of the a-IGZO TFT. Electronic devices and circuits inevitably present random current (or voltage) fluctuations at their output terminals. These fluctuations, which are commonly referred to as "*noise*", are intrinsic in nature. Their existence is not due to improper testing setups or faulty process steps that can potentially be avoided by human effort; instead, they arise from the random, microscopic processes of the charge carriers, which are inherent in the electronic components. This is the type of noise behavior this chapter would like to explore.

The smallest input signal level for a certain circuit to process with acceptable quality is fundamentally limited by noise. To tolerate noise problem, the design parameters usually need to be modified. For instance, in active-pixel sensor (APS) circuit, designer may want to trade device / pixel area, frame rate, drain current, etc. with lower TFT noise [127]. Before discussing the noise properties, we should familiar ourselves with the representation of noise signal. Due to its random nature, predicting the instantaneous value of noise at any given time is not possible. However, the random process which governs the observed noise behavior can usually be analyzed by a statistical model. In many cases, the statistical

model can predict the average power of noise; and therefore, the noise sources are commonly represented as "noise power spectral density" in units of A^2/Hz or V^2/Hz.

This chapter begins with a brief review of the two noise sources commonly observed in TFTs [127, 128]: thermal and flicker (1/*f*) noise. In Section 8.2, the experimental apparatus and their operation principles will be discussed. Finally, the a-IGZO TFT noise properties will be investigated in Section 8.3.

8.1.1 Thermal noise

A resistor which is in thermal equilibrium with its surroundings shows random short-circuit current (or open-circuit voltage) fluctuations at its two terminals. Such noise was first measured by Johnson [129-131], and soon after, its power spectrum density was derived by Nyquist [132] from an argument based on thermodynamics and the exchange of energy between resistive elements under thermal equilibrium. Therefore, thermal noise is also frequently referred to as Johnson noise or Nyquist noise. In microscopic point of view, thermal noise is fundamentally due to the random thermal motion of the electrons within resistive material (similar to Brownian movement) [133].

The thermal noise of a resistor R can be modeled by a parallel current source, with a noise power spectral density of

$$S_I(f) = \frac{4kT}{R} \tag{8-1}$$

where S_I has the unit of A^2/Hz, k is the Boltzmann constant and T is the Kelvin temperature . Since (8-1) is independent of frequency, thermal noise is categorized as white noise [134]. In MOSFET, the transistor channel also exhibits thermal noise. By treating the channel as a resistor whose incremental resistance is a function of the position along

channel length direction, van der Ziel [135] showed that the thermal noise in transistor drain current is

$$S_I(f) = \gamma\, 4kT\, g_{ds0}, \tag{8-2}$$

where

$$\gamma = \frac{1 - v + \frac{1}{3}v^2}{1 - \frac{1}{2}v} \text{ and} \tag{8-3}$$

$$g_{ds0} \equiv \left(\frac{\delta I_D}{\delta V_{DS}} \right)\Bigg|_{V_{DS} \sim 0} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_{th}). \tag{8-4}$$

In (8-3), the v is defined as

$$v \equiv V_{DS} / (V_{GS} - V_{th}); \tag{8-5}$$

and g_{ds0} is the channel conductance when $V_{DS} \sim 0$V (linear region). It can be easily shown that, when $V_{DS} << (V_{GS}-V_{th})$, $v \sim 0$ and $\gamma=1$. On the other hand, at the on-set of saturation region (and also deep saturation region), $V_{DS}=V_{GS}-V_{th}$, so $v = 1$ and $\gamma = 2/3$. (Note: even though in deep saturation region the $V_{DS}>V_{GS}-V_{th}$, because there is a voltage drop on the pinch–off region, the actual voltage drop along the channel is still $\sim (V_{GS}-V_{th})$. Therefore, v should be equal to unity in deep saturation region as well.) Not just in MOSFET, equation similar to (8-2) has also been applied to model the thermal noise in TFT (i.e. a-Si:H TFT) [128].

8.1.2 Flicker (1/f) noise

For surface conducting devices like MOSFETs or TFTs, flicker noise is generally the dominated low frequency noise source. This type of noise is mostly observed with a drain current noise power spectral density inversely proportional to frequency:

$$S_I(f) \propto \frac{1}{f^{\Gamma}}, \tag{8-6}$$

where Γ is more or less constant (~1) and usually lies between 0.8 and 1.4 [133]. Hence the flicker noise is also often referred to as "1/*f* noise".

Although the physical origins of 1/*f* noise in MOSFET (or TFT) have been discussed for nearly half a century, they are still obscure and under active research (to name a few: [136-139]). There are two different schools of thought: number fluctuation (Δn) theory and mobility fluctuation (Δμ) theory. The number fluctuation theory treats the 1/*f* waveform as a superposition of a large number of relaxation processes (each with a Lorentzian power spectrum of $\frac{4\tau}{\left(1+\omega^2\tau^2\right)}$) with a wide spread of time constants (τ). More importantly, the distribution function of τ (ρ(τ)) should proportional to 1/τ ($\rho(\tau) \propto 1/\tau$, i.e. the process with shorter τ is more likely to occur) [138]. In year 1957, McWhorter [140] first proposed that the relaxation process could be originated from the electron random trapping / de-trapping and the distribution of trapping times might arise from the tunneling of charge from the semiconductor surface to traps located in the oxide. He suspected that the oxide traps are homogeneous within a specific depth range, because the ρ(τ) is proportional to 1/τ under this assumption. Christensson et al. later pointed out such trapping / de-trapping can occur near the channel / gate insulator interface and successfully extend this concept to the MOSFET [141]. The Δn model describes the transistor drain current noise (S_{ID}) by following equation [142]:

$$S_{ID} = \frac{k^*}{f}\frac{\mu_{eff}}{C_{ox}L^2}\frac{I_D V_{DS}}{\left(V_{GS}-V_{th}\right)} \tag{8-7}$$

where C_{ox} is the gate insulator capacitance per unit area. k^* is a coefficient related to the tunneling possibility between channel and gate insulator traps

$$k^* = \frac{q^2 D_t(E_F) kT}{\ln \frac{\tau_2}{\tau_1}}, \tag{8-8}$$

where $D_t(E_F)$ is the active trap density in the vicinity of the Fermi level (E_F), and τ_1 and τ_2 are the lower and upper boundaries of time constants involved in the trapping / de-trapping process. The drain current noise is also often represented as normalized noise, $S_{ID}/(I_D)^2$. In standard MOSFET model, the linear region drain current can be written as

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right]. \tag{8-9}$$

Combining (8-7) and (8-9), we can have

$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f}\frac{1}{C_{ox}^2 WL}\frac{1}{(V_{GS} - V_{th})}\left[\frac{1}{(V_{GS} - V_{th}) - 1/2 V_{DS}}\right], \tag{8-10}$$

or

$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f}\frac{1}{C_{ox}^2 WL}\frac{1}{(V_{GS} - V_{th})^2}\left(\frac{1}{1 - \nu/2}\right), \tag{8-11}$$

where ν is defined in (8-5). From previous section, we have shown that when $V_{DS} << V_{GS}-V_{th}$ (linear region), $\nu \sim 0$; and in saturation region, $V_{DS}=V_{GS}-V_{th}$, so $\nu = 1$. The same results can also be derived from 1/*f* gate voltage noise (or input referred noise) [143, 144].

McWhorter's Δn theory implies that 1/*f* noise is fundamentally a surface effect. In contrast to this concept, in 1969, Hooge claimed the 1/*f* noise is no surface effect by formulating an empirical law, which appears to be representative to many observed 1/*f* noises in homogeneous samples [145]. The empirical law stated that the normalized current noise is inversely proportional to the total number of charge carriers in sample

$$\frac{S_{ID}}{I_D^2} = \frac{C}{f} = \frac{\alpha_H}{f\ N} \tag{8-12}$$

where $C \equiv \alpha_H / N$; N is the total number of charge carriers involved in the conduction of the

sample and α_H is an empirical dimensionless constant (also called Hooge's parameter). In the subsequent work, Hooge *et al.* showed that the 1/f noise should originate from noise in lattice scattering, which in term, causes random mobility fluctuation [146]. Many other studies also support this idea [147]. The α_H was originally proposed as a "universal constant" for homogeneous materials with the value of 2×10^{-3} but it was soon be found to be technology / material dependent and in MOSFET, V_{GS} dependent [138, 139]. Nonetheless, α_H can still be considered as a quality indicator. In high quality Si or SiGe MOSFETs, α_H can range from 10^{-6}~10^{-4}. In a-Si:H TFTs, the α_H is reported to be ~10^{-2} [148]. α_H values in range of 5~20 have also been reported in organic TFTs [149].

Following Rhayem [150], we derive the $\Delta\mu$ model for MOSFET (or TFT) by starting with the total number of carrier in the transistor channel,

$$N = \frac{1}{q}\left[C_{ox}WL\left(V_{GS} - V_{th}\right)\right]. \tag{8-13}$$

Merge (8-13) into (8-12) we have

$$\frac{S_{ID}}{I_D^2} = \frac{q}{C_{ox}WL}\frac{\alpha_H}{f}\frac{1}{\left(V_{GS} - V_{th}\right)} \ . \tag{8-14}$$

The S_{ID} can also be re-written as a function of I_D, under the assumption of $V_{DS} << V_{GS}$-V_{th}

$$S_{ID} \cong \frac{\mu_{eff}q}{L^2}\frac{\alpha_H}{f}I_D V_{DS}. \tag{8-15}$$

It should be notice that (8-15) is also consistent with the results from Klaassen [151] and Vandamme's works [152]. To derive the S_{ID} in saturation region, we combine (8-15) and (8-9) [142]

$$S_{ID} = \frac{\alpha_H}{f}q\mu_{eff}^2 C_{ox}\frac{W}{L^3}\left(V_{GS} - V_{th}\right)^3 v^2\left(1 - \frac{v}{2}\right). \tag{8-16}$$

In saturation region, $v = 1$ and therefore

$$S_{ID} = \frac{1}{2}\frac{\alpha_H}{f}q\mu_{eff}^2 C_{ox}\frac{W}{L^3}\left(V_{GS} - V_{th}\right)^3$$

	McWhorter Δn model	Hooge Δμ model
Linear Region	$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f}\frac{1}{C_{ox}^2 WL}\frac{1}{(V_{GS}-V_{th})^2}$	$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{f}\frac{q}{C_{ox} WL}\frac{1}{(V_{GS}-V_{th})}$
Saturation Region	$\frac{S_{ID}}{I_{D\_sat}^2} = \frac{k^*}{f}\frac{2}{C_{ox}^2 WL}\frac{1}{(V_{GS}-V_{th})^2}$	$\frac{S_{ID}}{I_{D\_sat}^2} = \frac{\alpha_H}{f}\frac{2\cdot q}{C_{ox} WL}\frac{1}{(V_{GS}-V_{th})}$

Table 8.1 Normalized flicker noise spectral density (S_{ID}/I_D^2) for Δn and Δμ in MOSFET or TFT. C_{ox} is the gate insulator capacitance per unit area; W and L are TFT channel length and width, respectively.

$$= \frac{\alpha_H}{f} q\sqrt{2}\left(\frac{\mu_{eff}}{C_{ox}}\right)^{1/2} \frac{1}{W^{1/2}L^{3/2}} (I_{D\_sat})^{3/2}, \tag{8-17}$$

where I_{D_sat} is the drain current in saturation region. Alternatively, we can also obtain the normalized drain current noise under saturation region:

$$\frac{S_{ID}}{I_{D\_sat}^2} = \frac{\alpha_H}{f} q\sqrt{2}\left(\frac{\mu_{eff}}{C_{ox}}\right)^{1/2} \frac{1}{W^{1/2}L^{3/2}} (I_{D\_sat})^{-1/2} \tag{8-18}$$

By substituting standard MOSFET equation (e.g. (2-3)) for I_{D_sat} , (8-18) becomes

$$\frac{S_{ID}}{I_{D\_sat}^2} = \frac{\alpha_H}{f}\frac{2\cdot q}{C_{ox} WL}\frac{1}{(V_{GS}-V_{th})}. \tag{8-19}$$

Table 8.1 summarizes the normalized 1/*f* noise spectral densities predicted by both Δn and Δμ models. It should be noticed that both models have similar mathematical forms and are both inversely proportional to the device area [$(WL)^{-1}$]. Beside the dependence of 1/*f* noise on C_{ox} (or gate insulator thickness), dependence on effective gate voltage (V_{GS}-V_{th}) can also be used to differentiate these two models.

Assuming that during I/V measurement, a constant voltage maintains the pure DC level;

the observed 1/*f* noise in current can only arise from the fluctuation of sample resistance. Since the resistance depends on the density and mobility of the charge carriers, it is naturally to conclude that the 1/*f* noise is due to charge number or mobility fluctuation. Perhaps the difficulty in achieving a conclusive physical origin for 1/ noise is that numerous experimental evidences support (or against) either theory: Experimental results collected for homogeneous samples usually follow the Δμ model [145, 146]. In MOSFET, *n*-MOS 1/*f* noise obeys the Δn model while the Δμ model explains *p*-MOS 1/*f* noise better [136, 138, 139]. The 1/*f* noises in a-Si:H TFT generally follow the Δμ model [148] but a trend towards Δn mode was also found in short channel device (L < 5μm) [142]. It is possible that both mechanisms exist simultaneously in the device: In long channel TFT, the excess bulk defects cause the Δμ 1/*f* noise to be the predominant one. On the other hand, in short channel device, the impact of interface trapping/de-trapping can become more significant.

8.2 Experimental

8.2.1 Noise measurement setup

Figure 8.1 and 8.2 illustrate the experimental setup that is used to measure the TFT drain current noise power spectrum under different bias conditions. The device-under-test (DUT) is voltage biased, and its current noise is analyzed. The core of this system is the filter/amplifier unit (a.k.a. 9812B Noise Analyzer made by ProPlus Design Solution, Inc.). The unit contains high quality RC low-pass filters (cut-off frequency of 0.1Hz is used) for removing the SMU (source-measure unit) noise from semiconductor parametric analyzer (Agilent 4156C). Thus the DUT bias voltages are very close to the pure DC signals and "noise free". The output load resistor (R_D) and input series resistor (R_G) are used for the

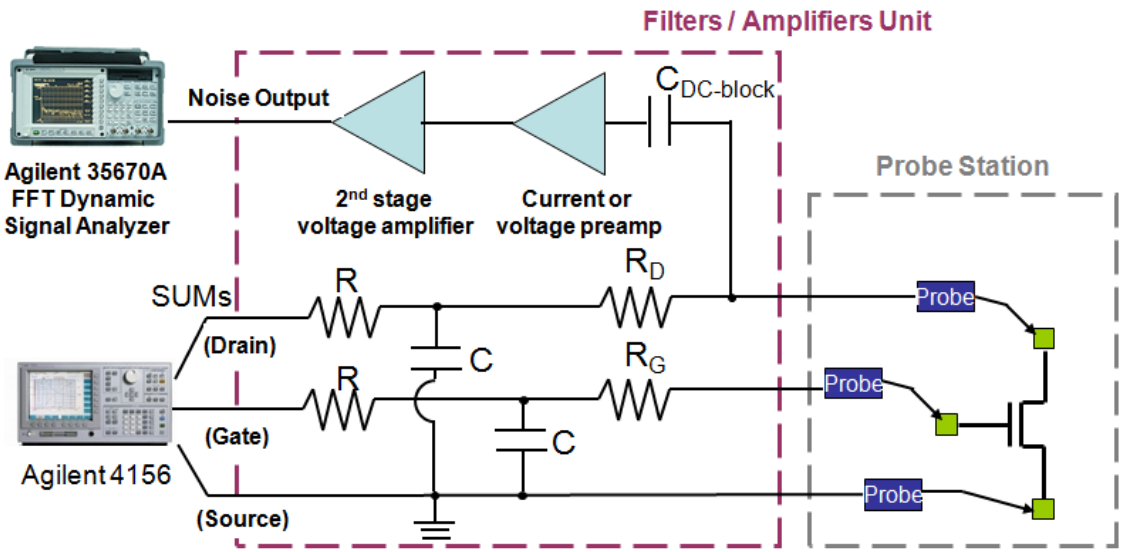


Figure 8.1 (Color) Circuit diagram of the experimental setup used for measuring the TFT drain current noise. The filter / amplifier unit is also known as 9812B noise analyzer. (Adapted from [153])

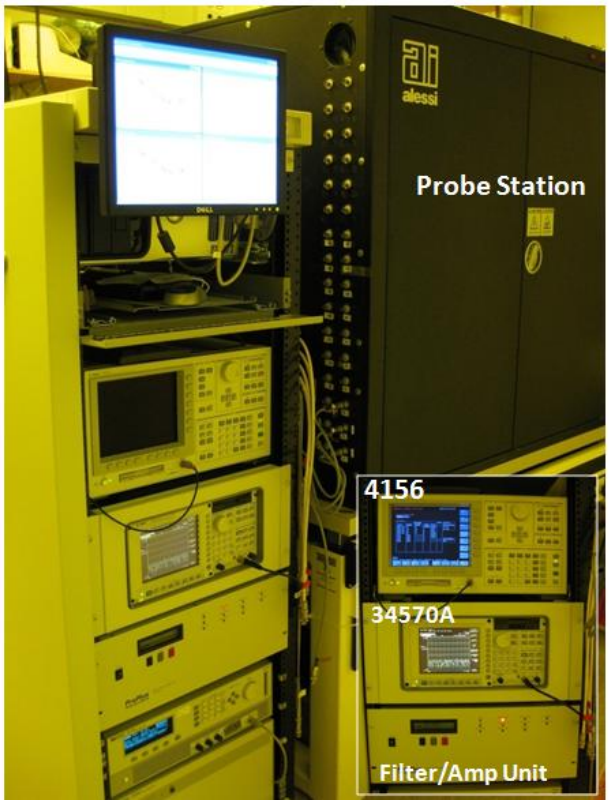


Figure 8.2 (Color) Photo of the noise measurement system. Device is placed inside the light-tight probe station, which also serves as a Faraday cage for electrical shielding.

purpose of impedance matching between the DUT and internal low noise amplifiers. The DUT can be either two or three terminals. For measuring resistor noise, the gate SMU is not used. For TFT noise measurement, the R_G is short (0 Ω) due to the high gate impedance. The computer program automatically selects optimal R_D according the bias condition and the selection of low noise amplifier [154]. For reference, the typical R_D value used in this study is 33KΩ or 100KΩ. The DC block capacitor (C_{DC_block}) serves as AC input coupling capacitance of low noise amplifiers. The amplifiers pick up and enhanced the AC noise signal form DUT. There are two amplifiers available in 9812B, voltage and current amplifiers. Each has a working frequency range of 1MHz and they are battery operated. The voltage amplifier has a voltage gain of 20; and the current amplifier has a feed-back resistor (R_a) of 40KΩ (Figure 8.3(b)). Both amplifiers are followed by a 2^{nd} stage amplifier with a voltage gain of 25. Therefore, the 9812B system can provide an overall voltage gain of 500 (Figure 8.3(a)) or current-to-voltage gain of 1mV/1nA on noise signal [153]. The selection between these two amplifiers usually depends on the device output impedance. For example, when TFT is bias in linear region, the output impedance is low and the voltage amplifier should be used. On the other hand, when the TFT is operated in saturation region with a high output impedance; the current amplifier should be chosen.

The noise measurement flow can be broken down into two stages. During the first stage, the computer controls the Agilent 4156C to establish bias on DUT (e.g. TFT or resistor). Multiple iterations are applied to make sure the DUT bias signals are stable and equal to the programmed value (< 2% error). The settling time usually takes at least four low-pass RC time constants, which correspond to ~40secs. During the second stage, the low noise amplifier circuit is engaged. The amplified TFT drain current noise signals are than collected by Agilent 35670A FFT dynamic signal analyzer. To have the frequency domain noise

spectrum, the 35670A applies fast Fourier transform (FFT) on the data collected in time domain. The entire frequency range is divided into several sub-bands by 35670A and the final noise spectrum is composed from data collected at each band. Progressive increases in average number are applied: data collected from low frequency band (0.4~25Hz) is average from ten measurements, while high frequency band (200 ~ 12.8 KHz) is average from more than forty measurements.

8.2.2 System calibration – thermal noise measurement

Figure 8.3 shows the equivalent circuits for noise measurements with voltage and current amplifiers. The R_D and I_{RD} are load resistor and its associated thermal noise source, respectively. R_{out} and I_X are the output impedance and the noise of the DUT, respectively. I_{Ra} is the thermal noise from the current amplifier feed-back resistor. R_{in} is the input impedance of the voltage amplifier. I_n and V_n are current noise source and voltage noise source associated with the amplifiers. The voltage amplifier output can be written as a function of above parameters as [155]

$$V_{OUT}^2 = A^2 R_{ref}^2 \left(I_X^2 + I_n^2 + \frac{4kT}{R_D} \right) + A^2 V_n^2 \left(\frac{R_{in}}{R_{in} + R_D // R_{out}} \right)^2 \tag{8-20}$$

and $$R_{ref} = R_D // R_{out} // R_{in} \ . \tag{8-21}$$

Similarly, the output of current amplifier is

$$V_{OUT}^2 = R_a^2 \left[I_X^2 + I_n^2 + 4kT \left(\frac{1}{R_D} + \frac{1}{R_a} \right) + V_n^2 \left(\frac{1}{R_D} + \frac{1}{R_a} \right)^2 \right]. \tag{8-22}$$

Since the amplifier output contains unwanted signal, the computer program performs the data correction routine on raw data based on (8-20) and (8-22) to extract the accurate noise

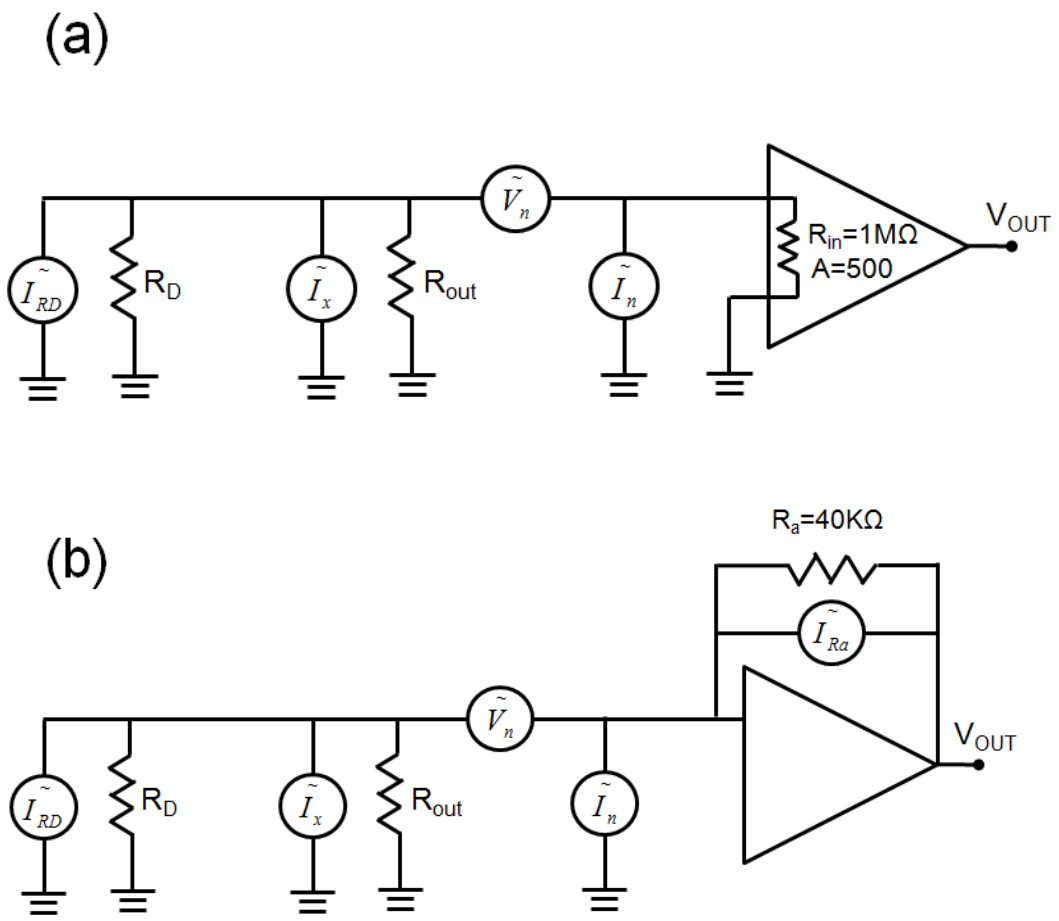


Figure 8.3 The equivalent circuits for noise measurements with (a) voltage and (b) current amplifiers. (Adapted from [155])

Amplifier	**$(I_n)^2$ (A^2/Hz)**	**$(V_n)^2$ (V^2/Hz)**
Voltage	1.598×10^{-25}	5.892×10^{-18}
Current	1.960×10^{-25}	2.750×10^{-20}

Table 8.2 Optimized amplifier noise parameters (I_n and V_n) for the measurement system used in this study.

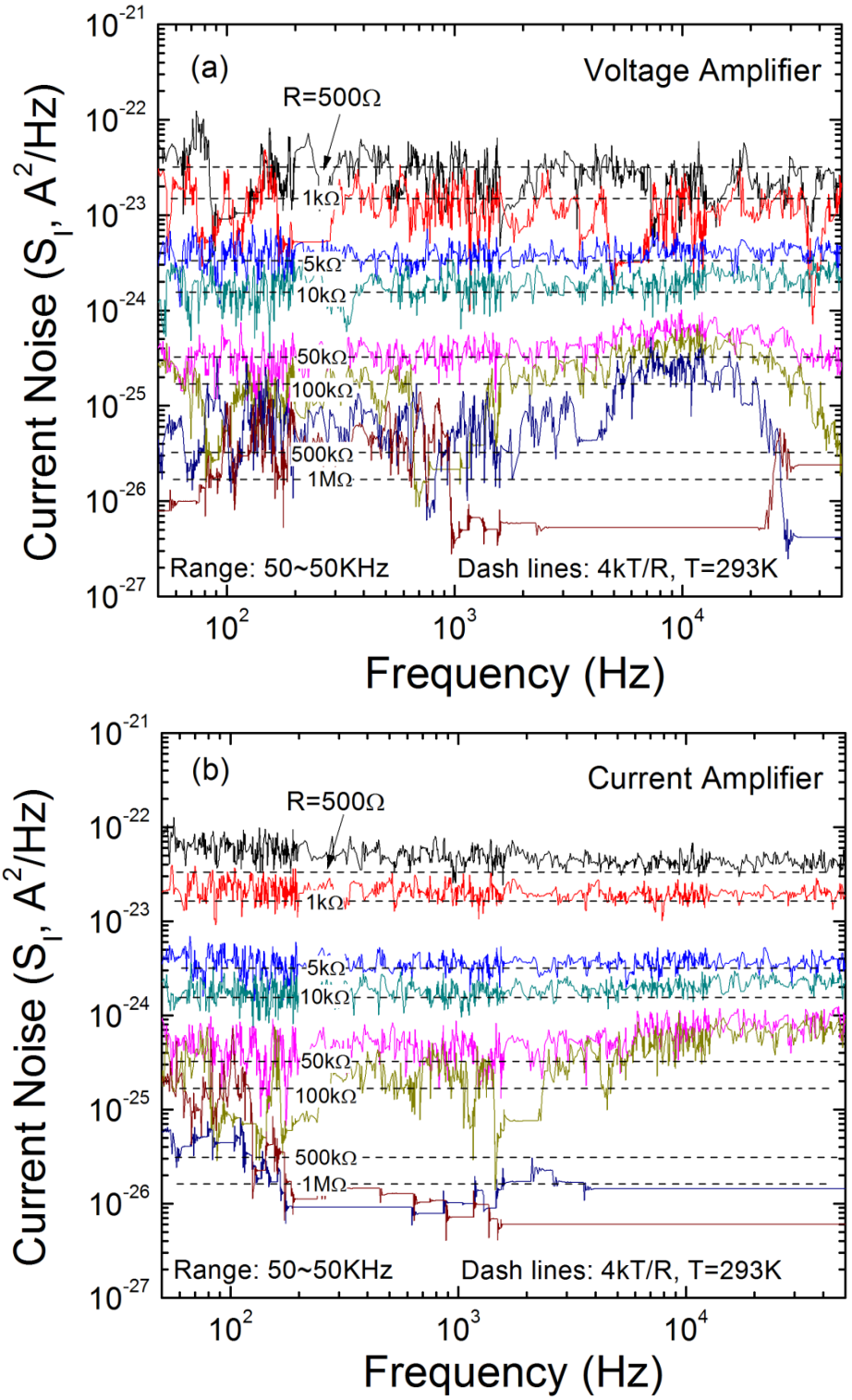


Figure 8.4 (Color) Thermal noise spectrums measured from high quality metal film resistors. Both (a) voltage and (b) current amplifier are used. Solid lines: actual measurement results (with data correction); dash lines: theoretical values.

signal of interest (i.e. I_X). Obviously, accurate I_n and V_n values are crucial for this data correction process and the extraction of amplifier noise sources (i.e. I_n and V_n) can be done by measuring the noise from internal R_D resistances during the calibration process [154]. Table 8.2 lists the optimized noise parameters we extracted. To verify the overall system performance, we measured the thermal noise spectrums from high quality metal film resistors ranging from 500 ~ 1MΩ (Figure 8.4). It should be noticed that these are all corrected data with parameters listed in Table 8.2 being used. From this data, we estimated the noise detection limit for our system to be ~$10^{-25}A^2$/Hz, corresponding to R < 100KΩ. In addition, the measurement data are very close to the theoretical values, proving that the optimized parameters (Table 8.2) are properly extracted.

8.3 Noise Properties of the a-IGZO TFTs

8.3.1 Example of the a-IGZO TFT drain current noise spectrum

Figure 8.5 shows two examples of S_{ID} spectrums collected for a-IGZO TFTs. Both data are measured for the common gate, RF sputter a-IGZO TFT whose properties have been discussed in Chapter 2 (In Section 8.3, unless otherwise specify, all noise spectrum data are collected from this type of TFT.) It is clear that when the device is operating under a higher I_D (by increasing V_{GS}), its noise level also increases. The noise spectrums have a $1/f^{\Gamma}$ shape, which almost extends the entire measurement range (4 ~ 10 KHz). The Γ of the spectrums in Figure 8.5 is 0.9, which is determined by the best linear fits (dash lines) of (8-6) from data between 6 ~500Hz. In fact, throughout this study, the Γ values we extracted are between 0.89 and 1.05 (with an average of 0.95). This fits the general description

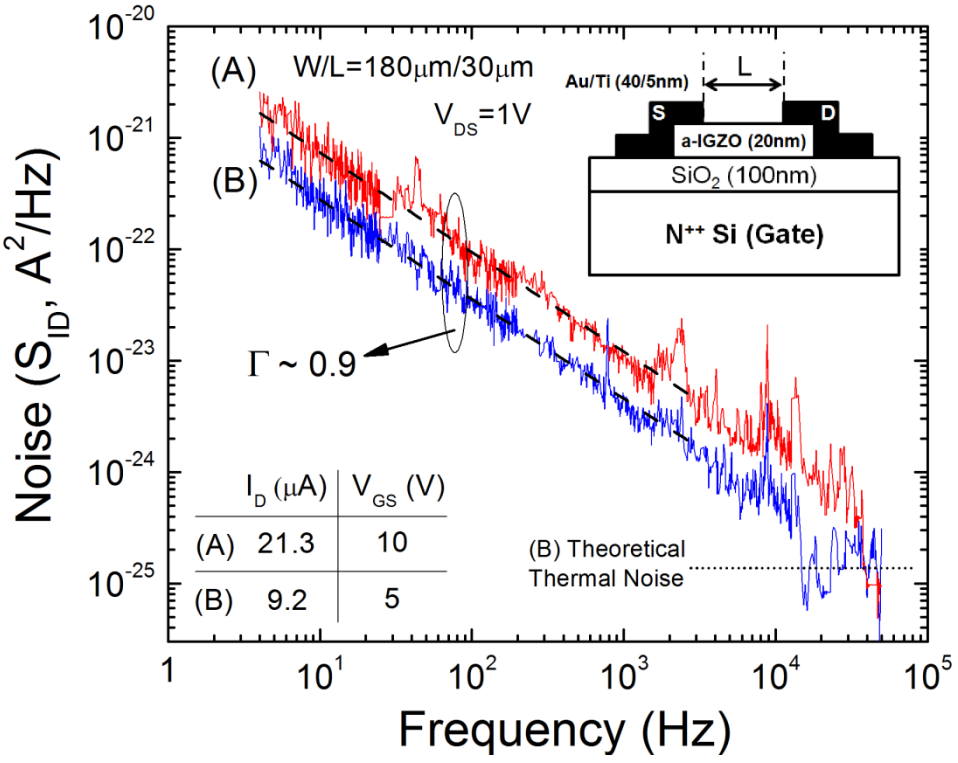


Figure 8.5 (Color) Example of a-IGZO TFT drain current noise spectrum (S_{ID}). Two linear region noise data are shown (V_{DS}=1V). Data A (red) and B (blue) are measured under V_{GS} of 10V and 5V, respectively. (Inset) The cross section view of the common gate, RF sputter a-IGZO TFT used in measurements. (Dot line) Thermal noise floor of condition B estimated from the theoretical model (8-2).

of 1/*f* noise from other literature [133, 138] and suggests the 1/*f* noise is the dominated noise source in our a-IGZO TFTs.

Data (B) in Figure 8.5 shows a small "flat" section in the high frequency range (>10 KHz). This part of spectrum is not very clear because it is approaching the detection limit of our setup. Nonetheless, the measured power spectrum density is close to the theoretical thermal noise floor predicted by (8-2). In most of the measurements, such as data (A), the flicker noise dominates the S_{ID} spectrum. Since this is the noise source that usually effects the most on circuit performance [127], we focus on the low frequency (f < 1KHz) 1/*f* noise in a-IGZO TFT for the rest of this study.

Device	TFT Dimensions			Measurement Conditions		R_{S_IGZO} (Ω/□)
	W (μm)	L (μm)	Area (μm^2)	V_{DS} (Volt)	I_D (A)	
#1	300	50	15000	1	5×10^{-5}	1.2×10^{5}
#2	180	60	10800	1.2	3×10^{-5}	
#3		30	5400	0.6		
#4		10	1800	0.2		
#5	60	10	600	0.2	1×10^{-5}	
#6	30	5	150	0.1	5×10^{-6}	

For all devices:
Surface current density ($\kappa = I_D/W$) is 0.167μA/μm.
Electric field along the channel ($E=V_{DS}/L$) is 0.02V/μm.

Table 8.3 Normalized measurement conditions for studying the channel area dependent noise properties.

8.3.2 Noise as a function of channel area

To further verify the nature of low frequency noise in a-IGZO TFTs, the dependence of noise on TFT channel area is investigated. The low frequency noise spectrums were measured from a set of devices with channel area ranging from 150 to 15,000 μm^2 (Table 8.3). Since these devices have different channel length (L), channel width (W) and small variation in threshold voltage (V_{th}), the normalized measurement conditions listed in Table 8.3 were used to properly extract noise spectrums. For measuring TFTs with different W, we control the drain currents (I_D) so that the surface current density ($\kappa = I_D/W$) is kept as a constant of 0.167μA/μm. For measuring TFTs with different L, we control the drain-to-source voltage (V_{DS}) so that the electric field along the channel ($E=V_{DS}/L$) is kept as a constant of 0.02V/μm. These values are chosen to ensure that all devices are under linear region during the noise measurement and the signal strengths are well above the detection limit. The concept of the normalization can be better understood by defining the a-IGZO

channel sheet resistant (R_{S_IGZO}) as

$$R_{S\_IGZO} \equiv \left(\frac{V_{DS}}{I_D}\right)\left(\frac{W}{L}\right) = \frac{E}{\kappa}. \tag{8-23}$$

Therefore, by maintaining the E and κ as constant, our normalized conditions give the same R_{S_IGZO} of 1.2×10^5 Ω/□ for all TFTs. By substituting the linear-region (V_{DS} << V_{GS}-V_{th}) TFT drain current equation (2-1) into (8-23), R_{S_IGZO} can also be expressed as

$$R_{S\_IGZO} = \left[\mu_{eff} C_{ox}\left(V_{GS} - V_{th}\right)\right]^{-1} . \tag{8-24}$$

Combine (8-13) and (8-24), we can then express the total number of electrons (N) in the TFT channel in terms of R_{S_IGZO} by:

$$N = \frac{W \cdot L}{q \cdot \mu_{eff} \cdot R_{S\_IGZO}}. \tag{8-25}$$

Equation (8-25) suggests that the N is directly proportional to the TFT channel area in our experiments.

Figure 8.6(a) illustrates the examples of noise measurement results. To minimize the error during noise data extraction, we first perform the best fits of the normalized noise spectrums to (8-12) or in its logarithmic form:

$$\log\left(\frac{S_{ID}}{I_D^2}\right) = \log C - \log f \tag{8-26}$$

from 6 to 500 Hz. This approach is valid because as we have pointed out in the previous section, all of our noise spectrums have the slopes very close to 1/*f*. The dash lines in Figure 8.6(a) represent such fits and the values of noise pre-factor C can be extracted from the *Y*-intercepts. It should be noticed that the pre-factor C can completely represent the entire spectrum and the S_{ID}/I_D^2 value can be calculated by (8-12) or (8-26) at any frequency point of interest. The S_{ID}/I_D^2 values at 30Hz for different TFTs are then estimated.

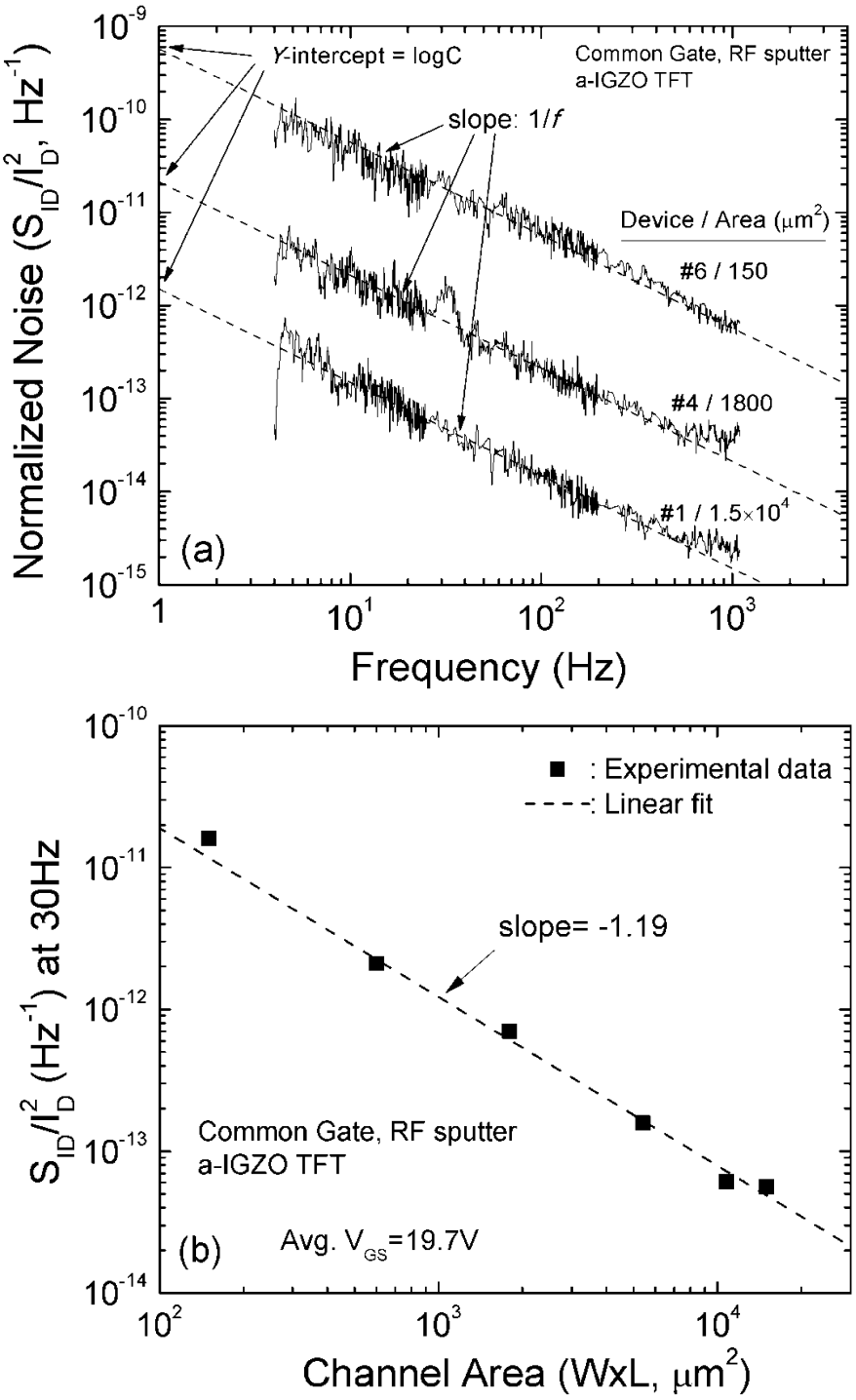


Figure 8.6 (a) Examples of the normalized noise spectrums collected from three TFTs with different channel areas (150, 1800 and 1.5×10^4 μm^2). Dash lines are the best linear fits to equation (8-26). (b) Normalized a-IGZO TFT drain current noise (S_{ID}/I_D^2) versus channel area. Data points (■) are sampled at 30Hz. Dash line is the best linear fit to the experimental data.

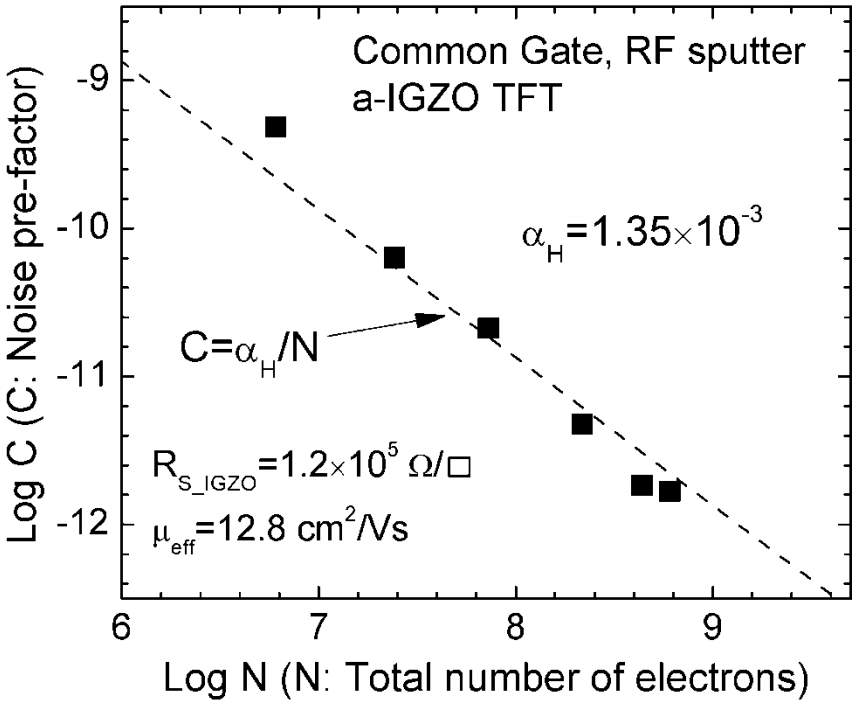


Figure 8.7 Illustration of α_H extraction based on area-dependent noise data. The total carrier numbers in TFT channel (N) are calculated by (8-25) and are proportional channel area. Noise pre-factors C are numerically extracted from experimental noise spectrums as illustrated in Figure 8.6(a). Symbol: experimental data; dash line: suggested best fit to the Hooge model (8-27).

As shown in Figure 8.6(b), it is clear that the S_{ID}/I_D^2 is inversely proportional to the channel area (W×L) with a dual-log slope very close to -1. This property further confirms that the observed low frequency noise in a-IGZO TFT is flicker noise in nature and the contribution from TFT parasitic resistances can be ignored [139]. However, since both Δn and $\Delta\mu$ theories predict the same dependence on area (Table 8.1), to discriminate between these two models, the 1/*f* noise must be studied as a function of gate voltage. This is the topic of next section.

If the $\Delta\mu$ model (8-12) is valid for our a-IGZO TFTs, we may extract the α_H by following the methodology from Hooge [145]. In Figure 8.7, the noise pre-factors (C) from

TFTs with different areas are plotted as a function of N, which is calculated by (8-25), in a dual-log scale. [The μ_{eff} =12.8cm^2/Vs (extracted from TFT #3) is used for N calculation.] Hooge's model states that the C should be inversely proportional to N [145]:

$$C = \frac{\alpha_H}{N}. \tag{8-27}$$

As shown in Figure 8.7, our experimental data agree fairly well to the model and from the suggested best fit of experimental data to (8-27), the α_H is determined to be 1.35×10^{-3}. [α_H is calculated from the *Y*-intercept of the dash line, which is not shown in Figure 8.7.]

8.3.3 Noise as a function of gate voltage

The dependence of TFT drain current noise on gate voltage was studied. The noise spectrums of a-IGZO TFT were measured under both linear (V_{DS}=1V) and saturation (V_{DS}=12V) regions. In order to extract the noise pre-factors S and S_{ID}/I_D^2 values, we followed the same methodology depicted in Section 8.3.2: the S values are first determined by the best linear fits of (8-26) from the normalized noise spectrums between 6 ~ 500Hz. The S_{ID}/I_D^2 values (e.g. at 30Hz) can then be calculated from (8-12). Figure 8.8 and 8.9 illustrate that the normalized drain current noise (S_{ID}/I_D^2) of our a-IGZO TFT has the power law dependence with V_{GS}-V_{th}. The power law coefficient is extracted to be between -1.1 and -1.2, which is closed to the prediction of mobility fluctuation ($\Delta\mu$) model (i.e. slope= -1, Table 8.1). A similar trend has also been observed for the a-Si:H TFT sample (Figure 8.8), which was fabricated by an industrial standard process [156, 157]. We further extracted the α_H from the linear region noise data. By rearranging (8-14), the α_H can be calculated by

$$\alpha_H = \left(\frac{S_{ID}}{I_D^2}\right)\frac{C_{ox}WL\,f}{q}\left(V_{GS}-V_{th}\right). \tag{8-28}$$

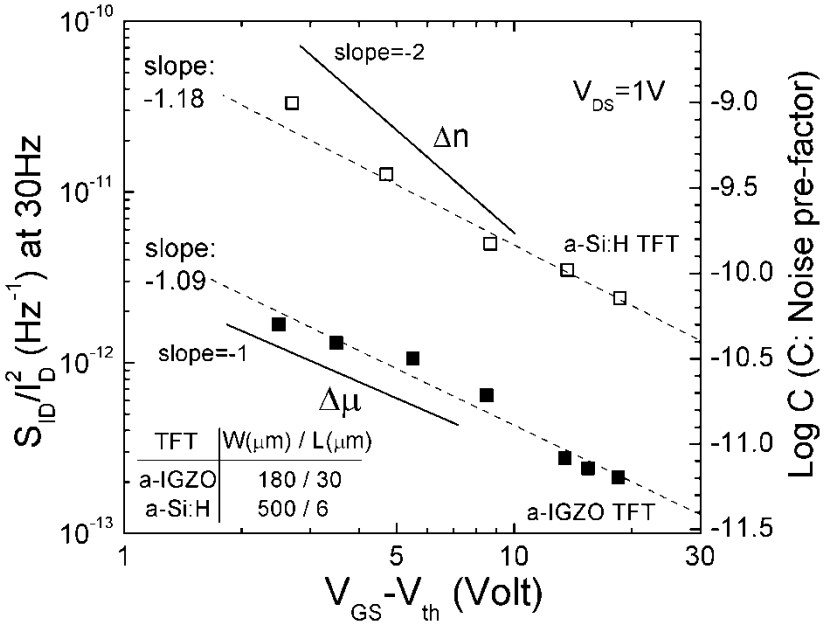


Figure 8.8 Linear region (V_{DS}=1V) S_{ID}/I_D^2 (at 30Hz) and noise pre-factor C as a function of V_{GS}-V_{th}. Solid (■) and open symbols (□) are experimental data for a-IGZO and a-Si:H TFTs, respectively. Dash line: linear fit to the experimental data. Solid lines with slope of -2 and -1 are also provided for the aid of eye.

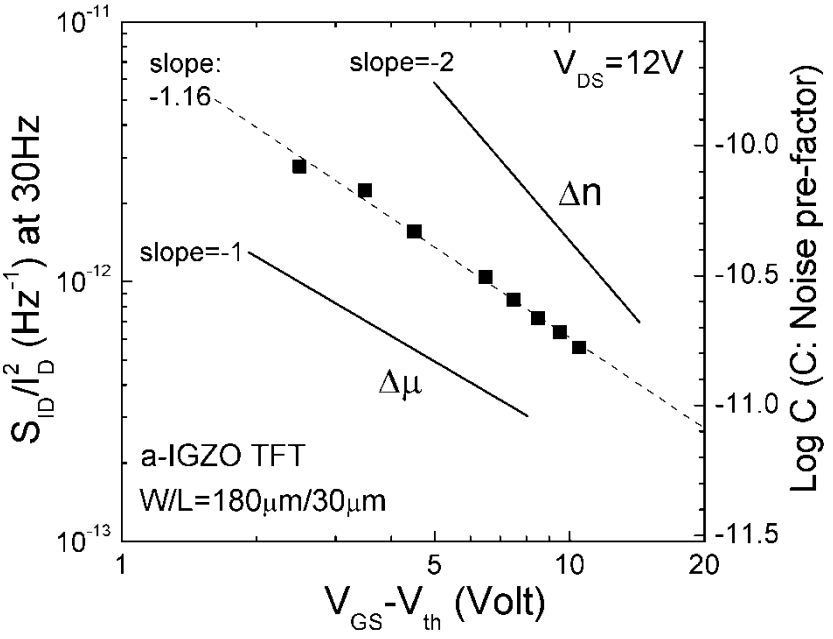


Figure 8.9 Saturation region (V_{DS}=12V) S_{ID}/I_D^2 (at 30Hz) and pre-factor C as a function of V_{GS}-V_{th}. Symbols: experimental data; dash line: linear fit to the experimental data.

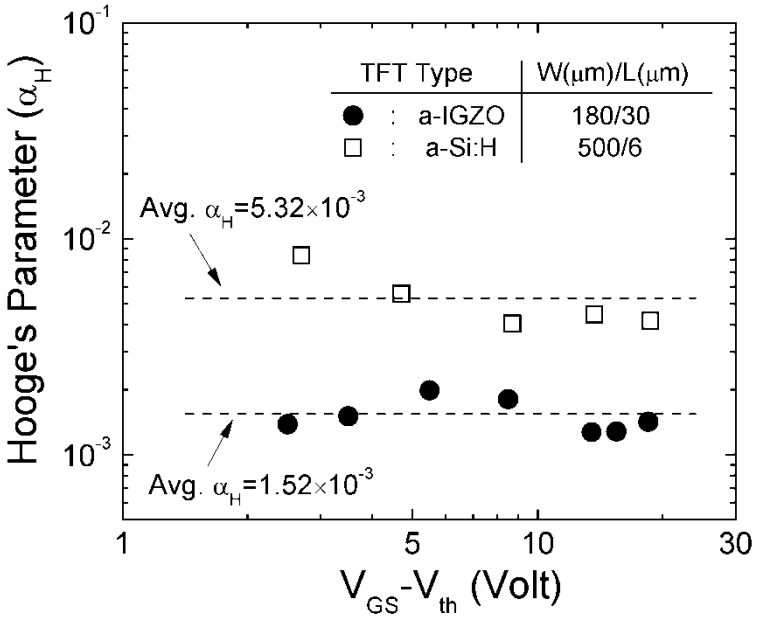


Figure 8.10 Hooge's parameters (α_H) versus V_{GS}-V_{th}. α_H values are extracted from the linear region noise data (V_{DS}=1V) based on (8-28). Symbol (●) and (□) are α_H values for a-IGZO and a-Si:H TFTs, respectively. Dash lines indicate the average α_H values.

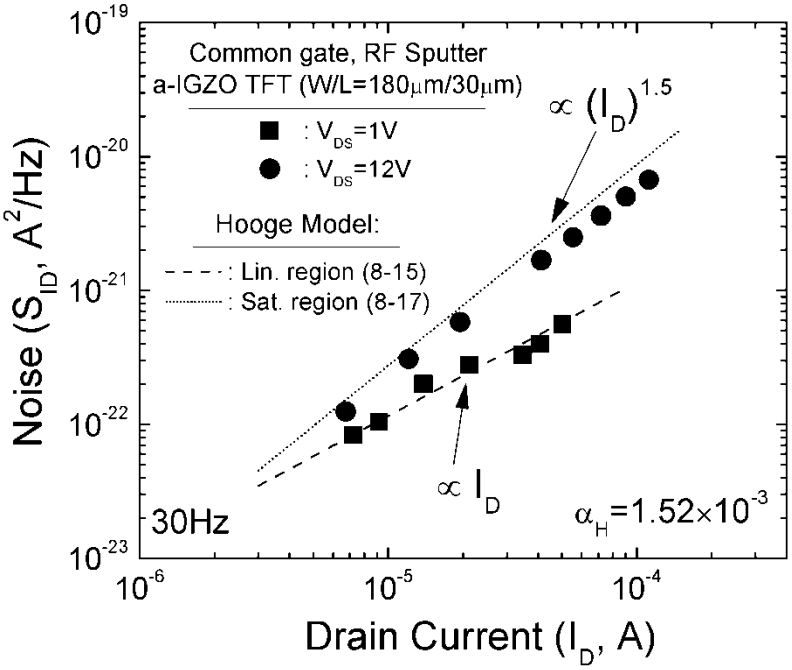


Figure 8.11 Drain current noise power density (S_{ID}, sampling at 30Hz) of a-IGZO TFT as a function of drain current (I_D). Symbol (■, linear region) and (●, saturation region) are experimental data. Dash and dot lines are calculated values based on Hooge Δμ model.

As shown in Figure 8.10, α_H is independent of V_{GS}-V_{th} for a-IGZO TFT (and also a-Si:H TFT). This property strongly suggests that the 1/*f* noise in a-IGZO TFT follows $\Delta\mu$ theory. The α_H has a value of 1.52×10^{-3}, which is very close to the value extracted from area dependent noise data ($\alpha_H = 1.35\times10^{-3}$, Figure 8.7). As a comparison, the a-Si:H TFT has a higher reported α_H either from our own measurement (5.32×10^{-3}) or other group ($\sim10^{-2}$ [148]). The α_H is frequently used as a figure of merit for the comparison of different technologies and it is usually lower for a higher quality material [138]. In amorphous semiconductor TFT, the α_H is thought to be fully, or at least partially, linked to the bulk defects [142]. Therefore, the observation in our experiments might be explained by a lower concentrations of conduction-band tail states in a-IGZO than as in a-Si:H, which have also been suggested by photofield-effect analysis (Chapter 4) and numerical simulation (Chapter 6).

Finally, to verify our extraction results, Figure 8.11 demonstrates the use of Hooge $\Delta\mu$ model in simulating the a-IGZO TFT S_{ID}. Just like what has been illustrated in Figure 8.5, we first perform the best linear fits of (8-6) [note: not (8-26)] from the noise spectrums between 6~500Hz. The experimental S_{ID} values shown in Figure 8.11 are then extracted from these fits at 30Hz. Equation (8-15) and (8-17) are used to calculate the simulated S_{ID} values (dash and dot lines). The α_H, μ_{eff}, C_{ox}, L and W used in the calculations are 1.52×10^{-3}, $12.8 cm^2/Vs$, 3.453×10^{-8} F/cm^2, 30μm and 180μm, respectively. The experimental data closely follow the trend simulated by the linear region equation (8-15). In addition, the saturation region noise also shows the $(I_D)^{1.5}$ law, as predicted by (8-17).

8.3.4 Noise from different device structures

The dependence of TFT drain current noise on device structure was also investigated. We measured the noise properties for three different kinds of RF sputter a-IGZO TFTs, which include common gate (type I / II) and defined gate devices (type III). Type I and type II TFTs have the same structure but one of them (type II) is not thermally annealed. Information related to their structures and electrical properties are listed in Table 8.4. Reader can refer to Section 2.1.2 and Section 2.1.3 for their detail processing steps. The linear region transfer properties for these TFTs are provided in Figure 8.12. In order to compare the I/V properties from different TFTs, a normalized scheme is adopt

$$\frac{I_D}{V_{DS}C_{ox}W/L} = \mu_{eff}\left(V_{GS} - V_{th}\right). \tag{8-29}$$

Compare to type I TFT, the type II TFT has a lower μ_{eff} and a higher V_{th}. This is due to the lack of thermal annealing process during TFT fabrication. In addition, the type II TFT drain current is less responsive to gate voltage near the on-set of on-region (i.e. Figure 8.12 (a), V_{GS}=3~5V). A similar phenomenon has also been noticed in 2D numerical simulation (Figure 6.1), and this could be closely associated with the increase in a-IGZO conduction band-tail slope (E_a). Therefore, we suspect that the thermal annealing is a critical step in making a high performance a-IGZO TFT with the reduced conduction band-tail slope.

We collected the noise spectrums for these three TFTs at the same $I_D/(V_{DS}C_{ox}W/L)$ of (~96.5cm^2/sec) and drain voltage (1V). The type II TFT has the highest normalized noise (S_{ID}/I_D^2), while the type I TFT has the lowest (Figure 8.13). It should be noticed that the high S_{ID}/I_D^2 of type II TFT is not due to its low mobility (or drain current), since both TFTs are measured at the same I_D of 2×10^{-5}A. If the previous speculation upon the annealing-induced band-tail states reduction is true, than our noise result supports the earlier idea

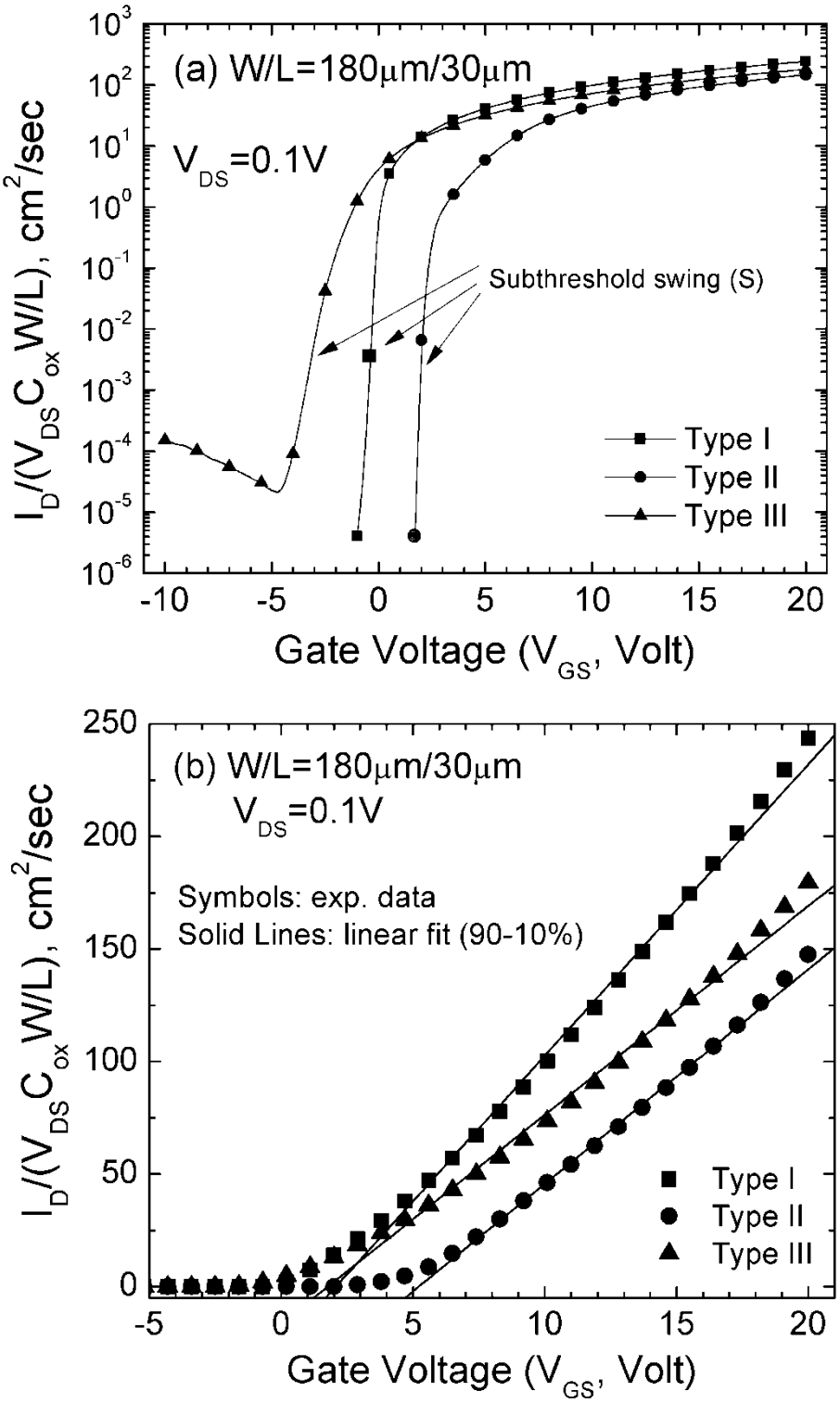


Figure 8.12 Normalized linear region transfer properties of various RF sputter a-IGZO TFTs in (a) semi-log and (b) linear plots. The definition of normalized *Y*-axis is in (8-29).

Various RF Sputter a-IGZO TFT Structures Used in Noise Study				
Device	**Structure**	**Gate Insulator**	**Annealing**	**Capping Layer**
Type I	Common gate	Thermal SiO_2 (100nm)	Yes	No
Type II			No	
Type III	Defined gate	Sputter SiO_2 (200nm)	Yes	Sputter SiO_2 (100nm)

Electrical Properties of Different RF Sputter a-IGZO TFTs			
Device	**μ_{eff} (cm^2/Vs)**	**V_{th} (V)**	**S (V/dec)**
Type I	12.8	2.07	0.15
Type II	9.54	5.21	0.14
Type III	9.28	1.77	0.52

Table 8.4 Structures and electrical properties of various RF sputter a-IGZO TFTs.

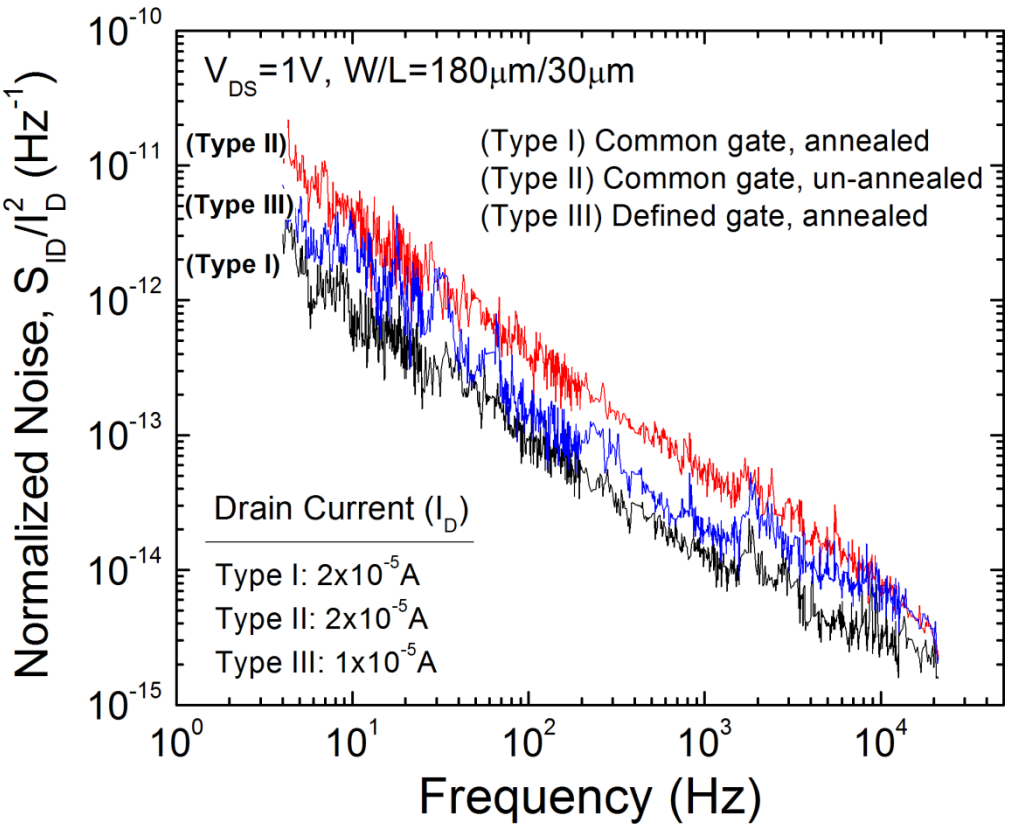


Figure 8.13 Normalized noise spectrums collected from various RF sputter a-IGZO TFTs.

that the 1/*f* noise in amorphous semiconductor TFT is primarily dominated by the bulk defects [142]. Nonetheless, because the TFT with 200nm sputter SiO_2 gate insulator (type III) has higher noise than the one with 100nm thermal SiO_2 (type I), our result also suggests that the gate insulator thickness and/or its interface properties may influence the noise level in a-IGZO TFT. In conclusion, we found that the TFT 1/*f* noise is not only an electrical property that is important for circuit design, but may also be used as a sensitive diagnostic tool to qualify the quality of semiconductor bulk / interface.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

In this dissertation, the inverted-staggered a-IGZO TFTs made by pulse-laser deposition (PLD) and RF magnetron sputtering have been investigated. The processing steps have a low thermal budget and the annealing temperature was kept below 300^0C. This is highly desirable for device fabrication over larger area glass or flexible substrates. The electrical properties of the a-IGZO TFT were evaluated. Compared to a-Si:H TFTs, a–IGZO TFTs have a much higher (×10 times) field-effect mobility (μ_{eff} =7~12 cm^2/Vs), excellent switching properties (subthreshold swing < 420mV/dec), and a low off-current (I_{D_off} < 1pA). This superior performance matrix makes a-IGZO TFTs suitable for demanding applications like large area HDTVs or high resolution flat panel imagers.

The advanced electrical analyses were also used to reveal more detail information of a-IGZO TFT electrical properties. Through transmission line analysis (TLM), the source/drain (S/D) series resistance in a-IGZO TFT is found to be only fraction of (1/1000) the typical value for a-Si:H TFT. Both aluminum (Al) and titanium (Ti) can be good metal materials for forming ohmic contact with a-IGZO. More importantly, the a-IGZO film thickness should be kept thin (< 40nm) to realize low S/D series resistance. Due to the

finite conduction band-tail slope in a-IGZO, the μ_{eff} in a-IGZO TFT is observed to be gate voltage dependent. We proposed a non-linear model to accurately model the TFT I/V properties. Such model is expected to serve as a good measurement standard, which can facilitate the comparison of the a-IGZO TFT electrical properties between research groups around the world.

Because the a-IGZO will be primarily used in optoelectronic applications; the TFT photofield-effect has also been studied. Our result shows that the a-IGZO TFT was stable under visible light illumination and suggests the possibility of operating a-IGZO TFT under a direct transmission mode without a light shielding electrode, which could increase the pixel aperture ratio. On the other hand, the a-IGZO TFT channel starts to absorb the light when the photon energy is approaching or above its optical band gap (~3eV, near UV region). The increase of I_{D_off} is proportional to the UV illumination intensity with a high quantum efficiency. This shows the potential for using a-IGZO TFT as UV-light photo-sensor / imager. By adapting the well developed photofield–effect theory for a-Si:H TFT, experimental data can be modeled and the a-IGZO mid-gap density-of-states (DOS) properties can be extracted. Compared to a-Si:H TFT, a low subthreshold swing in a-IGZO TFT is primarily due to a low mid-gap DOS.

We also demonstrated the device physics based on 2-D numerical simulation. For the first time, the DOS model, which can accurately describe the electrical properties of the a-IGZO thin film, was developed. The donor-like oxygen vacancy (OV) states are also included in DOS to reflect the nature of such defects. The simulation result suggests that the a-IGZO TFT has a very sharp conduction band-tail slope. The active layer is electrically “thin”; and both front and back channels can largely affect the TFT electrical properties. The 2D simulation technique was used to predict the potential impact of band-tail

states, S/D contact resistances and OV states on TFT I/V properties. Distinctive electrical features were discussed for the purpose of yield / diagnostic analysis.

To evaluate the a-IGZO TFT electrical instability, a systematic bias-temperature stress (BTS) study of RF sputter a-IGZO TFT was conducted. Both positive and negative BTS are applied and found to cause a positive and negative shift in transfer characteristics, respectively. We have demonstrated that the stretched-exponential equation can be used to model the BTS induced threshold voltage shift (ΔV_{th}) in a-IGZO TFTs. The model can also predict the dependence of ΔV_{th} evolution on stress voltage and temperature. This suggests that the charge injection from active layer and sub-sequent trapping near interface plays an important role in a-IGZO TFT electrical instability. In addition, we found that electron encounter a lower energy barrier which implies that the electron injection into state located near oxide/a-IGZO channel or oxide gate dielectric can be more efficient than hole-injection during the BTS experiments. This is similar to the case of c-Si MOSFET where barrier height for hole-injection into the oxide is larger than electron injection.

Finally, the low frequency noise properties of a-IGZO TFT were studied. The 1/*f* noise is the dominated noise source in a-IGZO. The TFT noise is found to be inversely proportional to the channel area and may limit the minimum TFT size to be used in detector circuit design. By studying the 1/*f* noise as a function of gate voltage, we determined that the 1/*f* noise in a-IGZO TFT follows the Hooge's mobility fluctuation model. The model is able to well predict the linear and saturation drain current noises. Compared to a-Si:H TFT, the a-IGZO TFT has a lower noise level in nature (lower Hooge's parameter) and this is very attractive to low-noise applications such as large area medical imager. The 1/*f* noise is also sensitive to the a-IGZO bulk / interface properties and may be used as a diagnostic tool for quality control.

9.2 Recommendations for Future Work

Two directions are suggested for future a-IGZO TFT research:

- High performance, low-noise a-IGZO TFT structure

The current a-IGZO TFT structure should be further improved and optimized. An industrially friendly process is also crucial for the future success in this technology. The development of a novel TFT passivation structure may be necessary. Such passivation structure should allow a thin a-IGZO layer while provide necessary protection. Optimization on the gate insulator is also inevitable, since the defects in oxide layer or near oxide/a-IGZO interface are known to be the cause for TFT instability and excess noise. Finally, the possibility of noise reduction by improving a-IGZO film quality (through thermal annealing or better deposition condition) should be explored.

- a-IGZO TFT based active pixel sensor (APS) circuit

The low noise nature of a-IGZO TFT makes it much more suitable to be used in APS circuit than a-Si:H TFT. High μ_{eff} of the a-IGZO TFT also means that the same current gain could be achieved in a smaller TFT area, a key factor for the potential enhancement in sensor resolution. We thus suggest implementing the a-IGZO TFT in APS circuit. Because such circuit may need to interact with the illumination from environment, the TFT shielding would be an important topic to investigate. How to properly interconnect the TFT circuit and photo-sensing device should also be carefully studied. Ideally, the photodiode on-the-top structure is the best approach since it allow a nearly 100% pixel aperture ratio. Nonetheless, the process compatibility is not always guarantee. Finally, since a high density pixel array is involved, the development of integrated gate driver may also be necessary.

Appendix – List of Publications

Journal papers:

(1) T.-C. Fung, C.-S. Chuang, C. Chen, K. Abe, R. Cottle, M. Townsend, H. Kumomi and J. Kanicki, "Two-Dimensional Numerical Simulation of Radio Frequency Sputter Amorphous In-Ga-Zn-O Thin-Film Transistors," J. Appl. Phys. 106, 084511 (2009)

(2) T.-C. Fung, K. Abe, H. Kumomi and J. Kanicki, "Electrical Instability of R.F. Sputter Amorphous In-Ga-Zn-O Thin-Film Transistors," IEEE/OSA J. Display Technology 5, pp.452-461 (2009)

(3) T.-C. Fung, C.-S. Chuang, K. Nomura, H.-P. D. Shieh, H. Hosono, and J. Kanicki, "Photofield-Effect in Amorphous In-Ga-Zn-O (a-IGZO) Thin-Film Transistors," J. Info. Display 9, pp.21-29 (2008)

Conference Proceeding:

(4) T.-C. Fung, K. Abe, H. Kumomi and J. Kanicki, "DC/AC Electrical Instability of R.F. Sputter Amorphous In-Ga-Zn-O TFTs," in SID Int. Symp. Dig. Tech. Papers, 2009, pp.1117-1120

(5) T.-C. Fung, K. Abe, H. Kumomi and J. Kanicki, "Bias-Temperature Stress Study of R.F. Sputter Amorphous In-Ga-Zn-O TFTs," in IDW' 08, AMD7-2 (Niigata, Japan, Oral Presentation)

(6) T.-C. Fung, K. Nomura, H. Hosono, and J. Kanicki, "PLD Amorphous In-Ga-Zn-O TFTs for Future Optoelectronics," in SID Vehicle and Photon '08, pp.5-4 (Dearborn, MI, USA)

(7) T.-C. Fung, C.-S. Chuang, B. G. Mullins, K. Nomura, T. Kamiya, H.-P. D. Shieh, H. Hosono, and J. Kanicki, "Photofield-Effect in Amorphous InGaZnO TFTs," in IMID'08 Digest, 2008, pp.1056 (Seoul, S. Korea, Oral Presentation)

(8) T.-C. Fung, C.-S. Chuang, C. Chen, K. Abe, H. Kumomi and J. Kanicki, "2-D Numerical Simulation of High Performance Amorphous In-Ga-Zn-O TFTs for Flat Panel Displays," in AM-FPD, 2008, pp.251-252. (Tokyo, Japan)

Bibliography

[1] F. Funada, Y. Takafuji, K. Yano, H. Take, and M. Matsuura, "An amorphous-Si TFT addressed 3.2-in. full color LCD," *SID Int. Symp. Digest Tech. Papers*, pp. 293-5, 1986.

[2] R. Zorn and S.-T. Wu, "Liquid crystal displays," in *Nanoelectronics and information technology*, second ed, R. Waser, Ed. Weinheim, Germany: Wiley-VCH, 2005.

[3] D. Hsieh, "Flat-panel display market outlook," DisplaySearch Nov. 2005.

[4] "Macroelectronics" usually refers to microelectronic devices which are distributed yet integrated over large area substrates with sizes much bigger than semiconductor wafers.

[5] A. Kuo, W. Tae Kyung, and J. Kanicki, "Advanced multilayer amorphous silicon thin-film transistor structure: film thickness effect on its electrical performance and contact resistance," *Jpn. J. Appl. Phys. 1*, vol. 47, pp. 3362-7, 2008.

[6] http://www.corning.com/displaytechnologies/en/products/eaglexg/large_gen.aspx

[7] J. Kanicki, F. R. Libsch, J. Griffith, and R. Polastre, "Performance of thin hydrogenated amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 69, pp. 2339-45, 1991.

[8] S. S. Kim, "The World's largest (82-in.) TFT-LCD," *SID Int. Symp. Digest Tech. Papers*, vol. 36, pp. 1842-1847, 2005.

[9] S. S. Kim, B. H. You, J. H. Cho, D. G. Kim, B. H. Berkeley, and N. D. Kim, "An 82-in. ultra-definition 120-Hz LCD TV using new driving scheme and advanced super PVA technology," *J. SID*, vol. 17, pp. 71-78, 2009.

[10] Y. Yoshida, Y. Kikuchi, S. Daly, and M. Sugino, "Invited paper: Image quality improvements in large-screen LC-TV," *SID Int. Symp. Digest Tech. Papers*, vol. 36, pp. 1852-1855, 2005.

[11] J.-H. Lan and J. Kanicki, "Planarized copper gate hydrogenated amorphous-silicon thin-film transistors for AM-LCDs," *IEEE Electron Device Lett.*, vol. 20, pp. 129-31, 1999.

[12] J.-H. Lan and J. Kanicki, "Buried busline a-Si:H TFT structures for AM-LCDs " *Proceedings AM-LCD'98*, pp. 77-81, 1998.

[13] J.-H. Song, H.-L. Ning, W.-G. Lee, S.-Y. Kim, and S.-S. Kim, "Views on the low-resistant bus materials and their process architecture for the larqe-sized post-ultra definition TFT-LCD," *Digest Tech. Papers IMID 2008*, vol. 8, pp. 9-12, 2008.

[14] T. Urabe, "The outstanding potential of OLED displays for TV applications," *Information Display,* vol. 24, pp. 14-17, 2008.

[15] J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim, "A new era of oxide thin-film transistors for large-sized AMOLED displays," *Information Display,* vol. 24, pp. 20-23, 2008.

[16] M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices,* vol. 48, pp. 845-51, 2001.

[17] H. L. Gomes, P. Stallinga, F. Dinelll, M. Murgia, F. Biscarini, D. M. De Leeuw, T. Muck, J. Geurts, L. W. Molenkamp, and V. Wagner, "Bias-induced threshold voltages shifts in thin-film organic transistors," *Appl. Phys. Lett.,* vol. 84, pp. 3184-3186, 2004.

[18] Y.-C. Lin, H. P. D. Shieh, and J. Kanicki, "A novel current-scaling a-Si:H TFTs pixel electrode circuit for AM-OLEDs," *IEEE Trans. Electron Devices,* vol. 52, pp. 1123-31, 2005.

[19] X. D. Wu, R. A. Street, R. Weisfield, S. Nelson, M. Young, M. Nguyen, and P. Nylen, "Imaging with page sized a-Si:H 2-dimensional sensor arrays," *Proc. SPIE - Int. Soc. Opt. Eng.,* vol. 2172, pp. 144-54, 1994.

[20] L. E. Antonuk, Y. El-Mohri, A. Hall, K.-W. Jee, M. Maolinbay, S. C. Nassif, X. Rong, J. H. Siewerdsen, Q. Zhao, and R. L. Weisfield, "A large-area, 97 m pitch, indirect-detection, active matrix, flat-panel imager (AMFPI)," *Proc. SPIE - Int. Soc. Opt. Eng.,* vol. 3336, pp. 2-13, 1998.

[21] R. L. Weisfield, M. A. Hartney, R. A. Street, and R. B. Apte, "New amorphous-Silicon image sensor for x-ray diagnostic medical imaging applications," *Proc. SPIE - Int. Soc. Opt. Eng.,* vol. 3336, pp. 444-452, 1998.

[22] R. L. Weisfield, R. A. Street, R. Apte, and A. Moore, "Improved page-size 127-m-pixel amorphous-silicon image sensor for X-ray diagnostic medical imaging applications," *Proc. SPIE - Int. Soc. Opt. Eng.,* vol. 3032, pp. 14-21, 1997.

[23] K. S. Karim and A. Nathan, "Readout circuit in active pixel sensors in amorphous silicon technology," *IEEE Electron Device Lett.,* vol. 22, pp. 469-71, 2001.

[24] K. S. Karim, A. Nathan, and J. A. Rowlands, "Alternate pixel architectures for large area medical imaging," *Proc. SPIE - Int. Soc. Opt. Eng.,* vol. 4320, pp. 35-46, 2001.

[25] K. S. Karim, G. Sanaie-Fard, T. Ottaviani, M. H. Izadi, and F. Taghibakhsh, "Amplified pixel architectures in amorphous silicon technology for large area digital imaging applications," *J. Korean Phys. Soc. ,* vol. 48, pp. 85-91, 2006.

[26] J. K. Jeong, J. H. Jeong, J. H. Choi, J. S. Im, S. H. Kim, H. W. Yang, K. N. Kang, K. S. Kim, T. K. Ahn, H.-J. Chung, M. Kim, B. S. Gu, J.-S. Park, Y.-G. Mo, H. D. Kim, and H. K. Chung, "Distinguished paper: 12.1-inch WXGA AMOLED display driven by indium-gallium-zinc oxide TFTs array," *SID Int. Symp. Digest Tech. Papers,* pp. 1-4, 2008.

[27] J.-H. Lee, D.-H. Kim, D.-J. Yang, S.-Y. Hong, K.-S. Yoon, P.-S. Hong, C.-O. Jeong, H.-S. Park, S. Y. Kim, S. K. Lim, S. S. Kim, K.-S. Son, T.-S. Kim, J.-Y. Kwon, and S.-Y. Lee, "World's largest (15-inch) XGA AMLCD panel using IGZO oxide TFT,"

SID Int. Symp. Digest Tech. Papers, pp. 625-628, 2008.

[28] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," *IEEE Trans. Electron Devices,* vol. 36, pp. 2868-72, 1989.

[29] J. Jang, "Poly-Si TFTs by non-laser crystallization methods," in *Thin film transistors - Materials and processes, Vol.2: Polycrystalline silicon thin film transistors*, Y. Kuo, Ed. Norwell, MA: Kluwer academic publishers, 2004.

[30] S. Y. Yoon, J. Y. Oh, C. O. Kim, and J. Jang, "Low temperature solid phase crystallization of amorphous silicon at 380C," *J. Appl. Phys.,* vol. 84, pp. 6463-5, 1998.

[31] J. Siddiqui, E. Cagin, D. Chen, and J. D. Phillips, "ZnO thin-film transistors with polycrystalline (Ba,Sr)TiO_3 gate insulators," *Appl. Phys. Lett.,* vol. 88, pp. 212903-1, 2006.

[32] T. Hirao, M. Furuta, H. Furuta, T. Matsuda, T. Hiramatsu, H. Hokari, and M. Yoshida, "Distinguished paper: High mobility top-gate Zinc Oxide Thin-Film Transistors (ZnO-TFTs) for active-matrix liquid crystal displays," *SID Int. Symp. Digest Tech. Papers,* vol. 37, pp. 18-20, 2006.

[33] T.-H. Kim, S.-Y. Kim, J.-H. Jeon, H.-H. Choe, K.-W. Lee, J.-H. Seo, J.-H. Shin, S.-H. K. Park, and C.-S. Hwang, "Electrical stability of ZnO TFT during gate-bias stress," *SID Int. Symp. Digest Tech. Papers,* vol. 39, pp. 1250-1253, 2008.

[34] C. Kim, S. Kim, and C. Lee, "Effects of rf power and substrate temperature during rf magnetron sputtering on crystal quality of ZnO thin films," *Jpn. J. Appl. Phys. 1,* vol. 44, pp. 8501-8503, 2005.

[35] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano, and H. Hosono, "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor in-Ga-Zn-O: experiment and ab initio calculations," *Phys. Rev. B,* vol. 75, pp. 35212-1, 2007.

[36] M. Orita, H. Tanji, M. Mizuno, H. Adachi, and I. Tanaka, "Mechanism of electrical conductivity of transparent InGaZnO4," *Phys. Rev. B,* vol. 61, pp. 1811-16, 2000.

[37] Materials Studio®, Accelrys Software Inc.

[38] M. Orita, H. Ohta, M. Hirano, S. Narushima, and H. Hosono, "Amorphous transparent conductive oxide InGaO3(ZnO)m (m4): a Zn 4s conductor," *Philos. Mag. B,* vol. 81, pp. 501-15, 2001.

[39] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, pp. 488-492, 2004.

[40] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4," *Thin Solid Films,* vol. 486, pp. 38-41, 2005.

[41] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering," *Appl. Phys. Lett.,* vol. 89, pp. 112123-1, 2006.

[42] H. Hosono, "Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application," *J. Non-Cryst. Solids,* vol. 352, pp. 851-858, 2006.

[43] H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples," *J. Non-Cryst. Solids,* vol. 198-200, pp. 165-169, 1996.

[44] H. Hosono, M. Yasukawa, and H. Kawazoe, "Novel oxide amorphous semiconductors: Transparent conducting amorphous oxides," *J. Non-Cryst. Solids,* vol. 203, pp. 334-344, 1996.

[45] P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes, Jr., "Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering," *Appl. Phys. Lett. ,* vol. 82, pp. 1117-19, 2003.

[46] M. J. Powell, B. C. Easton, and D. H. Nicholls, "Annealing and light induced changes in the field effect conductance of amorphous silicon," *J. Appl. Phys.,* vol. 53, pp. 5068-78, 1982.

[47] T.-C. Fung, K. Nomura, H. Hosono, and J. Kanicki, "PLD amorphous In-Ga-Zn-O TFTs for future optoelectronics," *Proc. SID Vehicles and Photons,* p. 5.4, 2008.

[48] R. Hayashi, M. Ofuji, N. Kaji, K. Takahashi, K. Abe, H. Yabuta, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Circuits using uniform TFTs based on amorphous In-Ga-Zn-O," *J. SID,* vol. 15, pp. 915-921, 2007.

[49] M. Ofuji, K. Abe, H. Shimizu, N. Kaji, R. Hayashi, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Fast thin-film transistor circuits based on amorphous oxide semiconductor," *IEEE Electron Device Lett.,* vol. 28, pp. 273-5, 2007.

[50] M. J. Powell and J. W. Orton, "Characteristics of amorphous silicon staggered-electrode thin-film transistors," *Appl. Phys. Lett. ,* vol. 45, pp. 171-3, 1984.

[51] A. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, "Electrical properties of amorphous silicon transistor and MIS-devices: comparative study of top nitride and bottom nitride configurations," *J. Electrochem. Soc.,* vol. 140, pp. 3679-3683, 1993.

[52] C. Chen, T. C. Fung, K. Abe, H. Kumomi, and J. Kanicki, "Study of the density of states of a-InGaZnO using field-effect technique," *66th Annual Device Res. Conf.,* pp. 151-2, 2008.

[53] T.-C. Fung, C.-S. Chuang, K. Nomura, H.-P. D. Shieh, H. Hosono, and J. Kanicki, "Photofield-Effect in Amorphous In-Ga-Zn-O (a-IGZO) Thin-Film Transistors," *J. Information Display (J. Korean Information Display Society),* vol. 9, pp. 21-29, 2008.

[54] C.-S. Chiang, S. Martin, J. Kanicki, Y. Ugai, T. Yukawa, and S. Takeuchi, "Top-gate staggered amorphous silicon thin-film transistors: series resistance and nitride thickness effects," *Jpn. J. Appl. Phys. 1,* vol. 37, pp. 5914-20, 1998.

[55] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.,* vol. 18, pp. 953-9, 1979.

[56] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Lett.* , vol. ED-1, pp. 170-3, 1980.

[57] J. Kanicki and S. Martin, "Hydrogenated Amorphous Silicon Thin-Film Transistors," in *Thin-Film Transistors*, C. R. Kagan and P. Andry, Eds. New York: Marcel Dekker, 2003, pp. 71-137.

[58] C.-Y. Chen and J. Kanicki, "Origin of series resistances in a-Si:H TFTs," *Solid-State Electron.*, vol. 42, pp. 705-13, 1998.

[59] S. Martin, C. S. Chiang, J. Y. Nahm, T. Li, J. Kanicki, and Y. Ugai, "Influence of the amorphous silicon thickness on top gate thin-film transistor electrical performances," *Jpn. J. Appl. Phys. 1*, vol. 40, pp. 530-7, 2001.

[60] T.-C. Fung and J. Kanicki, "TLM analysis on a-IGZO TFT," *Unpublished results*.

[61] R. L. Hoffman, "ZnO-channel thin-film transistors: channel mobility," *J. Appl. Phys.*, vol. 95, pp. 5813-19, 2004.

[62] W. B. Jackson, R. L. Hoffman, and G. S. Herman, "High-performance flexible zinc tin oxide field-effect transistors," *Appl. Phys. Lett.*, vol. 87, pp. 193503-1, 2005.

[63] R. E. Presley, D. Hong, H. Q. Chiang, C. M. Hung, R. L. Hoffman, and J. F. Wager, "Transparent ring oscillator based on indium gallium oxide thin-film transistors," *Solid-State Electron.* , vol. 50, pp. 500-3, 2006.

[64] C. Hyun, M. S. Shur, M. Hack, Z. Yaniv, and V. Cannella, "Above threshold characteristics of amorphous silicon alloy thin-film transistors," *Appl. Phys. Lett.*, vol. 45, pp. 1202-3, 1984.

[65] K. Abe and H. Kumomi, *private communication*, Feb. 2009.

[66] S. Kishida, Y. Naruke, Y. Uchida, and M. Matsumura, "Theoretical analysis of amorphous-silicon field-effect-transistors," *Jpn. J. Appl. Phys. 1*, vol. 22, pp. 511-17, 1983.

[67] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C.-C. Wu, "Modeling of amorphous InGaZnO4 thin film transistors and their subgap density of states," *Appl. Phys. Lett.*, vol. 92, pp. 133503-1, 2008.

[68] T. Sameshima, S. Usui, and M. Sekiya, "XeCl excimer laser annealing used in the fabrication of poly-Si TFTs," *IEEE Electron Device Lett.* , vol. ED-7, pp. 276-8, 1986.

[69] R. A. Street and L. E. Antonuk, "Amorphous silicon arrays develop a medical image," *IEEE Circuits Devices Mag.*, vol. 9, pp. 38-42, 1993.

[70] M. Ito, C. Miyazaki, M. Ishizaki, M. Kon, N. Ikeda, T. Okubo, R. Matsubara, K. Hatta, Y. Ugajin, and N. Sekine, "Application of amorphous oxide TFT to electrophoretic display," *J. Non-Cryst. Solids*, vol. 354, pp. 2777-82, 2008.

[71] T. Li, J. Kanicki, K. Wei, and F. L. Terry, Jr., "Interference fringe-free transmission spectroscopy of amorphous thin films," *J. Appl. Phys.*, vol. 88, pp. 5764-71, 2000.

[72] G. D. Cody, C. R. Wronski, B. Abeles, R. B. Stephens, and B. Brooks, "Optical characterization of amorphous silicon hydride films," *Sol. Cells*, vol. 2, pp. 227-43, 1980.

[73] J. Tauc, *Amorphous and liquid semiconductors*. New York: Plenum Press, 1974.
[74] C.-S. Chuang, T.-C. Fung, B. G. Mullins, K. Nomura, T. Kamiya, H.-P. D. Shieh, H. Hosono, and J. Kanicki, "Photosensitivity of Amorphous IGZO TFTs for Active-Matrix Flat-Panel Displays," *SID Int. Symp. Digest Tech. Papers*, pp. 1215-1218, 2008.
[75] R. A. Street, *Hydrogenated Amorphous Silicon*. Cambridge: Cambridge University Press, 1991.
[76] S. Sherman, S. Wagner, and R. A. Gottscho, "Correlation between the valence- and conduction-band-tail energies in hydrogenated amorphous silicon," *Appl. Phys. Lett.*, vol. 69, pp. 3242-4, 1996.
[77] J. Kakalios and H. Fritzsche, "Persistent photoconductivity in doping-modulated amorphous semiconductors," *Phys. Rev. Lett.*, vol. 53, pp. 1602-5, 1984.
[78] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, "Comparison of ultraviolet photo-field effects between hydrogenated amorphous silicon and amorphous lnGaZnO4 thin-film transistors," *Jap. J. Appl. Phys.* , vol. 48, p. 010203 (3 pp.), 2009.
[79] T.-C. Fung, C.-S. Chuang, B. G. Mullins, K. Nomura, T. Kamiya, H.-P. D. Shieh, H. Hosono, and J. Kanicki, "Photofield-Effect in Amorphous InGaZnO TFTs," *Digest Tech. Papers IMID 2008*, vol. 8, pp. 1208-1211, 2008.
[80] J.-D. Gallezot, S. Martin, and J. Kanicki, "Photosensitivity of a-Si:H TFTs," *Proc. IDRC*, pp. 407-410, 2001.
[81] R. E. I. Schropp, T. Franke, and J. F. Verwey, "The illumination flux dependence of the photofield-effect current in amorphous silicon," *J. Non-Cryst. Solids*, vol. 90, pp. 199-202, 1987.
[82] A. O. Harm, R. E. I. Schropp, and J. F. Verwey, "The photofield effect in a-Si:H thin film MOS transistors. Theory and measurement," *Philos. Mag. B*, vol. 52, pp. 58-70, 1985.
[83] R. E. I. Schropp, A. O. Harm, and J. F. Verwey, "A refined theoretical analysis of photofield-effect measurements in a-Si:H thin-film transistors," *Philos. Mag. B*, vol. 53, pp. 431-44, 1986.
[84] M. C. Hamilton and J. Kanicki, "Organic polymer thin-film transistor photosensors," *IEEE J. Sel. Top. Quantum Electron.* , vol. 10, pp. 840-8, 2004.
[85] W. B. Jackson, R. A. Street, and M. J. Thompson, "Anomalous surface photoconductivity in hydrogenated amorphous silicon," *Solid State Commun.*, vol. 47, pp. 435-8, 1983.
[86] W. B. Jackson and M. J. Thompson, "The effects of band bending on the photoconductivity in a-Si:H," *Physica B C*, vol. 117-118B+C, pp. 883-5, 1983.
[87] C. van Berkel and M. J. Powell, "Photo-field effect in amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 60, pp. 1521-7, 1986.
[88] W. Zimmerman, "Experimental verification of the Shockley-Read-Hall recombination theory in silicon," *Electron. Lett.*, vol. 9, pp. 378-9, 1973.
[89] H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Amorphous oxide channel TFTs," *Thin Solid Films*, vol. 516, pp. 1516-22, 2008.

[90] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *J. J. Appl. Phys., Part 1,* vol. 45, pp. 4303-4308, 2006.

[91] A. Suresh, P. Wellenius, A. Dhawan, and J. Muth, "Room temperature pulsed laser deposited indium gallium zinc oxide channel based transparent thin film transistors," *Appl. Phys. Lett.,* vol. 90, pp. 123512-1, 2007.

[92] K. Jeon, C. Kim, I. Song, J. Park, S. Kim, S. Kim, Y. Park, J.-H. Park, S. Lee, D. M. Kim, and D. H. Kim, "Modeling of amorphous InGaZnO thin-film transistors based on the density of states extracted from the optical response of capacitance-voltage characteristics," *Appl. Phys. Lett.,* vol. 93, pp. 182102-1, 2008.

[93] M. Shur and M. Hack, "Physics of amorphous silicon based alloy field-effect transistors," *J. Appl. Phys.,* vol. 55, pp. 3831-42, 1984.

[94] C.-Y. Chen and J. Kanicki, "Simulation of influence of density of states in a-Si:H on electrical performance of a-Si:H thin-film transistors," in *Proceedings of the International Workshop on Active Matrix Liquid Crystal Displays (AMLCD'95),* 1995, pp. 46-49.

[95] P. Kofstad, *Nonstoichiometry, Diffusion, and Electrical Conductivity in Binary Metal Oxides*. New York: Wiley Interscience, 1972.

[96] T.-C. Fung, C.-S. Chuang, C. Chen, K. Abe, R. Cottle, M. Townsend, H. Kumomi, and J. Kanicki, "Two-dimensional numerical simulation of radio frequency sputter amorphous In-Ga-Zn-O thin-film transistors," *J. Appl. Phys.,* vol. 106, p. 084511 (10 pp.), 2009.

[97] *ATLAS Device Simulation Software User's Manual*. Santa Clara, CA: Silvaco Inc., 2005.

[98] L. Hsu and E. Y. Wang, "Photovoltaic properties of In2O3/semiconductor heterojunction solar cells," in *13th IEEE Photovoltaic Specialists Conference* New York, NY, USA: IEEE, 1978, pp. 536-40.

[99] E. F. Archibong and E. N. Mvula, "Structure and electron detachment energies of Ga2O3- and Ga3O2," *Chem. Phys. Lett.,* vol. 408, pp. 371-6, 2005.

[100] S. Gowtham, M. Deshpande, A. Costales, and R. Pandey, "Structural, energetic, electronic, bonding, and vibrational properties of Ga3O, Ga3O2, Ga3O3, Ga2O3, and GaO3 clusters," *J. Phys. Chem. B,* vol. 109, pp. 14836-14844, 2005.

[101] K. Jacobi, G. Zwicker, and A. Gutmann, "Work function, electron affinity and band bending of zinc oxide surfaces," *Surf. Sci. ,* vol. 141, pp. 109-25, 1984.

[102] H. Kawazoe, H. Yanagi, K. Ueda, and H. Hosono, "Transparent p-type conducting oxides: design and fabrication of p-n heterojunctions," *MRS Bulletin,* vol. 25, pp. 28-36, 2000.

[103] H. Kawazoe, M. Yasukawa, H. Hyodo, M. Kurita, H. Yanagi, and H. Hosono, "P-type electrical conduction in transparent thin films of CuAlO2," *Nature,* vol. 389, pp. 939-42, 1997.

[104] X.-L. Guo, H. Tabata, and T. Kawai, "Pulsed laser reactive deposition of p-type ZnO film enhanced by an electron cyclotron resonance source," *J. Cryst. Growth,* vol. 223, pp. 135-139, 2001.

[105] M. Joseph, H. Tabata, H. Saeki, K. Ueda, and T. Kawai, "Fabrication of the low-resistive p-type ZnO by codoping method," *Physica B*, vol. 302-303, pp. 140-8, 2001.

[106] R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrated Circuits*, 3rd ed. New York: Wiley, 2003.

[107] J. Robertson, "Physics of amorphous conducting oxides," *J. Non-Cryst. Solids*, vol. 354, pp. 2791-5, 2008.

[108] K. Nomura, T. Kamiya, H. Yanagi, E. Ikenaga, Y. Ke, K. Kobayashi, M. Hirano, and H. Hosono, "Subgap states in transparent amorphous oxide semiconductor, In-Ga-Zn-O, observed by bulk sensitive X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 92, pp. 202117-1, 2008.

[109] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: electronic structure, electron transport, defects and doping," *IEEE/OSA J. Disp. Technol.*, vol. 5, pp. 273-88, 2009.

[110] K. Nomura, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Defect passivation and homogenization of amorphous oxide thin-film transistor by wet O2 annealing," *Appl. Phys. Lett.*, vol. 93, pp. 192107-1, 2008.

[111] A. Janotti and C. G. Van De Walle, "Oxygen vacancies in ZnO," *Appl. Phys. Lett.*, vol. 87, p. 122102, 2005.

[112] T. Kamiya, K. Nomura, M. Hirano, and H. Hosono, "Electronic structure of oxygen deficient amorphous oxide semiconductor a-InGaZnO4-x: optical analysis and first-principle calculations," *Phys. Stat. Sol. (c)*, vol. 9, pp. 3098-3100, 2008.

[113] K. Donghun, L. Hyuck, K. Changjung, S. Ihun, J. Park, P. Youngsoo, and C. JaeGwan, "Amorphous gallium indium zinc oxide thin film transistors: sensitive to oxygen molecules," *Appl. Phys. Lett.*, vol. 90, pp. 192101-1, 2007.

[114] J. Jae Kyeong, Y. Hui Won, J. Jong Han, M. Yeon-Gon, and K. Hye Dong, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, pp. 123508-1, 2008.

[115] T. Kamiya, H. Hiramatsu, K. Nomura, and H. Hosono, "Device applications of transparent oxide semiconductors: Excitonic blue LED and transparent flexible TFT," *J. Electroceramics*, vol. 17, pp. 267-275, 2006.

[116] K. Nomura, T. Kamiya, H. Ohta, K. Shimizu, M. Hirano, and H. Hosono, "Relationship between non-localized tail states and carrier transport in amorphous oxide semiconductor, In-Ga-Zn-O," *Phys. Stat. Sol. (a)*, vol. 205, pp. 1910-1914, 2008.

[117] C. J. Kim, D. Kang, I. Song, J. C. Park, H. Lim, S. Kim, E. Lee, R. Chung, J. C. Lee, and Y. Park, "Highly stable Ga2O3-In2O3-ZnO TFT for active-matrix organic light-emitting diode display application," *IEDM'06*, 2006.

[118] J. Y. Kwon, J. S. Jung, K. S. Son, T. S. Kim, M. K. Ryu, K. B. Park, Y. S. Park, S. Y. Lee, and J. M. Kim, "GaInZnO TFT for active matrix display," *proceedings AM-FPD'08*, pp. 287-290, 2008.

[119] M. Fuji, H. Yano, T. Hatayama, Y. Uraoka, T. Fuyuki, J. S. Jung, J. Y. Kwon, T. Nakanishi, and M. Kimura, "Degradation in Ga_2O_3-In_2O_3-ZnO thin film transistors under constant voltage stress," *Proceedings AM-FPD'08*, pp. 295-298, 2008.

[120] T.-C. Fung, K. Abe, H. Kumomi, and J. Kanicki, "Electrical instability of RF sputter amorphous In-Ga-Zn-O thin-film transistors," *IEEE/OSA J. Disp. Technol.*, vol. 5, pp. 452-61, 2009.

[121] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl. Phys. Lett.*, vol. 62, pp. 1286-8, 1993.

[122] M. J. Powell, "Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors," *Appl. Phys. Lett.*, vol. 43, pp. 597-9, 1983.

[123] M. J. Powell, C. van Berkel, I. D. French, and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," *Appl. Phys. Lett.* , vol. 51, pp. 1242-4, 1987.

[124] C. van Berkel and M. J. Powell, "Resolution of amorphous silicon thin-film transistor instability mechanisms using ambipolar transistors," *Appl. Phys. Lett.*, vol. 51, pp. 1094-6, 1987.

[125] M. Stutzmann, "The defect density in amorphous silicon," *Philos. Mag. B*, vol. 60, pp. 531-46, 1989.

[126] C. S. Chiang, J. Kanicki, and K. Takechi, "Electrical instability of hydrogenated amorphous silicon thin-film transistors for active-matrix liquid-crystal displays," *Jpn. J. Appl. Phys. 1*, vol. 37, pp. 4704-10, 1998.

[127] K. S. Karim, *Ph.D thesis: Pixel architectures for digital imaging using amorphous silicon technology*. Waterloo, Ontario, Canada: University of Waterloo, 2002.

[128] J. N. Boudry and L. E. Antonuk, "Current-noise-power spectra of amorphous silicon thin-film transistors," *J. Appl. Phys.* , vol. 76, pp. 2529-34, 1994.

[129] J. B. Johnson, "Thermal agitation of electricity in conductors," *Nature*, vol. 119, pp. 50-51, 1927.

[130] J. B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.*, vol. 29, pp. 367-368, 1927.

[131] J. B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.*, vol. 32, pp. 97-109, 1928.

[132] H. Nyquist, "Thermal agitation of electric charge in conductors," *Phys. Rev.*, vol. 32, pp. 110-113, 1928.

[133] M. J. Buckingham, *Noise in electronic devices and systems*. New York: John Wiley and Sons, 1983.

[134] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*, 4th ed. New York: John Wiley and Sons, 2001.

[135] A. van der Ziel, "Chapter 5: Thermal noise," in *Noise in solid state devices and circuits* New York: John Wiley and Sons, 1986.

[136] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 654-65, 1990.

[137] S. Rumyantsev, C. Young, G. Bersuker, and M. Shur, "Low frequency noise in high-k dielectric MOSFETs. How far from the channel are we probing the traps?," *20th Int. Conf. Noise and Fluctuations*, vol. CP1129, pp. 255-8, 2009.

[138] L. K. J. Vandamme and F. N. Hooge, "What do we certainly know about 1/f noise in MOSTs?," *IEEE Trans. Electron Devices,* vol. 55, pp. 3070-85, 2008.
[139] L. K. J. Vandamme, L. Xiaosong, and D. Rigaud, "1/f noise in MOS devices, mobility or number fluctuations?," *IEEE Trans. Electron Devices,* vol. 41, pp. 1936-45, 1994.
[140] A. L. McWhorter, "1/f Noise and germanium surface properties," in *Semiconductor surface physics*, R. H. Kingston, Ed.: Univ. of Pennsylvania Press, 1957, pp. 207-228.
[141] S. Christensson, I. Lundstrom, and C. Svensson, "Low frequency noise in MOS transistors -- 1, 2," *Solid-State Electron.,* vol. 11, pp. 797-802, 1968.
[142] D. Rigaud, M. Valenza, and J. Rhayem, "Low frequency noise in thin film transistors," *IEE Proc.-Circuits Devices Syst.,* vol. 149, pp. 75-82, 2002.
[143] C. G. Jakobson, I. Bloom, and Y. Nemirovsky, "1/f noise in CMOS transistors for analog applications," *Proc. IEEE Convention of Electrical Electronics Engineers in Israel*, pp. 557-560, 1996.
[144] Y. Nemirovsky, I. Brouk, and C. G. Jakobson, "1/f noise in CMOS transistors for analog applications," *IEEE Trans. Electron Devices,* vol. 48, pp. 921-927, 2001.
[145] F. N. Hooge, "1/f noise is no surface effect," *Phys. Lett.,* vol. 29A, pp. 139-140, 1969.
[146] F. N. Hooge and L. K. J. Vandamme, "Lattice scattering causes 1/f noise," *Phys. Lett.,* vol. 66A, pp. 315-316, 1978.
[147] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices,* vol. 41, pp. 1926-1935, 1994.
[148] J. Rhayem, D. Rigaud, M. Valenza, N. Szydlo, and H. Lebrun, "1/f noise modeling in long channel amorphous silicon thin film transistors," *J. Appl. Phys.,* vol. 87, pp. 1983-1989, 2000.
[149] P. V. Necliudov, S. L. Rumyantsev, M. S. Shur, D. J. Gundlach, and T. N. Jackson, "1/f noise in pentacene organic thin film transistors," *J. Appl. Phys.,* vol. 88, pp. 5395-5395, 2000.
[150] J. Rhayem, D. Rigaud, M. Valenza, N. Szydlo, and H. Lebrun, "1/f noise in amorphous silicon thin film transistors: effect of scaling down," *Solid-State Electron.,* vol. 43, pp. 713-721, 1999.
[151] F. M. Klaassen, "Characterization of low l/f noise in MOS transistors," *IEEE Trans. Electron Devices,* vol. ED-18, pp. 887-891, 1971.
[152] L. K. J. Vandamme, "Model for 1/f noise in MOS transistors biased in the linear region," *Solid-State Electron.,* vol. 23, pp. 317-323, 1980.
[153] *9812B noise analyzer user's manual*: ProPlus Design Solutions, Inc., 2008.
[154] *NoisePro™ for Windows™ user's manual*: ProPlus Design Solution Inc., 2008.
[155] *Application note: Configurations of 9812B noise analyzer*: ProPlus Design Solution, Inc., 2008.
[156] H. Lee, J.-S. Yoo, C.-D. Kim, I.-B. Kang, and J. Kanicki, "Hexagonal a-Si:H TFTs: a new advanced technology for flat-panel displays," *IEEE Trans. Electron Devices,* vol. 55, pp. 329-36, 2008.

[157] H. Lee, J.-S. Yoo, C.-D. Kim, I.-J. Chung, and J. Kanicki, "Asymmetric electrical properties of Corbino a-Si:H TFT and concepts of its application to flat panel displays," *IEEE Trans. Electron Devices*, vol. 54, pp. 654-62, 2007.