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# Title: COLD-CATHODE ELECTRON FIELD EMISSION OF BORON NITRIDE THIN FILM WITH A MEMS-BASED GATE FOR SPACE APPLICATIONS

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Abstract: Cold-cathode electron field emission is a technology emerging as an appealing alternative to high power thermionic emitters and gas plasma contactors that use a consumable (Xe gas, typically) for space electrodynamic tether systems and other space electric propulsion systems requiring low-power neutralizers. Example cold-cathode electron field emission technologies include Spindt-type cathodes and gated carbon nanotubes, both of which emit electrons through quantum mechanical tunneling of electrons, instigated by a high electric field applied at the emitter surface. Research at the University of Michigan indicates that nanostructured Boron Nitride (BN) is an attractive material for cold-cathode electron emission due to its low work function, structural robustness, chemical inertness (Spindt-type cathodes with Mo tips are known to degrade in an oxygen environment), and favorable emission characteristics.

To facilitate the acceleration of electrons away from the emission surface and toward the plasma anode (beyond the space charge limit), a MEMS-based gated structure has been developed in order to provide the high surface electric fields required for electron emission at the BN surface. This paper will describe the integrated device development for a gated-BN emitter to be used in the student-designed Field Emission Get-Away-Special Investigation (FEGI) project- a test platform for low-earth demonstration of various cold-cathode electron field emitter designs.

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# COLD-CATHODE ELECTRON FIELD EMISSION OF BORON NITRIDE THIN FILM WITH A MEMS-BASED GATE FOR SPACE APPLICATIONS

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**Cold-cathode electron field emission is a technology emerging as an appealing alternative to high power thermionic emitters and gas plasma contactors that use a consumable (Xe gas, typically) for space electrodynamic tether systems and other space electric propulsion systems requiring low-power neutralizers. Example cold-cathode electron field emission technologies include Spindt-type cathodes and gated carbon nanotubes, both of which emit electrons through quantum mechanical tunneling of electrons, instigated by a high electric field applied at the emitter surface. Research at the University of Michigan indicates that nanostructured Boron Nitride (BN) is an attractive material for cold-cathode electron emission due to its low work function, structural robustness, chemical inertness (Spindt-type cathodes with Mo tips are known to degrade in an oxygen environment), and favorable emission characteristics.**

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## Nomenclature

| | | | | | |
|---|---|---|---|---|---|
| BN | = | Boron Nitride | FEGI | = | Field Emission Get-Away-Special Investigation |
| CNT | = | Carbon Nanotube | MEMS | = | Microelectromechanical Systems |
| DWP | = | Dissolved Wafer Process | ONO | = | Oxide-Nitride-Oxide |
| SEM | = | Scanning Electron Microscope | | | |

## I. Introduction

CHARGE control can be a problem that can affect all systems in space. Differential charging of spacecraft surfaces or bulk charging of a spacecraft can damage on-board electronics and degrade sensor measurement and functionality. In order to prevent charge buildup, a simple method to emit charge from the spacecraft must be provided. For applications requiting low power electron emission, field emitters are ideal. In addition, neutralization

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systems are integral to many space propulsion systems including electrodynamic (ED) tethers and electric propulsion thrusters. Both need low-power electron neutralizers capable of elecctron emission from minimal area that will not degrade in a space plasma and spacecraft environment.

Present electron emission technologies include thermionic emitters or plasma contactors. Thermionic emitters require high power to thermally extract electrons from the surface. Plasma contactors require a consumable gas source to emit charge from the spacecraft as well as energy for a heater. Cold-cathode electron field emission requires less power and does not require a consumable, and is thus an appealing alternative. Examples of this technology include Spindt-type cathodes with gated micron scale molybdenum tips, and gated carbon nanotube (CNT) cathodes. In these cold-cathode emitters, emission is effected via quantum mechanical tunneling of electrons, instigated by a bias voltage applied between a nearby gate and the emitting surface, generating a strong electric field at the emitter surface. Field strengths are enhanced via the geometry of the emitting surface, allowing lower overall gate-to-surface voltages. The need for such fine structures, however, increases the environmental susceptibility of most cold cathode technologies. Spindt-type cathodes with Mo tips are known to degrade in an oxygen environment.

An alternative emitting surface, nanostructured thin film Boron Nitride (BN), has been identified as a potentially robust and chemically inert material with a low work function capable of sustaining electron emission in a space plasma environment. In order to enhance the electric field strengths with a reasonably low bias potential, a gated structure has been developed. Using MEMS fabrication methods, a conducting grid with dielectric spacer will be made to extract and accelerate electrons away from the emission surface. The gate/dielectric structure allows for "tip-less" emission from an otherwise flat, but nanostructured surface. This potentially allows for the BN emission surface to be fabricated independently of the gate structure on a different substrate.

## II. Thin Film Emission Surfaces

A gated structure has been developed to enhance electric fields over a thin film emission surface. Minor modifications to the existing gate can allow for integration with almost any planar emission surface with surface roughness less than 100Å. The initial gate design was developed around the properties of BN emitters, because research at the University of Michigan shows thin film Boron Nitride (BN) to be a favorable emission surface. However, integration with other effective emission surfaces like carbon nanotube (CNT) films is possible. Plans are in place to conduct integrated device field emission tests in a vacuum chamber later this summer with both BN and CNT thin films integrated with the gated structure.

### A. Boron Nitride

Thin films of polycrystalline Boron Nitride (BN) have been synthesized using the reduced-bias ion-assisted sputtering technique[1]. These large bandgap films have shown desireable field emission characteristics; due to the chemical inertness and high mechanical stability of the BN films, they are also anticipated to resist contamination and atomic oxygen disruption. In experiments using an anode placed ~25 µm from the BN surface, preliminary data suggest a low emission threshold of ~2.75 V/µm, with a current of ~10 µA at ~3.5V/µm.[2] Although average current densities measured to date have been below those of other field emission technologies such as Spindt-type cathodes and carbon nanotubes, the purported resilience of the BN emitting surface makes it highly favorable for space-based applications.

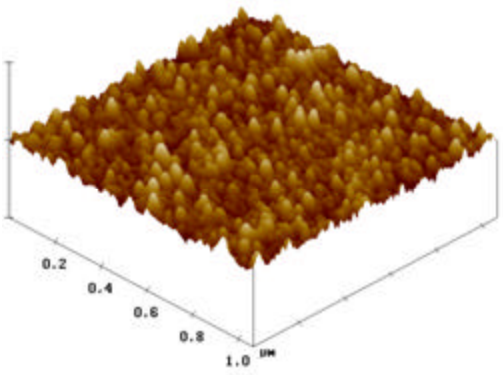


**Figure 1. Boron Nitride surface.** *AFM image of cubic boron nitride surface on Si(100) substrate.*

Initial results indicate that these nanostructured BN surfaces exhibit robust emission characteristics in the presence of residual gases such as oxygen, xenon, water vapor, and nitrogen - gases of relevance to space propulsion applications. For example, at an oxygen partial pressure of $10^{-6}$ torr, emission thresholds in the range of 1 to 4 V/µ have been reproducibly observed.[3] In addition, no permanent effect on the emission characteristics was observed from the exposure of the films to the gas. In all cases, the BN surface was shown to successfully sustain emission for testing periods on the order of 10 to 15 hours, with relatively

constant emission current levels and only moderate drift relative to pre-exposure levels, demonstrating the toughness of this emitter in environments of interest for space systems.

### B. Carbon Nanotubes

Carbon Nanotubes (CNT) are excellent candidate field emitting materials, and are a current hot topic of research. CNT emitters have shown sustainable current densities up to 1A/cm$^2$ at electric fields under 8V/μm.[4]

Current CNT cathode devices suspend a planar grid structure over a film of randomly oriented CNT segments. If the present MEMS gate structure were to be used instead, it could allow better control over the separation of the gate to the emitting surface as well as provide an intervening dielectric to minimize gate leakage. This would increase emitter efficiency and lower power consumption.

## III. Gate Design and Fabrication

### A. Gate Design

The first iteration of the gate design was tailored for use over a Boron Nitride surface. The gate is simply a poly-silicon conductive layer placed over a dielectric spacer with holes arrayed throughout. The dielectric is made very thin (1-2μm) to place the conductor as close to the emitting surface as possible to concentrate electric field lines and increase emission efficiency. A 1:1 ratio of the hole diameter to dielectric spacing produces more uniform field lines and therefore achieves higher emission efficiency. Due to the varying parameters of dielectric growth in the furnace, samples were designed to have hole diameters between 1-2μm, therefore targeting a dielectric thickness between 1-2μm. The holes were arrayed with spacing ranging from 5-10μm for the center-to-center distance. Higher densities of holes allow more emission area over a given sample. However, the addition of holes can weaken the delicate membrane that is clamped on the emitting surface.

A gate sample was designed to be 1cm$^2$ to correspond to the approximate size of a BN sample currently being tested at the University of Michigan. Each sample contains 11 opening windows filled with arrays of holes for emission. There is an additional window that does not contain any holes that is used to make contact to the gate conductor. The pattern of the twelve openings was designed in a "H" shape to allow for room for Vespel™ dielectric wedges to clamp the gate over the BN surface.

### B. Device Fabrication

The gate structure is fabricated using a two-mask process, as shown in Figure 2. The gate is released in a dissolved wafer process (DWP), and is therefore created upside-down in fabrication. The individual fabrication steps are well characterized from semiconductor fabrication; however there are a number of fabrication challenges due to small feature sizes and delicate structures on the devices themselves.

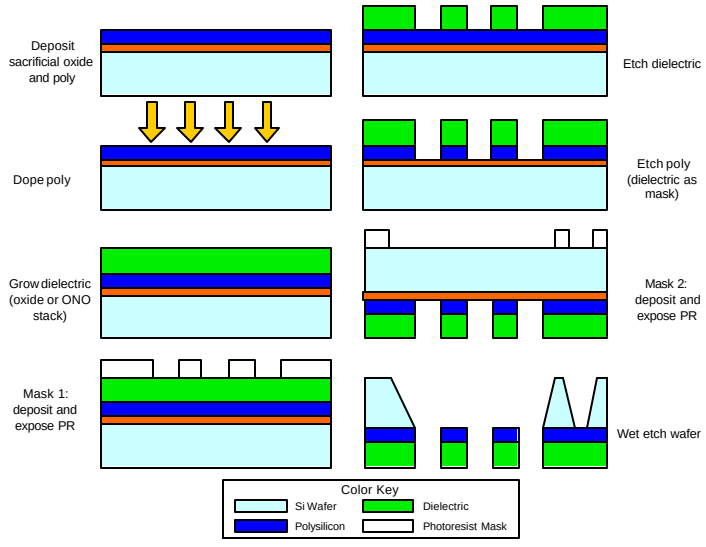


**Figure 2. Gate fabrication sequence.** *Showing each step of the DWP fabrication process.*

The first step in the process is a series of furnace runs to create the appropriate layering for the conductors and dielectrics. First, a sacrificial oxide is grown which acts as the etch stop in the dissolved wafer process. This 6000Å oxide acts as a buffer to absorb some boron atoms during the doping of the polysilicon conductor. Over the oxide, a 2000Å layer of polysilicon is grown and doped with Boron to a very high concentration (targeted >$10^{20}$ cm$^{-3}$). The polysilicon is the conducting layer that is biased relative to the emission surface. It is grown thick enough to ensure a uniform deposition across the wafer. However it is thin enough to not interfere with the desired 1:1 hole diameter to hole spacing ratio. On top of the conducting polysilicon, a dielectric triple

stack of oxide-nitride-oxide (ONO) is grown to electrically isolate the conducting grid and the emission surface. The ONO stack is used because the emission area openings act as a large diaphragm. Oxide and nitride have thermal coefficients above and below that of silicon. The alternating ONO layers help to cancel the thermal stresses in the diaphragm after the bulk silicon is removed in the DWP process. Both the oxide and nitride have dielectric coefficients above $10^7$ V/cm allowing a maximum of ~1000V to be applied between the gate and emitting surface assuming a gap spacing of 1µm. Since the holes are designed to be between 1-2µm in diameter, the targeted thickness for the ONO stack is 1-2µm. Furnace run parameters were computed to produce a 4000/2000/4000Å thick stack.

After all of the layers are grown in the furnaces, the lithography process is initiated. The first mask is used to create small pinholes with diameters from 1-2µm and spaced from 5-10µm apart. The process uses contact lithography to pattern the holes, pushing the lower limit of feature sizes for contact lithography. The holes are etched using a highly anisotropic Reactive Ion Etch (RIE) to produce straight sidewalls. Once the RIE has etched through the dielectric and conducting polysilicon layers, lithography is performed on the backside of the wafer to create the open areas exposing the holes. A second RIE etches through the hole openings, exposing the bulk silicon in preparation for the DWP process. The bulk silicon is then dissolved in a wet-etch EDP solution to expose the hole openings and contact area. The sacrificial oxide grown in the first step acts as an etch stop for the EDP. The sacrificial oxide is etched away leaving the completed sample with twelve square diaphragms, one for the electrical contact pad and eleven for the arrays of pinholes for emission.

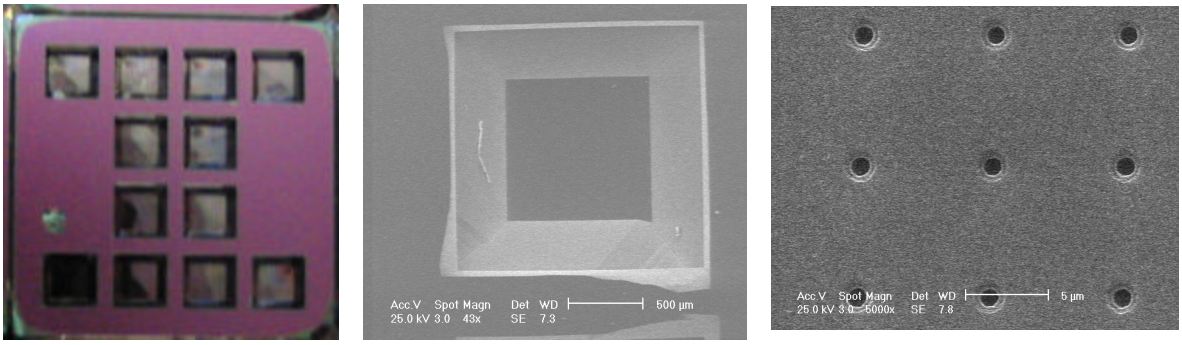


**Figure 3. Fabricated gate samples.** *(L-to-R) A single gate sample showing the "H" pattern (the contact pad is the lower left square). Pictures from the SEM show one of the emission hole openings as well as the array of micron-sized holes etched in the ONO dielectric.*

Once fabrication is complete, the twelve holes are very delicate since they are only 1-2µm thick over an area of $1mm^2$. Scribe lines are designed into the mask to allow for easy dicing of the fabricated wafer into $1cm^2$ samples. Random samples are inspected with an SEM to ensure that the fabrication of the holes was successful and that the samples are ready for integration with the emission surface for testing.

### C. Device Integration

The gated structure is clamped to the emitting surface using a mechanical clamp made of Vespel™ dielectric wedges. The BN emitting surface and gated structure are placed on a glass holder and in turn clamped with another Vespel™ dielectric wedge. Thin films of CNT deposited onto a silicon substrate can be integrated in a similar way with a re-designed gated structure and Vespel clamps. This integration method requires no outgassing epoxies and is ideal for ultra-high vacuum applications.

### D. Device Testing

For chamber testing, an anode is placed a few centimeters away from the integrated emitting surface and gated structure. Ammeters on the emitting film, gate, and anode measure emission current, gate leakage and anode collection, to determine the efficiency of the device. High voltage is applied to the gate structures with an external power supply. The performance of the integrated gate and emitter device will be compared with emitter-only testing ongoing at the University of Michigan. Current BN emission testing is performed by placing the BN sample over an anode separated with 25µm glass fiber spacers. The assembly is clamped using a UHV Vespel™ dielectric wedge.

The addition of the gate allows the gap to the conductor to be much lower, concentrating the field lines and allowing them to be much more uniform across the emission surface. The addition of the gate not only will improve emission performance, but is also necessary for the use of the integrated devices for space applications where the space plasma acts as the anode to the charge-loop of the emission system. The gate will accelerate electrons from the emitting surface past the space charge limit and into the local plasma.[5]

## IV. Field Emission Get-Away-Special Investigation (FEGI)

The FEGI experiment is being developed at the University of Michigan under the student-run Student Space Systems Fabrication Lab (S3FL). The experiment is designed to fly on the Space Shuttle as a Get Away Special payload, and will serve as a testbed for cold-cathode field emitters used in low earth orbit. One of the many field emitters flown on FEGI will be a gated Boron Nitride field emitter. The FEGI experiment requires flown field emitters to conform to the form factor of a standard TO-5 transistor header. In support of this project, a gate structure has been designed to follow this TO-5 header interface protocol, and contains one single emission window and four smaller areas for the gate contact.

Emitters on the FEGI experiment are mounted within vacuum enclosures that are sealed in a controlled environment and opened only during the active mission lifetime. The doors of the enclosures are sealed again after the duration of the experiment, allowing contamination analysis to be performed. Chemical analysis will reveal the contaminates exposed to the emitters on-orbit and how those contaminates may effect emission. The FEGI experiment faceplate is also equipped with environmental monitoring instruments to see how varying plasma parameters affect emission performance. These instruments include a Langmuir probe, electrostatic analyzer, pressure sensor, and current collection surfaces.

Emission data from the FEGI experiment will be a tremendous milestone towards the development of field emission devices robust enough to withstand the harsh space plasma environment.

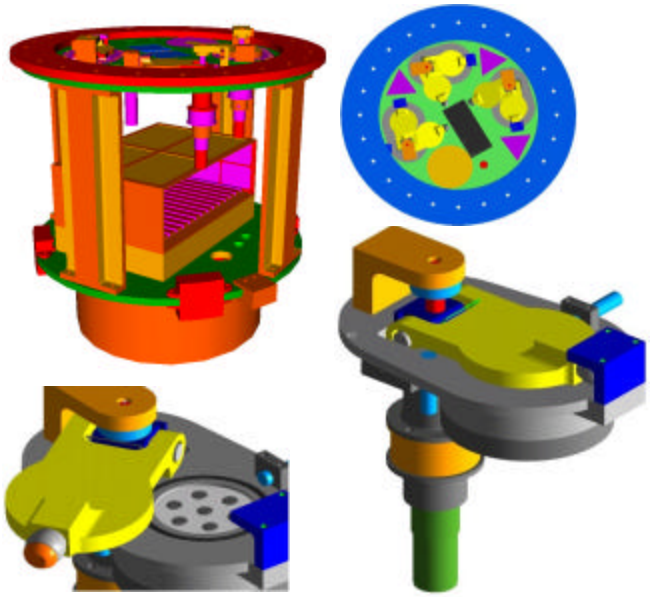

**Figure 4. FEGI Experiment.** *BN gated emitters will be placed inside vacuum enclosures (bottom) and placed on the experiment faceplate (top right) to validate emission in a space plasma.*

## V. Future development

The next stage of development is the integration of the gate with a BN emitting surface. Emission tests will be performed in a high vacuum chamber to see how the gate improves emission efficiency. Further iterations of the gate design may be necessary to further characterize fabrication parameters to produce gates with better dielectric thicknesses, hole diameters, and hole densities for emission area. In addition to testing with BN samples, the gate can be added to additional planar thin film emission surfaces including CNT and similar.

One possible future development is the addition of a second gate to be added over the first. The second gate at a different bias potential allows for the focusing of electrons Simulations show that increasing the initial bias on the first (lower) gate causes a larger deacceleration potential at the second gate, therefore focusing the electron beam without consuming extra energy. The MEMS fabrication techniques used could allow for a second gate to be added in a self-aligned manner with only a few additional processing steps.

## VI. Conclusion

A new gated structure has been developed to assist and improve cold cathode electron emission from a variety of thin film surfaces. With this gated structure, integrated devices of Boron Nitride, carbon nanotube, and other thin emitting films will be made with higher system efficiency and lower turn-on voltage than previous designs. Initial testing will be performed in the laboratory with BN and compared with previous results. The upcoming FEGI Shuttle mission at the University of Michigan will provide a test bed for this new structure mounted over BN (along with other cold cathode emitters). In addition, this gate is compatible with almost any planar thin film emission surface, and the gate's design can be optimized for many of these films.

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