Amorphous In-Ga-Zn-O Thin Film Transistors for Active-Matrix Organic Light-Emitting Displays

by

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CHAPTER I

Introduction

1.1 Transparent Electronics

It only takes a moment to envision the wonderful possibilities transparent electronics have to offer. Window panels could smartly adjust the shade in response to the change in environmental light, while simultaneously converting solar energy into electricity for household needs. Automobile windshields could transmit visual information - speed, navigation directions and alerts – directly in the driver's viewing field. Computers could be embedded into glass table tops, and shop windows could double as billboards.

Things that only exist in science fictions may soon become a reality (Fig. 1.1). The first wave in transparent electronics is the utilization of transparent electrodes. Materials such as indium tin oxide (ITO) already plays an important role in liquid crystal displays (LCDs), touch panels, organic light emitting diodes (OLEDs), and solar cells. Recently, rapid progress in the development of transparent thin film transistors (TFTs) marks the beginning of the second wave. Transparent TFTs based on oxide semiconductors, in addition to being transparent, have high mobilities and low processing temperatures, making them very competitive to existing organic/inorganic TFTs, even in

applications that don't immediately require transparency. They're expected to bring improvements in nowadays displays such as active-matrix liquid crystal displays (AMLCDs), active-matrix organic light emitting displays (AMOLEDs), and electronic papers (E-papers), including larger sizes, higher resolutions, and simpler manufacturing. The long term goal of transparent TFTs, however, is to utilize both the good electrical performance and visible transparency, and create new products which conventional technology cannot achieve.

The third wave in transparent electronics is believed to be approaching soon through the development of transparent high performance p-type oxide semiconductors. By combining n and p-type oxide semiconductors, a variety of transparent active devices can be achieved, including transparent solar cells that can be embedded into window panes, and cheaper blue, white, or even ultraviolet light emitting diodes (LEDs) that can compete with GaN based LEDs. The p-type and n-type TFTs will allow the fabrication of transparent complementary metal-oxide semiconductor (CMOS) integrated circuits (ICs). Ultimately, transparent electronics will not only be restricted to transparent components, and fully transparent products will finally appear.

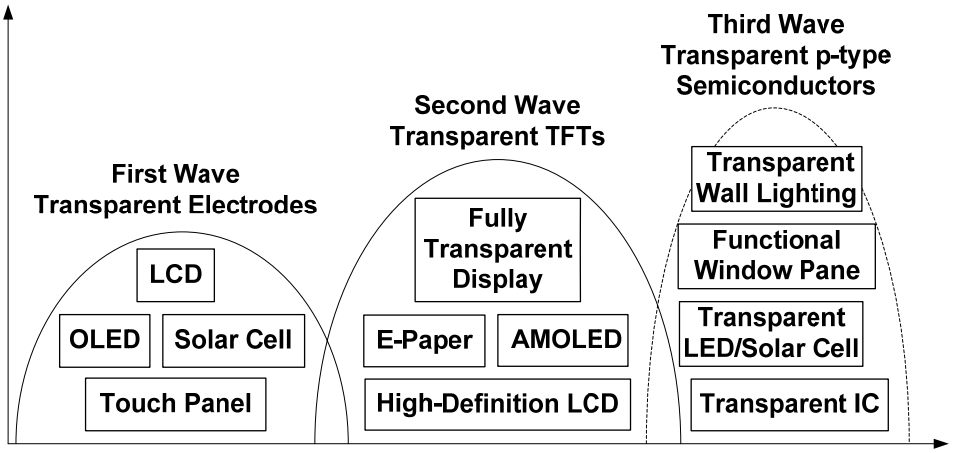

Figure 1.1 Developments in transparent electronics, the past, today, and the future. (Adopted from Nikkei Electronics Asia, November 2007, Cover Story)

1.2 Amorphous Oxide Semiconductor Thin Film Transistors

` Transparent oxide semiconductors that are attracting the most interest can be broadly divided into two categories: polycrystalline oxide semiconductors (POS) such as ZnO [1-6], and amorphous oxide semiconductors (AOS) including In-Zn-O [7-11], In-Sn-O [12], Zn-Sn-O [13-15], Zn-In-Sn-O [16, 17], and In-Ga-Zn-O (a-IGZO) [18-21]. These materials have large bandgaps and wide controllability of carrier concentrations, which make them very promising for transparent thin-film transistor (TFT) applications. POS TFTs show high field-effect mobilities comparable to low temperature polysilicon (LTPS) TFTs, but the polycrystalline structure exhibits grain boundaries that can deteriorate the reproducibility and uniformity of the device characteristics [22]. On the other hand, AOS TFTs have good uniformity and reasonably high field-effect mobilities even when deposited at room temperature on plastic substrates [18], and are preferred over POS TFTs for applications that require large area deposition at low temperature. Figure 1.2 summarizes the advantages and possible applications of AOS TFTs.

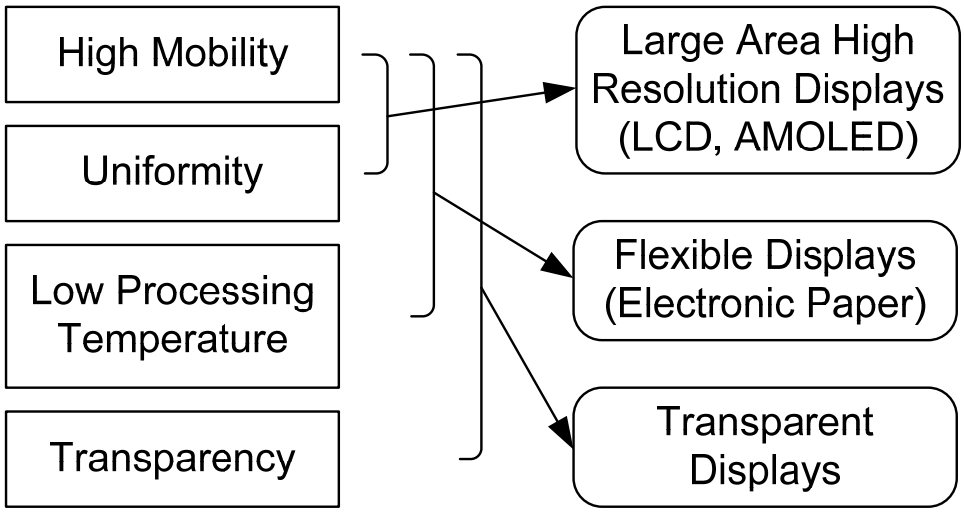

Figure 1.2 Besides transparency, amorphous AOS TFTs have additional useful characteristics to compete with existing technologies.

Among all AOS TFTs, a-IGZO TFTs have been most widely and intensively investigated. The devices typically have field-effect mobilities (μ_{FE}) in the range of 2~20cm^2/V-s, low off-currents 10^{-13}A, and sharp subthreshold swings (S). They're highly transparent, and can be deposited uniformly over large area by conventional sputtering methods. Several prototype displays based on a-IGZO TFTs have already been demonstrated, indicating a very promising future for these devices. Ito et al. reported a 4 inch QVGA E Ink display with 4 gray scales [23]. The a-IGZO pixel TFTs were fabricated by sputtering at room temperature, and exhibit field-effect mobilities ~2.6 cm^2/V-s, with current on-off (I_{ON-OFF}) ratios ~10^5. Son et al. demonstrated a 15 inch XGA AMLCD with a-IGZO TFTs having μ_{FE} ~4.2cm^2/V-s and S ~ 1V/dec. [24]. Jeong et al. demonstrated a full color 12.1 inch WXGA AMOLED [25]. A simple 2 transistors and 1 capacitor pixel circuit was used, and no nonuniformity in luminance was observed. The a-IGZO pixel TFTs showed great uniformity and good electrical performance (μ_{FE} = 17cm^2/V-s, S=0.22V/dec, I_{ON-OFF} ratio = 10^9).

1.3 Carrier Transport in Amorphous Oxide Semiconductors

The conduction mechanism in amorphous oxide semiconductors (AOS) is very different from that in conventional semiconductors. In AOS, the atomic bondings are ionic, and the conduction band minimum (CBM) is composed of vacant s-orbitals of metal cations. Hosono et al. predicted that for an AOS to have a large mobility comparable to its crystalline phase, it must consist heavy post transition metal (HPTM) cations with an electronic configuration $(n-1)d^{10}ns^0$, where $n \geqq 5$ [26]. The spatial spreads of the vacant s-orbitals of these HPTM cations are so large that they overlap with each

other, creating a continuous carrier conduction path. Since the s-orbitals are isotropic in shape, the magnitude of the overlap is insensitive to the bond angles, which is the origin of having high mobility even in amorphous phase. Figure 1.3 (a) illustrates the orbital drawing of the CBM of oxide semiconductors in both crystalline and amorphous phases. It can be easily seen from the figure that the electron path is not highly affected by the bond angles.

On the other hand, in conventional covalent semiconductors, such as silicon, the CBM is composed of sp^3 orbitals with strong spatial directivity. Therefore, the magnitude of the overlap between vacant orbitals of neighboring atoms is very sensitive to variation in the bond angles, which is why amorphous silicon has a much lower mobility, compare to that of crystalline silicon. Fig. 1.3 (b) illustrates the orbital drawing of the CBM of Si in crystalline and amorphous phases.

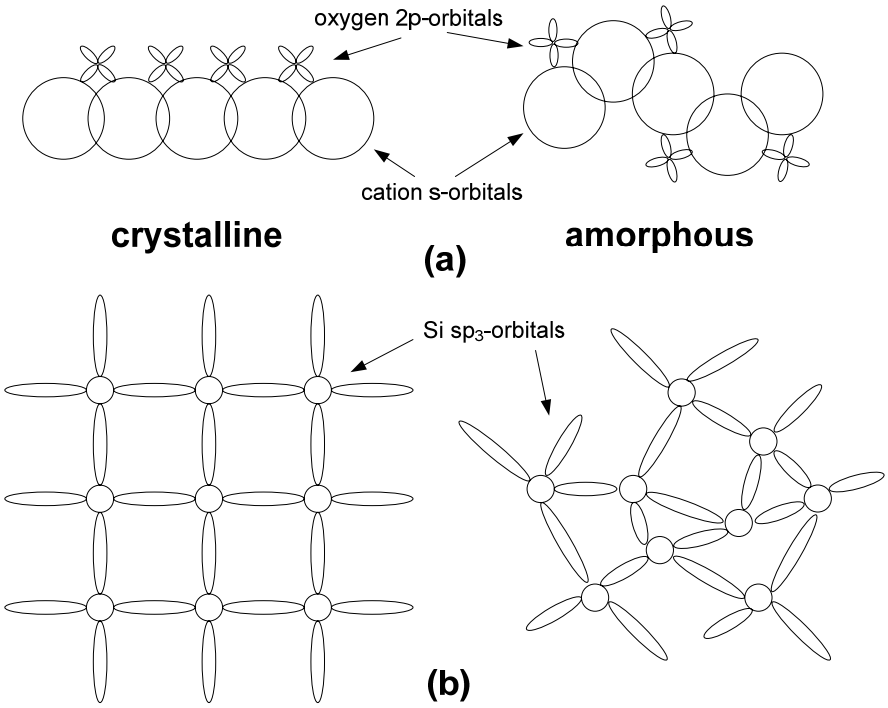

Figure 1.3 Schematic orbital drawing of the conduction band bottom (CBM) in (a) oxide semiconductors and (b) Si in crystalline phase and amorphous phase.

1.4 Thin Film Transistors for Active-Matrix Organic Light-Emitting Displays

Active-matrix organic light-emitting display (AMOLED) is now generally viewed as the ultimate next generation display because of its vivid color, high contrast ratio, fast response time, thin/light module, and low energy consumption [27, 28]. In this section, we focus on the current status and critical issues of the TFT backplane, which is one of the most crucial technologies for the success of AMOLEDs.

Amorphous silicon (a-Si) TFTs currently dominate the liquid crystal display (LCD) market due to their uniformity over large area, low cost of fabrication, and mature technology. However, the small field-effect mobility (~1cm^2/V-s) is insufficient to drive large-size high resolution AMOLEDs. Moreover, a-Si TFTs exhibit metastable shift in threshold voltage (V_T) when subject to prolonged gate bias [29, 30]. While this might not cause a problem in switching LCDs, in AMOLEDs, the OLED brightness is directly controlled by the TFT current, and the shift in V_T overtime causes a variation in display brightness and shortens the display lifetime. In consequence, complex pixel circuits with compensation ability are needed to realize acceptable a-Si TFT AMOLEDs, which greatly limits the display resolution [31, 32].

On the other hand, low temperature polysilicon (LTPS) TFTs have high field-effect mobilities (~100cm^2/V-s), good electrical stability, and provide both n- and p-type devices, which allow the integration of the driver circuit on the same glass substrate with the active matrix display. However, LTPS TFTs are mostly formed by crystallizing a-Si using solid phase crystallization [33] or excimer laser annealing [34], which increases the cost of fabrication and are restricted to smaller format applications. LTPS TFTs also suffer from the variation in device characteristics caused by the existence of grain

boundaries and require complex compensation pixel circuits to realize uniform AMOLEDs [35, 36].

Finally, AOS TFTs combine the advantages of a-Si and LTPS TFTs, and might be an alternative approach to realize reliable, high resolution AMOLEDs. They have reasonably high mobilities (2~40cm^2/V-s) and are uniform in device characteristics when deposited over large area at room temperature [7-21, 25, 37]. Simple 2Tr + 1Cap pixel circuits have been used without the observance of nonuniformity in luminance [25, 38]. The active layer can be fabricated by sputtering, and large-size fabrication can be easily implemented. The process is essentially the same as that for a-Si TFTs, so existing production lines can be used without significant changes. The long term reliability of AOS TFTs is still under investigation; however, it is believed that highly stable devices can be achieved after the optimization of the dielectric layer [39, 40], encapsulation layer [41], and active layer chemical composition [14]. The comparison among a-Si, LTPS, and AOS TFT technologies are summarized in Table 1.1.

Table 1.1 Comparisons between a-Si, LTPS, and AOS TFT technologies

TFT semiconductor material	**a-Si**	**LTPS**	**AOS**
Visible Transparency	poor	poor	good
Field-effect Mobility (cm^2/V-s)	~1	~100	2~40
Motherglass Generation Size (mm x mm)	Gen 8 (2160 x 2460)	Gen 4 (730 x 920)	Gen 8 (2160 x 2460)
TFT Uniformity	good	poor	good
Processing Temperature	~250°C	> 250°C	RT ~ 300°C
Cost/Yield	Low/High	High/Low	Low/High
Long Term Stability	poor	good	unknown
AMOLED Pixel Circuit	complex	complex	simple
Pixel TFT	NMOS	NMOS+PMOS	NMOS

1.5 Thesis Proposal Outline

This thesis commences in the first chapter by introducing the background and motivation of my research. In Chapter II, *ab initio* quantum mechanical calculations were performed on crystalline In-Ga-Zn-O to study its electronic structure including the band structure and density of states. The effect of point defects was also explored. In Chapter III, the basic electrical properties of inverted-staggered a-IGZO TFTs fabricated on glass substrates were studied. Several TFT parameter extraction methods were discussed, including the threshold voltage, field-effect mobility, non-linear factor, and source/drain contact resistance. In Chapter IV, the surface potential of operating a-IGZO TFTs were studied by scanning Kelvin probe microscopy. Important parameters including the field-effect mobility and source/drain contact resistance were extracted from the channel potential profile. In Chapter V, the effect of temperature on the electrical properties of a-IGZO TFTs was investigated. The thermally activated drain current was explored, and the density of deep states profile was calculated from measured data. In Chapter VI, current temperature stress measurements were performed on a-IGZO TFTs. Several factors were considered when investigating the electrically stability of the devices, including the stress time, stress temperature, stress current, and TFT biasing conditions. In Chapter VII, a-IGZO TFT SPICE model was developed based on the RPI a-Si:H TFT model. Several voltage- and current-programmed AMOLED pixel circuits were simulated using the a-IGZO TFT SPICE model. The effect of threshold voltage variation on the pixel circuit performance was investigated, and the potential advantages of using a-IGZO TFTs were discussed. Finally, in Chapter VIII, the thesis is ended by a summary/conclusion and suggested future work.

CHAPTER II

Ab initio Electronic Structure Calculation of In-Ga-Zn-O

2.1 Introduction

Despite the rapid progress in developing high performance oxide semiconductors, the underlying physics that determine the materials' electrical properties remain mostly unclear. Theoretical exploration of this relatively new class of semiconductor is beneficial for fundamental understanding and future material design. In the past few years, several density function theory (DFT) based calculations studying the electronic structure of crystalline or amorphous In-Ga-Zn-O have been reported. Orita et al. stated that the conduction band minimum (CBM) of crystalline In-Ga-Zn-O (c-IGZO) is formed by the overlapping of In 5s orbitals, and the InO_2 layers serve as the conduction path. They also expected that a very high conductivity can be achieved if dopant ions are introduced into the $GaZnO_2$ layers, which might have little effect in scattering carriers in the InO_2 layers [42]. Nomura et al. studied the local structure of a-IGZO and reported that the nearest neighbor distances are similar to those in c-IGZO, and the coordination numbers of the ions are reduced from the crystalline phase, resulting in a smaller density. They also reported that the CBM is formed by the In 5s orbitals [43]. Medvedeva et al. found that the CBM of c-IGZO is formed by the s orbitals of all cations and the p orbitals

of oxygen atoms, and the isotropic electron effective mass ($0.23m_e$) can be obtained by averaging over those of the corresponding single-cation oxide constituents [44]. Kamiya et al. studied the oxygen deficiencies in a-IGZO, and reported that an oxygen defect may serve as an electron trap or a shallow donor depending on its local structure (whether a vacancy site is formed) [45, 46]. Omura et al. studied the effect of native point defects in c-IGZO, and suggested that interstitial hydrogen serve as shallow donors, and interstitial oxygen occupying an octahedral interstitial site form defect states and trap both electrons and holes [47]. In this work, we perform *ab intio* quantum mechanics calculations on c-IGZO. Electronic structure of c-IGZO is explored, including the band structure and density of states. The effect of point defects (oxygen vacancies, substitution hydrogen, interstitial hydrogen and oxygen) on c-IGZO is also investigated.

2.2 In-Ga-Zn-O Unit Cell Structure and Calculation

The crystalline structure of In-Ga-Zn-O [42] (shown in Fig. 2.1) adopts rhombohedral symmetry (space group: R-3m) with lattice parameters a = b = 3.295Å, c = 26.07Å, $\alpha = \beta = 90°$, $\gamma = 120°$. It is a layered structure with alternating laminated layers of InO_2^- and $GaO(ZnO)^+$. These layers accumulate to form a unit cell in the following order: InO_2^-, $GaO(ZnO)^+$, $GaO(ZnO)^+$, InO_2^-, $GaO(ZnO)^+$, $GaO(ZnO)^+$, InO_2^-, $GaO(ZnO)^+$, and $GaO(ZnO)^+$. The In^{3+} ions in the InO_2^- layer form InO_6 octahedra, which are two-dimensionally connected in an edge-sharing network. The Ga^{3+} and Zn^{2+} ions randomly occupy the trigonal-bipyramidal sites (MO_5) in the $GaO(ZnO)^+$ layers, and are each coordinated by five oxygen atoms. The bond lengths and bond angles between metal and oxygen atoms of InO_6 and MO_5 are given in Fig. 2.2. The structure of c-IGZO is summarized in Table 2.1.

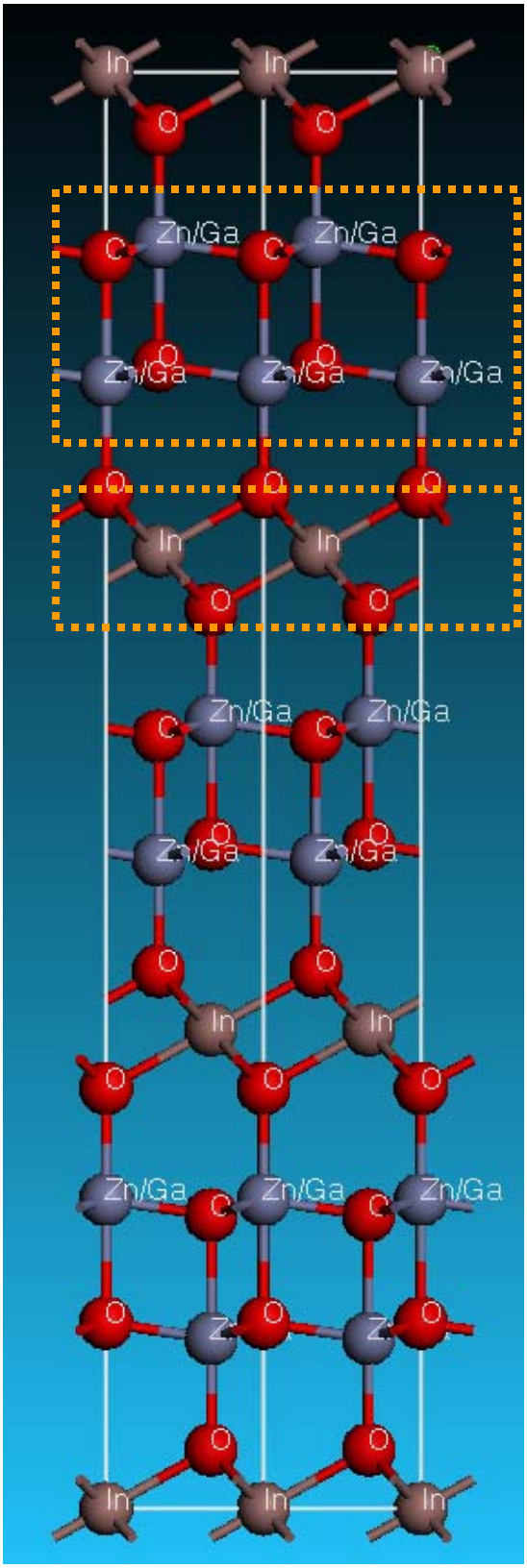

Figure 2.1 Crystalline structure of In-Ga-Zn-O

Table 2.1 Crystalline Structure of In-Ga-Zn-O [42]. Values inside the parentheses are of the relaxed structure after geometry optimization.

Space group	R-3M
Lattice parameters in hexagonal axes	a = b = 3.295 Å, c = 26.07 Å α = β = 90°, γ = 120°
Anisotropic displacement parameters	In (0, 0, 0) [(0, 0, 0)] Ga/Zn (0, 0, 0.2150) [(0, 0, 0.2156)] O(1) (0, 0, 0.1292) [(0, 0, 0.1292)] O(2) (0, 0, 0.2925) [(0, 0, 0.2911)]
Bond lengths (Å)	In-O(2) 2.17996 (2.19828) M1-O(1) 1.92335 (1.92571) M1-O(2) 2.02042 (1.96715) M1-O(1) 2.3681 (2.25368)
Bond angles (°)	O(2)-In-O(2) 98.182 (97.086) O(2)-In-O(2) 81.818 (82.914) O(1)-M1-O(1) 117.869 (117.636) O(1)-M1-O(2) 98.47 (98.930) O(1)-M1-O(1) 81.53 (81.070)

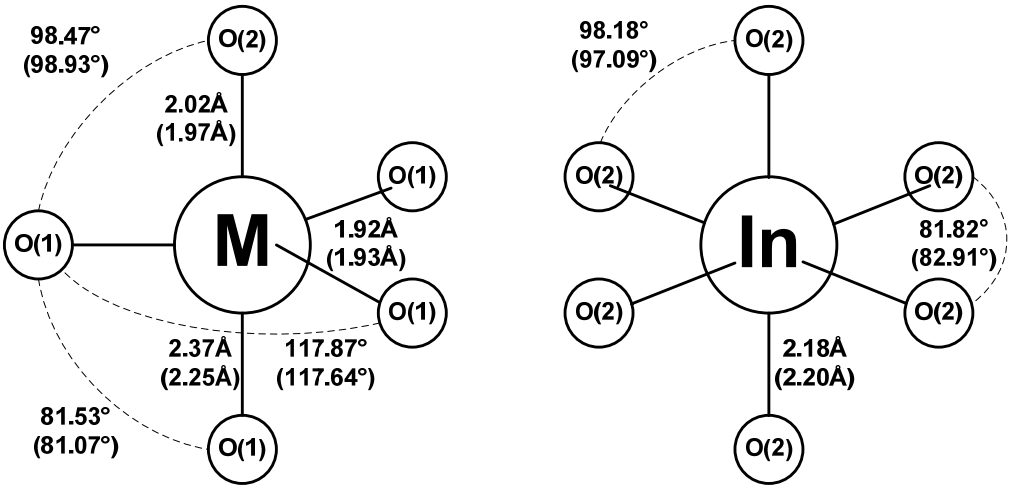

Figure 2.2 Bond lengths and bond angles of MO_5 and InO_6 in c-IGZO. Values inside the parentheses are of the relaxed structure after geometry optimization.

In this study, *ab intio* calculations were carried out using the CASTEP code [48] based on the DFT plane-wave pseudopotential method [49, 50] with the Perdew-Wang generalized- gradient approximation functional (PW91) [51]. We used the ultrasoft pseudopotentials [52] which treated the Zn/Ga 3d and In 4d states as valence electrons. A plane-wave basis cutoff energy of 380 eV with a 5x5x2 k-point grid was employed, and the Pulay density mixing scheme [53] was chosen for electronic structure minimization method. The In-Ga-Zn-O crystalline structure mentioned above (Fig. 2.1) was used as our initial unit cell (unrelaxed). In order to model the disorder caused by the randomly distributed Ga^{3+} and Zn^{2+} ions, "mixture atoms" with composition of 50% Ga and 50% Zn were used. A geometry optimization calculation was then performed on the initial unit cell using the Broyden-Fletcher-Goldfarb-Shanno (BFGS) algorithm [54]. The cell size was kept constant while the coordinates of the atoms were adjusted by an iterative process so that the total energy of the structure is minimized. The convergence criteria for the geometry optimization were total energy = 5.0e-6 eV/atom, force = 0.01 eV/Å, stress = 0.02 GPa, and displacement = 5.0e-4 Å. The relaxed bond lengths and bond angles are listed in the parentheses in Table 2.1 and Fig. 2.2. The relaxed structure is very close to that determined by single crystal X-ray diffraction measurements [55], within 2.8% differences.

An energy calculation was then carried out to study the electronic structure of c-IGZO. Gaussian smearing width of 0.1 eV and 0.2 eV were applied to the orbital occupancy and DOS calculation, respectively. Fig. 2.3 shows the calculated band structure and total density of states (DOS) profile. All energies are relative to the Fermi level (shifted to 0eV). Band structures along the high symmetry k-points in the Brillouin

zone: Γ(0, 0, 0), A(0, 0, 1/2), H(1/3, 1/3, 1/2), K(1/3, 1/3, 0), M(0, 1/2, 0), L(0, 1/2, 1/2), are displayed. The valence band maximum (VBM) is observed to be dispersionless (nearly flat) compared to the conduction band minimum (CBM). The band gap located at the Γ-point is substantially underestimated (1.781 eV) compared to the experimental value (3.2~3.5 eV), which is a well known problem of DFT calculations based on the

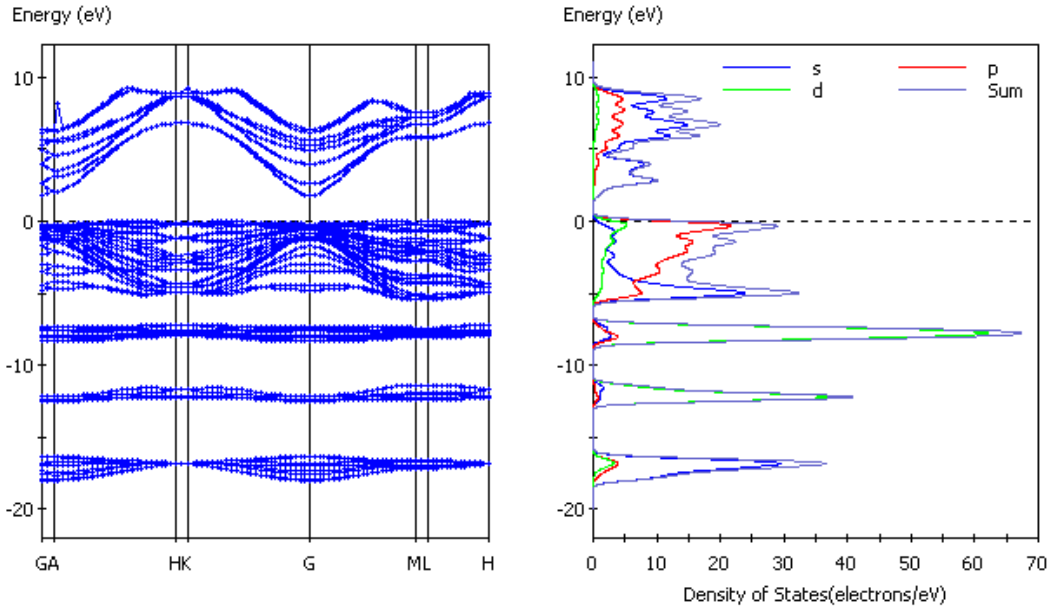

Figure 2.3 Band structure and total density of states of c-IGZO (Fermi level: 0 eV)

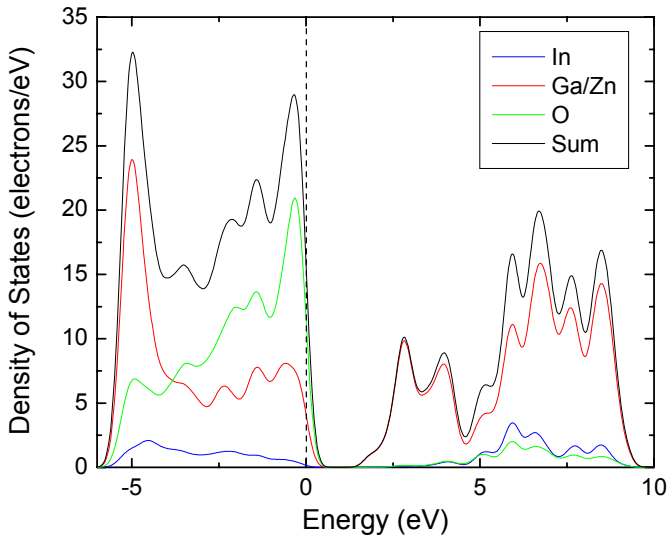

Figure 2.4 DOS contributed by each atom, In, Ga/Zn, and O.

local exchange-correlation (LDA) and gradient-corrected exchange-correlation (GGA) functionals [56]. The total DOS are broken down into the s-, p-, d-states. Examination of the DOS profile indicates that the VBM and CBM are mainly composed of the p- and s-states, respectively. The DOS contributed from each atom can be further observed from Fig. 2.4. We can see that the VBM is formed by the p-orbitals of oxygen atoms, while the CBM is mainly formed by the s-orbitals of the Ga/Zn mixture atoms. Fig. 2.5 shows the orbital drawing of the CBM (color mapping: reverse rainbow). We can see that the In 5s orbitals have the largest spatial spread of wave function, and are nearly overlapping with the neighboring In orbitals. Our result mostly agrees with Omura et al.'s observation [47]: Ga (in our case, Ga/Zn mixture atom) s states contribute most to the CBM, , while the In s states have the largest spatial spread of the wave function. Experimentally, the mobility of a-IGZO increases with the fraction of In_2O_3 content, and the incorporation of Ga^{3+} is very effective in suppressing electron carrier generation possibly due to the high ionic potential which is able to tightly attract oxygen ions [26]. However, further investigation that separates the effect of Zn^{2+} and Ga^{3+} is needed for better theoretical explanation.

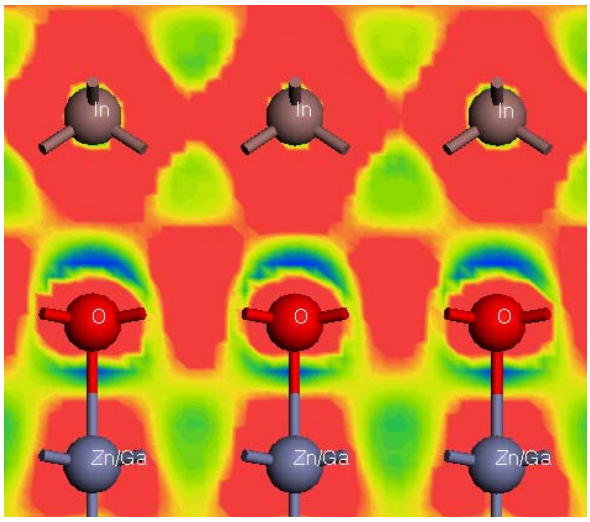

Figure 2.5 Orbital drawing of the conduction band minimum
(color mapping: reverse rainbow).

2.3 c-IGZO Super Cell with Point Defects

A supercell structure was used to investigate the effect of point defects on the electrical properties of c-IGZO. The supercell has lattice parameters that are multiples of those of the original unit cell (2x2x1). Energy calculation was performed on the defect-free supercell, and similar band structures (band gap: 1.766 eV) and DOS were obtained (Fig. 2.6), comparing to those of the original unit cell (Fig. 2.3). Please note that band structures along different high symmetry k-points: Γ(0, 0, 0), F(0, 1/2, 0), Q(0, 1/2, 1/2), Z(0, 0, 1/2) were displayed because of the P1 symmetry, and higher DOS were obtained due to the larger amount of atoms included in the supercell.

Several types of point defects were than introduced into the supercell, including oxygen vacancies, hydrogen substitutions, hydrogen and oxygen interstitials, which will be described in more detail in later subsections. For all cases, geometry optimization calculation was performed, especially to relax the atoms surrounding the defect (the cell size was kept constant). Then total energy calculation was carried out to study the electronic structures.

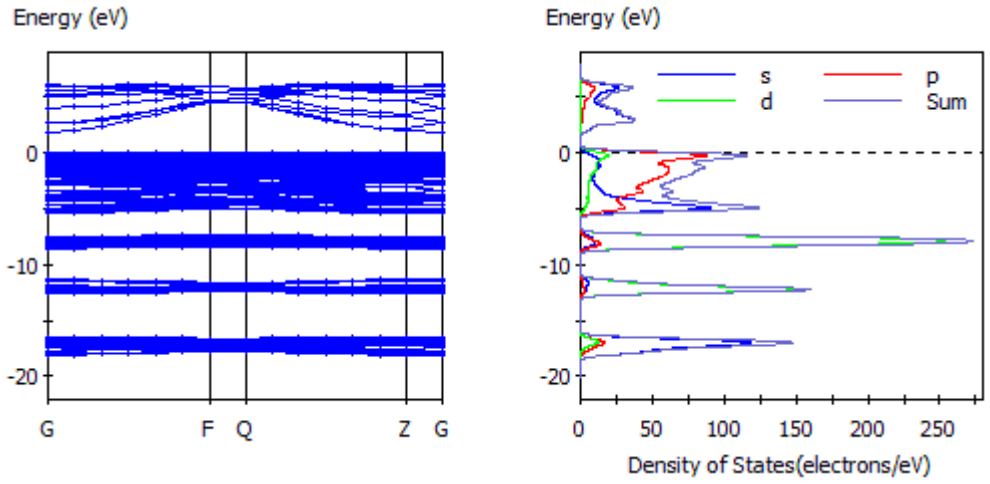

Figure 2.6 Band structure and total DOS of c-IGZO supercell. (Fermi level: 0 eV)

2.3.1 Oxygen Vacancies

Oxygen vacancies were created at two different sites. In O_{V1}, an oxygen atom bonded between four Zn/Ga mixture atoms was removed, while in O_{V2}, an oxygen atom bonded between three In and one Zn/Ga mixture atoms was removed. Figure 2.7 (a) and (b) shows the relaxed structure of O_{V1} and O_{V2}, respectively. The arrows indicate the displacement vectors of the surrounding atoms after relaxation. In O_{V1}, the three Zn/Ga mixture atoms located in the same $GaO(ZnO)^+$ layer are displaced inward by 8~10% of the equilibrium Zn-O bond length, while the Zn/Ga mixture atom located in the neighboring $GaO(ZnO)^+$ layer is displaced outward by ~5%. In $O_{V2,}$ the three In atoms are displaced inward by 3~5%, and the one Zn/Ga mixture atom is displaced inward by 9%. O_{V1} and O_{V2} have very similar band structure and density of states, shown in Fig. 2.8. In both cases, oxygen vacancies form fully occupied defect states (below the Fermi level) in the middle of the band gap, and raises the Fermi level above the VBM towards the CBM. The isosurfaces (isovalue = 0.04) of the highest occupied bands for O_{V1} and O_{V2} are shown in Fig. 2.7. It can be seen that the defect state is highly localized around the oxygen vacancy sites for both cases. The electronic structure of oxygen vacancies in ZnO proposed by Janotti and Van de Walle [57] can be used to explain the physical properties of oxygen vacancies in c-IGZO. The removal of an oxygen atom leaves four dangling bonds on the surrounding metal cations, forming a symmetric a_1 state located in the bandgap and three higher energy states above the CBM. The a_1 state is fully occupied by two electrons contributed by the four coordinated metal cations, and its energy is lowered when the four metal cations approach each other.

The n-type conductivity of metal oxide semiconductors including ZnO and a-IGZO has been observed to vary with the partial pressure of oxygen during the growth or thermal annealing process, therefore, oxygen vacancies have been traditionally viewed as the source of unintentional n-type doping. However, based on our calculation result, oxygen vacancies introduce fully occupied defect states 0.8eV below the CBM, and are deep rather than shallow donors, therefore, could not be the cause of the enhance in conductivity. Other origin must be responsible for this effect.

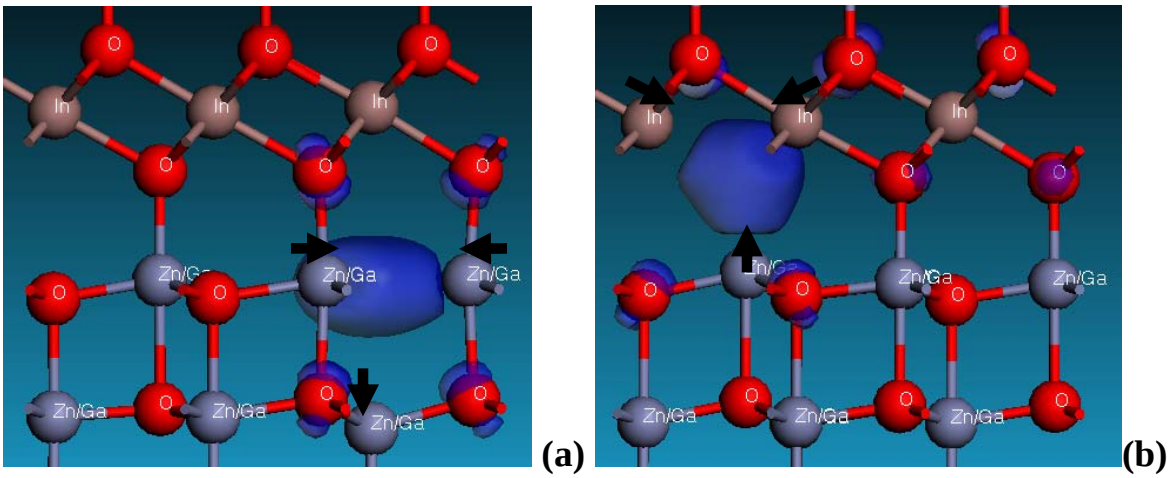

Figure 2.7 Isosurface of the highest occupied band of (a) O_{V1} and (b) O_{V2}.

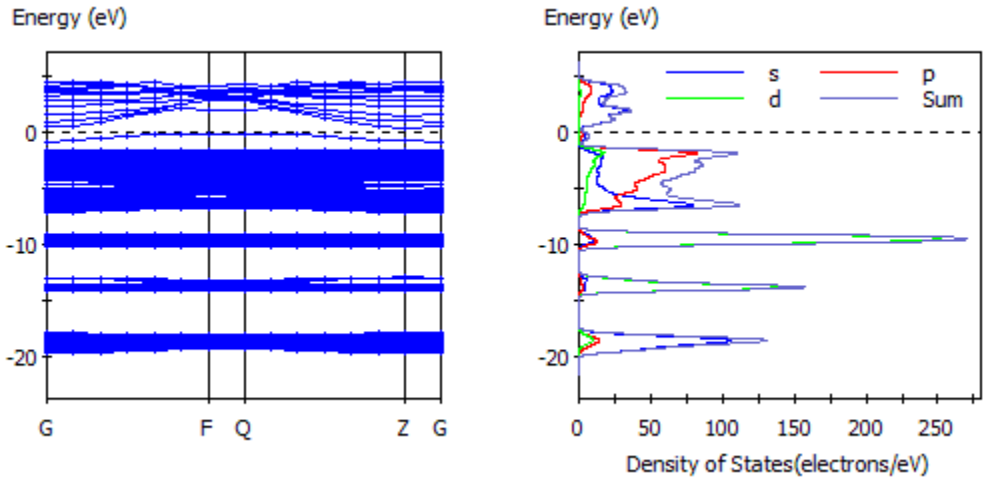

Figure 2.8 Band structure and DOS of c-IGZO supercell with oxygen vacancy.

2.3.2 Hydrogen Substitutions

C-IGZO supercell with a substitutional hydrogen atom located on an oxygen site was investigated. This configuration can also be regarded as a complex consisting of a hydrogen atom and an oxygen vacancy. Defects were created at two different sites. In H_{S1}, a hydrogen atom was placed at O_{V1} (bonded between four Ga/Zn mixture atoms), and in H_{S2}, a hydrogen atom was placed at O_{V2} (bonded between three In atoms and one Ga/Zn mixture atoms). Figure 2.9 (a) and (b) shows the relaxed structure of H_{S1} and H_{S2}, respectively. The arrows indicate the atom displacement directions during the geometry optimization process. We can see that the substitutional hydrogen atom forms a longer bonding with the Zn/Ga mixture atom located in the neighboring $GaO(ZnO)^+$ layer. In H_{S1}, the hydrogen atom and the Zn/Ga mixture atom is displaced outward by ~9% and 6%, respectively, while in H_{S2}, the displacement is ~2% and 11%, respectively. Figure 2.10 shows the similar band structures and DOS shared by H_{S1} and H_{S2}. We can see that the addition of hydrogen atoms turn the oxygen vacancies into shallow donors, and raises the Fermi level above the CBM. Janotti and Van de Walle also proposed the electronic structure of hydrogen substitutions occupying oxygen sites in ZnO [58]. The H 1s orbital combines with the a_1 state (formed by the four dangling bonds surrounding the oxygen vacancy) and results in a bonding state located deep in the valence band, and an antibonding state in the conduction band. Two of the three electrons (one from the hydrogen atom, and two from the coordinating metal cations) occupy the bonding state. The third electron occupies the antibonding state and then relaxes to the CBM. Our calculated electronic structure agrees with this model. The bonding state is found to be ~6eV below the VBM and the lowest energy antibonding/nonbonding states are found to

be ~1eV above the CBM (isosurfaces are shown in Fig. 2.9 (a) and (b) respectively). We can see that the six next-nearest-neighbor oxygen atoms also contribute to the bonding state orbital. A small discrepancy is observed, however, in ZnO [58] the substitutional hydrogen atom is equally bonded to all four Zn atoms in ZnO, while in c-IGZO the bonding seems weaker to the Zn/Ga mixture atom located in the neighboring $GaO(ZnO)^+$ layer, possibly because of the alternating layered structure of c-IGZO. Therefore, based on our calculation results, the dependency of c-IGZO conductivity on oxygen partial pressure can be better explained by hydrogen substitutions located on oxygen sites, since hydrogen can be easily incorporated during thin film growth or annealing processes.

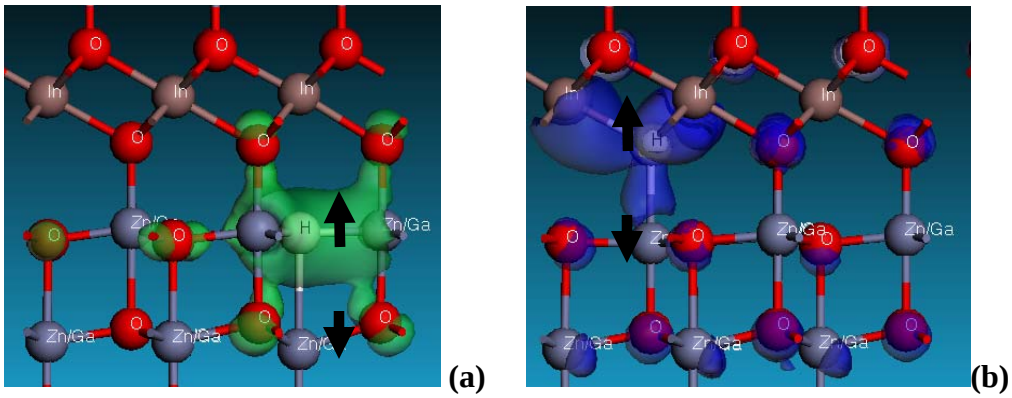

Figure 2.9 Relaxed structures of (a) H_{S1} and (b) H_{S2}. Isosurfaces of the bonding state (a) and the lowest energy antibonding/nonbonding states (b) are also shown.

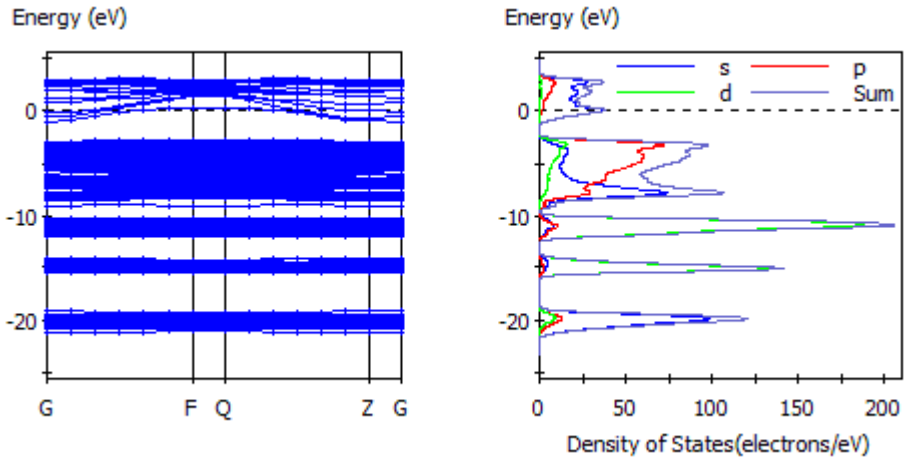

Figure 2.10 Band structure and DOS of c-IGZO supercell with hydrogen substitution.

2.3.3 Hydrogen Interstitials

Hydrogen interstitial atoms were placed at eight different sites, close to an oxygen atom to form an O-H bond, as shown in Fig. 2.11. BC indicates the bond-center sites, and AB indicates the anti-bonding sites. The symbol "//" means the O-H bond is parallel to the c axis; other bond directions are denoted by "⊥". The hydrogen atom was initially placed 1Å from an oxygen atom. After geometry optimization, $H_{AB\perp 1}$ relaxed into $H_{BC//1}$, and $H_{BC\perp 2}$ relaxed into $H_{AB\perp 2}$, while the other six interstitial sites seem stable. Fig. 2.12 shows the relaxed structure of two examples, $H_{BC//1}$ and $H_{AB\perp 2}$. In $H_{BC//1}$, the optimized

d Zn/Ga mixture atoms located on the

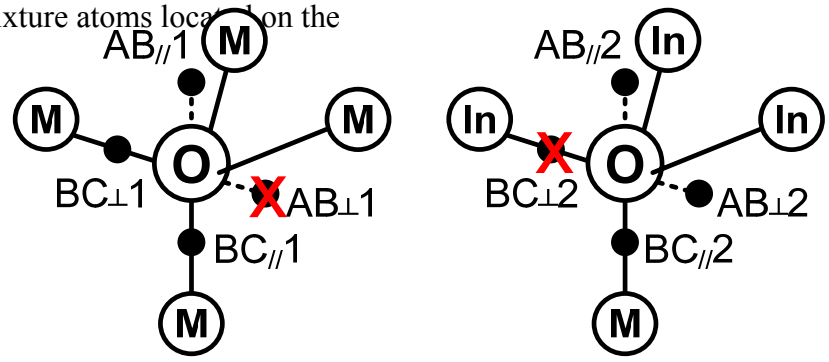

Figure 2.11 Hydrogen interstitial sites used in this calculation

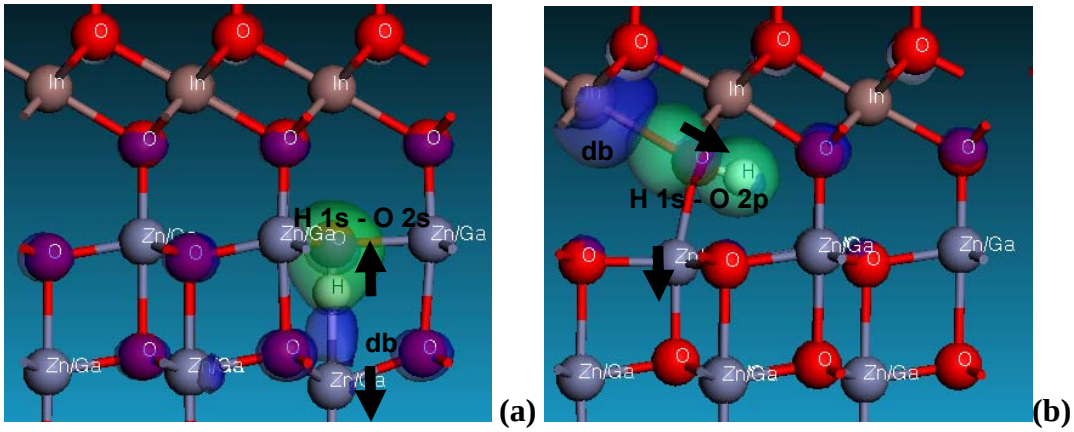

Figure 2.12 Relaxed structures of (a) $H_{BC//1}$ and (b) $H_{AB\perp 2}$. Isosurfaces of the H1s-O2s (a) H1s-O2p (b) bonding orbitals, and metal cation dangling bond orbitals are also shown

same bond moved outward by ~11% and 13% of their original M-O bond, respectively. In $H_{AB\perp 2}$, the optimized O-H bond length is 0.985 Å, and the oxygen moved outward by ~19% from the In atom, while the Zn/Ga mixture atom shifted downward by 14%. All of the six stable hydrogen interstitial models resulted in similar band structures and density of states, as shown in Fig. 2.13. Comparing to the defect free c-IGZO supercell (Fig. 2.6), the main differences are the higher Fermi level located above the CBM, and the hydrogen interstitial related states at energy levels -22eV and -9eV. The isosurfaces of the localized states around -22eV and -9eV are plotted in Fig. 2.12(a) and (b), and can be seen that they are associated with the H1s-O2s, and H1s-O2p bond orbitals, respectively, indicating that the hydrogen interstitial atoms bond strongly to oxygen atoms. Similar electronic structures were reported by other first-principles studies of ZnO [59] and c-IGZO [47]. An explanation of the donor-like behavior of hydrogen interstitials has been proposed by Van de Walle and Neugebauer [60]. The strong O-H bonding results in the creation of a dangling bond (db) on a neighboring metal cation, which has an energy level above the CBM; it is therefore energetically more favorable to leave it unoccupied (db^+). From our calculated electronic structure, we've found the dangling bond state to be ~1eV above the CBM (isosurface shown in Fig. 2.12).

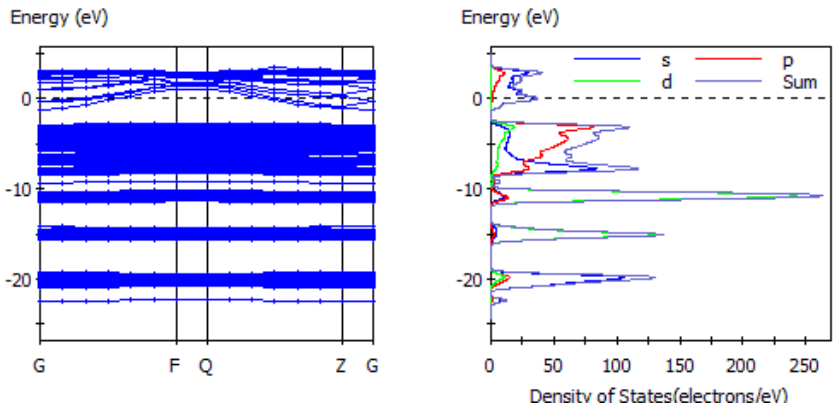

Figure 2.13 Band structure and DOS of c-IGZO supercell with hydrogen interstitial.

2.3.4 Oxygen Interstitials

Two different oxygen interstitial configurations were explored, split (O_{split}) and octahedral (O_{oct}). In O_{split}, the interstitial oxygen atom (O_i) was initially placed at an anti-bonding site of an In-O bond, 1.46Å from the oxygen atom (O_o). After geometry optimization (as shown in Fig. 2.14a), the O_i-O_o bond length became 1.51Å, forming a weaker bond compared to that of an isolated O_2 molecule (1.21Å). O_i and O_o each bonds to two metal cations, and occupy the same lattice site, forming a split interstitial. The In-O and M-O bonds are shortened by 1~2.5% compare to the defect free structure. In O_{oct}, the interstitial oxygen atom (O_i) was placed at an octahedral site coordinated by 6 oxygen atoms (O_o). After relaxation, the six surrounding O_o atoms displaced outward from O_i by 8~10% of the unrelaxed interatomic distance (as shown in Fig. 2.14b). It is reported by other first-principles studies that oxygen interstitials occur at either split or octahedral sites in ZnO [61, 62] and c-IGZO [47], which agrees with our calculated structure.

Figure 2.15 (a) and (b) shows the calculated band structure and density of states of O_{split} and O_{oct}, respectively. We observed that O_{split} forms fully occupied deep level states above the defect-free valence band maximum (VBM_0). The isosurface of the defect states is shown in Fig. 2.14(a), which is mainly contributed by the O_i-O_o anti-bonding ppπ^* orbital (doublet, only one is shown). Other O_i related localized states were also observed including ssσ at -21eV, and ssσ^* at -15.5eV. Limpijumnong et al. proposed that split interstitials formed by first row elements C, N, and O on oxygen sites in ZnO can be described by substitutional diatomic molecules [63]. Therefore, the physical property of the O_i-O_o defect is very similar to that of the free O_2 molecule with molecular orbitals ssσ, ssσ^*, ppσ, ppπ (doublet) located in the valence band filled with ten electrons, and ppπ^*

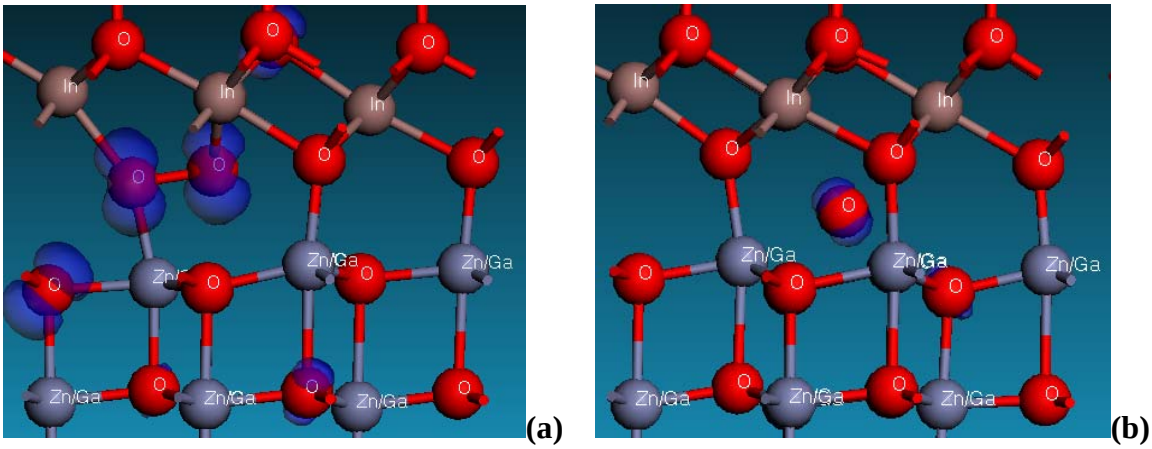

Figure 2.14 Relaxed structures of (a) O_{split} and (b) O_{oct}. Isosurfaces of the oxygen interstitial defect states are also shown.

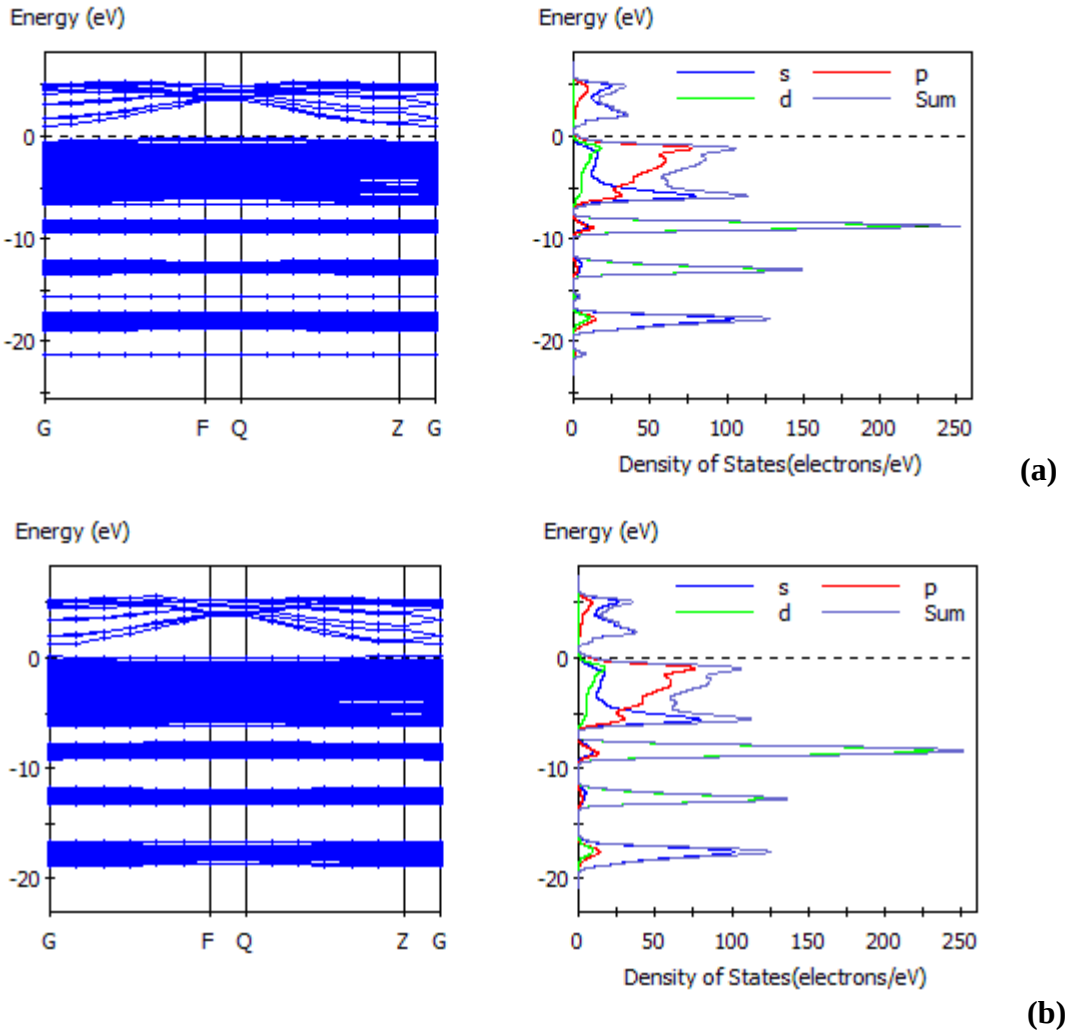

Figure 2.15 Band structure and DOS of c-IGZO supercell with oxygen interstitial (a) O_{split} and (b) O_{oct}

(doublet) located slightly above the VBM_0 filled with the remaining two electrons of the O atoms, and two electrons contributed from the four coordinating metal cations, which agrees with our calculated band structure of O_{split}. The longer O_i-O_o bond length can also be explained by the addition of extra electrons to the anti-bonding $pp\pi^*$ orbitals. By contrast, O_{oct} forms both occupied and unoccupied states above VBM_0. The defect states are mainly contributed by the p orbitals of O_i (isosurface shown in Fig. 2.14b), and serves as deep acceptors. Our result agrees with other reported first-principles studies of ZnO [61, 62] and c-IGZO [47], that oxygen interstitials can exist as electrically inactive split interstitials, or as deep acceptors at the octahedral site in n-type samples

2.4 Conclusion

Ab initio calculations were performed for crystalline In-Ga-Zn-O. (c-IGZO). The calculated electronic structure showed that the valence band maximum (VBM) is mostly composed of the p orbitals of the oxygen atoms. The conduction band minimum (CBM) mainly consists of the s orbitals of the Zn/Ga mixture atoms, while the In atoms have the largest spatial spread of states corresponding to CBM. The effect of different point defects was also investigated. Oxygen vacancies created fully occupied defect states within the band gap and serve as deep donors. Both hydrogen substitutions (H_s) and interstitials (H_i) act like shallow donors, and raise the Fermi level above the CBM. Oxygen split interstitials created fully occupied defect states above VBM, while oxygen octahedral interstitials create both occupied and unoccupied states, and may serve as acceptor states in c-IGZO. Our calculation results can theoretically explain the dependence of IGZO conductivity on oxygen partial pressure (H_s) [64] and its behavior when subject to hydrogen plasma treatment (H_i) [65] observed experimentally.

CHAPTER III

Electrical Properties of Amorphous In-Ga-Zn-O Thin Film Transistors

3.1 Introduction

In 2004, Nomura et al. reported the first transparent flexible TFTs using a-IGZO as the active channel layer [18]. a-IGZO thin films were deposited by pulsed laser deposition (PLD) at room temperature on polyethylene terephthalate (PET) substrates. The top-gate coplanar a-IGZO TFT showed saturation field-effect mobility around 7 cm^2/V-s, Off-current on the order of 10^{-7} A, and an On-Off current ratio ~ 10^3. The performance remained almost unaffected when the TFT was bent. Since then, research in developing high performance a-IGZO TFTs has progressed rapidly. Yabuta et al. fabricated TFTs using a-IGZO channel layer deposited by radio-frequency (rf) magnetron sputtering at room temperature [19]. Top-gate coplanar devices were fabricated on glass substrates, and exhibited high field-effect mobilities 10 cm^2/V-s, low Off-currents 10^{-12} A, and current On-off ratios up to 10^8, demonstrating that high quality a-IGZO thin films could be fabricated by mass-production compatible methods. In this chapter, we fabricate and characterize inverted-staggered rf magnetron sputtered a-IGZO TFTs, and provide analysis on the TFT electrical performance.

3.2 Experimental

Fig. 3.1 shows the top view and cross section of an inverted-staggered a-IGZO TFT used in this study. The TFTs were fabricated on glass substrates (Corning #1737). The gate electrode Ti (5nm)/Au (40nm)/Ti (5nm) was deposited by electron-beam vapor deposition and patterned by lift off (negative resist). 200nm thick silicon dioxide (SiO_2) thin film, as the gate insulator, was deposited by rf magnetron sputtering, and patterned by wet etch with buffered hydrofluoric acid (BHF). The a-IGZO thin film (30nm) was deposited by rf magnetron sputtering at an input rf-power of 200 W in Ar and O_2 mixing gases under the total pressure of 0.5 Pa (the partial pressure of O_2 was 25 mPa) at room temperature, and patterned by wet etch with hydrochloric acid (HCl). After annealing in air at 300°C for 20 min, the source/drain electrodes Ti (5nm)/Au (100nm)/Ti (5nm) were deposited by electron-beam vapor deposition and patterned by lift off (negative resist). A SiO_2 film as the back channel protection layer (100nm) was deposited by rf magnetron sputtering and patterned by wet etch with BHF. Finally, the TFTs were annealed in air at 200°C for 1 hour. Electrical measurements were done under ambient laboratory conditions and in dark, using a Hewlett-Packard 4156A semiconductor parameter analyzer controlled by ICS Metrics software.

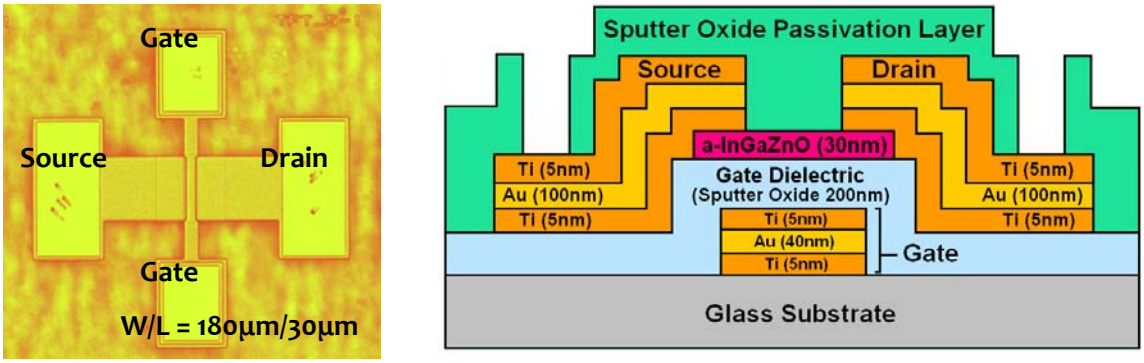

Figure 3.1 (a) Top view and (b) cross section of an a-IGZO TFT used in this study.

3.3 a-IGZO TFT Electrical Performance and Parameter Extraction

The a-IGZO TFT output characteristics were measured by sweeping the drain-to-source voltage (V_{DS}) from 0 to 20V for various gate-to-source voltage (V_{GS}) levels as shown in Fig. 3.2 (a). The inset shows a closer view of the plot for lower V_{DS} voltages (0 ~ 1V). It can be observed that there is no current crowding near the origin of the output characteristics. Current crowding is a phenomenon which the drain current increases slowly with increasing V_{GS} such that the output characteristics for different V_{GS} appear to crowd together, and usually occurs when the source/drain contact is not Ohmic [66]. The output characteristics of our a-IGZO TFTs indicate that a sufficient on-current can be maintained even with low V_{DS} voltages, which is desirable for AMOLED applications.

Fig. 3.2 (b) shows the measured TFT linear regime (V_{DS} = 0.1V) transfer characteristic. We extracted the apparent field-effect mobility (μ) and threshold voltage (V_T) by using the standard MOSFET equation.

$$I_D = \frac{W}{L} \cdot C_{ox} \cdot \mu \cdot (V_{GS} - V_T) \cdot V_{DS} \tag{3.1}$$

where W and L are the channel width and channel length, respectively, and C_{ox} is the gate insulator capacitance per unit area. To accommodate for the nonlinearity of our I_D-V_{GS} curve, a fitting range between 10% and 90% of the maximum measured I_D is chosen, as shown as the solid line in Fig. 3.2 (b). We extracted from the x-interception and slope V_T = 3.1V and μ = 9.4 cm^2/V-s, respectively.

Fig. 3.2 (c) shows the TFT transfer characteristics plotted in log scale for V_{DS} = 0.1V and 20V. Very low off-currents (10^{-13}~10^{-12}A), and current On-Off ratios exceeding 10^8 are achieved.

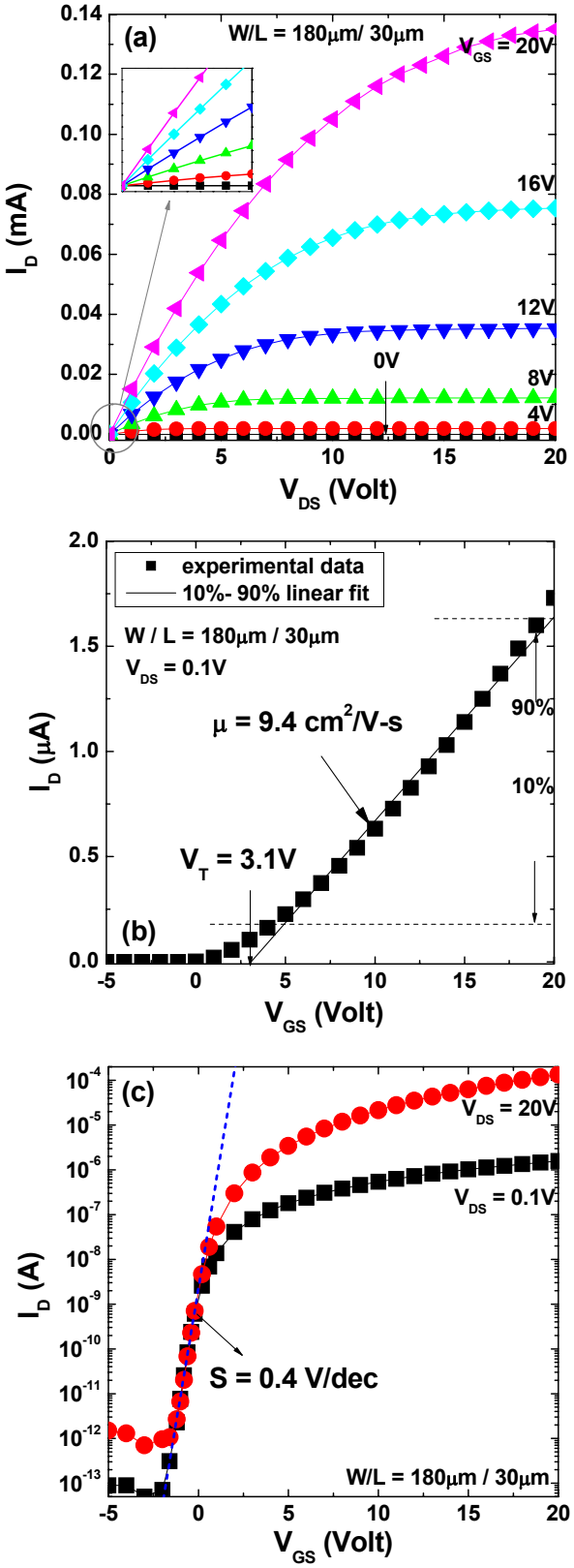

Figure 3.2 Measured (a) output characteristics, (b) linear regime transfer characteristics and (c) transfer characteristics plotted in log scale of a-IGZO TFTs.

The subthreshold slope (S) is extracted at the steepest point of the $\log(I_D)$-V_{GS} plot by using the following equation

$$S = \left(\frac{d\log(I_D)}{dV_{GS}} \right)^{-1} \tag{3.2}$$

The subthreshold slope of our a-IGZO TFTs is extracted to be as small as ~0.4V/dec, which allows achieving a high switching speed with a low gate driving voltage. If we assume that the density of deep bulk states N_{BS} and interface states N_{SS} is independent of energy, the subthreshold slope can be linked to N_{BS} and N_{SS} by [67]

$$S = \ln(10) \cdot \frac{kT}{e} \cdot \left[1 + \frac{e \cdot t_{ox}}{\varepsilon_i} \cdot (\sqrt{\varepsilon_s \cdot N_{BS}} + e \cdot N_{SS}) \right] \tag{3.3}$$

where k is the Boltzmann constant, T is the temperature, e is the absolute value of the electron charge, ε_i and ε_s are the insulator and semiconductor dielectric constant, respectively, and t_{ox} is the insulator thickness. Equation (3.3) does not permit the separate determination of N_{BS} and N_{SS}, but can be used to find upper limits $N_{BS\_max} = 4.28\times10^{16}$ $cm^{-3}eV^{-1}$ and $N_{SS\_max} = 6.16\times10^{11}$ $cm^{-2}eV^{-1}$ by assuming $N_{BS} = 0$ and $N_{SS} = 0$, respectively.

3.4 V_{GS} Dependent Field-Effect Mobility

The standard MOSFET equation assumes a linear relation between I_D and V_{GS}, which is not valid for our a-IGZO TFTs, as can be seen from Fig. 3.2 (b). This nonlinearity can be better observed by extracting the apparent field-effect mobility (μ) from the first derivative of the linear regime I_D-V_{GS} curve

$$\mu = \frac{\partial I_D / \partial V_{GS}}{W/L \cdot C_{ox} \cdot V_{DS}} \tag{3.4}$$

The apparent field-effect mobility (μ) as a function of V_{GS} is plotted in Fig. 3.3(b). We

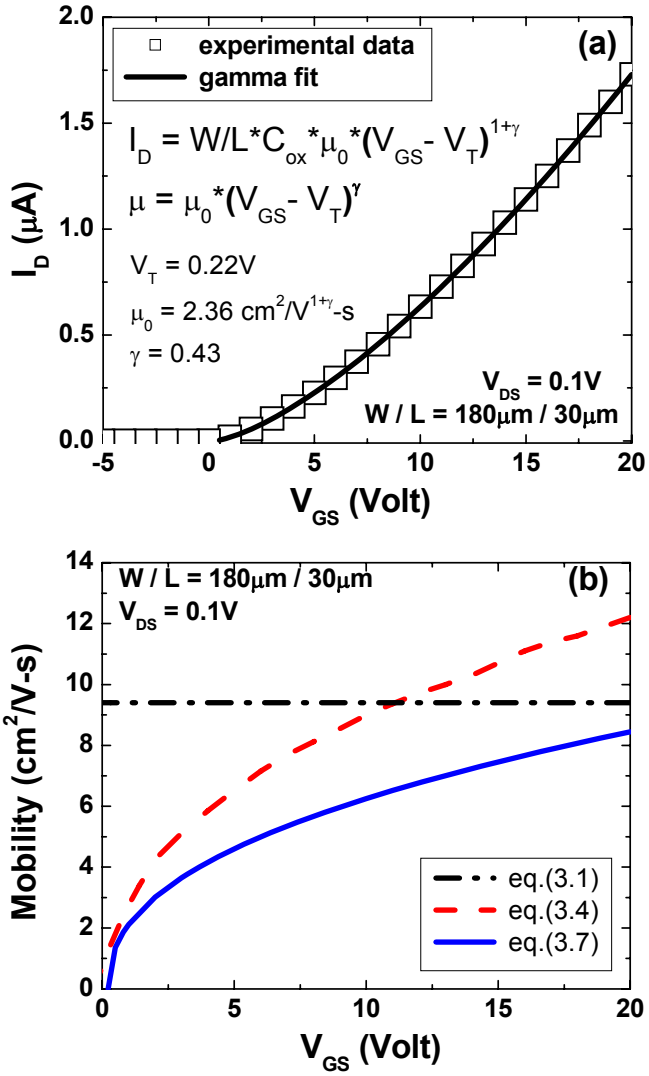

Figure 3.3 (a) Extracting the field-effect mobility and threshold voltage by considering the non-linearity of the TFT I-V curve (b) The V_{GS} dependence of the field-effect mobility (μ) extracted by eq.(3.1), (3.4) and (3.7).

can see that instead of maintaining a constant value, μ increases with V_{GS} and reaches a maximum value of 12.2cm^2/V-s within our measurement range, and the apparent field-effect mobility extracted by (3.1) can in fact be considered as an average of that extracted by (3.4). The V_{GS} dependence of μ can be explained by the energy dependent, density-of-localized-states near the Fermi level [68]. As V_{GS} increases, most localized states are filled, and more induced charges can contribute to the free carriers.

To better model the a-IGZO TFT I-V characteristics, a V_{GS} dependent field-effect mobility can be introduced

(3.5) $$\mu = \mu_0 \cdot (V_{GS} - V_T)^{\gamma}$$

where μ_0 (unit: $cm^2/V^{1+\gamma}$-s) is the fitting parameter associated with the field-effect mobility and γ is the nonlinearity factor. In a-Si TFTs, γ is related to the characteristic temperature T_0 of the exponentially distributed conduction band tail states [68],

(3.6) $$\gamma = 2 \cdot (\frac{T_0}{T} - 1)$$

where T is the ambient temperature, and $T_0 >> T$. Takechi et al. [69] reported that the exponential tail-states distributed model can also be used to describe the above threshold characteristics of a-IGZO TFTs, and found a smaller T_0 compared to that of a-Si TFTs.

By plugging (3.5) into (3.1), the MOSFET equation becomes

(3.7) $$I_D = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot (V_{GS} - V_T)^{1+\gamma} \cdot V_{DS}$$

The parameters V_T, μ_0, and γ can be extracted by fitting equation (3.7) to the TFT linear regime transfer characteristic, as shown as the solid line in Fig. 3.3 (a). The obtained values are V_T = 0.22V, μ_0 = 2.36 $cm^2/V^{1+\gamma}$-s, and γ = 0.43. Therefore, T_0 is ~365 K, smaller than the typical values (600~700 K) for a-Si TFTs [68, 69], which corresponds to a steeper tail states distribution. The field-effect mobility extracted by (3.7) is plotted in Fig. 3.3(b). Although the μ extracted by (3.4) and (3.7) are both V_{GS} dependent, (3.4) does not take into consideration the nonlinearity of the I_D-V_{GS} curve, and therefore overestimates μ by a factor of $1+\gamma$ compared to the gamma method.

(3.8) $$\frac{\partial I_D / \partial V_{GS}}{W/L \cdot C_{ox} \cdot V_{DS}} = (1+\gamma) \cdot \mu_0 \cdot (V_{GS} - V_T)^{\gamma}$$

3.5 Source/Drain Contact Resistance

We investigated the source/drain contact resistance (R_S/R_D) of the a-IGZO TFTs by using the transmission line method (TLM) [70]. The total TFT ON resistance (R_T) can be described by

$$R_T = \frac{V_{DS}}{I_D} = R_S + R_D + r_{ch} \cdot L \tag{3.9}$$

where r_{ch} is the TFT channel resistance per unit length. Using equations (3.1) and (3.9), we can express the total TFT ON resistance R_T as a function of the apparent field-effect mobility (μ) and threshold voltage (V_T).

$$R_T = \frac{V_{DS}}{I_D} = \frac{L}{W \cdot C_{ox} \cdot \mu \cdot (V_{GS} - V_T)} \tag{3.10}$$

Applying the same equation to the ideal TFT (conduction channel only, without R_S/R_D) allows us to express the TFT channel resistance per unit length r_{ch} as a function of the intrinsic mobility (μ_{in}) and threshold voltage (V_{Tin})

$$r_{ch} = \frac{1}{W \cdot C_{ox} \cdot \mu_{in} \cdot (V_{GS} - V_{Tin})} \tag{3.11}$$

The intrinsic TFT parameters μ_{in} and V_{Tin} are representative of the electrical characteristics of the conduction channel without the influence of the source/drain contact resistance.

We applied the TLM to our a-IGZO TFTs by analyzing a series of TFTs with the same channel width (180μm) but different channel lengths (10μm, 30μm, 60μm). The apparent TFT parameters are summarized in Table 3.1. The apparent threshold voltage (V_T), subthreshold slope (S), and off-current values (I_{OFF}) are similar for the 3 TFTs, while the apparent field-effect mobility (μ) slightly increases with the channel length.

Table 3.1 The field-effect mobility (μ), threshold voltage (V_T) , subthreshold slope (S), and off-current (I_{OFF}) of TFTs with different channel length.

L (μm)	10	30	60
μ (cm^2/V-s)	7.7	7.94	8.16
V_T (V)	3.2		
S (V/dec)	0.4		
I_{OFF} (A)	$10^{-13} \sim 10^{-12}$		

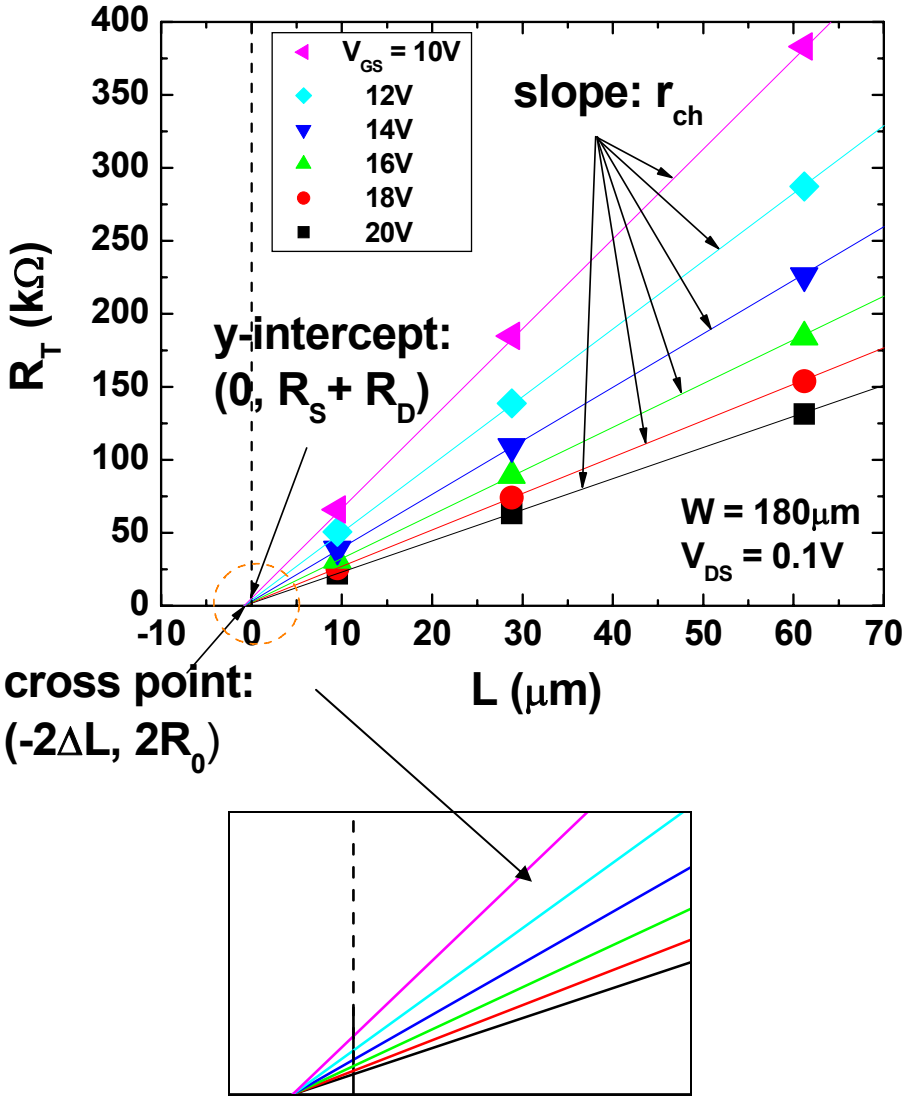

Figure 3.4 The total TFT ON resistance (R_T) versus channel length (L) for several levels of V_{GS}.

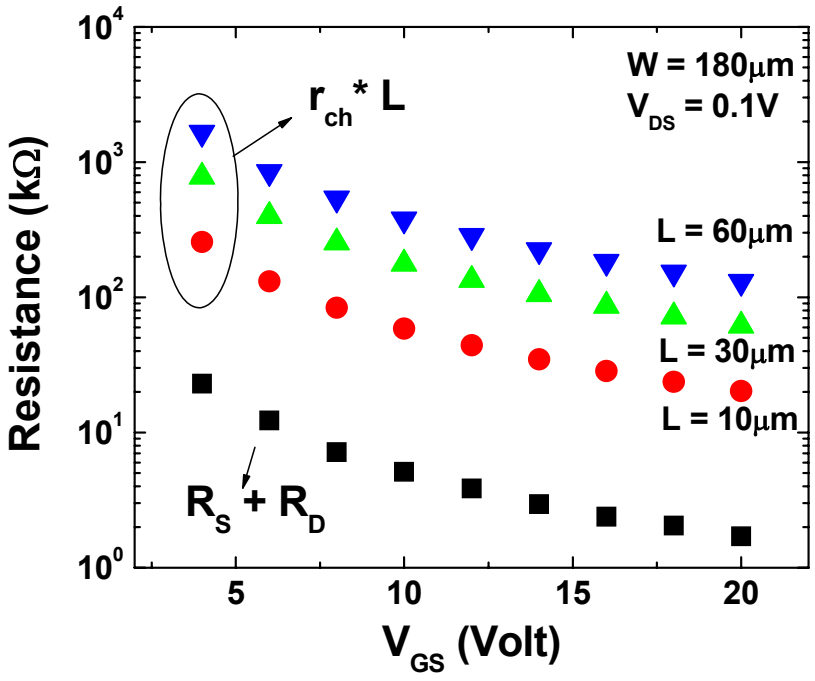

Figure 3.5 The Contact resistance (R_S + R_D) and the channel resistance (r_{ch}* L) as a function of V_{GS}.

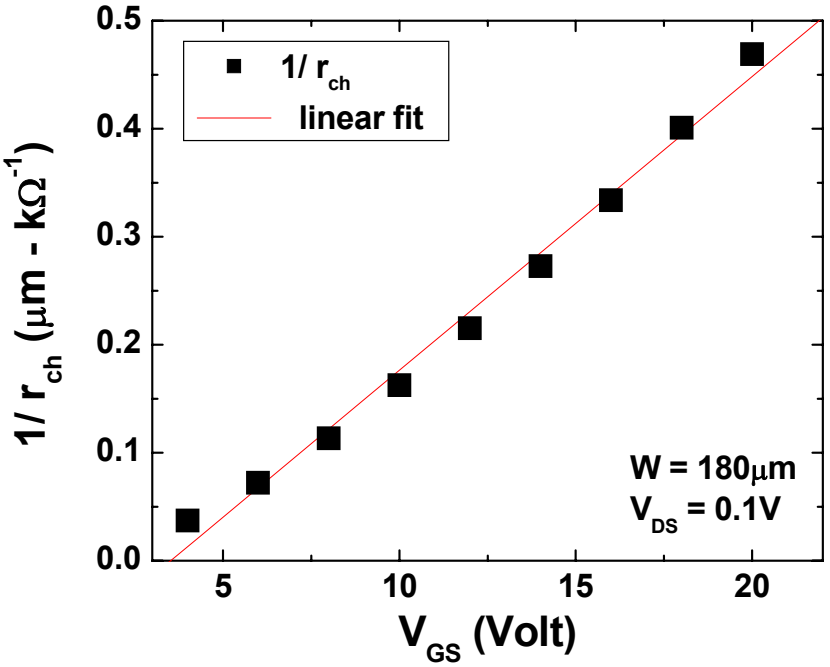

Figure 3.6 Extracting the intrinsic field-effect mobility and threshold voltage by plotting 1/r_{ch} versus V_{GS}.

This channel length dependence of μ is due to the effect of R_S/R_D, which will be clearer later on. The extraction of the TFT source/drain contact resistance and intrinsic field-effect mobility and threshold voltage is then rather straightforward. We first plot R_T as a function of the TFT channel length for different V_{GS}, as shown in Fig. 3.4. By fitting the R_T-L plot to equation (3.9), $R_S + R_D$ and r_{ch} can thus be obtained from the y-interception and slope for different V_{GS} biases, respectively. The extracted source /drain contact resistance ($R_S + R_D$) and channel resistance ($r_{ch} \times L$) are both V_{GS} dependent as shown in Fig. 3.5. $R_S + R_D$ is 1.7kΩ at $V_{GS} = 20V$ and increases to 23 kΩ at $V_{GS} = 4V$, and is more than one order of magnitude smaller than the TFT channel resistance, depending on the channel length. The intrinsic TFT parameters can then be obtained by plotting $1/r_{ch}$ versus V_{GS}. The TFT channel resistance per unit length (r_{ch}) and contact resistance (R_S+R_D) are extracted from the slope and y-intercept of the plots for different V_{GS}, respectively. ΔL and R_0 are extracted from the common cross point of all $R_T - L$ curves shown in Fig. 3.6. Using equation (3.11), V_{Tin} and μ_{in} can be extracted by the x-interception and the slope, respectively. The data shown in Fig. 3.6 yield $V_{Tin} = 3.5V$ and $\mu_{in} = 8.8cm^2/V\text{-}s$. It can be observed from Table 3.1 that the TFT apparent field-effect mobility is slightly smaller than its intrinsic value. This effect is more severe for shorter channel length devices, since the channel resistance is smaller and therefore more comparable to the source/drain contact resistance.

The effect of the source/drain contact resistance can also be represented as an increase of the apparent channel,

$$(3.12) \quad R_T = R_S + R_D + \frac{L}{W \cdot C_{ox} \cdot \mu_{in} \cdot (V_{GS} - V_{Tin})} = 2 \cdot R_0 + \frac{L + 2 \cdot \Delta L}{W \cdot C_{ox} \cdot \mu_{in} \cdot (V_{GS} - V_{Tin})}$$

where R_0 represents the limit of R_S/R_D for a very high V_{GS}, and ΔL is associated with the

effective channel length. Both ΔL and R_0 are independent of V_{GS}. The values of ΔL and R_0 are extracted from the common cross point of the R_T-L curves, whose coordinate is (-2 ΔL, 2 R_0), as shown in Fig. 3.4. We obtained $\Delta L \sim 0.5\mu m$, which indicates that the effective channel length is longer than the physical channel length (the current path extends beyond the source/drain contact edges), and $R_0 \sim 0\Omega$, which implies a negligible source/drain contact resistance at very high V_{GS} voltages. It should be noticed that although the standard MOSFET equation is used in eq. (3.10) ~ eq. (3.12), the nonlinear factor (γ) can also be included to take into consideration the nonlinearity of I_D-V_{GS}.

3.6 Conclusion

We fabricated inverted-staggered rf magnetron sputtered a-IGZO TFTs on glass substrates. The devices demonstrated good electrical properties: field-effect mobility and threshold voltage extracted by linear fit method yield 10 cm^2/V-s and 3V, respectively, very sharp subthreshold slope 0.4 V/dec, Off-current in the order of 10^{-13}~10^{-12}A, and current On-off ratio exceeding 10^8. The nonlinearity of the transfer characteristics was investigated, and a V_{GS} dependent field-effect mobility was introduced. The source/drain contact resistance examined by the TML method suggests that a good Ohmic contact exists between the source/drain electrodes and a-IGZO active layer. Combining the high performance and the ability for large area deposition, a-IGZO TFTs are very suitable for future flat panel display applications.

CHAPTER IV

Surface Potential Study of Amorphous In-Ga-Zn-O Thin Film Transistors

4.1 Introduction

Scanning Kelvin probe microscopy (SKPM) offers the possibility to measure two-dimensional (2D) electrostatic potential distribution with high spatial resolution, and has been successfully applied to studies of many inorganic/organic semiconductor structures. Arakawa et al. reported on 2D potential distribution of cleaved GaAs HEMTs [71], and observed a potential knee possibly originating from the trapped charge at the epitaxial layer/substrate interface. The current crowding phenomenon was also confirmed to occur at the edge of the drain electrode. Sadewasser et al. obtained the surface work function of chalcopyrite solar cells [72], and observed downward band bending at the grain boundaries due to charged defect states. Recently, an extensive amount of work characterizing the surface potential of organic TFTs has been reported, investigating the charge transport mechanism [73-75], hole density of states [76] contact resistance [77, 78], field-effect mobility [79], and local fluctuation of the surface potential due to inhomogeneities of the organic layer [80, 81]. So far, to the best of our knowledge, the potential profile of working transparent metal-oxide thin-film transistors (TFTs) has not

been reported. In this work we utilize SKPM to map the surface potential in the channel region of amorphous In-Ga-Zn-O (a-IGZO) TFTs with bias voltage. The provided information will be very useful for understanding the device operation principles and for designing higher performance device structures.

4.2 Experimental Setup

Fig. 4.1 shows our experimental setup. We use an Asylum MFP-3D system in noncontact mode to perform SKPM. The system has two feedback loops. The z feedback loop operates as an atomic force microscope (AFM), and generates surface topography images. In the voltage feedback loop, both DC and AC bias signals are applied to the cantilever. Assuming that the electrical interaction between the cantilever tip and the sample can be approximated by two parallel plates, the voltage between can be written as

$$V(t) = V_{DC} + V_{AC}\sin(\omega t) - V_{ch} \tag{4.1}$$

where V_{DC} is the applied DC signal, V_{AC} and ω are the amplitude and frequency of the

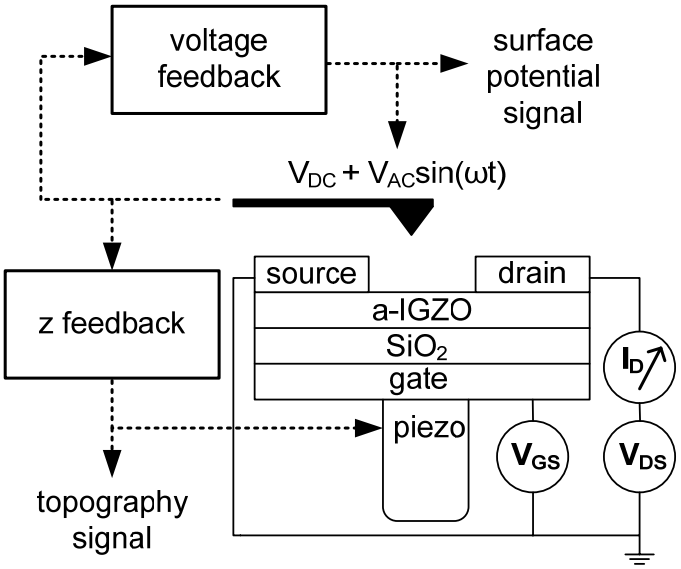

Figure 4.1 Experimental setup used for a-IGZO TFT surface potential measurements.

applied AC signal, and V_{ch} is the surface potential of the sample (TFT back channel). An expression of the electrostatic force between the tip and sample can be derived from (4.1)

$$F(t) = C \cdot V(t)^2/d$$

$$= (C/d) \cdot \left\{ [(V_{DC} - V_{ch})^2 + \frac{1}{2} \cdot V_{AC}{}^2] + 2 \cdot (V_{DC} - V_{ch}) \cdot V_{AC} \sin(\omega t) - \frac{1}{2} \cdot V_{AC}{}^2 \cos(2\omega t) \right\} \quad (4.2)$$

where C is the capacitance, and d is the tip-to-sample spacing. The amplitude of the AC part with frequency ω is zero when $V_{DC} = V_{ch}$, that is, when the applied DC bias signal matches the surface potential. The voltage feedback loop thus varies V_{DC} to zero the ω signal, and the image created from the variation in V_{DC} is the image representing the TFT surface potential. The MFP-3D system utilizes a dual pass technique. During the first pass, topography z(x) is obtained by the non-contact AFM mode. After completing a line, the tip is elevated 300nm above z(x). The same line is scanned again, and the surface potential data is collected during the second pass. It has been shown that if the channel is free of net space charge, then the surface potential closely follows the channel potential in the accumulation layer for TFTs based on unintentionally doped semiconductors [73, 74, 79, 82]. Therefore, we consider that the TFT back channel surface potential measured by SKPM represents the potential profile within the TFT channel.

The a-IGZO TFT used in this study has an inverted-staggered structure. A heavily-doped n-type Si wafer and thermally-oxidized SiO_2 layer (100 nm thick) serve as the gate electrode and gate dielectric, respectively. The a-IGZO active layer (20 nm) was deposited by RF magnetron sputtering at room temperature, and patterned by wet etch. Finally, an Au/Ti stacked film (40nm/5nm) was deposited as source/drain electrodes by electron-beam vapor deposition and patterned by lift-off [37, 83]. The a-IGZO TFT (W/L = 60μm /10μm) transfer and output characteristics are shown in Fig. 2. The device

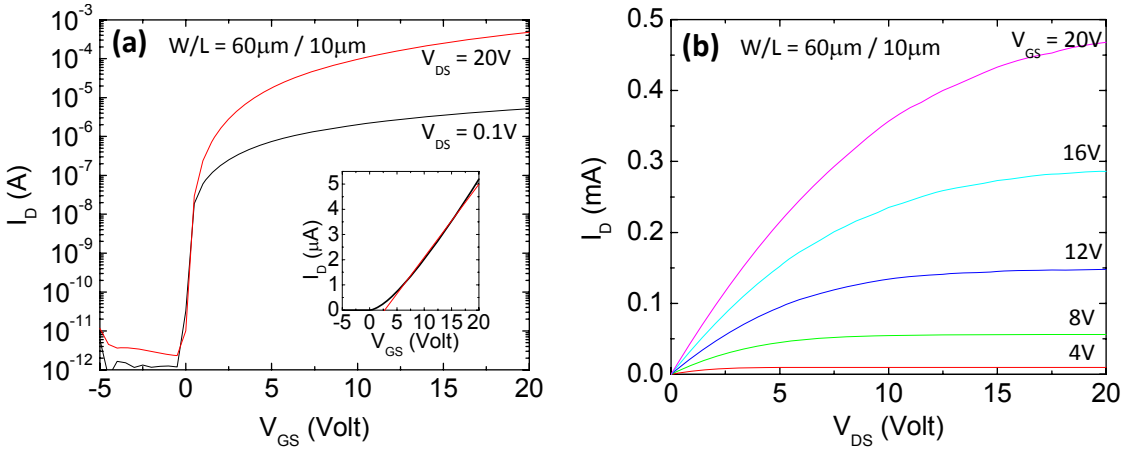

Figure 4.2 Transfer characteristics (a) and output characteristics (b) of a-IGZO TFT.

demonstrated good electrical properties: field-effect mobility and threshold voltage extracted by linear fit method (shown in inset of Fig. 4.2a)yield 12 cm^2/V-s and 3V, respectively, very sharp subthreshold slope 0.15 V/dec, Off-current in the order of 10^{-12}~10^{-11}A, and current On-off ratio exceeding 10^7. The a-IGZO TFT was biased when collecting the topography and surface potential images. The gate was biased by the Asylum MFP-3D system, while the source/drain was biased externally by a Keithley 2400 SourceMeter. The drain current was also measured simultaneously by the Keithley 2400. All instruments were grounded together.

4.3 Surface Potential Measurement Results

Figure 4.3 (a) shows the a-IGZO TFT (W/L = 60µm /10µm) channel region surface topography (z). The channel (x = 5µm ~15µm) between the source and drain electrodes can be clearly seen. Figure 4.3 (b) shows the TFT potential profile (V_{ch}) obtained without bias (V_{GS} = V_{DS} = 0V), and serves as a base line for this experiment (This potential was subtracted from all potential profiles with bias). Figure 4.3 (c) and (d)

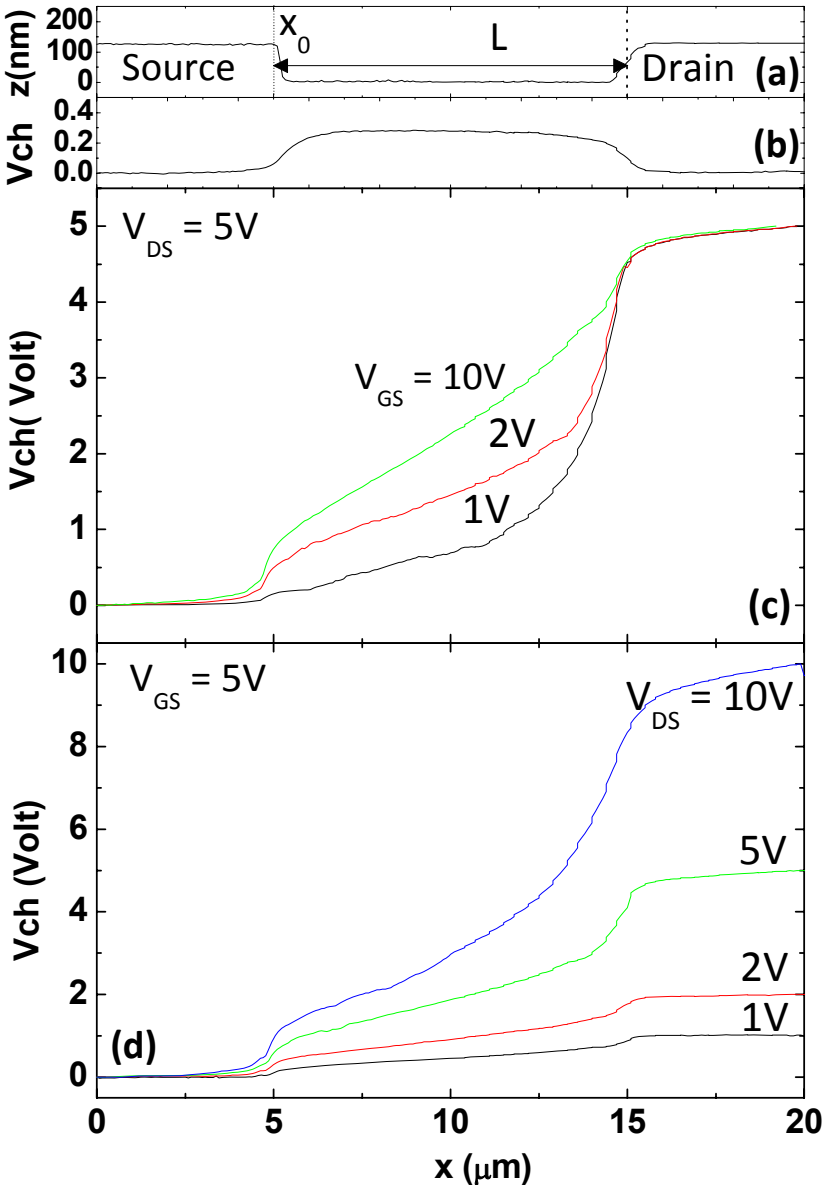

Figure 4.3 a-IGZO TFT surface topography (a), and potential profiles obtained without bias (b), and when V_{DS} = 5V while V_{GS} was increased from 1, 2, to 10V (c), and when V_{GS} = 5V while V_{DS} was increased from 1, 2, 5, to 10V (d).

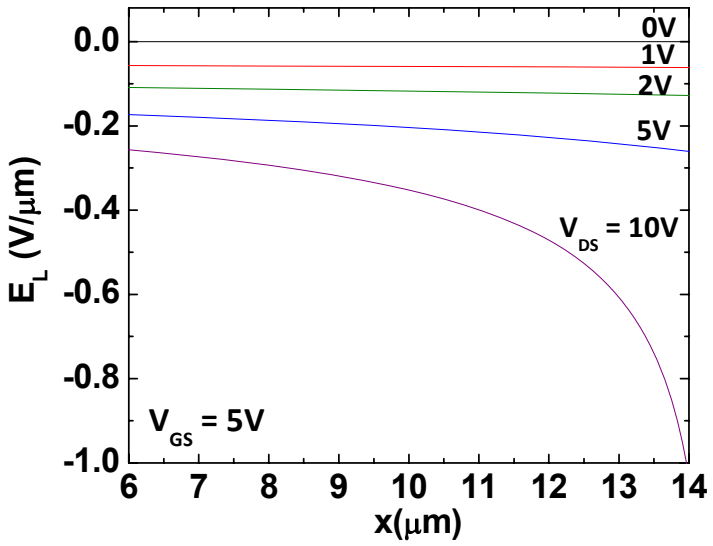

Figure 4.4 Lateral electrical field along the TFT channel.

shows the potential profiles obtained when V_{DS} = 5V while V_{GS} was increased from 1, 2, to 10V, and V_{GS} = 5V while V_{DS} was increased from 1, 2, 5, to 10V, respectively. A sudden rise in potential $V_{S/D}$ at the source/channel and channel/drain interfaces is observed. The source/drain contact resistance $R_{S/D} = (V_S + V_D) / I_D$ is determined to be 28.6 kΩ (V_{DS} = 1V, V_{GS} = 5V, I_D = 7μA), which is consistent with the previously reported contact resistance extracted from the transmission line method ($R_{S/D}$ ~20kΩ, V_{DS} = 0.1V, V_{GS} = 5V, W = 180μm) [84]. Useful information related to the operation principle of a-IGZO TFT can also be studied based on the channel region potential profiles. In the linear regime of TFT operation, a linear increase of potential (V_{ch}) from the source to drain was observed. The potential profile becomes superlinear in the saturation regime, and rises more at the drain end than at the source end. This can be better appreciated when plotting the lateral electric field along the channel, $E_L(x) = -dV_{ch}(x)/dx$, as shown in Fig. 4.4. Notice that the electric field changes rapidly at the

drain end for increasing values of V_{DS}. At the source end, the magnitude of the field increases with V_{DS} for small values of V_{DS} but increases at a slower rate as the TFT enters the saturation regime.

The drain current (I_D) was also measured while collecting the surface potential images and can be described by

$$\begin{aligned} I_D &= W \cdot \mu(x) \cdot Q_{ch}(x) \cdot E_L(x) \\ &= W \cdot C_{ox} \cdot \mu_0 \cdot [V_{GS} - V_T - V_{ch}(x)]^{1+\gamma} \cdot \frac{dV_{ch}(x)}{dx} \end{aligned}$$

$$\Rightarrow I_D \cdot dx = W \cdot C_{ox} \cdot \mu_0 \cdot [V_{GS} - V_T - V_{ch}(x)]^{1+\gamma} \cdot dV_{ch}(x) \tag{4.3}$$

where W is the channel width, C_{ox} is the gate capacitor per unit area, V_T is the TFT threshold voltage, $E_L(x) = - dV_{ch}(x)/dx$ is the lateral electric field along the channel, $[V_{GS} - V_T - V_{ch}(x)] = V_{ox}$ is the potential drop across the gate insulator, and $Q_{ch}(x) = - C_{ox} \cdot [V_{GS} - V_T - V_{ch}(x)]$ is the induced channel charge per unit area. The field-effect mobility $\mu(x) = \mu_0 \cdot [V_{GS} - V_T - V_{ch}(x)]^{\gamma}$ is dependent on V_{ox} where μ_0 is the fitting parameter associated with the field-effect mobility and γ is the nonlinearity factor [83-85]. We can therefore find $V_{ch}(x)$ by integrating equation (4.3) from x_0 to x, where x_0 is the x

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rise at x_0 due to the spurce contact resistance R_S. $I_D \int_{x_0}^{x} dx = W \cdot C_{ox} \cdot \mu_0 \int_{V_{ch}(x_0)}^{V_{ch}(x)} (V_{GS} - V_T - V_{ch})^{1+\gamma} \, dV_{ch}$

$$\Rightarrow I_D = \frac{W \cdot C_{ox} \cdot \mu_0}{(2+\gamma) \cdot (x - x_0)} \cdot \left\{ (V_{GS} - V_T - V_S)^{2+\gamma} - [V_{GS} - V_T - V_{ch}(x)]^{2+\gamma} \right\} \tag{4.4}$$

Solving for $V_{ch}(x)$ yields

(4.5) $$V_{ch}(x) = (V_{GS}\text{-}V_T) - \left[(V_{GS}\text{-}V_T\text{-}V_S)^{2+\gamma} - \frac{(2+\gamma)\cdot I_D \cdot (x\text{-}x_0)}{W \cdot C_{ox} \cdot \mu_0} \right]^{\frac{1}{2+\gamma}}$$

Figure 4.5 shows the calculated $V_{ch}(x)$ using $\mu_0 = 7.7$ cm^2/V$^{1+\gamma}$-s, $\gamma = 0.3$, $V_T \sim 0.6$V, and $x_0 = 5\mu$m. Comparable nonlinear factor values ($\gamma = 0.3\sim0.45$) have been reported for different a-IGZO TFT samples [83-85]. A good fit between the measured and modeled data can be seen, indicating that the standard MOSFET equation incorporated with the nonlinear factor and source/drain contact resistance describes very will the channel potential of a-IGZO TFTs (we failed to model $V_{ch}(x)$ with $\gamma = 0$). Please note that Eq. (4.5) is only valid until the "pinch off" point in the channel where $V_{ch}(x) < V_{GS} - V_T$.

The apparent current-voltage characteristics of a-IGZO TFTs which is constant along the channel (independent of x) can be obtained by integrating equation (4.3) from x_0 to $(x_0 + L)$

(4.6) $$I_D = \frac{W \cdot C_{ox} \cdot \mu_0}{(2+\gamma)\cdot L} \cdot \left[(V_{GS}')^{2+\gamma} - (V_{GS}'\text{-}V_{DS}')^{2+\gamma} \right] \qquad \text{for } V_{DS}' \le V_{GS}'$$

where $V_{GS}' = (V_{GS} - V_T - V_S)$ is the voltage across the gate insulator at the source end of the channel ($x = x_0$), and $V_{DS}' = (V_{DS} - V_D - V_S)$ is the effective drain-to-source voltage.

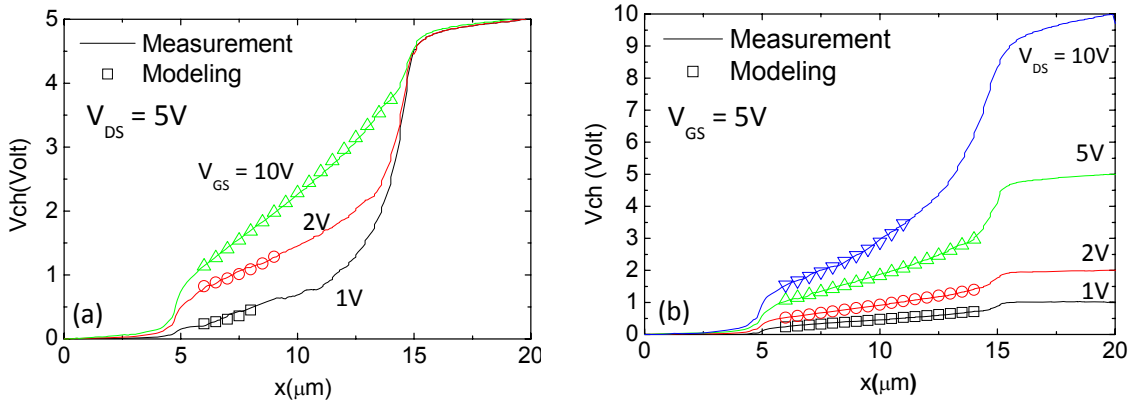

Figure 4.5 Measured (lines) and calculated (symbols) $V_{ch}(x)$

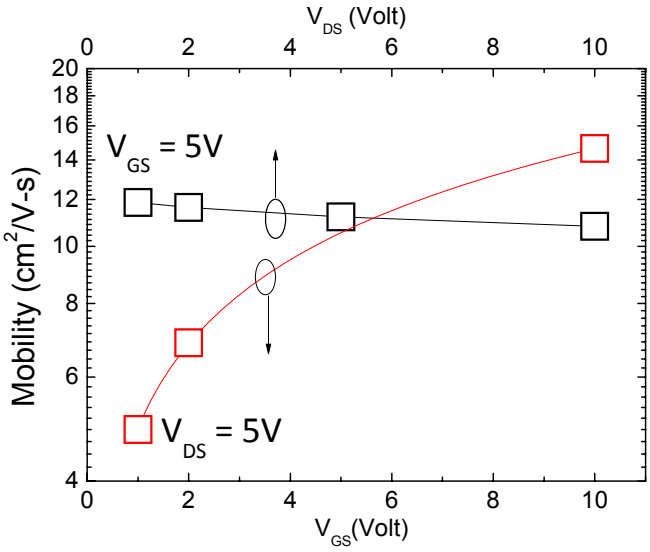

Figure 4.6 The apparent field-effect mobility as a function of V_{GS} and V_{DS}.

In the linear regime at small drain-to-source voltages, eq. (4.6) can be simplified to

$$I_{D\_lin} \cong \frac{W \cdot C_{ox} \cdot \mu_0}{L} \cdot (V_{GS}')^{1+\gamma} \cdot V_{DS}' \qquad \text{for } V_{DS}' << V_{GS}' \tag{4.7}$$

In eq. (4.6) I_D saturates when $V_{DS}' = V_{GS}'$, and can be written as

$$I_{D\_sat} = \frac{W \cdot C_{ox} \cdot \mu_0}{(2+\gamma) \cdot L} \cdot (V_{GS}')^{2+\gamma} \qquad \text{for } V_{DS}' > V_{GS}' \tag{4.8}$$

By comparing eq. (4.7) and (4.8) with the standard MOSFET equation, we can find the apparent field-effect mobility (μ)

$$\mu = \mu_0 \cdot (V_{GS}')^{\gamma} \tag{4.9}$$

Therefore, μ can be calculated by using the parameters (μ_0, γ, V_T and V_S) obtained form the TFT potential profile. Figure 6 summarizes the apparent field-effect mobility as a function of both V_{GS} and V_{DS} extracted from surface potential measurements (symbols: data, line: calculated fit). V_{DS} extracted from surface potential measurements. We can see that μ is mainly affected by V_{GS}, which can be explained by the energy dependent,

density-of localized-states near the Fermi level. As V_{GS} increases, more localized states are filled and more induced charges can contribute to the free carriers [68]. Similar V_{GS} dependent field-effect mobility was extracted from a-IGZO TFT transfer characteristics using the gamma method [84, 85]. We also observe that μ slightly decreases with V_{DS} due to the non-negligible source contact resistance R_S. When the drain current I_D increases with V_{DS}, $V_S = R_S \cdot I_D$ also increases, and therefore reduces the voltage drop across the gate insulator, which can be seen as a smaller effective V_{GS}.

4.4 Conclusion

Surface potential of a-IGZO TFT channel region was studied by performing scanning Kelvin probe microscopy. The device was biased during the measurement, and the effect of V_{GS} and V_{DS} on the channel potential profile $V_{ch}(x)$ was discussed. In the linear region, a linear increase in $V_{ch}(x)$ was observed, while in the saturation region, the potential rises more near the drain end. The source/drain contact resistance $R_{S/D} \sim 28$ kΩ was extracted from the sudden potential rise $V_{S/D}$ at the source/channel and channel/drain interfaces, and agrees with the previously reported value extracted from the transmission line method. The effect of the V_{GS} dependent mobility and source/drain contact resistance was included in the standard MOSFET equation to fit our measured $V_{ch}(x)$. The good agreement between measured and calculated data establishes a good description of operation principles in a-IGZO TFTs. The field-effect mobility (μ) extracted from the surface potential profile increases with V_{GS}, which can be explained by the V_{GS} dependent trapped charges and free carriers. μ also slightly decreases with V_{DS} due to the increased I_D which causes a larger potential drop at the source/channel interface, therefore, making the effective V_{GS} smaller.

CHAPTER V

Temperature Dependent Study of Amorphous In-Ga-Zn-O Thin Film Transistors

5.1 Introduction

In the previous chapter, we presented a-IGZO TFTs with high electrical performance, including decent field-effect mobilities, large current on-off ratios and sharp subthreshold swings. All these device parameters are highly dependent on the density of localized gap states (DOS) of a-IGZO. Knowledge of these states is essential for fundamental understanding and improving the material's electrical properties. So far, DOS of a-IGZO has been widely studied by 2-D device simulations [86], capacitance-voltage (CV) analyses [87], hard X-ray photoemission (HX-PES) [88], optical measurements [45, 46], and first principle calculations based on the density function theory (DFT) [43, 45, 46]. All these investigations have revealed that the DOS of a-IGZO is smaller than that of hydrogenated amorphous silicon (a-Si:H), resulting in sharper subthreshold swings and lower operation voltages. In this chapter, we study the temperature effect on a-IGZO TFTs, and calculate the DOS based on the temperature dependent field-effect measurements. Similar approach has been used to determine the DOS of a-Si:H [89, 90], and has been proven that this method can provide meaningful information of the DOS with high reliability.

5.2 Temperature Dependent Field-Effect Measurements

5.2.1 Experimental

Temperature dependent field-effect measurements were performed on inverted-staggered rf magnetron sputtered a-IGZO TFTs. The fabrication of these devices was discussed in chapter II. Measurements were done in air and in dark using a Hewlett-Packard 4156A semiconductor parameter analyzer controlled by ICS Metrics software. The device temperature was regulated by a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Before each measurement, the TFTs were placed on the heated chuck which is set at the desired measurement temperature for 30min to allow for thermal equilibrium.

5.2.2 Temperature Effect on a-IGZO TFTs

We measured the drain current (I_D) versus the gate-to-source voltage (V_{GS}) at different temperatures ranging from 20°C to 80°C, as shown in Fig. 5.1 (drain-to-source voltage (V_{DS}) = 0.1V). The TFT parameters as a function of temperature are shown in Fig. 5.2. The field-effect mobility (μ) and threshold voltage (V_T) were extracted by using the standard MOSFET equation

$$I_D = \frac{W}{L} \cdot C_{ox} \cdot \mu \cdot (V_{GS} - V_T) \cdot V_{DS} \tag{5.1}$$

where W and L are the channel width and channel length, respectively, and C_{ox} is the gate insulator capacitance per unit area. To accommodate for the nonlinearity of the I_D-V_{GS} curve, a fitting range between 10% and 90% of the maximum measured I_D is chosen. From Fig. 5.2 (a) we can see that as the temperature rises from 20°C to 80°C, the field-effect mobility (μ) is weakly thermally activated, and increases from 9 to 11cm^2/V-s with

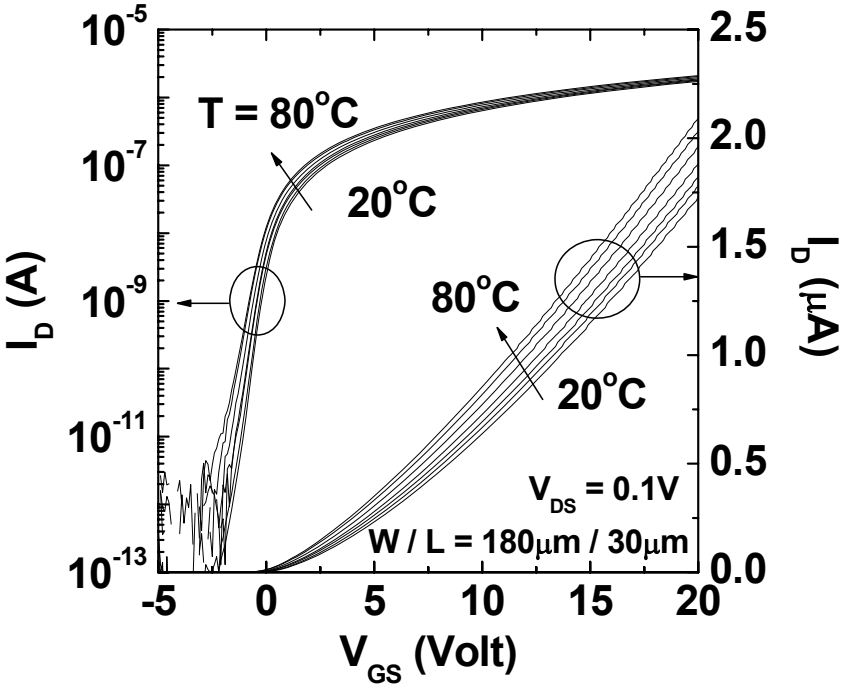

Figure 5.1 a-IGZO TFT transfer characteristics (I_D-V_{GS}) measured at various temperatures ranging from 20°C to 80°C.

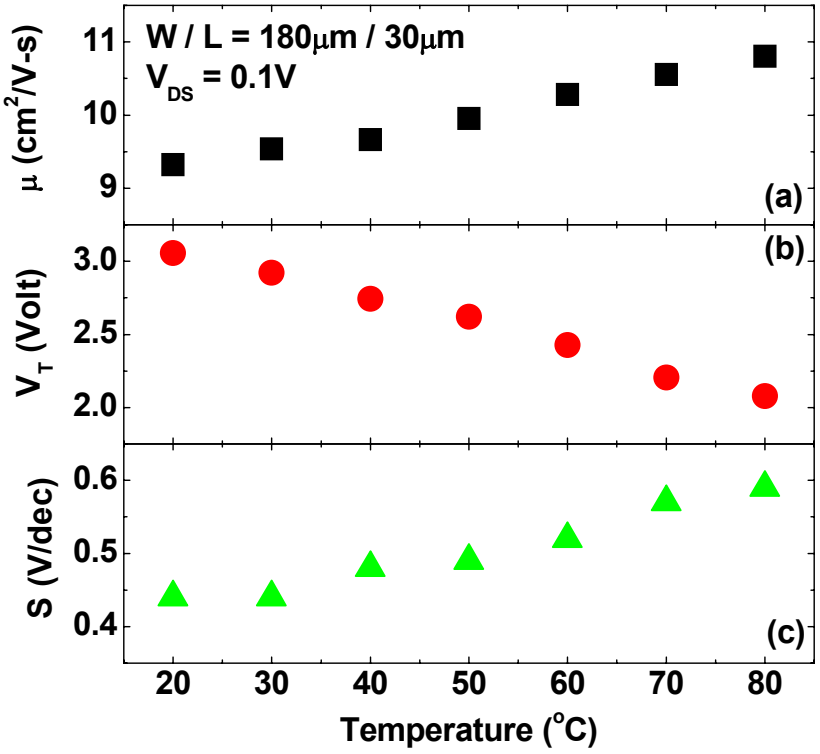

Figure 5.2 Temperature dependence of the (a) field-effect mobility, (b) threshold voltage, and (c) subthreshold slope of a-IGZO TFTs.

a very low activation energy(E_{a_μ}) 26meV. Fig. 5.2 (b) shows that the threshold voltage (V_T) linearly decreases with temperature (from 3 to 2V) with a temperature coefficient (K_{VT}) -17mV/°C. The temperature dependence of μ and V_T are similar to what we commonly observed from a-Si:H TFTs [91, 92], which can be explained by the multiple trapping model described by LeComber and Spear [93]: at higher temperatures, more electrons can escape from the localized states and contribute to the free carriers, which causes a higher mobility and smaller threshold voltage. The field-effect mobility and threshold voltage of a-IGZO TFTs are less sensitive to temperature compared to those of a-Si:H TFTs (E_{a_μ} ~60meV, K_{VT} ~ -36 mV/°C) [91].

The subthreshold slope (S) is extracted at the steepest point of the $\log(I_D)$-V_{GS} plot by using the following equation

$$S = \left(\frac{d\log(I_D)}{dV_{GS}} \right)^{-1} \tag{5.2}$$

From Fig. 5.2 (c) we can see that subthreshold slope (S) slightly increases with temperature from 0.4 to 0.6 /dec. We can also observe from Fig. 5.1 that the off-current (I_{OFF}) almost remained the same (10^{-12}~10^{-13}A) within the investigated temperature range. This stable operation even at elevated temperature makes a-IGZO TFTs favorable for future FPD applications, which is very different from a-Si:H TFTs, where the S and I_{OFF} are very sensitive to temperature [94].

5.2.3 Meyer-Neldel Rule

We observed that the drain current is thermally activated and can be described by

$$I_D = I_{D0} \cdot \exp(-E_a / kT) \tag{5.3}$$

where I_{D0} is the prefactor, E_a is the activation energy, k is the Boltzmann constant and T

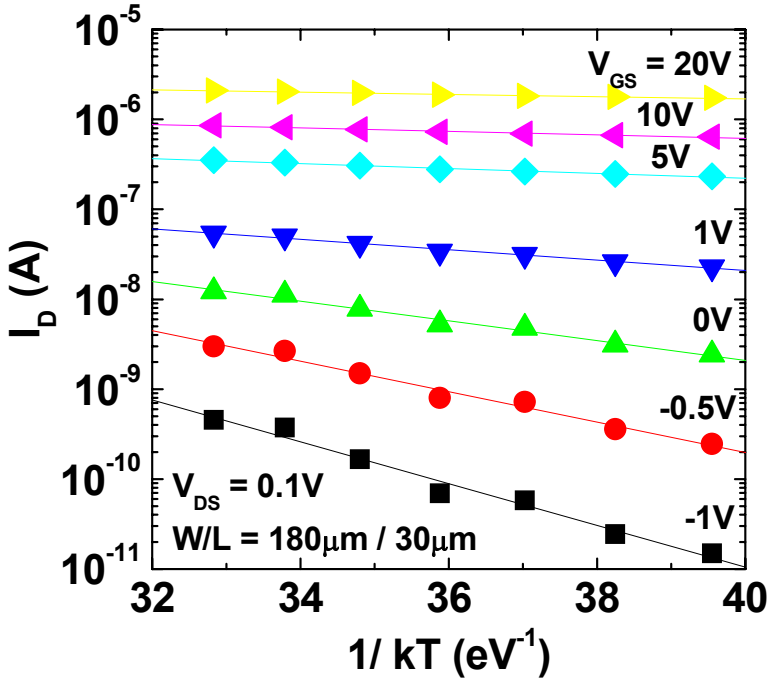

Figure 5.3 Temperature dependence of the drain current in the subthreshold regime (Vgs < 1V) (a), and the above threshold regime (Vgs > 1V) (b). Scatter dots represent the measured data; lines are used to extract Ea.

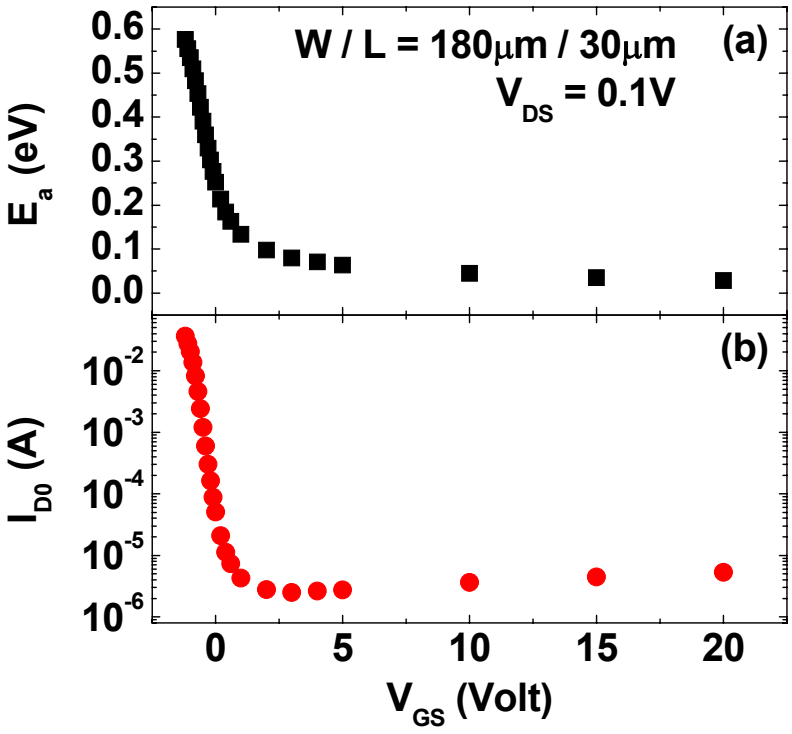

Figure 5.4 Activation energy (E_a) (a) and prefactor (I_{D0}) (b) as a function of V_{GS}.

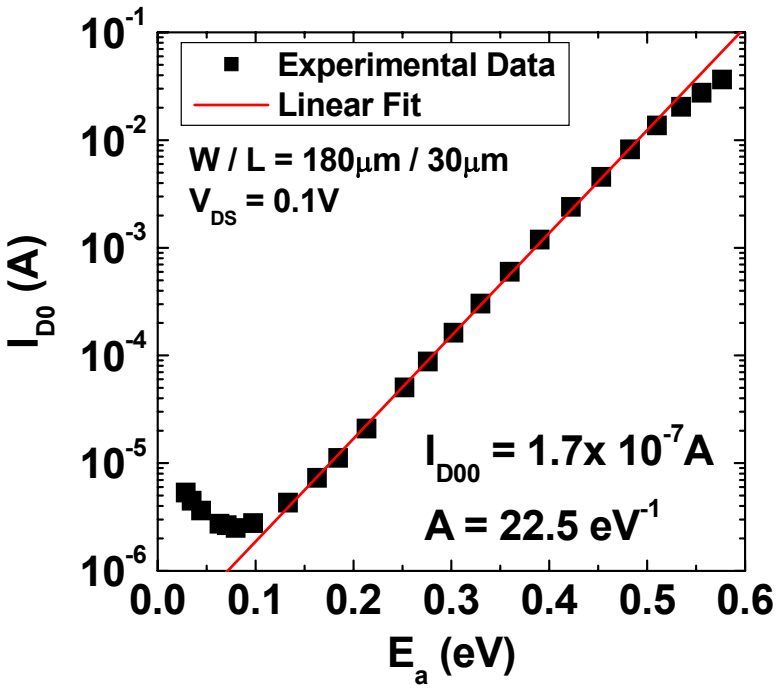

Figure 5.5 Prefactor (I_{D0}) versus activation energy (E_a). Their relation can be expressed as $I_{D0} = I_{D00} \exp(A \cdot E_a)$. A is observed to be ~ 22.5eV^{-1} in the subthreshold regime, and ~ 0 eV^{-1} in the above threshold regime.

is the temperature. I_{D0} and E_a can be easily extracted by plotting log(I_D) vs. 1/kT, as shown in Fig. 5.3. Both I_{D0} and E_a are V_{GS} dependent (shown in Fig. 5.4), and their relation obeys the Meyer-Neldel rule [95]

$$I_{D0} = I_{D00} \cdot \exp(A \cdot E_a) \tag{5.4}$$

where A is the Meyer-Neldel (MN) parameter. The Meyer-Neldel rule in generally considered to be an intrinsic property of a material, and is reported to be applicable whenever the Fermi level position is varied, regardless of whether this shift is caused by introducing extra defect states to the sample or as in this case, by applying an electric field [90]. For our a-IGZO TFTs, as shown in Fig. 5.5, A is observed to be a constant (~22.5 eV^{-1}) over a broad range of activation energies between 0.15 and 0.5 eV, which corresponds to the subthreshold regime (V_{GS} = -1 V to 1 V). On the other hand, in the

above threshold regime (V_{GS} > 1 V) where the activation energy is smaller than 0.1 eV, A decreases to a value close to zero. At even lower activation energy values (< 0.05eV), which corresponds to V_{GS} > 5V, A becomes negative.

5.3 Density of States Calculation

5.3.1 Method of Analysis

The drain current (I_D), as a function of V_{GS}, can be derived from (5.3) and (5.4)

$$I_D(V_{GS}) = I_{D00} \cdot \exp[(A - \beta) \cdot E_a(V_{GS})] \tag{5.5}$$

where $\beta = 1/kT$. Fig. 5.6 shows the energy band diagram near the semiconductor-insulator interface. The activation energy E_a is the energy difference between the Fermi level (E_F) and the edge of the conduction band (E_C), which equates to the average energy a trapped electron needs to gain in order to escape from the localized state [96]. As we can see from Fig. 5.6, E_a is not only a function of V_{GS}, but also a function of x (the distance measured from the insulator-semiconductor interface). Therefore, the activation energy extracted from log(I_D) vs. 1/kT (shown in Fig. 5.4) can be seen as the "average effect" on I_D caused by $E_a(x)$ at a particular V_{GS} level. We can then rewrite (5.5) as

$$I_D(V_{GS}) = \frac{I_{D00}}{d_s} \cdot \int_0^{d_s} \exp[(A - \beta) \cdot E_a(x)]dx \tag{5.6}$$

where d_s is the thickness of the a-IGZO semiconductor layer. As shown in Fig. 5.6, $E_a(x)$ can also be written as $E_{aFB} - y(x)$, where E_{aFB} is the activation energy under flat band condition, and y(x) is the band bending (measured in eV) caused by V_{GS} larger than the flat band voltage (V_{FB}). The drain current I_D can thus be expressed as a function of y(x)

$$I_D(V_{GS}) = \frac{I_{FB}}{d_s} \cdot \int_0^{d_s} \exp[(\beta - A) \cdot y(x)]dx \tag{5.7}$$

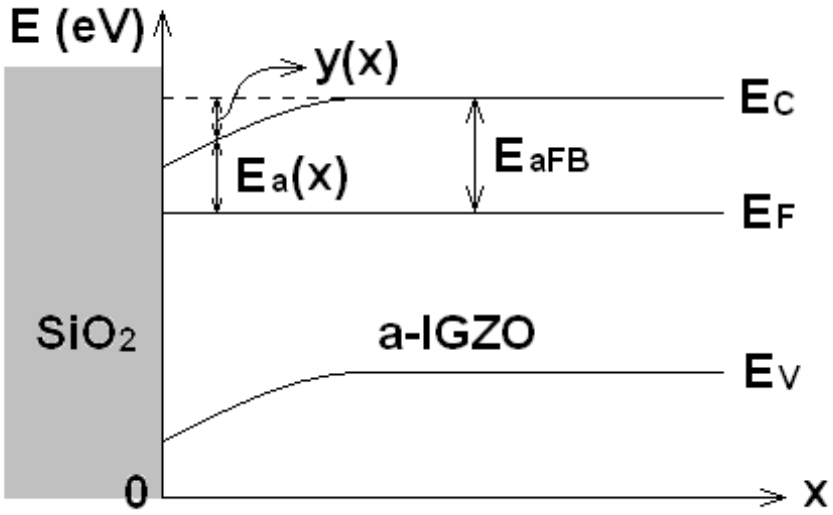

Figure 5.6 Energy band diagram of an a-IGZO TFT near the semiconductor-insulator interface.

where

(5.8) $$I_{FB} = I_{D00} \cdot \exp[(A - \beta) \cdot E_{aFB}]$$

To determine the charge density (n) and the amount of band bending inside the semiconductor, Poisson equation needs to be solved for the electric field, which is related to the applied gate voltage. The Poisson equation is given by

(5.9) $$\frac{d^2y(x)}{dx^2} = \frac{e \cdot n(y)}{k_s \cdot \varepsilon_0}$$

where e is the absolute value of the electronic charge, k_s is the dielectric constant of the semiconductor (a-IGZO), and ε_0 is the permittivity of free space. The electric field (E) inside the semiconductor

(5.10) $$E(x) = -\frac{dy(x)}{dx}$$

can be solved by multiplying both sides of (9) by 2 dy(x)/dx and then integral over x. Together with the boundary conditions $y(d_s) = dy(d_s)/dx = 0$, dy(x)/dx can be solved.

$$\int_{d_s}^{x} 2\cdot\frac{dy}{dx}\cdot\frac{d^2y}{dx^2}\,dx = \int_{d_s}^{x}\frac{d}{dx}\left(\frac{dy}{dx}\right)^2 dx = \int_{d_s}^{x} d\left(\frac{dy}{dx}\right)^2 = \left(\frac{dy(x)}{dx}\right)^2$$

(5.11)

$$\int_{d_s}^{x}\frac{2\cdot e}{k_s\cdot\varepsilon_0}\cdot\frac{dy}{dx}\cdot n(y)\,dx = \frac{2\cdot e}{k_s\cdot\varepsilon_0}\int_0^{y(x)} n(y)\,dy$$

$$\Rightarrow\quad \frac{dy(x)}{dx} = -\left(\frac{2\cdot e}{k_s\cdot\varepsilon_0}\int_0^{y(x)} n(y)\,dy\right)^{1/2}$$

The negative sign is to make the field in the correct direction. Another boundary condition is required to solve the relation between the electric field and the applied gate bias.

(5.12)

$$k_s\cdot E(0^+) = -\,k_s\cdot\frac{dy(0^+)}{dx} = k_{ins}\cdot\frac{V_{GS} - V_{FB} - y(0^+)}{d_{ins}}$$

where k_{ins} and d_{ins} are the dielectric constant and thickness of the gate insulator, respectively. To simplify the calculation, we assume that y(0) is much smaller than V_{GS} - V_{FB}. Using (5.11) and (5.12), the applied gate bias can be solved as

(5.13)

$$V_{GS} - V_{FB} \equiv V_F = -\frac{k_s\cdot d_{ins}}{k_{ins}}\cdot\frac{dy(0^+)}{dx}$$

$$= \frac{k_s\cdot d_{ins}}{k_{ins}}\cdot\left(\frac{2\cdot e}{k_s\cdot\varepsilon_0}\int_0^{y_s} n(y)\,dy\right)^{1/2}$$

where $y_s = y(0^+)$, and

(5.14)

$$\frac{dV_F}{dy_s} = \frac{k_s\cdot d_{ins}}{k_{ins}}\cdot\left(\frac{e}{2\cdot k_s\cdot\varepsilon_0}\right)^{1/2}\cdot\left(\int_0^{y_s} n(y)\,dy\right)^{-1/2}\cdot n(y_s)$$

Using (5.11), we can now transform (5.7) into an integral over y

(5.15)

$$\frac{I_D - I_{FB}}{I_{FB}} = \frac{1}{d_s}\cdot\int_0^{d_s}\{\exp[(\beta - A)\cdot y(x)] - 1\}\,dx$$

$$= \frac{1}{d_s}\cdot\int_0^{y_s}\frac{\exp[(\beta - A)\cdot y(x)] - 1}{\left(\frac{2\cdot e}{k_s\cdot\varepsilon_0}\int_0^{y(x)} n(y)\,dy\right)^{1/2}}\,dy$$

The charge density can be solved by differentiating (5.15) with respect to V_F and using (5.14)

$$\frac{1}{I_{FB}}\cdot\frac{dI_D}{dV_F} = \frac{1}{d_s}\cdot\frac{\exp[(\beta - A)\cdot y_s] - 1}{\left(\frac{2\cdot e}{k_s\cdot\varepsilon_0}\int_0^{y_s} n(y)\,dy\right)^{1/2}}\cdot\frac{dy_s}{dV_F}$$

$$= \frac{\exp[(\beta - A)\cdot y_s] - 1}{\left(\frac{k_s\cdot d_{ins}}{k_{ins}}\right)\cdot d_s\cdot\left(\frac{e}{k_s\cdot\varepsilon_0}\right)\cdot n(y_s)} \qquad (5.16)$$

$$\Rightarrow n(y_s) = \frac{k_{ins}\cdot\varepsilon_0}{e\cdot d_{ins}\cdot d_s}\cdot\frac{I_{FB}\cdot\{\exp[(\beta - A)\cdot y_s] - 1\}}{dI_D/dV_F}$$

Now we can obtain $y_s(V_F)$ from plugging (5.16) into (5.14) and using (5.13)

$$\frac{dy_s}{dV_F} = \frac{k_{ins}}{k_s\cdot d_{ins}}\cdot\frac{V_F}{I_{FB}}\cdot\frac{dI_D}{dV_F}\cdot\frac{1}{\exp[(\beta - A)\cdot y_s] - 1} \qquad (5.17)$$

Integrating (5.17) immediately yields

$$\exp[(\beta\text{-}A)\cdot y_S(V_F)] - (\beta\text{-}A)\cdot y_S(V_F) - 1$$
$$= \frac{\beta\text{-}A}{I_{FB}}\cdot\frac{d_s}{d_{ins}}\cdot\frac{k_{ins}}{k_s}\cdot[V_F\cdot I_D(V_F) - \int_0^{V_F} I_D(V_F')\,dV_F'] \qquad (5.18)$$

Using (5.18) we can calculate the amount of band bending at the semiconductor-insulator interface $y_s(V_F)$ from experimental data $I_D(V_F)$ measured at a single temperature (in this case, 20°C). Then the charge density $n(y_s)$ is obtained from (5.16). An example of the calculated $y_s(V_F)$ and $n(y_s)$ is illustrated in Fig. 5.7. The method to determine the appropriate flat band voltage (V_{FB}) will be discussed in the next section. Finally, the DOS function N(E) is calculated from

$$N(E) = \left|\frac{dn(y_s)}{dy_s}\right|_{y_s=E} \qquad (5.19)$$

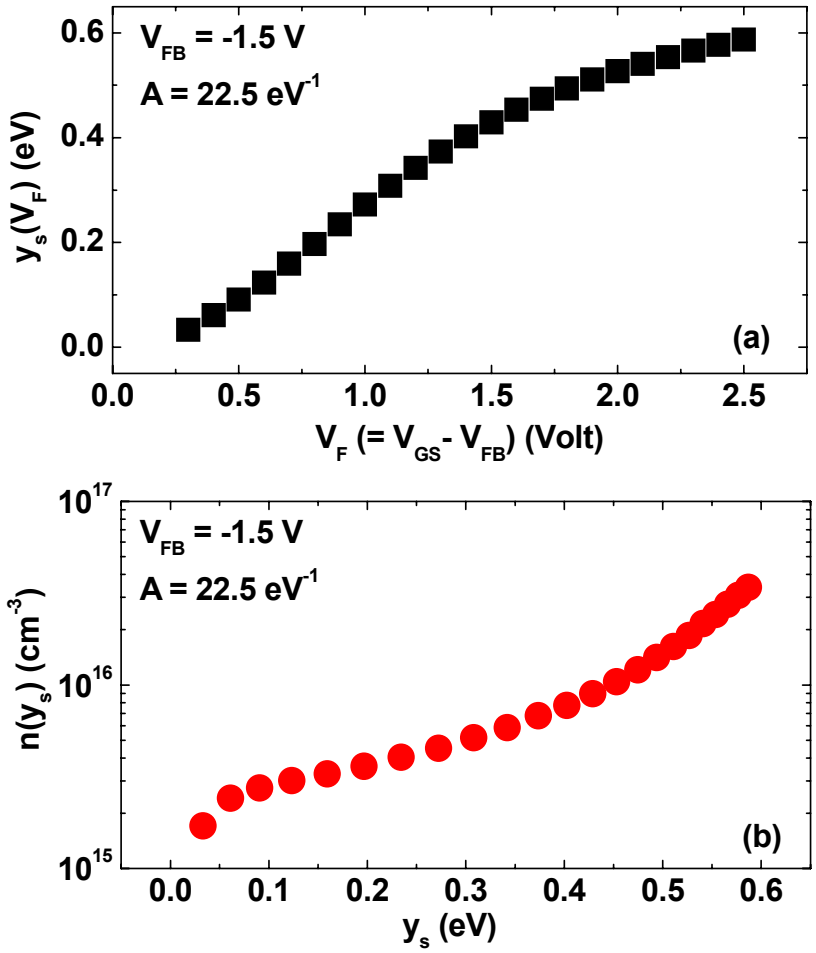

Figure 5.7 Calculated (a) band bending at the semiconductor-insulator interface (y_s) as a function of V_F ($=V_{GS}-V_{FB}$) and (b) induced charge density (n) as a function of y_s.

Here, we assume that most induced charge is localized and 0 K Fermi statistics is applicable for the occupancy of the localized states. The biggest advantage of using 0 K Fermi statistics is that N(E) can be easily calculated from $n(y_s)$ by differentiation. 0 K approximation of Fermi statistics is valid when the characteristic energy of N(E) is much higher than the measurement temperature (25meV at 20°C). This requirement can be checked by observing the calculated DOS profile. Although finer structures of the DOS can be obtained when finite temperature statistics is used, assuming a 0 K Fermi statistics is good enough for estimating the order of N(E).

5.3.2 Calculated Density of States

We calculated the DOS separately in the subthreshold and above threshold regimes of the a-IGZO TFT, as shown in Fig. 5.8, since the two regimes exhibit different Meyer-Neldel relations. The calculated a-IGZO DOS from the subthreshold regime (deep states) appears to be low ($<10^{18}$ $eV^{-1}cm^{-3}$) with a characteristic energy of about 120 meV. This agrees with the density of deep states profile extracted from a-IGZO TFT SPICE simulations, as shown in Fig. 5.8, where the RPI a-Si:H TFT model was used, and the DOS variation was assumed to be exponential with energy [97]. It also agrees with the maximum density of deep bulk states $N_{BS\_max} = 4.28\times10^{16}$ $cm^{-3}eV^{-1}$ extracted from the TFT subthreshold slope in Chapter III. The DOS calculated from the above threshold regime (tail states) is larger and has a steeper slope with a characteristic energy of about 30 meV, which is very close to the value extracted from the V_{GS} dependent field-effect mobility in Chapter III: $\gamma = 0.43$, $T_0 = 365$ K (31meV). However, the validation of the DOS calculated from the above threshold regime can be questioned for the following two reasons, which also apply to a-Si:H TFTs: (i) the free carriers can no longer be ignored in (5.19), and (ii) the characteristic energy is very close to the measurement temperature, therefore using 0 K Fermi statistics might lead to certain amount of error. Recognizing these limitations, we argue that the investigation of the effect of the MN parameter on the DOS profile still provides insight into the fundamental understanding of the material's electrical property.

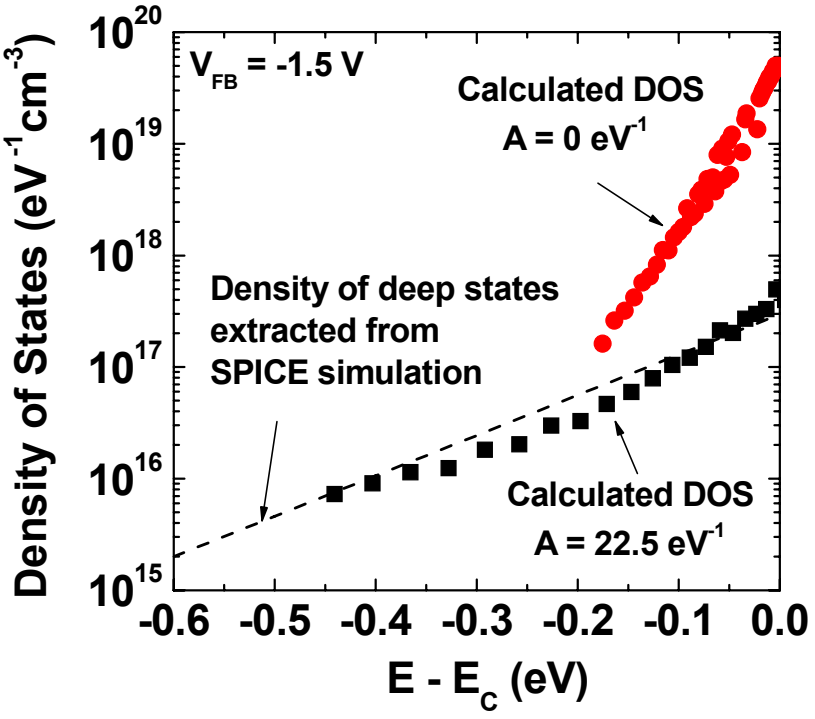

Figure 5.8 Calculated density of states (DOS) from both the subthreshold regime and above threshold regime as a function of E-E_C, V_{FB} = -1.5V were used.

5.3.3 Determination of the Flat Band Voltage

The calculation procedure described in this paper requires knowledge of the flat band voltage (V_{FB}). Using improper values of V_{FB} would lead to incorrect DOS. To determine the correct values of V_{FB}, we theoretically calculate the activation energy E_a as a function of V_{GS}. From (5.3), we can obtain

$$E_a(V_{GS}) = -\frac{1}{I_D(V_{GS})} \cdot \frac{dI_D(V_{GS})}{d\beta} \tag{5.20}$$

where $dI_D(V_{GS})/d\beta$ can be calculated from (5.15)

$$\frac{dI_D(V_{GS})}{d\beta} = \frac{I_D(V_{GS})}{I_{FB}} \cdot \frac{dI_{FB}}{d\beta} + \frac{I_{FB}}{d_s} \cdot \left(\frac{k_s \cdot \varepsilon_0}{e}\right)^{1/2} \cdot \int_0^{y_s} \frac{y \cdot \exp[(\beta - A) \cdot y]}{\sqrt{2 \cdot \int_0^{y} n(y')dy'}}\, dy \tag{5.21}$$

Here we assume that the dependence of both n and y on β can be neglected in the scope of this analysis, meaning that at any temperature (in the investigated range) most induced charge is localized, and that the shift of the Fermi level with temperature is negligibly small [90]. By plugging (5.21) into (5.20) we obtain,

$$E_a(V_{GS}) = E_{aFB} - \frac{I_{FB}}{I_D(V_{GS})\cdot d_s}\cdot\left(\frac{k_s\cdot\varepsilon_o}{e}\right)^{1/2} \cdot\int_0^{y_s}\frac{y\cdot\exp[(\beta\text{-}A)\cdot y]}{\sqrt{2\cdot\int_0^{y} n(y')dy'}}\,dy \tag{5.22}$$

where

$$E_{aFB} = -\frac{1}{I_{FB}}\cdot\frac{dI_{FB}}{d\beta} \tag{5.23}$$

The activation energy can thus be calculated from experimental data $I_D(V_{GS})$ measured at a single temperature (in this case, 20°C) using any desired V_{FB}. A proper V_{FB} value can be obtained by matching the calculated E_a with the E_a extracted from temperature dependent field effect measurements. In order to check the consistency, the prefactor I_{D0} is calculated as a function of E_a from

$$I_{D0}(V_{GS}) = I_D(V_{GS})\cdot\exp[\beta\cdot E_a(V_{GS})] \tag{5.24}$$

using measured $I_D(V_{GS})$ data and calculated $E_a(V_{GS})$ values. The best fit of the theoretical calculations to the measured data is shown in Fig. 5.9 and Fig. 5.10 with V_{FB} = -1.5V, E_{aFB} = 0.6V, and A = 22.5eV^{-1} and 0eV^{-1} in the subthreshold regime and the above threshold regime, respectively.

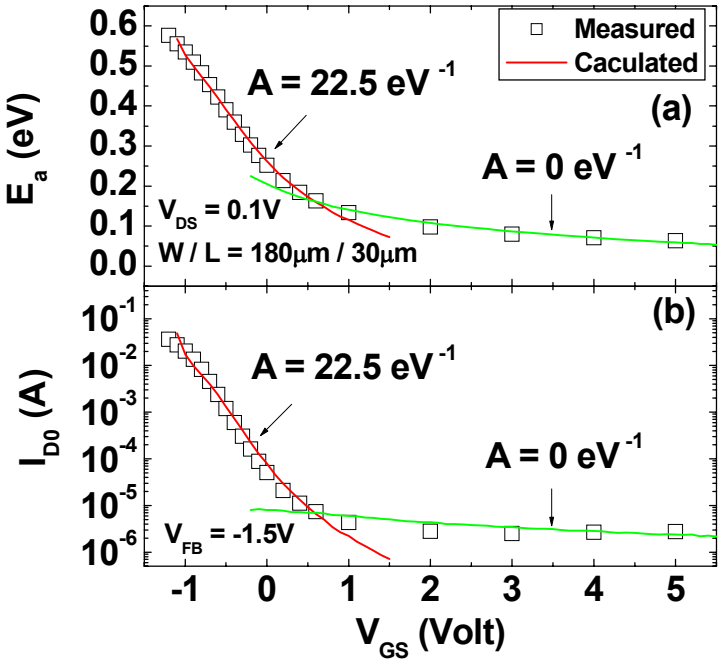

Figure 5.9 Calculated and measured (a) activation energy (E_a) and (b) prefactor (I_{D0}). By using different Meyer-Neldel parameters (A) in the subthreshold and above threshold regimes, we were able to match the calculated E_a and I_{D0} with the experimental data.

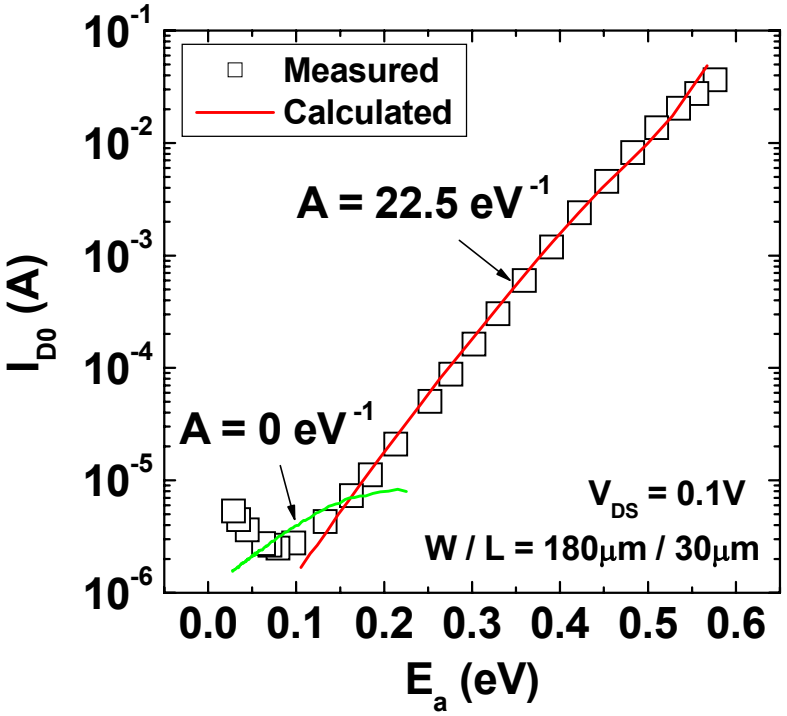

Figure 5.10 Measured and calculated prefactor as a function of activation energy.

5.4 Conclusion

We investigated the effect of temperature on rf magnetron sputtered a-IGZO TFTs. The field effect mobility is weakly thermally activated (activation energy ~ 26meV). The threshold voltage linearly decreases with temperature with a temperature coefficient of -17mV/^{o}C. The current On-Off ratio and subthreshold slope almost remained the same within the investigated temperature range. The density of states of rf magnetron sputtered a-IGZO was calculated by a straight forward method based on temperature dependent field effect measurements. The Meyer-Neldel (MN) rule was also taken into account during the calculation. The appropriate flat band voltage and MN parameter were obtained by matching the calculated activation energy with the measured data. The calculated DOS from the subthreshold regime is low ($<10^{18}$ $eV^{-1}cm^{-3}$) with a characteristic energy of ~120meV, and shows good agreement with the density of deep states extracted from SPICE simulations, and with the maximum density of deep bulk states $N_{BS\_max} = 4.28\times10^{16}$ $cm^{-3}eV^{-1}$ extracted from the TFT subthreshold slope. We believe that this method provides a simple and fast interpretation of the field effect measurements and gives us a good image of the DOS profile. More accurate results can be obtained by considering the free charge in (5.19), and calculating the DOS by deconvolution of the localized charge with the Fermi-Dirac distribution function. The order of magnitude of the a-IGZO DOS extracted from temperature field-effect measurements agrees with that extracted from CV measurements [87], and are smaller compare to that of a-Si [98], which can explain the superior electrical properties including higher field-effect mobility and sharper subthreshold slope.

CHAPTER VI

Current Temperature Stress Study of Amorphous In-Ga-Zn-O Thin Film Transistors

6.1 Introduction

The TFT long term reliability is a critical issue, especially in certain applications such as AMOLEDs, where the drive TFT constantly supplies a current to the organic light-emitting diode (OLED) instead of just acting like a switch. Studies investigating the electrical stability of a-IGZO TFTs have been reported [39, 40, 99-102]. A parallel shift in TFT transfer characteristics when subject to bias/current stress is commonly observed, and several possible degradation mechanisms have been proposed. Nomura et al. suggested that shallow traps are the origin of subthreshold slope deterioration and large (>10V) threshold voltage shifts (ΔV_T) observed in unannealed devices, while deep charged traps which cannot be removed by annealing are responsible for small ΔV_T (~1V) [102]. On the other hand, Lee et al. [39] and Suresh et al. [40] attributed the instability to charge trapping in the channel/dielectric interface or in the bulk dielectric layer. In this chapter we study the electrical stability of inverted-staggered rf magnetron sputtered a-IGZO TFTs by performing current temperature stress (CTS) measurements, and investigate factors affecting the CTS including stress time, stress current, stress temperature, and TFT biasing conditions.

6.2 Current Temperature Stress Measurement Setup

Current temperature stress (CTS) measurements were performed on inverted-staggered rf magnetron sputtered a-IGZO TFTs. The fabrication of the devices was discussed in chapter II. The measurements were done in air and in dark using a Hewlett-Packard 4156A semiconductor parameter analyzer controlled by ICS Metrics software. The device temperature was regulated by a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Before each measurement, the TFTs were placed on the heated chuck which is set at the desired measurement temperature for 30min to allow for thermal equilibrium.

We used two different stress schemes for the CTS measurements: CTS_lin and CTS_sat [92]. CTS_lin and CTS_sat are equivalent to operating the TFT in the linear and saturation regime, respectively. For CTS_lin, during the stress mode, the gate was biased at 20V while a stress current (I_{STR}) was applied to the drain of the TFT, as shown in Fig. 6.1(a). The same TFT were stressed for a total stress time (t_{STR}) of 10000s, as illustrated in Fig. 6.2. At certain times (t_{STR} = 100s, 200s, 500s, 1000s, 2000s, 4000s, 6000s, 8000s, and 10000s), the stress mode was interrupted and switched to the sweep mode where a quick gate voltage sweep (V_{GS} = -5 →20V) was applied to measure the transfer characteristic in the saturation regime of operation (V_{DS} = 20V). For CTS_sat, during the stress mode, the gate and drain were externally shorted together, and I_{STR} was applied to the drain, setting the voltages at the gate/drain (V_{GS} = V_{DS}), as shown in Fig. 6.1(b). The total stress time and number of points when the stress mode was interrupted are the same as CTS_linear. In the sweep mode, the gate/drain voltages (V_{GS} = V_{DS}) were swept from -5 to 20V to measure the transfer characteristics in the saturation regime. The same

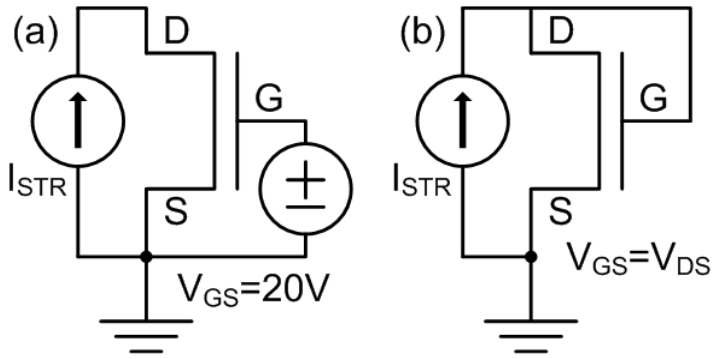

Figure 6.1 The two CTS measurement setups (stress mode) used in this study (a) CTS_lin (V_{GS} = 20V) and (b) CTS_sat (V_{GS} = V_{DS})

Table 6.1 CTS conditions used in this study

	Stress mode	Sweep mode	I_{STR} (μA)	T_{STR} (°C)
CTS_lin	I_D = I_{STR} V_{GS} = 20V V_{DS}*	V_{GS} = -5→20V V_{DS} = 20V	10	40, 50, 60, 70, 80
			1, 10, 40, 100	60
CTS_sat	I_D = I_{STR} V_{DS} =V_{GS}**	V_{GS} = V_{DS} = -5→20V	100	40, 50, 60, 70, 80
			40, 60, 80, 100	60

* V_{DS} increases with ΔV_T during the stress mode.
** V_{DS} = V_{GS} increases with ΔV_T during the stress mode.

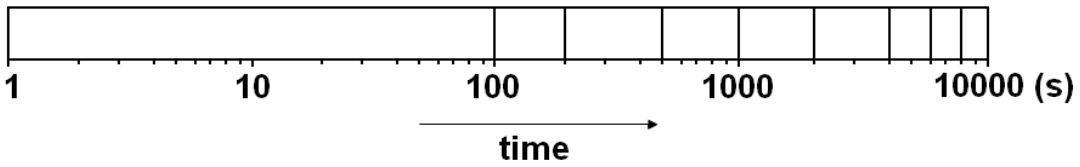

Figure 6.2 The CTS was performed on a single TFT for a total of 10000s. The white space indicates the stress mode, the black lines indicate when the stress mode is interrupted and switched to the sweep mode.

measurement procedure described above was repeated for several levels of stress current (I_{STR}) and stress temperature (T_{STR}) for both CTS setups. Table 6.1 summarizes the CTS conditions used in this paper. For both CTS setups, after the 10000s CTS measurement, the TFT was annealed at 300°C in air for 1 hour to recover its initial characteristics, as shown in Fig. 6.3.

6.3 CTS Effect on a-IGZO TFT Electrical Properties

Fig. 6.4(a) shows an example of the TFT transfer characteristics measured during the sweep mode (V_{DS} = 20V, V_{GS} = -5 → 20V) of CTS_lin. The CTS_lin was performed at T_{STR} = 80°C with V_{GS} held at 20V, and I_{STR} = 10μA. For this level of stress current (I_{STR} = 10μA), the drain-to-source voltage (V_{DS}) of the TFT is measured to be around 0.6V, which indeed corresponds to the linear regime of operation. Fig. 6.4(b) shows an

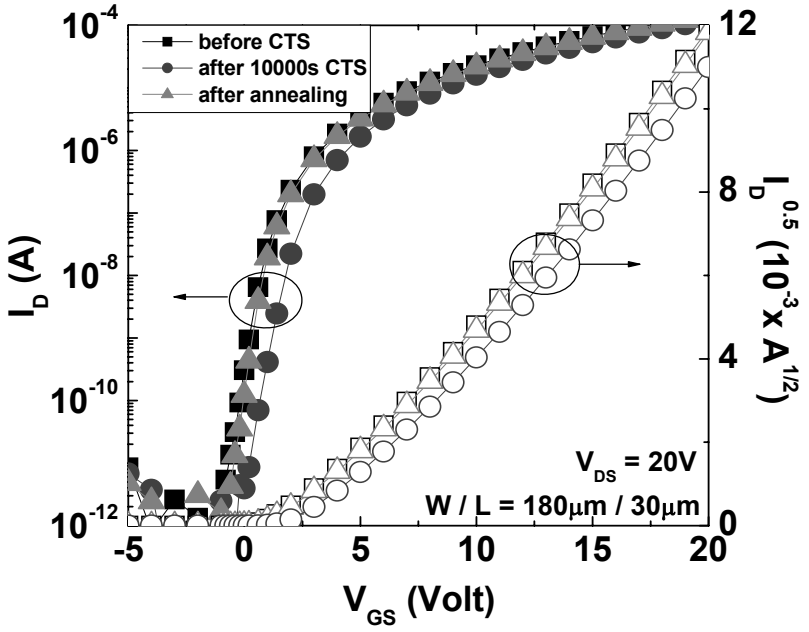

Figure 6.3 a-IGZO TFT transfer characteristics before CTS, after 10000s CTS, and after thermal annealing at 300°C in air for 1 hour.

example of TFT transfer characteristics measured during the sweep mode ($V_{DS} = V_{GS} = -5 \rightarrow 20V$) of CTS_sat. The CTS_sat was performed at $T_{STR} = 80°C$ with the gate and drain tied together, and $I_{STR} = 100\mu A$, which sets $V_{GS} = V_{DS} \sim 16.5V$. As we can see from Fig. 6.4, even after suffering through these strict CTS conditions for 10^4sec, the TFT subthreshold slope and off-current remained almost the same, the field effect mobility slightly (10%) decreases, and the threshold voltage only shifted ~2V for both CTS setups.

6.3.1 Stress Temperature Effect

We performed CTS measurements for both CTS setups at stress temperatures ranging from 40°C to 80°C. The stress currents are 10μA and 100μA for CTS_lin and CTS_sat, respectively. $I_{STR} = 10\mu A$ is sufficient for the maximum drive current level of a 15" XGA full color AM-OLED (subpixel area $A_{pix} \sim 30000\mu m^2$), assuming a brightness (υ) of 1000 Cd/m^2 and an OLED efficiency (η) of 5Cd/A:

$$I_{OLED} = \frac{\upsilon \cdot A_{pix}}{\eta} \tag{6.1}$$

We used a much higher I_{STR} for CTS_sat to enhance the TFT parameter shifts, since we observed that the TFTs are electrically more stable when stressed under CTS_sat compared to CTS_lin for the same I_{STR} level (see next section for further details). The device degradation is defined as the change in threshold voltage (V_T)

$$\Delta V_T = V_T(t = t_{STR}) - V_T(t = 0) \tag{6.2}$$

V_T was extracted from linearly fitting $I_D^{1/2}$-V_{GS} measured in the sweep mode. The fitting range is chosen to be V_{GS}=5~20V to avoid the effect of the subthreshold regime at smaller V_{GS} values. It should be noticed that the fitting range would affect the extracted

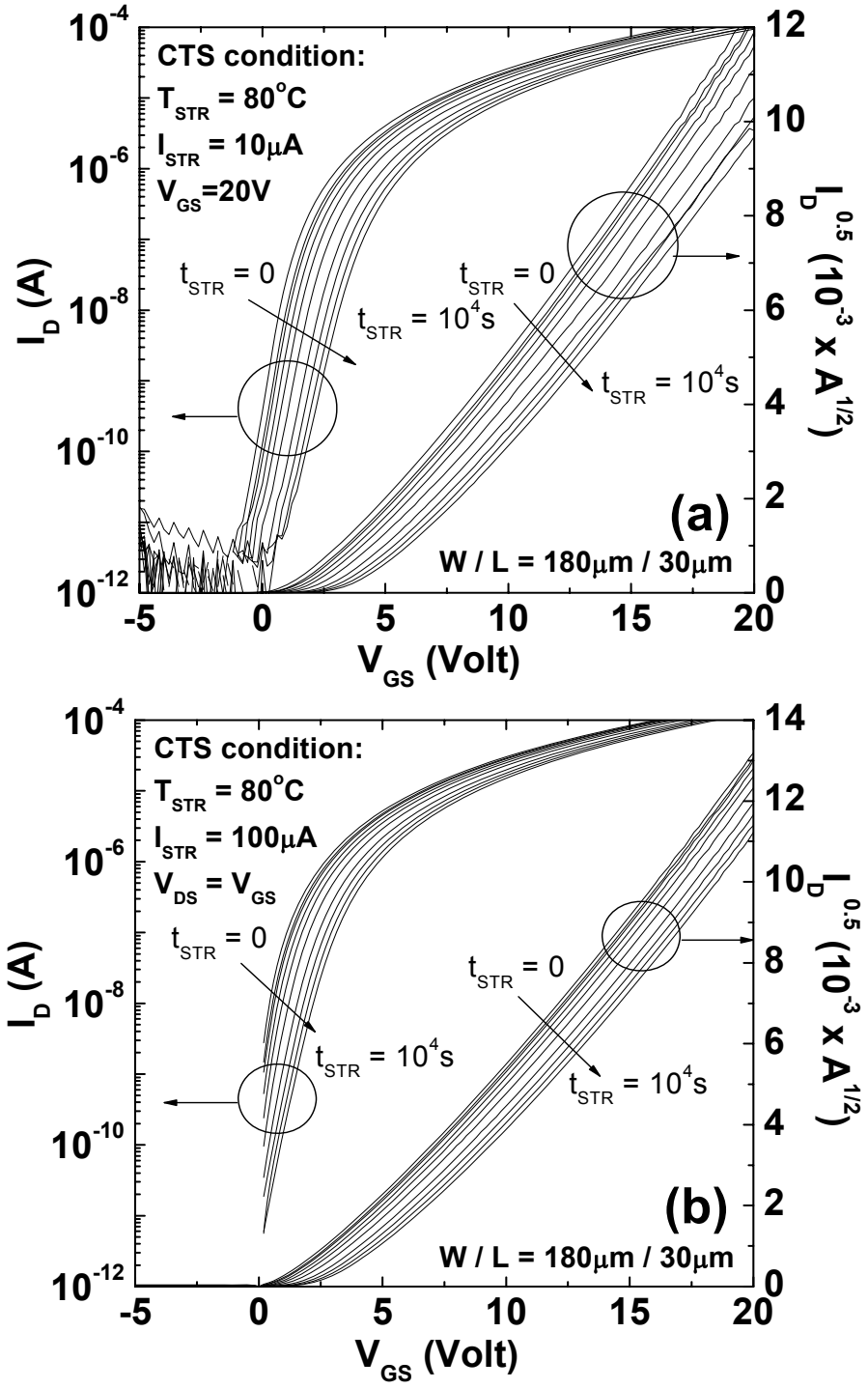

Figure 6.4 a-IGZO TFT transfer characteristics measured during the sweep mode of (a) CTS_lin and (b) CTS_sat.

V_T, due to the nonlinearity of the $I_D^{1/2}$-V_{GS} curve, and therefore should be carefully chosen. Fig. 6.5(a) and Fig. 6.5(b) show the TFT threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various T_{STR} under CTS_lin and CTS_sat, respectively. For both CTS setups, ΔV_T increases with T_{STR} for a given t_{STR}. We also observed that

$$\Delta V_T \propto t_{STR}^{\beta} \tag{6.3}$$

β is extracted to be 0.4±0.05 for our a-IGZO TFTs, and corresponds to a Gaussian distribution barrier with width kT/β in energy (~65meV when T=300K) [103]. We have not observed any temperature dependence of β in the investigated T_{STR} range so far.

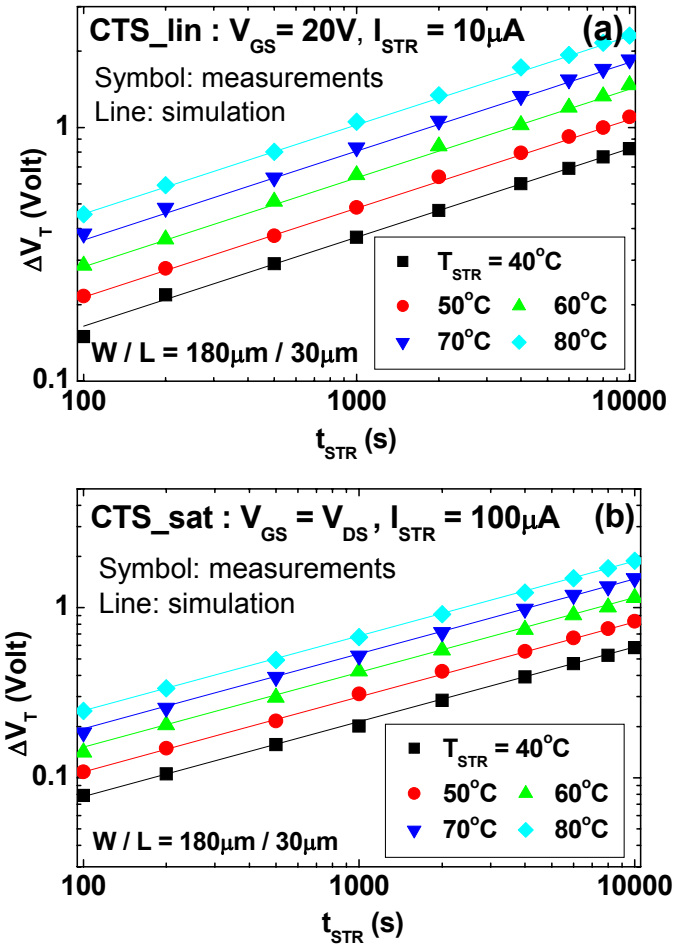

Figure 6.5 Threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various stress temperatures (T_{STR}) for (a) CTS_lin and (b) CTS_sat.

A model that unifies the effect of stress temperature (T_{STR}) and stress time (t_{STR}) on defect creation was developed for a-Si:H TFTs [104]. This model assumes a distribution of energy barriers $D(E_a)$ for defect creation exists during bias stress: after a time t at a temperature kT all possible defect-creation sites with $E_a \leqq kT\ln(\nu t)$ will have converted into defects. The thermalization energy is therefore defined by

$$E = k \cdot T_{STR} \cdot \ln(\nu \cdot t_{STR}) \tag{6.4}$$

where k is the Boltzmann constant and ν is the attempt-to- escape frequency. We investigated possible application of this thermalization energy concept to a-IGZO TFTs. By plotting ΔV_T as a function of E, a unique curve is obtained for both CTS setups with only one fitting parameter, the attempt to escape frequency ν, as can be seen from Fig. 6.6. The value of ν is 10^7 Hz for CTS_lin and 10^6 Hz for CTS_sat, and was determined to ensure the best overlap of the ΔV_T -E curves for all stress temperatures. It should be noticed that the thermalization energy is a function of ln(ν), therefore the effect of 10^6 Hz and 10^7 Hz are actually very close (14% difference). For a-Si:H TFTs, ν was extracted to be 10^{10} Hz and is believed to be associated with the breaking of weak Si-Si bonds [104]. Although the physical meaning of ν is unclear for our a-IGZO TFTs, Eq. (6.4) describes very well our experimental data in the investigated T_{STR} and t_{STR} range.

6.3.2 Stress Current Effect

We also performed CTS measurements at various I_{STR} levels. For CTS_lin, I_{STR} = 1μA, 10μA, 40μA, and 100μA, and for CTS_sat, I_{STR} = 40μA, 60μA, 80μA, and 100μA. Again, For CTS_sat, we didn't explore lower I_{STR} levels for the same reason mentioned previously. The stress temperature (T_{STR}) was fixed at 60°C. Fig. 6.7 shows the threshold

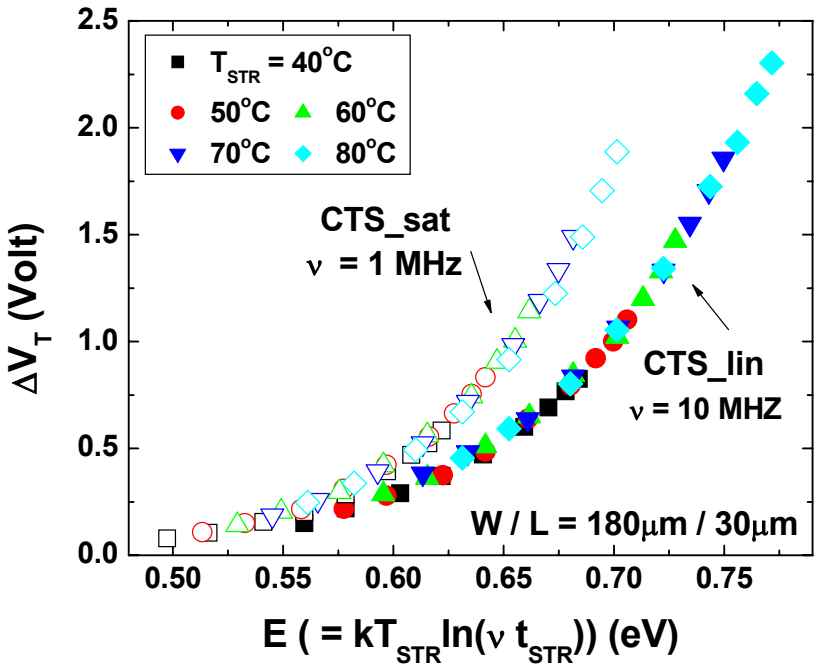

Figure 6.6 Threshold voltage shift (ΔV_T) as a function of thermalization energy (E), unifying the effect of stress temperature (T_{STR}) and stress time (t_{STR}).

voltage shift (ΔV_T) as a function of t_{STR} for various I_{STR} levels under CTS_lin and CTS_sat. For CTS_lin, we can see that ΔV_T-t_{STR} is almost independent of I_{STR}. On the other hand, for CTS_sat, ΔV_T-t_{STR} increases with I_{STR}, and becomes independent of I_{STR} once normalized to the injected charge Q_{inj} (=I_{STR} x t_{STR}), as shown in Fig. 6.8. Q_{inj} is commonly used to evaluate the ΔV_T caused by trapped charge in the gate dielectric for c-Si MOSFETs [105]. We attribute this behavior to the following. The V_{GS} is fixed at 20V for all levels of I_{STR} in CTS_lin, therefore the channel induced charge will remain almost the same as long as the TFT operates in the linear regime. However, in CTS_sat, the V_{GS} adjusts accordingly to I_{STR}, and therefore, at higher I_{STR} values, we have a higher V_{GS}, and thus more channel induced charge. The V_{GS} and V_{DS} values are summarized in Table 6.2 for both CTS setups and all I_{STR} levels. We conclude from our experimental results that for the same I_{STR}, the a-IGZO TFTs are electrically more stable when V_{GS} is smaller.

Table 6.2 V_{DS} and V_{GS} values for both CTS conditions.

CTS condition	I_{STR} (μA)	V_{DS}*(V) (t_{STR} = 0)
CTS_lin V_{GS} = 20V T_{STR} = 60°C	1	0.06
	10	0.56
	40	2.4
	100	7.5
CTS_sat V_{GS} = V_{DS} T_{STR} = 60°C	40	11.9 (=V_{GS})
	60	13.8 (=V_{GS})
	80	15.5 (=V_{GS})
	100	17.0 (=V_{GS})

* During CTS, V_{DS} increases with t_{STR}.

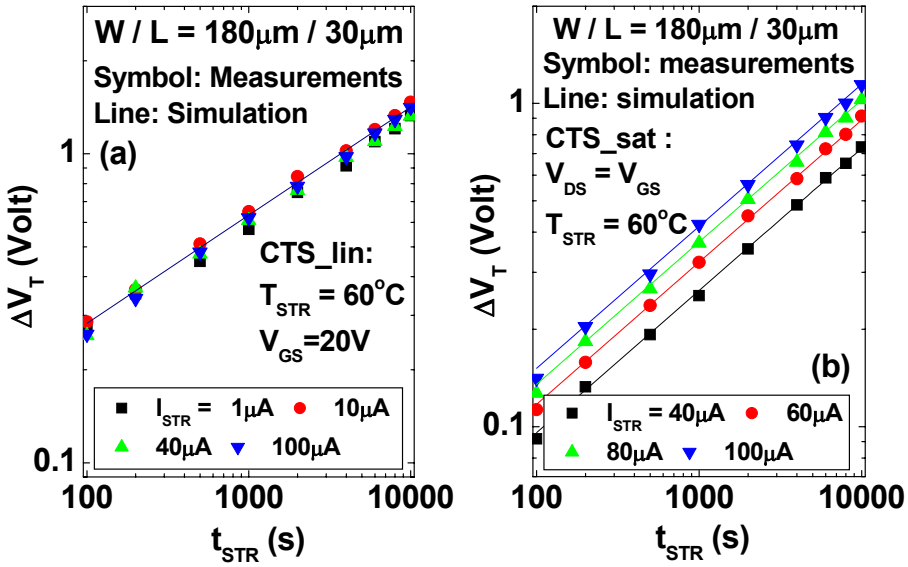

Figure 6.7 Threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various stress current (I_{STR}) levels under (a) CTS_lin and (b) CTS_sat.

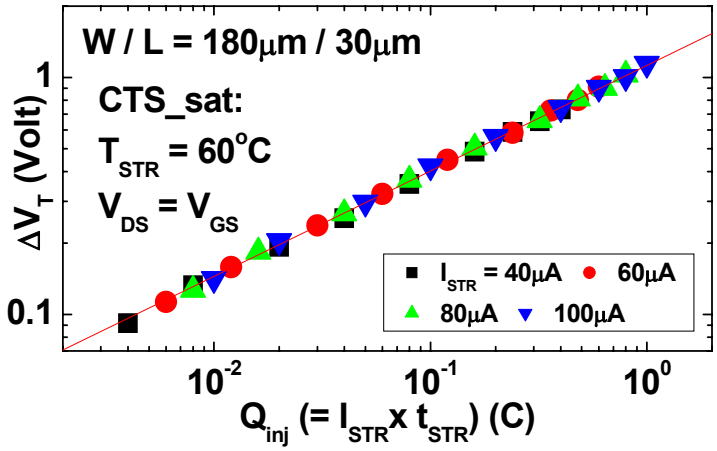

Figure 6.8 Threshold voltage shift (ΔV_T) as a function of injected charge (Q_{inj}) for various stress current (I_{STR}) levels under CTS_sat.

6.4 Current Temperature Stress Measurement Modeling

In CTS_sat, V_{GS} increases with V_T in order to maintain a constant I_D, which is similar to the ΔV_T compensation mechanism in AMOLED pixel circuits. A model that can describe/predict the ΔV_T as a function of stress time (t_{STR}), stress temperature (T_{STR}), and stress current (I_{STR}) is beneficial to designing AMOLED pixel circuits. A stretched-exponential model based on the charge injection/trapping concept was developed for a-Si:H TFTs when subject to constant voltage stress [106]. We modified this model taking into account that the gate overdrive voltage $[V_{GS}(t)-V_T(t)]$ is constant during CTS_sat. Identical equation has also been derived for a-Si:H TFTs when subject to constant current stress, based on the carrier-induced defect creation model [30].

$$\Delta V_T = [V_{GS}(t) - V_T(t)]^{\alpha} \cdot \left(\frac{t_{STR}}{\tau}\right)^{\beta} \tag{6.5}$$

where α and β are the exponents for the gate overdrive voltage and stress time, respectively, $\tau = \tau_0 \exp(E_\tau/kT_{STR})$, and E_τ is the average effective barrier that the electrons in the a-IGZO channel need to overcome before they can enter the insulator, and τ_0 is the thermal prefactor for emission over the barrier. This power law relation shows that there is no upper bound for ΔV_T which is in contrast to the stretched-exponential model. It should also be noticed that for very short stress times ($t_{STR} << \tau$), the stretched-exponential equation reduces to the exact same power law equation. However, Eq. (6.5) is only valid in the linear regime of operation since it assumes a uniform charge density along the channel. The channel charge in the saturation regime is reduced by the drain voltage and becomes $[1+1/(2+\gamma)]$ times smaller, where γ is the nonlinear factor of the TFT transfer characteristics. Therefore, in the saturation regime, Eq. (6.5) becomes

(6.6) $$\Delta V_T = [\frac{V_{GS}(t) - V_T(t)}{1 + 1/(2+\gamma)}]^{\alpha} \cdot (\frac{t_{STR}}{\tau})^{\beta}$$

Eq. (6.6) is not suitable for CTS_sat or any current-programmed pixel circuits, since we do not control V_{GS} directly. It is therefore more straightforward to express (6.6) as a function of I_{STR} by using

(6.7) $$I_{STR} = \frac{1}{2+\gamma} \cdot K \cdot (V_{GS} - V_T)^{2+\gamma}$$

where $K = (W/L)C_{ox}\mu_0$. Plugging (6.7) into (6.6), we can write the power law equation as a function of I_{STR} instead of gate overdrive voltage

(6.8) $$\Delta V_T = \frac{(\frac{2+\gamma}{K} \cdot I_{STR})^{\frac{\alpha}{2+\gamma}}}{(1+\frac{1}{2+\gamma})^{\alpha}} \cdot (\frac{t_{STR}}{\tau})^{\beta}$$

The nonlinear factor γ was extracted to be ~0.48 for our a-IGZO TFTs. By plotting $\log(\Delta V_T)$ as a function of $\log(I_{STR})$ for several levels of t_{STR}, as shown in Fig. 6.9, we can obtain $\alpha/(2+\gamma) \sim 0.5$ from the slopes, and thus $\alpha \sim 1.24$.

On the other hand, CTS_lin can be modeled by the stretched-exponential model [39, 106, 107], since V_{GS} is held constant.

(6.9) $$\Delta V_T = [V_{GS} - V_{T0}]^{\alpha} \cdot \{1 - \exp[-(\frac{t_{STR}}{\tau})^{\beta}]\}$$

The simulation results of CTS_lin and CTS_sat are shown as the lines in Fig. 6.5 and Fig. 6.7. The same value of $\alpha = 1.24$ were used in both simulations. $\beta = 0.35$ for CTS_lin and $\beta = 0.44$ for CTS_sat. The fitting parameter τ as a function of $(kT_{STR})^{-1}$ is plotted in Fig. 6.10. τ_0 is extracted to be 4.4 ms for both CTS setups, while $E_\tau = 0.7$eV and 0.62eV for CTS_lin and CTS_sat, respectively. The parameters used in CTS simulations are summarized in Table 6.3.

Table 6.3 CTS Modeling Parameters

	CTS_lin	CTS_sat
α	1.24	
β	0.35	0.44
γ	NA	0.48
τ_0	4.4ms	
E_τ	0.7eV	0.62eV

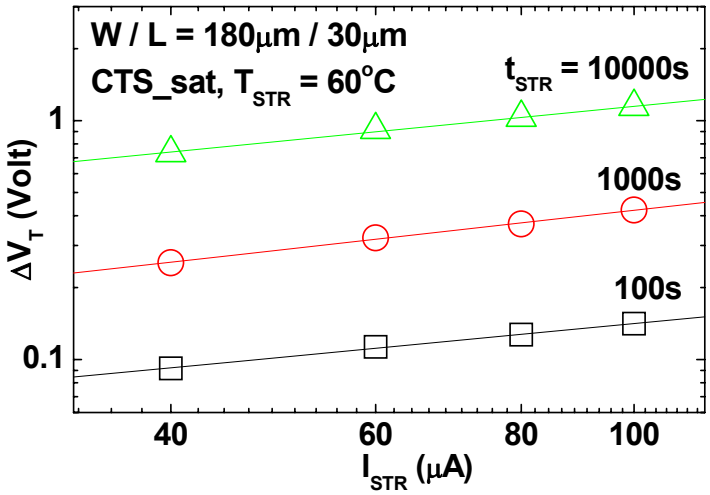

Figure 6.9 Threshold voltage shift (ΔV_T) as a function of stress current (I_{STR}) for various t_{STR} levels.

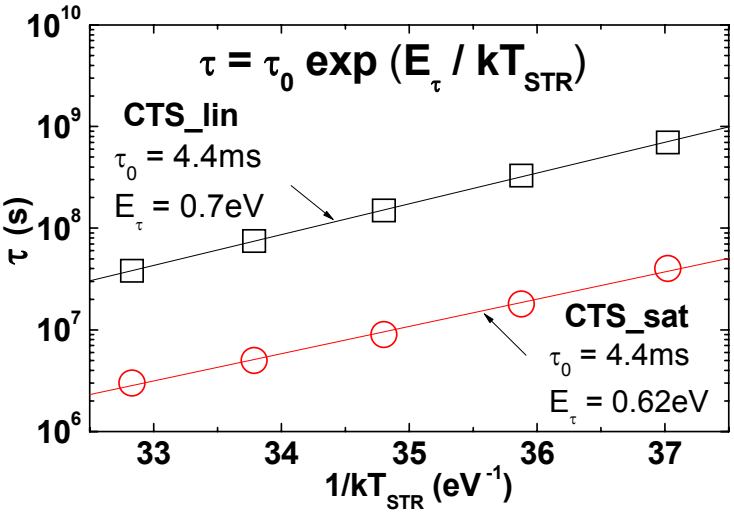

Figure 6.10 Extracting the average effective barrier E_τ and thermal prefactor τ_0 from fitting parameter τ.

6.5 Conclusion

CTS measurements were performed to evaluate the electrical stability of a-IGZO TFTs. Several factors were considered, including the stress time (t_{STR}), stress temperature (T_{STR}), stress current (I_{STR}), and biasing condition. We observed that the threshold voltage shift (ΔV_T) follows a power-law relationship with t_{STR} and I_{STR}, and that maintaining a lower temperature and smaller V_{GS} is beneficial to the TFT's electrical stability. We also found that for the same level of I_D, the TFTs are more stable when operating in the saturation regime then in the linear regime. The a-IGZO TFTs exhibit ΔV_T ~1V under 10000s stress with I_{STR} = 100μA, and T_{STR} = 60°C. The subthreshold slope, off-current, and field- effect mobility remain almost unchanged during the stress. The stretched-exponential model modified for CTS describes very well ΔV_T as a function of t_{STR}, T_{STR}, and I_{STR}, suggesting that charge trapping in the interface/dielectric is the origin of electrical instability.

CHAPTER VII

Amorphous In-Ga-Zn-O Thin Film Transistors for Active-Matrix Organic Light-Emitting Displays: Pixel Circuit Simulation

7.1 Introduction

In the previous chapters, we have explored the electrical properties of a-IGZO TFTs, and concluded that a-IGZO TFTs are very promising for AMOLED applications. The low off-current prevents the OLED current leaking from the TFTs during the Off-state. The sharp subthreshold slope is beneficial to the TFT switching speed. The high field-effect mobility allows extra freedom when designing the pixel circuit. Smaller device sizes can be used, which increases the pixel aperture ratio, and lower gate overdrive voltages (V_{GS}-V_T) are sufficient to provide the desire current level. From the CTS measurement results presented in the previous chapter, lower gate overdrive voltages are also very beneficial to the TFT electrical stability. Several a-IGZO TFT AMOLEDs have been demonstrated by other groups, indicating a promising future for these devices [25, 83]. In this chapter, we examine the possible application of a-IGZO TFTs to AMOLEDs by performing circuit simulations. a-IGZO TFT SPICE model is developed based on experimental data. Several voltage- and current-programmed pixel circuits are simulated, and the advantage of using a-IGZO TFTs is discussed.

7.2 SPICE Model used in Simulation

7.2.1 a-IGZO TFT SPICE Model

a-IGZO TFT SPICE model was developed based on the Rensselaer Polytechnic Institute (RPI) a-Si:H TFT model [97]. This semi-empirical, physics-based model takes into account the gate-bias-dependent field-effect mobility, and assumes an exponential distribution of deep localized states. Inverted-staggered rf magnetron sputtered a-IGZO TFTs described in chapter II were used in this study. Needed a-IGZO TFT SPICE parameters were extracted from experimental data by following the procedure previously developed for a-Si:H TFTs. Synopsys HSPICE simulation tool was then used to simulate the TFT characteristics (illustrated as the open circles in Fig. 7.1). We can see that the RPI a-Si:H TFT model with appropriate a-IGZO TFT SPICE parameters can reproduce very well our measured device characteristics.

7.2.2 OLED SPICE Model

To model the behavior of the OLED, we used two junction diodes D_1 D_2 (HSPICE diode model level 1) with series resistors R_{S1} R_{S2} connected in parallel with a capacitor C, shown as the inset of Fig. 7.2. SPICE parameters were extracted based on experimental data obtained within our group [31], and summarized in Table 7.1. The OLED area was assumed to be 12000μm^2 which is about the subpixel area of an RGB 3" QVGA display (63.5μm x 190.5μm). The OLED capacitor was calculated by assuming the capacitance per unit area is 25nF/cm^2. The OLED I-V curve simulated by HSPICE is shown in Fig. 7.2.

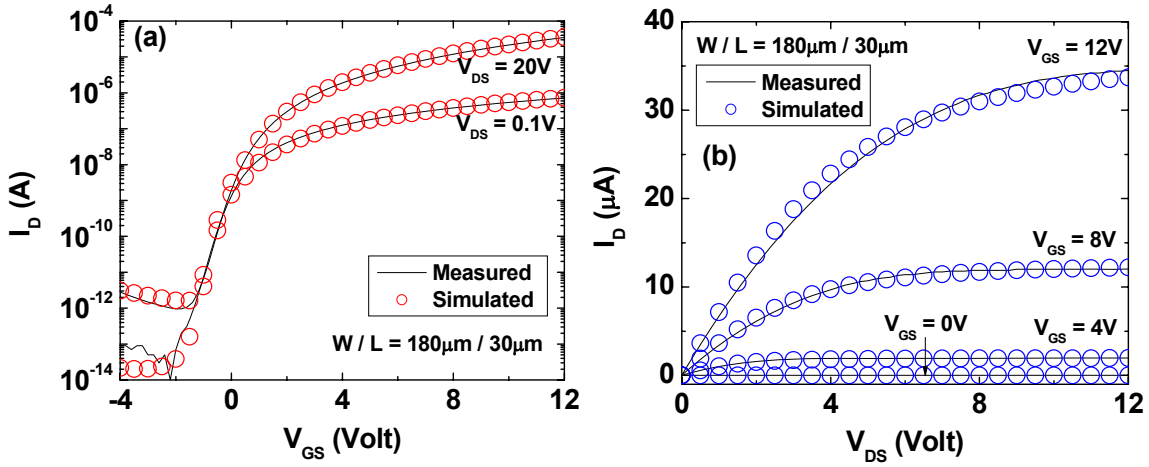

Figure 7.1 Measured and simulated (using HSPICE) a-IGZO TFT (a)transfer and (b)output characteristics.

Table 7.1 OLED SPICE Parameters

Area	12000 μm^2
D1	I_S = 4.2nA, n = 7.8, I_K = 13A
D2	I_S = 60fA, n = 3.6, I_K = 32mA
R_{S1}	2.6mΩ
R_{S2}	27mΩ
C	3pF

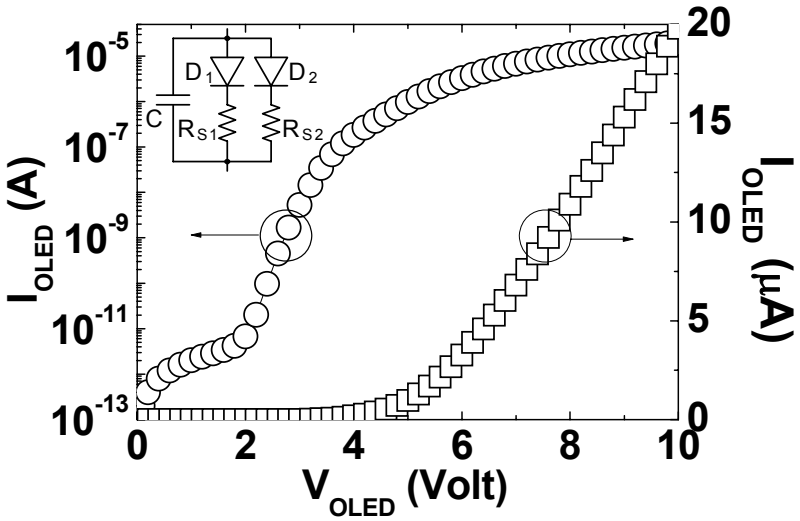

Figure 7.2 Simulated OLED I-V characteristics

7.3 AMOLED Pixel Circuit Simulations

7.3.1 Simple Voltage-Programmed Pixel Circuit

So far, all reported AMOLEDs driven by a-IGZO TFTs are based on the 2-TFT voltage-programmed pixel circuit [25, 38], as shown in Fig. 7.3 (a). The pixel circuit consists of one switching TFT (T1), one driving TFT (T2), and one storage capacitor (C_{ST}). The anode and cathode of the OLED are connected to the source of T2 and ground, respectively. The signals of V_{SCAN} and V_{DATA} are supplied by external drivers. Synopsys HSPICE simulation tool with the a-IGZO TFT and OLED SPICE models developed in the previous section were used to evaluate the pixel circuit performance. An example of simulated operation waveform is shown in Fig 7.4 (a). The total frame time is 16.7 ms, which corresponds to a 60Hz frame rate. During the ON-State, the scan line signal V_{SCAN} turns on T1, and the data voltage signal V_{DATA} charges the storage capacitor C_{ST} to the desired voltage (~V_{DATA}). The voltage stored on C_{ST} will remain constant even during the OFF-State when T1 is turned off by V_{SCAN}, except for the initial drop due to charge feedthrough. The drive transistor T2 is designed to operate in the saturation regime, so that the gate voltage (V_{G2}) determines the drive current and OLED brightness. Parameters used in the simulation are summarized in Table 7.2. Since the field-effect mobility of a-IGZO TFTs is ~10 times larger than that of a-Si:H TFTs, smaller device sizes (W/L = 24μm/4μm) and lower supply voltages (V_{DD} = 10V) can be used in this circuit. An additional TFT can be added to this circuit to prevent a sudden peak current from damaging the OLED, as shown in Fig 7.3 (b). The simulated operation waveforms are shown in Fig. 7.4 (b). This circuit operates similar as the 2-TFT circuit except the current flows through the OLED only during the expose period.

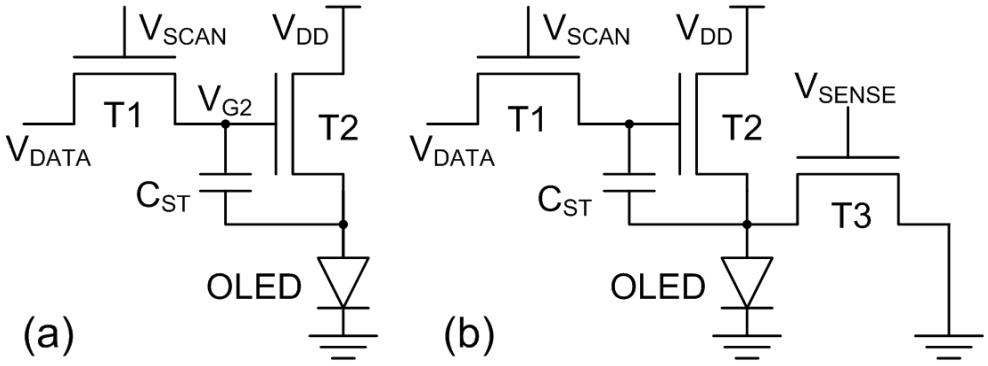

Figure 7.3 Schematic diagrams of the (a) 2-TFT voltage-programmed pixel circuit and (b) the same circuit with an additional TFT (T3).

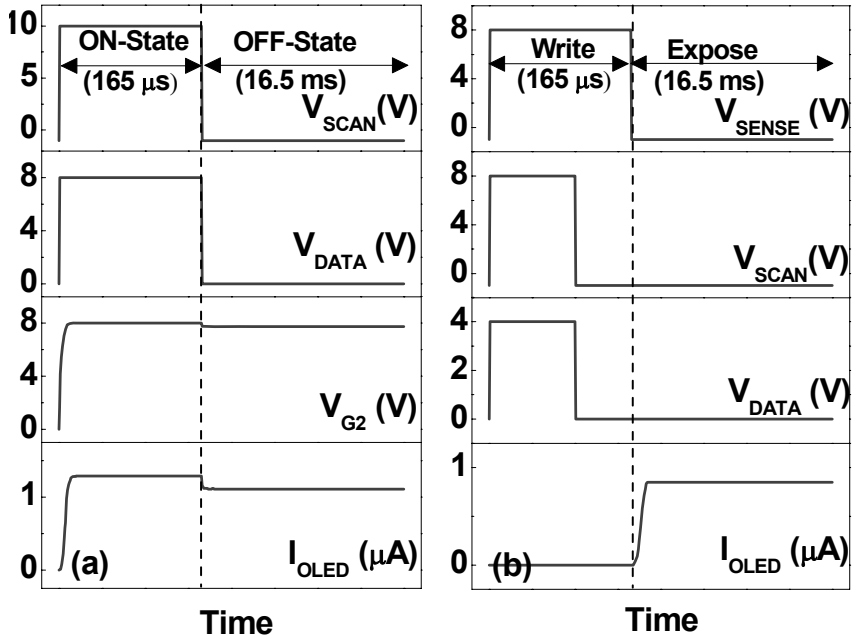

Figure 7.4 Operation waveforms of the pixel circuits in Fig. 7.3(a), and (b), respectively, simulated by HSPICE.

Table 7.2 Parameters used in HSPICE simulation for pixel circuits in Fig. 7.3(a) and (b).

	(a)	(b)		(a)	(b)
T1	4/4		**V_{DD} (V)**	10	8
T2	24/4		**V_{SCAN} (V)**	-1→10	-1→8
T3	NA	8/4	**V_{SENSE} (V)**	NA	-1→8
C_{ST}	1pF		**V_{DATA} (V)**	3 ~ 9	1 ~ 7

7.3.2 Current-Scaling Current-Mirror Pixel Circuit

The 2-TFT voltage-programmed pixel circuit is very simple in design and enables a high aperture ratio. However, due to the current-driven nature of OLEDs and their steep I-V characteristics, current-programmed pixel circuits are more suitable to precisely generate distinct grey levels. Moreover, even if the a-IGZO TFTs are electrically very stable, it is still desirable to use a pixel circuit that can compensate for any non-ideal factors. Several current-programmed pixel circuits were developed for AMOLEDs [108-110]. Our group has previously explored the possible application of a- IGZO TFTs to a current-scaling pixel circuit that provides a wide dynamic OLED current (I_{OLED}) range and compensation abilities [83]. Here, we apply a-IGZO TFTs to a current-scaling current-mirror pixel circuit [111]. This circuit has similar performance as the previous circuit with a simpler driving scheme.

The current-scaling current-mirror pixel circuit consists of two switching TFTs (T1 and T2), one mirror TFT (T4), one driving TFT (T3), and two storage capacitors (C_{ST1}, C_{ST2}) connected between the scan line and ground with a cascade structure, as shown in Fig 7.5. The anode and cathode of the OLED are connected to V_{DD} and the drain of T3, respectively. The signals of V_{SCAN} and I_{DATA} are supplied by external drivers. Fig. 7.6 shows an example of operation waveforms simulated by HSPICE. The frame time is 16.7 ms which corresponds to a 60Hz frame rate. During the ON-State, the scan line signal V_{SCAN} turns on T1 and T2. Initially the data current signal I_{DATA} flows through T1 and T2, and charges up the storage capacitors C_{ST1} and C_{ST2}. Once the voltage stored between C_{ST1} and C_{ST2} (the gate voltage of T4) reaches a certain value, all I_{DATA} flows through T1 and T4. T3 and T4 are designed to have the same geometry and operate in the

saturation regime. Since the gates of T3 and T4 are tied together, a current with the same amount as I_{DATA} flows through T3, which is the current that drives the OLED during the ON-State ($I_{OLED\_ON} = I_{DATA}$). When the pixel changes from the ON- to OFF-State, V_{SCAN} turns off T1 and T2. The voltage stored between C_{ST1} and C_{ST2} (V_{G3}) is reduced due to the feedthrough effect. V_{G3_OFF} can be derived from the charge conservation theory and is roughly given by

$$V_{G3\_OFF} = V_{G3\_ON} - \Delta V_{SCAN} \cdot \frac{C_{ST2} // C_{OV\_T2}}{C_{ST1} + C_{ST2} // C_{OV\_T2}} \tag{7.1}$$

Since the gate bias of T3 is reduced from V_{G3_ON} to V_{G3_OFF} by the ratio of the cascaded storage capacitors, a scaled down current flows through the OLED during the Off-State (I_{OLED_OFF}). Consequently, a very large data current (I_{DATA}) can be used to charge the pixel to shorten the pixel programming time, while a smaller driving current (I_{OLED_OFF}) can be achieved for lower gray scales. Parameters used to simulate this circuit are listed in Table 7.3 for both a- IGZO TFTs and a-Si:H TFTs [111]. Smaller device sizes (W/L = 20μm/4μm) and lower supply voltages (V_{DD} = 12V) can be used for this circuit based on a-IGZO TFTs.

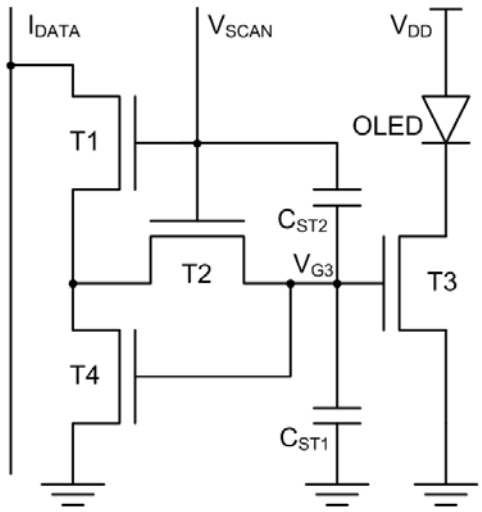

Figure 7.5 Schematic diagram of the 4-TFT current-scaling current-mirror pixel circuit.

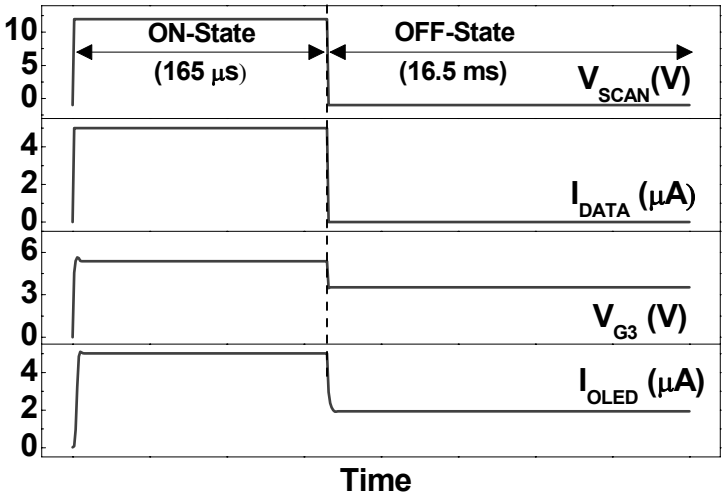

Figure 7.6 Operation waveforms of the 4-TFT current-scaling current-mirror pixel circuit simulated by HSPICE.

Table 7.3 Parameters used in HSPICE simulation for the 4-TFT current-scaling current-mirror pixel circuit.

	a-IGZO	a-Si:H [111]
T1, T3, T4	20/4	150/6
T2	4/4	10/6
C_{ST1} (fF)	360	
C_{ST2} (fF)	60	
V_{DD} (V)	12	18
V_{SCAN} (V)	-1→12	-5→25
I_{DATA} (μA)	0.2 ~ 5	

7.3.3 Pixel-Circuit Simulation Results

The OLED currents (I_{OLED}) delivered by the 2-TFT voltage-programmed pixel circuit and the 4-TFT current-scaling current-mirror pixel circuit as a function of V_{DATA} and I_{DATA}, respectively, are shown in Fig. 7.7. Since the OLED current value is different

during the ON- and OFF-states (I_{OLED_ON} and I_{OLED_OFF}), we define the average OLED current (I_{OLED}) during one frame time as

$$I_{OLED} = \frac{I_{OLED\_ON} \cdot t_{ON} + I_{OLED\_OF} \cdot t_{OFF}}{t_{ON} + t_{OFF}} \tag{7.2}$$

where t_{ON} (165μs) and t_{OFF} (16.5ms) are the ON- and OFF-state periods, respectively (the frame rate is set to be 60Hz). As we can see from Fig 7.7, wide dynamic I_{OLED} range (~10^3) was achieved by both pixel circuits.

7.3.4 Impact of TFT Instability on Pixel-Circuit Operation

We also simulated the two pixel circuits assuming that the drive TFTs (T2 in Fig. 7.3 (a), T3 and T4 in Fig. 7.5) exhibit 1V of threshold voltage shift (ΔV_T), as shown in Fig. 7.7. The percentage change in I_{OLED} (ΔI_{OLED}) is defined as

$$\Delta I_{OLED} = \frac{I_{OLED}(\Delta V_T = 0) - I_{OLED}(\Delta V_T)}{I_{OLED}(\Delta V_T = 0)} \cdot 100\% \tag{7.3}$$

We can see that the 4-TFT current-scaling current-mirror pixel circuit can compensate for ΔV_T within operating error range from 9 to 25%, depending on the I_{OLED} level, while the 2-TFT voltage-programmed pixel circuit does not compensate for ΔV_T at all (ΔI_{OLED}: 40~90%). Keeping in mind that 1V of ΔV_T is quite large comparing to the small gate overdrive (0~5V) designed to be used in the pixel circuit simulations. To further investigate the compensation ability of the 4-TFT current-scaling current-mirror pixel circuit, we plotted ΔI_{OLED} as a function of I_{OLED} for ΔV_T = 0.2V, 0.5V, and 1V, as shown in Fig. 7.8. We can observe that ΔI_{OLED} is more severe at lower I_{OLED} levels due to the smaller gate overdrive of the drive TFT. The percentage error can be maintained below 10% for all levels of I_{OLED} if ΔV_T is smaller than 0.2V. This result indicates that we need electrically very stable a-IGZO TFTs to be used for AMOLEDs.

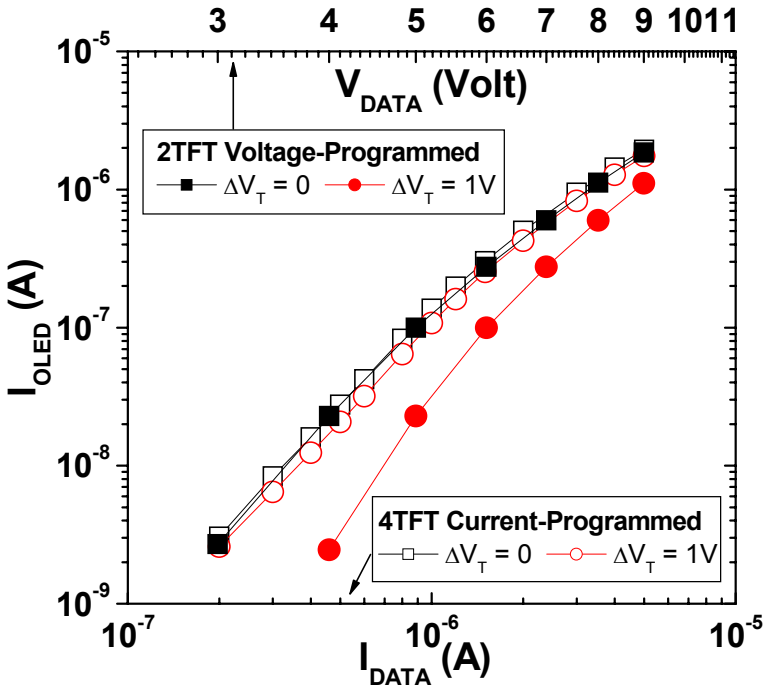

Figure 7.7 I_{OLED} as a function of V_{DATA} for the 2-TFT voltage-programmed pixel circuit (solid symbols), and I_{DATA} for the 4-TFT current-scaling current-mirror pixel circuit (hollow symbols).

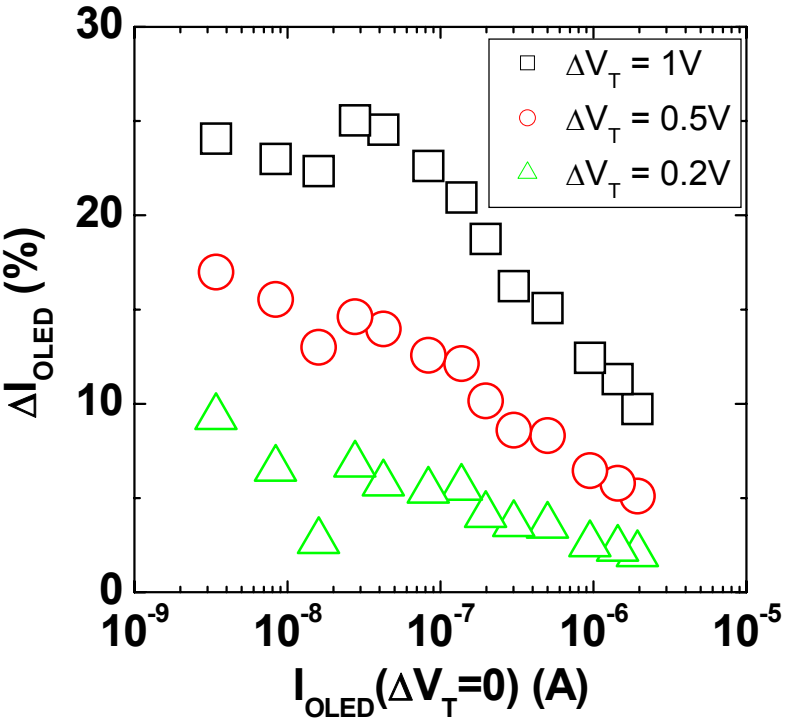

Figure 7.8 ΔI_{OLED} as a function of I_{OLED} for the 4-TFT current-scaling current-mirror pixel circuit at several levels of ΔV_T.

7.4 Conclusion

a-IGZO TFT SPICE model was developed based on experimental data. Both simple voltage- and current-programmed pixel circuits were simulated. Smaller device sizes and lower supply voltages could be used compare to a-Si:H TFT pixel circuits. The pixel circuits are very sensitive to the TFT instability due to the designed small gate overdrive. The first issues that must be resolved include the attainment of ΔV_T smaller than 0.2V for the lifetime of the display. The electrical stability of a-IGZO TFTs should be improved by the proper choice of passivation [41] and dielectric material [39, 40], and careful optimization of the IGZO composition [14]. We believe that a-IGZO TFTs, once fully optimized, are very competitive for higher resolution and lower power consumption AMOLED application.

CHAPTER VIII

Conclusions and Future Work

8.1 Summary

The focus of this work has been to provide a more thorough understanding of the device performance of amorphous In-Ga-Zn-O (a-IGZO) thin film transistors (TFTs), along with the underlying semiconductor physics and their possible application to active-matrix organic light-emitting displays (AMOLEDs).

In Chapter II, the electronic structure of crystalline In-Ga-Zn-O (c-IGZO) along with the impact of point defects are studied by *ab initio* calculations based on the density function theory. The calculated electronic structure showed that the valance band maximum (VBM_0) is mostly contributed by the p orbitals of the oxygen atoms. The conduction band minimum (CBM_0) mainly consists of the s orbitals of the Zn/Ga mixture atoms, while the In atoms have the largest spatial spread of wave function. Oxygen vacancies create fully occupied defect states within the bandgap and serve as deep donors. Both hydrogen substitutions and interstitials act like shallow donors, and raise the Fermi level above the CBM. Oxygen split interstitials created fully occupied defect states above VBM_0, while oxygen octahedral interstitials create both occupied and unoccupied states, and may serve as acceptors.

In Chapter III, DC characterization and analysis of the electrical performance of inverted-staggered a-IGZO TFTs is presented. The devices demonstrated field-effect mobilities and threshold voltages around 10 cm^2/V-s and 3 V, respectively, as well as subthreshold slopes of 0.4 V/dec and very low Off-currents in the range of 10^{-13}~10^{-12} A. The nonlinearity of the TFT transfer characteristics (I_D-V_{GS}) was discussed and a gate bias (V_{GS}) dependent field-effect mobility with a nonlinear exponent (γ) was introduced into the TFT parameter-extraction method. Lastly, the source/drain contact resistance was extracted to be small and negligible comparing to the TFT channel resistance.

In Chapter IV, the operation principle of a-IGZO TFTs is revealed by surface potential imaging using scanning Kelvin probe microscopy (SKPM). The device was biased during the measurement, and the effect of V_{GS} and V_{DS} on the channel potential profile $V_{ch}(x)$ was discussed. In the linear region, a linear increase in $V_{ch}(x)$ was observed, while in the saturation region, the potential rises more near the drain end. The source/drain contact resistance $R_{S/D}$ ~ 28 kΩ was also extracted from the sudden potential rise $V_{S/D}$ at the source/channel and channel/drain interfaces, and agrees with the previously reported value extracted from the transmission line method. The effect of the V_{GS} dependent mobility and source/drain contact resistance was included in the standard MOSFET equation, and describes very well our measured $V_{ch}(x)$. The field-effect mobility (μ) extracted from the surface potential profile increases with V_{GS}, which can be explained by the V_{GS} dependent trapped charges and free carriers. μ also slightly decreases with V_{DS} due to the increased I_D which causes a larger potential drop at the source/channel interface, therefore, making the effective V_{GS} smaller.

In Chapter V, the effect of temperature on a-IGZO TFTs is described. Devices were measured at temperatures ranging from 20°C to 80°C, and TFT parameters were extracted. The field–effect mobility is weekly thermally activated with an activation energy around 26 meV, while the threshold voltage linearly decreases with temperature with a coefficient of -17 mV/°C. The current On-Off ratio and subthreshold slope almost remained the same within the investigated temperature range. The Meyer-Neldel (MN) parameter was observed to be constant (22.5 eV^{-1}) over a broad range of activation energies. Finally, based on the temperature-dependent field-effect measurements, the density of deep sates (DOS) was calculated to be small ($<10^{18}$ $eV^{-1}cm^{-3}$) with a characteristic energy of 120 meV.

In Chapter VI, the electrical stability of a-IGZO TFTs is evaluated by current temperature stress (CTS) studies. Several factors were considered in this study including the stress time (t_{STR}), stress temperature (T_{STR}), stress current (I_{STR}), and TFT biasing condition. When subject to CTS, the TFT transfer characteristics (I_D-V_{GS}) exhibit a parallel shift, showing an increase in threshold voltage (ΔV_T), while the field-effect mobility, subthreshold slope, and Off-current remain almost unchanged. ΔV_T was found to be more severe at higher T_{STR}, and follows a power-law relationship with t_{STR} and I_{STR}. It was also observed that for the same level of I_{STR}, the TFTs are electrically more stable when operating in the saturation regime than in the linear regime. The stretched-exponential model modified for CTS describes very well ΔV_T as a function of t_{STR}, I_{STR}, and T_{STR}, suggesting that charge injection/trapping in the gate dielectric layer is the mechanism of the TFT electrical instability.

In Chapter VII, the application of a-IGZO TFTs to AMOLED pixel circuits is examined by SPICE simulations. SPICE model of a-IGZO TFTs was developed based on experimental data. Both simple voltage-programmed pixel circuits and current-programmed pixel circuits with ΔV_T compensation ability were simulated. Comparing to hydrogenated amorphous silicon (a-Si:H) TFT pixel circuits, smaller device sizes and lower supply voltages could be used in a-IGZO TFT pixel circuits due to the superior electrical properties. The impact of TFT instability on pixel circuit operation was also investigated. Simulation results showed that electrically very stable ($\Delta V_T \sim 0$) a-IGZO TFTs are required. However, it is believed that, a-IGZO TFTs, once fully optimized, have great potential for higher resolution and lower power consumption AMOLEDs.

8.2 Future Work

Although tremendous progress has been made in understanding and developing high performance a-IGZO TFTs, much work remains to realize fully transparent large area electronics. Candidate topics include:

- **Exploring different gate dielectrics, or gate dielectric surface treatment**

  A key aspect of achieving high performance TFTs is the proper choice of gate dielectric. The gate dielectric quality plays an important role in determining the TFT characteristics. Device properties including subthreshold slope, leakage current, and field-effect mobility are reported to be closely related to the gate dielectric chemical composition [112, 113], and the dielectric/ semiconductor interface roughness [114]. Charge trapping in the bulk dielectric and at the dielectric/semiconductor interface has been suggested as one of the mechanisms causing electrical instability [39, 40]. Hysteresis in TFT transfer characteristics is also attributed to polarization of the dielectric/semiconductor interface via charge trapping induced by device operation [112]. Electrical performance of a-IGZO TFTs with different gate dielectrics have been reported, including silicon dioxide (SiO_2) [115-117], titanium silicon dioxide ($TiSiO_2$) [118], aluminum titanium oxide (ATO) [119], silicon nitride [25, 38, 120], hafnium oxide (HfO_2) [121], yttrium oxide [18, 19], and MgO-$Ba_{0.6}Sr_{0.4}TiO_3$ (MgO-BST) [122]. However, few works have been focused on comparison of TFT characteristics with different gate dielectric materials [114].

- **Reducing the source/drain contact resistance**

From chapter II and III, we've seen that a-IGZO directly forms low resistance contacts with the Au/Ti source/drain electrodes without further doping of the contact region. However, due to the high conductivity of a-IGZO thin films, for shorter channel (L = 10μm) TFTs, the channel resistance is only one order of magnitude higher than the source/drain contact resistance. Therefore, in high resolution applications, where small device dimension is required, a non-negligible portion of bias voltage drops across the contact and deteriorates the device performance. To solve this problem, a high conductivity a-IGZO buffer layer is needed at the metal/semiconductor interface [118, 123]. Coplanar homojunction a-IGZO TFTs have been reported by applying Ar [124, 125] or H_2 [126] plasma treatment, and by depositing hydrogenated silicon nitride (SiN_x:H) protection layer [117] to form highly conductive a-IGZO contact regions. The device performance was observed to improve with reduced contact resistance.

- **Optimization of electrical stability**

As mentioned in chapter IIV, due to the small gate overdrive voltage (V_{GS}-V_T), electrically very stable ($\Delta V_T \sim 0$) a-IGZO TFTs are required to realize AM-OLED backplane circuits. Several factors were reported to affect the electrical stability of AOS TFTs and need to be optimized, including the semiconductor chemical composition [14], the gate dielectric and the dielectric/semiconductor interface roughness [39, 40], the passivation layer [41], and the thermal annealing process [102].

- **a-IGZO TFTs on plastic substrates**

  Although a-IGZO TFTs can be fabricated at room temperature [18, 19], a post thermal annealing (>300°C) step which reduces the a-IGZO trap density is often required to improve the device electrical performance [21, 127]. However, such high temperature would not be compatible with flexible electronics fabricated on plastic substrates. Nomura et al. observed that wet O_2 annealing is more effective in enhancing the TFT performance than dry O_2 annealing, and expected that the optimization of the post annealing condition using a H_2O-containing atmosphere can reduce the post annealing temperature [21]. Nakata et al. reported on using an excimer laser to anneal the a-IGZO for an extremely short time without causing heat damage to the substrate [128], which might be suitable for applications where fabrication cost is not an issue. Of course the ultimate solution is to optimize the processing condition so that post annealing is not required.

Although a-IGZO TFTs (or other types of AOS TFTs) is a relatively new and unexplored category of thin-film devices, the potential lies in their transparency, uniformity, low processing temperature, and good electrical performance. Thus, in concluding this thesis and surveying the work done, it is reasonable to suggest that in the near future a-IGZO TFT based applications will be available, and fully transparent electronics will finally appear (not only in dreams).

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