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THREE-TERMINAL PUNCH-THROUGH DEVICES

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ABSTRACT

The objective of this investigation is to study the gate field controlled barrier injection transit-time (GFC-BARITT) device and static injection transistor (SIT) theoretically and experimentally. The GFC-BARITT device is proposed and its potential is explored.

The physics of three-terminal punch-through (TTPT) devices, SIT, metal semiconductor metal (MSM) and n^+pn^+ GFC-BARITT devices are studied in detail. The particle current injection process for various TTPT devices is examined and identified as diffusion over a gate controlled potential barrier. Dc, small-signal and large-signal ac models for the TTPT devices have been derived by using (1) drift and (2) drift-diffusion approximations. The transit-time effect is included in the small- and large-signal models. Also the small-signal noise properties of the TTPT devices are considered. The potential distribution in the device is calculated by using a two-dimensional Poisson equation solver. The level of carrier injection in GaAs GFC-BARITT devices is lower than that in silicon of InP devices. However, the level of carrier injection in SIT devices is independent of the material. To obtain high current from TTPT devices, high carrier saturation velocity and high carrier injection are required. The forward bias voltage V_F and the gate-source distance are the most critical parameters for the operation of these devices.

A noniterative large-signal model is proposed. This model was applied to the various FET devices. The results indicate that InP FETs can generate more power than either the GaAs or Si FETs. FETs are treated as a special mode of operation of the SIT device, because either an increase in the channel doping concentration or the channel width of a SIT device results in an FET mode of operation.

MSM and n^+pn^+ GFC-BARITT devices and ring oscillators were fabricated utilizing silicon on sapphire (SOS). The principles of operation of GFC-BARITT devices and their superiority over MOSFETs for digital logic circuits are discussed.

TABLE OF CONTENTS

	Page
CHAPTER I. INTRODUCTION	1
1.1 Introduction	1
1.2 Principles of Operation of Three-Terminal Punch-Through Devices	2
1.2.1 GFC-BARITT Devices	2
1.2.1a MSM GFC-BARITT Device: Current Transport Mechanism	4
1.2.2 Static Induction Transistors (SITs)	11
1.3 Outline of the Present Study	14
CHAPTER II. DEVICE PHYSICS AND DC CHARACTERISTICS OF GFC-BARITT AND SIT DEVICES	16
2.1 Device Physics	16
2.2 The GFC-BARITT Device	16
2.2.1 Diffusion Effect in the Low Field Region	19
2.2.2 Dc Current Density of a GFC-BARITT Device	28
2.2.2a Drift-Diffusion Current Approximation	28
2.2.2b Drift Current Approximation	33
2.2.3 Potential Distribution	36
2.3 Static-Induction Transistor	43
2.3.1 Physics of the SIT Device	46
2.3.2 Dc Characteristics of the SIT Device	47
2.4 Dc Characteristics of a Vertical Field-Effect Transistor	52
2.5 Thermionic Saturation of the Diffusion Current	57

Page

CHAPTER III. SMALL- AND LARGE-SIGNAL MODEL 59

3.1 Introduction 59
3.2 Small-Signal Circuit Elements 60

3.2.1 Transconductance 60

3.2.1.1 Silicon Devices 62

3.2.1.1a GFC-BARITT and SIT Devices 62
3.2.1.1b Vertical FETs 62

3.2.1.2 III-V Compound Semiconductor Devices 63

3.2.1.2a GFC-BARITT and SIT Devices 63
3.2.1.2b Vertical FETs 64

3.2.2 Conductance 64

3.2.2.1 Silicon Devices 65

3.2.2.1a GFC-BARITT and SIT Devices 65
3.2.2.1b Vertical FETs 65

3.2.2.2 III-V Compound Semiconductors 65

3.2.2.2a GFC-BARITT Devices and SITs 65
3.2.2.2b Vertical FETs 66

3.2.3 Gate-Source Capacitance 66

3.2.3a GFC-BARITT and SIT Devices 66
3.2.3b Vertical FETs 68

3.2.4 Drain-Gate Feedback Capacitance 68

3.2.4a GFC-BARITT and SIT Devices 68
3.2.4b Vertical FETs 69

3.2.5 Drain-Source Capacitance 69

3.2.5a GFC-BARITT and SIT Devices 69
3.2.5b Vertical FETs 70

Page

3.3 Diffusion Effects on Small-Signal Circuit Parameters 71

3.3.1 The Transconductance 71
3.3.2 The Conductance 72
3.3.3 The Gate-Source Capacitance 72
3.3.4 The Drain-Gate Feedback Capacitance 73
3.3.5 The Drain-Source Capacitance 73

3.4 Carrier Transit Time Effect 74

3.4.1 Silicon Devices 75
3.4.2 III-V Compound Semiconductor Devices 76

3.5 Large-Signal Analysis 77

3.5.1 Introduction 77
3.5.2 Large-Signal Circuit Parameters 78

3.5.2.1 GFC-BARITT and SIT Devices 79
3.5.2.2 Vertical FETs 82

3.5.2.2a Silicon FETs 82
3.5.2.2b III-V Compound Semiconductor FETs 86

3.6 Small-Signal Circuit Properties 88

3.6.1 Admittance Parameters 88
3.6.2 S-Parameters 91
3.6.3 Gain and Gain Bandwidth Product 93
3.6.4 The Stability Analysis 95

3.7 Large-Signal Power and Gain of the TTPT Devices 95

3.8 Noise Analysis 97

3.8.1 Introduction 97
3.8.2 Noise in Punch-Through Diodes 99
3.8.3 Noise Sources of the Three-Terminal Punch-Through Devices 100
3.8.4 The Noise Figure and the Noise Measure 103
3.8.5 The Noise Temperatures 106

Page

CHAPTER IV. DEVICE SIMULATION PROGRAM (SIM-GFC) 109

4.1 Introduction 109
4.2 Program Description 110
4.3 Material Parameters 111
4.4 Device Physics 118

4.4.1 The Potential Distribution 118
4.4.2 The Injected Carrier Distribution 127
4.4.3 The Space-Charge Effect 133

4.5 Dc Characteristics 135

4.5.1 The Impurity Concentration Effect 135
4.5.2 Temperature Effect 139
4.5.3 The Geometry Effect 144
4.5.4 Dc and Small-Signal Device Parameters 151

4.6 Small-Signal Performance 166

4.6.1 GFC-BARITT Devices 167
4.6.2 SIT Devices 177

4.7 Large-Signal Performance 197

4.7.1 Results and Discussions of the Large-Signal Operation 204

4.8 Comparison of the Different Devices 218

CHAPTER V. DEVICE FABRICATION AND MEASUREMENTS 221

5.1 Introduction 221
5.2 Material Selection 222

5.2.1 SOS Samples 225

5.3 Device Fabrication 228
5.4 Dc Characteristics 233
5.5 Introduction to Digital Circuit Applications 240

5.5.1 Basic Structure and Principles of Operation 242
5.5.2 Ring Oscillator Fabrication 245
5.5.3 Results and Discussion 246
5.5.4 Delay Time 256

5.5.4.1 A GFC-BARITT Device Inverter 256
5.5.4.2 Injection Control Logic 259

Page

5.5.5 Conclusion 260

5.6 Comparison of the Theoretical and Experimental Results 265

CHAPTER VI. CONCLUSIONS AND SUGGESTIONS FOR FURTHER STUDY 268

APPENDIX A. FACR METHOD 271

APPENDIX B. SIM-GFC PROGRAM 277

LIST OF REFERENCES 279

LIST OF FIGURES

Figure		Page
1.1	Structure of an Ideal GFC-BARITT Device.	3
1.2	MSM GFC-BARITT Device.	5
1.3	MSM GFC-BARITT Device Energy Bands.	7
1.4	Energy Band Diagram at $\|V_{DS}\| \geq \|V_{FB}\|$.	9
2.1	GFC-BARITT Device.	18
2.2	Field, Velocity and Carrier Distributions of a TTPT Device.	27
2.3	A TTPT Device.	29
2.4	SIT Device. (G = Gate, D = Drain and S = Source).	47
2.5	A SIT Device.	50
2.6	Vertical FET Structure.	53
3.1	Small-Signal Equivalent Circuit of a SIT or a GFC-BARITT Device.	61
3.2	Equivalent Circuit Used in Noise Analysis.	104
4.1	Flow Chart.	112
4.2	The Potential Distribution.	121
4.3	A Multi-Channel Surface Gate (Insulator or Schottky) TTPT Device.	126
4.4	Carrier Distribution as a Function of Distance at the Different Points Across the Channel, y and Distance Along the Conduction Path, x.	129
4.5	V_F Vrriation as a Function of V_{DS} at Different Gate Voltages (Device S2).	134
4.6	Dc Current of a SIT as a Function of the Channel Doping Concentration (Device S2).	136

Figure		Page
4.7	Dc Current of a GFC-BARITT Device as a Function of the Channel Doping Concentration (Device B1).	137
4.8	The Current Voltage Characteristics of a SIT Operating in FET and Injection (SIT) Modes (Device S1).	141
4.9	A GFC-BARITT Device Current as a Function of the Channel Doping at T = 400°K (Device B1, Compared to Fig. 4.7 at T = 300°K).	143
4.10a	The Gate-Source Spacing, W_{GS}, Effect on the I-V Characteristics of a GFC-BARITT Device.	146
4.10b	The Gate-Source Spacing, W_{GS}, Effect on the I-V Characteristics of a GFC-BARITT Device.	147
4.11a	The I-V Characteristics of the Vertical FETs.	148
4.11b	The I-V Characteristics of the Vertical FETs.	149
4.11c	The I-V Characteristics of the Vertical FETs.	150
4.12a	Small-Signal Parameters of a GFC-BARITT Device as a Function of V_{DS} for Different Values of V_{GS} (Device B2).	153
4.12b	Small-Signal Parameters of a GFC-BARITT Device as a Function of the V_{DS} with Different V_{GS} Voltages (Device B2).	154
4.12c	The Small-Signal Parameters of a GFC-BARITT Device as a Function of the V_{DS} with Different V_{GS} Voltages (Device B2).	155
4.12d	Small-Signal Parameters of a GFC-BARITT Device as a Function of the V_{DS} with Different V_{GS} Voltages (Device B2).	156
4.13a	The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3.	158
4.13b	The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3.	159

Figure | Page
4.13c The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3. 160
4.13d The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3. 161
4.14a The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4. 162
4.14b The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4. 163
4.14c The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4. 164
4.14d The Small-Signal Equivalent Circuit Parameters of A GaAs FET, S4. 165
4.15a The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of the V_{DS} at Different Frequencies 0.1 to 0.6 GHz. (V_{GS} = 0 V) 168
4.15b The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of the V_{DS} at Different Frequencies 0.1 to 0.6 GHz. (V_{GS} = 0 V) 169
4.15c The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of the V_{DS} at Different Frequencies 0.1 to 0.6 GHz. (V_{GS} = 0 V) 170
4.15d The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of the V_{DS} at Different Frequencies 0.1 to 0.6 GHz. (V_{GS} = 0 V) 171
4.15e The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of the V_{DS} at Different Frequencies 0.1 to 0.6 GHz. (V_{GS} = 0 V) 172

Figure		Page

4.15f	The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of the V_{DS} at Different Frequencies 0.1 to 0.6 GHz. (V_{GS} = 0 V)	173
4.16a	The Transit-Time Effect on the Small-Signal Device Performance of Device B4.	175
4.16b	The Transit-Time Effect on the Small-Signal Device Performance of Device B4.	176
4.17a	The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel Doping.	178
4.17b	The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel	179
4.17c	The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel	180
4.17d	The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of	181
4.17e	The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of the Channel Doping.	182
4.17f	The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of the Channel Doping.	183
4.18a	The Small-Signal Performance of a GaAs SIT, S6 as a Function of the V_{DS}. (V_{GS} = 0 V)	184
4.18b	The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V)	185
4.18c	The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V).	186
4.18d	The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V)	187
4.18e	The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V)	188

Figure		Page

4.18f	The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V)	189
4.19a	The Small-Signal Performance of a SI SIT, S2 as a Function of the Channel Doping, N_D. (V_{DS} = V_{pt} + 8 V and V_{GS} = -3 V)	191
4.19b	The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping, N_D at Different Frequencies.	192
4.19c	The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping, N_D at Different Frequencies. (V_{DS} = V_{PT} + 8 V and V_{GS} = -3 V)	193
4.19d	The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping , N_D at Different Frequencies. (V_{DS} = V_{PT} + 8 V and V_{GS} = -3 V)	194
4.19e	The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping N_D at Different Frequencies. (V_{DS} = V_{PT} + 8 V and V_{GS} = -3V)	195
4.19f	The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping at Different Frequencies. (V_{DS} = V_{PT} + 8 V and V_{GS} = -3 V)	196
4.20	A Large-Signal Amplifier Circuit.	198
4.21	The Current and Voltage Waveforms under Large-Signal Conditions.	202
4.22a	The Large-Signal Performance of a GaAs FET (Device S7) at 5.0 GHz.	206
4.22b	The Large-Signal Performance of a GaAs FET (Device S7) at 5.0 GHz.	207
4.22c	The Large-Signal Performance of a GaAs FET (Device S7) at 5.0 GHz.	208
4.23a	The Large-Signal Performance of an InP FET (Device S8) at 5.0 GHz.	209
4.23b	The Large-Signal Performance of an InP FET (Device S8) at 5.0 GHz.	210
4.23c	The Large-Signal Performance of an InP FET (Device S8) at 5.0 GHz.	2.11

Figure		Page

4.24	The Output Power of a Si FET (Device S9) at 5.0 GHz as a Function of the Input Powers.	212
4.25a	The Large-Signal Performance of an InP FET (Device S8) as a Function of Frequency.	213
4.25b	The Large-Signal Performance of an InP FET (Device S8) as a Function of Frequency.	214
4.25c	The Large-Signal Performance of an InP FET (Device S8) as a Function of Frequency.	215
5.1	Profile of the Ion Implanted Impurities.	227
5.2	Fabrication Processes of the MSM and Junction (J) GFC-BARITT Devices.	229
5.3	Ideal Schottky Barrier GFC-BARITT Device.	234
5.4	Fabricated GFC-BARITT Device.	235
5.5	$n^+p^-n^+$ Device (Z = 0.2025 cm, L_G = 5 μm and L_{DS} = 20 μm).	236
5.6	MSM GFC-BARITT Device. (Z = 500 μm, L_{SG} = 2.5 μm, L_{GD} = 12.5 μm, and 0.5 μm thick).	237
5.7	Insulated Gate $n^+n^-n^+$ SIT Device. (Z = 125 μm, L_{SG} = 3.5 μm, L_{GS} = 10 μm, L_{DS} = 30 μm, and 0.5 μm thick).	238
5.8	$n^+p^-n^+$ GFC-BARITT Device. (Z = 125 μm, L_{SG} = 5 μm, L_{GS} = 10 μm, L_{DS} = 30 μm, and 0.5 μm thick).	241
5.9	Inverter Structures.	243
5.10	Fabrication Steps.	247
5.11	Photomicrograph of the Five-Stage Ring Oscillators.	248
5.12	Output Waveforms of the Complementary ICL Ring Oscillator.	249
5.13	Output Waveforms of the CMOS/SOS Ring Oscillator.	250
5.14	Switching Speed of the Injection Controlled Logic Gate as a Function of the Power Dissipation.	251

Figure		Page
5.15	Switching Speed of the Punch-Through Logic Gate as a Function of Power Dissipation	252
5.16	GFC-BARITT Device Inverter Circuit with a Capacitive Load.	257
5.17	ICL inverter Circuit with a Capacitive Load.	261
5.18	Inverter Structure for Semiconductors with High Electron Mobilities.	263

LIST OF TABLES

Table		Page
1.1	Potential Power Devices	14
2.1	Power Performance of SITs	45
4.1	List of the Devices	119
5.1	Energy Bandgap for Various Semiconductor Materials.	224
5.2	Ion-Implantation Data	226

LIST OF SYMBOLS

A**	The effective Richardson's constant.
D	One half of the device thickness.
D_n	Diffusion coefficient.
D_p, D_n	The hole and electron diffusion coefficients.
E	Electric field.
E_c	The field at the peak velocity.
E_{FB}	The field at the forward-biased junction side.
E_{RB}	The maximum field at the reverse-biased junction side.
E_{sat}	The field where velocity reaches half of the saturated velocity.
f	Frequency.
f_T	Cut-off frequency.
$f_{2\pi}$	Frequency where the phase delay becomes 2π.
F	The noise figure.
G	The carrier generation rate.
$J_o = qv_{sat}n_p$	Current density.
J_p, J_n	Hole and electron current densities, respectively.
J_{so}	Maximum current density of a BARITT diode.
k_1	A constant.
k_2	A constant.
L_{DS}	Channel length.
L_F	Length of the depletion layer from the forward-biased junction side.

L_n Diffusion length for electrons.

L_R Length of the depletion layer from the reverse-biased junction side of the n^+pn^+ diode.

L_S Distance between the source and the point where the velocity of carrier saturates.

m^* Effective mass of electrons.

M Noise measure.

n Electron density.

n_i Intrinsic carrier density.

$n_{inj}(I)$ Density of the injected carriers at the Ith segment.

n_{po} Minority carrier density at thermal equilibrium.

n_s Source doping concentration.

$n_{th} = N_D$ SIT.

N Number of segments or BARITT diodes of a GFC-BARITT device.

N Number of channels.

N_A Impurity concentration of the p-type semiconductor.

N_D Impurity concentration of the n-type semiconductor.

p Hole density.

P_{DC} Dissipated power.

P_{in} RF input power.

P_o Output power.

p_t, n_t Hole and electron densities which would exist if the Fermi level coincided with the trap level.

r_o A constant which is less than unity.

r_s Source resistance.

Re The "real part".

R_f Thermal noise of the source parasitic resistance.

R_m	Thermal noise of the gate parasitic resistance.
t	Time.
T	Temperature in °K.
T_{OFF}	Turn-off time of an inverter.
T_{ON}	Turn-on time of an inverter.
V	Voltage.
$v(x)$	Carrier velocity as a function of the local electric field along the conduction path.
v_p, v_n	Hole and electron drift velocities (dependent upon E).
v_{sat}	Saturated velocity.
V_{o1}	Initial output voltage.
V_{o2}	Final output voltage.
V_{TE}	Velocity of the thermionic emission over a potential barrier of zero height.
V_B	Built-in potential of a p-n junction of an MSM BARITT diode.
V_{B1}	Total barrier height.
V_{B2}	Built-in potential between the gate and channel.
V_F	Forward biasing voltage across the source-channel junction.
V_{FB}	Flat band voltage.
$V_F(I)$	Forward bias voltage at the Ith segment.
V_{PTG}	Punch-through voltage for the distance of L_{DS}-L_G.
V_{GS}	Source gate voltage.
$V_T = kT/q$	k is the Boltzmann constant and q is the electronic charge.
W_{GS}	Distance between the source and the gate.
W_s	Channel width.
x	Distance that carriers travel in the conduction path.
y_{in}	Input admittance.

Y_L	Load admittance.
Z	Gate width.
Z_s	Impedance of the noise source.
$\alpha(I)$	Barrier modulation parameter.
α_p, α_n	Hole and electron ionization coefficients.
Δf	Frequency bandwidth.
η_a	Power efficiency.
η_c	Collector efficiency.
ϕ	Forward bias due to V_{DS}.
ϕ_G	Barrier height inducted by the gate-source voltage.
$\phi_G(I)$	Potential of the Ith segment along the y-direction due to applied gate-source voltage.
ϕ_{n_1}	Minimum barrier height of a metal-semiconductor junction (Schottky barrier).
ϕ_{so}	Junction potential barrier.
θ	Delay angle due to transit time.
τ_p, τ_n	Hole and electron lifetimes.
ω	Angular frequency.

CHAPTER I. INTRODUCTION

1.1 Introduction

This study is concerned with basic device theory and modelling of Three-Terminal Punch-Through (TTPT) devices, such as Gate-Field-Controlled Barrier Injection Transit Time (GFC_BARITT) and Static Induction Transistor [1] (SIT) devices. Even though the operating principles of these two devices are different, both can be characterized by the same type of mathematical expressions. The theory developed in this study directly pertains to n^+pn^+ and Metal Semiconductor-Metal (MSM) GFC-BARITT devices, and $n^+n^-n^+$ SITs. The results can be easily adapted to the analysis of the other device structures, such as p^+np^+ GFC-BARITT and $p^+p^-p^+$ SIT devices.

As a result of the low gate-source capacitance and the parasitic capacitance, and the high transconductance of TTPT devices in general, they are capable of operation at high frequencies. The experimental studies of SIT devices indicate that they are promising in the areas of high frequency and high power analog circuit applications [2]. Although there has been some experimental work on SIT devices [1] and [3], there have been no published studies on the theoretical capabilities and limitations of TTPT devices. For these reasons, this present study will focus on the theoretical constraints of the maximum frequency of operation of TTPT devices. An experimental study of the switching speed of SOS GFC-BARITT

devices to show their feasibility for digital circuit applications and the fabrication of a new MSM GFC-BARITT device are also included.

1.2 Principles of Operation of Three-Terminal Punch-Through Devices

There are two types of TTPT devices. These are (a) the minority carrier devices such as the GFC-BARITT and Lateral Punch Through Transistor [4], and (b) the majority carrier devices such as the junction gate SIT and the insulated gate SIT devices. In all these devices, the carrier injection, either majority or minority, is controlled by a third electrode. This electrode can be an insulated gate as in the GFC-BARITT devices, a junction gate as in SIT devices or an ohmic-contact gate as in Lateral Punch-Through Transistors. In the following sections, the GFC-BARITT and SIT devices will be considered.

1.2.1 GFC-BARITT Devices. The principles of operation of a MSM GFC-BARITT device are presented here for the first time and a procedure for fabrication in silicon on sapphire (SOS). The GFC-BARITT device is characterized by a narrow insulated gate close to the forward-biased junction of a two-junction device as shown in Fig. 1.1. This structure includes $n^+n^-n^+$, $n^+p^-n^+$, $p^+p^-p^+$, $p^+n^-p^+$, MSM-type structures, and also some of the space-charge limited triodes [5] and [6]. Depending on the type of structure used, a GFC-BARITT device can be (i) a minority-carrier type (n^+pn^+, p^+n^+p and MSM structures) or (ii) a majority-carrier type ($n^+n^-n^+$ and $p^+p^-p^+$ structures). A SIT device is a special type of majority

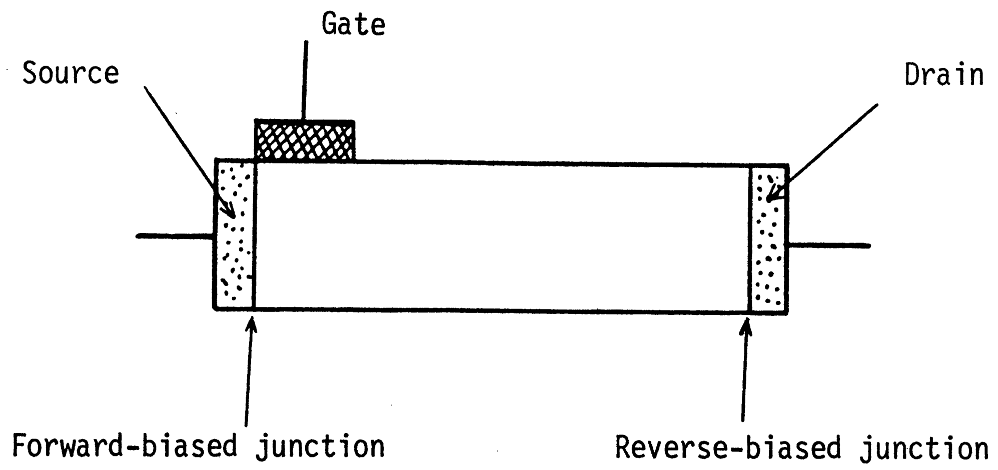


Fig. 1.1 Structure of an Ideal GFC-BARITT Device.

carrier device which uses a junction gate instead of an insulated gate.

In a minority-carrier type of structure, the carrier injection is controlled by a reverse-biased junction in a punch-through diode such as that found in MSM, p^+np^+ or n^+pn^+ type of BARITT diodes. An insulated gate electrode has been added to a BARITT diode to control the injection through the gate. A two-terminal diode then becomes a three-terminal device with all the features of a transit-time device. The advantages of a three-terminal device over a two-terminal device are: (i) a three-terminal device requires simple circuitry, and (ii) its efficiency is also much higher than that of a two-terminal device.

The operation of a pn junction-type GFC-BARITT device can be summarized as the control of the injection of the minority carriers from the source to the channel through an insulated gate. Even though the same principle holds true for the injection of the minority carriers in a MSM GFC-BARITT device, the details of the current transport of a MSM device are different from that of a p-n junction type device. Because of this difference the following section elaborates on the current transport mechanism of a MSM GFC-BARITT device.

1.2.1a _MSM GFC-BARITT Device: Current Transport Mechanism._ A MSM BARITT device with an insulated gate in the close vicinity of the forward-biased junction is shown in Fig. 1.2. A MSM BARITT diode allows current to flow when the applied bias voltage exceeds a critical voltage across the drain-source terminals. The critical

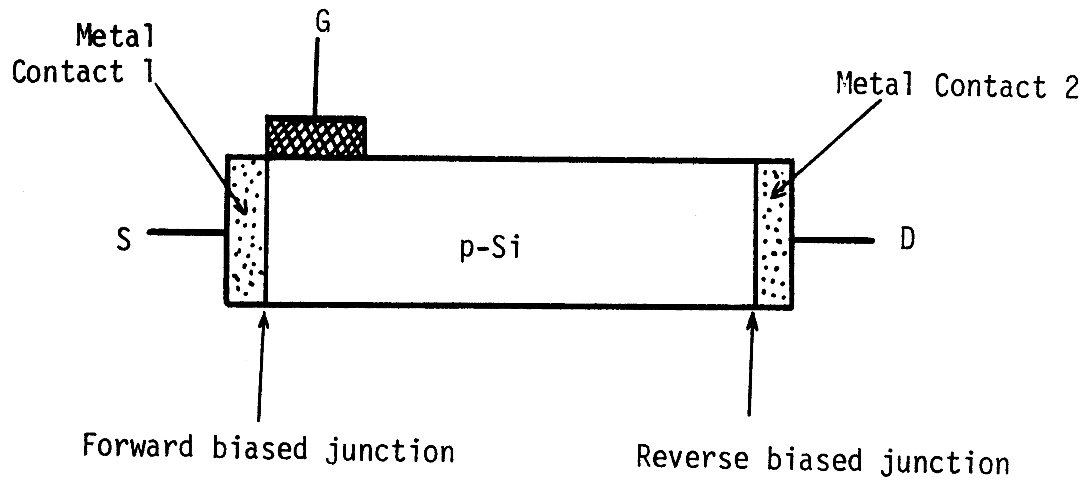


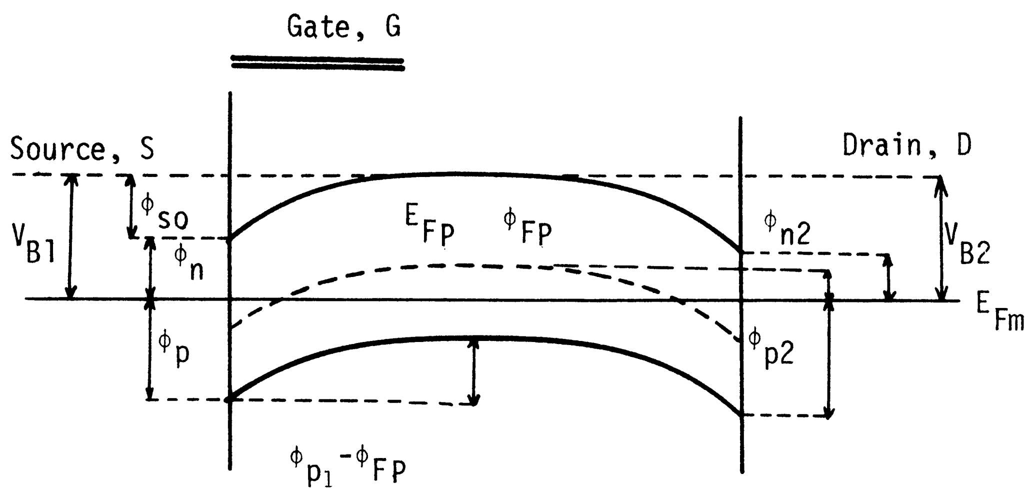
Fig. 1.2 MSM GFC-BARITT Device.

voltage is referred to as the punch-through (V_{PT}) or the reach through (V_{RT}) voltage at which the depletion regions of the forward and reverse biased junctions are joined together. For voltages in excess of V_{PT}, the barrier height between contact 1 metal (the source) and the semiconductor will be lowered. This is illustrated in Figs. 1.3(a) and 1.3(b). As a result of this lowering of the barrier, electrons from the metal will be injected into the semiconductor by way of thermionic emission. The current transport mechanism of an MSM BARITT diode prior to punch-through has been analyzed in [7] and is outside the scope of this present study.

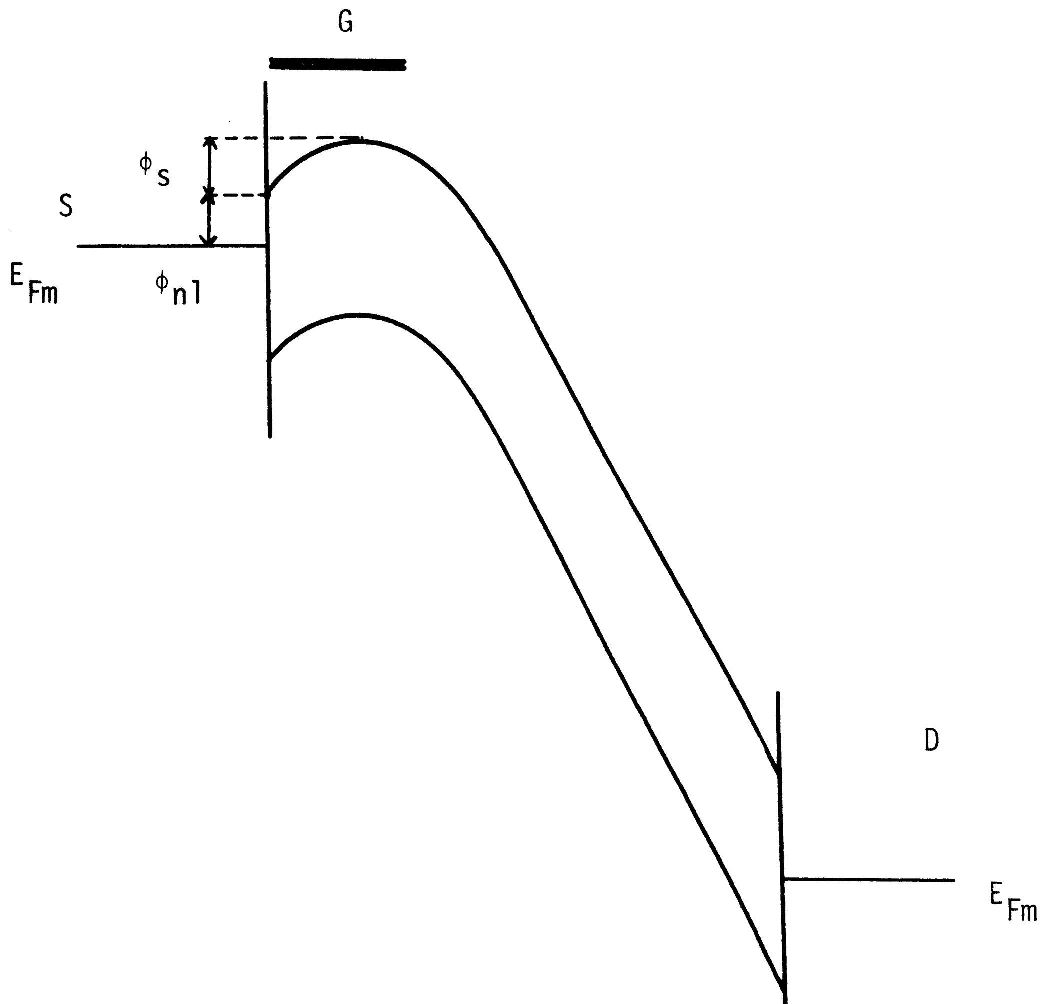
In Fig. 1.3(a), the initial energy band diagram and the barrier heights are indicated. In that figure, $\phi_{p1}-\phi_{FP}$ is the Schottky barrier height against the holes in the p-type semiconductor. ϕ_{n1} is the minimum barrier height against the electron injection from metal to semiconductor. ϕ_{so} is the junction potential barrier also against the electron injection. V_{B1} is the final barrier height for the electron injection at contact 1. At contact 2, the same symbols with index number 2 have the same meaning as those in contact 1. However, in Fig. 1.3(b), the total barrier height against the electrons is reduced. The electron current can be approximated as in Eq. 1.1, by following Sze's treatment [7]:

$$J_{DS} = A^{**}T^2 \, \mathrm{DEXP}(-V_{B1}/V_T) \quad , \qquad (1.1)$$

where A** is the effective Richardson's constant, T is the temperature in degrees Kelvin, and V_{B1} is the total barrier height against



(a) At thermal equilibrium.



(b) At $V_{DS} \geq V_{PT}$ (beyond punch-through).

Fig. 1.3 MSM GFC-BARITT Device Energy Bands.

electron injection and $V_T = kT/q$ where k is the Boltzmann constant and q is the electronic charge.

As the voltage is increased further, a point is reached at which the energy band at contact 1 become flat. This is the flat band condition with the corresponding flat band voltage, V_{FB}. For voltages in excess of V_{FB}, the energy band is bent further down. If the length of the p-semiconductor is L_{DS}, the corresponding flat band voltage expression is given by

$$V_{FB} = \frac{qN_A}{2\varepsilon_s} L_{DS}^2 , \tag{1.2}$$

where N_A is the impurity concentration of the p-semiconductor and ε_s is the semiconductor permittivity.

The increase in the applied voltage V_{DS} between the V_{PT} and V_{FB} voltages results in an exponential increase of the electron current. The electron current, however, increases slowly with V_{DS} in excess of V_{FB}. This current increase is due to the barrier lowering effect of the electric field shown in Fig. 1.4. The reduction in barrier height is given by Eq. (1.3):

$$\Delta\phi_{n1} = \left(\frac{q(V_{DS} - V_{FB})}{4\pi\varepsilon_s L_{DS}} \right)^{1/2} . \tag{1.3}$$

The minimum barrier height, ϕ_{n1} is one of the main differences between a pn junction (n^+pn^+ or p^+np^+) and a MSM BARITT diode.

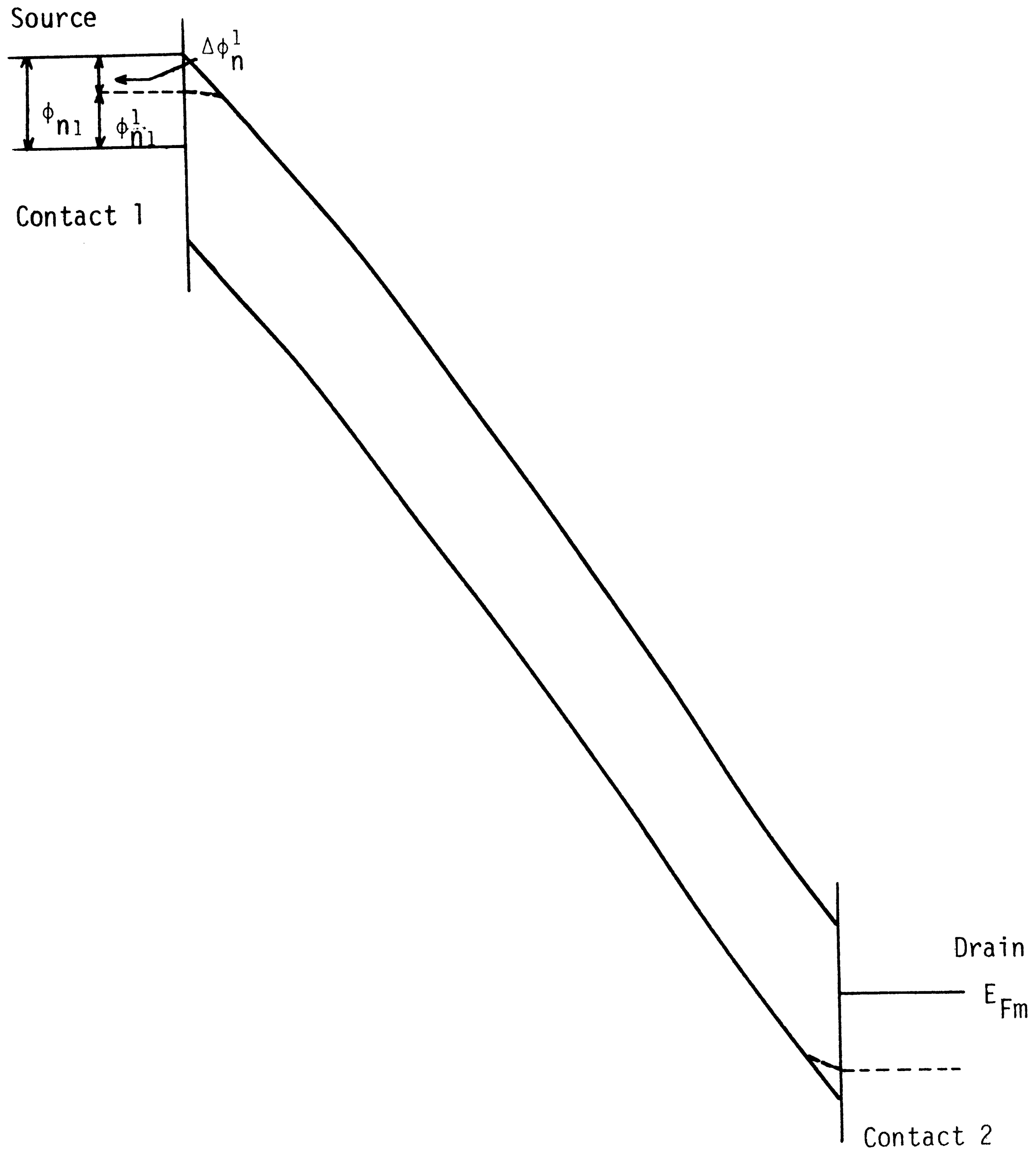


Fig. 1.4 Energy Band Diagram at $|V_{DS}| \geq |V_{FB}|$.

Unlike a MSM BARITT diode in which the metallurgy determines the minimum barrier height, the pn junction type BARITT diode has no such characteristic. There is, however, a space-charge limitation to the injection of the minority carriers in the case of a pn junction type BARITT diode. If ϕ^{1}_{n1} ($\phi^{1}_{n1} = \phi_{n1} - \Delta\phi_{n}$) is high, a MSM BARITT diode biased even at voltages in excess of V_{PT}, does not show its usual exponential current voltage (I-V) characteristic until the avalanche breakdown occurs. This unique characteristic of a MSM diode distinguishes it from other pn junction type diodes.

In the discussion given above, the assumption was made that the doping concentration was light enough and the length of the semiconductor was long enough so that the flat band condition occurs before avalanche breakdown occurs at the reverse-biased junction. In this analysis, neither the role of an insulated gate close to the forward biased junction (contact 1), nor the effect of the diffusion of the injected carriers at the low field region on the I-V characteristics have been considered.

The following discussion considers the effect of the insulated gate on the I-V characteristics of an M-pS-M BARITT diode. The applied gate voltage will modify the minimum barrier height ϕ^{1}_{n1} of the forward biased junction of a MSM BARITT device. For a positive gate voltage, the barrier height V_{B1} and the minimum barrier height of an MSM BARITT diode are lowered. This is why a M-pS-M GFC-BARITT device is able to conduct higher currents than a conventional M-pS-M BARITT diode of the same size. However, if the gate voltage is negative, the current flow will be reduced.

<u>1.2.2 Static Induction Transistors (SITs)</u>. One can characterize a SIT as a three-terminal punch-through device, even though the punch-through occurs between the gate and the drain rather than between the source and the drain. If the channel of a vertical FET is lightly doped, then the whole channel will be depleted at the pinch-off condition. If the drain-source voltage is further increased beyond the pinch-off condition, the FET operates as a SIT, assuming that the drain-gate breakdown does not occur.

The SIT is a majority carrier injection-type device. Only the Dc analysis of this device has been undertaken [1]. The Dc current expressions for different approximations are given by

$$I_{DS} = q\left[\frac{kT}{2\pi m^*}\right]^{1/2} An_s \exp\left[-\left(\frac{\phi + r_o V_{GS}}{V_T}\right)\right] \tag{1.4}$$

for the thermionic emission approximation and

$$I_{DS} = qA\frac{D_n}{L_n} n_s \exp\left[-\left(\frac{\phi + r_o V_{GS}}{V_T}\right)\right] \tag{1.5}$$

for the diffusion approximation.

The following expressions are given for the multi-channel SIT device in [3]:

$$I_{DS\phi} = A\int_{-D}^{+D} \exp\left[-\frac{\phi(y) - (V_{GS}(y) - I_{DS}r_s)}{V_T}\right] dy \tag{1.6}$$

and

$$I_{DS} = I_{DS1} I_{DS\phi}$$

for the thermionic approximation and

$$I_{DS} = I_{DS2} I_{DS\phi}$$

for the diffusion approximation.

Where

$$I_{DS1} = qn_s \left(\frac{kT}{2\pi m^*}\right)^{1/2} N \quad ,$$

$$I_{DS2} = q \frac{D_n}{W_G} n_s N \quad ,$$

D_n = diffusion coefficient,

L_n = diffusion length

N = number of channels,

r_o = a constant which is less than unity,

r_s = source resistance

k = Boltzmann constant,

m^* = effective mass of electrons,

W_{GS} = the distance between the source and the gate

$A = ZW_s$

Z = gate width

W_S = channel width

n_s = the source doping concentration

ϕ = forward bias due to V_{DS} and

V_{GS} = the source gate voltage.

As the published reports indicate, the SIT is a high power device [2], [8]. The major limitation of a SIT device is that its performance is too process-sensitive as reported in [9] and [10]. This makes it difficult to fabricate reproducible SIT devices. The process sensitivity of the SIT as a power device is not as critical as in the case of digital circuit applications.

A summary of the principles of operation and limitations of various TTPT devices including SIT devices are listed in Table 1.1.

1.3 Outline of the Present Study

The objective of this study is to carry out a theoretical and experimental investigation of the capabilities and limitations of TTPT GFC-BARITT and SIT devices. Analytical equations, mainly circuit models and computer solutions of the analytical device expressions are utilized to determine dc small-signal, noise, and large signal behavior of these devices.

In Chapter II, dc expressions for the GFC-BARITT and SIT devices are derived for different semiconductors, dc expressions are given for three different simplified cases: (i) a drift-diffusion approximation, (ii) a drift approximation, and (iii) a thermionic diffusion approximation.

In Chapter III, small-signal, noise, and large-signal models for GFC-BARITT and SIT devices are discussed. Also, the effect of the transit time on the performance of these devices are considered. The carrier temperature variation as a function of the electric field, and its effect on the device noise is also accounted for.

Table 1.1

Potential Power Devices

Device	Type	Conduction	Modulation	Major Limitation
GFC-BARITT n^+pn/p^+np^+	minority carrier	injection of minority carriers	through an insulated gate	insulated gate technology
$n^+n^-n^+$/ $p^+p^-p^+$	majority carrier	injection of majority carriers	through an insulated gate	insulated gate technology
MSM	minority carrier	thermionic emission or injection of minority carriers	through an insulated gate	insulated gate technology
SIT $n^+n^-n^+$	majority carrier	injection of majority carriers	reverse bias pn junction	limited voltage swing
Lateral punch-through transistor	minority carrier	injection of minority carriers	ohmic gate	limited voltage swing due to ohmic gate (high gate current)

In Chapter IV, the outline of a computer program is developed which calculates the Dc current voltage characteristics, the small signal circuit gain, and noise, and large-signal circuit gain and efficiency of TTPT devices. In addition, a simple model for the vertical field effect transistors is included in the simulation program (SIM-GFC). All of the calculations can be extended to silicon and/or III-V compound semiconductors, such as GaAs and InP.

In Chapter V, the fabrication, design, and testing of a GFC-BARITT device are given. The resulting experimental and theoretical data are then compared.

Finally, in Chapter VI, a summary of the results of this work, and some suggestions are given for the further study of the TTPT devices.

CHAPTER II. DEVICE PHYSICS AND DC CHARACTERISTICS OF GFC-BARITT AND SIT DEVICES

2.1 Device Physics

This chapter presents a discussion of the physics of two types of punch-through semiconductor devices. These are:

(a) A majority carrier device which is called a static induction transistor [1] and

(b) A minority carrier device which is proposed and studied for the first time here, the GFC-BARITT device. This is basically a barrier injection transit-time device with a third terminal which controls the injection of the carriers from the source to the channel.

Both of these devices are two-dimensional and it is difficult to derive analytical expressions for the device parameters. Therefore, where possible, analytical expressions have been used along with some numerical approximations. Expressions for the dc current and voltage characteristics include a field-dependent velocity expression to account for the effect of the velocity saturation in the drift region and the effect of the carrier diffusion at the low-field region. A simplified solution of the carrier distribution is also given.

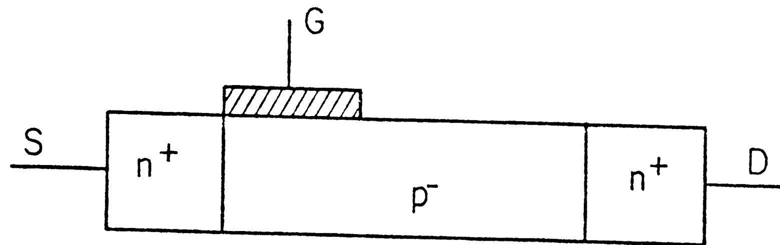
2.2 The GFC-BARITT Device

Although the device theory that is developed throughout this chapter is general in nature, only the n^+pn^+ abrupt-junction

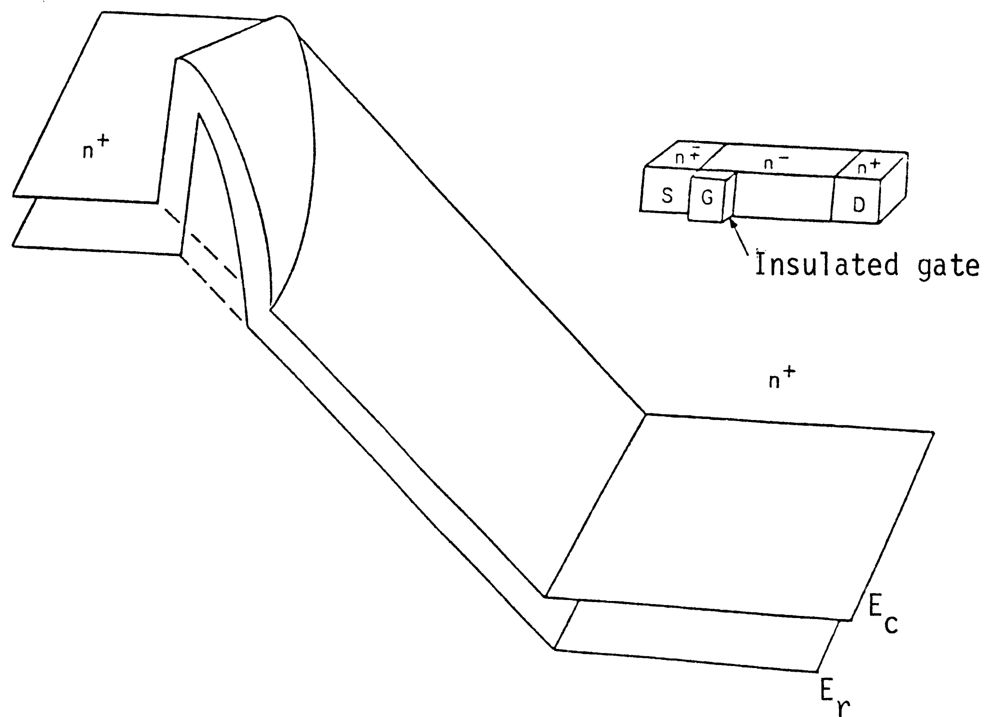
uniformly doped silicon and GaAs or InP structures will be dealt with in detail. A Gate Field Controlled BARITT device (GFC-BARITT) is a BARITT with an insulated gate. Adding an insulated gate to the source side of the BARITT structure results in a GFC-BARITT device. A typical device structure which is considered in this study is shown in Fig. 2.1(a). A two-dimensional band structure of a GFC-BARITT device is shown in Fig. 2.1(b). The principle of operation of this device is based on the control of the injection of carriers from the source electrode into the fully depleted channel through an insulated gate. This device looks and acts like a BARITT diode from the drain side and responds like a MOSFET from the gate side.

Although the operating principle is simple, the description of the characteristics of the device is complicated. In general, this device exhibits the disadvantages of a BARITT diode such as (i) space charge limitation of the injection of the minority carriers (self limitation) and (ii) diffusion effects at the low field region. It also has some advantages over BARITT diodes such as (i) a three-terminal device can be used in microwave and high-speed circuits, (ii) since the gate is insulated, the only limitation on RF input voltage is the gate breakdown voltage and (iii) Class B and C amplifiers can be realized with this device. Changing the polarity of the gate voltage either enhances or suppresses the injection of the minority carriers. As a result the drain-source current can be modulated.

The structure shown in Fig. 2.1(a) is an n^+pn^+ abrupt-junction GFC-BARITT device. One can describe the device operation physically



(a) Ideal device structure.



(b) Two-dimensional energy band diagram.

Fig. 2.1 GFC-BARITT Device.

as the injection of carriers from one terminal, modulation of these injected carriers through a second terminal (gate), their drift in a high-field region, and the collection of the carriers at the third terminal. Physically abrupt-junctions are not necessary. They can be either a graded junction or a Schottky barrier but the gate has to be insulated. Throughout this study uniformly doped n^+pn^+ structures are considered for simplicity.

2.2.1 Diffusion Effect in the Low Field Region. The exact distribution of the injected carriers requires the simultaneous solution of the basic semiconductor device equations. These are Poisson's equation and the hole and electron continuity equations together with several auxiliary equations which relate the basic solution variables (hole density, electron density and voltage) to the electric field, current density and charge generation. The equations are:

Principal Equations:

$$\nabla^2 V = \frac{q}{\varepsilon_s}(n - p - N_D) \quad , \tag{2.1}$$

$$\frac{\partial p}{\partial t} = -\mathrm{div}(J_p/q) + G \tag{2.2}$$

and

$$\frac{\partial n}{\partial t} = \mathrm{div}(J_n/q) + G \quad . \tag{2.3}$$

Auxiliary Equations:

$$E = -\text{grad } V \quad , \tag{2.4}$$

$$J_p/q = pv_p - D_p \text{ grad } p \quad , \tag{2.5}$$

$$J_n/q = -nv_n + D_n \text{ grad } n \tag{2.6}$$

and

$$G = \alpha_p |J_p/q| + \alpha_n |J_n/q| + \frac{pn - n_i^2}{\tau_p(n + n_t) + \tau_n(p + p_t)} \quad . \tag{2.7}$$

The variables in Eqs. 2.1 through 2.7 are defined as follows:

V = the voltage,

p = the hole density,

n = the electron density,

N_D = the doping density (positive for donors, negative for acceptors),

t = time,

J_p, J_n = the hole and electron current densities, respectively,

G = the carrier generation rate,

E = the electric field,

D_p, D_n = the hole and electron diffusion coefficients,

v_p, v_n = the hole and electron drift velocities (dependent upon E),

α_p, α_n = the hole and electron ionization coefficients,

τ_p, τ_n = the hole and electron lifetimes,

n_i = the intrinsic carrier density and

p_t, n_t = the hole and electron densities which would exist if the Fermi level coincided with the trap level.

The generation recombination term, Eq. (2.7) contains the effects of impact ionization and trapping. Both of the terms will be neglected under the low-field punch-through operating conditions.

In this analysis, however, the exact solutions of the basic device equations (Eq. 2.1 through Eq. 2.3) will not be attempted. Instead, Poisson's equation is solved for low injections to determine the potential distribution. Then the barrier height and the location of the point of the carrier injection are determined. From the known potential distribution, the distribution of the injected carriers can be determined by solving only one continuity equation. Since TTPT devices are monopolar devices, the effects of only the injected carriers are important.

Since for an $n^+p^-n^+$ and M-pS-M GFC-BARITT and $n^+n^-n^+$ SIT devices, the electrons are injected carriers, the problem to be solved is

$$\frac{\partial n_p(x,t)}{\partial t} = -\frac{1}{q}\,\mathrm{div}(J_n) \quad , \tag{2.8}$$

where n_p is the density of the injected carriers.

In the steady state, Eq. (2.8) reduces simply to

$$\frac{1}{q}\,\mathrm{div}(J_n) = 0 \quad . \tag{2.9}$$

At the low field region, the current density is given by

$$J_n = q n_p(x)\mu_n E(x) + q D_n \frac{\partial n_p}{\partial x} \quad . \tag{2.10}$$

Assuming that the electric field is a linear function of the distance along the conduction path, x, the electric field can be expressed as

$$E(x) = \frac{2(V_{DS} + V_B)}{L_{DS}^2}\, x \quad , \tag{2.11}$$

where V_{DS} is the applied voltage between the drain and the source, V_B is the built-in potential of the n^+p junction between the drain or source and the channel, and L_{DS} is the length of the channel or distance between the drain and the source electrodes.

By defining

$$\gamma = \frac{2(V_{DS} + V_B)}{L_{DS}^2}$$

Eq. (2.11) becomes

$$E(x) = \gamma x \quad . \tag{2.12}$$

Using Eq. (2.12) in the expression of the current density yields

$$J_n(x) = qn_p(x)\mu_{no} E(x) + qD_n n_p' \quad , \qquad (2.13)$$

where μ_{no} is the low-field mobility and n_p' is the first derivative of $n_p(x)$ with respect to x.

In Eq. (2.13), mobility variation along the path of conduction x is omitted for simplicity. This is a valid assumption for the first-order approximation, since Eq. (2.13) is only valid at the low field region.

Finally, the continuity equation (Eq. 2.9) results in

$$qD_n n_p'' x + qn_p'(x)\mu_{no}\gamma x + q\mu_{no}\gamma n_p(s) = 0 \quad , \qquad (2.14)$$

where $n_p''(x)$ is the second derivative of $n_p(x)$ with respect to x. After further simplification Eq. (2.14) becomes

$$n_p''(x) + \alpha x n_p'(x) + \alpha n_p(x) = 0 \quad , \qquad (2.15)$$

where

$$\alpha = \frac{2V_{DS}}{L_{DS}^2 V_T} \quad ,$$

$$V_T = kT/q$$

and k is the Boltzmann constant, and T is the temperature in degrees Kelvin. After rearranging and integration Eq. (2.15) over x, the

second-order nonlinear differential equation reduces to a first-order differential equation:

$$\frac{d}{dx}\left[n_p'(x) + \alpha x n_p(x)\right] = 0 \ . \qquad (2.16)$$

Therefore

$$n_p'(x) + \alpha x n_p(x) = k_1 \ , \qquad (2.17)$$

where k_1 is a constant. Rewriting Eq. (2.17) as in Eq. (2.18):

$$\frac{dn_p(x)}{dx} + \alpha x n_p(x) = k_1 \qquad (2.18)$$

and then rearringing Eq. (2.18) results in

$$\frac{dn_p(x)}{n_p(x)} + \alpha x \, dx = k_1 \frac{dx}{n_p(x)} \ . \qquad (2.19)$$

Now Eq. (2.19) can be integrated over x which yields

$$\ln(n_p(x)) + \frac{1}{2}\alpha x^2 - \ln k_2 = k_1 \int \frac{dx}{n_p(x)} \ . \qquad (2.20)$$

The right-hand side of Eq. (2.20) can be approximated as $k_1(x/n_{sat})$ to obtain an analytical solution where n_{sat} is the carrier density at a point, L_S, where the velocity of the carriers saturate. Equation (2.20) then becomes

$$\ln(n_p(x)/k_2) + 0.5\ \alpha x^2 \approx k_1 \frac{x}{n_{sat}} \quad . \tag{2.21}$$

Finally, $n_p(x)$ can be obtained from Eq. (2.21) and expressed as

$$n_p(x) = k_2 \exp[-0.5\ \alpha x^2 + k_1(x/n_{sat})] \quad . \tag{2.22}$$

Applying the boundary conditions to Eq. (2.22), k_1 and k_2 can be found:

(i) the first boundary is the injection point at $x = 0$

$$n_p(x)_{x=o} = n_{inj} \quad \text{this gives} \quad k_2 = n_{inj} , \tag{2.23}$$

where n_{inj} is the density of the injected carriers into the channel and

(ii) the second boundary is a virtual point where the carrier velocity saturates. This boundary was introduced by McCleer [11] and gives the following:

$$n_p(x)|_{x=L_S} = n_{sat} \quad ,$$

$$n_{sat} = n_{inj} \exp(-0.5\ \alpha L_S^2 + k_1 L_S/n_{sat})$$

and

$$k_1 = n_{sat}\left[0.5\ \alpha L_S - \frac{\ln(n_{inj}/n_{sat})}{L_S}\right] \quad . \tag{2.24}$$

To clarify the boundary conditions, the electric field [Fig. 2.2(a)] the velocity [Fig. 2.2(b)] and the density of minority carriers [Fig. 2.2(c)] are shown as a function of distance x in Fig. 2.2.

The current density must be the same along the path of conduction, x. Therefore, n_{sat} can be obtained by equating the pure diffusion current at x = 0 to the drift current at x = L_S. This gives

$$qD_n \left.\frac{\partial n_p}{\partial x}\right|_{x=o} = qv_{sat}n_{sat} \quad , \qquad (2.25)$$

where v_{sat} is the carrier saturation velocity. Finally, by combining Eqs. (2.22 through 2.24) with Eq. (2.25), a nonlinear expression for n_{sat} can be found as follows:

$$n_{sat} = \frac{0.5\ \alpha L_S D_n}{v_{sat}} n_{inj} - \frac{D_n}{v_{sat} L_S} \ln(n_{inj}/n_{sat}) n_{inj} \quad , \qquad (2.26)$$

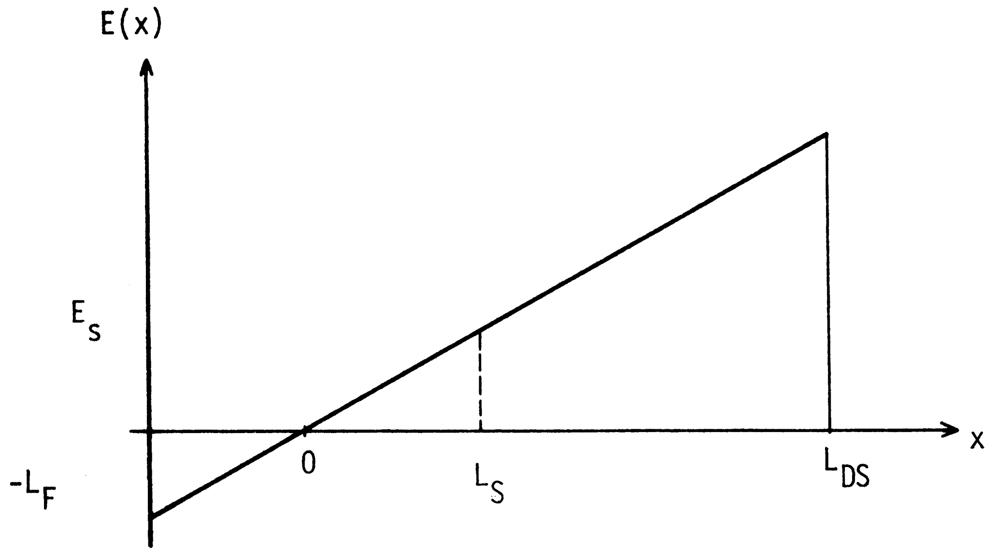
where $n_{inj} = n_{po} \exp[(V_F - \phi_G/V_T]$,

$$L_S = \frac{E_{TH}}{2V_{DS}/L_{DS}^2} \quad ,$$

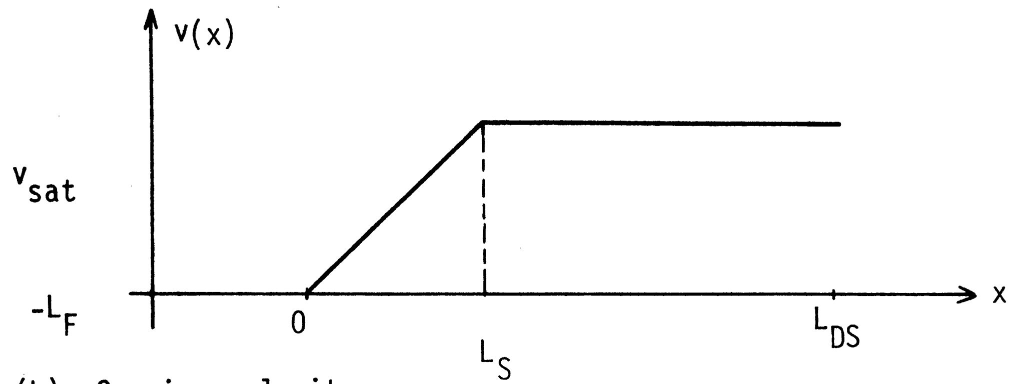
$$E_{TH} = v_{sat}/\mu_{no},$$

V_F = the forward biasing voltage across the source-channel junction and

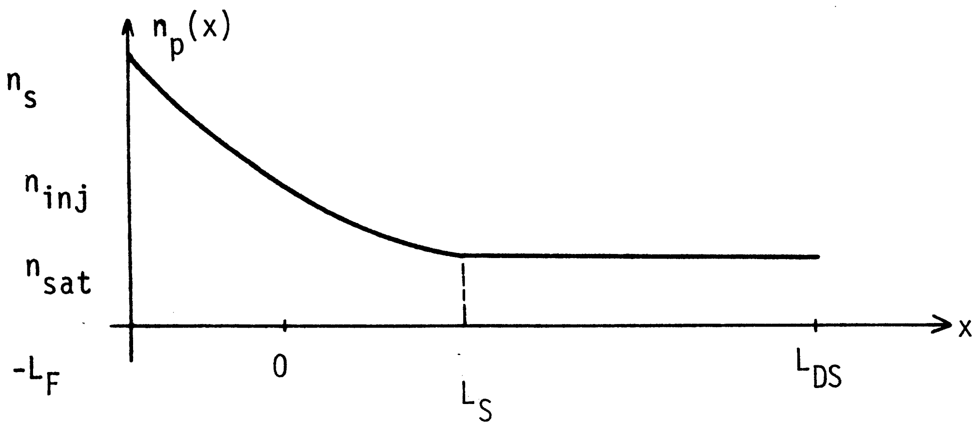
ϕ_G = the barrier height induced by the gate-source voltage.



(a) Electric field.



(b) Carrier velocity.



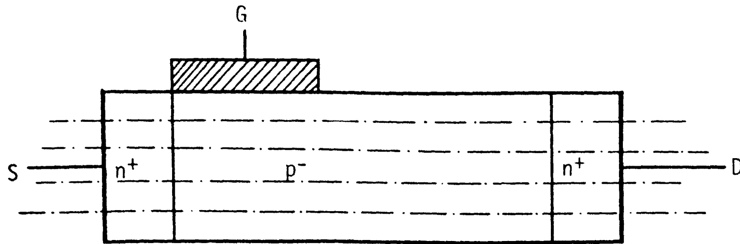
(c) Injected carrier.

Fig. 2.2 Field, velocity and carrier distributions of a TTPT Device.

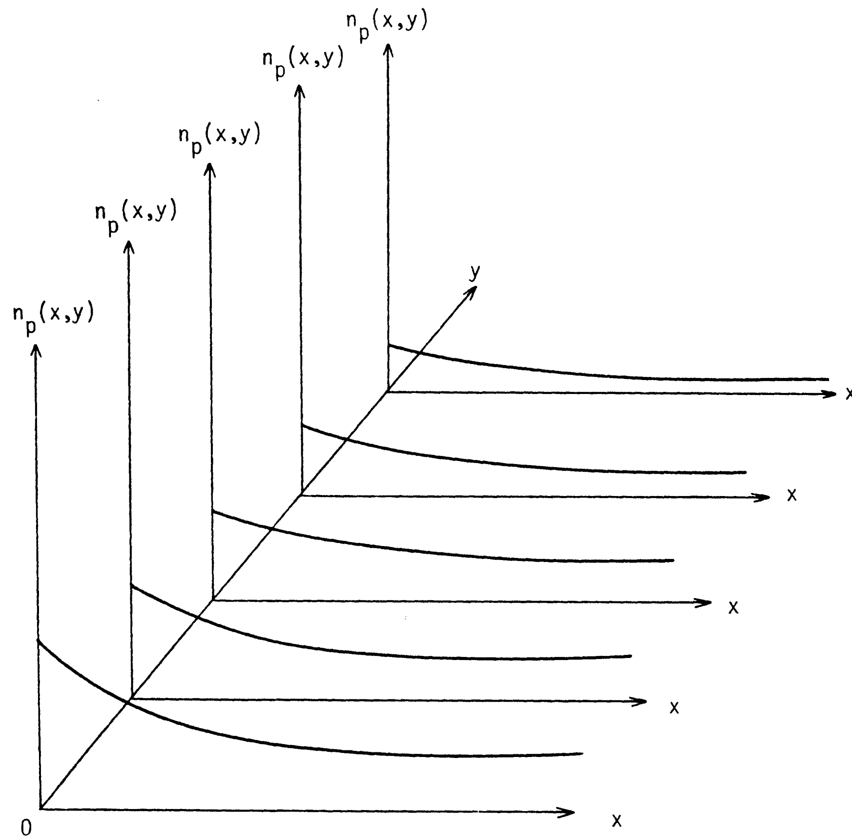
2.2.2 Dc Current Density of a GFC-BARITT Device. The expression for the current density J_{DS} requires knowledge of the distribution of the carriers and the field along the path of conduction. For an exact solution of the current density, Poisson's equation and the continuity equation must be solved simultaneously with the appropriate boundary conditions. This is true for any semiconductor device. It is, however, extremely difficult to obtain analytical solutions for the current density, potential and carrier distributions.

By considering the principle of the device operation, one may obtain quasi-numerical expressions for the current density and electric field. This approach is satisfactory as far as the understanding of a certain device and simplifies the equations considerably. In the course of this study, analytical solutions of the characteristic equations of a device are obtained by making certain simplifications. From Section 2.2.1 the carrier distribution in the device can be used to obtain the current density. In another approach, the diffusion effect is neglected by assuming that all the injected carriers drift along the channel and contribute to the current. In the following sections, two approximations for the current density expression will be given.

2.2.2a Drift-Diffusion Current Approximation. The GFC-BARITT device operation is governed by the two-dimensional potential distribution. A device is divided into a number of thin devices as shown in Fig. 2.3(a) where each of them has different injection levels as in Fig. 2.3(b). The next important problem is to find the level



(a) Device segmented into N numbers of Δy-thick BARITT diodes.



(b) Carrier distribution in each segment.

Fig. 2.3 A TTPT Device.

of injection in each segment or Δy-thick BARITT diode. The potential distribution is assumed to be the superposition of the potential along the x-direction and the potential along the y-direction. The superposition assumption will simplify the problem of the two-dimensional potential distribution in a GFC-BARITT device. The potential along the y-direction "gate potential" is then expressed as:

$$\phi_G(I) = (V_{GS} + V_{B2}) \left[1 - \left(\frac{I - 0.5}{N}\right)\right]^2 , \quad (2.27)$$

where V_{GS} = the applied gate-source voltage at the surface of the channel,

V_{B2} = the built-in potential between the gate and the channel,

N = the number of segments or BARITT diodes of a GFC-BARITT device and

$\phi_G(I)$ = the potential of the Ith segment along the y-direction due to the applied gate-source voltage.

The potential distribution along the x-direction can be approximated from the BARITT diode expression [12]. In general, it is a quadratic function of x (conduction path). The potential $V_F(I)$ at the source side of the device must be known in addition to a general knowledge of the potential variation along x. The combination of $V_F(I)$ and $\phi_G(I)$ will give the level of forward biasing of each Δy-thick BARITT diode or segment. The density of injected carriers, n_{inj} can be expressed as:

$$n_{inj}(I) = n_{po} \exp\left(\frac{q}{kT}(V_F(I) - \phi_G(I))\right) , \quad (2.28)$$

where n_{po} = the steady state density of minority carriers in the channel (p-type semiconductor), $n_{po} = n_i/N_A$,

$V_F(I)$ = the forward bias voltage at the Ith segment. An expression for this will be derived in the next section,

N_A = the impurity concentration of the p-type semiconductor,

$n_{inj}(I)$ = the density of the injected carriers at the Ith segment.

The current density, $J_{DS}(I)$ of the Ith segment is:

$$J_{DS}(I) = qv_{sat}n_{sat}(I) \quad , \tag{2.29}$$

where n_{sat} is given in Eq. (2.26) and v_{sat} is the saturated velocity of the carriers. Rearranging Eq. (2.29) and combining it with the expression for n_{sat}, the $J_{DS}(I)$ expression of the Ith segment becomes

$$J_{DS}(I) = qn_{inj}(I) \exp[-0.5\ \alpha L_S^2 + k_1^1 L_S]v_{sat} \quad , \tag{2.30}$$

where

$$k_1^1 = 0.5\ \alpha L_S - \frac{\ln(n_{inj}(I)/n_{sat})}{L_S} \quad .$$

The expression in Eq. (2.30) is given for the total current which is equal to the drift current beyond L_S. If one requires drift and diffusion currents separately, the distribution function of the carriers in the channel can be used. The diffusion current density would therefore be:

$$J_{DS_{diff}}(x,I) = qD_n \frac{\partial n_p(x,I)}{\partial x} \tag{2.31}$$

or

$$J_{DS_{diff}}(x,I) = qD_n(k_1 - \alpha x)n_p(x,I)$$

and the drift current density is

$$J_{DS_{drift}}(x,I) = q\mu_{no}n_p(x,I)\, E(x)$$

or (2.32)

$$J_{DS_{drift}}(x,I) = q\mu_{no}n_p(x,I)\, \gamma x \quad ,$$

where

$$n_p(x,I) = n_{inj}(I)\, \exp[0.5\, \alpha x^2 + k_1^1 x] \quad .$$

For $x \geq L_S$,

$$\frac{\partial n_p(x,I)}{\partial x} = (k_1^1 - \alpha x)n_p(x,I) \quad ,$$

$E(x) = \gamma x$, the linear electric field, and

μ_{no} = the low field mobility.

At every point

$$J_{DS}(I) = J_{DS_{diff}}(x,I) + J_{DS_{drift}}(x,I) \quad .$$

At $x = L_S$ the point diffusion current becomes negligible. Therefore at $x \geq L_S$, the total current density, $J_{DS}(I)$ is equal to $J_{DS_{drift}}$ (L_s, I).

Finally, the total current I_{DS} can be obtained from the current density expression of the Ith segment which is given in Eq. (2.30):

$$I_{DS} = 2Z\Delta y \sum_{I=}^{N} J_{DS}(I) \quad , \tag{2.33}$$

where Z = the width of the device,

$\Delta y = D/N$,

D = the half of the channel width $(W_S/2)$ and

N = the number of segments into which the GFC-BARITT device is divided.

2.2.2b Drift Current Approximation. In the previous section the effect of the diffusion was discussed. The velocity of the carriers was assumed to be a linear function of the field at the low field region, but constant at the high field region. This approximation, by itself, may introduce a larger error than by neglecting the diffusion effect. Therefore, in this section the effect of the diffusion is neglected, but the velocity as a nonlinear function of the electric field is considered.

A nonlinear velocity expression as a function of the electric field for Si [13] and for III-V compound semiconductors [14] are given as follows.

For silicon:

$$v(E) = v_{sat} \frac{E}{E + E_{sat}} \quad . \tag{2.34}$$

For III-V compound semiconductors:

$$v(E) = \frac{[\mu_{no}E + v_{sat}(E/E_c)^4]}{[1 + (E/E_c)^4]} , \tag{2.35}$$

where v_{sat} = the saturated velocity,

E_c = the field at the peak velocity,

E_{sat} = the field where velocity reaches half of the saturated velocity, and

E = the electric field.

The assumptions for the drift current approximation are:

(a) Negligible generation-recombination in the depleted channel and hole current (unipolar conduction) are assumed.

(b) The device is an n^+pn^+ structure and is divided into N number of segments as in Section 2.2.1, Fig. 2.3(a).

(c) The diffusion effect at the low field region of the device is neglected.

(d) The carrier distribution along the conduction path is uniform.

(e) The potential of the Ith segment due to the applied gate voltage is $\phi_G(I)$.

(f) The forward bias voltage due to the applied voltage between the drain and source terminals is $V_F(I)$.

The current density of the Ith segment is

$$J_{DS}(x,I) = qn_p(x,I)v(E) \tag{2.36}$$

and

$$n_p(x,I) = n_{po} \exp[(V_F(I) - \phi_G(I)/V_T] \quad . \tag{2.37}$$

The field dependent velocity expressions are given in Eq. (2.34) and Eq. (2.35).

The current density expression for Si devices is

$$J_{DS}(x,I) = qn_p v_{sat} \frac{E}{E + E_{sat}} \quad , \tag{2.38}$$

where E = dV/dx, the field along the conduction path, x. The integration of Eq. (2.38) with respect to x results in an average current density expression for the low level injection case as follows:

$$J_{DS}(I) = qv_{sat} \frac{V_{DS}}{V_{DS} + E_{sat}L_{DS}} n_{po} \exp \frac{q}{kT} [V_F(I) - \phi_G(I)] \quad . \tag{2.39}$$

The current density of GaAs or InP can be found by using Eq. (2.35) for v(E) in Eq. (2.36) and integrating Eq. (2.36) with respect to the conduction path, x. This yields

$$J_{DS}(I) = J_o \exp([V_F(I) - \phi_G(I)] / V_T) \, , \tag{2.40}$$

where

$$J_o \simeq q \frac{n_i^2}{N_A} \frac{[0.5\ \mu_{no} E_{RB} + 0.2\ v_{sat}(E_{RB}/E_c)^4]}{[1 + 0.2(E_{RB}/E_c)^4]}$$

and

$$E_{RB} \simeq 2V_{DS}/L_{DS} \ .$$

Finally, the drift current can be obtained either from Eq. (2.39) or from Eq. (2.40) and given by

$$I_{DS} = 2Z \frac{D}{N} \sum_{I=1}^{N} J_{DS}(I) \ . \qquad (2.41)$$

The current in a GFC-BARITT device can be calculated either from Eq. (2.41) or from Eq. (2.33), if only $V_F(I)$ is known. In the next section, an expression for $V_F(I)$ of the Ith segment of a GFC-BARITT device will be derived.

2.2.3 Potential Distribution. Each segment of a GFC-BARITT device is a BARITT diode. Therefore, Poisson's equation for each segment can be expressed as

$$\frac{\partial E}{\partial x} = -\frac{qN_A}{\varepsilon_s} - \frac{qn_p(x,I)}{\varepsilon_s} \ . \qquad (2.42)$$

Equation (2.42) is the general expression which includes the space charge effect (or injected carrier effect) on the field distribution. It is necessary however to solve Eq. (2.42) simultaneously with the current density and the continuity equations. To obtain an

analytic solution of the problem (Eq. 2.42), some simplifying assumptions have been made. These are:

(i) The potential along the y-direction is assumed to be constant so one could solve a one-dimensional Poisson's equation.

(ii) The injected carrier distribution $n_p(x)$ is replaced by J_{DS}/v. This gives

$$\frac{\partial E}{\partial x} = -\frac{2}{\varepsilon_s} N_A - \frac{J_{DS}(I,x)}{\varepsilon_s v} . \qquad (2.43)$$

The expressions for the velocities are given in Eq. (2.34) for Si and in Eq. (2.35) for GaAs or InP.

The inclusion of the velocity expression in Eq. (2.35) for III-V compound semiconductors is difficult to implement as it is. A modified expression for the velocity is given by

$$v(E) = v_{sat} \frac{E}{E + E_{sat}} , \qquad (2.44)$$

where

$$E_{sat} = v_{sat}/2\mu_{no}$$

and v_{sat} is the saturated velocity of GaAs or InP. Equation (2.44) has the form of Eq. (2.34) and therefore the solution of Eq. (2.43) will be valid for Si, GaAs and InP. Substituting the velocity expression in Eq. (2.43) gives for silicon and GaAs, respectively,

$$\frac{\partial E}{\partial x} = -\frac{qN_A}{\varepsilon_s} - \frac{1}{\varepsilon_s} \frac{J_{DS}(x,I)}{v_{sat}} \frac{E + E_{sat}}{E} \tag{2.45}$$

and

$$\frac{\partial E}{\partial x} = \left(-\frac{qN_A}{\varepsilon_s}\right) - \frac{1}{\varepsilon_s} \frac{J_{DS}(x,I)}{v_{sat}} - \frac{1}{\varepsilon_s} \frac{J_{DS}(x,I)}{v_{sat}} \frac{E_{sat}}{E} \,. \tag{2.46}$$

After rearranging Eq. (2.46)

$$\frac{\partial E}{\partial x} = \alpha_i \left(\frac{E_{sat}}{E}\right) + \beta_i \quad , \tag{2.47}$$

where

$$\alpha_i = -\frac{J_{DS}(I)}{\varepsilon_s v_{sat}}$$

and

$$\beta_i = -\frac{qN_A}{\varepsilon_s} + \alpha_i \quad .$$

From Eq. (2.47)

$$dx = \frac{E\, dE}{E_{sat}\alpha_i + \beta_i E} \quad . \tag{2.48}$$

Finally, the integration results in

$$x = \left| \frac{1}{\beta_i^2} (\alpha_i E_{sat} + \beta_i E) - \frac{\alpha_i}{\beta_i^2} E_{sat} \ln(\alpha_i E_{sat} + \beta_i E) \right|_{E=o}^{E} \quad . \tag{2.49}$$

Substituting the boundary values gives

$$x = \frac{E}{\beta_i} + \frac{\alpha_i}{\beta_i^2} E_{sat} \ln(\alpha_i E_{sat}) - \frac{\alpha_i}{\beta_i^2} E_{sat} \ln(\alpha_i E_{sat} + \beta_i E) \quad . \quad (2.50)$$

Replacing E with -(dV/dx) and integrating both sides of Eq. (2.50) gives

$$\frac{1}{2} x^2 \Big|_{x=-L_F}^{L_R} = \frac{1}{\beta_i^2} V \Big|_{V_B-V_F}^{V_R-V_B} + \frac{\alpha_i}{\beta_i^2} E_{sat} [\ln(\alpha_i E_{sat})] x \Big|_{-L_F}^{L_R}$$

$$- \frac{\alpha_i E_{sat}}{\beta_i^2} \int_{x=-L_F}^{L_R} \ln(\alpha_i E_{sat} + \beta_i E) dx \quad . \quad (2.51)$$

Replacing dx from Eq. (2.48) and integrating over E results in

$$\frac{1}{2} [L_R^2 - L_F^2] = \frac{V_{DS}}{\beta_i} + \frac{\alpha_i E_{sat}}{\beta_i^2} \mathrm{Ln}(\alpha_i E_{sat}) L_{DS} + \frac{\alpha_i E_{sat}}{\beta_i^4}$$

$$\cdot \Big\{ (\alpha_i E_{sat} + \beta_i E_{RB}) [1 - \ln(\alpha_i E_{sat} + \beta_i E_{RB})] - (\alpha_i E_{sat} - \beta_i E_{FB})$$

$$\cdot [1 - \ln(\alpha_i E_{sat} - \beta_i E_{FB})] \Big\} + \frac{\alpha_i^2 E_{sat}^2}{2\beta_i^4}$$

$$\cdot \Big\{ [\ln(\alpha_i E_{sat} + \beta_i E_{RB})]^2 - [\ln(\alpha_i E_{sat} - \beta_i E_{FB})]^2 \Big\} , \quad (2.52)$$

where L_R = the length of the depletion layer from the reverse-biased junction side of the n^+pn^+ diode

L_F = the length of the depletion layer from the forward-baised junction side,

E_{FB} = the field at the forward-biased junction side and

E_{RB} = the maximum field at the reverse-biased junction side.

Expressions for L_F and L_R can be obtained from the conventional depletion layer expressions, namely,

$$L_R = \left[\frac{2\varepsilon_s(V_R + V_B)}{qN_A}\right]^{1/2} \tag{2.53}$$

and

$$L_F = \left[\frac{2\varepsilon_s(V_B - V_F(I))}{qN_A}\right]^{1/2} , \tag{2.54}$$

where

$$V_{DS} = V_R + V_F(I)$$

and

$$L_{DS} = |L_R| + |L_F| \quad .$$

Equation (2.52) can be simplified by neglecting the smaller terms such as

(i) $|E_{RB}| >> |E_{FB}|$ neglect E_{FB} terms,

(ii) $|L_R| >> |L_F| \rightarrow |L_{DS}| >> L_F$

and

(iii) $|E_{sat}| \gg |E_{FB}|$.

Equation (2.52) then becomes

$$\frac{1}{2} L_{DS}^2 - L_{DS}|L_F| = \frac{V_{DS}}{\beta_i} + \frac{\alpha_i}{\beta_i^2} E_{sat} L_{DS} \ln(\alpha_i E_{sat}) + \frac{\alpha_i E_{sat}}{\beta_i^4}$$

$$\cdot \Big\{(\alpha_i E_{sat} + \beta_i E_{RB})(1 - \ln(\alpha_i E_{sat} + \beta_i E_{RB}))$$

$$- \alpha_i E_{sat}(1 - \ln(\alpha_i E_{sat}))\Big\} + \frac{\alpha_i^2 E_{sat}^2}{2\beta_i^4}\Big\{[\ln(\alpha_i E_{sat} + \beta_i E_{RB})]^2$$

$$- [\ln(\alpha_i E_{sat})]^2\Big\} \qquad (2.55)$$

and

$$-L_{DS}\left(\frac{2\varepsilon_s}{qN_A}\right)^{1/2} (V_B - V_F(I))^{1/2} = -\frac{1}{2} L_{DS}^2 + \frac{V_{DS}}{\beta_i} + \frac{\alpha_i}{\beta_i} E_{sat} L_{DS}$$

$$\cdot \ln(\alpha_i E_{sat}) + \frac{\alpha_i E_{sat}}{\beta_i^4} \Big\{(\alpha_i E_{sat} + \beta_i E_{RB})$$

$$\cdot (1 - \ln(\alpha_i E_{sat} + \beta_i E_{RB})) - \alpha_i E_{sat}(1 - \ln(\alpha_i E_{sat}))\Big\}$$

$$+ \frac{\alpha_i^2 E_{sat}^2}{2\beta_i^4}\Big\{[\ln(\alpha_i E_{sat} + \beta_i E_{RB})]^2 - [\ln(\alpha_i E_{sat})]^2\Big\} , \qquad (2.56)$$

where $E_{RB} = 2V_{DS}/(L_{DS} - L_F)$.

The $V_F(I)$ value of each segment in a GFC-BARITT device can be obtained by an iterative solution of Eq. (2.54), (2.56) and the current density expression from Section 2.2.1 or 2.2.2.

The expression in Eq. (2.56) is valid for all levels of injection. It can, however, be simplified for two extreme cases:

(i) Low level injection ($\alpha_i = 0$) can be reduced to a simple expression.

(ii) High level injection

(a) For a low level injection case, a similar expression for $V_F(I)$ has been reported for a p^+np^+ BARITT diode [12] as

$$(V_B - V_F(I))^{1/2} = \left(\frac{qN_A}{2\varepsilon_s}\right)^{1/2} \left[\frac{L_{DS}}{2} - \frac{V_{DS}}{L_{DS}} \frac{\varepsilon_s}{qN_A}\right]. \qquad (2.57)$$

After rearranging Eq. (2.56) and defining

$$V_{FB} \triangleq \left(\frac{qN_A}{2\varepsilon_s}\right) L_{DS}^2 \qquad \text{(flat band voltage)} ,$$

$$|V_F(I)| = V_B - \frac{(V_{FB} - V_{DS})^2}{4V_{FB}} , \qquad (2.58)$$

where V_{DS} is greater than the reach-through voltage, V_{RT} but is smaller than the flat band voltage, V_{FB}.

(b) For the high level injection case,

$$\alpha_i = \beta_i$$

and

$$(V_B - V_F(I))^{1/2} = \left(\frac{qN_A}{2\varepsilon_s}\right)^{1/2} \frac{1}{L_{DS}} \left[\left(\frac{L_{DS}^2}{2} - \frac{V_{DS}}{\alpha_i} + \frac{E_{sat}}{\alpha_i} L_{DS} \ln(\alpha_i E_{sat})\right)\right.$$

$$+ \frac{E_{sat}}{\alpha_i}(E_{sat} + E_{RB})[1 - \ln(\alpha_i(E_{sat} + E_{RB}))] - \frac{E_{sat}^2}{\alpha_i^2}[1 - \ln(\alpha_i E_{sat})]$$

$$\left. - \frac{E_{sat}^2}{2\alpha_i^2}\left([\ln(\alpha_i(E_{sat} + E_{RB}))]^2 - [\ln(\alpha_i E_{sat})]^2\right)\right] . \qquad (2.59)$$

The solution of a two-dimensional Poisson's equation is numerically possible within a reasonable time of computation [15], [16]. Instead of the iterative solution of $V_F(I)$, the potential distribution in every mesh point in the device can be obtained by using the rapid Poisson solver and then searching for the maximum barrier height, $V_F(I) - \phi_G(I)$. The algorithm and the program for the Poisson solver are given in Appendix A.

2.3 Static-Induction Transistor

The saturation of the current in conventional FETs is attributed to different mechanisms by different researchers. According to Shockley, pinch-off is the cause of the current saturation [17]. On the other hand, Nishizawa claims that the series channel resistance is responsible for the current saturation of FETs [1]. He then proposed a triode-like operation of a FET by reducing the series channel resistance. Recently, such a device has been realized and triode-like characteristics were reported [1].

Since then many applications of this device have been considered [3], [18]. The SIT has potential applications in high power, high frequency analog areas due to its:

(i) high input resistance,

(ii) low output resistance,

(iii) high transconductance,

(iv) small gate time constant and minority carrier storage unlike Bipolar Junction Transistors (BJTs) and

(v) negative temperature coefficient at high currents which offers stable operation [3] and a higher breakdown voltage due to the large distance between the gate and the drain.

In Table 2.1 the power performance of SITs at different frequencies is shown. This illustrates the potential of SIT devices.

In addition to all of these characteristics which favor high-power high-frequency operation there are some physical limitations to high power and high frequency performance of a SIT such as: (i) at high injection levels, there will be majority carrier storage at the low-field injection region; (ii) it is a normally on device and therefore the voltage swing of the input signal is limited; (iii) distributed gate capacitance of a planar SIT is high which limits the high frequency performance, and (iv) the drain current is very sensitive to the lateral diffusion of a vertical SIT which makes it difficult to fabricate reproducible devices.

Even though the SIT is a promising device for high power and relatively high frequency applications, it has not attracted enough

Table 2.1

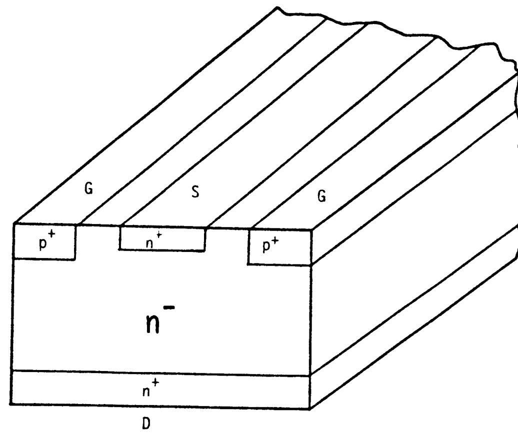
Power Performance of SITs

Frequency	Power	Efficiency	Reference
8 MHz	2 kW		[1]
200 MHz	40 W		[3]
1.0 GHz	10 W		[1]
2.5 GHz	10 W		[8]
1.0 GHz	100 W		[2]
100 MHz	216 W	55 percent	[8]
700 MHz			[8]

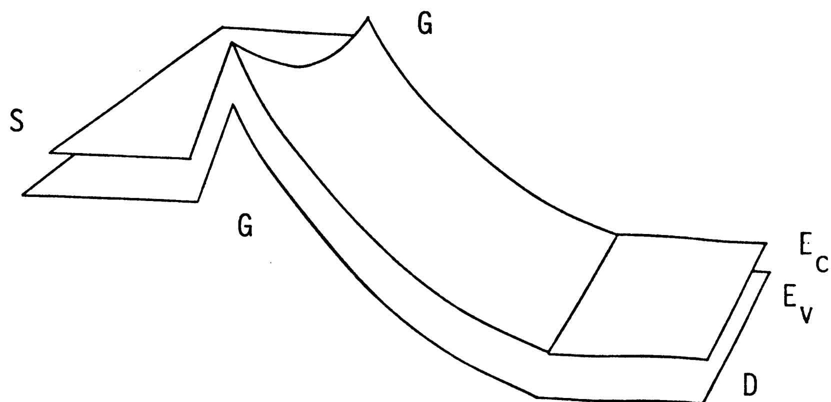
research interest especially in the United States. Recently, there has been a growing interest in SIT devices. The potential distribution [18], [19], [20], applications to digital circuits [21], [22], Dc characteristics [3], [23], [24], possibility of VLSI applications (which is not promising [9], [18]), and applications in microwave circuits [2], [8], [24] of SITs have been studied by different groups. None of these groups has comprehensively studied this device. Most of them have reported the results of their experimental studies.

2.3.1 Physics of the SIT Device. The SIT device is a special case of vertical Junction Gate Field Effect Transistor (J-FET). If a JFET is made of a thin and lightly doped semiconductor, then at a low gate-drain voltage, the whole channel can be depleted before the breakdown occurs. A typical SIT structure is an $n^+n^-n^+$ one as shown in Fig. 2.4(a). Since the channel is n^--type materials, then at low applied voltages between the gate and source it is completely depleted and a barrier at the source side of the channel is created. This barrier is induced electrostatically by the gate-source potential difference. In a long-channel FET this is called the pinch-off mode where current saturates. But since the whole channel is depleted unlike the pinch-off case in FETs, the increase in the drain-source voltage reduces the statically induced barrier at the source side of the channel and exponentially increases the current.

The principle of the current conduction is very much like that of a BARITT diode. The only difference is that in a BARITT



(a) A Vertical SIT



(b) Two-Dimensional Energy Band Diagram.

Fig. 2.4 SIT Device. (G = Gate, D = Drain and S = Source).

diode, minority carriers are injected but in the case of a SIT majority carriers are injected. The barrier height is shown in Fig. 2.4(b) for an $n^+n^-n^+$ SIT. Even though the barrier height and structure of a SIT are different from those of a GFC-BARITT device, the form of the device expressions are the same. Therefore, most of the results of Section 2.2.2 can be used directly for SITs as well as for GFC-BARITT devices.

2.3.2 Dc Characteristics of the SIT Device. At low gate-drain bias conditions, the channel may not be depleted completely. In this case, the device operates as a FET and its characteristic expressions such as the Dc current, small signal, and circuit parameters (g_m, g_{ds}, C_{gd} and C_{ds}) will be dealt with briefly, because there have been extensive studies of FETs [25], [26] and numerical studies [27], [28] and [29] in the last fifteen years.

By replacing the minority carrier density, n_{po} in Section 2.2.2a and Section 2.2.2b, with N_D, the Dc current density and current expressions for GFC-BARITT devices become valid for SITs. If the distance between the drain and the source is much larger than the distance between the two gates on both sides of the source then the potential distribution in a SIT is very much like that of a GFC-BARITT device. The current expressions of a GFC-BARITT device are modified and repeated here for a SIT device. It is assumed that the SIT is divided into a number of N segments such as in a GFC-BARITT device. The current density of the Ith segment for silicon is

$$J_{DS}(I) = qN_D \frac{v_{sat} V_{DS}}{(V_{DS} + E_{sat} L_{DS})} \exp[(V_F(I) - \phi_G(I))/V_T] \quad . \qquad (2.60)$$

The $V_F(I)$ expressions derived in Section 2.2.3 are not valid for SITs. In the case of a GFC-BARITT device, depletion is between the drain and the source but in the case of a SIT device, the depletion is between the drain and the gate. Therefore, the potential distribution in a SIT is different from that of a GFC-BARITT device. The actual potential distribution can be obtained by numerical solution of the two-dimensional Poisson's equation.

It is possible, however, to obtain a simple approximation for $V_F(I)$. In Fig. 2.5, along the OM path, the potential is a quadratic function of distance. This potential is

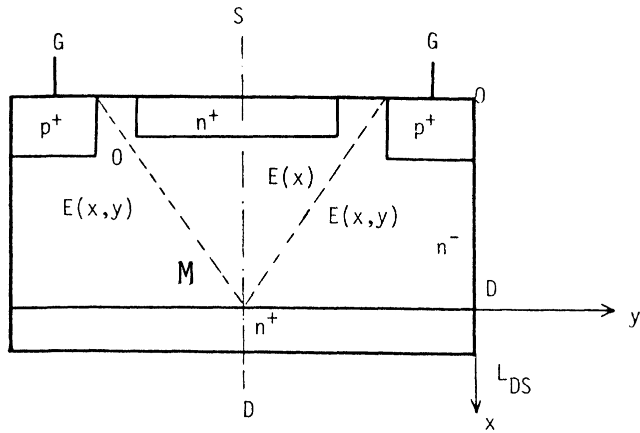
$$V(x,y) = (V_{GS} + V_{DS}) \frac{(x^2 + y^2)}{(L_{DS}^2 + D^2)} , \tag{2.61}$$

where D is the half of the channel, $D = 0.5\ W_S + W_{GS}$. The potential along the x-direction is

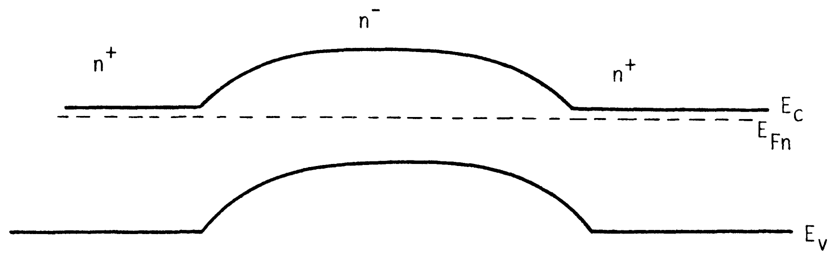
$$V(x,y) = \frac{L_{DS}}{(L_{DS}^2 + y^2)^{1/2}} (V_{DS}) \frac{(x^2 + y^2)}{(L_{DS}^2 + D^2)} . \tag{2.62}$$

At the zero bias case, there is a charge accumulation region on the n^--side of the n^+n^- junction of a SIT device which is a "Debye length" wide as shown in Fig. 2.5(b). $V_F(I)$ is the maximum barrier height value of the Ith segment in a SIT. From Eq. (2.62), assuming that this barrier height occurs at $x = \lambda_D$ from the source terminal, then

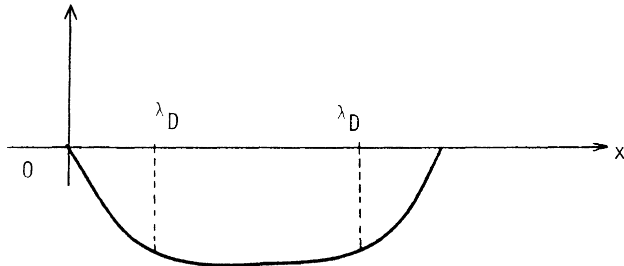
$$V_F(I) = \frac{L_{DS}}{(L_{DS}^2 + \frac{D^2}{N^2} I^2)^{1/2}} (V_{DS}) \frac{(\lambda_D^2 + \frac{D^2}{N^2} I^2)}{(L_{DS}^2 + D^2)} , \tag{2.63}$$



(a) Structure.



(b) Energy band diagram of an $n^+n^-n^+$ diode.



(c) Built-in potential of an $n^+n^-n^+$ diode.

Fig. 2.5 A SIT Device.

where

$$\lambda_D = \left(\frac{\varepsilon_s V_T}{2qN_D}\right)^{1/2} .$$

Equation (2.63) along with the $\phi_G(I)$ expression given by Eq. (2.28) are used in the current density expression given in Eq. (2.60).

A simple expression of the DC current of a SIT device is

$$I_{DS} = 2Z \frac{D}{N} \sum_{I=1}^{N} J_{DS}(I) , \qquad (2.64)$$

where $J_{DS}(I)$ is the current density of the Ith segment and is given in Eq. (2.60), $J_{DS}(I)$ in Eq. (2.60) is the result of the drift approximation of the injected carriers. In reality, at the low field region, the diffusion of the majority carriers are also important. The drift-diffusion approximation given in Section 2.1 is valid for SIT devices with a change of carrier type. The results of Section 2.2.2a are modified and given for SIT devices next.

The density of carriers in the saturated velocity region is given by

$$n_{sat} = \frac{\alpha L_S}{2v_{sat}} D_n n_{inj} - \frac{D_n}{v_{sat} L_S} n_{inj} \ln(n_{inj}/n_{sat}) , \qquad (2.65)$$

where $n_{inj} = N_d \exp(V_F(I)) - \phi_G(I))/V_T$.

The distribution of the injected carriers in the channel is given by

$$n_p(x) = n_{inj} \exp[-0.5 \ \alpha x^2 + k_1^1 x] , \qquad (2.66)$$

where

$$k_1^1 = -[1/L_S \ln(n_{inj}/n_{sat}) - 0.5\ \alpha L_S] \quad .$$

Nishizawa et al. [3] claim that there is no minority carrier storage effect in a SIT device and therefore it is a high frequency device. It is true that there is no minority carrier storage effect, but there is a majority carrier storage effect which degrades the high frequency performance. An expression of the carrier distribution in Eq. (2.66) clearly indicates that the carrier storage effect will be important at high injection. This means that SIT devices are no exception as far as power and speed or high frequency performance of solid state devices are concerned. The degree of majority carrier storage is given in Eq. (2.66) may not be exact, but nevertheless it physically predicts a phenomenon which is expected.

2.4 Dc Characteristics of a Vertical Field-Effect Transistor

A simple analysis of a vertical FET is given in this section for completeness. A more complete model especially for GaAs FETs has been given in detail elsewhere [26]. A one-dimensional analysis of this special FET structure is relatively simpler than those of conventional FET structures since the gate is at the center of the drain and the source electrodes.

The FET structure which will be analyzed, is shown in Fig. 2.6. The following assumptions are made:

(i) The device is divided into two regions: the first region is L'_{DS} long and $D-y_{max}$ wide and is a voltage controlled resistor and

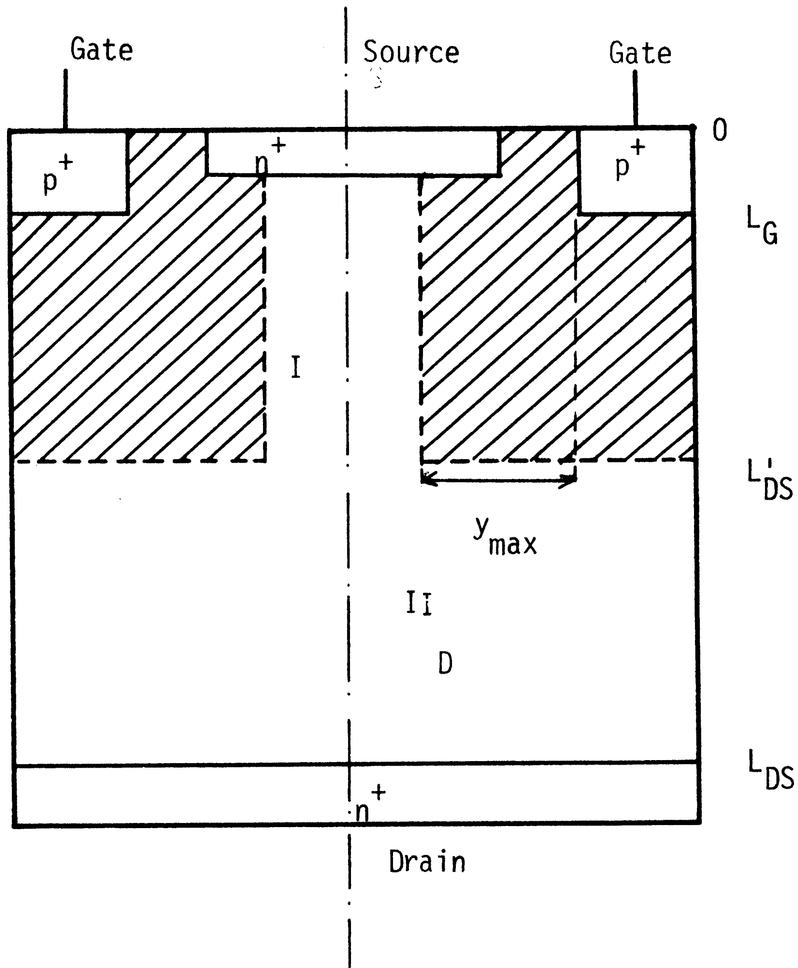


Fig. 2.6 Vertical FET Structure.

the second section is $L_{DS} - L'_{DS}$ long and D wide and is an N-type bulk resistor.

(ii) the voltage distribution in Region I is a linear function of conduction path, x

$$V(x) = \frac{V_{DS}}{L'_{DS}} x \quad . \tag{2.67}$$

(iii) The effect of the velocity saturation is taken into account.

(iv) The depletion of the channel along the conduction path, x, is assumed to be gradual.

The current transport expression in Region I is given in the following sections for different materials.

(a) For a silicon device,

$$J_{DS} = qN_D\mu_n(E) \frac{dV(x)}{dx} \quad , \tag{2.68}$$

where

$$\mu_n(e) = v_{sat} \frac{1}{E_{sat} + E}$$

and

$$L'_{DS} = L_G + \left[\frac{2\varepsilon_s(V_{GS} + V_{B2} + V_{DS})}{qN_D}\right]^{1/2} \quad .$$

By rearranging Eq. (2.68) and replacing the field by (dV/dx). a simpler equation is obtained as follows:

$$J_{DS} E_{sat} dx + J_{DS} dV = qn N_D v_{sat} dV \quad . \tag{2.69}$$

Finally, integration of Eq. (2.69) results in the following current density expression:

$$J_{DS} = q\, N_D\, v_{sat} \frac{V_{DS}}{(V_{DS} + E_{sat} L'_{DS})} \quad . \qquad (2.70)$$

The total drain-source current can be expressed as

$$I_{DS} = 2qZ(D - y_{max})\, J_{DS} \quad . \qquad (2.71)$$

Since the FET structure in Fig. 2.6 is symmetrical, the device expressions are derived for a half-width device where y_{max} is the maximum depletion width in the perpendicular direction of the conduction path, y, from the gate-channel junction.

The expression for y_{max} can be obtained by starting with the conventional depletion approximation:

$$y_{dep}(x) = \left[\frac{2\varepsilon_s (V_{GS} + V_{b2} + V(x))}{qN_D} \right]^{1/2} \quad . \qquad (2.72)$$

Rearranging Eq. (2.72) yields

$$y_{dep}(x) = c_o (V'_{GS} + c_1 x)^{1/2} \quad , \qquad (2.73)$$

where

$$c_o = \left(\frac{2\varepsilon_s}{qN_D} \right)^{1/2} ,$$

$$V'_{GS} = V_{GS} + V_{b2}$$

and

$$c_1 = V_{DS}/L'_{DS} \quad .$$

Finally, y_{max} is given by

$$y_{max} = y(x)_{dep}\Big|_{x=L_G} \quad . \tag{2.74}$$

Inserting Eq. (2.73) into Eq. (2.74) gives

$$y_{max} = [c_0^2(V'_{GS} + c_1 L_G)]^{1/2} \quad . \tag{2.75}$$

Then the drain-source terminal current I_{DS} becomes

$$I_{DS} = 2qZ\, N_D\, v_{sat} \frac{V_{DS}}{(V_{DS} + E_{sat}L'_{DS})} (D - y_{max}) \quad . \tag{2.76}$$

(b) For a III-V compound semiconductor device an expression for the terminal current I_{DS} can be derived by applying the same procedure as the one used for silicon devices. The current density J_{DS} expression can be obtained from Section 2.2.2a with some minor modifications to Eq. (2.40) and is given by

$$J'_{DS} = q\, N_D \left\{ \frac{0.5\, \mu_{no} \dfrac{V_{DS}}{L'_{DS}} + 0.2\, V_{sat}(V_{DS}/L'_{DS}E_c)^4}{1 + 0.2\, (V_{DS}/L'_{DS}E_c)^4} \right\} \tag{2.77}$$

and the total terminal current is given by

$$I_{DS} = 2Z(D - y_{max})J'_{DS} \quad . \qquad (2.78)$$

The y_{max} expression given in Eq. (2.75) can be used in Eq. (2.78).

2.5 Thermionic Saturation of the Diffusion Current

In the preceding sections, drift-diffusion and drift approximations of the carrier transport have been considered. These transport equations however are incapable of describing the conduction process in the vicinity of the potential barrier maximum. Therefore, the only other mechanism to account for is the thermionic emission. Within the barrier injection range, current flow cannot be regarded as limited only by diffusion through the barrier region; thermionic emission at the barrier maximum must also be taken into account as suggested and done by Persky [12]. The empirical modification of the current transport equation based on the concept of thermionic saturation of the diffusion current [12] is as follows:

$$J_n = \frac{q\mu_n n_p E + qD_n \frac{dn_p}{dx}}{[1 + D_n \frac{dn_p}{dx} /(n_p v_{TE})]} \quad , \qquad (2.79)$$

where v_{TE} = the velocity of the thermionic emission over a potential barrier of zero height and

$v_{TE} = (kT/2\pi m^*)^{1/2}$.

v_{TE} must be the limiting velocity in the absence of field-aided drift.

Equation (2.79) is considered as a current transport equation instead of the standard drift-diffusion equation, and the following assumptions are made:

(i) the velocity variation with field is neglected so that Einstein's relation can be used;

(ii) the space charge field effect of the injected carriers is neglected.

(iii) the recombination-generation effect is neglected and

(iv) a one-sided abrupt junction is assumed.

A new current density expression is obtained for a BARITT diode [12] and is given by,

$$J_n = qD_n n_s e^{-\psi_{ME}} \Big/ \left[\sqrt{(2\pi)}\, \lambda_D + \frac{D_n}{v_{TE}} \right] , \tag{2.80}$$

where n_s = the carrier density at the source terminal and

$\psi_{ME} = (V_{FB} - V_{DS})^2 / 4(V_{FB} V_T)$.

For $\sqrt{2\pi\lambda_D} << D_n/v_{TE}$, Eq. (2.80) reduces to

$$J_n = qv_{TE} n_s e^{-\psi_{ME}} . \tag{2.81}$$

The thermionic saturation of the diffusion current becomes important when the doping concentration of the channel $\gtrsim 10^{17}$ cm^{-3}.

In this approach negligence of the velocity saturation effect may introduce an error which may be comparable to an error introduced by using only the drift diffusion current transport equation.

One can conclude that any simplifying assumption will introduce an error to the current transport equation unless the basic device equations are simultaneously solved in a two-dimensional space.

CHAPTER III. SMALL- AND LARGE-SIGNAL MODEL

3.1 Introduction

The determination of the circuit and noise properties of a solid-state device is facilitated by the assumption of small-signal conditions. Under small-signal conditions, the Dc equations are usually expressed in first-order Taylor series and their quiescent values and the resulting equations for the perturbation quantities are linearized. This usually results in coupled nonlinear ordinary differential equations [11], [30].

There is another approach for the small-signal modeling of semiconductor devices which is the "Charge Control Analysis" [25]. This approach relates circuit elements with physical processes since there is a one-to-one correspondence between the static charge distribution and the terminal voltages and currents. By assuming that the terminal voltages and currents change sufficiently slowly so that the internal charge distribution can be regarded as a succession of static distributions, the dynamic model of both types of devices (SIT and GFC-BARITT devices) are obtained. This approach is called the quasi-steady-state approximation and was first used for Junction Field-Effect Transistor (JFET) modeling [31].

In the following sections, the small-signal circuit elements of both devices will be derived as a function of the device parameters. The small-signal equivalent circuit which is considered throughout

this chapter is shown in Fig. 3.1. Generally, the form of the expressions for SITs and GFC-BARITT devices are the same. This makes it possible to describe the small-signal circuit model of both devices with common expressions. However, this is not possible under all quiescent conditions. Under such conditions, the expression for the circuit element of each device is given separately. Some of the expressions are dependent on the parameters of the semiconductor material. Therefore, whenever it is necessary, expressions are given for devices made of silicon and also of III-V compound semiconductors. In the last section of this chapter, a simple noise analysis of SIT and GFC-BARITT devices will be given. Finally, the effect of the transit time of the drifting carriers along the conduction path between the source and the drain is included.

3.2 Small-Signal Circuit Elements

3.2.1 Transconductance. Transconductance is defined as the variation of the drain-source current with respect to gate voltage at a constant drain-source voltage:

$$g_m \triangleq \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS} = \text{constant}}$$

In Chapter II the expression for I_{DS} was given as a function of the terminal voltage V_{GS} and V_{DS}.

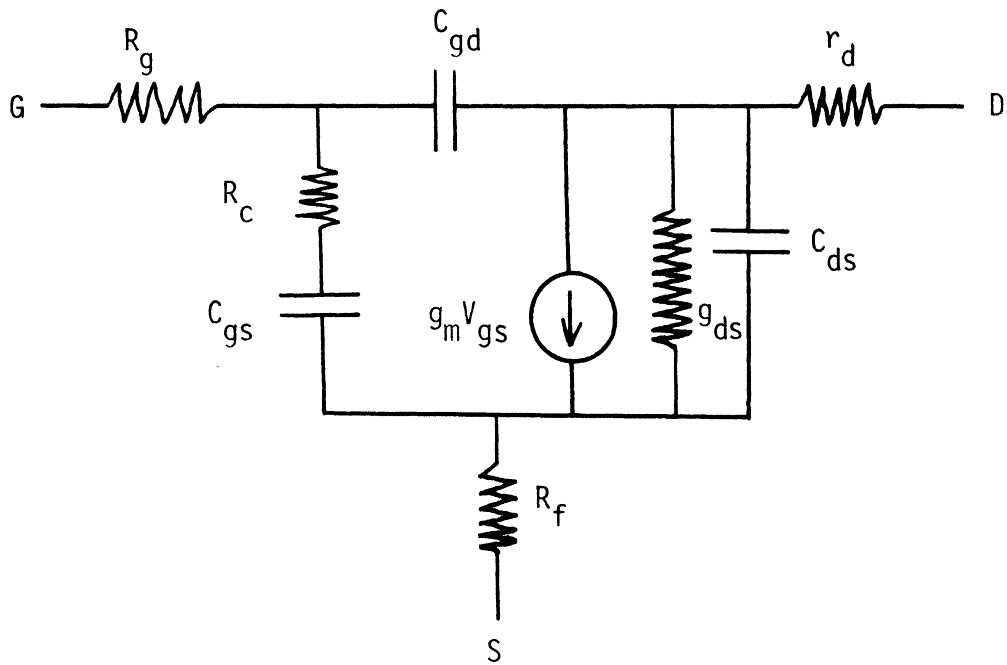


Fig. 3.1 Small-Signal Equivalent Circuit of a SIT or a GFC-BARITT Device.

3.2.1.1 Silicon Devices.

3.2.1.1a GFC-BARITT and SIT Devices. For a silicon device, the drift approximation of I_{DS} for $n^+p^-n^+$ type GFC-BARITT or $n^+n^-n^+$ type SIT devices is

$$I_{DS} = 2q \frac{v_{sat} V_{DS} Z}{(V_{DS} + E_{sat} L_{DS})} n_{th} \frac{D}{N} \sum_{I=1}^{N} \exp[(V_F(I) - \phi_G(I))/V_T] \quad , (3.1)$$

where $\phi_G(I) = (V_{GS} + V_{B2})\ (1 - [(I - 0.5)/N]^2)$,

$n_{th} = n_{po}$ for a GFC-BARITT device,

n_{po} = the minority carrier density at thermal equilibrium.

Differentiation of Eq. 3.1 with respect to V_{GS} results in the transconductance expression which does not include the transit-time effect:

$$g_m = G_{MO} \sum_{I=1}^{N} \left[1 - \left(\frac{1 - 0.5}{N} \right)^2 \right] \exp[(V_F(I) - \phi_G(I))/V_T] \quad , \qquad (3.2)$$

where

$$G_{MO} = -2q\, Z \frac{D}{N} n_{th} \frac{v_{sat}}{V_T} \frac{V_{DS}}{(V_{DS} + E_{sat} L_{DS})} \quad .$$

3.2.1.1b Vertical FETs. The drain-source current is given in Eq. (2.77) and repeated in Eq. (3.3):

$$I_{DS} = 2qZN_D v_{sat} \frac{V_{DS}}{(V_{DS} + E_{sat}L'_{DS})} (D - y_{max}) \quad , \qquad (3.3)$$

where $L'_{DS} = C_o(V'_{GS} + V_{DS})^{1/2} + L_G$,

$$y_{max} = [C_o(V'_{GS} + C_1 L_G) - L_G^2]^{1/2},$$

$$C_o = (2\varepsilon_s/qN_D)^{1/2}, \quad C_1 = V_{DS}/L'_{DS}.$$

The transconductance expression is obtained from Eq. 3.3 and given in Eq. 3.4:

$$g_{m2} \cong ZqN_D v_{sat} \frac{V_{DS}}{(V_{DS} + E_{sat}L'_{DS})} \frac{C_o^2}{y_{max}} . \qquad (3.4)$$

3.2.1.2 III-V Compound Semiconductor Devices.

3.2.1.2a GFC-BARITT and SIT Devices. The current expression is given by

$$I_{DS} = 2Z \frac{D}{N} J_o \sum_{I=1}^{N} \exp[(V_F(I) - \phi_G(I))/V_T] \quad , \qquad (3.5)$$

where

$$J_o = qn_{th} \left\{ \frac{2.5\, \mu_{no} E_c^4 \left(\frac{2V_{DS}}{L_{DS}}\right) + V_{sga} \left(\frac{2V_{DS}}{L_{DS}}\right)^4}{5E_c^4 + \left(\frac{2V_{DS}}{L_{DS}}\right)^4} \right\} \quad ,$$

$n_{th} = N_D$ for a SIT and

$n_{th} = n_i^2/N_A$ for a GFC-BARITT device.

The transcondutance is then given by

$$g_{m_1} = -2Z \frac{D}{N} \frac{1}{V_T} \sum_{I=1}^{N} \left[1 - \frac{(1 - 0.5)^2}{N^2} \right] J_{DS_1} \quad , \qquad (3.6)$$

where

$$J_{DS_1} = J_o \ \exp[(V_F(I) - \phi_G(I))/V_T] \ .$$

3.2.1.2b Vertical FETs. The current expression is given in Eq. 2.79 is as follows:

$$I_{DS} = 2Z(D - y_{max})J_o \qquad (3.7)$$

$$= \left\{ C_o^2 (V'_{DS} + C\ L_G) - L_G^2 \right\}^{1/2} \ .$$

The transconductance is given by Eq. (3.8):

$$g_{m_2} \simeq 2ZJ_o \frac{C_o^2}{y_{max}} \ . \qquad (3.8)$$

3.2.2 Conductance. Conductance is defined as the variation of the drain-source current with respect to the drain-source voltage as follows:

$$g_{ds} \triangleq \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{GS}=\text{constant}} \ .$$

Both the SIT and GFC-BARITT devices are high conductance or low output impedance devices.

3.2.2.1 Silicon Devices.

3.2.2.1a GFC-BARITT and SIT Devices. The derivation of the conductance from the current transport equation is given in Eq. (3.9). This conductance is valid for the GFC-BARITT and SIT devices.

$$g_{ds} \cong \frac{E_{sat}L_{DS}}{(V_{DS} + E_{sat}L_{DS})V_{DS}} I_{DS} + \frac{2ZD}{V_{DS}V_T N} \sum_{I=1}^{N} J_{DS}(I)V_F(I) \quad , (3.9)$$

where I_{DS} = the total current given in Eq. 3.1,

$J_{DS}(I)$ = the current density and

$V_F(I)$ = the forward biasing voltage of the Ith segment.

3.2.2.1b Vertical FETs. The conductance is obtained from the derivation of Eq. 2.77 with respect to V_{DS} and given in Eq. 3.10

$$g_{ds} \cong I_{DS} \left[\frac{E_{sat}L'_{DS}}{V_{DS}(V_{DS} + E_{sat}L'_{DS})} - \frac{1}{2} \frac{LG}{L'_{DS}} \frac{C_o^2}{y_{max}} \frac{1}{(D - y_{max})} \right] . \quad (3.10)$$

3.2.2.2 III-V Compound Semiconductors. The conductance expression is different from that of silicon due to the complicated velocity electric field expression.

3.2.2.2a GFC-BARITT and SIT Devices. The current transport equation is given in Eq. 3.5. From that expression, the conductance equation is derived and given in Eq. (3.11):

$$g_{ds} = \frac{2Z}{V_T} \frac{D}{N} \frac{1}{V_{DS}} \sum_{I=}^{N} V_F(I) J_{DS}(I) + 4 \frac{Z}{N} \frac{D}{V_{DS}}$$

$$\left[1 + \frac{q \frac{V_{sga}}{J_o} \left(\frac{2V_{DS}}{L_{DS}} \right)^4 n_{th} - 4 \left(\frac{2V_{DS}}{L_{DS}} \right)^4}{5E_c^4 + \left(\frac{2V_{DS}}{L_{DS}} \right)^4} \sum_{I=1}^{N} J_{DS}(I) \right] , \qquad (3.11)$$

where $J_{DS}(I)$ is the current density expression for III-V compound semiconductor devices as given in Eq. (2.40). V_{sga} is the saturated velocity of GaAs or InP and E_c is the electric field where negative differential mobility starts. J_o is as given in Eq. (3.5).

3.2.2.2b Vertical FETs. The conductance is obtained from Eq. (2.76) for silicon and from Eq. (2.78) for III-V compound semiconductor devices:

$$g_{ds} = 2Z \frac{\partial J_{DS}}{\partial V_{DS}} (D - y_{max}) - 2ZDJ_{DS} \frac{\partial y_{max}}{\partial V_{DS}} . \qquad (3.12)$$

After evaluation, Eq. (3.12) becomes

$$g_{ds} = 4Z \frac{D}{V_{DS}} \left[1 + \frac{q \frac{V_{sga}}{J_o} n_{th} \left(\frac{2V_{DS}}{L_{DS}} \right)^4 - 4 \left(\frac{2V_{DS}}{L_{DS}} \right)^4}{5E_c^4 + \left(\frac{2V_{DS}}{L_{DS}} \right)^4} \right]$$

$$-2ZDJ_{DS} \frac{L_G}{L'_{DS}} \frac{C_o^2}{y_{max}} \frac{1}{(D - y_{max})} \qquad (3.13)$$

3.2.3 Gate-Source Capacitance.

3.2.3a GFC-BARITT and SIT Devices. The total gate charge under small-signal conditions is:

$$Q_{GS}(t) = Q_{GS}(0) + \frac{\partial Q_{GS}(0)}{\partial V_{GS}} V_{gs}(t) \quad , \qquad (3.14)$$

where $Q_{GS}(0)$ = the charge at steady state and

$V_{gs}(t)$ = the small-signal gate-source voltage.

The gate-source capacitance is defined as

$$C_{gs} = \left| \frac{\partial Q_{GS}(0)}{\partial V_{GS}} \right|_{V_{DS}=\text{constant}}$$

The gate-source capacitance is the result of the variation of the charge in the channel with respect to the variation of the gate-source voltage. This charge is due to the injection of the carriers from the source into the channel:

$$Q_{GS} = q Z(1 + YV) \frac{D}{N} n_{th} L_G \sum_{I=1}^{N} e^{[(V_F(I)-\phi_G(I))/V_T]} , \qquad (3.15)$$

where YV is one for a vertical structure or YV is zero for a planar structure. Equation (3.15) does not include the effect of the carrier distribution. In reality, the stored charge in the channel is less than what is found from the drift-approximation of the injected carriers.

The effects of the diffusion on the small signal circuir parameters will be analyzed later in this chapter. For simplicity, in this section, diffusion effects will be ignored.

The gate-source capacitance is derived from the steady-state channel charge (Eq. (3.15) and given in Eq. (3.16)):

$$C_{gs} \cong C_{gs}(0)\frac{1}{V_T}\sum_{I=1}^{N}\left[1-\left(\frac{I-0.5}{N}\right)^2\right]e^{-([\phi_G(I)-V_F(I)]/V_T)} , \quad (3.16)$$

where $C_{gs}(0) = qZ(D/N)n_{th}L_G$. For the insulated gate devices, the total capacitance $C_{gs_t} = C_{gs}C_{ox}/(C_{gs} + C_{ox})$ where C_{ox} is the oxide capacitance.

3.2.3b Vertical FETs. The gate-source capacitance is due to the charge of the depletion layer. From Section 2.4, C_{gs} is obtained as

$$C_{gs} = 2qZN_D \left\{ \left[(W_G + y_{max}) \frac{\partial L'_{DS}}{\partial V_{GS}} + (L'_{DS} - L_G) \frac{\partial y_{max}}{\partial V_{GS}}\right] + L_G \frac{\partial y_{dep}(x)}{\partial V_{GS}} \right\} , \quad (3.17)$$

where

$$\frac{\partial L'_{DS}}{\partial V_{DS}} = \frac{1}{2} C_o (V_{GS} + V_{b_2} + V_{DS})^{-1/2} ,$$

$$\frac{\partial y_{dep}(x)}{\partial V_{GS}} = \frac{1}{2}\frac{C_o^2}{y_{dep}} \quad \text{and} \quad \frac{\partial y_{max}}{\partial V_{GS}} = \frac{1}{2}\frac{C_o^2}{y_{max}}\left(\frac{L_G}{L'_{DS}}\right).$$

3.2.4 Drain-Gate Feedback Capacitance.

3.2.4a GFC-BARITT and SIT Devices. Under the small-signal approximation, this capacitance is the variation of the charge at the gate due to the change in the drain-source voltage:

$$C_{gd} \triangleq \left.\frac{\partial Q_{GS}(0)}{\partial V_{DS}}\right|_{V_{GS}=\text{constant}} .$$

Differentiation of the $Q_{GS}(0)$ with respect to V_{DS} results in the following expression for C_{gd}:

$$C_{gd} \cong qZ \frac{D}{N} \frac{n_{th} L_G}{V_T} \sum_{I=1}^{N} \frac{V_F(I)}{V_{DS}} e^{[(V_F(I)-\phi_G(I))/V_T]} \quad . \tag{3.18}$$

3.2.4b Vertical FETs. The feedback capacitance of the drain-gate is due to the variation of the drain-gate depletion layer with V_{DS}:

$$C_{gd} = 2qZN_D \left\{ \left[(W_G + y_{max}) \frac{\partial L'_{DS}}{\partial V_{DS}} + (L'_{DS} - L_G) \frac{\partial y_{max}}{\partial V_{DS}} \right] + L_G \frac{\partial y_{dep}}{\partial V_{DS}} \right\} \quad , \tag{3.19}$$

where

$$\frac{\partial Y_{dep}(L_G)}{\partial V_{DS}} = \frac{1}{2} \frac{C_o^2}{Y_{dep}(L_G)} \frac{L_G}{L_{DS}} \quad ,$$

$$\frac{\partial y_{max}}{\partial V_{DS}} = \frac{1}{2} \frac{C_o^2}{Y_{max}} \frac{L_G}{L_{DS}}$$

and

$$\frac{\partial L'_{DS}}{\partial V_{DS}} = \frac{1}{2} C_o (V_{GS} + V_{b2} + V_{DS})^{-1/2} \quad .$$

3.2.5 Drain-Source Capacitance.

3.2.5a GFC-BARITT and SIT Devices. The drain-source capacitance is defined as the variation of the channel charge with respect to a change of the drain-source voltage:

$$C_{ds} = \frac{\partial Q_{DS}}{\partial V_{DS}}\bigg|_{V_{GS}=\text{constant}} ,$$

where

$$Q_{DS} = 2qZn_{th}\frac{D}{N} L_{DS} \sum_{I=1}^{N} e^{[(V_F(I)-\phi_G(I))/V_T]} . \quad (3.20)$$

This, however, does not include the diffusion effect. C_{ds} is obtained from Eq. (3.20) as follows:

$$C_{ds} \cong 2qZn_{th}\frac{D}{N} L_{DS} \frac{1}{V_T} \sum_{I=1}^{N} \frac{V_F(I)}{V_{DS}} e^{[(V_F(I)-\phi_G(I))/V_T]} . \quad (3.21)$$

By comparing Eq. (3.21) with Eq. (3.18), C_{ds} can be related to C_{gd} as in Eq. (3.22):

$$C_{ds} = \frac{L_{DS}}{L_G} C_{gd} . \quad (3.22)$$

<u>3.2.5b</u> <u>Vertical FETs</u>. The drain-source capacitance can be approximated as

$$C_{ds} = \frac{\partial Q_{DS}}{\partial V_{DS}}\bigg|_{V_{GS}=\text{constant}} ,$$

where

$$Q_{DS} = 2qZL'_{DS}(D - y_{max})N_D$$

and

$$C_{ds} = 2qZN_D \left[\frac{\partial L'_{DS}}{\partial V_{DS}} (D - y_{max}) - L'_{DS} N_D \frac{\partial y_{max}}{\partial V_{DS}} \right] . \qquad (3.23)$$

3.3 Diffusion Effects on Small-Signal Circuit Parameters

In this section, the small-signal circuit parameters are obtained by using the drift-diffusion device expressions of the GFC-BARITT and the SIT device given in Chapter II. Derivation of the small-signal parameters is the same as in the previous sections. Therefore, in this section only the final expressions will be given.

3.3.1 The Transconductance. The drift-diffusion current expression in Eq. (2.24) is differentiated with respect to V_{GS}, and the resulting g_m expression is given by

$$g_m = AM \sum_{I=1}^{N} \left[DRVGS \exp(USS1 + USS2) + V_T \frac{\partial}{\partial V_{GS}} USS2 \exp(USS1 + USS2) \right] , \qquad (3.24)$$

where

$$AM \triangleq qZ \frac{W_S}{N} \frac{n_{th}}{V_T} v_{sat} ,$$

$$DRVGS \triangleq 1 - \left(\frac{I - 0.5}{N} \right)^2 ,$$

$$USS1 \triangleq (V_F(I) - \phi_G(I))/V_T$$

and

$$USS2 \triangleq -0.5 \ \alpha L_S^2 + k'_1 L_S .$$

<u>3.3.2 The Conductance</u>. The conductance is obtained by differentiating Eq. (2.24) with respect to V_{DS}:

$$g_{ds} = AM \sum_{I=1}^{N} \left\{ \frac{\partial V_F(I)}{\partial V_{DS}} \exp(USS1 + USS2) - \frac{\partial}{\partial V_{DS}} (USS2) \exp(USS1 + USS2) \right\}, \tag{3.25}$$

where AM, USS1 and USS2 are defined in Section 3.3.1.

<u>3.3.3 The Gate-Source Capacitance</u>. C_{gs} is obtained from the stored charge in the channel. For the insulated gate devices, the total gate-source capacitance is obtained from the series combination of the insulated gate capacitance and the stored charge capacitance.

The stored charge capacitance is

$$C_{gs} = AC \sum_{I=1}^{N} \left\{ \frac{1}{V_T} \frac{\partial \phi_G(I)}{\partial V_{GS}} \exp(USS1) \sum_{J=1}^{NN} \exp(USS3) + \exp(USS1) \cdot \sum_{J=1}^{NN} \frac{\partial}{\partial V_{GS}} (USS3) \exp(USS3) \right\}, \tag{3.26}$$

where $USS3 \triangleq k_1' \frac{L_S}{NN} J - 0.5\alpha \left(\frac{L_S}{NN} J\right)^2$,

NN = an integer and

$$AC \triangleq qZ \frac{W_S}{N} n_{th} \frac{L_G}{NN}$$

Equation (3.26) is valid for $L_S \geq L_G$, if $L_S < L_G$, then after replacing L_G with L_S just in AC, Eq. (3.26) becomes applicable for this case also.

The total capacitance, G_{gs_t}, is defined as

$$C_{gs_t} = C_{ox}C_{gs}/(C_{ox} + C_{gs}) ,$$

where C_{ox} is the oxide capacitance.

3.3.4 The Drain-Gate Feedback Capacitance. C_{gd} is also obtained from the stored charge in the channel by differentiating it with respect to V_{DS}:

$$C_{gd} = AC \sum_{I=1}^{N} \left\{ \frac{1}{V_T} \frac{\partial V_F(I)}{\partial V_{DS}} \exp(USS1) \sum_{J=1}^{NN} \exp(USS3) + \exp(USS1) \cdot \sum_{J=1}^{NN} \frac{\partial}{\partial V_{DS}} (USS3)\exp(USS3) \right\} . \quad (3.27)$$

Equation (3.27) is derived for $L_S \geq L_G$, for the cases of $L_G > L_S$, just in AC, L_G has to be replaced by L_S.

3.3.5 The Drain-Source Capacitance. C_{ds} is approximated from the C_{gd} expression by

$$C_{ds} = \frac{L_S}{L_G} C_{gd} . \quad (3.28)$$

For $L_S > L_{DS}$, L_S should be replaced by L_{DS}. If $L_S < L_G$, replace (L_G/NN) with (L_S/NN) in Eq. (3.27).

3.4 Carrier Transit Time Effect

The carriers are injected from the source electrode, drift along the channel and are collected at the drain electrode after a drift time, τ_d. Because of this drift time, changes in the drain-source current will occur in τ_d second following the changes in input. This delay causes a phase difference θ between the terminal voltage and the terminal current. The drift time is also called a "transit time". It is formulated as

$$\tau_d = \int_0^{L_{DS}} \frac{dx}{v(x)} , \qquad (3.29)$$

where v(x) = the carrier velocity as a function of the local electric field along the conduction path, and

x = the distance that carriers travel in the conduction path.

This transit time is included in the device expressions through the assumption of an unattenuated current wave expression in the drift region [28]:

$$i_{ds} = I_{DS} \exp(-j\omega\tau_d) . \qquad (3.30)$$

The small signal transconductance and conductance expressions are obtained from the current wave equation in Eq. (3.30), and given in Eq. (3.31) and Eq. (3.32), respectively:

$$g_m^* = g_m e^{-j\omega\tau_d} \qquad (3.31)$$

and

$$g_{ds}^{*} = g_{ds}\, e^{-j\omega\tau_d} \quad . \tag{3.32}$$

Assuming a linear electric field distribution along the channel, the τ_d expression will be evaluated for silicon and for the III-V compound semiconductor devices.

3.4.1 Silicon Devices. The velocity expression of silicon as a function of field is inserted in Eq. (3.29):

$$\tau_d = \int_{x=L_F}^{L_{DS}} \frac{dx}{v_{sat}\dfrac{E(x)}{(E_{sat} + E(x))}} \quad , \tag{3.33}$$

where $E(x) = \gamma_1 x$,

$\gamma_1 = 2(V_{DS} + V_B)/(L_{DS} - L_F)^2$,

L_F = the depletion width at the forward biased junction and

L_{DS} = the channel length.

The integration of Eq. (3.33) results in

$$\tau_d = \frac{1}{\gamma_1 v_{sat}}\left\{E_{sat}\ \ln\left(\frac{L_{DS}}{L_F}\right) + \gamma_1(L_{DS} - L_F)\right\} \quad , \tag{3.34}$$

where

$$L_F = \left[\frac{2\varepsilon_s\,(V_B - V_F)}{qN_A}\right]^{1/2}$$

for a GFC-BARITT device and L_F = the Debye length for a SIT.

The transit time effect on g_m and g_{ds} can be accounted for by inserting Eq. (3.34) into Eq. (3.31) for transconductance and in Eq. (3.32) for conductance.

3.4.2 III-V Compound Semiconductor Devices. The field distribution is a linear function of the conduction path. In this section the only difference is the expression of the carrier velocity which is given in Eq. (2.36) in Chapter II. Following the procedure for silicon devices the conductance and transconductance expressions are derived and given in Eq. (3.35) and Eq. (3.36), respectively. These expressions are in the form of numerical integrations. Explicit expressions could not be derived due to complex carrier velocity expressions for III-V compound semiconductors.

Conductance:

$$g_{ds}^{*} = g_{ds}\, e^{-j\theta} \quad . \tag{3.35}$$

Transconductance:

$$g_m^{*} = g_m\, e^{-j\theta} \quad , \tag{3.36}$$

where $\theta = \omega\tau_d$ and τ_d. The transit time is given in Eq. (3.37):

$$\tau_d \overset{\Delta}{=} \Gamma \sum_{J=1}^{NN} \left\{ \frac{1 + (\gamma_1/E_c)^4 \Gamma^4 J^4}{\gamma_1 \mu_{no} \Gamma J + (v_{sga})(\gamma_1/E_c)^4 \Gamma^4 J^4} \right\}, \tag{3.37}$$

where

$$\Gamma = \frac{(L_{DS} - L_F)}{NN} .$$

3.5 Large-Signal Analysis

3.5.1 Introduction. The dc analysis of the TTPT SIT and the GFC-BARITT devices have been done by closely following the BARITT diode analysis. The large-signal behavior of these devices are different from those of the BARITT diodes. The negative resistance is essential for the use of a BARITT diode. On the other hand, the TTPT devices amplify the input signal which is applied to the gate and transmit the amplified signal to the output port. The directionality of the three-terminal devices is an advantage over the two-terminal BARITT diodes.

The simplified analysis of the BARITT diodes overestimates the efficiency and the power capability of these devices [32], [33]. Numerical analysis [34],[35],[36],[50] and experimental studies [35],[37] have shown that the early predictions for the efficiency and the power capability of the BARITT diodes are orders of magnitude higher than the real values. The three-terminal punch-through devices have the high efficiency capability of the bipolar junction transistors (BJTs) and the high frequency operation capability of the punch-through diodes. A collector efficiency up to 55 percent for a SIT has been reported [2].

In this section, the large-signal analysis is done by making the following assumptions:

(i) The model is valid for operating frequencies below the cut-off frequency which is defined as the frequency where the phase difference between the input signal and the output signal becomes 2π.

(ii) The quiescent point is chosen in such a manner that the gate channel junction is not forward biased in the case of a SIT analysis.

(iii) A load impedance is calculated to match the predetermined voltage of the device.

(iv) The electric field along the channel is assumed to be determined by the dc bias conditions.

(v) The change in barrier height at the injection junction follows the input signal.

(vi) The space charge effects will be ignored.

The small-signal circuit parameters will be modified for the large-signal case. In the next section, the derivation of those parameters is given.

3.5.2 Large-Signal Circuit Parameters. The equivalent circuit model which is used for the small-signal approximation, will be used in the large signal cases also. Instead of calculating circuit elements from the dc device expressions, they are obtained by using the average values of the time-dependent circuit parameters. A similar approach has been used to derive the large-signal circuit parameters of a MESFET from the dc device expressions [38],[39]. The derivation of the large-signal circuit elements is given for silicon and for III-V compound semiconductors in the following sections.

3.5.2.1 GFC-BARITT and SIT Devices. The time-dependent current is given by Eq. (3.38):

$$I_{ds}(\omega t) = I_{DSO} \sum_{I=1}^{N} \exp\left[\frac{VF(I) - \phi_G(I)}{V_T}\right]$$

$$\cdot \exp\left[\frac{V_{in}(I)DERV_{GS}(I)\sin(\omega t) + V_o(I)DERV_{DS}\sin(\omega t - \theta)}{V_T}\right], \qquad (3.38)$$

where I_{DSO} is the leakage current. $DERV_{GS}(I) = \partial V_F(I)/\partial V_{GS}$ and $DERV_{DS} = \partial V_F(I)/\partial V_{DS}$. The Fourier series expansion of Eq. (3.38) separates the dc and ac currents. Considering only the first harmonic,

$$I_{ds}(\omega t) = a_o + a_1 \cos(\omega t) + b_1 \sin(\omega t) , \qquad (3.39)$$

where a_o is the average dc current,

$$a_o = \frac{1}{2\pi}\int_0^{2\pi} I_{ds}(\omega t)\, d\omega t ,$$

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} I_{ds}(\omega t)\cos(\omega t)\, d\omega t$$

and

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} I_{ds}(\omega t)\sin(\omega t)\, d\omega t .$$

The $V_{in}\sin(\omega t)$ is the input RF voltage and the $V_o\sin(\omega t - \theta)$ is the output RF voltage due to the voltage drop across the load impedance under large signal conditions. These two RF voltages can be assumed to be known. From the known terminal voltages, the required load impedance can then be calculated. A detailed explanation of the large signal modeling is given in Section 4.7 of Chapter IV.

The Fourier coefficients are

$$a_o = \frac{I_{DSO}}{2\pi} \int_{o}^{2\pi} \sum_{I=1}^{N} \exp\left[\frac{V_{DSQ} \cdot DERV_{DS} - V_{GSQ} \cdot DERV_{GS}(I)}{V_T}\right]$$

$$\cdot \exp\left[+ \frac{V_{in}}{V_T} DERV_{GS}(I) \sin(\omega t) + \frac{V_o}{V_T} DERV_{DS} \sin(\omega t - \theta)\right] \cdot d\omega t \quad , \qquad (3.40)$$

$$I_1(I,J) = \exp\left[\frac{VDSQ \cdot DERV_{DS} - VGSQ \cdot DERV_{GS}(I)}{V_T}\right]$$

$$\cdot \exp\left[+ \frac{V_{in}}{V_T} DRV_{GS}(I) \sin(\omega t) + \frac{V_o}{V_T} DRV_{DS} \sin(\omega t - \theta)\right] , \qquad (3.41)$$

$$I_2(I,J) = I_1 \sin(\omega t) \quad , \qquad (3.42)$$

and

$$I_3(I,J) = I_1 \cos(\omega t) \quad . \qquad (3.43)$$

The average dc current I_{DS} is given by Eq. (3.44):

$$I_{DS} = \frac{I_{DSO}}{M} \sum_{J=1}^{M} \sum_{I=1}^{N} I_1(I,J) \quad . \qquad (3.44)$$

The coefficient of $\cos(\omega t)$, a_1 can be expressed as a function of ENT1 which is given in Eq. (3.45);

$$ENT1 = \frac{2}{M} \sum_{J=1}^{M} \sum_{I=1}^{N} I_3(I,J) \qquad (3.45)$$

and

$$a_1 = I_{DSO}\,\mathrm{ENT1} \quad . \tag{3.46}$$

The coefficient of $\sin(\omega t)$ b_1 is given as a function of ENT2 in Eq. (3.48):

$$\mathrm{ENT2} = \frac{2}{M} \sum_{J=1}^{M} \sum_{I=1}^{N} I_2(I,J) \quad , \tag{3.47}$$

$$b_1 = I_{DSO}\,\mathrm{ENT2} \quad , \tag{3.48}$$

where I_{DSO} is

$$I_{DSO} = z \frac{W_S}{N} \frac{n_{th}}{V_T} V_{sat}$$

for the drift diffusion model. It is valid for both Si and III-V compound semiconductors. In the case of the drift model,

$$I_{DSO} = J_o \frac{W_S}{N}$$

for the III-V compound semiconductors and

$$I_{DSO} = Z\, V_{sat} \frac{W_S}{N} \frac{V_{DS}}{V_{DS} + E_{sat} L_{DS}} n_{th}$$

for silicon.

The effective g_m is given by Eq. (3.49):

$$g_{m_{eff}} = DERV_{GS}(I)\left(b_2^2 + \frac{a_1^2}{2}\right)^{1/2} . \qquad (3.49)$$

The conductance can be found and is similar to the transconductance:

$$g_{ds_{eff}} = DERV_{DS}\left(b_1^2 + \frac{a_1^2}{2}\right)^{1/2} . \qquad (3.50)$$

The gate-source capacitance can be approximated from the time dependent gate charge

$$Q_{GS}(\omega t) = Z\frac{W_S}{N}\frac{L_G}{M}\sum_{I=1}^{N} n_{inj}(I)\exp\left[\frac{V_{in}(I)}{V_T}\sin(\omega t) + \frac{V_o}{V_T}\sin(\omega t - \theta)\right], \qquad (3.51)$$

where

$$AC = Z\frac{W_S}{N}\frac{L_G}{M}q ,$$

$$c_{gd_{eff}} = AC(b_1^2 + 0.5\ a_1^2)^{1/2} DERV_{GS}(I) , \qquad (3.52)$$

$$c_{gd_{eff}} = AC(b_1^2 + 0.5 a_1^2)^{1/2}\ DERV_{DS}(I) \qquad (3.53)$$

and

$$c_{ds_{eff}} = C_{ds}(\text{small signal value}) . \qquad (3.54)$$

3.5.2.2 Vertical FETs.

3.5.2.2a Silicon FETS. The total current $I_{ds}(\omega t)$ is given by Eq. (3.55):

$$I_{ds}(\omega t) = AF \frac{V_{DSQ} + V_o \sin(\omega t - \theta)}{[L_{DS}E_{sat} + V_{DSQ} + V_o \sin(\omega t - \theta)]} (D - Y_{max}(\omega t)) \quad , \tag{3.55}$$

where

$$AF = 2ZqN_D V_{sat}$$

and

$$Y_{max}(\omega t) = C_o^{1/2} (V_{GSQ} + V_{in} \sin \omega t)^{1/2} \; .$$

The Fourier series expansion of the $I_{ds}(\omega t)$ will result in the dc and the ac currents:

$$I_{DS} = \frac{1}{2\pi} \int_0^{2\pi} I_{ds}(\omega t)\, d\omega t \quad . \tag{3.56}$$

The new numerical integrals can be defined as follows:

$$IE1 = \frac{(V_{DSQ} + V_o \sin(\omega t - \theta))}{(L_{DS}E_{sat} + V_{DSQ} + V_o \sin(\omega t - \theta))} \left[D - C_o^{1/2}(V_{GSQ} + V_{in} \sin \omega t)^{1/2}\right] \quad , \tag{3.57}$$

$$I_{DS} = \frac{AF}{360} \sum_{J=1}^{M} EI1 = a_0 \quad , \tag{3.58}$$

$$a_1 = \frac{AF}{90} \sum_{J=1}^{M} EI1 \cos\left(\frac{\pi}{180} J\right) \tag{3.59}$$

and

$$b_1 = \frac{AF}{90} \sum_{J=1}^{M} EI1 \sin\left(\frac{\pi}{180} J\right) \quad . \tag{3.60}$$

From the total current, I_{eff} is obtained and

$$I_{ds}(\omega t) = a_o + a_1 \cos(\omega t) + b_1 \sin(\omega t) , \tag{3.61}$$

$$I_{eff} = [b_1^2 + \frac{a_1^2}{2}]^{1/2} . \tag{3.62}$$

The effective transconductance $g_{m_{eff}}$ is

$$g_{m_{eff}} = DERV_{GS}(I)\ I_{eff} , \tag{3.63}$$

where

$$DERV_{GS}(I) = 0.5\ C_o^{1/2} .$$

The effective conductance is

$$g_{ds_{eff}} = DERV_{DS}\ I_{eff} , \tag{3.64}$$

$$DERV_{DS} = \frac{E_s L'_{DS}}{(V_{DSQ} + V_o \frac{2}{\pi} + E_s L'_{DS})^2} .$$

The gate charge is $Q_{GS}(\omega t)$:

$$Q_{GS}(\omega t) = 2ZqN_D[L_G Y_{max}(\omega t) + Y_{GD}(\omega t) Y_{max}(\ t)] . \tag{3.65}$$

The source gate capacitance is given by Eq. (3.66):

$$C_{gs}(\omega t) = ZqN_D \left[L_G + C_o^{1/2}(V_{DSQ} + V_o \sin(\omega t - \theta))^{1/2}\right] \left[\frac{C_o}{V_{GSQ} \pm V_{in} \sin(\omega t)}\right]^{1/2} . \quad (3.66)$$

The effective C_{gs} at the fundamental frequency is given by Eq. (3.67):

$$C_{gs_{eff}} = 2ZqN_D(EI5^2 + 0.5EI6^2)^{1/2} , \quad (3.67)$$

where

$$EI5 = \frac{C_o^{1/2}}{M} \sum_{J=1}^{M} \left[L_G + C_o^{1/2}\left(V_{DSQ} + V_o \sin\left(\frac{\pi}{M} j - \theta\right)\right)^{1/2} \frac{1}{\left(V_{GSQ} + V_{in}\sin \frac{2\pi}{M} J\right)^{1/2}} \sin\left(\frac{2\pi}{M} J\right)\right]$$

and

$$EI6 = \frac{C_o^{1/2}}{M} \sum_{J=1}^{M} \left[L_G + C_o^{1/2}\left(V_{DSQ} + V_o \sin\left(\frac{2\pi}{M} J - \theta\right)\right)^{1/2} \cdot \frac{1}{\left[V_{GSQ} + V_{in}\sin\left(\frac{2\pi}{M} J\right)\right]^{1/2}} \cos\left(\frac{2\pi}{M} J\right)\right] .$$

The effective C_{gd} at the fundamental frequency is obtained similar to g_{gs} and given in Eq. (3.68):

$$C_{gd_{eff}} = 2ZqN_D(EI7^2 + EI8^2/2)^{1/2} \quad , \qquad (3.68)$$

where

$$EI7 = \frac{C_o}{M} \sum_{J=1}^{M} EI0^{1/2} \sin\left(\frac{2\pi}{M} J\right) \; ,$$

$$EI8 = \frac{C_o}{M} \sum_{J=1}^{M} EI0^{1/2} \cos\left(\frac{2\pi}{M} J\right)$$

and

$$EI0 = \frac{V_{GSQ} + V_{in} \sin\left(\frac{2\pi}{M} J\right)}{V_{DSQ} + V_o \sin\left(\frac{2\pi}{M} J - \theta\right)} \; .$$

The effective C_{ds} at the fundamental frequency is equal to $C_{gd_{eff}}$ in Eq. (3.69):

$$C_{ds_{eff}} = C_{gd_{eff}} \; . \qquad (3.69)$$

<u>3.5.2.2b</u> <u>III-V Compound Semiconductor FETs</u>. The current, transconductance and conductance expressions of the III-V compound semiconductor (III-V C-S) FETs are different than those of the Si FETs. The capacitance expressions are the same as those given in Section 3.5.2.2a.

The total time dependent current can be expressed as in Eq. (3.70):

$$I_{ds}(\omega t) = 2Z(D - Y_{max})J_o qN_D \; , \qquad (3.70)$$

where

$$J_o = \frac{2.5\mu_{no}E_c^4EF + v_{sga}EF^4}{5E_c^4 + EF^4} \quad ,$$

$$V'_{DS}(\omega t) = V_{DSQ} + V_o \sin(\omega t - \theta) \quad ,$$

$$V'_{GS}(\omega t) = V_{GSQ} + V_{in} \sin(\omega t)$$

and

$$EF = 2V'_{DS}(\omega t)/L_{DS} \quad .$$

By following the usual procedure, I_{eff} is obtained and given in Eq. (3.71):

$$I_{eff} = \frac{2ZqN_D}{M} (b_1^2 + 0.5\, a_1^2)^{1/2} \quad , \qquad (3.71)$$

where

$$a_1 = \sum_{J=1}^{M} ET1 \cos\left(\frac{2\pi}{M} J\right) \quad ,$$

$$b_1 = \sum_{J=1}^{M} ET1 \sin\left(\frac{2\pi}{M} J\right) \quad ,$$

$$ET1 = D - (C_o\, V_{GSQ}(\omega t))^{1/2}\, J_o$$

The effective transconductance, $g_{m_{eff}}$ is derived from the effective ac current I_{eff} and given by Eq. (3.72):

$$g_{m_{eff}} = DERV_{GS}\, I_{eff} \qquad (3.72)$$

and finally the effective conductance is given in Eq. (3.73):

$$g_{ds_{eff}} = DERV_{DS}\ I_{eff} \quad . \qquad (3.73)$$

3.6 Small-Signal Circuit Properties

3.6.1 Admittance Parameters. An equivalent circuit of a SIT or GFC-BARITT device is shown in Fig. 3.1. In this equivalent circuit, parasitic resistances of the electrodes are included to analyze their effect on the performance of the device.

The y-parameters are obtained by a straightforward circuit analysis of the equivalent circuit in Fig. 3.1. These expressions for the y-parameters are:

$$y_{11} = G_g(1 - \beta_1) \ , \qquad (3.74)$$

$$y_{12} = -G_g \cdot \beta_2 \ , \qquad (3.75)$$

$$y_{21} = G_d \cdot \beta_3 \ , \qquad (3.76)$$

$$y_{22} = G_d(1 - \beta_4) \ , \qquad (3.77)$$

where

$$\beta_1 = -\frac{\gamma'_1}{x_{11}} G_g + \frac{\gamma'_2 G_g}{z_{11} x_{11}} ,$$

$$\beta_2 = \frac{G_g}{z_{11} x_{21}} - \frac{\gamma'_1 G_d}{x_{21}} - \frac{\gamma'_2 G_d}{z_{21} x_{21}} ,$$

$$\beta_3 = \frac{G_g}{x_{11} z_{11}} - \frac{G_g}{z_{11} x_{11}} \left(\frac{z'_{12}}{z'_{12} - z'_{21}} \right) ,$$

$$\beta_4 = \frac{G_d}{z_{11} x_{21}} - \frac{G_d}{x_{21} z_{21}} - \frac{G_d}{x_{21} z_{11}} \left(\frac{z'_{12}}{z'_{12} - z'_{22}} \right) ,$$

$$\gamma'_1 = \frac{x'_{32}}{z_{11}} , \quad \gamma'_2 = \left(\frac{x'_{32} z'_{12} - x'_{33}}{z'_{12} - z'_{22}} \right) ,$$

$$z'_{12} = \frac{z_{12}}{z_{11}} , \quad z'_{22} = \frac{z_{22}}{z_{21}} , \quad zy'_1 = \frac{zy_1}{z_{11}} , \quad zy'_2 = \frac{zy_2}{z_{21}} ,$$

$$z_{11} = x'_{22} - x'_{12} \ , \quad z_{12} = x'_{23} - x'_{13} \ , \quad zy_1 = xy'_1 + xy'_2 \ ,$$

$$zy_2 = xy'_2 \ ,$$

$$z_{21} = x'_{32} + x'_{22} \ , \quad z_{22} = x'_{33} + x'_{23} \ ,$$

$$x'_{12} = \frac{x_{12}}{x_{11}} \ , \quad x'_{13} = \frac{x_{13}}{x_{11}} \ , \quad xy'_1 = \frac{xy_1}{x_{11}} \ , \quad x'_{32} = \frac{x_{32}}{x_{31}} \ ,$$

$$x'_{33} = \frac{x_{33}}{x_{31}} \ ,$$

$$x'_{22} = \frac{x_{22}}{x_{21}} \ , \quad x'_{23} = \frac{x_{23}}{x_{21}} \ , \quad xy'_2 = \frac{xy_2}{x_{21}} \ ,$$

$$G_g = \frac{1}{R_m} \ , \quad G_d = \frac{1}{R_d} \ ,$$

$$x_{11} = \frac{1}{R_m} - j\omega C_{gs} - y_1 \ , \quad x_{21} = g_m^* + j\omega C_{gs} \ ,$$

$$x_{12} = j\omega C_{gs} \ , \quad x_{13} = y_1 \ , \quad x_{22} = G_{ds}^* + j\omega C_{ds} + j\omega C_{gs} \ ,$$

$$x_{13} = y_1 \ , \quad x_{23} = g_m^* + G_{ds}^* + j\omega C_{ds} \ , \quad xy_1 = V_{in} \frac{1}{R_m} \ ,$$

$$x_{31} = y_1 - g_m^* \ , \quad x_{32} = G_{ds}^* + j\omega C_{ds} \ , \quad xy_2 = V_{out} \frac{1}{R_d} \ ,$$

$$x_{33} = g_m^* - \frac{1}{r_s} - G_{ds}^* - j\omega C_{ds} - y_1$$

and

$$y_1 = \frac{(1/R_c) - j\omega C_{gs}}{1 + \omega^2 \ C_{gs} R_c^2} \ .$$

In the case of the equivalent circuit of the intrinsic device, the y-parameters become much simpler than those given in Eqs. (3.74) through (3.77).

The y-parameters for $R_m \tilde{=} 0$, $R_f \tilde{=} 0$ and $R_d \tilde{=} 0$ become

$$y_{11} = \frac{1}{R_c} + j\omega(C_{gs} + C_{gd}) \quad , \qquad (3.78)$$

$$y_{12} = j\omega C_{gd} \quad , \qquad (3.79)$$

$$y_{21} = -(g_m^* + j\omega C_{gd}) \qquad (3.80)$$

and

$$y_{22} = g_{ds}^* + j\omega(C_{ds} + C_{gd}) \quad , \qquad (3.81)$$

where the asterisk implies that the transit time is accounted for in the g_m and g_{ds} expressions. R_c is the gate charging resistance; and it is usually measured. In this case, however, the dc contact resistance will be used.

3.6.2 S-Parameters. At high frequencies the measurements are made in terms of the scattering, s-parameters. Therefore, it is useful to relate measured parameters to intrinsic device parameters. Such expressions are given in a text [40]. In this section, the y-parameters are known, therefore, the s-parameters will be calculated in terms of the y-parameters. The expressions which relate the s-parameters with the y-parameters are:

$$s_{11} = \frac{(1 - y'_{11})(1 + y'_{22}) + y'_{12}y'_{21}}{(1 + y'_{11})(1 + y'_{22}) - y'_{12}y'_{21}} , \quad (3.82)$$

$$s_{12} = \frac{-2y'_{12}}{(1 + y'_{11})(1 + y'_{22}) - y'_{12}y'_{21}} , \quad (3.83)$$

$$s_{21} = \frac{-2y'_{21}}{(1 + y'_{11})(1 + y'_{22}) - y'_{12}y'_{21}} , \quad (3.84)$$

$$s_{22} = \frac{(1 + y'_{11})(1 - y'_{22}) + y'_{12}y'_{21}}{(1 + y'_{11})(1 + y'_{22}) - y'_{12}y'_{21}} . \quad (3.85)$$

If only the s-parameters for the devices are known, then the y-parameters can be calculated by using the following expressions given in Reference [40]:

$$y'_{11} = y_{11}R_o = \frac{(1 - s_{11})(1 + s_{22}) + s_{12}s_{21}}{(1 + s_{11})(s_{22} + 1) - s_{12}s_{21}} , \quad (3.86)$$

$$y'_{12} = y_{12}R_o = \frac{-2s_{12}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} , \quad (3.87)$$

$$y'_{21} = y_{21}R_o = \frac{-2s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} , \quad (3.88)$$

$$y'_{22} = y_{22}R_o = \frac{(1 + s_{11})(1 - s_{22}) + s_{12}s_{22}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} , \qquad (3.89)$$

where R_o = the resistance of the transmission line system (i.e., 50 ohm or 75 ohm, etc.) and

y'_{ij} = the normalized y-parameters.

3.6.3 Gain and Gain Bandwidth Product. Gain is one of the figures of merit for the amplifying devices. For the case of small signal, one can define two types of gain:

(i) Maximum available gain (MAG)

$$MAG = \frac{|y_{21}|^2}{4 \text{ Real } (y_{11}) \text{ Real } (y_{22})} \qquad (3.90)$$

and

(ii) the maximum unilateral gain (MUG). It is given in terms of the s-parameters in Eq. (3.91):

$$MUG = \frac{|s_{21}|^2}{(1 - |s_{11}|^2)(1 - |s_{22}|^2)} \qquad (3.91)$$

for $|s_{11}| < 1$

$|s_{22}| < 1$

and

$s_{12} = 0$.

In addition to the gain of an amplifying device, its cut-off frequency, noise figure, and noise measure are also important figures of merit. The noise analysis is rather lengthy and will therefore be done in a different section. The cut-off frequency, f_T also known as "unity gain-bandwidth product" can readily be calculated in terms of the small-signal circuit parameters:

$$f_T = \frac{g_m}{2\pi(C_{gs})} . \qquad (3.92)$$

Equation (3.92) is derived by assuming a very simplified equivalent circuit for the device. The f_T is obtained from the equality of the input and output currents. The resulting Eq. (3.92) may be misleading in many cases as discussed in [41]. Because of the effect of the transit time on g_m is neglected. Also, the g_m used is the dc transconductance; the ac transconductance is expected to be less than the dc value.

An alternative expression for the f_T is given in Eq. (3.95) and is a more physically meaningful one than Eq. (3.92). The phase shift is due to transit time θ.

$$\theta = \omega\tau_d . \qquad (3.93)$$

The device is useful up to $\theta = 2\pi$:

$$2\pi = 2\pi f_T \tau_d , \qquad (3.94)$$

$$f_T = \frac{1}{\tau_d} . \qquad (3.95)$$

3.6.4 The Stability Analysis. Under certain terminating conditions, the devices may oscillate due to the internal feedback of the device. The inherent stability conditions are given in Reference [40] and listed below:

(i) $|s_{12}s_{21}| < 1 - |s_{11}|^2$, (3.96)

(ii) $|s_{21}s_{12}| < 1 - |s_{22}|^2$, (3.97)

(iii) $2|s_{12}s_{21}| < 1 - |s_{11}|^2 - |s_{22}|^2 + s_{11}s_{22} - s_{12}s_{21}$. (3.98)

All three inequalities have to be satisfied simultaneously for the inherent stability of a device.

3.7 Large-Signal Power and Gain of the TTPT Devices

An equivalent circuit of the three-terminal punch-through devices is shown in Fig. 3.1. The same equivalent circuit will be used with the large-signal circuit parameters to obtain the output power gain and the efficiency of these devices. The y- and s-parameters of the equivalent circuit are already known from Section 3.6. In the large signal case, the load impedance, Z_L, cannot be assumed to match the output impedance of the device, unlike the small-signal case.

The load current, i_L, can be approximated as

$$i_L = I_{eff} . \tag{3.99}$$

From Section 3.5, the I_{eff} is directly used instead of the $-g_m^* V_{gs}$ approximation. The g_m^* is the average transconductance, therefore V_{gs} must be the effective gate voltage.

The output power, P_o, is

$$P_o = I_{eff}^2/\mathrm{Real}(y_L) \tag{3.100}$$

and the dissipated power, P_{DC}, is

$$P_{DC} = V_{DSQ} I_{ds}(\mathrm{average}) \quad . \tag{3.101}$$

The collector efficiency, η_c, is

$$\eta_c = \frac{P_o}{P_{DC}} \quad . \tag{3.102}$$

The added power efficiency, η_a is given in Eq. (3.103) :

$$\eta_a = \eta_o - \frac{P_{in}}{P_{DC}} \quad . \tag{3.103}$$

The input power, P_{in}, is

$$P_{in} = \frac{V_{gs}^2}{2} Re(y_{in}) \quad , \qquad (3.104)$$

where the y_{in} is the input admittance as

$$y_{in} = y_{11} - \frac{y_{12} y_{21}}{y_{22} + y_L}$$

and y_L is the load admittance. The power gain, G_p, is defined as

$$G_p = \frac{P_o}{P_{in}} \quad . \qquad (3.105)$$

Then finally the power gain expression is given in Eq. (3.106):

$$G_p = \frac{2V_o I_{eff}}{V_{gs}^2 Real(y_{in})} \quad . \qquad (3.106)$$

3.8 Noise Analysis

3.8.1 Introduction. The noise contributions to the small-signal current and voltage of the injection type devices, specifically for BARITT diodes, arises from two main sources:

(i) the shot noise due to the randomness of the injection process at the forward biased junction discussed in [42] through [44] and

(ii) diffusion noise due to the carrier velocity fluctuations in the dirft-diffusion region of a BARITT diode and analyzed in [42], [43], and [45].

SIT and GFC-BARITT devices are also injection type devices, therefore the noise analyses of a BARITT diode can be extended to SIT and GFC-BARITT devices. In the case of the three-terminal SIT and GFC-BARITT devices, the gate noise current has to be derived in addition to the drain-source noise currents.

A formal procedure to derive the gate noise current of FETs has been given by Van der Ziel [46]. Following the approach of Van der Ziel, an expression for the noise current of the gate is obtained. Only the major part of the gate noise is considered because Van der Ziel has derived the gate noise from the coupling of the drain source noise current through the gate electrode. In addition to this coupling noise, there is another source of noise which is due to the gate-channel interface. This is especially important for the insulated gate device at low frequency operation [47], [48]. The noise due to the insulator semiconductor interface is also important for GaAs MESFETs because there is a thin insulating film on the surface of the GaAs which excludes the area of the gate electrode [49].

The noise figures of the insulated gate FETs and MESFETs have been compared and it has been noted that these devices have almost identical noise figures at microwave frequencies [50]. One can therefore conclude that the noise due to the insulator-semiconductor interface is negligible at microwave frequencies. In the following sections, then, noise sources of SIT and GFC-BARITT devices will be analyzed at high frequencies.

3.8.2 Noise in Punch-Through Diodes. The modeling of a device (SIT or GFC-BARITT) is done by dividing the device into N-numbers of segments. Each segment is a BARITT diode. This approach will be assumed for noise analysis also. There are a number of studies on the noise analysis of the BARITT diodes [11], [42] through [44], which can be applied to the Ith segment of a SIT or a GFC-BARITT device. In this study, Statz's [43] analysis will be followed and applied to a SIT or a GFC-BARITT device.

The total mean-square open-circuit noise voltage, including the shot noise in the injection region and the diffusion noise in the drift-diffusion region of a BARITT diode has been derived [43] and given in Eq. (3.107):

$$|\bar{v}_n^2| = \frac{4qv_{sat}J_o\Delta f}{\omega^2 A}\left[\frac{1-\cos\theta}{\alpha^2+\omega^2\varepsilon_s^2} + \frac{2D_nL_{DS}}{\varepsilon_s^2 v_{sat}^3}\left(1-\frac{\sin\theta}{\theta}\right)\right], \qquad (3.107)$$

where $\omega = 2\pi f$,

f = the frequency,

Δf = the frequency bandwidth,

$J_o = qv_{sat}n_p$, the current density,

A = the cross-sectional area of a BARITT diode,

$\alpha(I)$ = the barrier modulation parameter,

$\alpha(I) = \sqrt{(2\varepsilon_s)/kTN_D \ln(J_{so}/J_o)}\ J_o$,

J_{so} = the maximum current density of a BARITT diode and

θ = the phase angle.

3.8.3 Noise Sources of the Three-Terminal Punch-Through Devices. Equation (3.107) is modified to express the open-circuit noise voltage between the drain and the source terminals of the Ith segment of a SIT or a GFC-BARITT device.

$$|\bar{V}ds_n^2| = \frac{4qv_{sat}\, fJ_{DS}(I)}{ZW_S/N\, \omega^2}\left[\frac{1-\cos\theta}{\alpha(I)^2+\omega^2\varepsilon_s^2} + \frac{2D_nL_{DS}}{\varepsilon_s^2 v_{sat}^3}\left(1-\frac{\sin\theta}{\theta}\right)\right], \quad (3.108)$$

where

$$\alpha(I) = \sqrt{\frac{2\varepsilon_s}{k_BTN_D}\ln\left(\frac{J_{DSo}}{J_{DS}(I)}\right)J_{DS}(I)}$$

and

$$J_{DSo} \cong qv_{sat}\frac{V_{DS}}{(V_{DS}+E_{sat}\cdot L_{DS})}N_D\, e^{(V_B/V_T)},$$

where V_B = the built-in potential of the source channel juntion,

ZW_S/N = the cross-sectional area of the Ith BARITT diode,

L_{DS} = the length of the channel .

Since the noise voltage of the Ith segment of the device is known from Eq. (3.108), the noise voltage of the whole device can be calculated. To derive an expression for the noise figure, the short-circuit noise currents of the three-terminal device must be known. The short-circuit drain-source noise current is obtained from Eq. (3.108) as:

$$|\overline{i^2_{ds_n}}| = \sum_{I=1}^{N} |\overline{g^2_{ds}(I)}| \; |\overline{V^2_{ds_n}}| \;, \tag{3.109}$$

where $g_{ds}(I)$ = the small signal conductance of the Ith segment. By inserting Eq. (3.108) into Eq. (3.109), then the mean square short-circuit noise current can be explicitly expresses as in Eq. (3.110):

$$|\overline{i^2_{ds_n}}| = \sum_{I=1}^{N} g^2_{ds}(I) \left\{ \frac{4qv_{sat}\Delta f J_{ds}(I)}{\omega^2 Z W_S/N} \left[\frac{1 - \cos\theta}{\alpha(I)^2 + \omega^2 \varepsilon_s^2} + \frac{2D_n L_{DS}}{\varepsilon_s^2 v_{sat}^3}\left(1 - \frac{\sin\theta}{\theta}\right)\right]\right\} \;. \tag{3.110}$$

To find an expression for the gate noise current, i_{g_n}, only the portion of voltage variation along the channel will be coupled through the gate capacitance, C_{gs}, because the gate electrode of a SIT or a GFC-BARITT device, L_G is normally much shorter than the channel length, L_{DS}. To be specific, the entire shot noise will be coupled through the gate-source capacitance; however, only the (L_G/L_{DS}) fraction of diffusion noise will be coupled. In Eq. (3.108) the first term is due to shot noise and the second one is due to the diffusion noise. Following Van der Ziel's approach [46], the gate charge due to the coupling of the noise voltage of the channel is:

$$q_{gs_n} = C_{gs} V'_{ds_n}(I) \tag{3.111}$$

or

$$|q^2_{gs}| = C^2_{gs} \, |V'^2_{ds_n}(I)| \quad , \tag{3.112}$$

where V'_{ds_n} implies that some portion of the V_{ds_n} is coupled through the gate capacitance. It is defined as

$$V'_{ds}(I) = \left(\frac{L_G}{L_{DS}}\right) V_{ds_{diff}} + V_{ds_{shot}} \quad . \tag{3.113}$$

V'_{ds} is given explicitly in Eq. (3.114) below:

$$|V'^2_{ds_n}(I)| = \frac{4qv_{sat}\Delta f}{\omega^2 ZW_S/N} \, J_{DS}(I) \left[\frac{1 - \cos\theta}{\alpha(I)^2 + \omega^2 \varepsilon^2_S} + \left(\frac{L^2_G}{L^2_{DS}}\right) \cdot \frac{2D_n L_{DS}}{\varepsilon^2_S v^3_{sat}} \left(1 - \frac{\sin\theta}{\theta}\right) \right] \quad . \tag{3.114}$$

The gate current is assumed to be

$$i_{gs_n} = j\omega q_{gs} \quad . \tag{3.115}$$

The mean square gate noise current then becomes

$$|\overline{i^2_{gs_n}}| = \sum_{I=1}^{N} \omega^2 C^2_{gs} \, |\overline{V'^2_{ds_n}(I)}| \quad , \tag{3.116}$$

where $|\overline{V'^2_{ds_n}(I)}|$ is given in Eq. (3.114). Finally, by inserting Eq. (3.114) into Eq. (3.116), the mean square gate noise current expression becomes

$$|\overline{i^2_{gs_n}}| = \sum_{I=1}^{N} \omega^2 C_{gs}^2 \left\{ \frac{4qv_{sat}\Delta f}{\omega^2 Z\, W_S/N} \quad J_{DS}(I) \left[\frac{1 - \cos\theta}{\alpha(I)^2 + \omega^2 \varepsilon_s^2} + \frac{L_G^2}{L_{DS}} \frac{2D_n}{\varepsilon_s^2 v_{sat}^3} \left(1 - \frac{\sin\theta}{\theta}\right)\right]\right\}. \quad (3.117)$$

3.8.4 <u>The Noise Figure and the Noise Measure</u>. The noise figure of the device can be derived from an equivalent circuit of a SIT or a GFC-BARITT device as shown in Fig. 3.2.

In Fig. 3.2 it is assumed that a SIT or a GFC-BARITT device can be represented with a noiseless intrinsic small signal model with two noise sources, i_{gs_n} and i_{ds_n}. Other noise sources which are neglected, are:

(i) the noise due to the interface of the gate and the channel [47], [48], [51] and

(ii) the generation-recombination noise which could arise from both bulk and surface effects [25], [52] through [55].

The noise figure, F, and the noise measure, M, are defined in Eq. (3.118) and Eq. (3.119), respectively. F can be defined as

$$F = \frac{\text{the total available output noise power}}{\text{the portion of the noise power at the output due to the source alone}} . \quad (3.118)$$

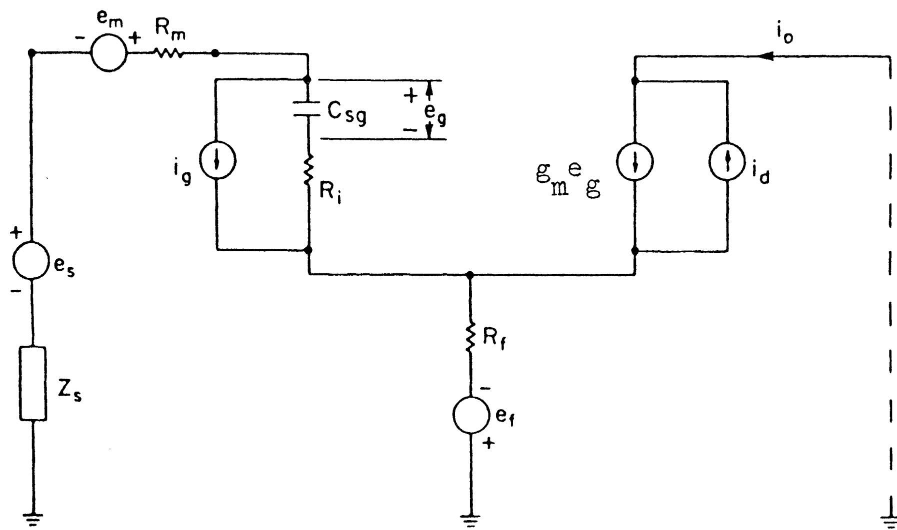


Fig. 3.2 Equivalent circuit used in noise analysis.

The noise figure as a figure of merit is not by itself a sufficient guide for the selection of an amplifying device. A low noise amplifier may also have a low gain and can thus defer the noise problem to a subsequent amplifier stage. Not accounting for the network gain is a shortcoming of the noise figure definition. This is overcome by introducing the M, which is defined by Haus [51] and given in Eq. (3.119) as

$$M = \frac{F - 1}{1 - 1/\text{gain}} . \qquad (3.119)$$

The F expression for the common-source biasing conditions is given [26] for the equivalent circuit shown in Fig. 3.2:

$$F = 1 + \frac{1}{R_s}\left\{R_m + R_f + |Z_t| \frac{|\overline{i^2_{gs_n}}|}{TW} + \frac{|ZI|^2}{TW} |\overline{i^2_{ds_n}}| - 2\,\text{Re}\left[Z_t \frac{ZI^*}{TW} C_r \left(|\overline{i^2_{gs_n}}|\,|\overline{i^2_{ds_n}}|\right)^{1/2}\right]\right\} , \qquad (3.120)$$

where $TW \triangleq 4kT_0\Delta f$,

$ZI \triangleq (1 + y_{11} Z_t)/y_{21}$,

$Z_t = Z_s + R_m + R_f$,

Z_s = the impedance of the noise source,

R_m = thermal noise of the gate parasitic resistance,

R_f = the thermal noise of the source parasitic resistance and

Re = the "real part".

C_r is the correlation factor and is defined as:

$$C_r = \frac{\overline{i^*_{gs_n} \, i_{ds_n}}}{\sqrt{\overline{|i^2_{gs_n}|} \; \overline{|i^2_{ds_n}|}}}$$

and R_s = the input resistance which can be chosen from Eq. (3.120) in such a manner as to optimize the noise figure. The correlation coefficient C_r is obtained by assuming:

$$\text{(i)} \quad i_{gs_n} = \sum_{I=1}^{N} j\omega C_{gs} \, |\overline{V'^2_{ds_n}}|^{1/2} \tag{3.121}$$

and

$$\text{(ii)} \quad i_{ds_n} = \sum_{I=1}^{N} g_{ds}(I) \, |\overline{V^2_{ds_n}}|^{1/2} \; . \tag{3.122}$$

The small signal conductance $g_{ds}(I)$ is a complex parameter, because of the transit effect on the drifting carriers along the channel. Under these assumptions, an expression for the correlation coefficient is obtained and given in Eq. (3.123)

$$C_r = -j \sum_{I=1}^{N} \frac{g_{ds}(I)}{|g_{ds}(I)|}. \tag{3.123}$$

<u>3.8.5 The Noise Temperatures</u>. The importance of the noise temperature of the carriers in the channel has been emphasized in [56]. The carrier temperature at high field is not equal to the lattice temperature of the semiconductor. The increase in the

carrier temperature increases the noise contribution of the carriers in the drift region. The empirical expressions of the electron temperature as a function of the electric field have been given for silicon [57] and for gallium arsenide (GaAs) [58]. These expressions are given in Eq. (3.124) for silicon and in Eq. (3.125) for GaAs. One has to be cautious in using these equations as the general theoretical expressions, because these are semi-empirical expressions.

For silicon:

$$T_n \cong T_o[0.5(1 + \sqrt{1 + 4(E/E_{sat})^2}) + (E/E_{sat})^2] \qquad (3.124)$$

and for GaAs

$$T_n \cong T_o[1 + 6(E/E_{sat})^3] \quad , \qquad (3.125)$$

where T_o = the room temperature.

The carrier temperature expressions are electric field dependent, and in a detailed noise analysis, therefore one has to include the carrier temperature expressions into the channel noise expression. However, in this study an average carrier temperature value will be used for simplicity. Despite the fact that:

(i) the above expressions are not general and are only semi-empirical, and

(ii) the use of an average temperature will introduce an error into the carrier temperature value itself, one would however

expect improvement for the calculations of the intrinsic noise sources with the field dependent carrier temperature over the constant carrier temperature case.

Assuming an average field $E = (V_{DS}/L_{DS})$, Eq. (3.124) and Eq. (3.125) finally become:

For silicon:

$$T_n \cong T_o \left[0.51 + \sqrt{1 + 4\left(\frac{V_{DS}}{L_{DS}} \frac{1}{E_{sat}}\right)^2} + \left(\frac{V_{DS}}{L_{DS}} \frac{1}{E_{sat}}\right)^2 \right] \quad (3.126)$$

and for GaAs:

$$T_n \cong T_o \left[1 + 6\left(\frac{V_{DS}}{L_{DS}} \frac{1}{E_{sat}}\right)^2 \right] . \quad (3.127)$$

CHAPTER IV. DEVICE SIMULATION PROGRAM (SIM-GFC)

4.1 Introduction

SIM-GFC is a program which has been developed to solve the device expressions given in Chapters II and III. It can simulate a GFC-BARITT device, SIT and a vertical FET (which is treated as a special case of a SIT device). SIM-GFC consists mainly of subroutines which are the solutions to the various analytical expressions developed earlier for the various devices. Even though it includes some numerical solutions it is an inexpensive program.

SIM-GFC has four levels: (i) $V_F(I)$ is approximated for each segment directly for each gate- and the drain-source voltage in Level 1. This is the fastest and simplest level. (ii) Analytical expressions of the two-dimensional potential distribution are solved point-by-point to find $V_F(I)$ in Level 2. (iii) Level 3 includes the numerical solution of the two-dimensional Poisson's equation. A Fourier Analysis and Cyclic Reduction (FACR) algorithm is used, because it is the fastest algorithm to solve the two-dimensional Poisson's equation [16]. The effect of the space charge is neglected. (iv) Level 4 calculates the small and large signal parameters from the given dc current-voltage data. This level is useful for simulation of the performance of the SIT and GFC-BARITT devices. In all the device expressions, the forward bias voltage of the source-channel junction is the most critical parameter and the most difficult to

obtain analytically. Therefore, if experimental data is used to obtain the forward bias voltage, accuracy of the small and large signal device parameters will be improved.

In each level, SIM-GFC evaluates the dc, small signal, and large signal device parameters, and then calculates the maximum available gain, maximum frequency of operation, power output, collector efficiency, the noise figure and noise measure of the chosen device (a SIT or a GFC-BARITT device). The program handles three different types of semiconductor materials: silicon, GaAs, and InP. The details of the SIM-GFC program will be given in Section 4.2. The material parameters as a function of the doping concentration and temperature are given in Section 4.2. The results of the simualtion of the various device characteristics are presented in Section 4.3 through Section 4.7 and a comparison of the various TTPT devices is given in Section 4.8.

4.2 Program Description

SIM-GFC is written to solve and evaluate all the device expressions which were derived in Chapters II and III. Some of those expressions are in analytical form and some are in numerical form. It consists of many function subroutines which make it easy to expand the program. The program has four levels. To increase the efficiency of programming, most of the subroutines are used in all four levels.

Levels 1,2 and 3 have the same functions as far as device simulation is concerned. The only difference is that, in Level 1,

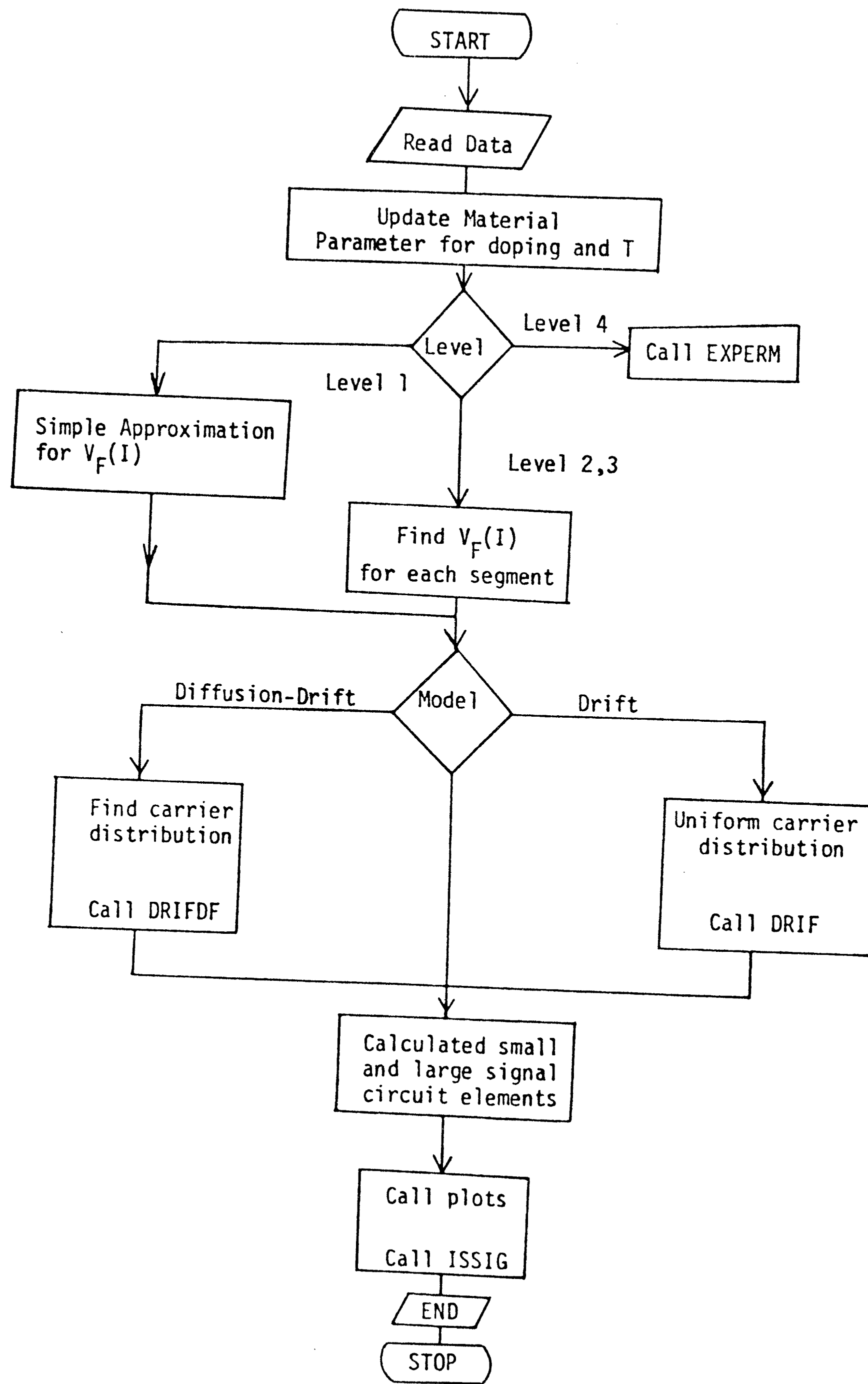
a simple analytical expression for the forward bias voltage, $V_F(I)$, is used and the effect of the space charge is neglected. In Level 2, the two-dimensional potential distribution expression is solved for point-by-point to find $V_F(I)$ at each x and y point. In Level 3, to obtain $V_F(I)$ a numerical two-dimensional Poisson's equation solver; POT1 subroutine [16] is used. In Level 4, a practical case is considered; the device parameters are indirectly calculated from the experimentally measured dc current-voltage values and V_F voltages are obtained from the known dc values. The small and large signal parameters are then obtained from the calculated V_F values.

The flow chart of the SIM-GFC program is shown in Fig. 4.1. A summary of the functions of the SIM-GFC program is given in Appendix B.

4.3 Material Parameters

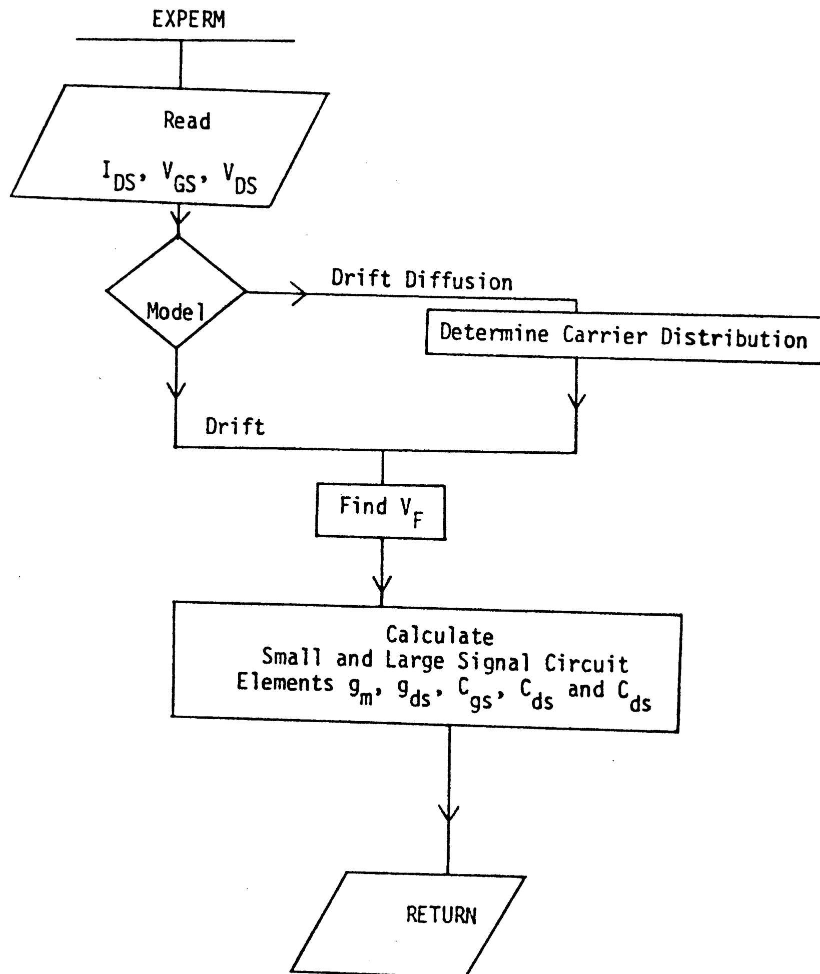
In order to simulate devices under different operating conditions, such as different impurity concentrations and temperatures, the expressions for the material properties must include the effects of those parameters. In the SIM-GFC program, the intrinsic carrier density, the energy band gap, the mobility expression, saturation velocity and the breakdown field expressions are updated for different temperatures and impurity concentrations. Some of these expressions are semi-empirical.

The material parameters as a function of temperature are as follows:



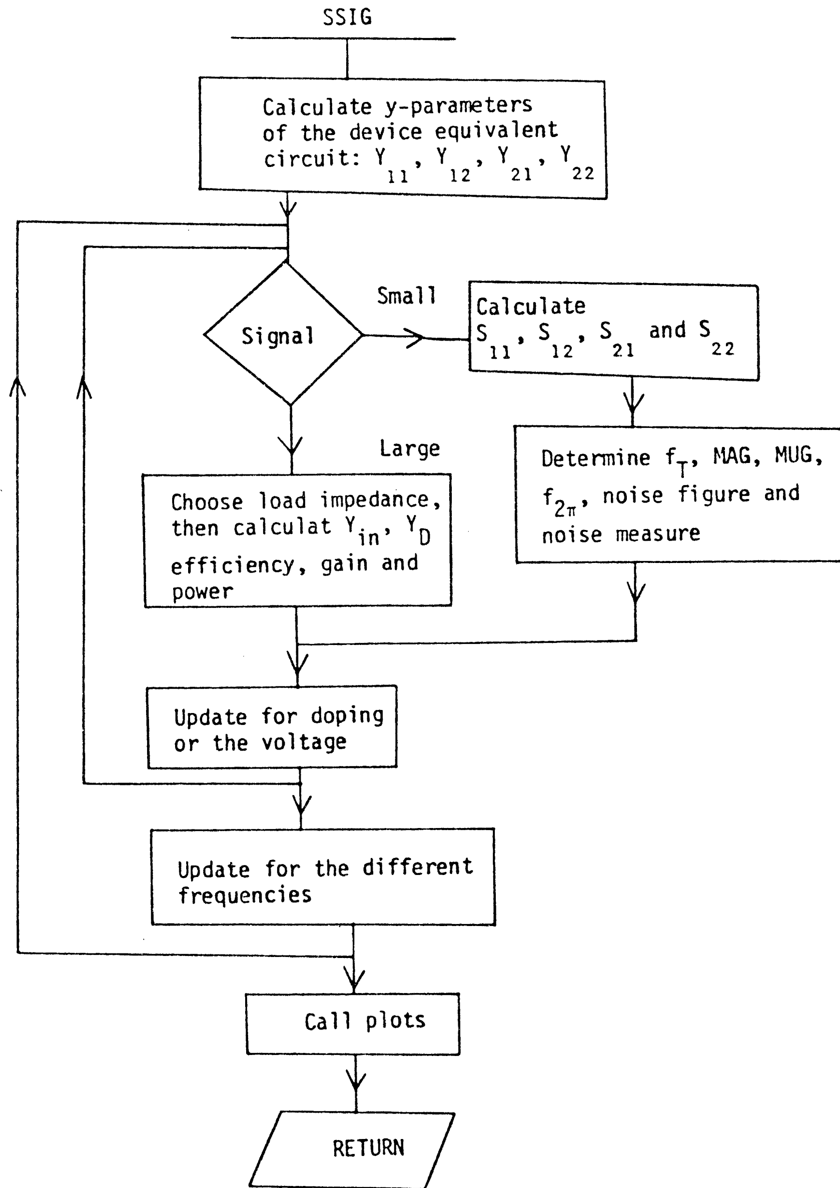
(a) Main program of SIM-GFC.

Fig. 4.1 Flow Chart.



(b) EXPERM subroutine.

Fig. 4.1 Flow Chart.



(c) SSIG subroutine.

Fig. 4.1 Flow Chart.

(A) Energy band gap: A semi-empirical expression is given in Eq. (4.1) for silicon, in Eq. (4.2) for GaAs and in Eq. (4.3) for InP [59].

For silicon

$$E_G(T) = 1.16 - 7.02 \times 10^{-4} \times T^2/(T + 1108). \qquad (4.1)$$

For GaAs

$$E_G(T) = 1.52 - 5.8 \times 10^{-4} \times T^2/(T + 300) \quad . \qquad (4.2)$$

For InP

$$E_G(T) = 1.42 - 5.8 \times 10^{-4} T^2/(T + 300) \quad . \qquad (4.3)$$

(B) Intrinsic Carrier Density: The temperature variation of the intrinsic carrier density expressions for Si, GaAs and InP is the same [30]. Only the values of the expressions for different materials are different.

For silicon

$$n_i(T) = 1.328 \cdot 10^{-3} \cdot T^{1.5} e^{-E_G(T)/2kT} \quad . \qquad (4.4)$$

For GaAs

$$n_i(T) = 2.82 \cdot 10^{-3} \cdot T^{1.5} e^{-E_G(T)/2kT} \quad . \qquad (4.5)$$

For InP

$$n_i(T) = 7.808 \cdot 10^{-4} \cdot T^{1.5} e^{-E_G(T)/2kT} . \qquad (4.6)$$

(C) Saturation Velocity and Mobility: The temperature dependent mobility and velocity expressions are empirical [59]. Primarily the mobility of the carriers has a very complex expression and is semi-empirical. This is because the quality of the crystal, density of the defects and the amount and type of contamination are different for different growth systems. The semi-empirical expressions of the saturation velocity and the mobility as a function of temperature are given below.

For silicon: The saturation velocity expression is given in Eq. (4.7):

$$v_{sat} = 2.4 \times 10^7/[1 + 0.8 \exp (T/600°K)] . \qquad (4.7)$$

The mobility expression for electrons is given in Eq. (4.8):

$$\mu_n(T) = 2.4\mu_n(T = 300°K)/(1 + 0.8 \exp(T/600°K)) . \qquad (4.8)$$

For GaAs: The saturation velocity expression is

$$v_{sat}(T) = v_{sat}(T = 300°K) \quad (T/300°K)^{-1} . \qquad (4.9)$$

The mobility expression is

$$\mu_n(T) = \mu_n(T = 300°K) \cdot (T/300°K)^{-1} . \quad (4.10)$$

For InP: The saturation velocity and the mobility expressions are given in Eq. (4.11) and Eq. (4.12), respectively:

$$v_{sat}(T) = v_{sat}(T = 300°K) \cdot (T/300°K)^{-1} \quad (4.11)$$

and

$$\mu_n(T) = \mu_n(T = 300°K) \cdot (T/300°K)^{-1} , \quad (4.12)$$

where $v_{sat}(T = 300°K)$ and $\mu_n(T = 300°K)$ are the room temperature values of the velocity and the mobility respectively.

The material parameters as a function of impurity concentration are:

(A) Mobility: An empirical expression is given for Si, GaAs, and InP in Eq. (4.13). It has been reported that this expression can accurately predict the mobility as a function of the impurity concentration [60].

$$\mu_n(N_D) = \mu_n(10^{16})/[1 + \sqrt{(N_D/10^{17})}] , \quad (4.13)$$

where $\mu_n(10^{16})$ means the mobility of the semiconductor with carrier concentration of $10^{16} cm^{-3}$.

(B) Breakdown Field: The breakdown electric field is obtained from the avalanche breakdown voltage expression given in [30]. The breakdown field expression is given by Eq. (4.14) which is valid for any semiconductor:

$$BE_F = 15.492 \left(\frac{E_G}{1.12}\right)^{3/4} \left(\frac{10^{16}}{N_D}\right)^{3/8} \left(\frac{qN_D}{2\varepsilon_s}\right)^{1/2} . \qquad (4.14)$$

Equation (4.14) includes the temperature effect on the breakdown field through the temperature variation of the energy band gap E_G.

4.4 Device Physics

The physics of the various devices has been investigated through a study of the potential distribution, the carrier injection and the effect of the space charge. In the following sections each subject has been analyzed in detail. The various devices considered throughout this chapter are listed in Table 4.1. The various dimensions are shown in the associated illustration.

4.4.1 The Potential Distribution. The potential distribution inside the device (a TTPT device) is calculated by the solution of the two-dimensional Poisson's equation in Level 3. The potential minimum in the vicinity of the source electrode is nonuniform across the device thickness as shown in Fig. 4.2. The effect of the gate voltage and its polarity on the potential minimum, V_F, is shown in Fig. 4.2(a)-(b). The two-dimensional Poisson's equation is solved numerically by using this fast Poisson's equation solver, POT1.

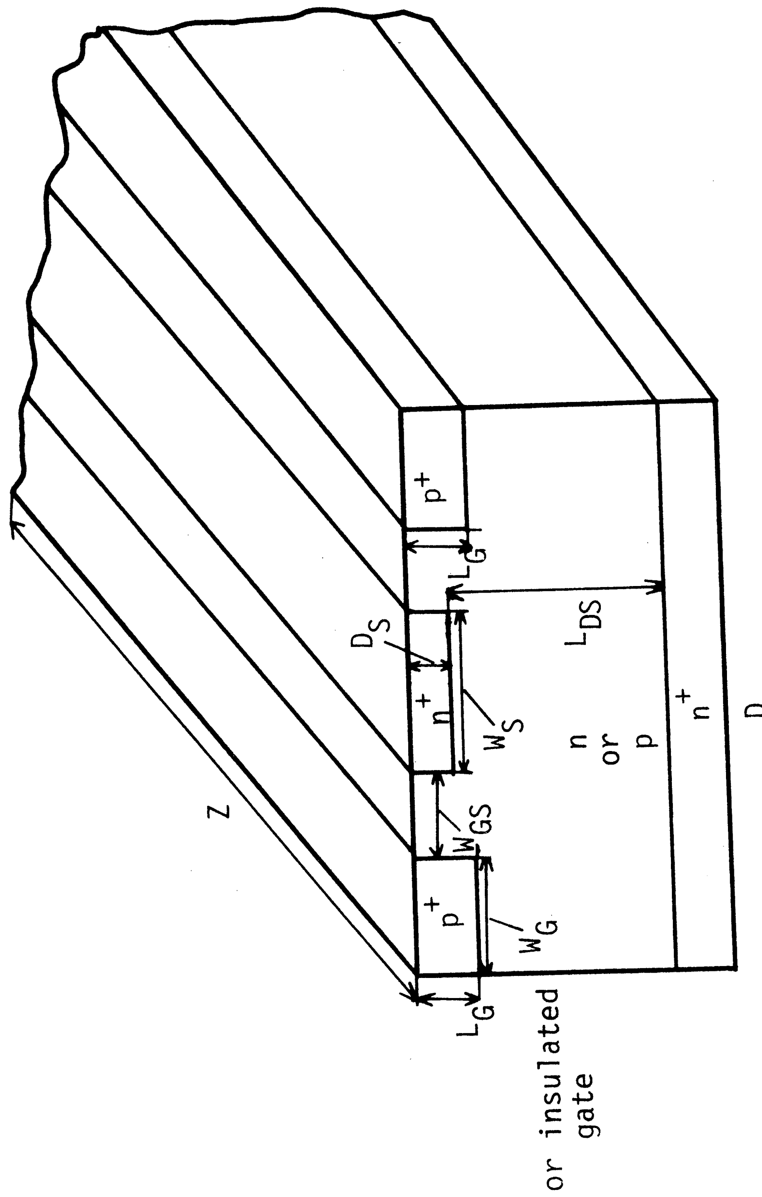
There is, however, a limitation on the polarity of the gate voltage for the junction-gate and the ohmic-gate type devices. The

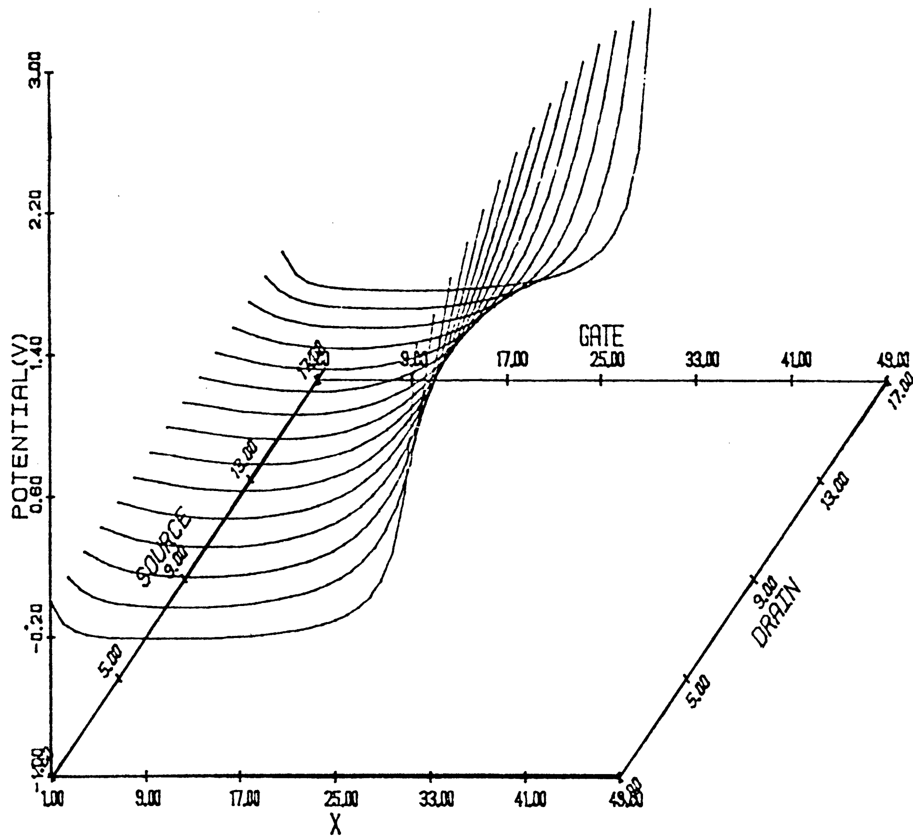
Table 4.1

List of the Devices

Symbol	Device	N_D (cm^{-3})	Z (cm)	L_{DS} (μm)	L_G (μm)	W_{GS} (μm)	W_S (μm)	W_G (μm)	D_s (μm)	T_{ox} (μm)	Type of Device	Material
S1	SIT	10^{15}	13.92	5	2	1.3	3	4	0.6	--	vertical	Si
B1	GFC-B	10^{14}	13.92	20	2	2.3	3	--	--	0.1	vertical	Si
S2	SIT	10^{14}	13.92	20	2	2.3	3	0	0.6	--	vertical	Si
B2	GFC-B	10^{15}	13.92	5	2	1.3	3	--	--	0.1	vertical	Si
B3	GFC-B	10^{15}	13.92	5	2	0.3	3	--	--	0.1	vertical	Si
S3	SIT	$5x10^{15}$	13.92	5	2	2.3	3	4	0.6	--	vertical	Si
S4	SIT	$5x10^{15}$	13.92	5	2	2.3	3	4	0.6	--	vertical	GaAs
S5	SIT	$5x10^{15}$	13.92	5	2	2.3	3	4	0.6	--	vertical	InP
B4	GFC-B	10^{14}	0.2085	20	10	0.5	0.5	--	--	0.1	lateral	Si
S6	SIT	$2x10^{15}$	0.187	12	2	4.0	4.0	--	--	--	vertical	GaAs
S7	SIT	$5x10^{16}$	13.92	5	2	0.2	1.0	4.0	0.6	--	vertical	GaAs
S8	SIT	10^{14}	13.92	20	2	0.1	0.5	4.0	0.6	--	vertical	Si

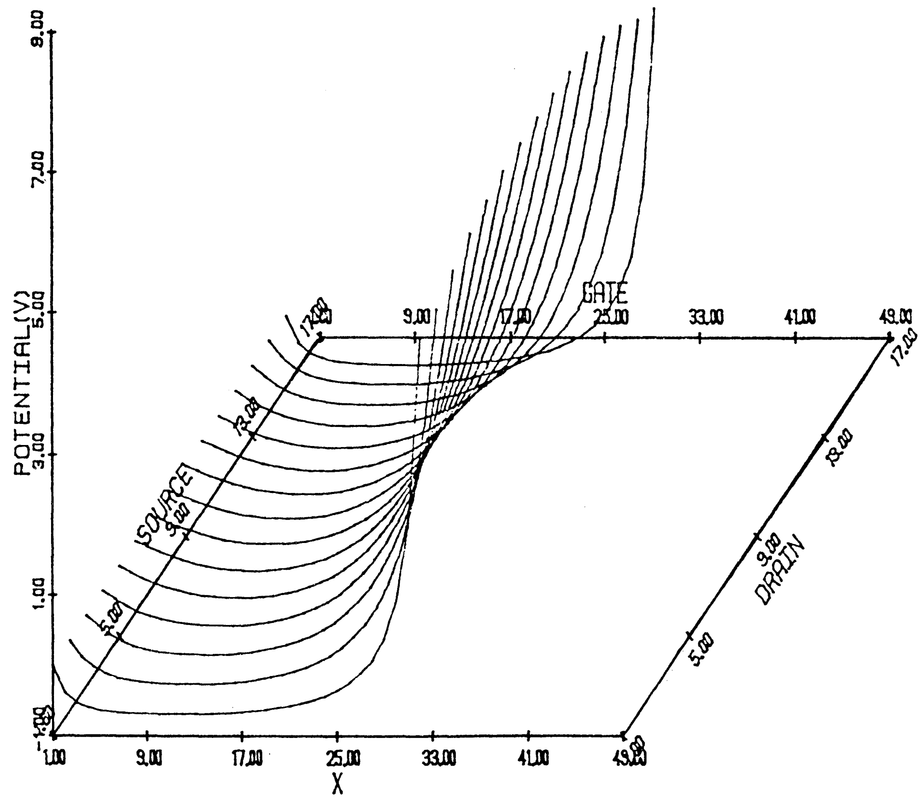
Table 4.1 (cont.)





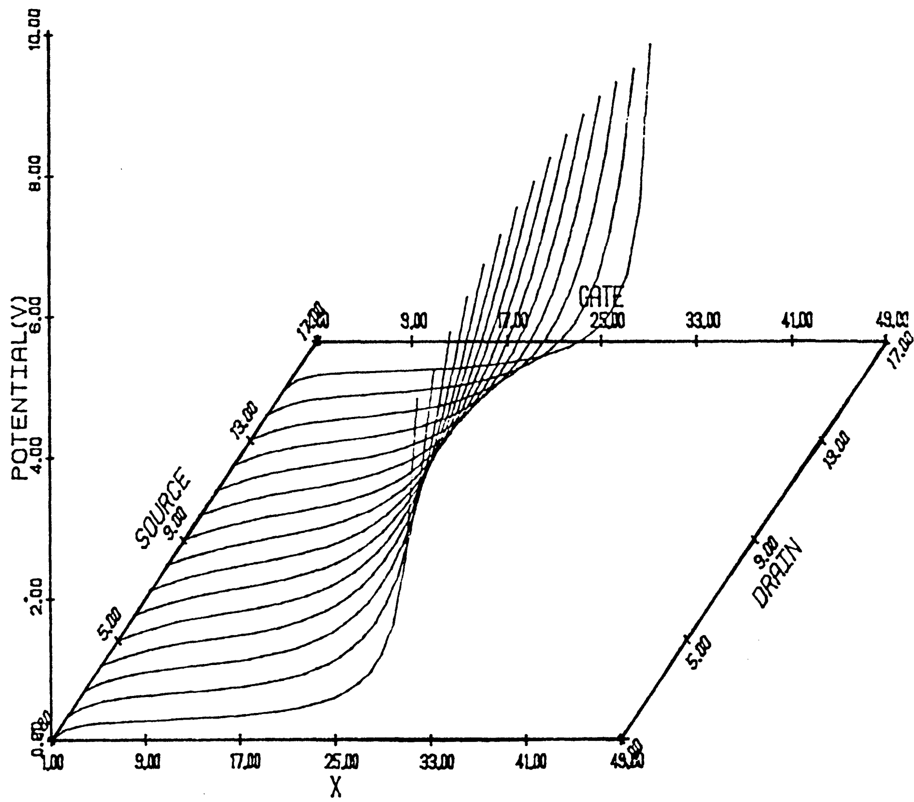
(a) Small negative gate voltage, V_{GS}.

Fig. 4.2 The Potential Distribution.



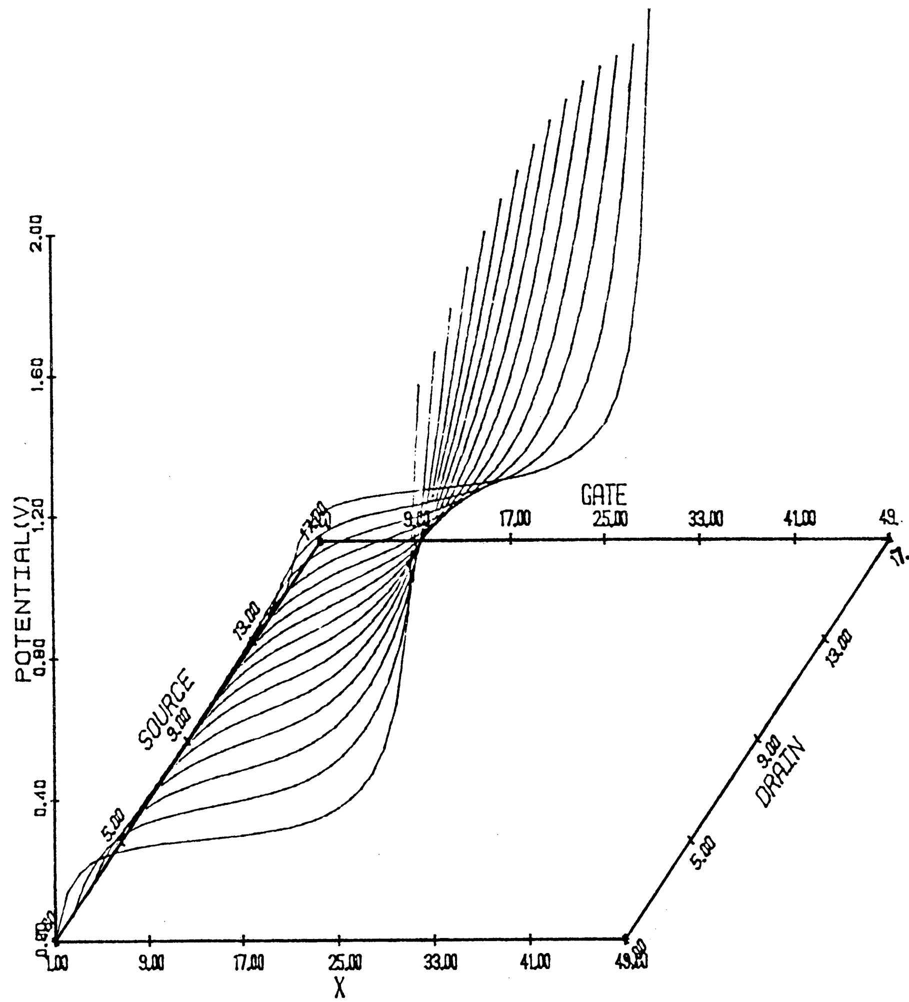
(b) Large negative V_{GS}.

Fig. 4.2 The Potential Distribution.



(c) Small positive V_{GS}.

Fig. 4.2: The Potential Distribution.



(d) Large positive V_{GS}.

Fig. 4.2: The Potential Distribution.

gate voltage should have a polarity which prevents a current flow through the gate in the case of the non-insulated gate devices. On the other hand, if the gate is insulated, the gate voltage can be used either to reduce or to increase the potential barrier at the vicinity of the source as illustrated in Fig. 4.2. In Fig. 4.2(b), the gate voltage increases the barrier height; Fig. 4.2(c)-(d) illustrate the barrier reduction effect of the gate voltage in the case of the insulated devices.

In the solution of the two-dimensional Poisson's equation, the effect of the injected carriers is neglected. That is why Fig. 4.2(c) and Fig. 4.2(d) show a negative barrier height indicating that the forward bias voltage is larger than the built-in potential V_B of the source-channel junction. This is physically impossible, because there is always an induced barrier height present due to the injected carriers which prevents the formation of a negative barrier height. Figure 4.2(c) and (d) indicate that it is possible to reduce the barrier height through an applied gate voltage, even under the punch-through condition. The non-uniformity of the barrier height across the device thickness is common to all cases: positive or negative applied gate voltages.

The potential distributions in Fig. 4.2 are given for the vertical double-gate devices. The effect of the gate voltage on the built-in potential becomes insignificant, if the gates are placed far from the source electrode. Another ineffective gate control structure is the one with a surface gate as shown in Fig. 4.3.

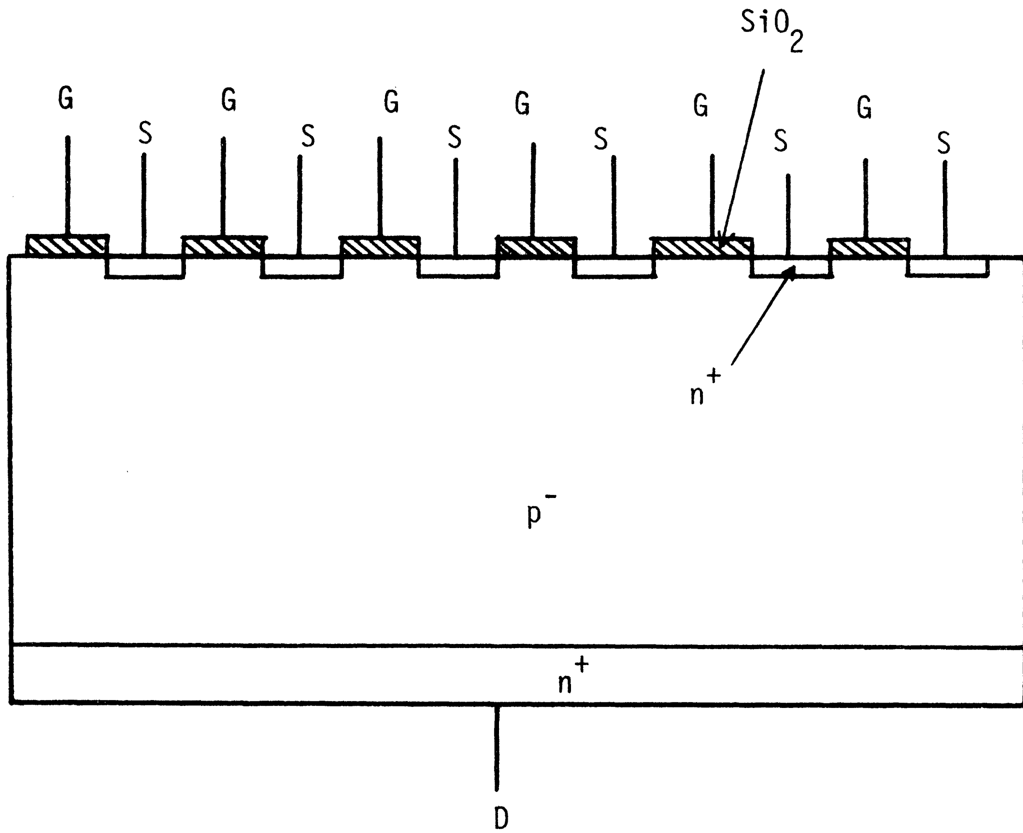


Fig. 4.3 A Multi-Channel Surface Gate (Insulator or Schottky) TTPT Device.

If a shallow n^+ source structure is used, such a structure may be used in power applications of the TTPT devices. To achieve a high blocking gain, a planar structure with a self-aligned gate-source must be used, such as the one shown in Fig. 1.1. Blocking gain, g_B, is defined as the ratio of V_{DS} and the gate voltage, V_{GS}, which turns off the device.

$$g_B \stackrel{\Delta}{=} \left.\frac{V_{DS}}{V_{GS}}\right|_{I_{DS}=o} .$$

4.4.2 The Injected Carrier Distribution. The carrier distribution in the punch-through devices has been assumed to be uniform [1], [3]. In BARITT diodes, McCleer [11] has shown the importance of the diffusion effect. In any type of injection device the carrier diffusion effect in the vicinity of the injecting junction limits the carrier transport. The diffusion effect is important even for majority carrier injection type devices such as SITs because of the carrier storage effect. The diffusion of the carriers becomes insignificant if the transport of the carriers is limited by the drift mechanism. This means that there is no barrier against the carrier inection (in the case of ohmic contacts), if the carrier transport is limited by the drift mechanism.

The effect of the diffusion varies for different semiconductors. This can be analyzed by considering the current continuity requirement. The diffusion current at the injection point is equal to the drift current beyond the carrier velocity saturation point. Then the current continuity requires that

$$qD_n \frac{n_{inj}}{L_{EF}} = qv_{sat}n_{sat} , \qquad (4.15)$$

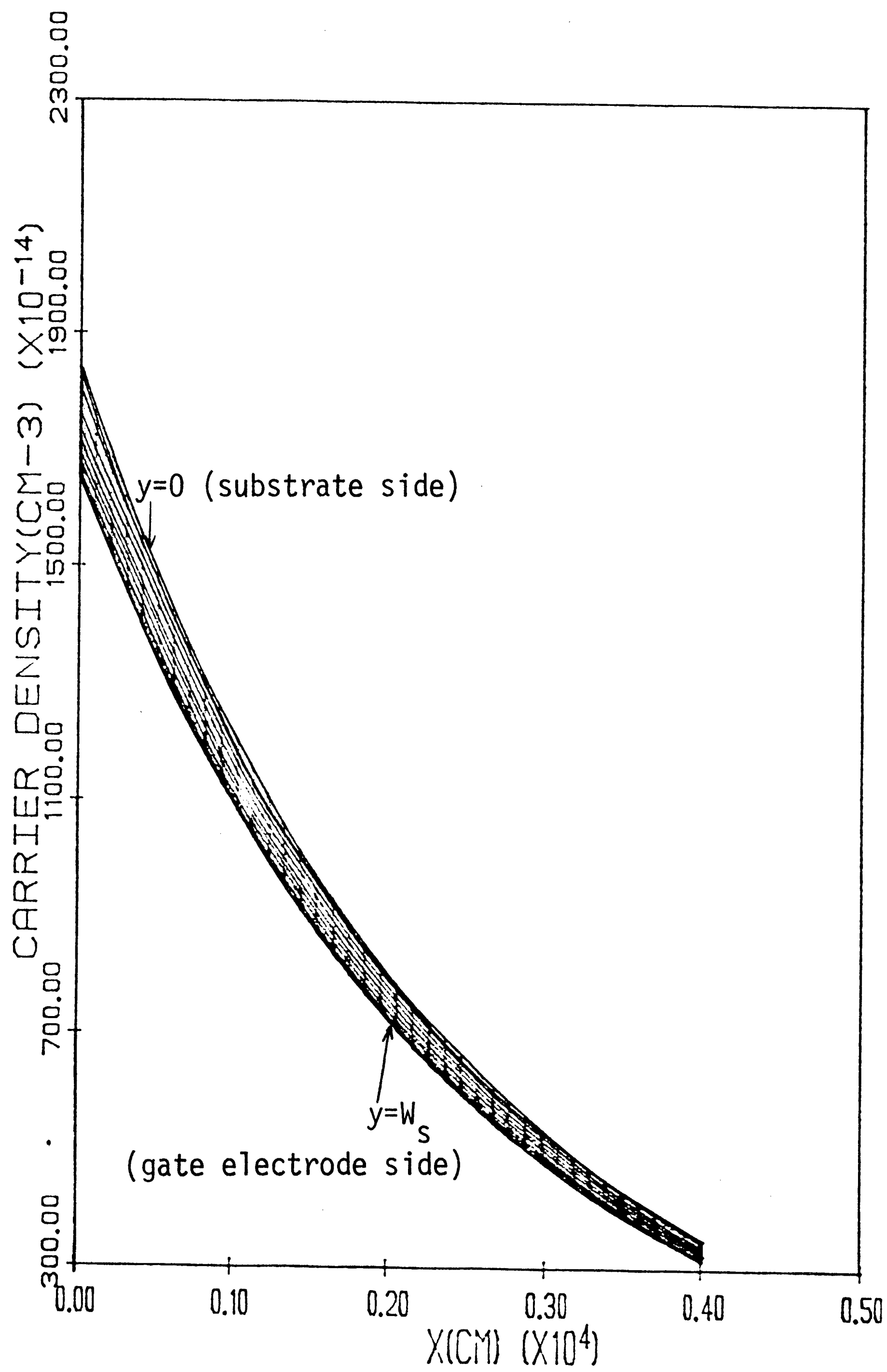
where L_{EF} is the effective diffusion length, n_{inj} is the density of the injected carriers at the injection point, n_{sat} is the density of the carriers beyond the velocity saturation point, and v_{sat} is the saturation velocity of the carriers.

After rearranging Eq. (4.15), n_{sat} can be obtained:

$$n_{sat} = n_{inj} \frac{(D_n/v_{sat})}{L_{EF}} \quad . \tag{4.16}$$

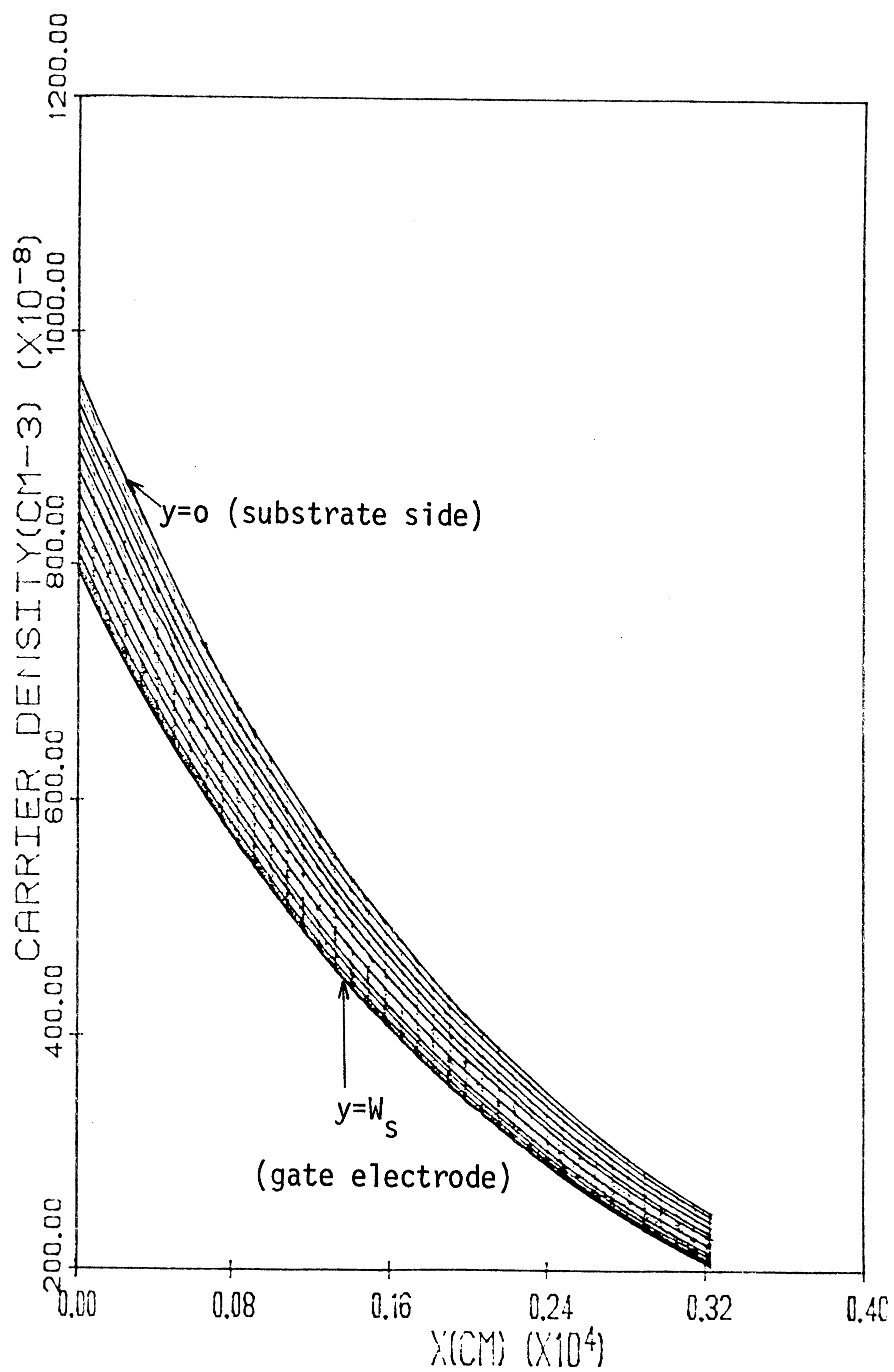
in Eq. (4.16), L_{EF} can only be larger than or equal to (D_n/v_{sat}). L_{ef} is determined by the field distribution in the device which can be assumed as material independent. From the analysis of Eq. (4.16), it can be conlcuded that in semiconductors with high diffusion coefficients (high low field mobility) and low saturation velocity, the drift is the limiting mechanism. Thus the drift approximation can be used to describe the current transport in high mobility semiconductor TTPT devices, such as GaAs and $In_{1-x}Ga_xAs/InP$. The diffusion is more important in low mobility semiconductors such as silicon. Therefore, the drift-diffusion approximation must be used to describe the current transport of silicon TTPT devices.

The carrier distribution for a Si device shown in Fig. 4.4(a), for an InP device in Fig. 4.4(b) and for a GaAs device in Fig. 4.4(c). All the devices are GFC-BARITT devices of the same size and for the same bias voltage. The analysis of the carrier distributions confirms the conclusions which resulted from consideration of Eq. (4.16). The n_{inj}/n_{sat} ratio for each device is different. It is highest for the silicon device and lowest for the GaAs device. This means that the carrier distribution in the Si device is highly nonuniform



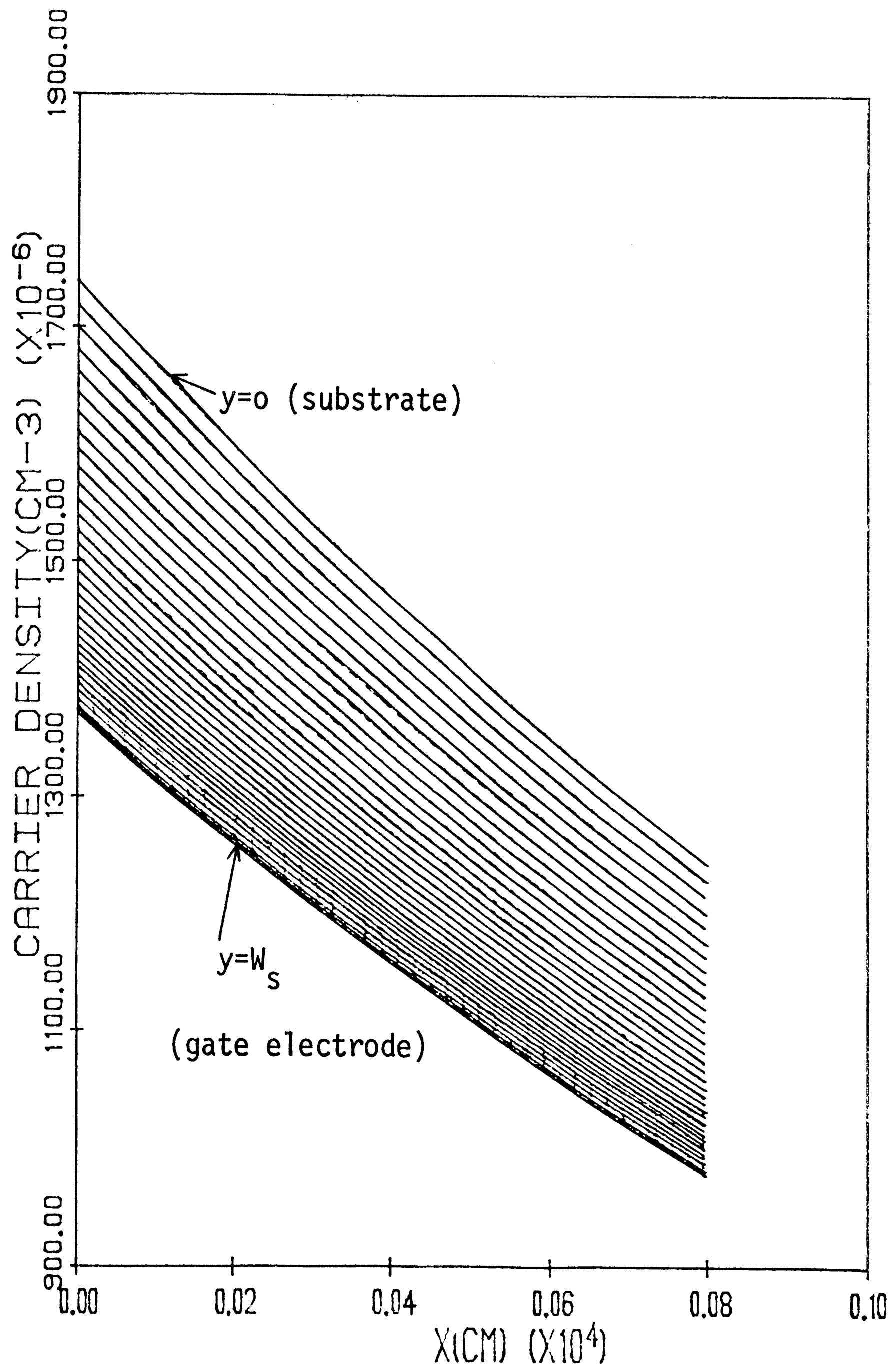
(a) Si device.

Fig. 4.4 Carrier Distribution as a Function of Distance at the Different Points Across the Channel, y and Distance Along the Conduction Path, X. The Reality Scales are 10^{14} for Carrier Density and 10^{-4} for x.



(b) InP device.

Fig. 4.4 Carrier Distribution as a Function of Distance at the Different Points Across the Channel, y and Distance Along the Conducting Path, x. The Real Scales Are 10^{14} for Carrier Density and 10^{-4} for x.



(c) GaAs device.

Fig. 4.4 Carrier Distribution as a Function of Distance at the Different Points Across the Channel, y and Distance Along the Conduction Path, x. The Real Scales are 10^6 for Carrier Density and 10^{-4} for x.

due to the diffusion effect. On the other hand, in the GaAs device, the carrier distribution is uniform beyond a very short low field region. The distance at which carrier velocity saturates, is shorter in the GaAs devices than the Si devices due to the low electric field requirement to saturate the velocity of the carriers. The InP device falls between the Si and the GaAs devices as would be expected.

The same results have been confirmed for the SIT devices. Therefore, the conclusions which are given for GFC-BARITT devices can be generalized for all the TTPT devices. One additional conclusion can be drawn from the analysis of Fig. 4.4. Besides the (n_{inj}/n_{sat}) ratios, the injection level is also different for each semiconductor device. Since all the devices have the same size and bias voltages, a comparison of the n_{inj} in Si, InP and GaAs devices is justified. The density of the injected carriers n_{inj} is lowest for the GaAs devices and highest for the Si devices. The reason for the different n_{inj} is the difference in the built-in potentials due to the different energy band gaps (E_G) of the semiconductor at y. GaAs has the highest built-in potential because it has the highest E_G (1.43 eV). The barrier height in the majority carrier injection type devices (SITs) is formed by the low and high carrier concentrations and the gate induced potential barrier. The carrier injection in SIT devices will not be affected by the energy band gap of the semiconductors. It is typically a minority carrier injection device property.

4.4.3 The Space-Charge Effect. The space-charge effect on the device characteristics has been investigated in Level 4 of the SIM-GFC program. It is an indirect approach to a complicated problem. Physically, the injected carriers will induce a barrier against the carrier injection. The "injected carrier induced-barrier" becomes significant when the density of the injected carriers is equal to or larger than the ionized impurity concentration of the channel. Therefore, it is expected that at high injection conditions, the rate of injection will slow down. This translates to a forward bias voltage (V_F) variation with respect to the drain-source Voltage, V_{DS}.

The forward bias voltage, V_F, must vary slowly with an increase in V_{DS} at high level injection condition. From the source current, I_{DS}, and voltage, V_{DS}, data in Level 4 of the SIM-GFC program the corresponding V_F value for each given I_{DS} and V_{DS} values has been determined and plotted. The V_F as a function of V_{DS} for a SIT reported in Reference [24] is shown in Fig. 4.5. Figure 4.5 illustrates the space-charge effect on the V_F variation as a function of V_{DS}. It is clear that the increase in V_F with V_{DS} slows down at high V_{DS} values or high current values. If the effect of the injected carriers is negligible, V_F must increase linearly with the increase in V_{DS}. This phenomenon has been observed in GFC-BARITT devices also.

It can be concluded that the injected carriers slow down the further injection. This effect manifests itself in the V_F variation as a function of V_{DS}. The effect of the injected carriers is

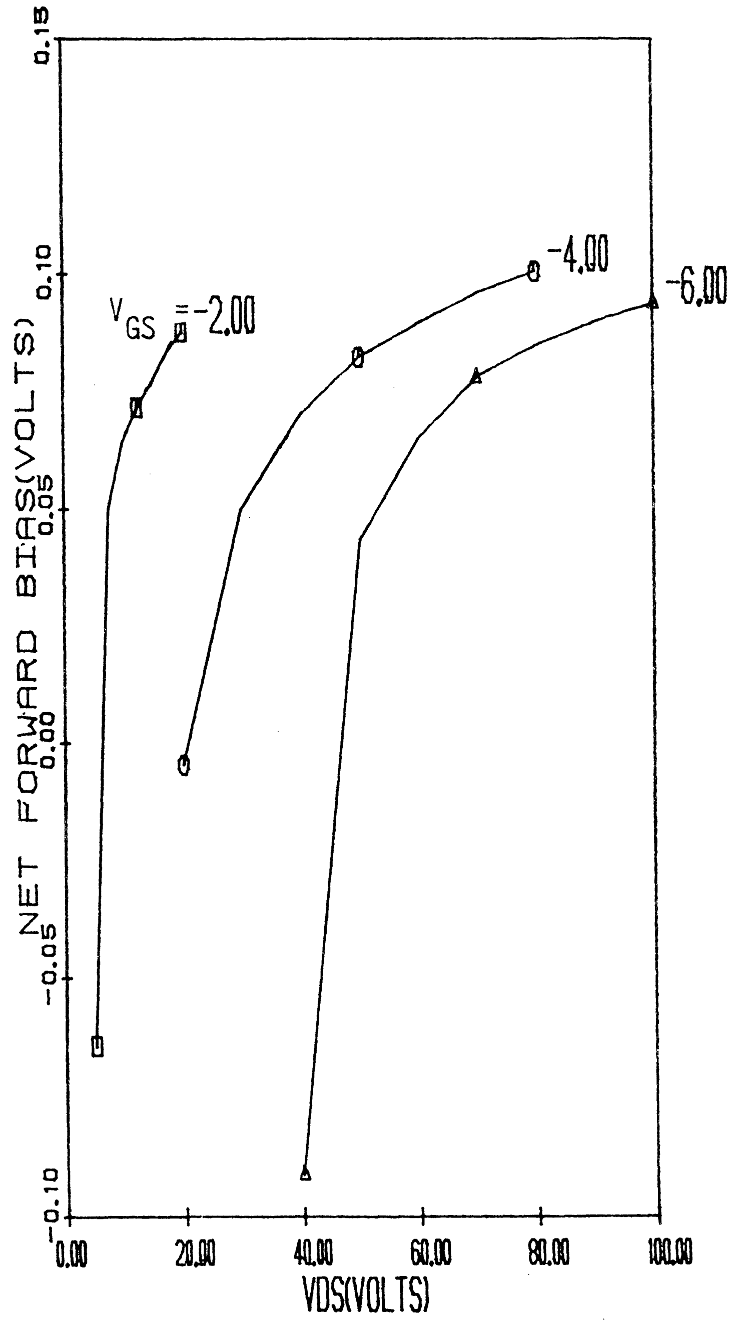


Fig. 4.5: V_F Variation as a Function of V_{DS} at Different Gate Voltages (Device S2).

strongly dependent on the distribution of these carriers. For instance, if the injected carriers are stored in the vicinity of the injection junction, the effect of the space-charge limitation (injected carrier effect on the injection) will become significant at relatively low injection levels. This means that the space charge limitation becomes effective at high current levels for semiconductors with high diffusion coefficients such as $Ga_xIn_{1-x}As$ GaAs and InP.

4.5 Dc Characteristics

In this section, the effects of the doping concentration, temperature and the device geometry on the device characteristics have been investigated. The same size SIT and GFC-BARITT devices have been studied to understand the similarities and the differences between these two devices.

4.5.1 The Impurity Concentration Effect. SIT and GFC-BARITT devices with the same size and biasing have been studied. The active region doping is increased with equal increments. For each substrate doping level, the dc I-V characteristics and small-signal device parameters have been calculated and the results are plotted as a function of the doping concentration.

The current plots for a SIT in Fig. 4.6 and for a GFC-BARITT device in Fig. 4.7 are shown. The gate voltage, V_{GS} was kept fixed, but V_{DS} was varied for each doping level. V_{DS} is composed of the punch-through voltage of the L_{DS} long channel, V_{PT}, and a fixed incremental voltage, ΔV_{DS}. V_{PT} varies with the doping concentration. However, ΔV_{DS} and the size are held constant.

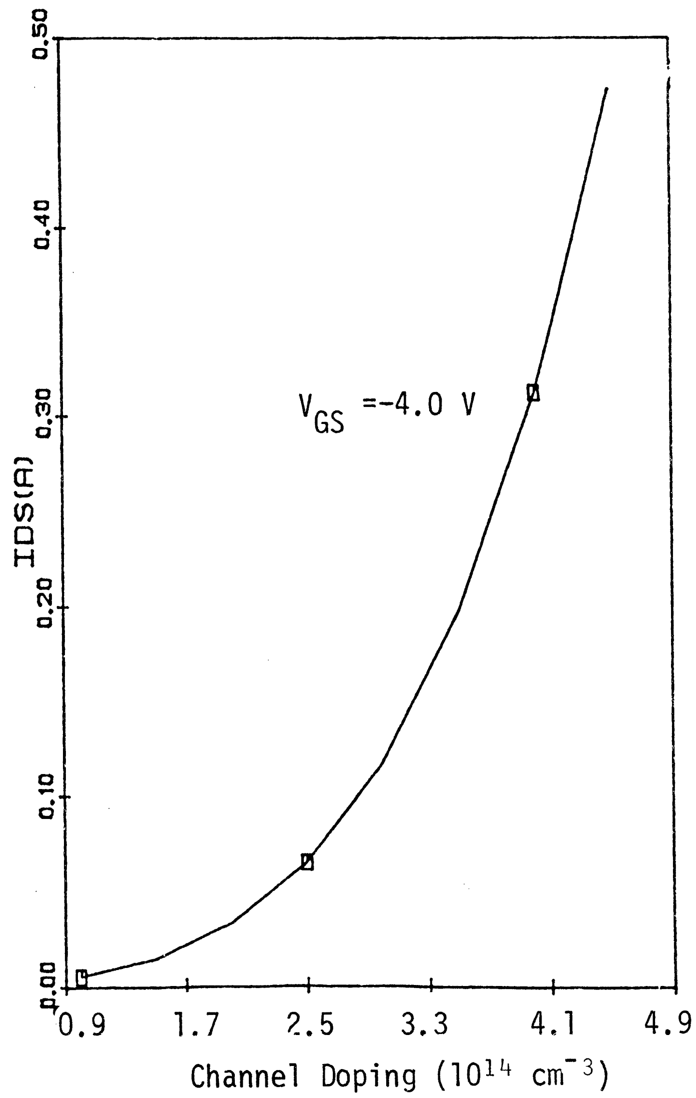


Fig. 4.6 Dc Current of a SIT as a Function of the Channel Doping Concentration (Device S2).

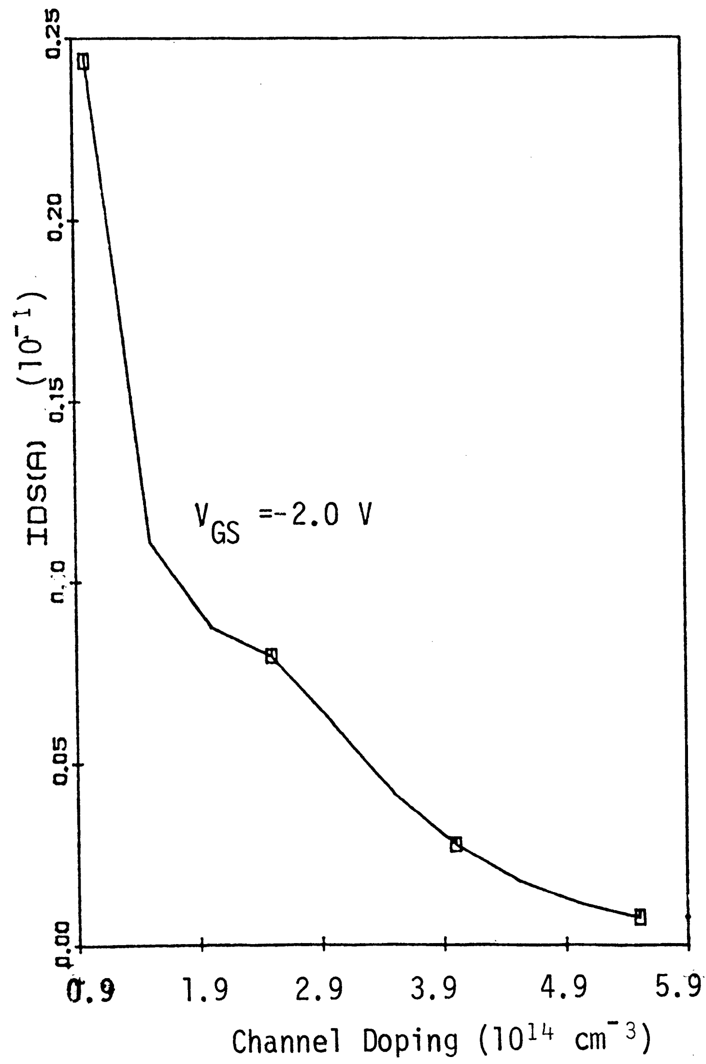


Fig. 4.7 Dc Current of a GFC-BARITT Device as a Function of the Channel Doping Concentration (Device B1).

The analysis of Fig. 4.6 indicates that the current, I_{DS} of a SIT increases with an increase in the doping concentration. The rate of increase in I_{DS} is not however, only due to the increase is the number of majority carriers in the channel. It is rather due to a combination of two factors: (a) direct increase in the density of the major carriers with the channel doping and (b) increase in V_{DS} due to V_{PT} increase. If the first effect were dominant, I_{DS} would increase linearly with the doping concentration. Figure 4.6 shows an exponential growth of I_{DS} with the doping. It is a typical current increase with the increase in V_{DS}. Therefore, the second effect, V_{DS} increase, is the main source of the current growth shown in Fig. 4.6.

The dc current of a GFC-BARITT device, on the other hand, decreases with an increase in the channel doping as seen in Fig. 4.7. Two main factors contributing to the current decay are: (as the reduction in forward bias voltage V_F and (b) the decrease in the number of the minority carriers in the channel, with the increasing doping concentration. Even though the drain source voltage V_{DS} increases with the increasing V_{PT}, the increase in the flat band voltage, V_{FB}, is much larger than the increase in V_{DS}. V_F is proportional to the $(V_{FB}/V_{DS})^2/4V_{FB}$. Therefore, an increase in V_{FB} will reduce V_F. The second contributor to minority carrier density, n_{po}, is

$$n_{po} = n_i^2/(\text{channel doping}) .$$

Since the intrinsic density, n_i, is fixed, an increase in the channel doping decreases n_{po} in the channel. The current I_{DS} increases with the number of the injected minority carrier density n_p where

$$n_p = n_{po} e^{[V_F - \phi_G]/V_T} .$$

A low injection due to low V_F and n_{po} results in a low current. Figure 4.7 shows an exponential decrease in current, I_{DS}, with increasing doping concentration, which implies that the reduction in V_F is the main cause of this rapid I_{DS} decrease.

The effect of the channel doping concentration on the drain-source current, I_{DS}, is different for SIT and GFC-BARITT devices. The I_{DS} of a SIT increases with an increase in the channel doping concentration. The I_{DS} increase in a SIT device is expected to be linear with the doping concentration for a fixed V_{DS}. The I_{DS} of a GFC-BARITT device, on the other hand, decreases exponentially with the doping concentration which is mainly due to the decrease of the forward biasing voltage, V_F.

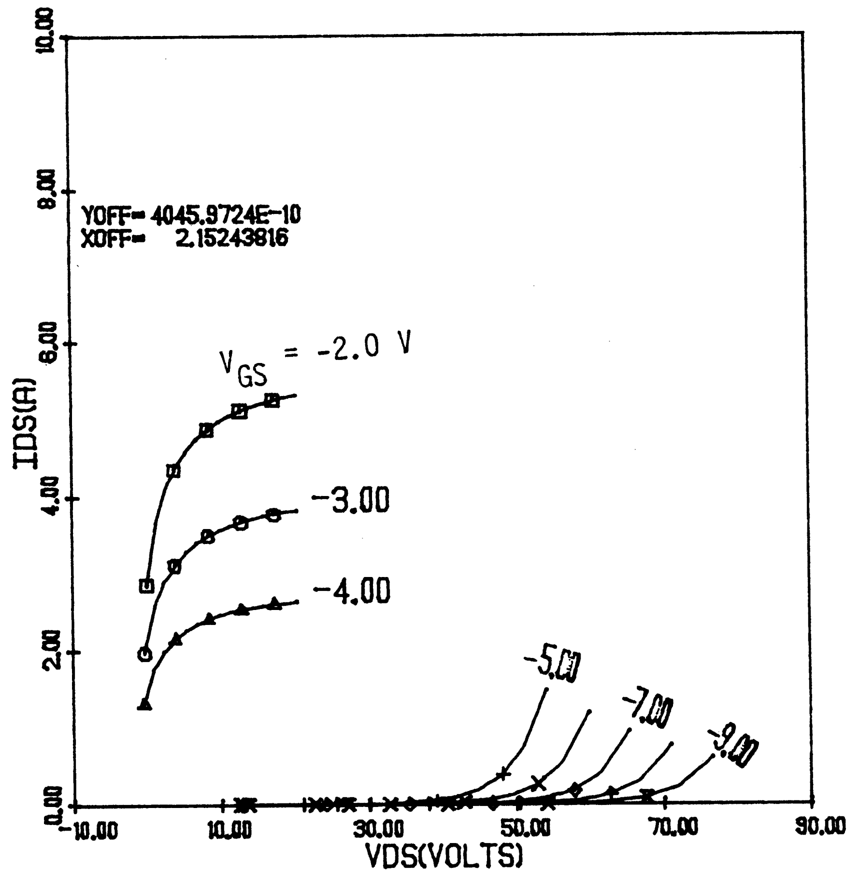
4.5.2 Temperature Effect. The performance of power devices at high temperature is important, especially for device reliability. If any device has a positive temperature coefficient, the device current will increase with the increasing temperature, and finally, a thermal runaway will occur. Thermal runaway will result in the destruction of the device. In Section 4.3, the temperature-dependent material parameters, were given and have been implemented into the SIM-GFC program.

The temperature effect on the device characteristics analyzed in this section is valid for low level injection. In Fig. 4.8(a) and Fig. 4.8(b), the temperature effect on I_{DS} of a SIT device is shown for T = 300°K and T = 400°K. The device size and the bias have been chosen in such a way that a SIT device operates in a mixed mode as a FET at low gate biases, V_{GS}, and as a SIT at high V_{GS}. The comparison of Fig. 4.8(a) and Fig. 4.8(b) indicates that the SIT mode at low level injection has a positive temperature coefficient, and the FET mode is less temperature sensitive, (has a smaller positive temperature coefficient). In Fig. 4.9, a GFC-BARITT device I_{DS} at 400 °K temperature is shown. In Fig. 4.7, the same size GFC-BARITT device I_{DS} at 300°K temperature was given. A comparison of the two figures reveals that the GFC-BARITT device has a positive temperature coefficient. The I_{DS} at 400°K is almost two hundred times that of I_{DS} at 300°K.

The I_{DS} increase with the temperature increase in larger in GFC-BARITT devices than in SIT devices. The injected carrier density as a function of temperature for a GFC-BARITT device is given in Eq. 4.18 and for a SIT device in Eq. 4.19. The intrinsic carrier density is given by

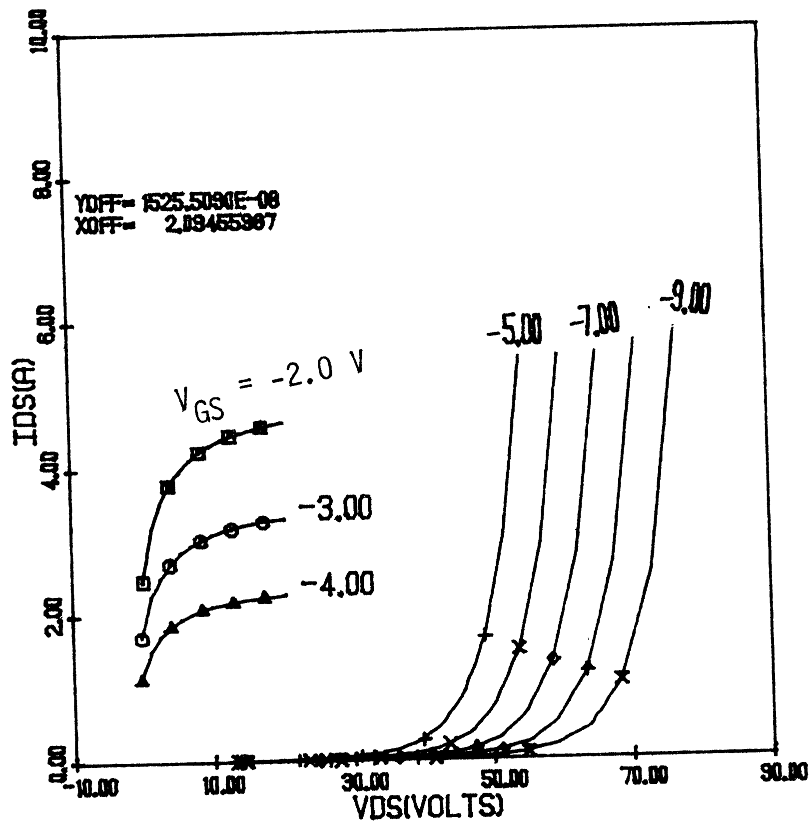
$$n_i(T) = n_o T^{1.5} \exp[-E_G(T)/2kT] \quad , \qquad (4.17)$$

where n_o is a constant and is different for various semiconductors, and T is the temperature in degrees Kelvin. The injected carrier density for a GFC-BARITT device is



(a) I-V Characteristics at T = 300°K.

Fig. 4.8 The Current Voltage Characteristics of a SIT Operating in FET and Injection (SIT) Modes (Device S1).



(b) I-V Characteristics at T = 400°K.

Fig. 4.8 The Current Voltage Characteristics of a SIT Operating in FET and Injection (SIT) Modes (Device S1).

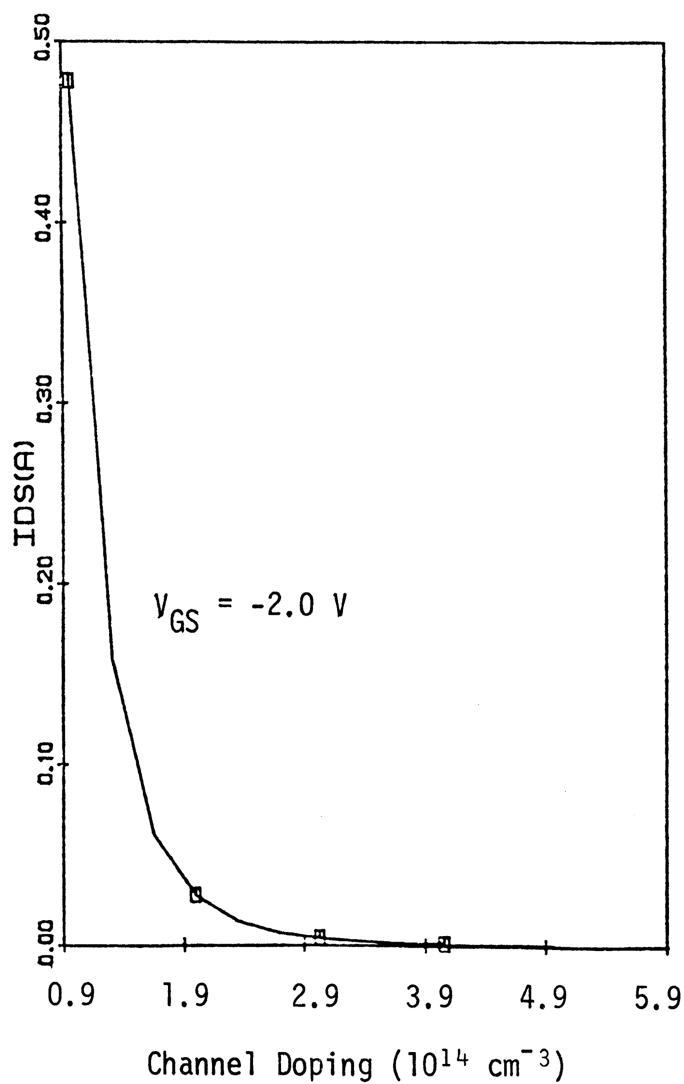


Fig. 4.9 A GFC-BARITT Device Current as a function of the Channel Doping at T = 400°K (Device B1 Compared to Fig. 4.7 at T = 300°K).

$$n_{inj}(T) = (n_i^2(T)/N_D)\exp[(V_F - \phi_G)/kT] \qquad (4.18)$$

and for a SIT device,

$$n_{inj}(T) = N_D \exp[(V_F - \phi_G)/kT] \quad . \qquad (4.19)$$

At low level injection, both the minority and majority carriers density increase with temperature. In Eq. (4.17), the $n_i(T)$ is strongly temperature dependent. The n_{inj} in Eq. (4.18) includes the square of $n_i(T)$, therefore the n_{inj} in GFC-BARITT device is even more strongly temperature dependent. In Eq. (4.19), the n_{inj} increases with temperature, if the $(V_F - \phi_G)$ is negative. When the $(V_F - \phi_G)$ becomes positive, the n_{inj} will decrease with increasing temperature. The n_{inj} in Eq. (4.18), however, starts to decrease at much higher temperature for a positive $(V_F - \phi_G)$.

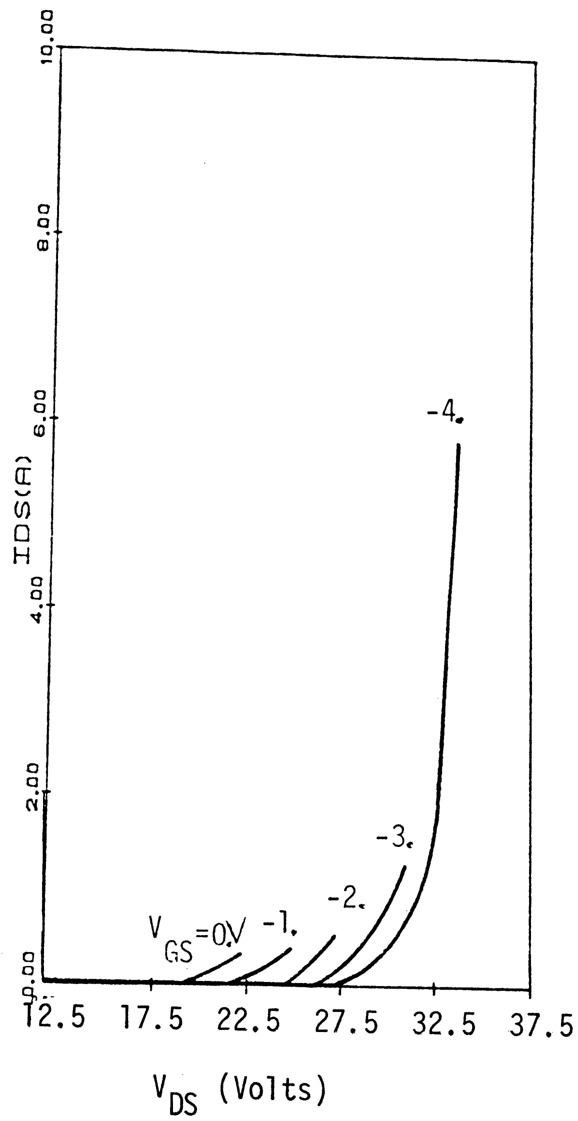
It can be concluded that the TTPT devices have a positive temperature coefficient at low level injection, and a negative temperature coefficient at medium and high level injection.

4.5.3 The Geometry Effect. The geometry of the device affects its performance. The most critical element of the device geometry is the spacing, W_{GS}, between the source and the gate. It is essential to place the gate close to the carrier injection point near the source. If the gate if far from the injection point, the gate voltage cannot perturb the barrier height so as to modulate I_{DS}.

It is shown in Fig. 4.10(a) for a GFC-BARITT device with a W_{GS} of 1.3 μm and in Fig. 4.10(b) for a device with a W_{GS} of 0.3 μm.

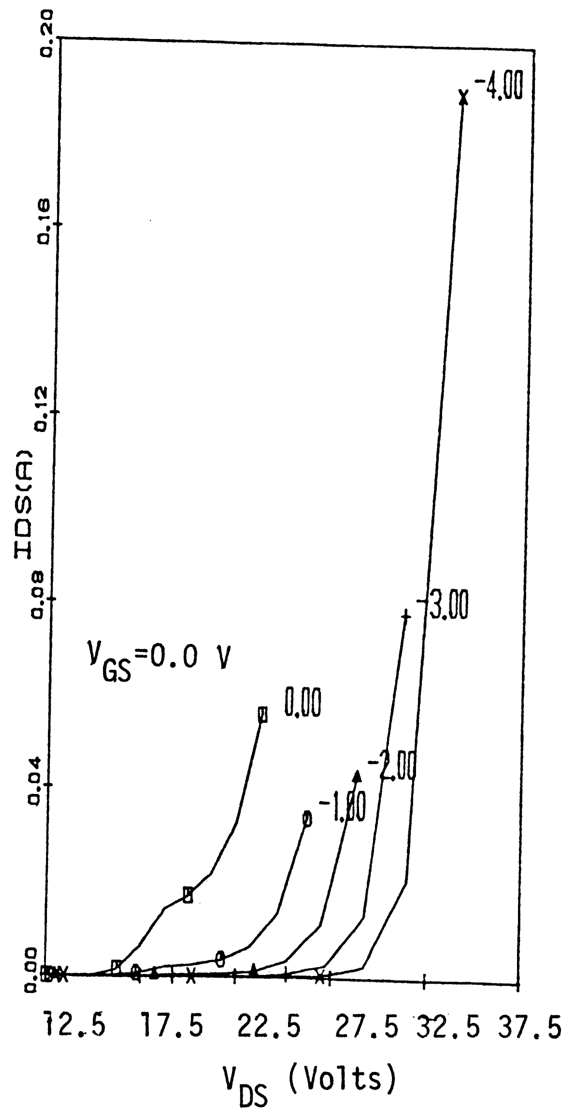
A comparison of Fig. 4.10(a) and Fig. 4.10(b) indicates that an increase in W_{GS} diminishes the gate voltage control over I_{DS}. As seen in Fig. 4.10(a), an increasing gate voltage does not affect I_{DS} as much because W_{GS} is larger. On the other hand, in Fig. 4.10(a), I_{DS} is controlled with a small gate voltage due to the small W_{GS} (0.3 μm). The effect of W_{GS} on a SIT device is different from that of a GFC-BARITT device. If W_{GS} becomes too large, A GFC-BARITT device will operate like a BARITT diode (a two-terminal device) but in the case of a SIT device, it is always a three terminal device, except the mode of its operation changes from carrier injection to ohmic conduction type. In other words, a SIT device with a large W_{GS} will operate as a FET. A SIT device will operate under various conditions such as large channel thickness, W_S and heavy channel doping.

A SIT device operation as a FET is demonstrated in Fig. 4.11. The simple FET model as SIM-GFC conceptually predicts the device characteristics such as the negative resistance of the I-V characteristics of the III-V compound semiconductor FETs. The I-V characteristics of the same size Si FET in Fig. 4.11(a), GaAs FET in Fig. 4.11(b) and InP FET in Fig. 4.11(c) are shown. The importance of the high low-field mobility becomes apparent from the comparison of the I-V characteristics. At low bias, V_{DS}, voltage, the GaAs FET has the highest current, I_{DS}, and transconductance, g_m. At high V_{DS}, however, the InP FET performance is the best due to its high peak and high



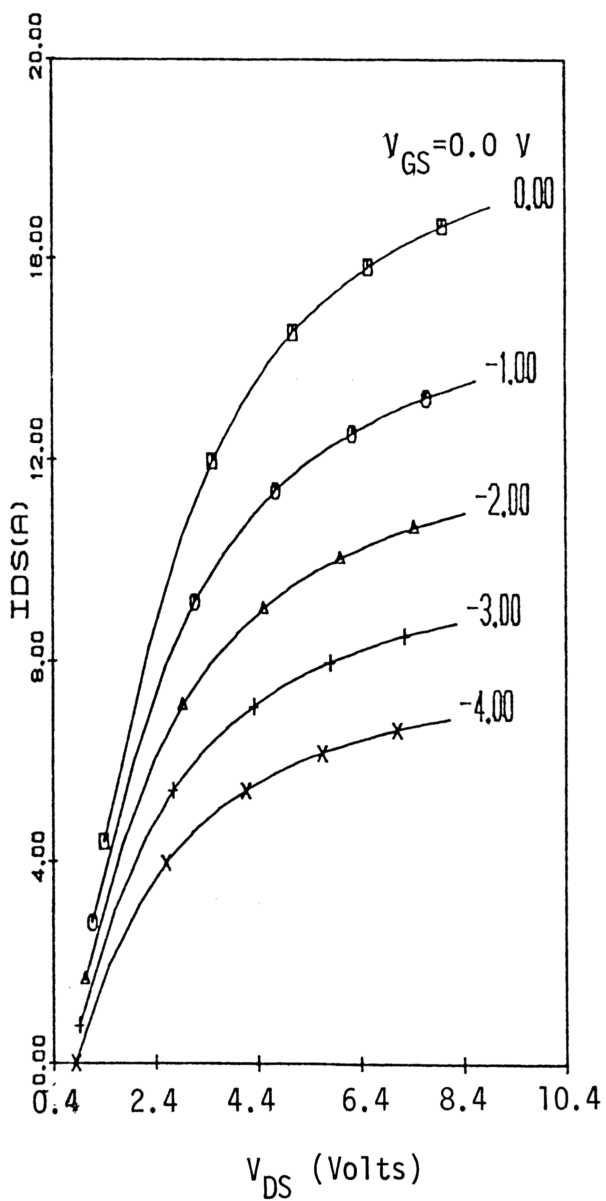
(a) The I-V Characteristics with 1.3 μm W_{GS} Spacing (Device B2).

Fig. 4.10 The Gate-Source Spacing, W_{GS}, Effect on the I-V Characteristices of a GFC-BARITT Device.



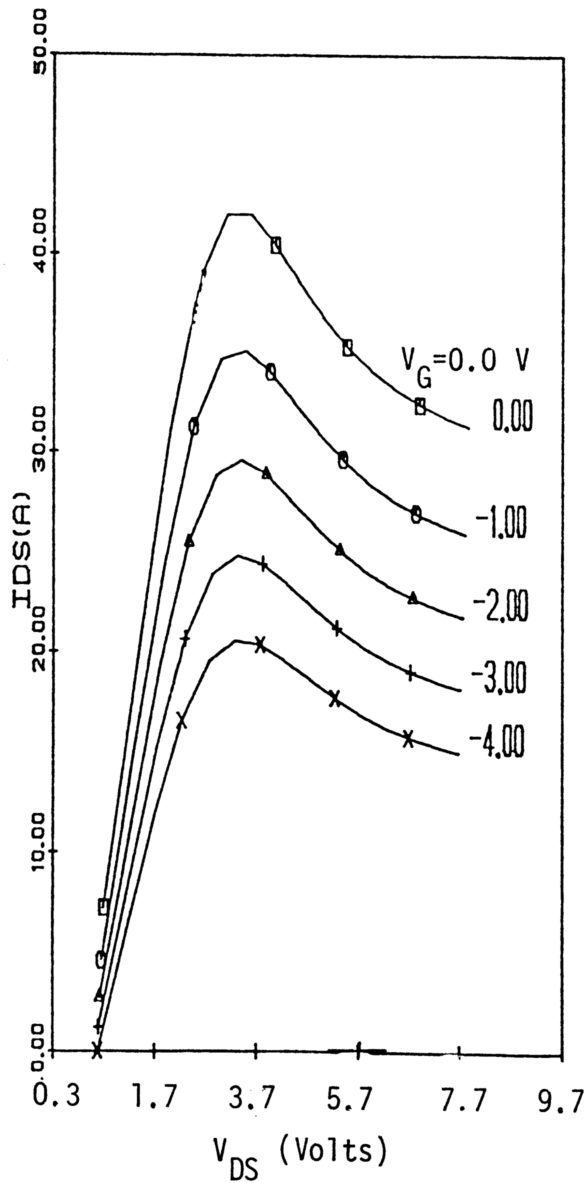
(b) The I-V Characteristics with 0.3 μm W_{GS} Spacing (Device B3).

Fig. 4.10 The Gate-Source Spacing, W_{GS}, Effect on the I-V Characteristics of a GFC-BARITT Device.



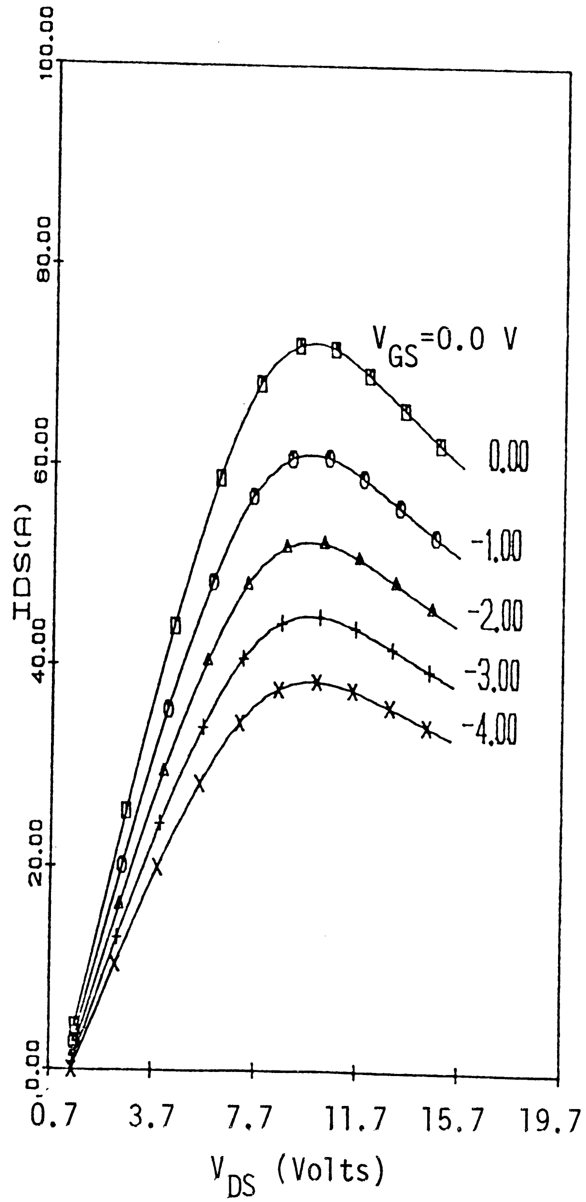
(a) Si Device, S3.

Fig. 4.11 The I-V Characteristics of the Vertical FETs.



(b) GaAs device, S4.

Fig. 4.11 The I-V Characteristics of the Vertical FETs.



(c) InP device, S4.

Fig. 4.11 The I-V Characteristics of the Vertical FETs.

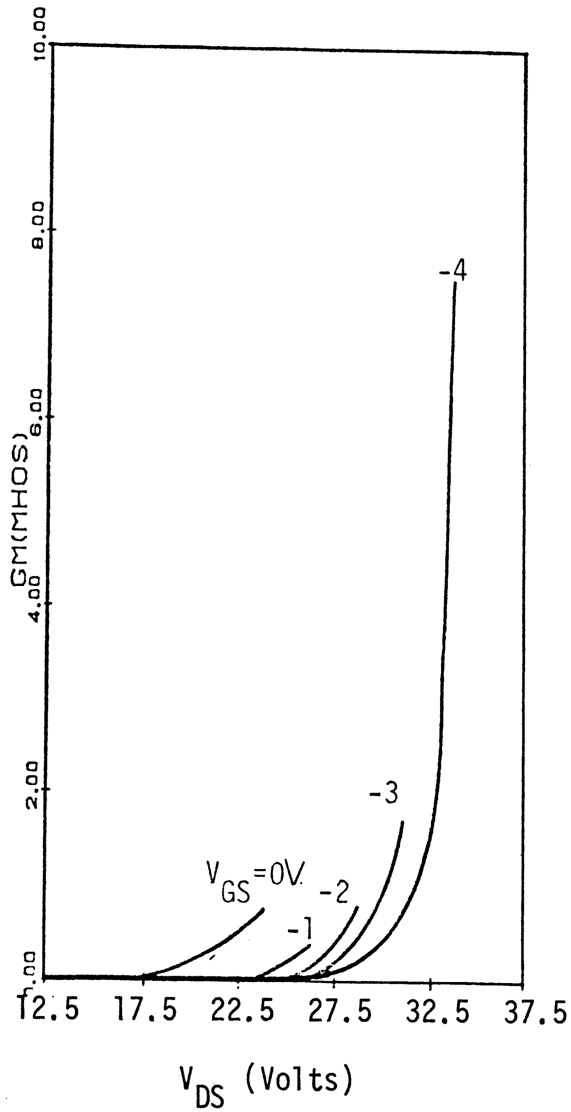
saturation velocity. A GaAs FET saturates at low bias voltages and its peak carrier velocity is lower than that of the InP FET. The I-V characteristics of the GaAs, InP and Si SIT devices (in SIT device mode) has also been studied. The performance of these three devices is not signficantly different from one another.

It can be concluded that W_{GS} is the most critical geometrical parameter which determines the mode of the device operation. For large W_{GS}, a GFC-BARITT device operates as a FET. The III-V compound semiconductor punch-through devices are not significantly advantageous over silicon devices. The real advantages of these semiconductors over silicon becomes significant for the non-punch-through devices which utilize the low field mobility such as FETs.

4.5.4 Dc and Small-Signal Device Parameters. Dc and small-signal device parameters, I_{DS}, g_m, g_{ds}, C_{gs}, C_{gd} and C_{ds} have been calculated to describe the small-signal equivalent circuit of the TTPT devices and FETs. The dc I-V characteristics of the TTPT devices and FETs have been analyzed under various operating conditions in the preceding sections. The I_{DS} of a TTPT device increases exponentially with a V_{DS} increase, but the I_{DS} of a FET saturates at high V_{DS} voltages. The V_{DS} where I_{DS} saturates is the highest for an INp FET in comparison with GaAs and Si FETs. The III-V compound semiconductor FETs show a common negative dc resistance effect in their I-V characteristics.

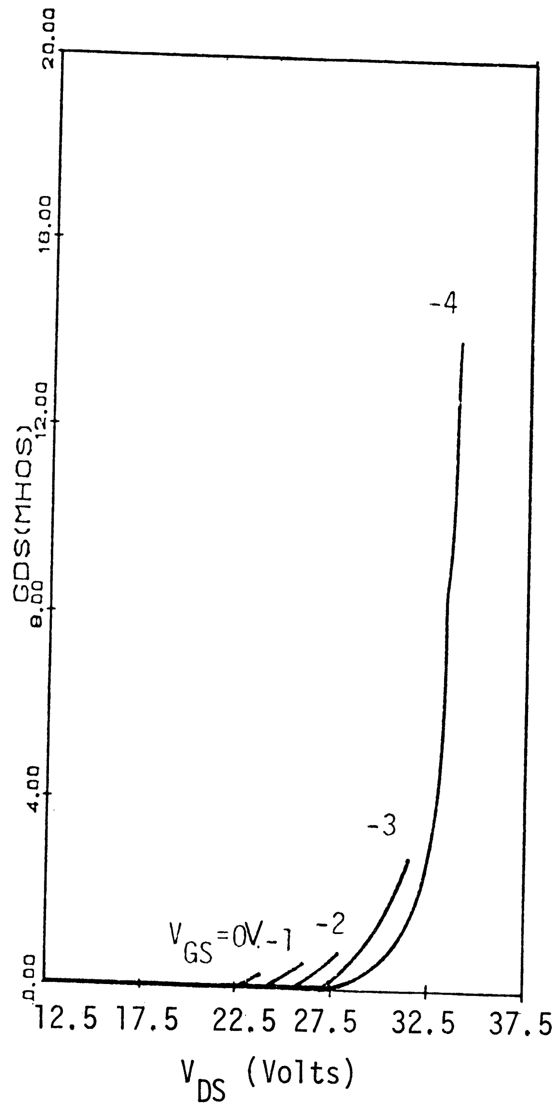
The small-signal device parameters of the TTPT devices increase also exponentially with the dc drain-source voltage with the exception of C_{ds}. The effect of the stored charge in the channel due to the injected carriers are included in the calculation of the gate-source, C_{gs} and drain-gate, C_{dg}, capacitances. In the insulated gate TTPT devices, C_{gs}, is a series combination of the insulated gate capacitance and the channel capacitance. The total source-gate capacitance C_{gs} of an insulated gate TTPT GFC-BARITT device is smaller than the C_{gs} of an ohmic or Schottky gate TTPT device. On the other hand, the blocking gain (V_{DS}/V_{GS}) of a GFC-BARITT device is smaller than the blocking gain of the other TTPT devices (SITs and lateral punch-through transistors). The reason for the low blocking gain of a GFC-BARITT device is due to the voltage division between the insulated gate capacitance and the channel capacitance.

The small-signal device parameters of a GFC-BARITT device are given in Fig. 4.12 as a function of the dc bias voltages, V_{DS} and V_{GS}. As shown in Fig. 4.12, the increase in V_{DS} increases g_m, g_{ds}, C_{gs} and C_{dg} exponentially. However, an increase in V_{GS}, decreases these parameters. The small-signal parameters of the other TTPT devices are not shown because their variations as a function of V_{DS} and V_{GS} are similar to the plots shown in Fig. 4.12(a) through 4.12(d). III-V compound semiconductor TTPT devices do not show any more interesting characteristics than those for silicon.



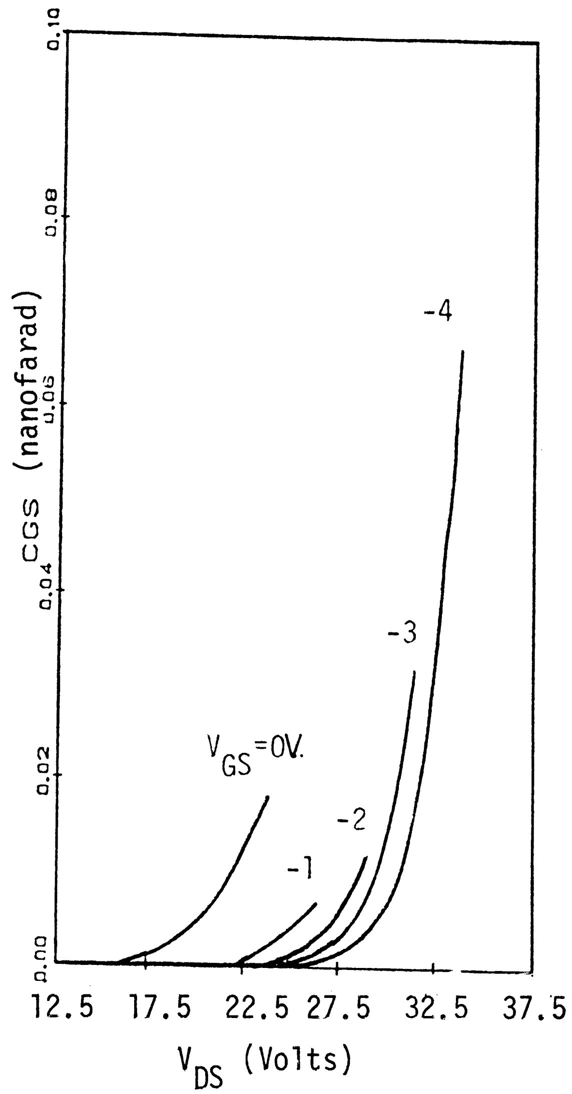
(a) The transconductance.

Fig. 4.12 Small-Signal Parameters of a GFC-BARITT Device as a Function of V_{DS} for Different Values of V_{GS} (Device B2).



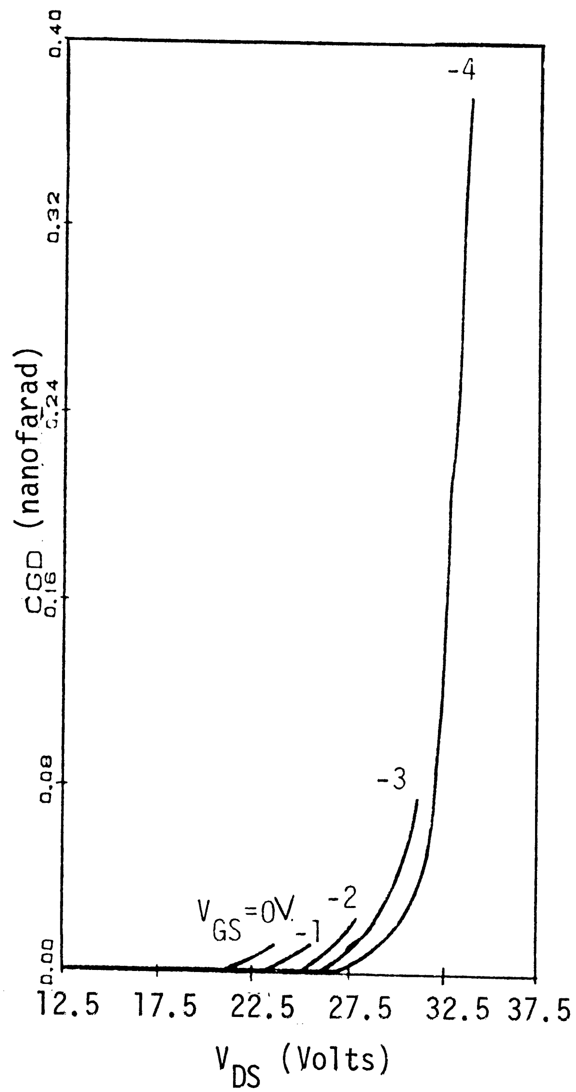
(b) The conductance.

Fig. 4.12 Small-Signal Parameters of a GFC-BARITT Device as a Function of V_{DS} for Different Values of V_{GS} (Device B2).



(c) The gate-source capacitance.

Fig. 4.12 Small-Signal Parameters of a GFC-BARITT Device as a Function of V_{DS} for Different Values of V_{GS} (Device B2).



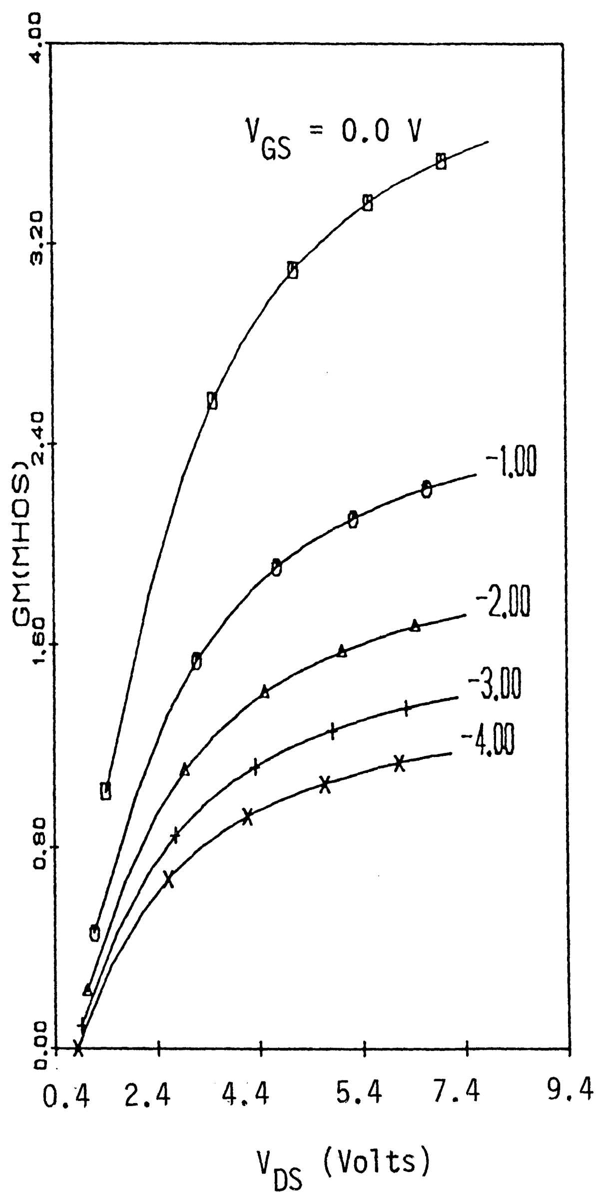
(d) The gate-drain feedback capacitance.

Fig. 4.12 Small-Signal Parameters of a GFC-BARITT Device as a Function of V_{DS} for Different Values of V_{GS} (Device B2).

The small-signal device characteristics of a SI FET are shown in Fig. 4.13(a) through 4.13(d). The transconductance and conductance of the III-V compound semiconductor FETs show the effect of the dc negative resistance as seen in Fig. 4.14(a) and Fig. 4.14(b). In Fig. 4.13(a) and Fig. 4.14(a), the transconductances follow the dc current variation as a function of V_{DS} and V_{GS}. The conductance of an FET decreases with increasing bias voltages V_{DS}, and V_{GS} as shown in Fig. 4.13(b) and Fig. 4.14(b). In Fig. 4.14(b) the conductance, g_{ds}, increases from the +3 volt point to +4 point due to the dc negative resistance effect. Beyond the bias voltage where the current, I_{DS}, saturates, the g_{ds} decreases rapidly. In Fig. 4.13(c) through (d) and 4.14(c) through (d), the capacitances decrease with increasing V_{DS} and V_{GS}, because these capacitances, C_{gs} and C_{dg} are the parallel plate capacitances of the depletion regions.

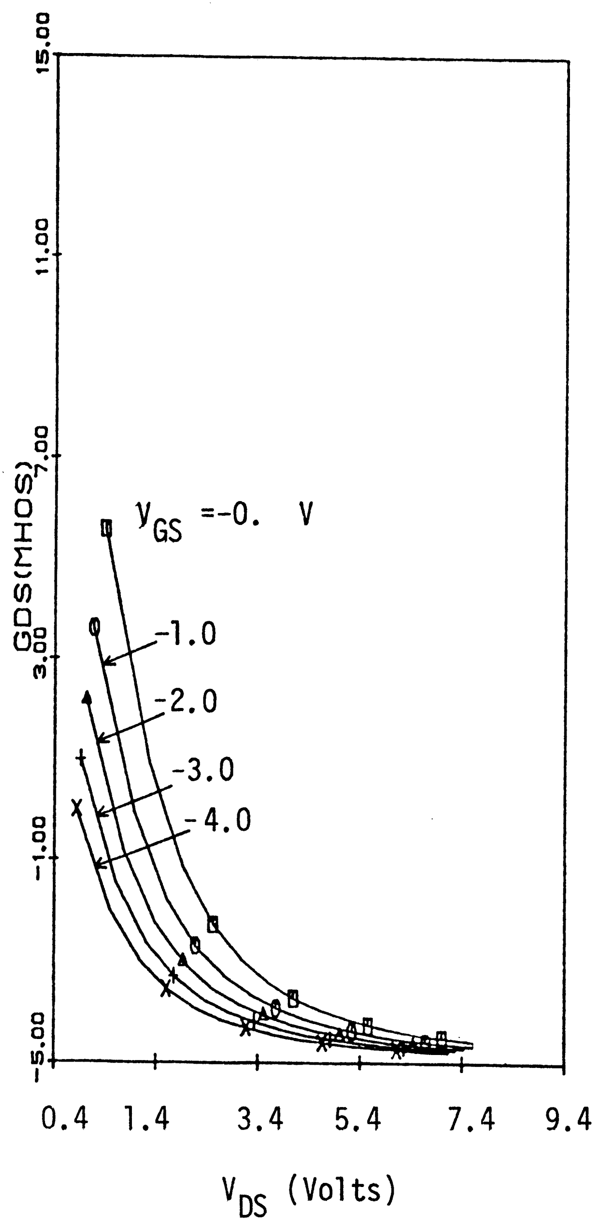
From the analysis of the dc current and small signal device characteristics of the various TTPT devices and FETs it can be concluded that using III-V compound semiconductors to fabricate SIT or majority carrier injection type GFC-BARITT devices is not as advantageous as silicon. The current ratio of a III-V compound semiconductor SIT and a Si SIT (RIDS) is approximately equal to the ratio of their saturation velocities (RV_{sat}):

$$\text{RIDS} \propto \frac{v_{sat}\text{ of III-V compound semiconductor}}{v_{sat}\text{ of silicon}} .$$



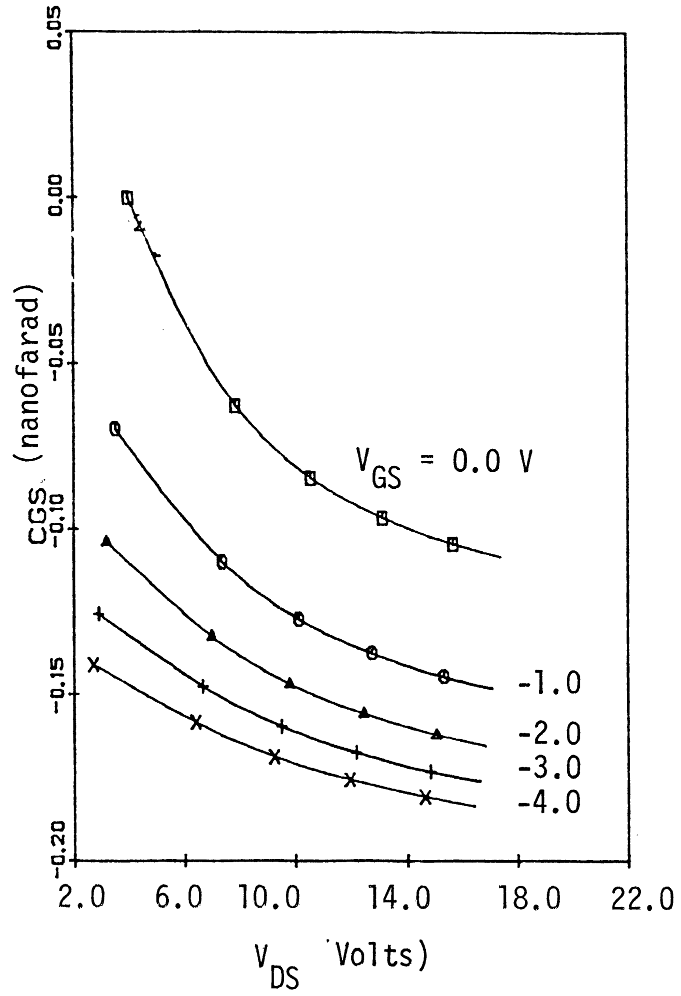
(a) The transconductance.

Fig. 4.13 The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3.



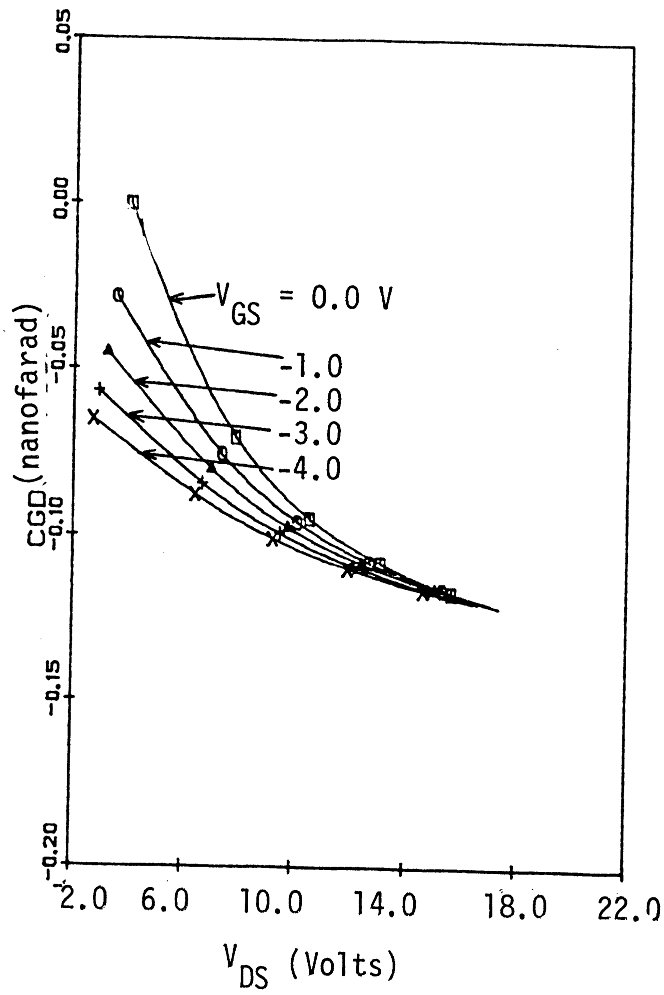
(b) The conductance.

Fig. 4.13 The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3.



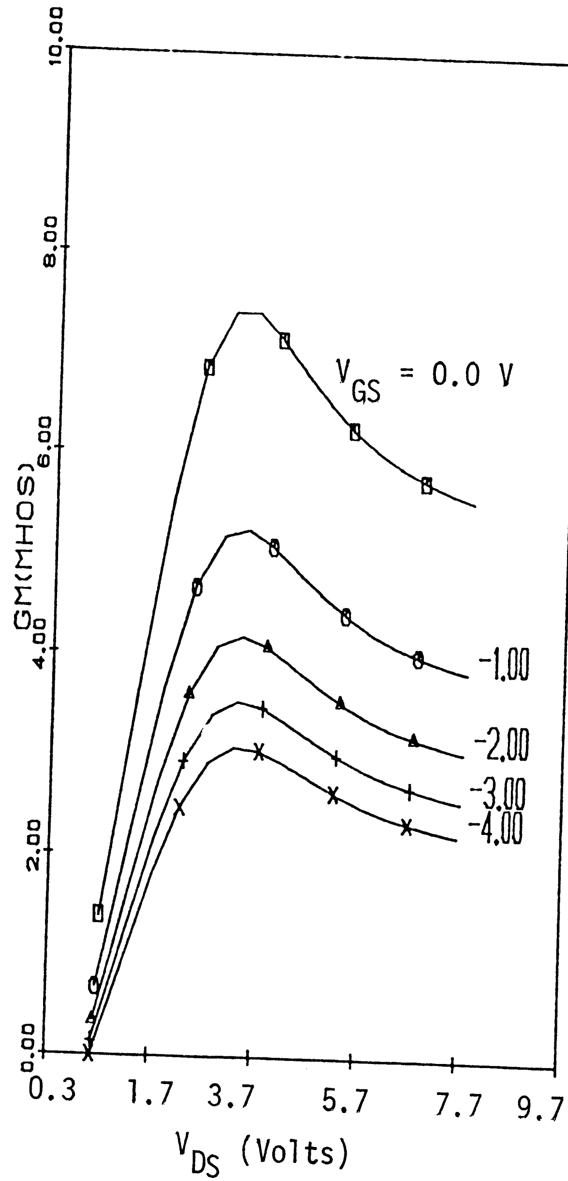
(c) The gate-source capacitance.

Fig. 4.13 The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3.



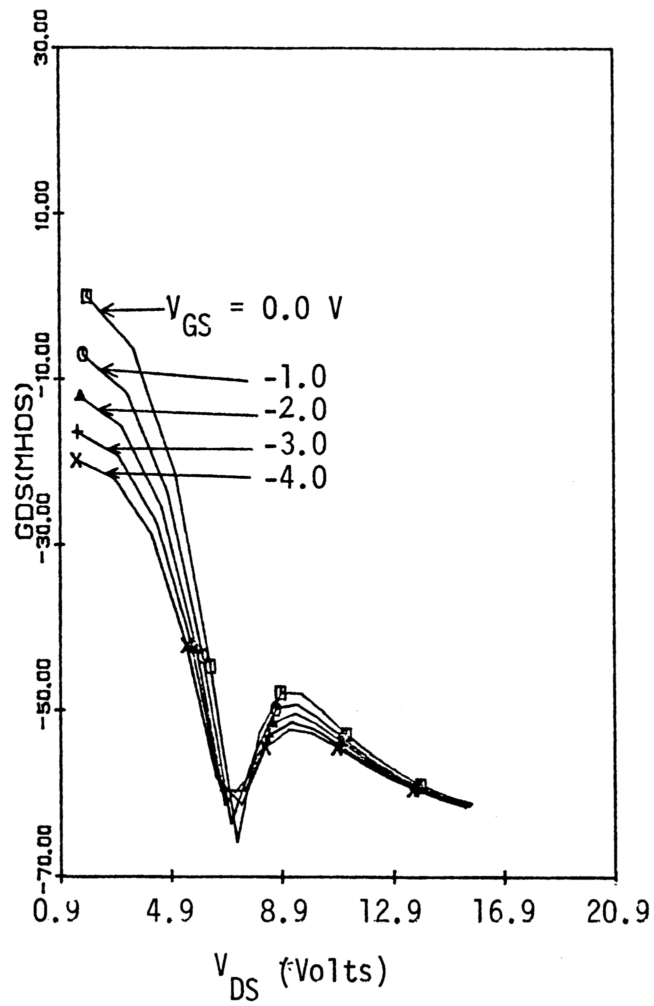
(d) The gate-drain capacitance.

Fig. 4.13 The Small-Signal Equivalent Circuit Parameters of a Silicon FET, S3.



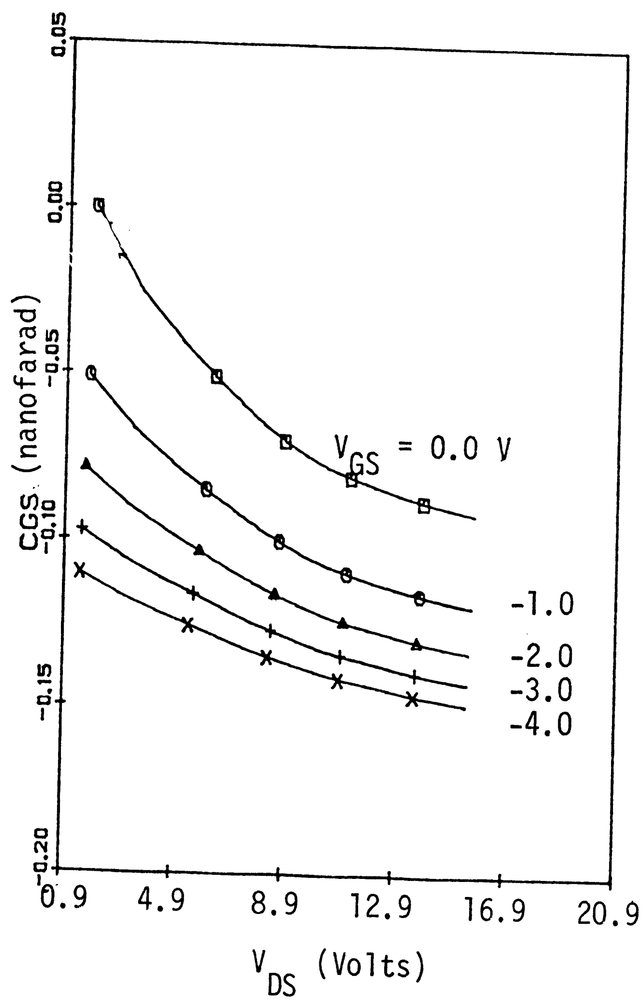
(a) The transconductance.

Fig. 4.14 The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4.



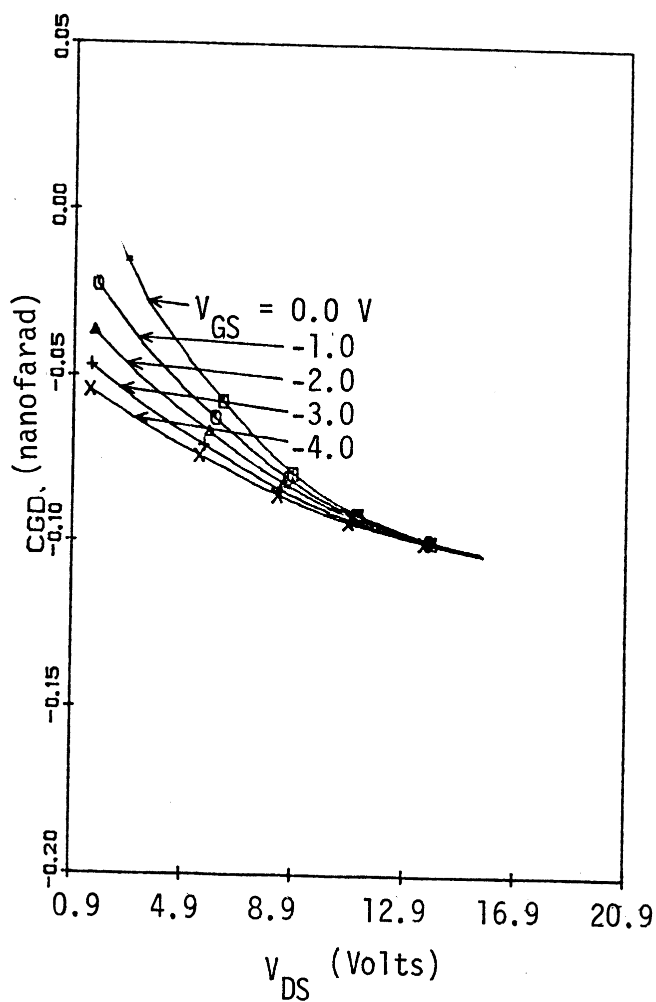
(b) The conductance.

Fig. 4.14 The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4.



(c) The gate-source capacitance.

Fig. 4.14 The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4.



(d) The gate-drain capacitance.

Fig. 4.14 The Small-Signal Equivalent Circuit Parameters of a GaAs FET, S4.

The same RIDS figure of merit to select a material for a SIT device is not valid for the GFC-BARITT or the minority carrier injection type punch-through devices. The carrier injection in silicon GFC-BARITT devices is higher than in those of the III-V compound semiconductor devices. In other words, the critical factor in GFC-BARITT devices is the injection of the carriers and not the drift of those carriers as in the case of the majority carrier devices.

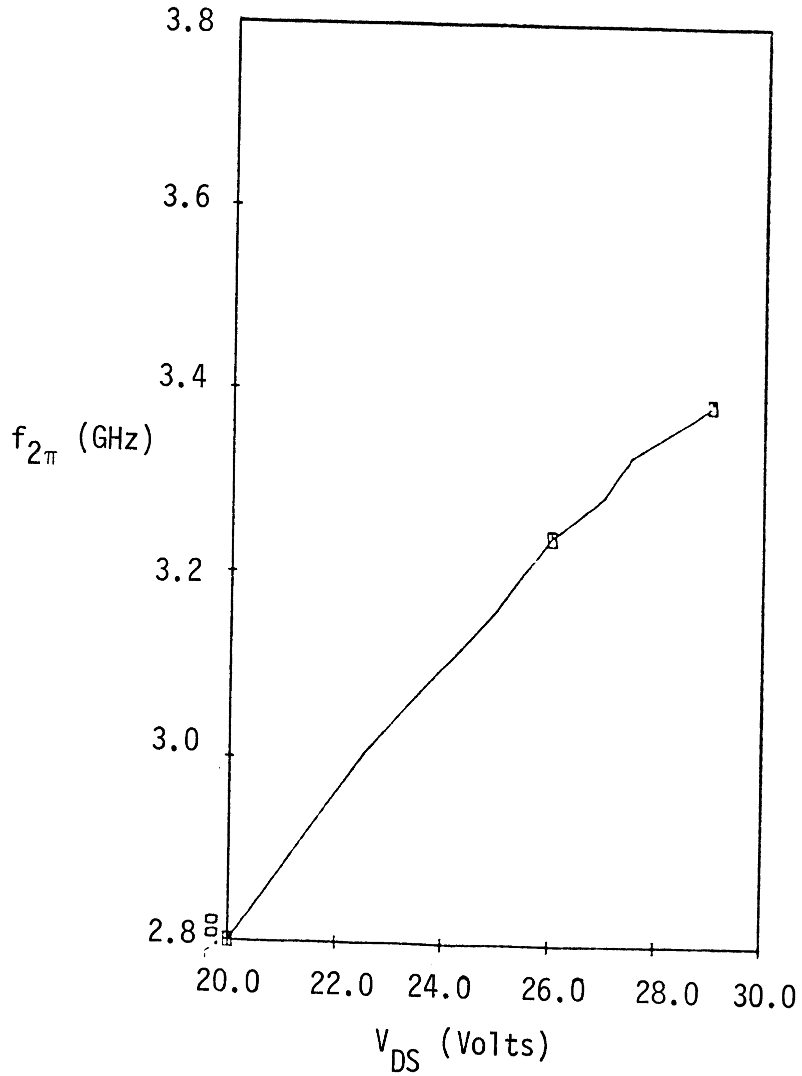
The GaAs and InP GFC-BARITT devices can be used to achieve high power and frequency operations. Also, these devices can operate at high temperatures due to their high energy band gaps. The biggest advantage of using a III-V compound semiconductor over silicon is to fabricate FETs. This can be seen from the comparison of the small signal parameters of the Si and GaAs FETs in Fig. 4.13 and Fig. 4.14, respectively. The C_{gs} for a Si and a GaAs FET is the same but the g_m of a GaAs FET is almost 2.2 times higher than the g_m of a Si FET which results in the higher frequency operation of the GaAs FETs.

4.6 Small-Signal Performance

The small-signal circuit performance of the SIT and GFC-BARITT devices have been investigated as a function of the dc bias voltage. V_{DS}, the channel doping concentration and the frequency. The small-signal circuit performance of the TTPT devices is evaluated in terms of the cut-off frequency, maximum available gain, maximum unilateral gain, noise figure, noise measure and the 360 degree phase frequency.

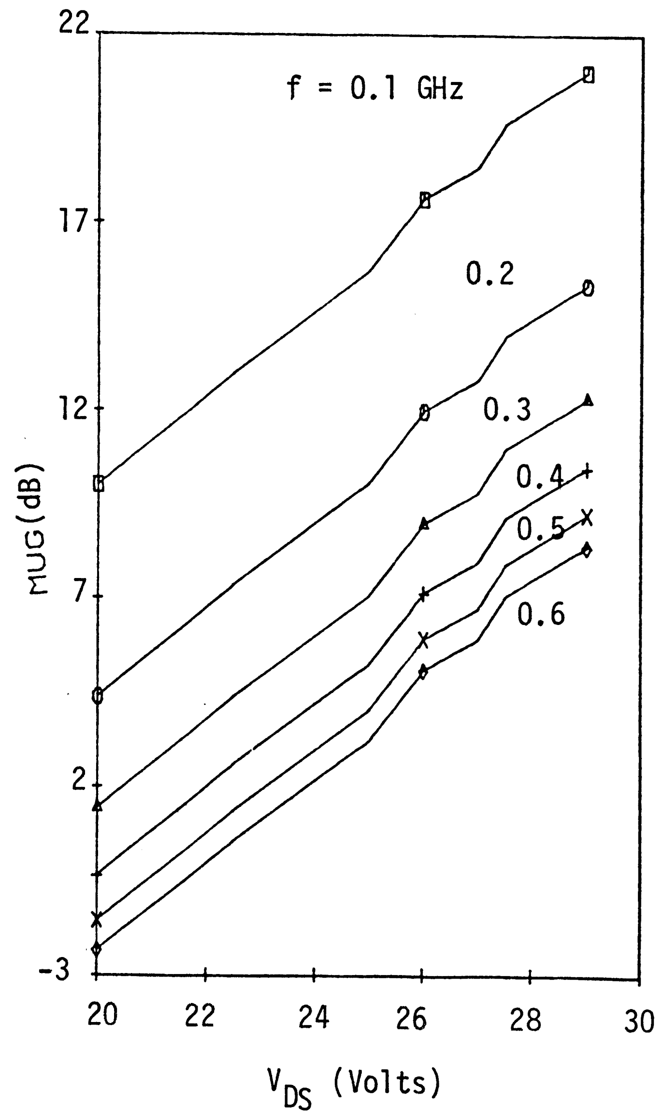
4.6.1 GFC-BARITT Devices. The performance of a GFC-BARITT device improves as a function of the dc bias, V_{DS}. The maximum available gain, the maximum unilateral gain and the cut-off frequency increase with V_{DS}. The small-signal transconductance increases exponentially with V_{DS} and this improves the gain and the cut-off frequency. The 360-degree phase frequency is inversely proportional to the transit time. The transit time decreases with increasing V_{DS}. As a result, the 360-degree phase frequency also increases with V_{DS}. The noise figure and the noise measure decrease with V_{DS}. The noise measure is not only a function of the noise figure, but it is also a function of the gain. Even if the noise figure is small, the noise measure increases with decreasing gain. It reaches its limiting value of the noise figure minus one (F-1) at high gain. The performance of a GFC-BARITT device does not improve indefinitely as a function of V_{DS}, due to the space charge limitation which occurs at high bias voltages.

In Fig. 4.15, the gain, the noise figure and the noise measure are shown as a function of both the operating frequency (0.1-0.6 GHz) and the dc bias, V_{DS}. The cut-off and 360-degree phase frequencies are also shown as a function of V_{DS}. The small-signal characteristics were calculated using values of V_F which were calculated from the measured dc I-V characteristics of a Si GFC-BARITT device which was fabricated in this laboratory. The increase in the operating frequency decreases the gain and the noise figure but increases the noise measure. The noise figure increases slowly with V_{DS}, because the noise temperature increases with the electric



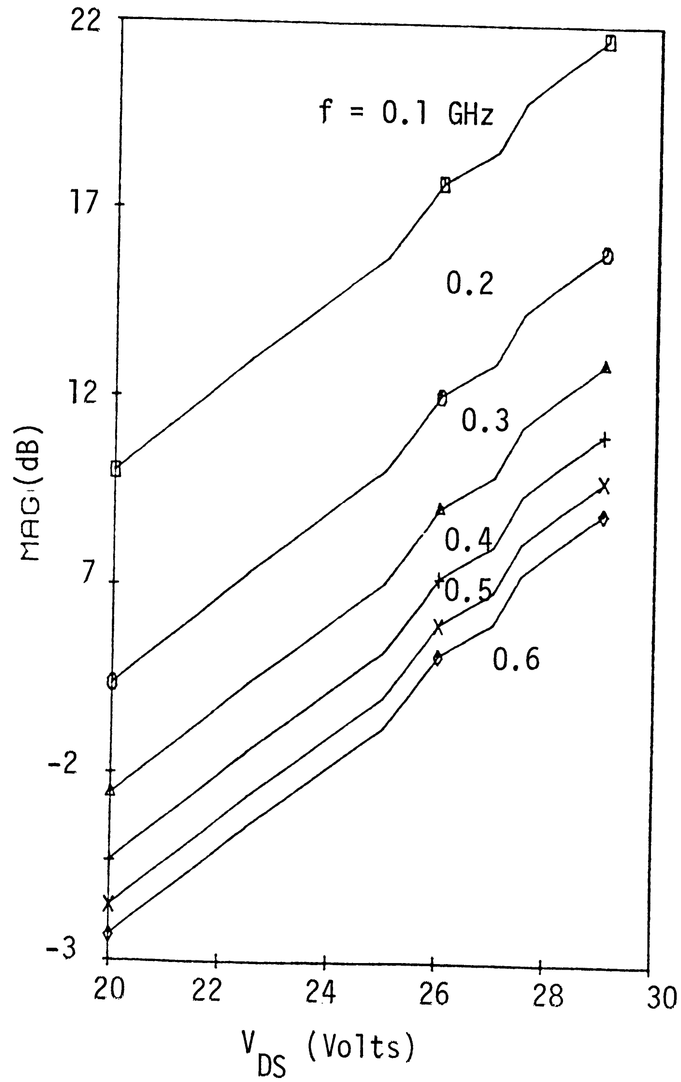
(a) 360-degree phase angle frequency, $f_{2\pi}$.

Fig. 4.15 The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of V_{DS}. (V_{GS} = 0 V)



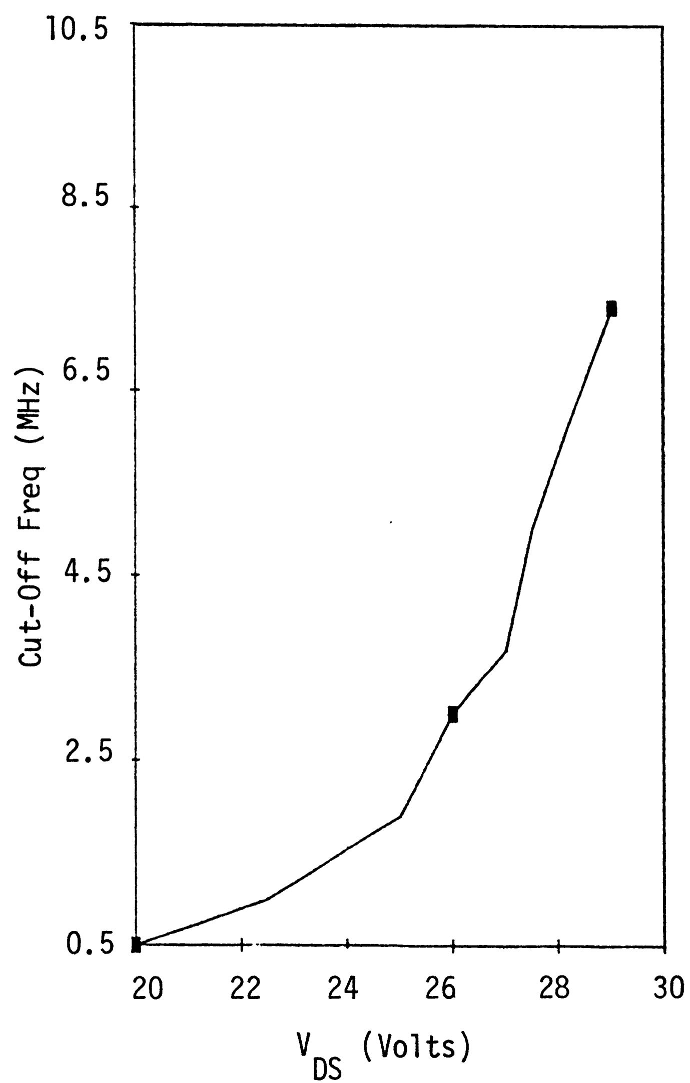
(b) The maximum unilateral gain.

Fig. 4.15 The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of V_{DS} (V_{GS} = 0 V)



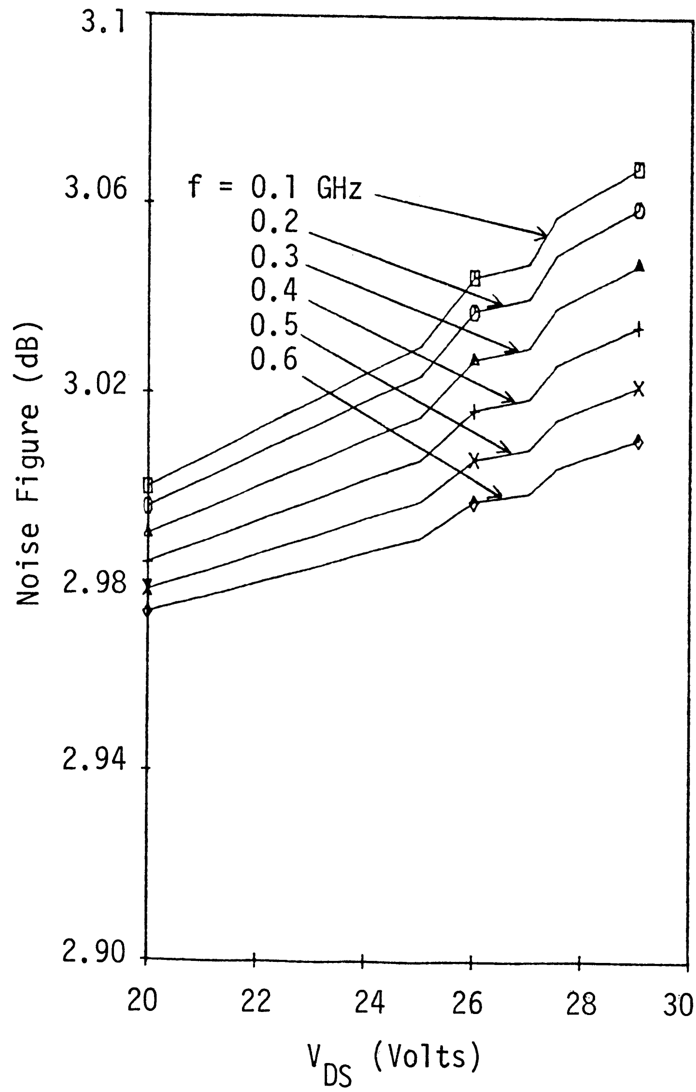
(c) The maximum available gain.

Fig. 4.15 The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of V_{DS} at Different Frequencies. (V_{GS} = 0 V)



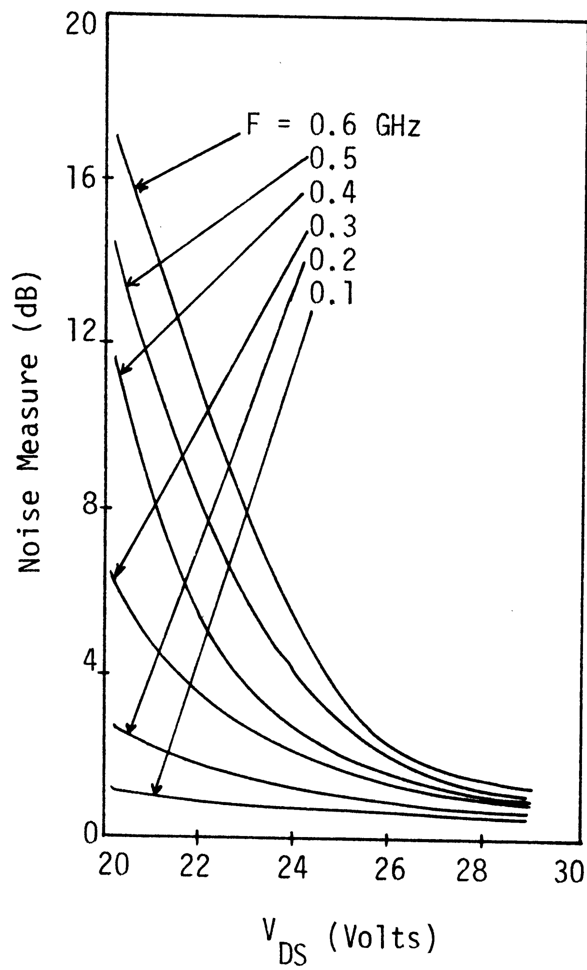
(d) The cut-off frequency, f_T.

Fig. 4.15 The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of V_{DS}. (V_{GS} = 0 V)



(e) The noise figure.

Fig. 4.15 The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of V_{DS} at Different Frequencies. (V_{GS} = 0 V.)



(f) The Noise Measure.

Fig. 4.15 The Small-Signal Performance of a Si GFC-BARITT Device, B4, as a Function of V_{DS} at Different Frequencies. (V_{GS} = 0 V.)

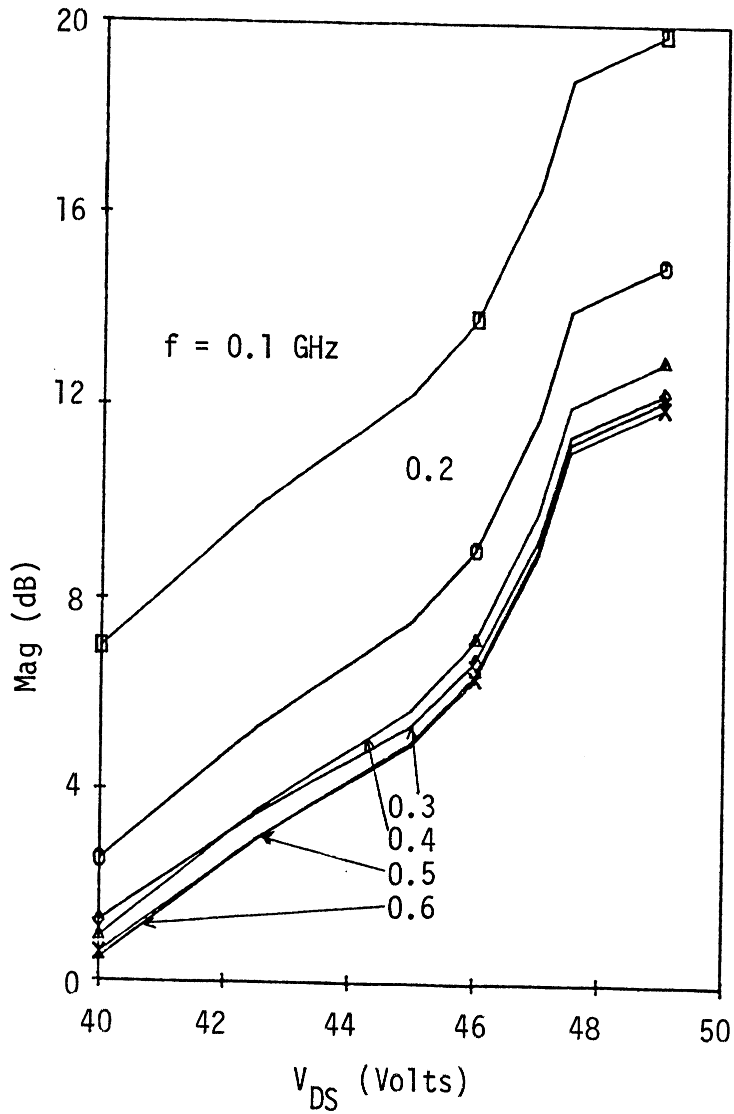
field which is also directly proportional to V_{DS}. The noise measure in Fig. 4.15(f) decreases with V_{DS} due to the higher maximum available gain (MAG) at high V_{DS} values.

The 360-degree phase frequency is a useful figure of merit to point out the significance of the transit time effect. The cut-off frequency is defined as the frequency at which the current gain becomes unity. It becomes a useful figure of merit for the devices if the transit time is small. It is important to determine the 360-degree phase frequency in addition to the cut-off frequency of high power, high frequency devices. If the 360-degree phase frequency ($f_{2\pi}$) is larger than the conventional cut-off frequency (f_T), the effect of the transit time on the device characteristics may be neglected. If, however, the $f_{2\pi}$ is smaller than or equal to f_T, the negligence of the transit time effect may result in an over-estimation of the device performance.

The effect of the transit time on g_m and g_{ds} has been neglected and the calculated small-signal gain noise figure and measure are shown in Fig. 4.15. The same device characteristics have been calculated by inclusion of the transit time effect and the new results are seen in Fig. 4.16. The transit time lowers the cut-off frequency, f_T, but its effect on the maximum available gain, MAG, is small, because the transit time effect is cancelled in the MAG expression

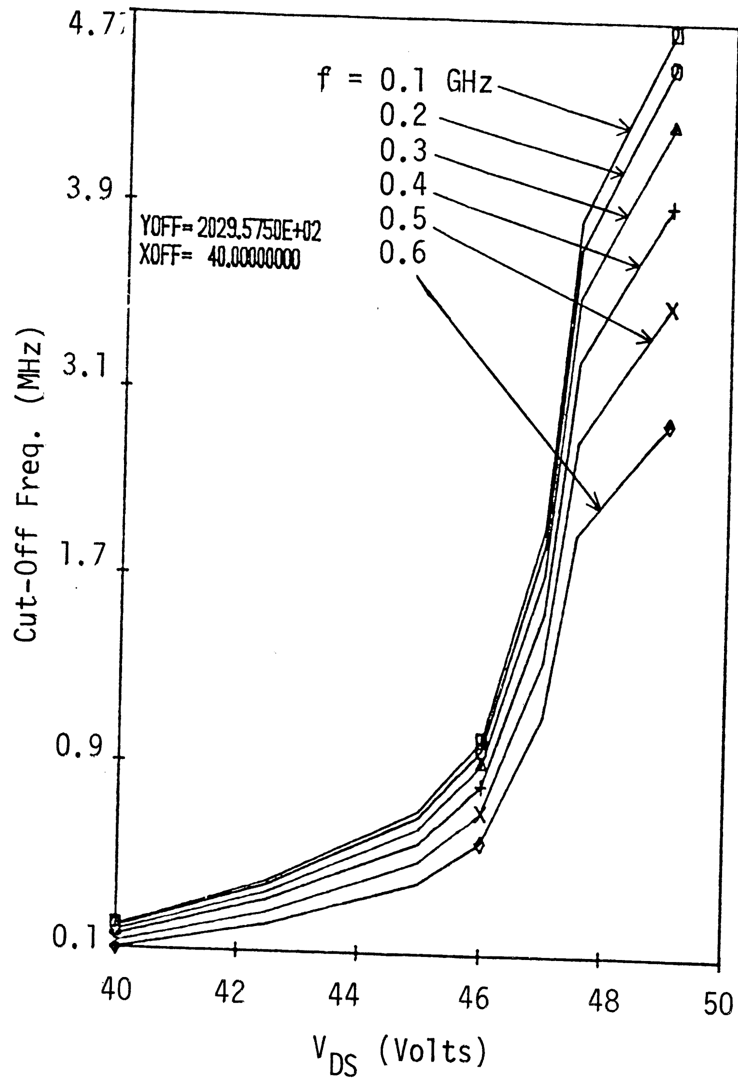
$$MAG = \frac{|y_{21}|^2}{4\ \mathrm{Real}(y_{11})\ \mathrm{Real}(y_{22})} .$$

The y_{21} includes $e^{-j\omega\tau_d}$ through g_m. The y_{22} includes $e^{-j\omega\tau_d}$ through g_{ds}.



(a) The MAG.

Fig. 4.16 The Transit-Time Effect on the Small-Signal Device Performance of Device B4. (V_{GS} = 0 V.)

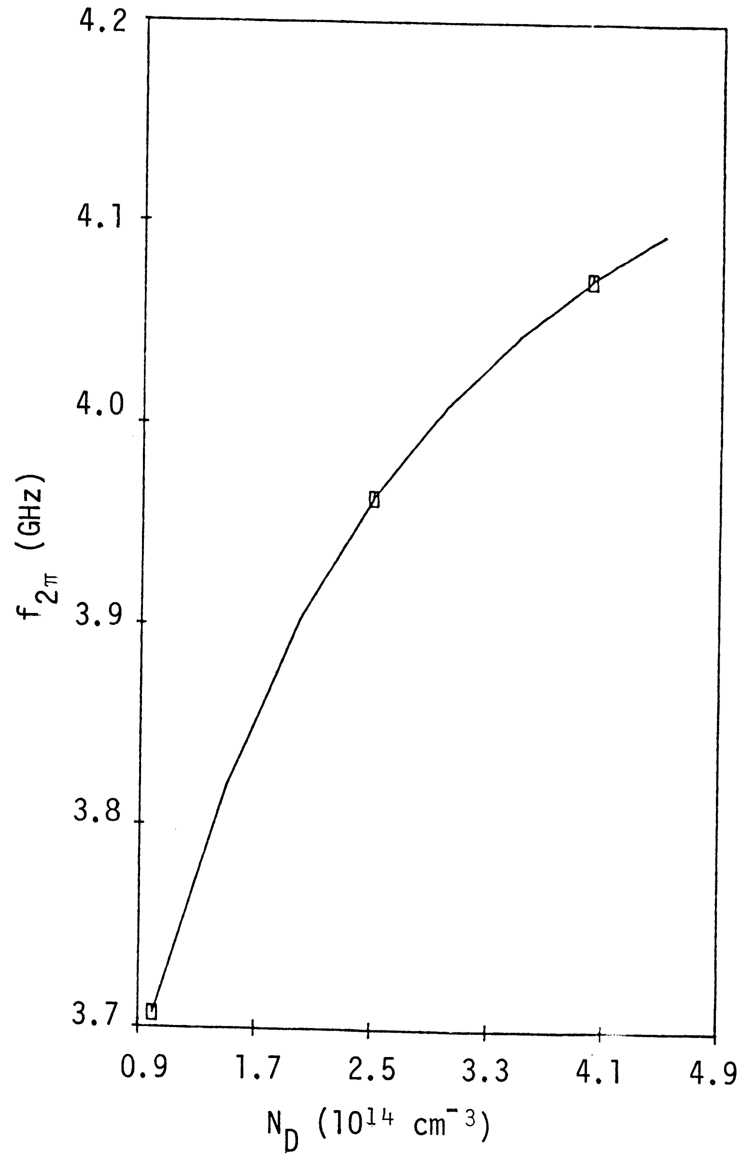


(b) The cut-off frequency, f_T.

Fig. 4.16 The Transit-Time Effect on the Small-Signal Device Performance of Device B4. (V_{GS} = 0 V.)

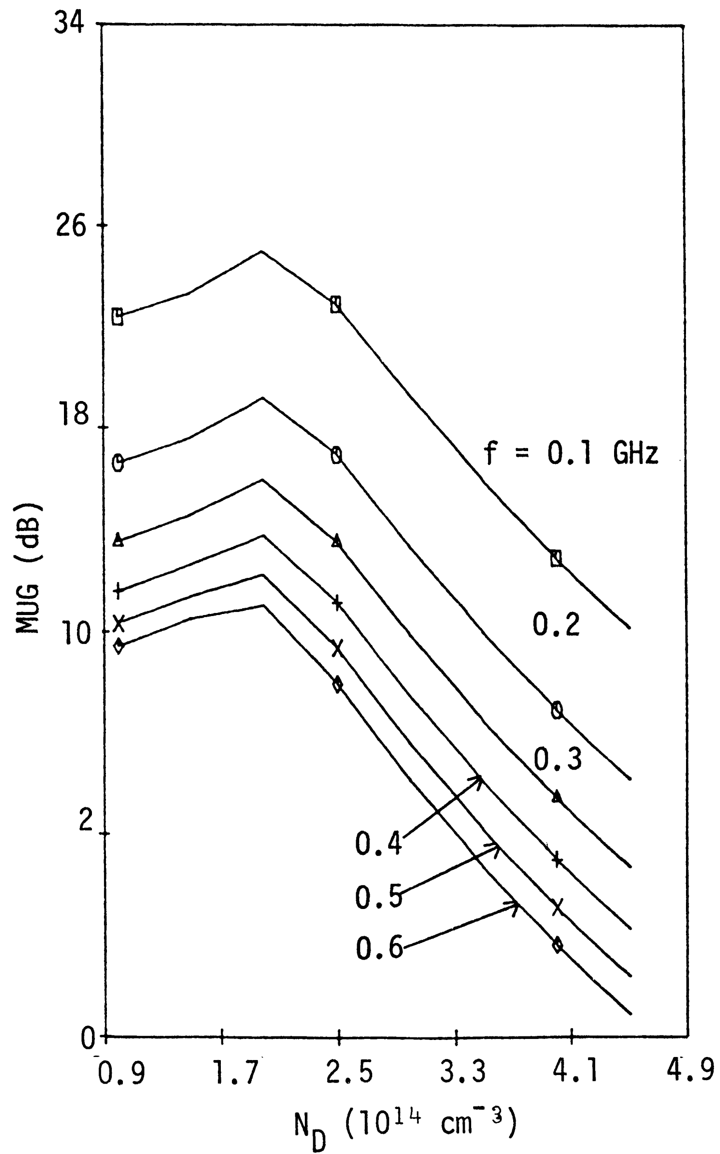
The effect of the channel doping concentration on the performance of the devices is shown in Fig. 4.17. The $f_{2\pi}$ increases with increasing channel doping concentration because the size of the device is fixed. Increasing the impurity concentration increases the electric field in the depleted channel and, as a result, the transit time decreases. The maximum available gain (MAG) and the maximum unilateral gain (MUG) decrease with the impurity concentration. On the other hand, the noise measure, M, increases with N_D. The rise in M is due to the degradation of MAG at high impurity concentrations, and not due to a rise of the noise figure. In Fig. 4.17(d), f_T decreases with N_D unlike that of $f_{2\pi}$. In this case, the upper frequency limit of the device is determined by the unity current gain because the transit time effect is negligible.

4.6.2 SIT Devices. The $f_{2\pi}$, MAG, MUG, f_T, noise figure and the noise measure are shown in Fig. 4.18 as a function of the dc bias, V_{DS}. An analysis of Fig. 4.18 indicates that $f_{2\pi}$ increases with V_{DS} up to 30 V. For V_{DS} in excess of 30 V, $f_{2\pi}$ degrades due to the electric field dependence of the GaAs carrier velocity. The MAG, MUG and f_T increase, with V_{DS} as in the case of the GFC-BARITT device. The noise figure and noise measure decrease with V_{DS}. The frequency dependence of these parameters follow the pattern of the GFC-BARITT devices given in Section 4.6.1. As can be seen from Figs. 4.17(a) and 4.18(a), the $f_{2\pi}$ of Si SIT devices does not vary in the same manner as $f_{2\pi}$ for GaAs devices.



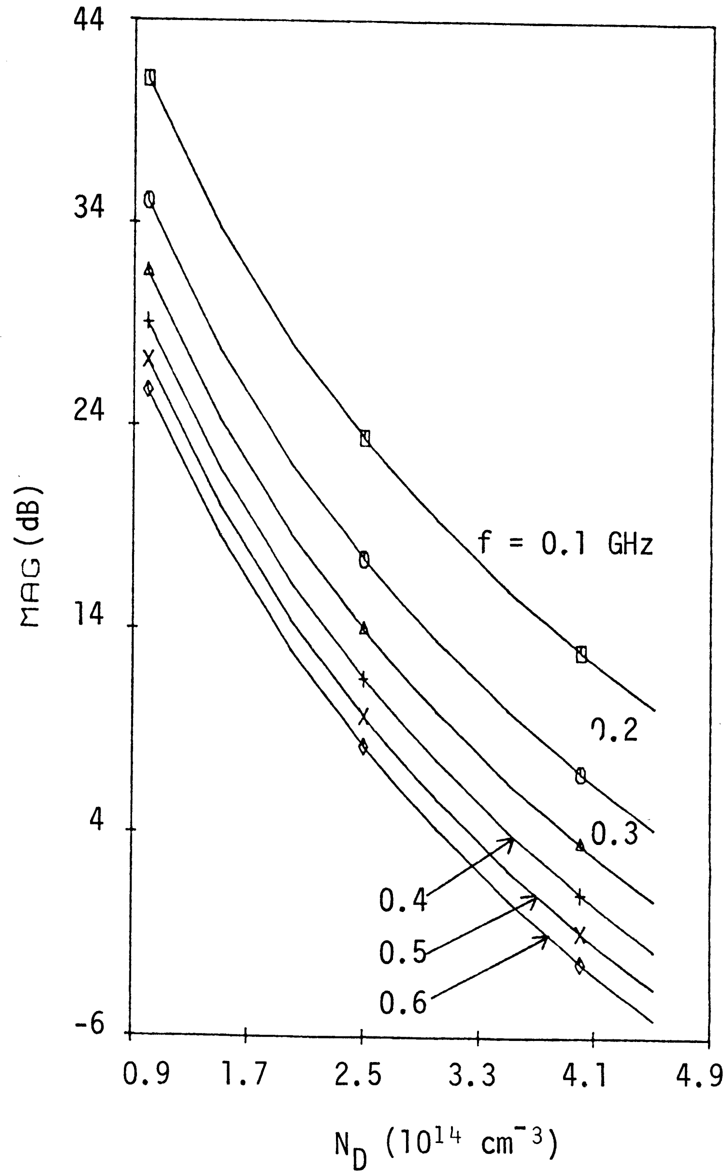
(a) The 360-degree phase frequency, $f_{2\pi}$.

Fig. 4.17 The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel Doping. (V_{GS} = 2.0 V.)



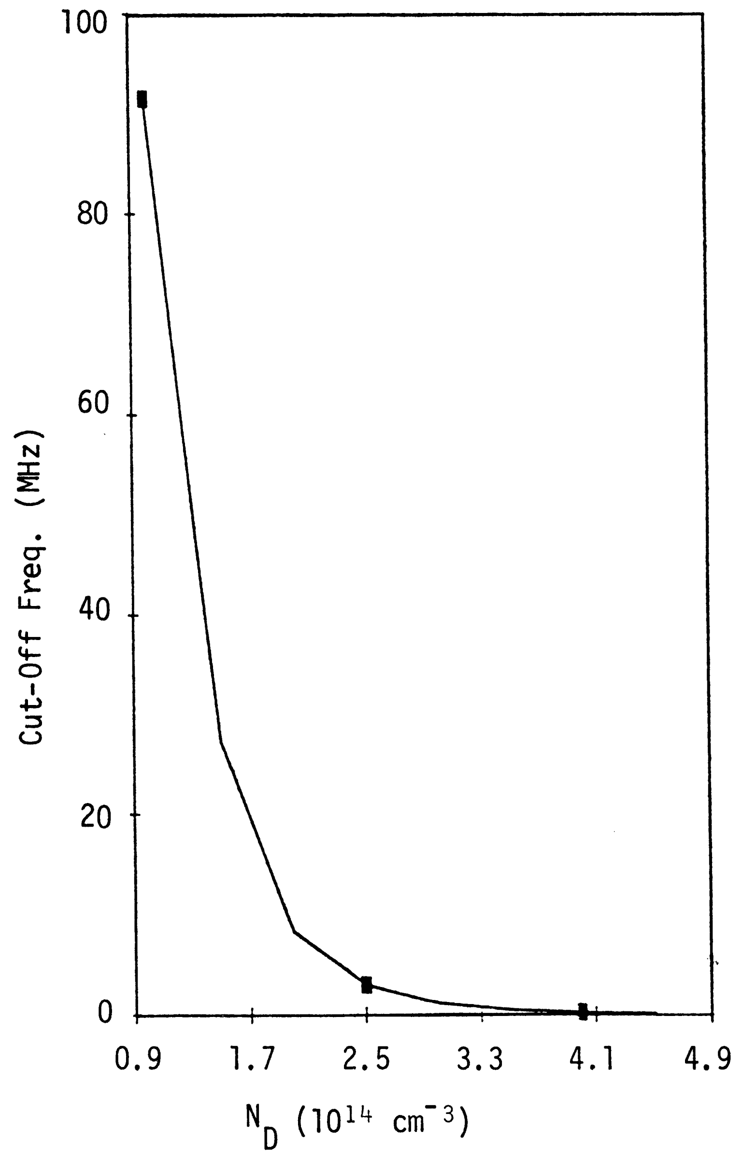
(b) The MUG.

Fig. 4.17 The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel Doping at Different Frequencies.



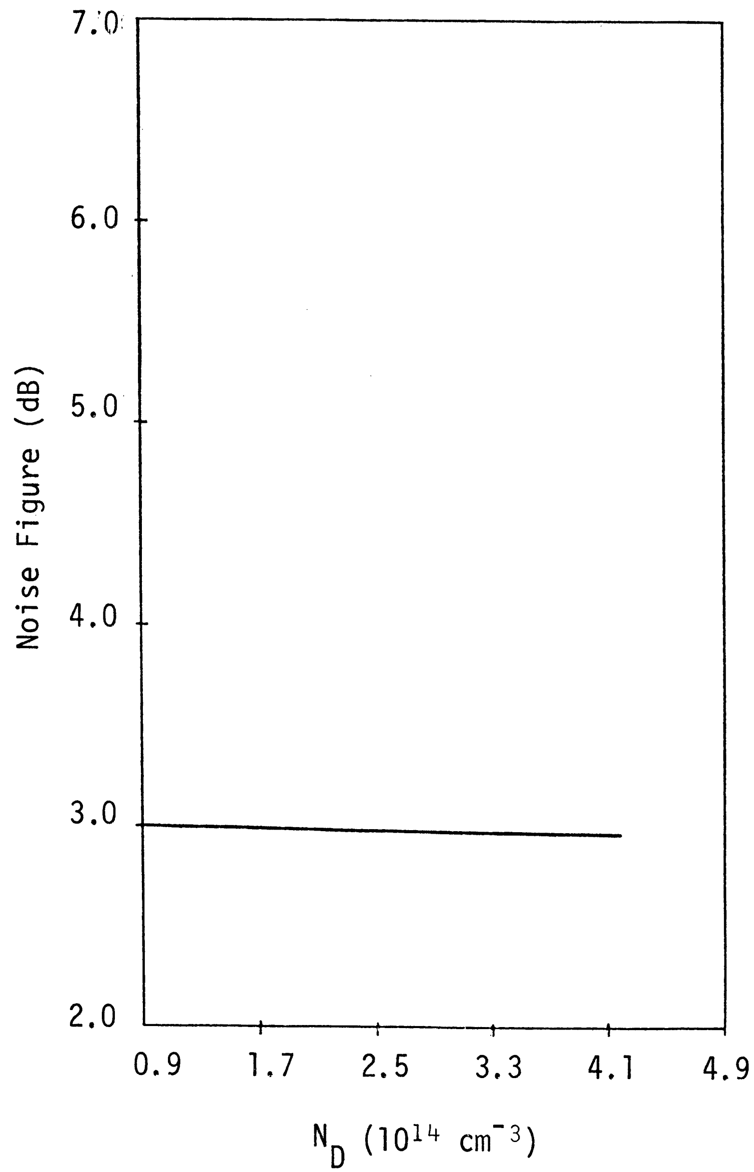
(c) The MAG.

Fig. 4.17 The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel Doping at Different Frequencies.



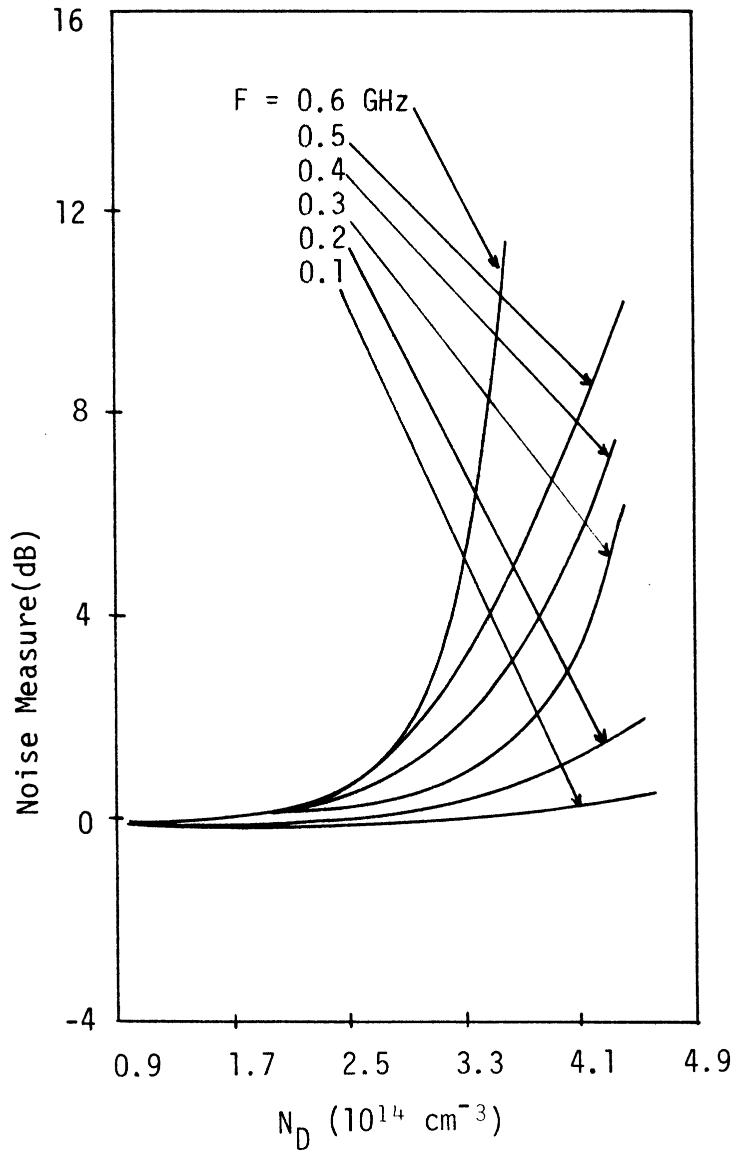
(d) The cut-off frequency.

Fig. 4.17 The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel Doping. (V_{GS} = -2.0 V and V_{DS} = ΔV_{DS} + V_{PT}.)



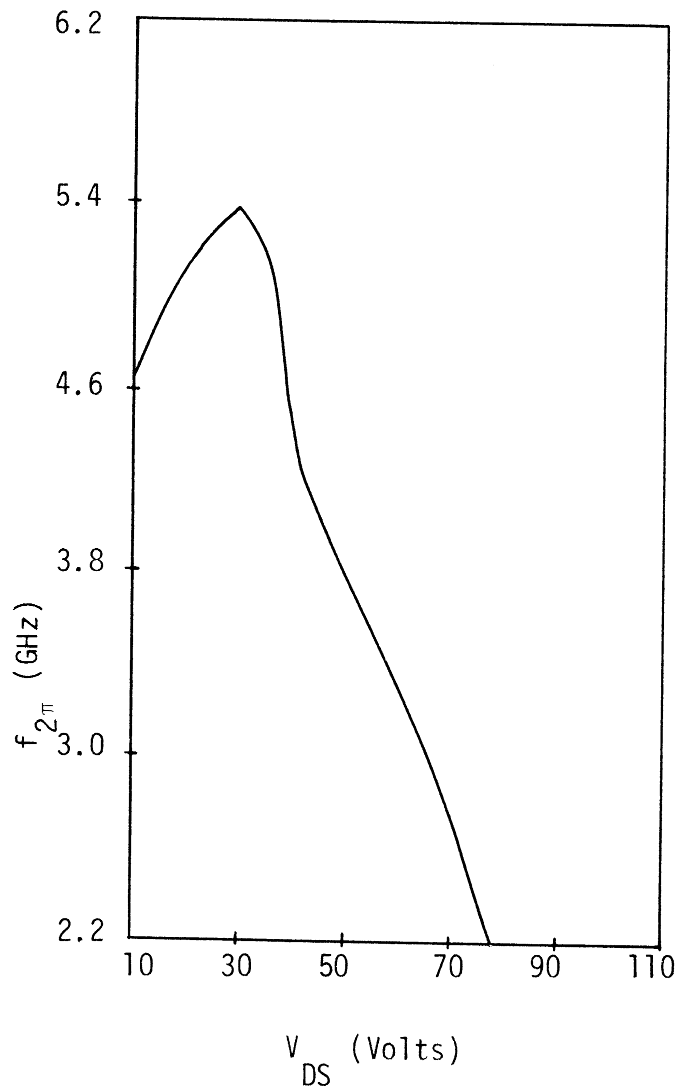
(e) The noise figure.

Fig. 4.17 The Small-Signal Performance of aGFC-BARITT Device, B1, as a Function of the Channel Doping.



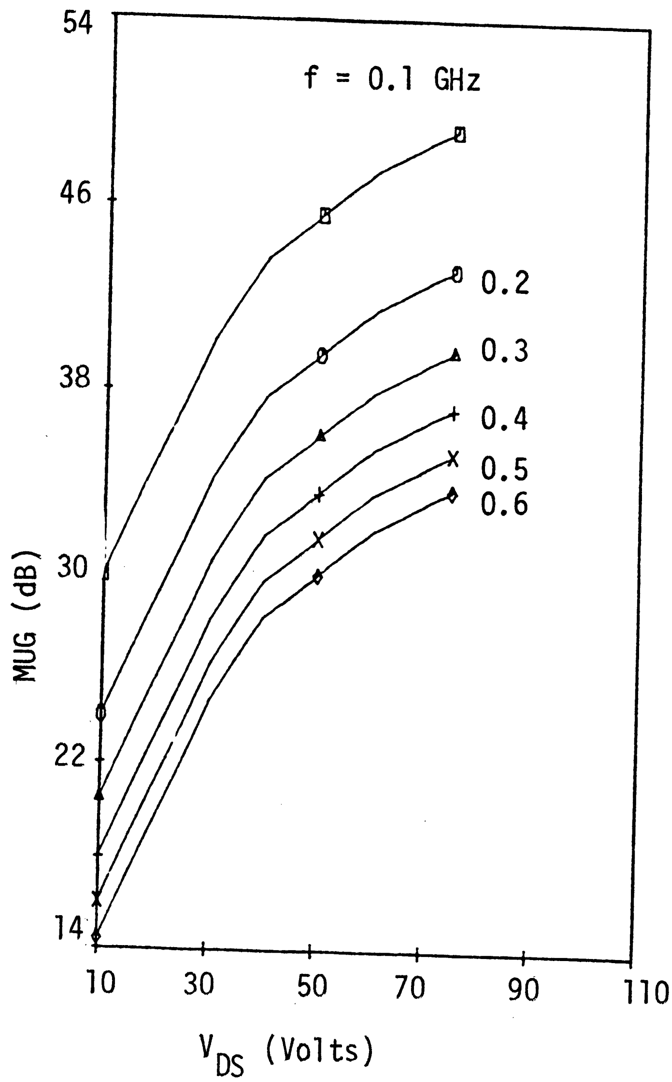
(f) The noise measure.

Fig. 4.17 The Small-Signal Performance of a GFC-BARITT Device, B1, as a Function of Channel Doping at Different Frequencies.



(a) The $f_{2\pi}$.

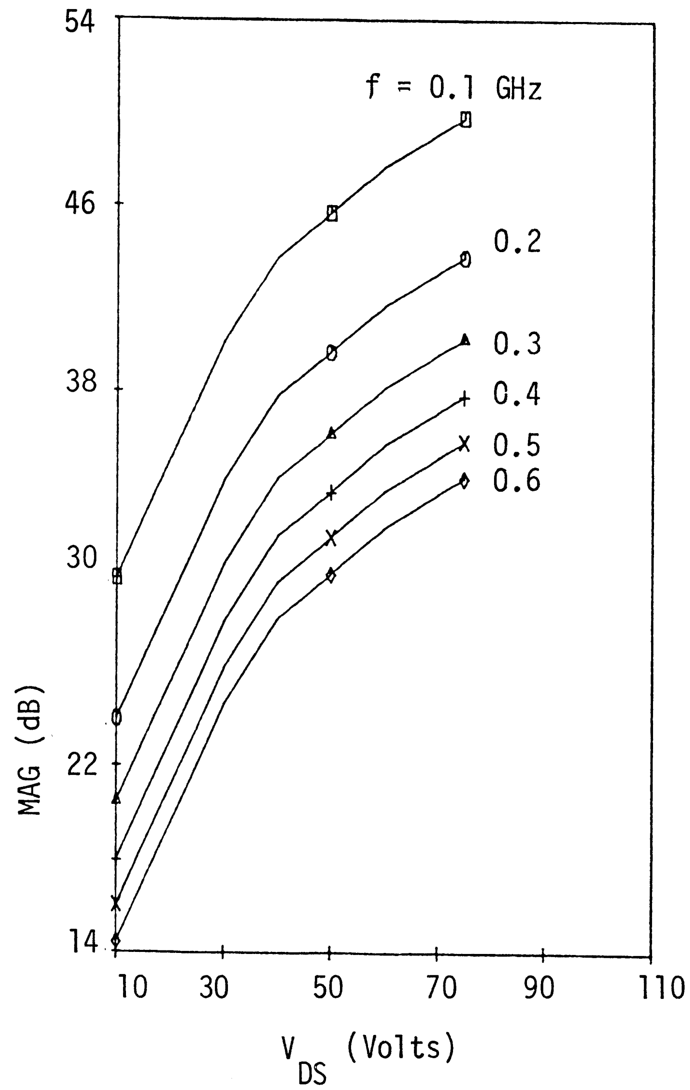
Fig. 4.18 The Small-Signal Performance of a GaAs SIT, S6 as a Function of V_{DS}. (V_{GS} = 0 V)



(b) The MUG.

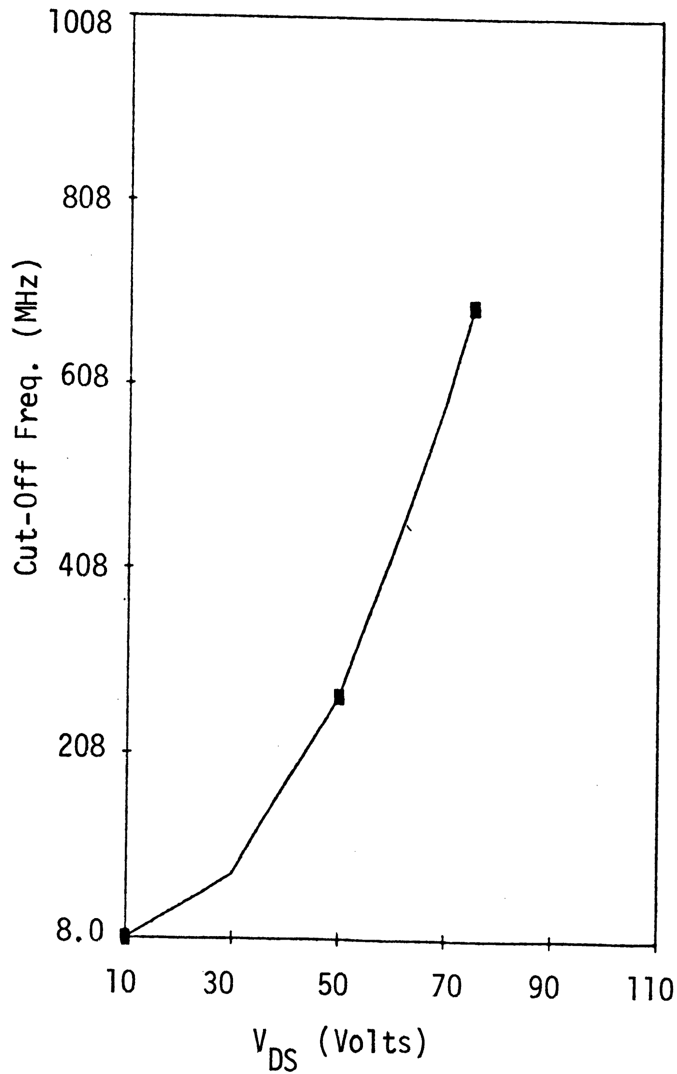
Fig. 4.18 The Small-Signal Performance of a GaAs SIT, S6.

(V_{GS} = 0 V)



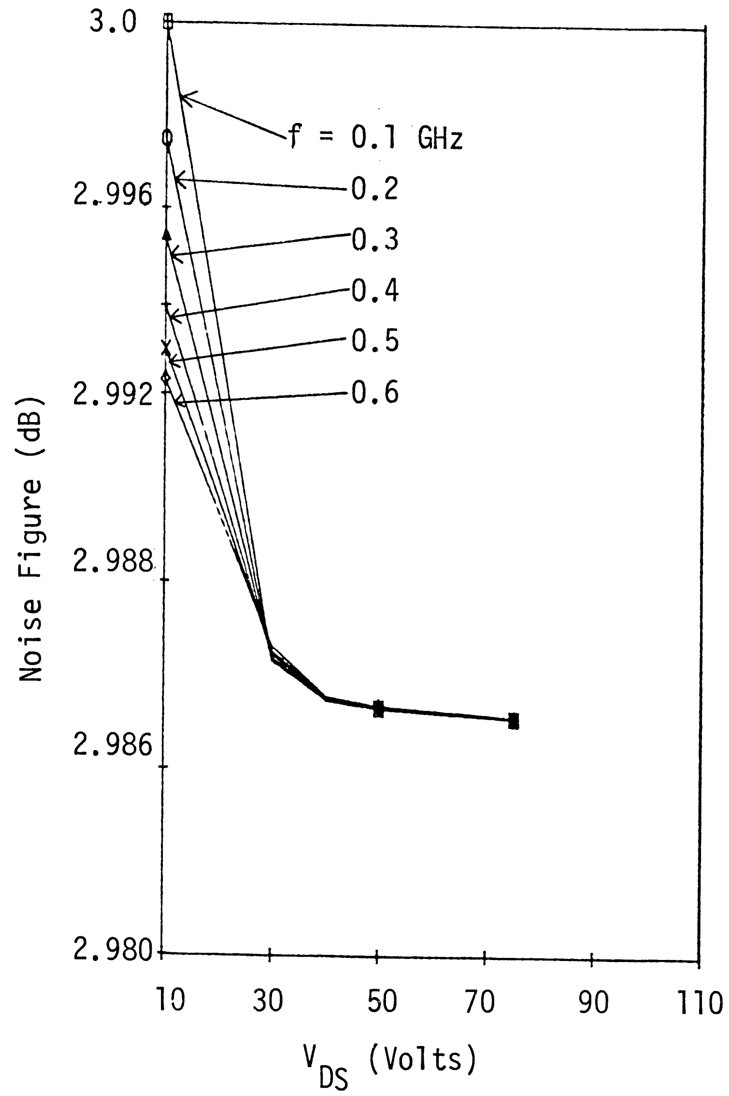
(c) The MAG.

Fig. 4.18 The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V.)



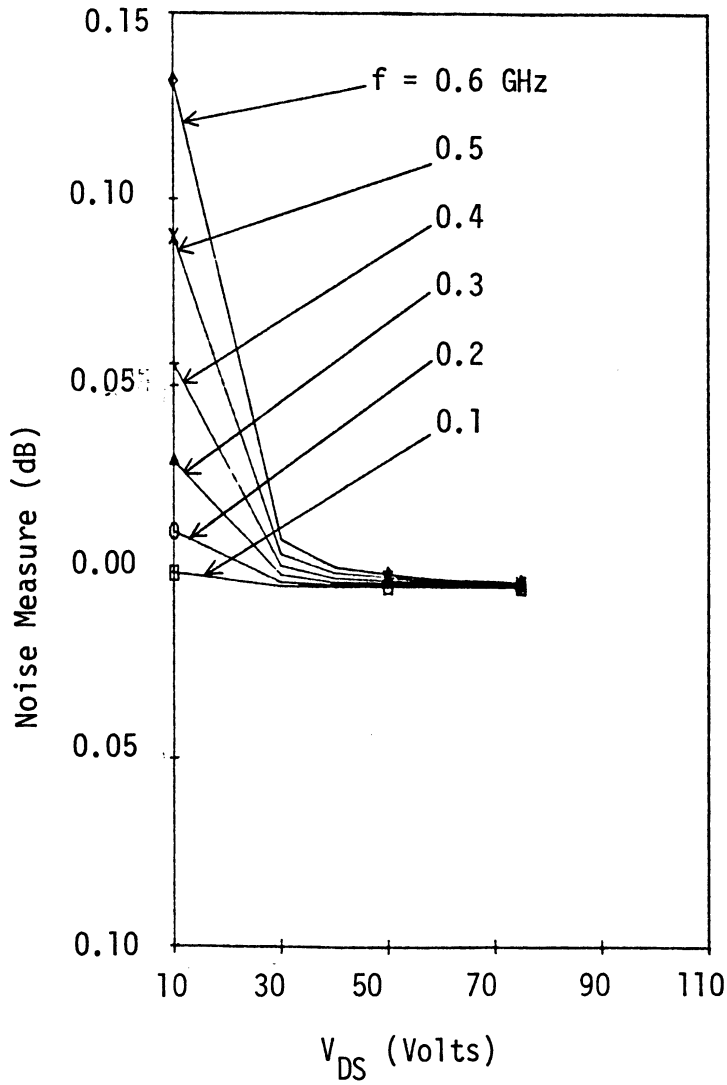
(d) The f_T.

Fig. 4.18 The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V)



(e) The Noise Figure.

Fig. 4.18 The Small-Signal Performance of a GaAs SIT, S6. (V_{GS}= 0 V)



(f) The Noise Measure.

Fig. 4.18 The Small-Signal Performance of a GaAs SIT, S6. (V_{GS} = 0 V)

There is a significant difference in the performance variation of a SIT and a GFC-BARITT device with impurity concentration. In Fig. 4.19, it is seen that the $f_{2\pi}$, MAG, MUG and f_T rise with V_{DS}. However, the noise figure, F, and measure, M, decreased with N_D due to an increase in the gain.

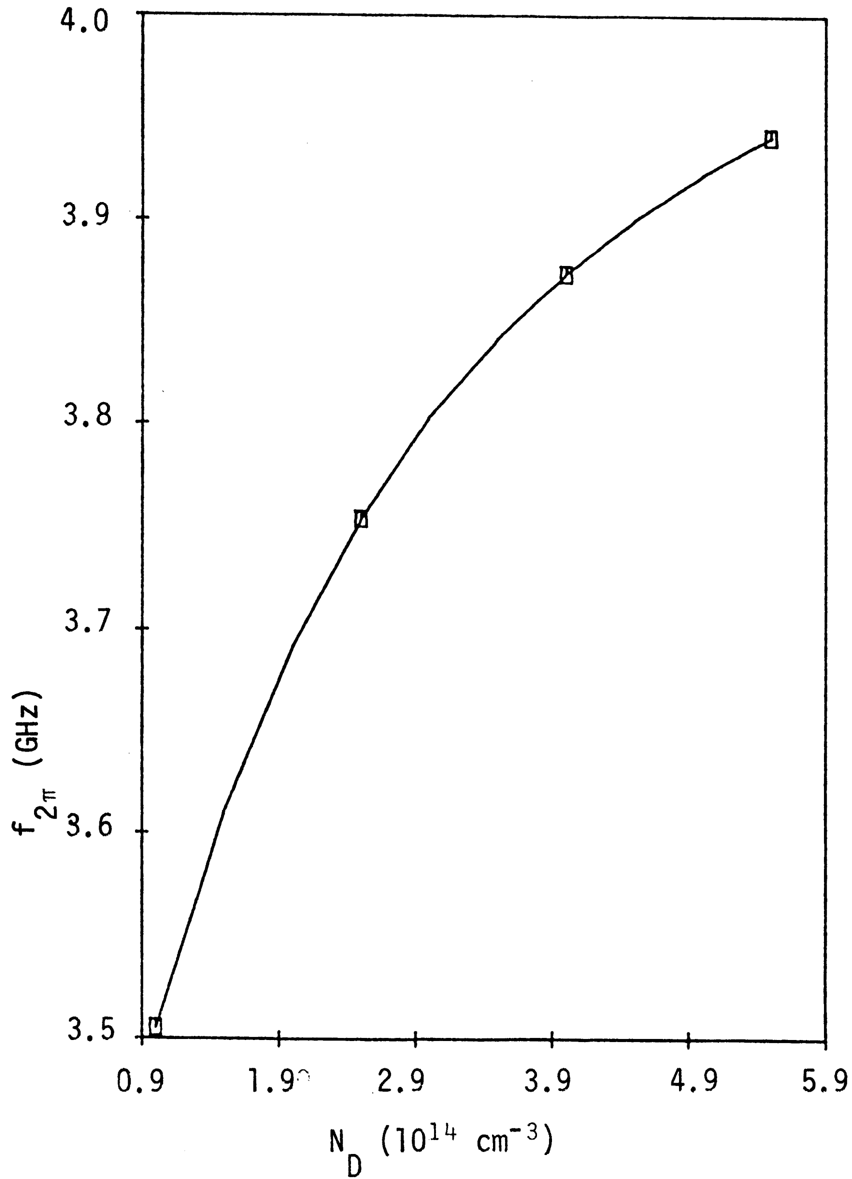
The results of the small signal performance of the TTPT devices can be summarized as follows:

(i) The MAG, MUG and f_T of the minority carrier injection type TTPT devices decrease with channel doping concentration at fixed dc bias voltages, but the $f_{2\pi}$ and the noise measure rise with it for fixed device bias and geometry. This is because increasing impurity concentration lowers the carrier injection which results in a low transconductance.

(ii) On the other hand, the MAG, MUG, $f_{2\pi}$ and f_T increase with N_D for Si majority carrier injection TTPT devices. The noise measure is lowered however due to the increasing MAG.

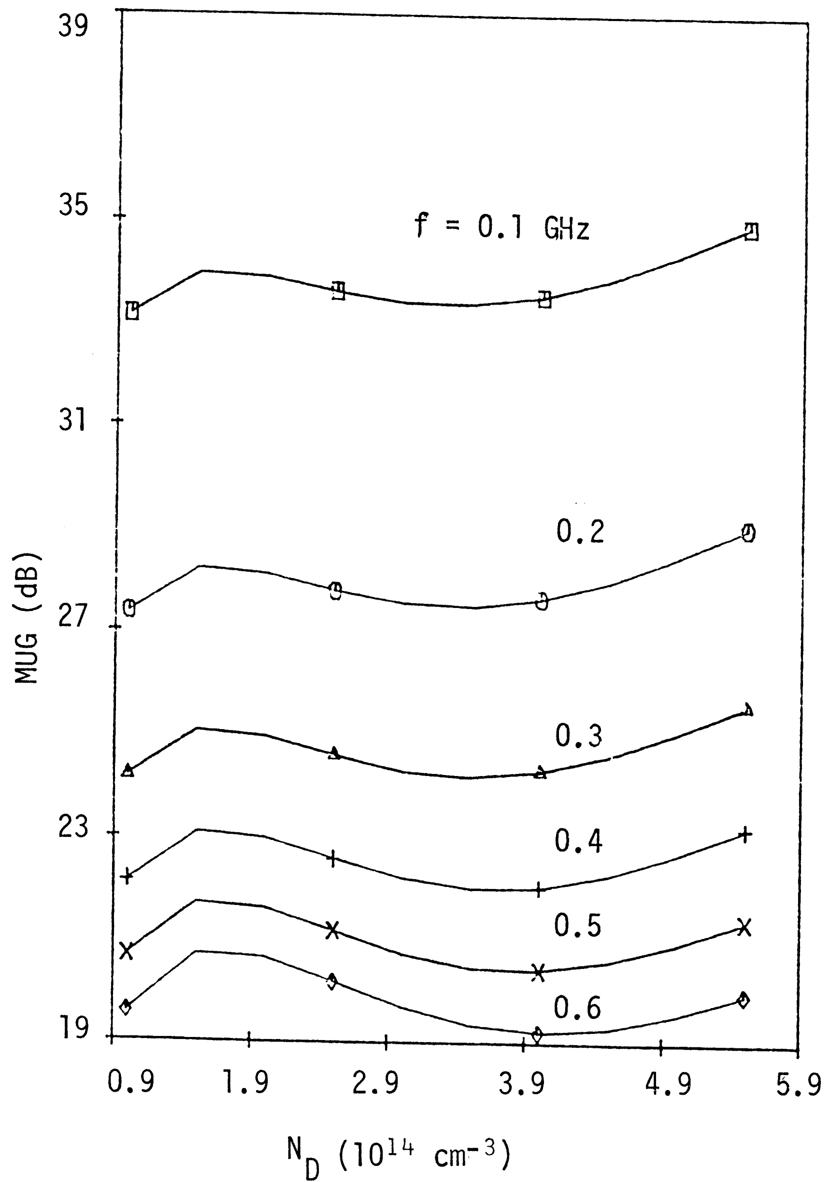
(iii) A higher dc bias voltage for both minority and majority carrier injection type TTPT devices results in a higher MAG, MUG, $f_{2\pi}$ and f_T, but lower noise measure. The improvement in the small signal device properties with dc bias does not continue indefinitely, carrier storage at high injection level limits the device performance. The variation of $f_{2\pi}$ of the III-V compound semiconductor SIT device as a function of V_{DS} follows the drift velocity variation as a function of the electric field.

(iv) The MAG and MUG decrease, but the noise figure and noise measure increase with the increasing frequency of operation.



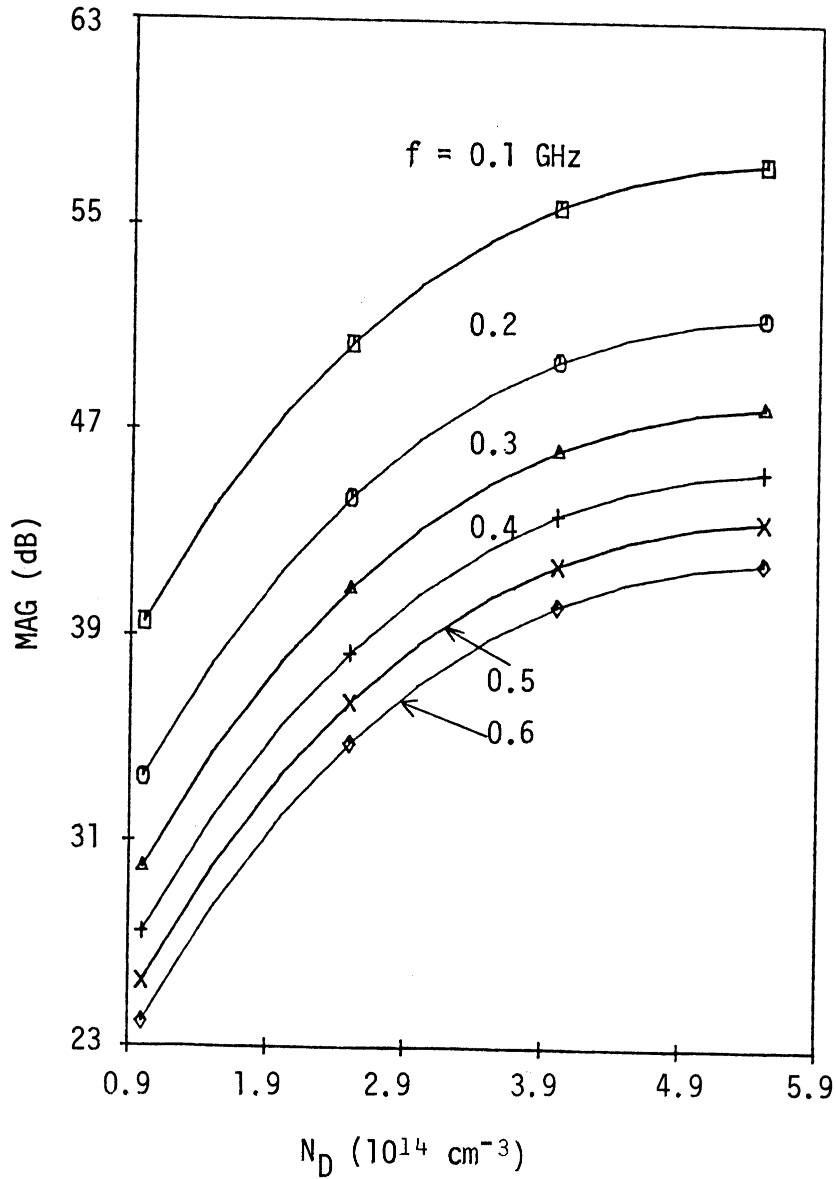
(a) The $f_{2\pi}$.

Fig. 4.19 The Small-Signal Performance of a Si SIT, S2, as a Function of Channel Doping, N_D. ($V_{DS} = V_{PT}$ + 8 V and V_{GS} = -3 V.)



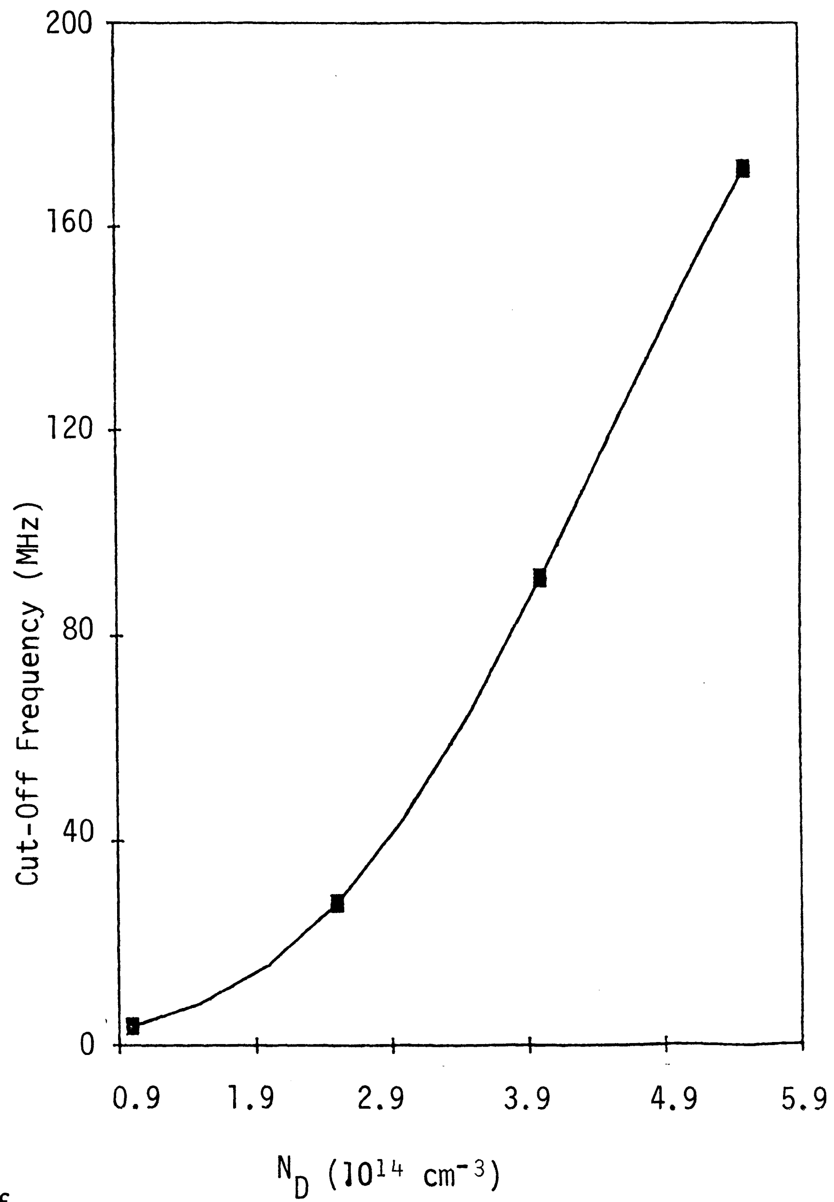
(b) The MUG.

Fig. 4.19 The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping, N_D at Different Frequencies. (V_{DS} = V_{PT} + 8 V and V_{GS} = -3 V.)



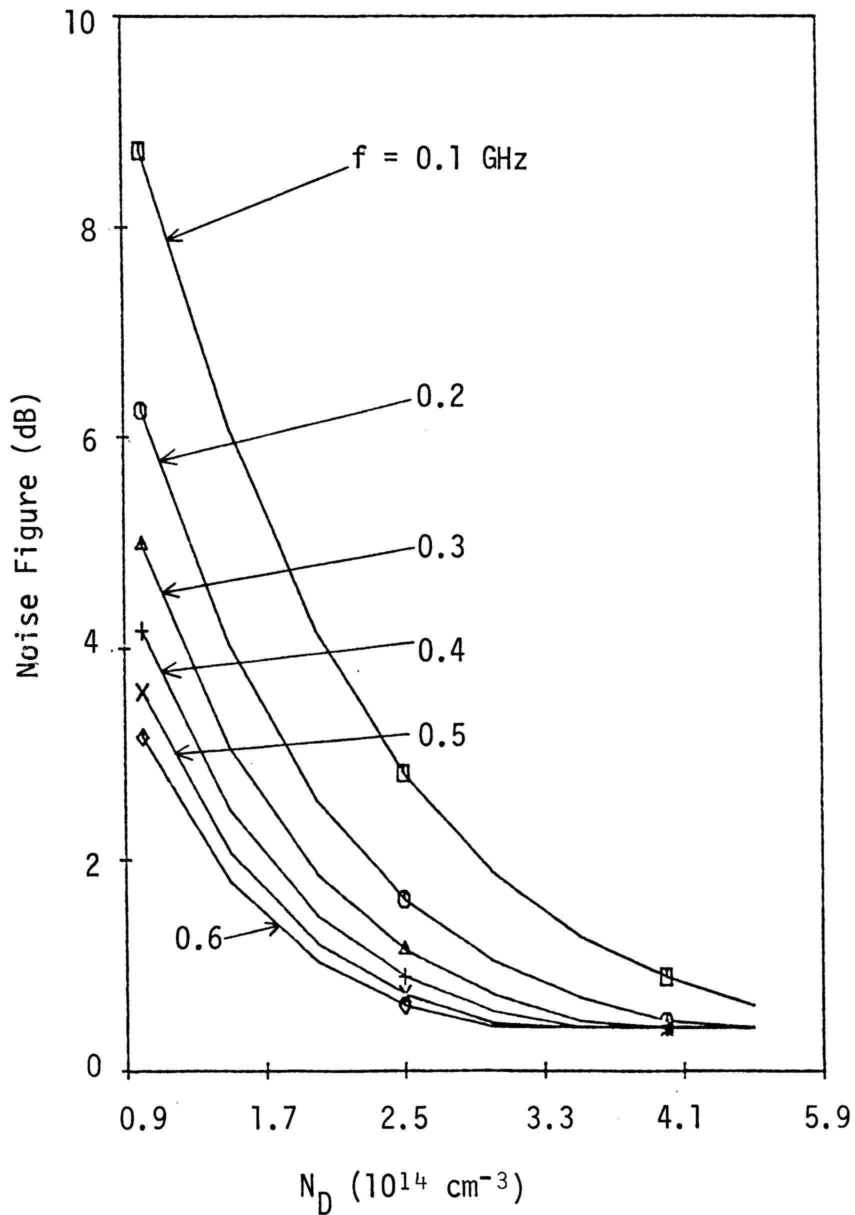
(c) The MAG.

Fig. 4.19 The Small-Signal Performance of a Si SIT, S2 as a Function of the Channel Doping, N_D at Different Frequencies. ($V_{DS} = V_{PT} + 8$ V and $V_{GS} = -3$ V.)



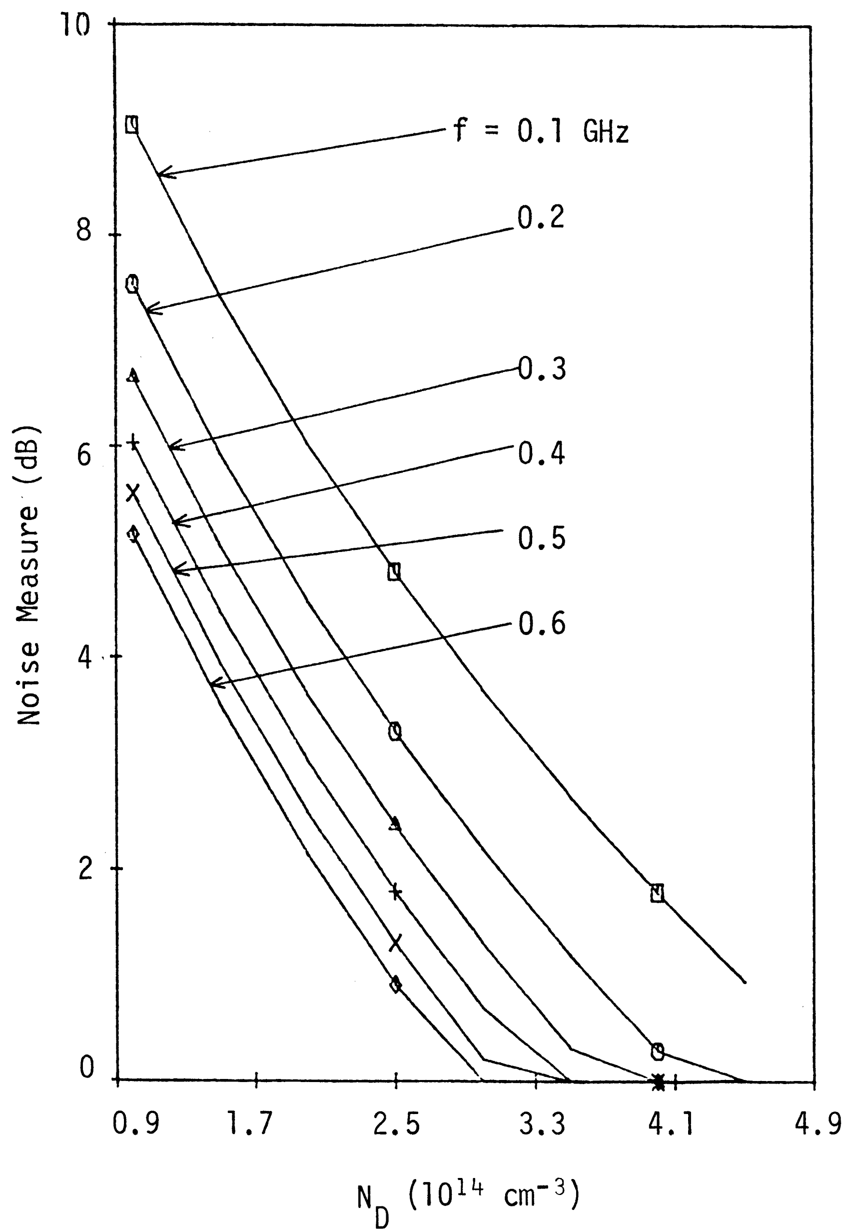
(d) The f_T.

Fig. 4.19 The Small-Signal Performance of a Si SIT, S2 as a Function of Channel Doping, N_D ($V_{DS} = V_{PT} + 8$ V and $V_{GS} = -3$ V).



(e) The Noise Figure.

Fig. 4.19 The Small-Signal Performance of a Si SIT, S2 as a Function of Channel Doping N_D at Different Frequencies. ($V_{DS} = V_{PT}$ + 8 V and V_{GS} = -3 V.)



(f) The Noise Measure.

Fig. 4.19 The Small-Signal Performance of a Si SIT, S2 as a Function of Channel Doping at Different Frequencies. ($V_{DS} = V_{PT}$ + 8 V and V_{GS} = -3 V.)

4.7 Large-Signal Performance

The large signal performance of TTPT devices is calculated in conjunction with the circuit shown in Fig. 4.20. The blocking capacitances, C_{in} and C_o are large so that, at the operating frequencies they will be short circuits. The y-parameters represent the average device response within a period. The input and output admittances of the device are given in Eq. 4.20 and 4.21, respectively:

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_L} \tag{4.20}$$

and

$$Y_o = Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_S} , \tag{4.21}$$

where Y_L is the load and Y_S is the source, admittances. These expressions were given originally in Reference [40]. For inherent stability of the amplifier, the real part of the input and output admittances must be positive.

The elements of large-signal equivalent circuit of a device vary with the input signal and the resulting output signal. Device and circuit interaction makes it very difficult to obtain a large signal model for the solid state electronics devices in general. In some cases, the large signal characteristics of a device are directly obtained from a device simulation [14], [36]. This is, however, a very expansive and complicated way. It is almost impossible to solve the device equation numerically for more than two-dimensional cases.

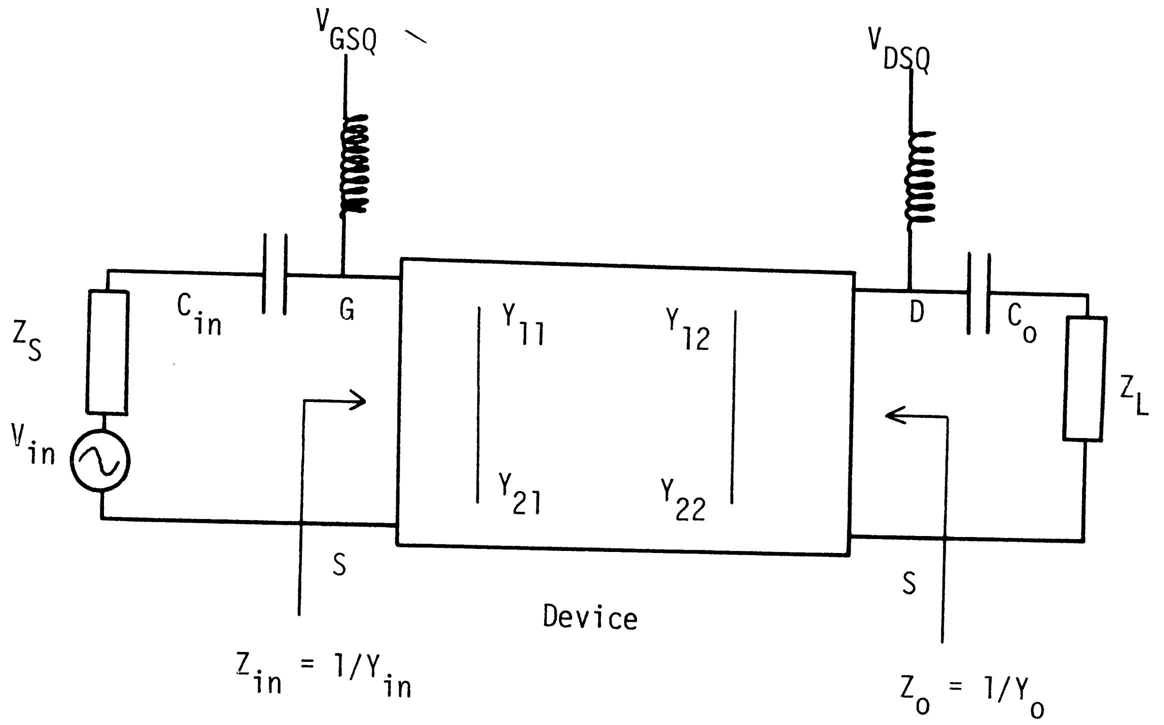


Fig. 4.20 A Large-Signal Amplifier Circuit.

There are some semi-empirical large signal models for GaAs FETs to reduce iterative circuit design of the power amplifiers and oscillators [38], [39]. In one of these models [38], expressions for an instantaneous equivalent circuit in terms of terminal voltages have been established from the measured bias dependence of the small signal S-parameters. The major drawback of this model is that it requires extensive measurement of the S-parameters at all the possible dc bias conditions that the RF signal can sweep. Also, S-parameter measurements are not easy.

Another model [39] is the derivation of RF equivalent circuit elements in terms of signal voltages, based on static characteristics of an FET such as dc drain current voltage curves and the RF input voltage. The major drawback of this model is that it requires iterative solution of the nonlinear equivalent circuit elements and the output RF voltage. The parameters all of which are used in the latest model, are easy to measure. The large-signal model based on static FET characteristics can be described as follows:

(i) Input RF voltage, $V_{in}(t)$ and Y_L were known.

(ii) Initial values for nonlinear elements (g_m, g_{ds}, and c_{gs}) were assumed.

(iii) The parasitic inductances and capacitance, C_{gd}, C_{ds} and the contact resistances were assumed to be independent from variations of RF voltages.

(iv) Y_S and the output RF voltage, $V_o(t)$ and the phase difference between the input and the output voltages, were calculated from the known nonlinear elements and Y_L.

(v) Expressions for the nonlinear elements (g_m, g_{ds} and c_{gs}) were derived as the functions of $V_{in}(t)$, $V_o(t)$ and θ.

(vi) From the known $V_{in}(t)$, $V_o(t)$ and θ, the values of g_m, g_{ds} and C_{gs} were revised.

(vii) By using the revised values of the nonlinear elements, Y-parameters and the new values for $V_o(t)$ and θ were calculated which will again change the nonlinear element values. When this process converges, the equivalent circuit of GaAs FET is then obtained for given $V_{in}(t)$ and Y_L values.

(viii) The source admittance, Y_S was kept matched to the device input admittance as it varied with input power and Y_L. Finally, the input and output powers were calculated by using known terminal voltages, ($V_{in}(t)$, $V_o(t)$), Y_S and Y_L.

In the present study, a new method for the large-signal modelling of the solid state electronics devices have been proposed to overcome some of the problems of large signal modelling such as S-parameter measurements and/or time consuming, iterative computation. The method can be summarized as follows:

(i) $V_{in}(t)$ is known, $V_{in}(t) = V_{gs} \sin \omega t$.

(ii) $V_o(t)$ is also assumed known, and its magnitude is taken as a fraction of dc voltage, V_{DSQ}

$$V_o(t) = kV_{DSQ} \sin(\omega t + \theta) \quad ,$$

where k is a fraction of one, $0 < k < 1.0$ and θ is the phase angle.

(iii) Any reasonable angle value can be assigned for θ, but it is assumed that

$$\theta = 2\pi f \tau_d ,$$

where f is the frequency of operation and τ_d is the drift-transit-time. Figure 4.21 illustrates the phase relation among the drain-source RF current, $I_{ds}(t)$, $V_o(t)$ and $V_{in}(t)$.

(iv) Instantaneous drain-source current, $I_{ds}(t)$ and nonlinear equivalent circuit elements are calculated at the fundamental frequency of operation, since the input and the output RF voltages are known.

(v) The effective values of g_m, g_{ds}, c_{gs}, c_{gd} and c_{ds} are obtained, then Y-parameters of the device are obtained.

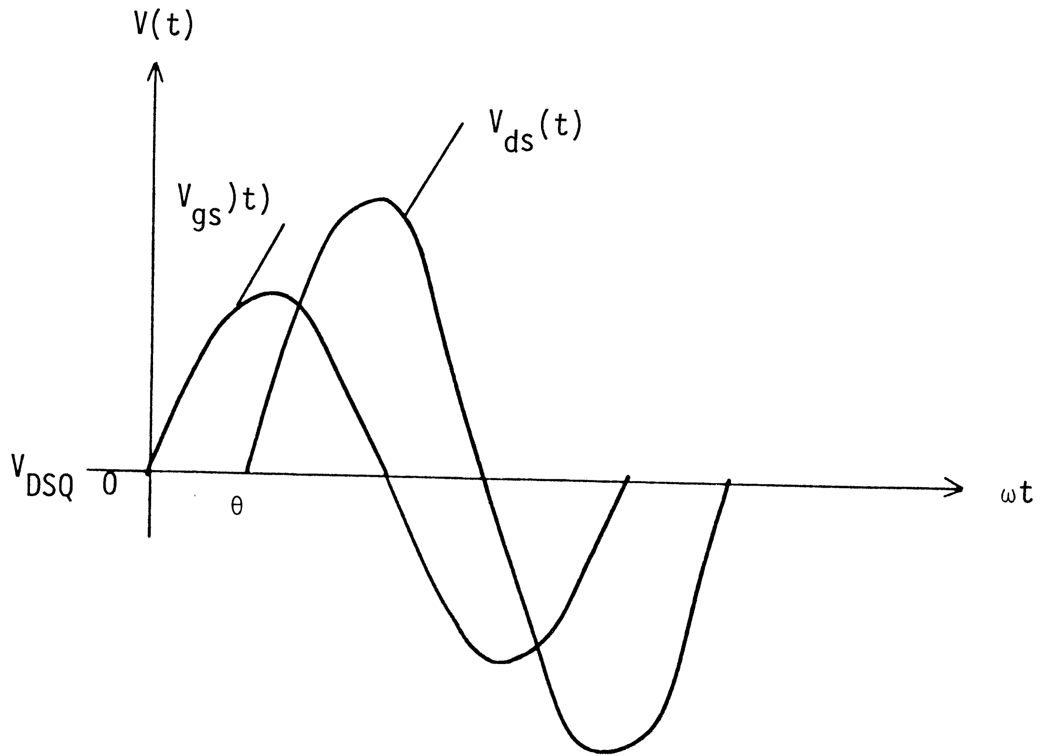
(vi) The real parts of the load and output admittances

$$\text{Real } (Y_L) + \text{Real}(Y_o) = \frac{I_{eff}}{kV_{DSQ}} ,$$

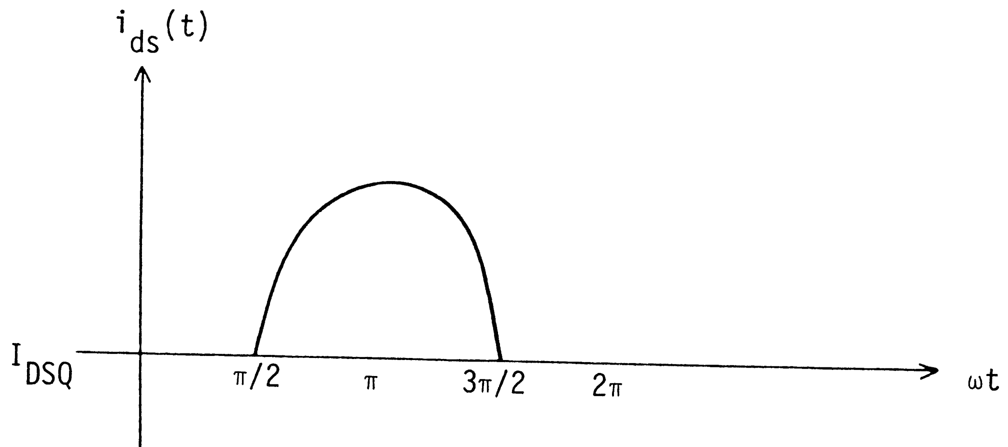
where I_{eff} is the effective value of the drain source current $i_{ds}(t)$.

(vii) The source admittance, Y_S, which is slightly mismatching input admittance, Y_{in}. Y_{in} is given by Eq. (4.20). Ideally, Y_S should be conjugate matched to Y_{in}. Instead

$$Y_S = \text{conjugate}\left(Y_{11} - \frac{Y_{12}Y_{21}}{(\text{Real } Y_{22} + 0.5\ I_{eff}/kV_{DSQ})}\right) .$$



(a) The input, $V_{gs}(t)$ and output, $V_{ds}(t)$.



(b) The current, I_{ds}.

Fig. 4.21 The Current and Voltage Waveforms under Large-Signal Conditions.

(viii) From known Y_S, the output admittance, Y_o can be obtained from Eq. (4.21).

(ix) Finally, Y_L can be determined by assuming a conjugate match of the imaginary parts of Y_L and Y_o

$$Y_L = \frac{I_{eff}}{kV_{DSQ}} - Y_o \quad . \tag{4.22}$$

(x) The input and output RF powers and the dc power dissipation can be calculated from known Y_S, Y_L, $V_{in}(t)$ and I_{eff}

$$P_o = I_{eff}^2/\mathrm{Real}(Y_L) \quad . \tag{4.23}$$

(xi) If the calcuated Y_L is not reasonable meaning if the real part of Eq. (4.22) is negative, then choose different values for the output RF voltage and repeat the steps from (i) to (x).

This approach eliminates the need fo the iterative solutions of the equivalent circuit parameters (C_{gm}, g_{ds}, C_{gs}, C_{dg}, and C_{ds}) of the device. In the present approach the RF terminal voltages $V_o(t)$ and $V_{in}(t)$ are assumed, then the device characteristics are estimated. Therefore, large-signal device characteristics can be calcualted without the use of the iterative computation method.

Summarized, the large-signal model is applicable to large-signal amplifier design utilizing various devices including FETs, TTPT devices and Bipolar Junction Transistors (BJTs). The main advantage of this approach is to relate the device physics directly to the circuit design. Therefore, the large-signal behavior of a device

can be used as a guideline for the actual design of an amplifier. As a result, the turnaround time of an actual circuit design may be shorter. Since the averages of the large signal effects on the device parameters are included, along with the various simplifying assumptions, the calculated results are expected to be guidelines for the actual circuit design. The calculated results will be much closer to the experimental results if the basic model is adequate, such as including the contact resistances and the various parasitic capacitances and inductances.

The large-signal circuit expressions are given in Chapter III. In the next section the large-signal power gain, collector efficiency and output power are given.

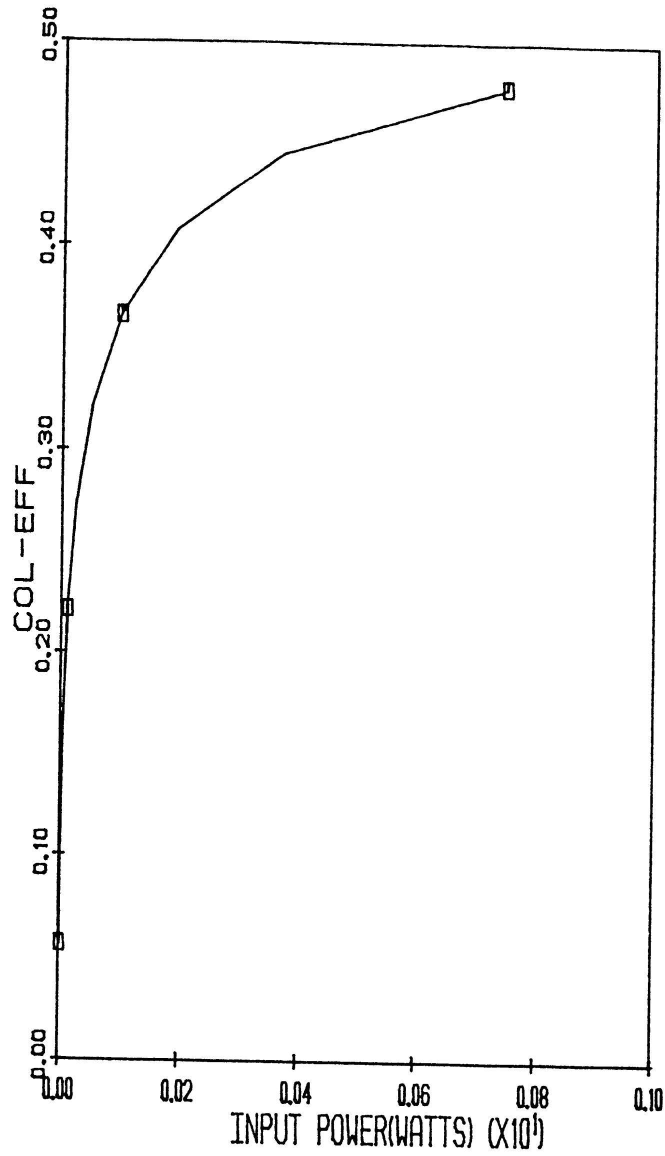
4.7.1 Results and Discussion of Large-Signal Operation. The large signal performance of the various devices has been investigated by using the model described in the preceding section. The collector efficiency, η_c, output power P_o and power gain G_p of the FET have been calculated as a function of the input power and frequency of the RF input signal.

The large signal performance of the FET is less sensitive to the output RF voltage $V_o(t)$, than to the input voltage, $V_{in}(t)$. On the other hand, the large-signal performance of the TTPT devices is equally sensitive to the output, $V_o(t)$ and input, $V_{in}(t)$ voltages. Any large-signal calculations of the TTPT devices must include the space charge effect of the injected carriers. Otherwise the results will be erroneous. Therefore, only the large-signal calculations of FETs are given.

The variation of the forward biasing voltage, V_F of a TTPT device as a function of the drain-source and the gate-source voltages must be obtained from the measured dc I-V characteristics. Then the calculated V_F values can be listed in a table or as a two-dimensional array with V_{GS} as it y-coordinate and V_{DS} as its x-coordinate. During the large-signal computations, the magnitude of $V_{GS}(t)$ and $V_{ds}(t)$ is obtained at each integration time interval, and then the corresponding V_F can be read directly from the V_F table.

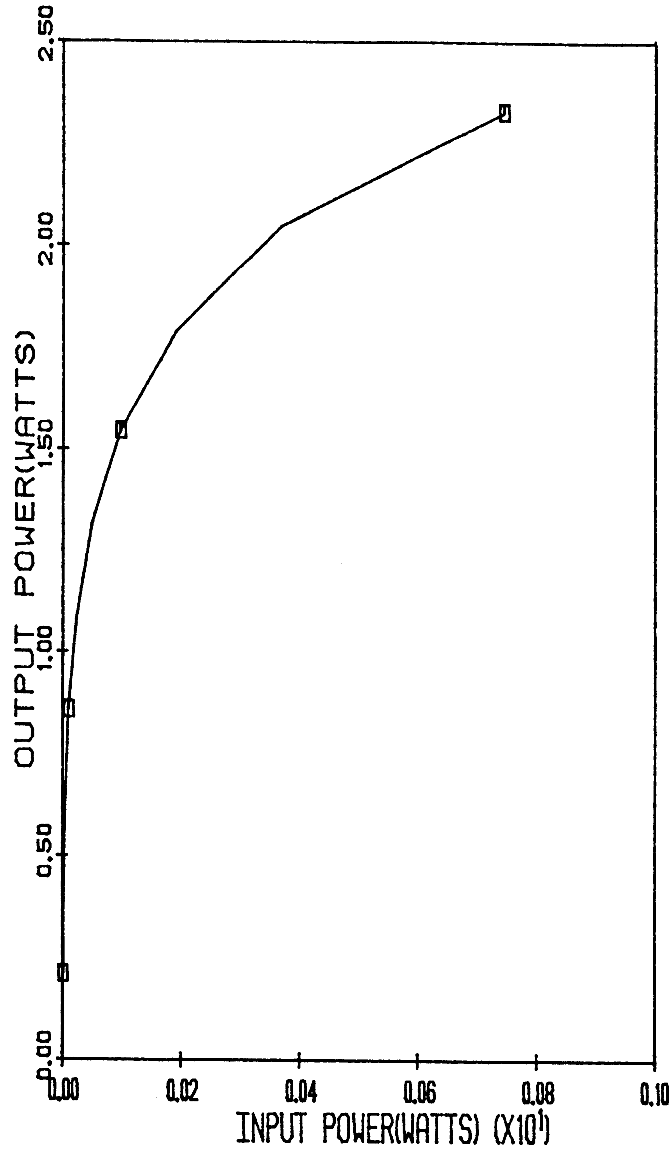
The large-signal model has been used to investigate the large-signal performance of various FETs. As a demonstration, the collector efficiency, the output power and the power gain of GaAs and InP FETs at an operating frequency of 5.0 GHz are shown in Fig. 4.22 and Fig. 4.23, respectively. The output power as seen in Fig. 4.22(b) or in Fig. 4.23(b) saturates with increasing input power. While the collector efficiency and the output power increase with input power, the power gain decreases with it. As it is predicted earlier in this chapter, InP FETs perform better than the GaAs FETs under small and large signal operating conditions. From the comparison of Fig. 4.22(b) and Fig. 4.23(b) it can be concluded that InP FETs give 30 percent higher output power than comparable GaAs FETs. The output power for the same size Si FET gives much lower output power as seen in Fig. 4.24. Also the power gain of the InP FET is the highest.

The η_c, P_o and G_p of an InP FET as a function of the operating frequency are shown in Fig. 4.25. In Fig. 4.25(a) the collector efficiency and in Fig. 4.25(b) the output power do not vary with frequency. The reason being that the large-signal model is responsible



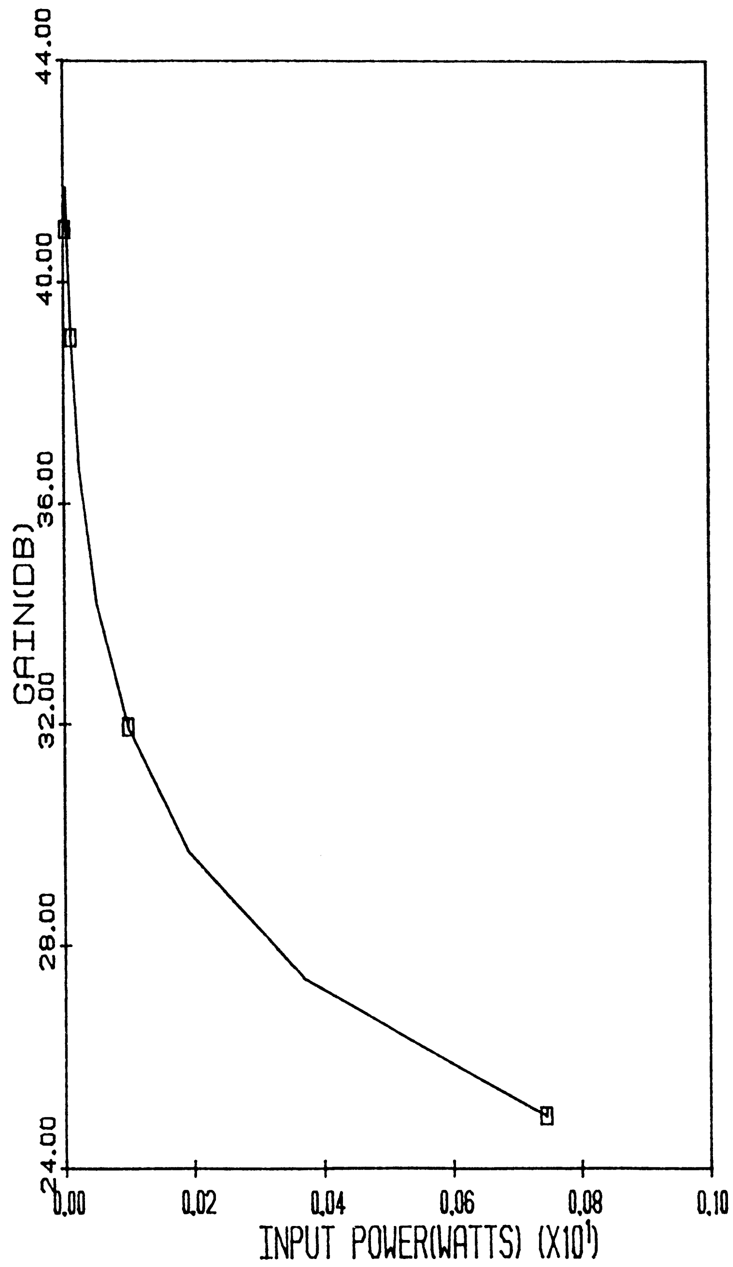
(a) Collector Efficiency.

Fig. 4.22 The Large-Signal Performance of a GaAs FET (Device S7) at 5.0 GHz.



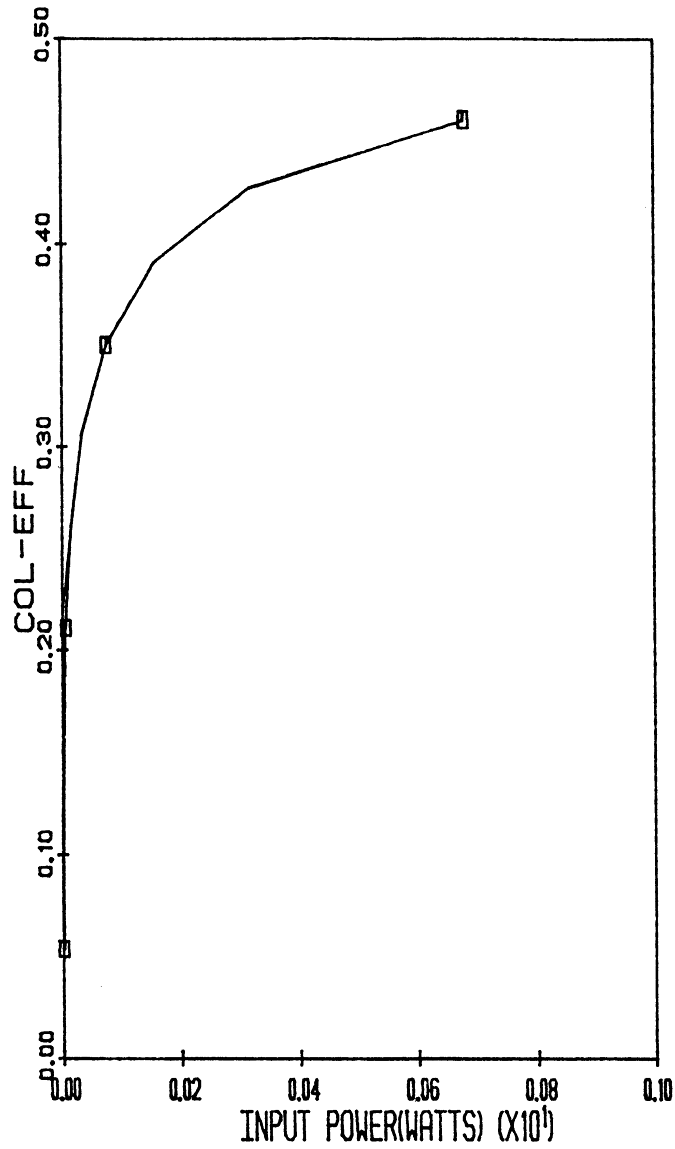
(b) Output Power.

Fig. 4.22 The Large-Signal Performance of a GaAs FET (Device S7) at 5.0 GHz.



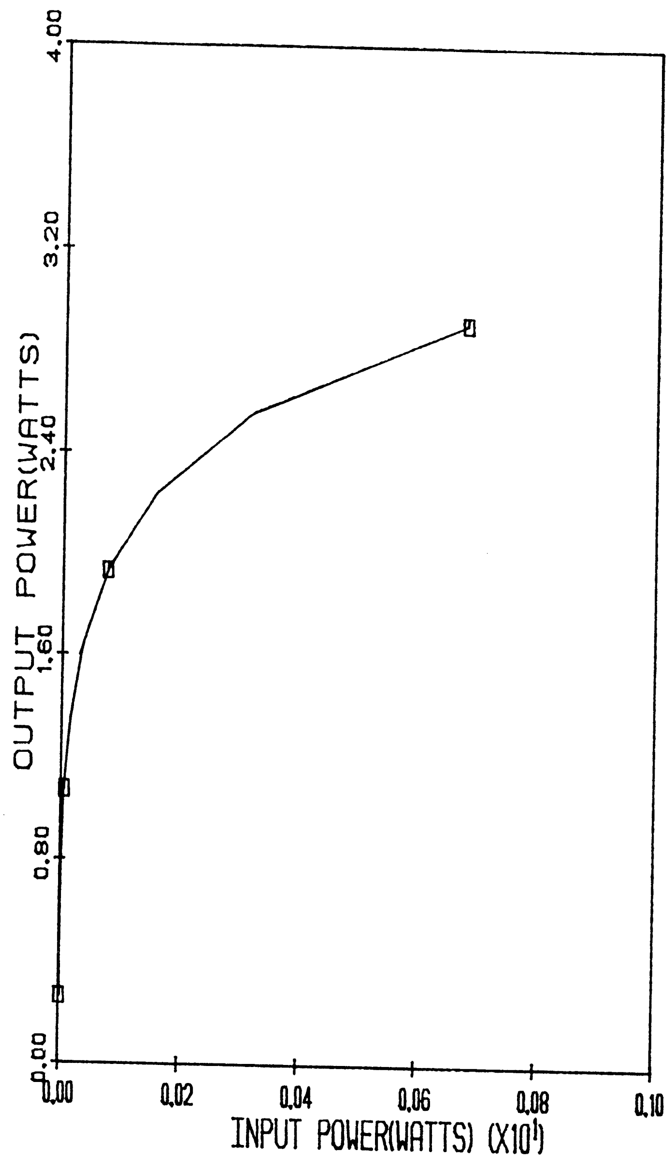
(c) Power Gain.

Fig. 4.22 The Large-Signal Performance of a GaAs FET (Device S7) at 5.0 GHz.



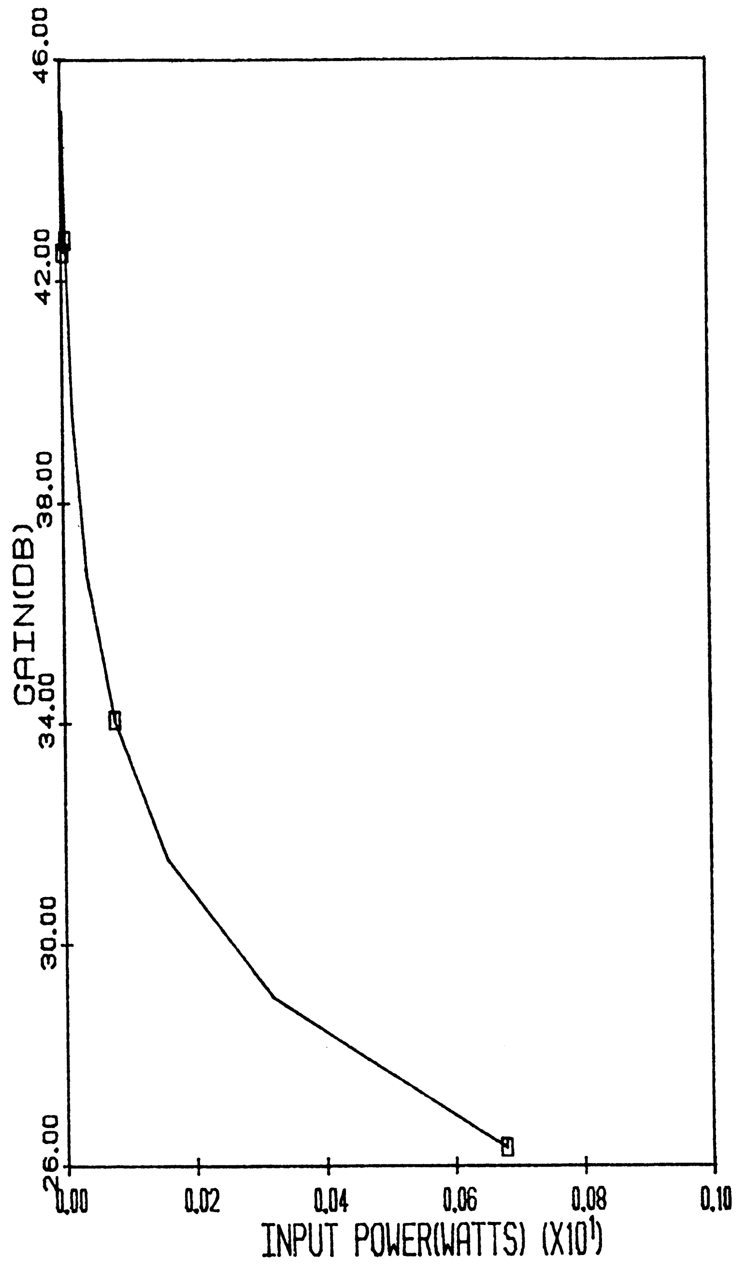
(a) Collector Efficiency.

Fig. 4.23 The Large-Signal Performance of an InP FET (Device S8) at 5.0 GHz.



(b) Output Power.

Fig. 4.23 The Large-Signal Performance of an InP FET (Device S8) at 5.0 GHz.



(c) Power Gain.

Fig. 4.23 The Large-Signal Performance of an InP FET (Device S8) at 5.0 GHz.

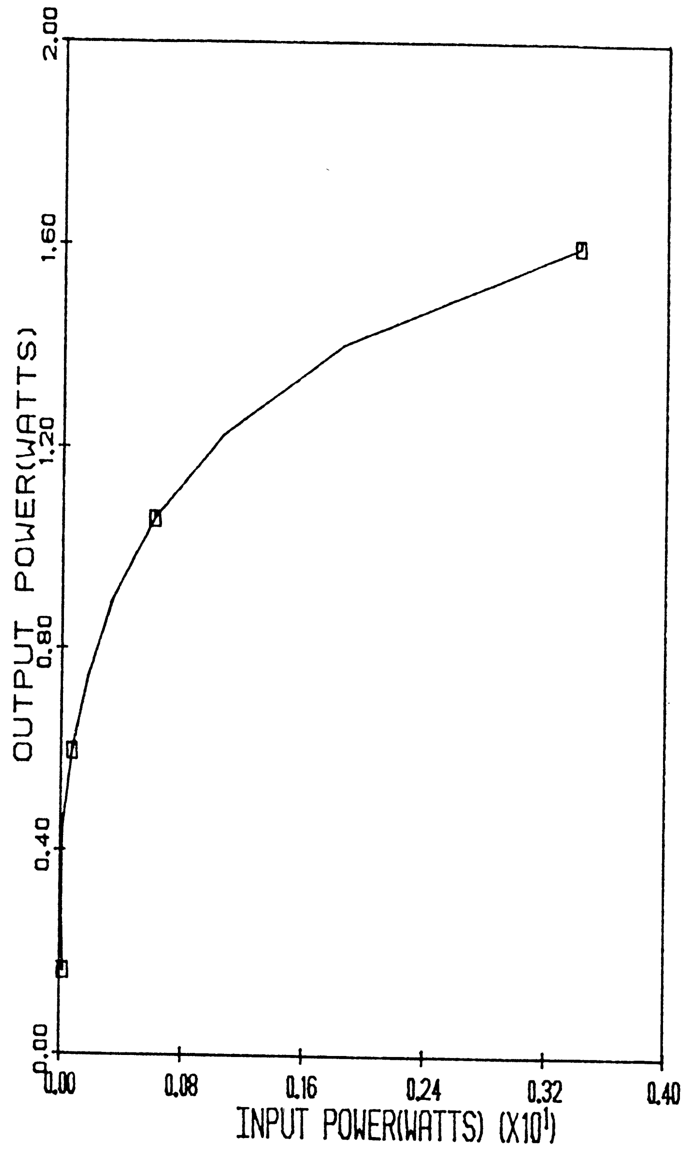
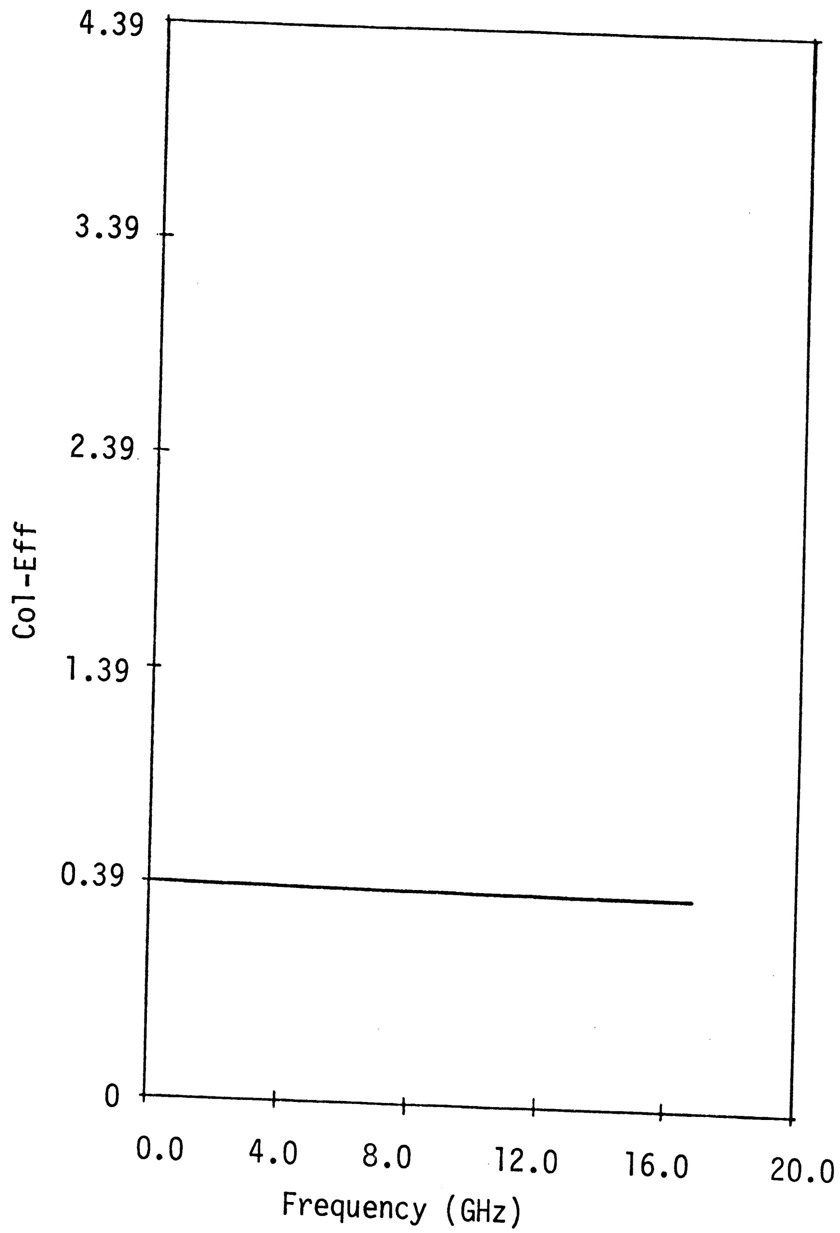
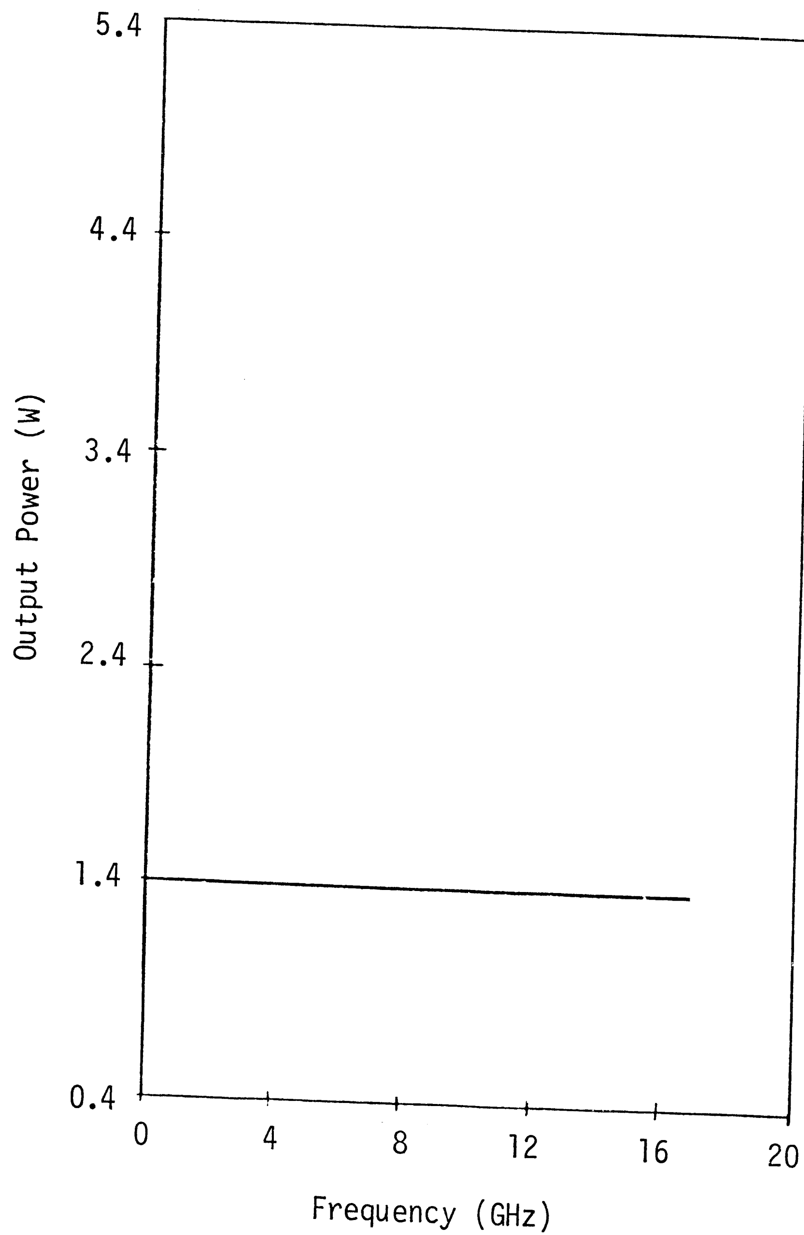


Fig. 4.24 The Output Power of a Si FET (Device S9) at 5.0 GHz as a Function of the Input Power.



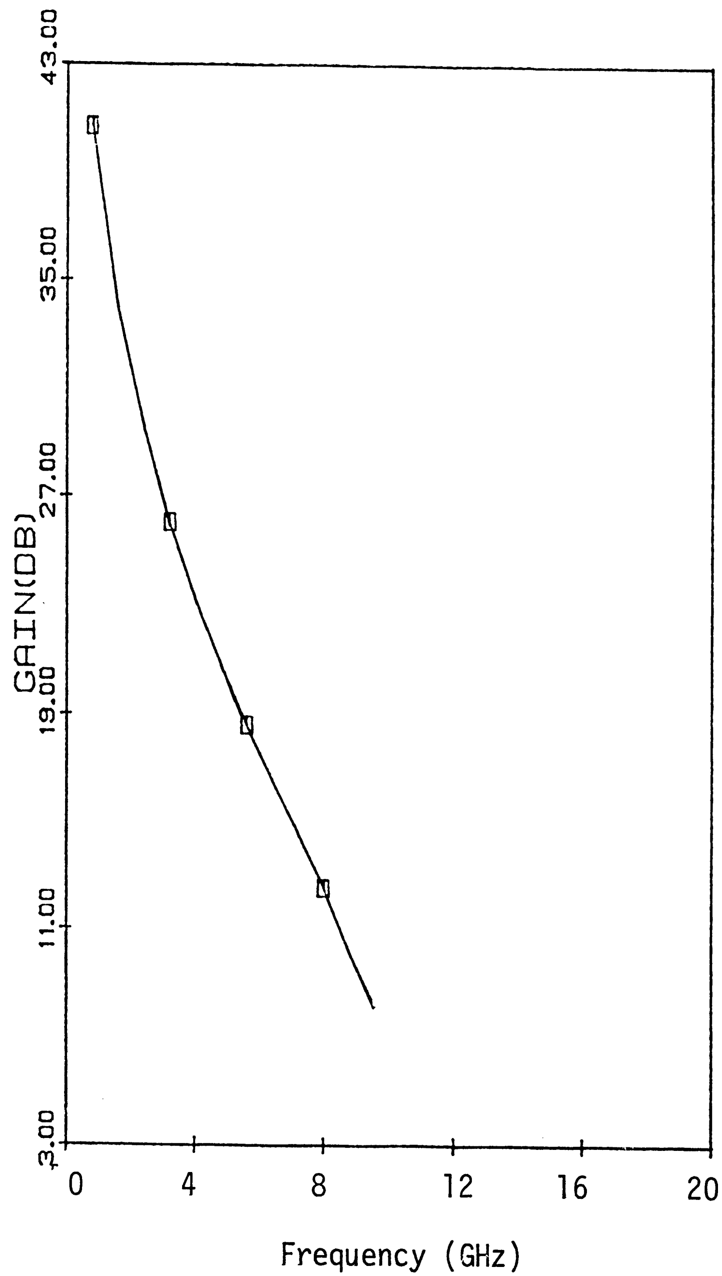
(a) Collector efficiency.

Fig. 4.25 The Large-Signal Performance of an InP FET (Device S8) as a Function of Frequency. (The Collector Efficiency Is Equal to COL-EFF-1.0.)



(b) Output power.

Fig. 4.25 The Large-Signal Performance of an InP FET (Device S8) as a Function of Frequency. (The Real Output Power Is 1 Watt Less than the Value Shown on the Power Axis.)



(c) Power Gain.

Fig. 4.25 The Large-Signal Performance of an InP FET (Device S8) as a Function of Frequency.

not the properties of the FETs. The effective drain-source current of an FET varies only with $V_{in}(t)$, if $V_{DSQ} + V_o(t)$ is more than the voltage which saturates the drain-source current. Also, at each frequency of operation the load impedance is calculated to keep the magnitude of the RF output voltage constant. Therefore the output power and the collector efficiency of a FET do not vary with the frequency of operation, but the gain does.

The power gain as a function of frequency is shown in Fig. 4.25(c). The power gain decreases with increasing frequency of operation. However, beyond a 10.0 GHz frequency of operation the gain oscillates and the real part of the input impedance becomes negative. This means that the solution is not valid beyond 10.0 GHz. The magnitude of the output voltage must be varied.

The large-signal performance of TTPT devices has also been investigated using the approximate forward bias voltage V_F. The results of the large-signal calculations for the TTPT devices are inadequate due to the approximated V_F and therefore were not included here.. Nevertheless, these results indicate the trends of the large signal performance of the TTPT devices which are:

(i) The input power increases rapidly as a function of either the input RF voltage, $V_{in}(t)$ or the output RF voltage, $V_o(t)$. The input capacitance increases with the carrier injection. The real part of the input admittance increases as the square of C_{gs} as shown in Eq. (4.24):

$$\mathrm{Real}(Y_{in}) \propto \frac{\omega^2 C_{gs}^2 R_c}{1 + \omega^2 C_{gs}^2 R_c^2} \quad . \tag{4.24}$$

The Real(Y_{in}) causes high input power which is not desirable. The TTPT devices can produce high output power with a reasonable gain, if the voltage swing is increased and the carrier injection is reduced by applying high $|V_{GSQ}|$ and $|V_{DSQ}|$.

(ii) The output power and efficiency of the TTPT devices are sensitive to the phase difference between the $V_{in}(t)$ and $V_o(t)$.

(iii) These devices also show the output power saturation for high input powers.

(iv) The gain decreases with both increasing input power and frequency.

(v) The output power and the collector efficiency decrease with increasing frequency, but increase with increasing input power.

The results of the large-signal computations can be summarized as follows:

(i) The large-signal model was demonstrated for FETs and predicts the trends of performance correctly.

(ii) The proper choice of the output voltage swing can prevent the operation of a FET in the linear region. Also, by choosing the magnitude of the input RF voltage to be less than or equal to the quiescent votlage, V_{GSQ}, the problem of the forward biasing of the gate-soruce junction can be prevented.

(iii) The InP or a semiconductor with a high saturation velocity is the best material to fabricate high frequency and high power FETs.

(iv) The input capacitance of the TTPT devices increases exponentially with the input RF voltage which causes high input power. For the high power and high frequency operation of the TTPT,

the output voltage swing, V_{ds}, must be increased and the carrier injection must be decreased to obtain a low C_{gs}, by applying a large $|V_{GSQ}|$.

(v) The exponential I-V characteristics of the TTPT devices makes these devices very sensitive to the phase difference between the $V_o(t)$ and the $V_{in}(t)$. It may cause some difficulty to design amplifying circuits with these devices.

4.8 Comparison of the Different Devices

The similarities and differences of the TTPT devices among themselves are outlined first. Then they are compared with the FETs. The properties of the various devices determine their area of application.

The TTPT devices are the lateral punch-through transistor [4], GFC-BARITT and SIT devices [3]. The lateral punch-through and GFC-BARITT devices are the same except for their gates. The gate of a GFC-BARITT device is insulated and the input voltage swing is limited only by the breakdown voltage of the gate-source or the gate-drain whichever occurs first. However, the gate of a lateral punch-through transistor is ohmic. The gate source junction must be biased such that this junction is reverse biased at all times, to prevent current flow through the gate. The same limitation is also applicable to the SIT devices.

The gate type is especially important for digital Integrated Circuit (IC) applications. Insulated gates make it easy to form an inverter circuit. The junction or ohmic gate type devices such as

lateral punch-through transistors, SITs and MESFETs, require complicated circuitry to obtain level shifting to prevent the forward biasing of the source-gate junction. The principles of operating of the GFC-BARITT devices and the lateral punch-through transistors are identical. The insulated gate electrodes make GFC-BARITT devices superior over others for applications in digital ICs.

The insulated gate, however, reduces the transconductance of the device. Meanwhile, the total gate-source capacitance of a GFC-BARITT device is smaller than other TTPT devices. The SIT devices have higher current and transconductance compared to the same size GFC-BARITT devices at the same bias conditions. If the channel doping concentration of a SIT and a GFC-BARITT device is the same the drain-gate breakdown voltages of these devices will be the same. The gate-source voltage swing of the SIT devices is limited by the gate-source forward biasing rather than the gate-source breakdown voltages, because the forward biased gate-source junction in the case of analog circuit applications increases the input power and the gate-source capacitance. Since the gate-source junction is forward biased, most of the input power is dissipated at the input, therefore the output power saturates when the gate-source junction becomes forward biased.

The output power of a GFC-BARITT device also saturates but at higher input power or RF voltage. The gate insulator must be protected against the static charge. The saturation of the output power is also observed in MESFET amplifiers [39].

The TTPT devices are high field devices. Even though the saturation velocity is the most important material parameter for the

TTPT devices improved performance, the III-V compound semiconductor TTPT devices are not superior to their silicon counterparts due to their high diffusion coefficients which results with low storage capacitance and high built-in potential which enables high RF voltage swing. Since the saturation velocities of silicon and III-V compound semiconductors are almost equal, the performance improvement of the III-V compound semiconductor TTPT devices are not expected to be significant. The FETs utilize the low electric field mobilities. Therefore GaAs or InP MESFETs can operate at much higher frequencies than their silicon counterparts due to the higher mobilities of the III-V compound semiconductors.

The results of the comparison of the various devices can be summarized as follows:

(i) The insulated gate GFC-BARITT devices are better than the other TTPT devices with the junction or ohmic type gate for the digital and analog circuit applications.

(ii) The TTPT devices have high power capability at lower microwave frequencies than the FETs.

(iii) FETs can operate at higher frequencies than the TTPT devices, because FETs utilize the high mobility of the III-V compound semiconductors.

(iv) The performance of the TTPT devices is less material dependent than that of the FETs.

CHAPTER V. DEVICE FABRICATION AND MEASUREMENTS

5.1 Introduction

In order to demonstrate the properties of the GFC-BARITT devices discussed previously, several devices were fabricated. These included structures such as (i) $n^+p^-n^+$ and (ii) M-p-Si-M. First, single devices utilizing Silicon On Sapphire (SOS) were fabricated to study the dc characteristics and to compare the experimental results with the theory developed in a previous chapter. The requirement for an insulated gate limits GFC-BARITT devices to silicon. The formation of a gate insulator on most of the III-V compound semiconductors is technologically difficult [61]. This was the main reason for choosing SOS as a material to fabricate these devices. Some considerations for material selection for TTPT devices are given in a later section.

This chapter is organized as follows: In Section 5.2 the technological problems related to different semiconductors are discussed. In Section 5.2.1, the chosen material, SOS, is analyzed. The fabrication procedure for the GFC-BARITT and insulated gate SIT devices are given in Section 5.3. The results of the dc measurements of single TTPT devices are analyzed in Section 5.4. In Section 5.5 the digital circuit applications of the GFC-BARITT device and the injection controlled logic are discussed. The basic inverter structures and principles are given in Section 5.5.1 In order to characterize the switching speed of the inverters, some ring

oscillators have been fabricated. The fabrication procedure of the ring oscillator circuits are different from those for single device fabrication. In Section 5.5.2 the fabrication procedure for the ring oscillators is given. A discussion of the switching characteristics of the inverter circuits is presented in Section 5.5.3. The theoretical expressions for the gate delay time for various inverters are given in Section 5.5.4. The conclusions which have been reached from the experimental study of the various inverters are summarized in Section 5.5.5. Finally, a comparison of the theoretical results which were presented in Chapter IV, with the experimental results obtained in Chapter V, are presented in Section 5.6.

5.2 Material Selection

In this study, SOS was chosen due to the simplicity of the technology associated with it. The well known silicon technology increases the yield and shortens the fabrication period for the realization of GFC-BARITT devices. With the present technology of III-V compound semiconductors, GFC-BARITT devices can also be fabricated. The depletion-type Metal-Insulator Semiconductor FET (MISFET) utilizing gallium arsenide (GaAs) [62], indium phosphide (InP) [63] and the ternary compound of GaAs and InP, $In_{1-x}Ga_xAs$ [64] have been reported. The fabrication of the enhancement type GaAs MISFET is still considered to be a technological problem.

The formation of the gate insulator for the enhancement type GaAs MISFET (E-MISFET) is not very likely because of basic physical properties and is not due to technological problems because the

GaAs technology is the most advanced among the technologies of the III-V compound semiconductors. The operation of InP [63] and recently $In_{1-x}Ga_xAs$ [64] E-MISFETs have been reported. The gate insulator technology which has been successful for InP and $In_{1-x}Ga_xAs$ E-MISFETs, has not been successful for GaAs E-MISFETs. It can be concluded that the fabrication of an E-MISFET requires a semiconductor with a narrow energy bandgap (E_G), narrower than the E_G of GaAs.

The energy bandgaps for various semiconductors are listed in Table 5.1. GaAs has the largest E_G, and the lowest intrinsic carrier concentration which results in the largest built-in potential between the source and the channel. The large built-in potential, V_B, requires a large band bending at the interface of the insulated gate and the channel. A large gate voltage is therefore necessary to bend the energy band and lower V_B at the source and the channel. The resulting large electric field, E, may cause (i) larger gate leakage current, (ii) local breakdown at the interface of the GaAs and the insulated gate due to interface nonuniformities, and (iii) charging of the interface states. The combined effects of the large electric field on the gate and the channel interface can prevent the inversion of the surface of p-GaAs. In the case of a D-MISFET the channel can be depleted with a smaller gate voltage because the depth of the depletion is independent of the energy bandgap. Therefore, any device can be fabricated from GaAs, if, and only if, it requires the depletion of the carriers. GaAs D-MISFETs have been reported with various gate insulators [65-68] which confirms the point raised above.

Table 5.1

Energy Bandgap for Various Semiconductor Materials

Material	$In_{1-x}Ga_xAs/InP$	Si	InP	GaAs
E_G (eV)	0.75	1.12	1.3	1.43
Intrinsic Carrier Density (cm^{-3})	$\sim 5.2 \times 10^{12}$	1.49×10^{10}	8.7×10^{7}	2.18×10^{6}
D-MISFET	yes	yes	yes	yes
E-MISFET	yes	yes	yes	no

Therefore, it can be concluded that it is possible to fabricate GaAs GFC-BARITT devices as well as InP, Si or $In_{1-x}Ga_x/InP$, since the function of the gate in a GFC-BARITT device is to induce a barrier to reduce the injection of the carriers from the source to channel. Nevertheless, SOS has been chosen due to its well known technology.

5.2.1 SOS Samples. The silicon-on-sapphire samples which were implanted were obtained from Hughes Research Laboratories. The information on the ion-implantation is listed in Table 5.2. The ion-implantation information given in Table 5.2 was employed to calculate the impurity concentration. The initial impurity distribution before any high temperature processing was estimated by following Gibbon's formulation [69] and is shown in Fig. 5.1. The impurity distribution is approximated by a Gaussian function which is given in Eq. (5.1):

$$n_p(x_p) = \frac{\phi}{\phi_p\sqrt{2\pi}} \cdot \exp - \frac{(x_p - R_p)^2}{2\sigma_p^2} , \qquad (5.1)$$

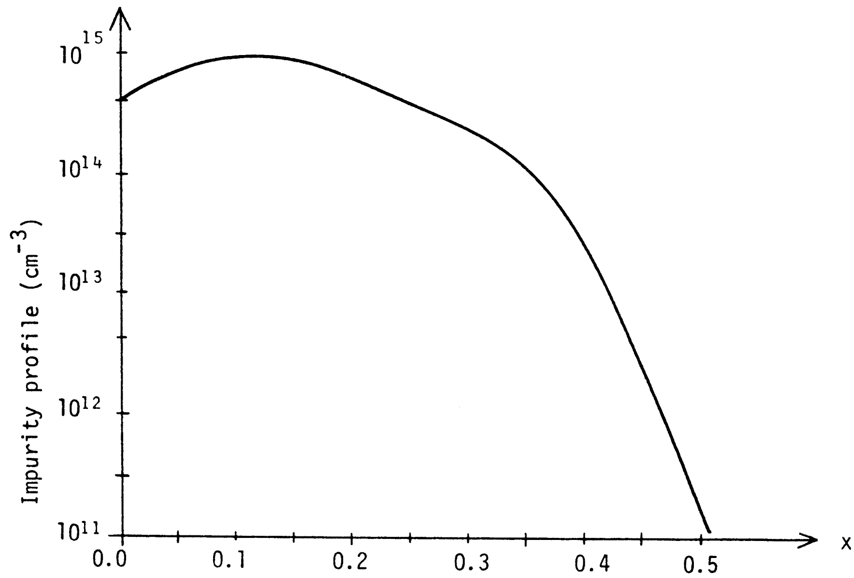
where ϕ is the ion dose, σ_p is the standard deviation in the projection range, and R_p is the projection range.

The impurity distributions in Figs. 5.1(a) and in Fig. 5.1(b) will change during the annealing at 925°C and more importantly during the dry-oxidation of the gate and/or diffusion of the n^+ drain and source terminals. The calculation of the final impurity distribution is rather complicated and will not be attempted here. Instead, an average doping concentration of 10^{14} cm^{-3} will be assumed for both p-type and n-type examples. The oxidation time at 1000°C is 90 minutes.

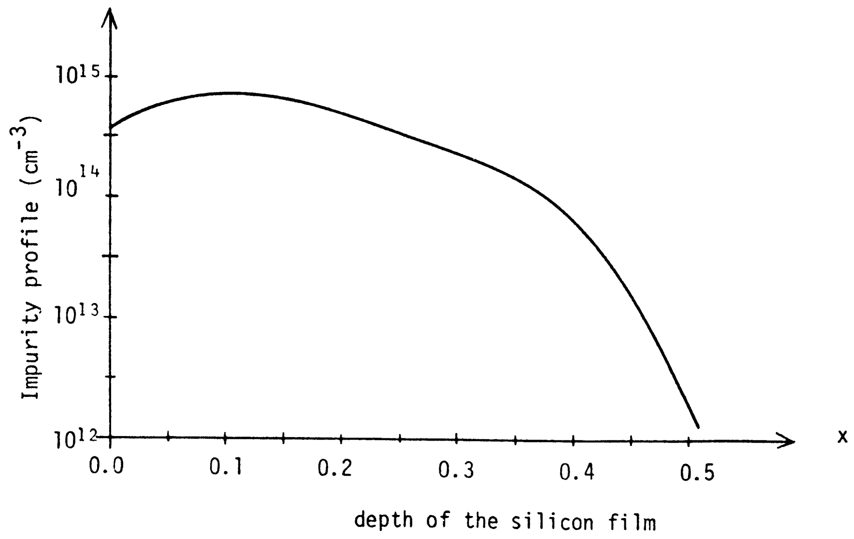
Table 5.2

Ion-Implantation Data

Material	Impurity	Ion Dose	Ion Energy	Annealing	
				Temp.	Time
0.5 μm SOS	Boron	10^{10} cm^{-2}	80 keV	925°C	30 min
0.5 μm SOS	Phosphorous	10^{10} cm^{-2}	200 keV	925°C	30 min



(a) Boron profile.



(b) Phosphorus profile.

Fig. 5.1 Profile of the Ion Implanted Impurities.

The impurity distribution will be almost uniform across the thin silicon film. The enhanced diffusion of the ion-implanted boron and phosphorous in the silicon film is known to exist [70]. Therefore, the uniform impurity distribution is justifiable.

5.3 Device Fabrication

Two different procedures have been developed to fabricate (i) a junction (J)-type GFC-BARITT (JGFC-BARITT) device and (ii) a Schottky Barrier (SB) GFC-BARITT (SBGFC-BARITT) device. An insulated gate SIT device can be fabricated by using the JGFC-BARITT device procedure with the n-type silicon film on sapphire.

The main difference between the fabrication of the SB GFC-BARITT and the JGFC-BARITT devices is the formation of the drain and the source electrodes. Therefore, all the processing steps of the device fabrication are described, and the special steps for different devices are pointed out.

Step 1:

Figure 5.2 shows the various steps employed for device fabrication. The wafers were first cleaned by following a standard cleaning procedure and then dry oxidized at 1000°C for 90 minutes to obtain a 900 Å film of SiO_2. Immediately after oxidation, a 0.23 μm thick Si_3N_4 film is deposited at 773°C in a CVD reactor. After the CVD Si_3N_4 deposition, the positive photoresist (PR) AZ1350B was spun-on the samples to protect the active device areas as shown in Fig. 5.2(a). Using PR as a mask, Si_3N_4 was etched for 11 minutes in a plasma composed of 200 CF_4:25 O_2 with 1.25 kW power and 13.5 MHz frequency. Following the

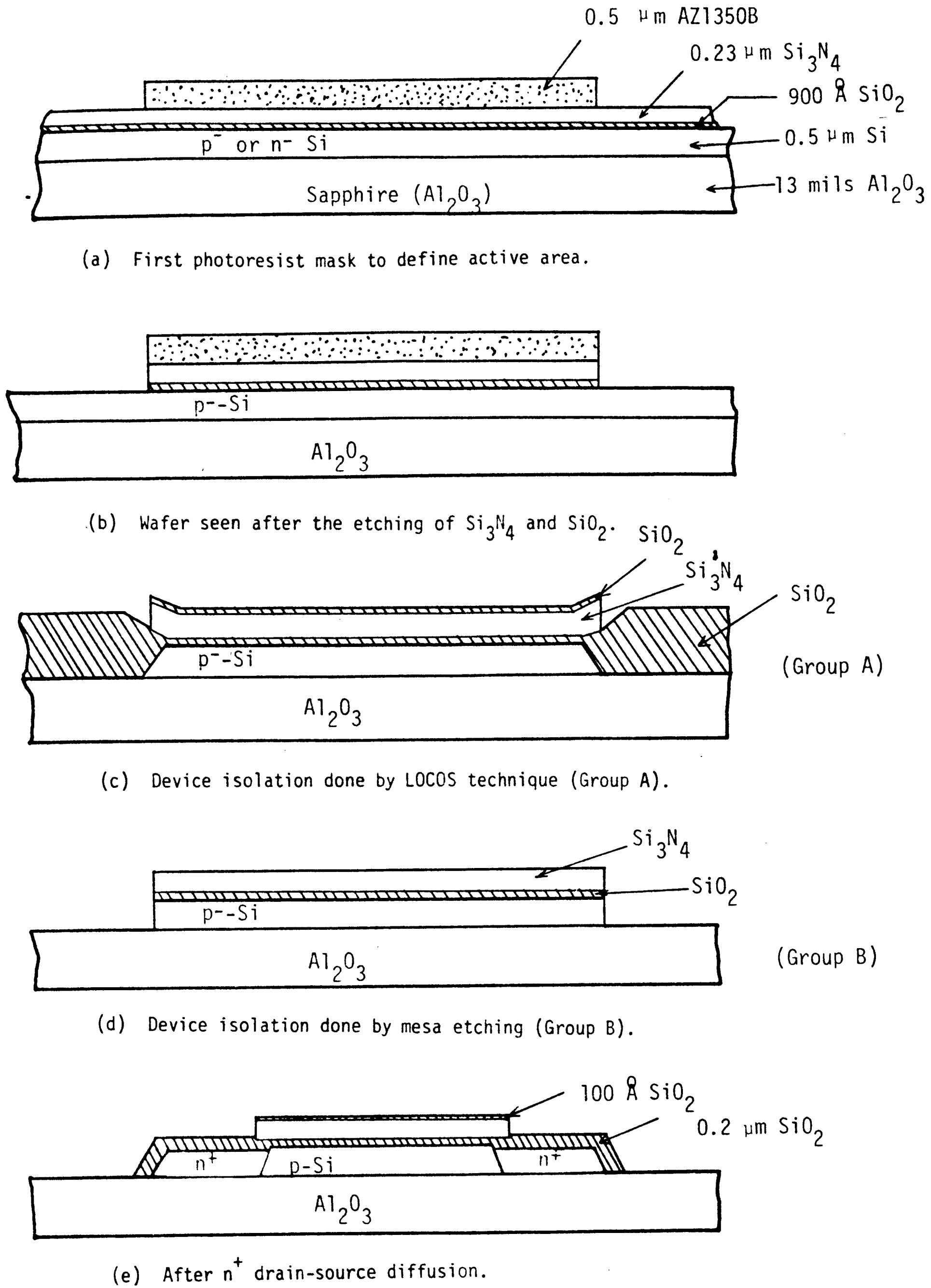
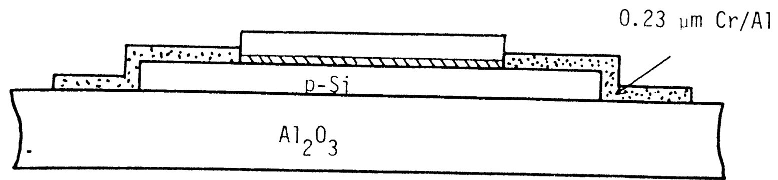
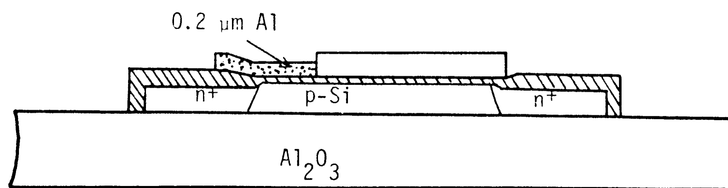


Fig. 5.2 Fabrication Processes of the MSM and Junction (J) GFC-BARITT Devices.

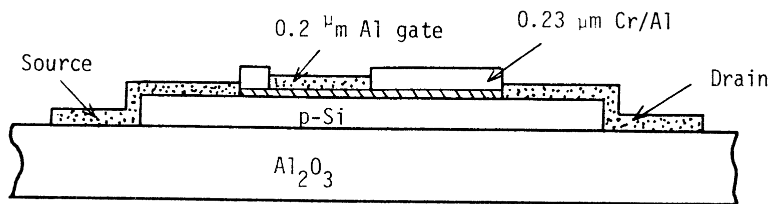
Fig. 5.2 (cont.)



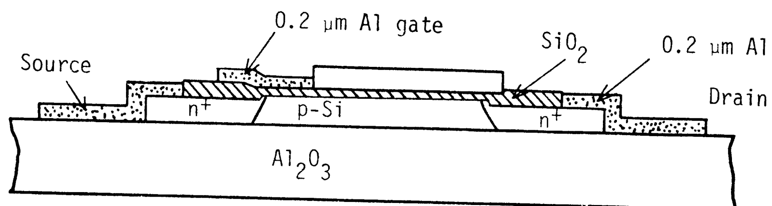
(f) After Schottky barrier drain-source formation.



(g) Gate definition for junction drain-source device.



(h) Gate definition for MSM device (final device)



(i) Metallization of the J-GFC-BARITT device.

plasma etching, a thin dry oxide was etched for one minute in buffered hydrofluoric acid (HF). At the end of Step 1, the wafer is as shown in Fig. 5.2(b).

Step 2:

The samples were cleaned again and some of them were oxidized at 1000°C for four hours in atmospheric steam (Group A). The other samples were etched for two minutes in a chemical etchant at 85°C (Group B). Group A and Group B are shown in Fig. 5.2(c) and Fig. 5.2(d) respectively. The chemical etchant was composed of 50 milligrams of potassium hydroxide (KOH), 50 centileters deionized water (DIH_2O) and 10 centiliters of isopropyl alcohol.

Step 3:

The drain and source windows are opened by using the previously defined plasma etching. The injection junctions were formed (i) by diffusing phosphorous at 950°C for five minutes for the JGFC-BARITT and $n^+n^-n^+$ SIT devices and (ii) by depositing Cr and then Al for SB GFC-BARITT devices. In Fig. 5.2(e) the junction type and in Fig. 5.2(f) the Schottky barrier type devices are shown. To form the Schottky barrier on silicon 300 Å Cr and 2000 Å Al were deposited. Without a thin Cr film, the Al resulted in very low barrier height Schottky contacts. The devices with only Al drain and source electrodes were essentially resistors.

Step 4:

To deposit the gate electrodes, PR was used as a mask and the PR in the gate region was removed. In other words, the PR protects the rest of the device other than the gate electrode regions. A Si_3N_4 layer was plasma etched as in Step 1. After etching, a 0.3 μm thick Al film was evaporated over the samples. The metal from the PR protected areas of the wafers were lifted off in an acetone solution with one-minute ultrasonic agitation. In Fig. 5.2(g) the JGFC-BARITT device with a narrow gate is shown. At this point, the processing of the SB GFC-BARITT device is complete.

Step 5:

The metallization of the JGFC-BARITT device is the final step of the device fabrication. The finished device is shown in Fig. 5.2(i).

Steps 1 through 5 describe the process steps of insulated gate SIT as well as GFC-BARITT devices. It is apparent that the mesa-etch isolation and the Schottky barrier injecting junction devices are less process involved and faster to fabricate. Figures 5.2(d) through 5.2(i) show only the processing steps for mesa-etch isolated or Group B wafers. The processing steps for the local oxidation process isolated or Group A wafers are the same as those of Group B.

The technology to fabricate TTPT devices which is outlined in this study, is far from being the optimum one. The source of a JGFC-BARITT device can be self-aligned to prevent the overlap between the gate metal and the source electrode. In the present

Schottky barrier GFC-BARITT device process, the distance between the source and gate is determined by the alignment tolerance (misalignment) of the mask-aligner. This results in low yield. Nevertheless a sufficient number of the junction and the Schottky barrier type GFC-BARITT devices were operational to test the dc characteristic. The Schottky barrier GFC-BARITT devices shown in Fig. 5.2(h) are especially inefficient, because the injection area is shallow. A better SB GFC-BARITT device structure is shown in Fig. 5.3. Photomicrographs of the fabricated devices are shown in Fig. 5.4.

5.4 Dc Characteristics

The fabricated devices were probed and the dc current-voltage (I-V) characteristics were displayed on a curve tracer. In Fig. 5.5, the I-V characteristics of an $n^+p^-n^+$ GFC-BARITT device are shown. As seen in Fig. 5.5(a), this device operates like an enhancement-type MOSFET with positive applied gate voltages. However, at high drain-source, V_{DS}, voltage ($|V_{DS}| \geq |V_{PT}|$), the JGFC-BARITT device shows exponential I-V characteristics. For negative gate voltages, the device also shows exponential I-V characteristic as seen in Fig. 5.5(b).

The Metal p-Si Metal (MSM) GFC-BARITT device characteristics are shown in Fig. 5.6(a) for positive gate voltages and in Figl 5.6(b) for negative gate voltages. The gate length of the SB GFC-BARITT devices is 5 μm and the length of the channel between the drain and the source is 20 μm. Therefore, the E-MOSFET operation

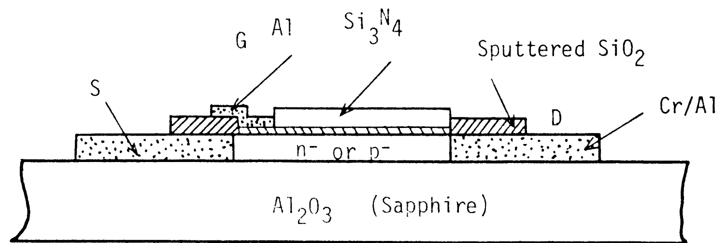
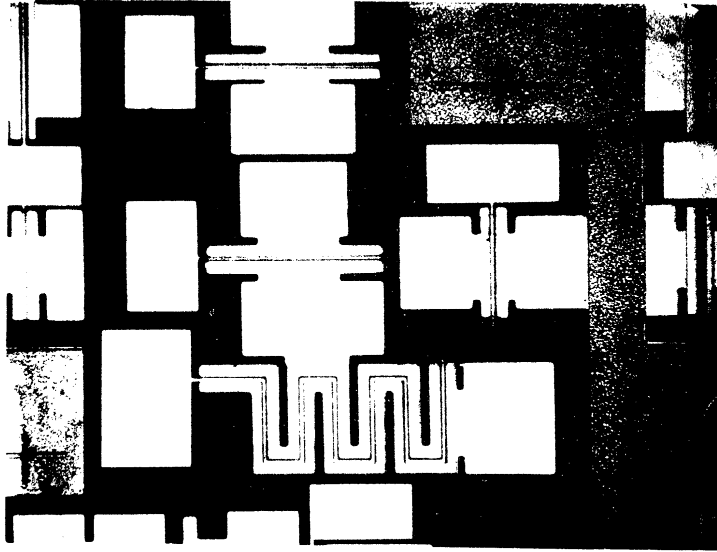
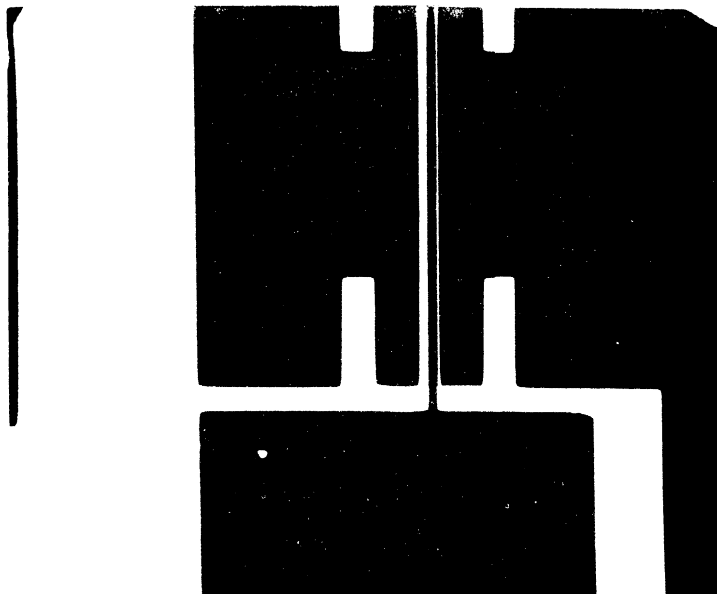


Fig. 5.3 Ideal Schottky Barrier GFC-BARITT Device.

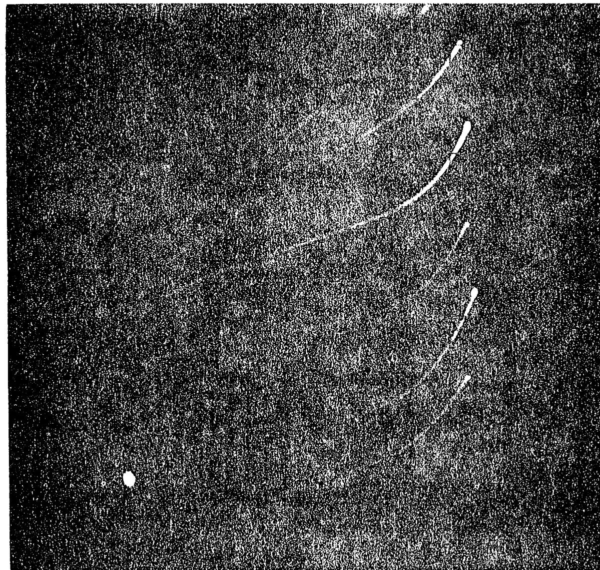


(a) Die photomicrograph.



(b) Enlarged photomicrograph of a single device.

Fig. 5.4 Fabricated GFC-BARITT Devices.

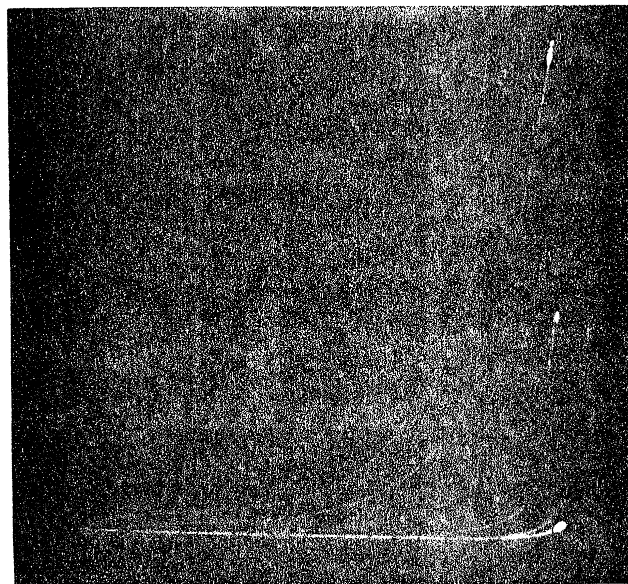


Vertical: 0.1 mA/div

Horizontal: 5 V/div

Gate bias: 2.0 V/step

(a) Turn-on characteristics.



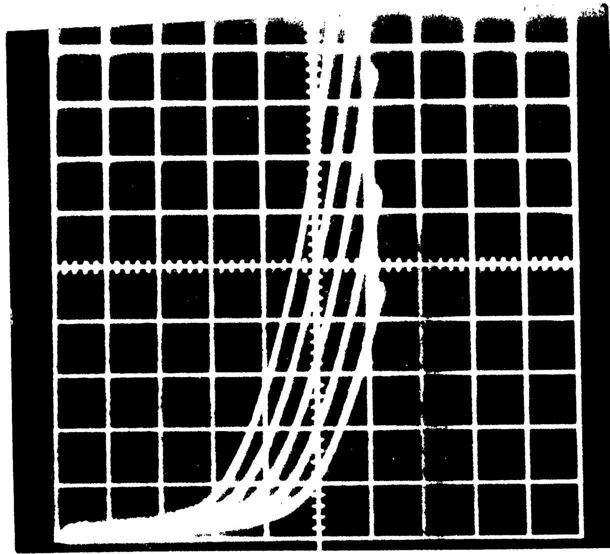
Vertical: 0.1 mA/div

Horizontal: 5 V/div

Gate Bias: -2.0 V/step

(b) Turn-off characteristics.

Fig. 5.5 $n^+p^-n^+$ Device (Z = 0.2025 cm, L_G = 5 μm and L_{DS} = 20 μm.

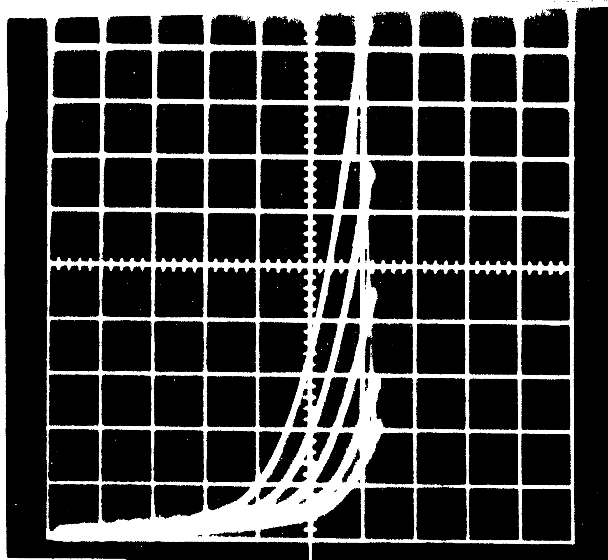


Vertical: 0.2 mA/div

Horizontal: 10 V/div

Gate bias:: 5.0 V/step

(a) Turn-on characteristics.



Vertical: 0.2 mA/div

Horizontal: 10 V/div

Gate bias: -5 V/step

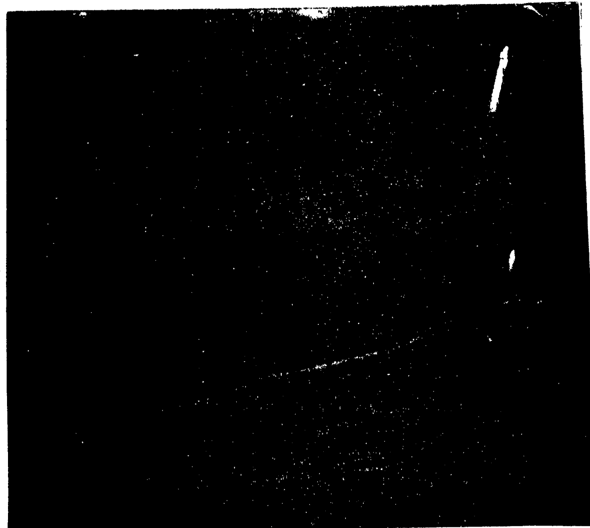
(b) Turn-off I-V characteristics.

Fig. 5.6 MSM GFC-BARITT Device. (z = 500 μm, L_{SG} = 2.5 μm, L_{GD} = 12.5 μm, and 0.5 μm thick.

of the GFC-BARITT device cannot be observed in Fig. 5.6(a) at low V_{DS} ($|V_{DS}| \leq |V_{PT}|$). The SB GFC-BARITT devices with Cr/Al drain source contacts were operational. However, alumimum contacts used as Schottky barriers did not work. To the best of our knowledge, this is the first study of a M-p-Si-M punch-through structure. There have been published reports on M-n-Si-M punch-through diodes (M-n-Si-M BARITT diode) [7] and p-channel SB-MOSFETs [30], [71] through [73]. Most recntly, n-channel SB-MOSFETs with molybdenum drain-source contacts have been fabricated in our laboratory [73].

In Fig. 5.7 the I-V characteristics of an $n^+n^-n^+$ Insulated Gate (IG) SIT or a majority carrier GFC-BARITT device are shown. This device operated as an IGFET for positive gate voltages as shown in Fig. 5.7(a). Negative gate voltages deplete the channel and induce a barrier height for electron injection in the vicinity of the source electrode. At low V_{DS} voltages, the gate induced barrier height prevents carrier injection. However, at high V_{DS} voltages, this barrier height is reduced by V_{DS}. Therefore, the current is negligible at low V_{DS} voltages and increases exponentially at high V_{DS} voltages as seen in Fig. 5.7(b).

In all the devices tested, the terminal which is closer to the gate is biased as a source electrode and the other terminal is biased as a drain electrode. The devices were fabricated asymmetrically deliberately in order to test the function of the gate-source distance. The theoretical study concluded that the control of the injection required a gate electrode which is located near the injection point. This theory was proven experimentally by

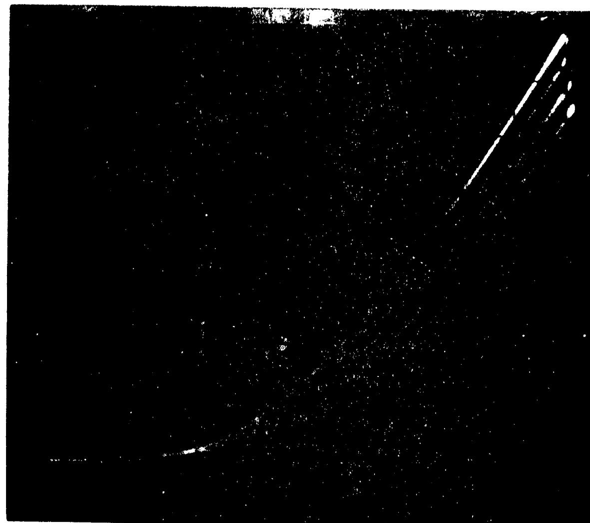


Vertical: 0.2 mA/div

Horizontal: 5 V/div

Gate bias: 5 V/step

(a) Turn-on characteristics.



Vertical: 0.2 mA/div

Horizontal: 5 V/div

Gate bias: -5 V/step

(b) Turn-off characteristics.

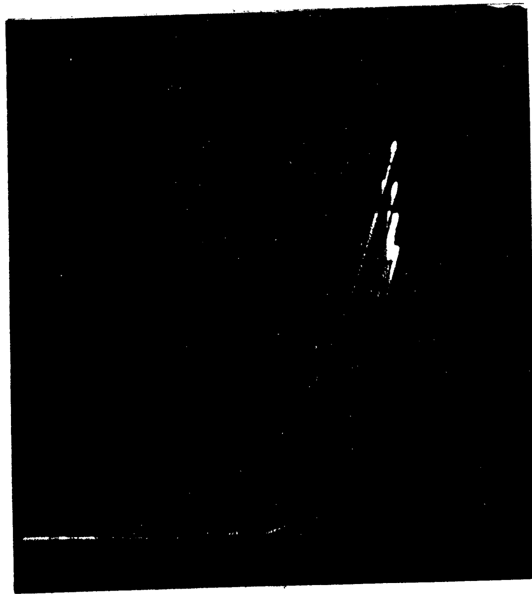
Fig. 5.7 Insulated Gate $n^+n^-n^+$ SIT with Z = 125 μm, L_{SG} = 3.5 μm, L_{GS} = 10 μm, L_{DS} = 30 μm, and 0.5 μm thick.

biasing the terminal far from the gate as the source and biasing the one closer to the gate as the drain. The I-V characteristics of a normally biased device is shown in Fig. 5.8(a). After interchanging the source and the drain terminals, the resulting I-V characteristics are shown in Fig. 5.8(b). As can be seen in Fig. 5.8(b), if the source is far from the gate, the gate voltage cannot modulate the drain-source current, I_{DS}. All the devices tested in this study required a small distance between the source and the gate electrodes to control I_{DS} through an insulated gate.

5.5 Introduction to Digital Circuit Applications

Two fast inverter schemes for the semiconductor on insulator (SOI) system have been proposed. The switching speed of a Complementary Metal Oxide Semiconductor on SOI (CMOS/SOI) or specifically CMOS/SOS logic can be increased by replacing the slow p-channel MOSFET with a faster device. A p-channel MOSFET is slower than the $n^+n^-n^+$ depletion-type MOSFET (or IGFET) due to its lower hole mobility as given in [74]. A p-channel MOSFET can be replaced by (i) a gate-field controlled (GFC) diode and (ii) a GFC-BARITT device which can result in a faster inverter due to their high current capabilities.

The concept of the insulated gate effect on the diode characteristics was developed by Grove [55]. Recently, a vertical GFC-diode/SOI has been reported [75]. To the best of our knowledge the planar GFC-diode/SOS has been reported for the first time in this work. In the following sections, the principles of operation of a GFC-diode/SOS called Injection Controlled Logic (ICL) and a

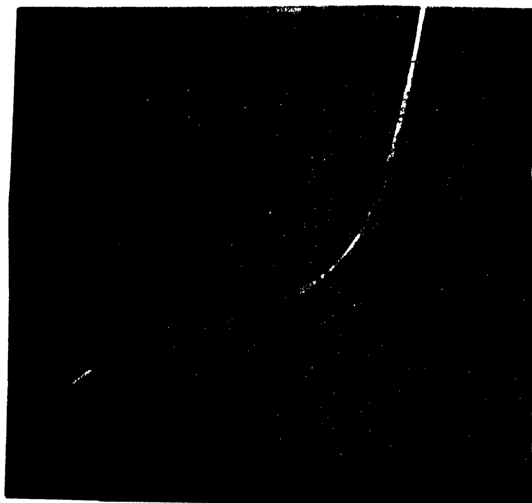


Vertical: 0.05 mA/div

Horizontal: 10 V/div

Gate bias: -2 V/step

(a) Source and gate closer than the gate and drain.



Vertical: 0.01 mA/div

Horizontal: 10 V/div

Gate bias: -5 V/step

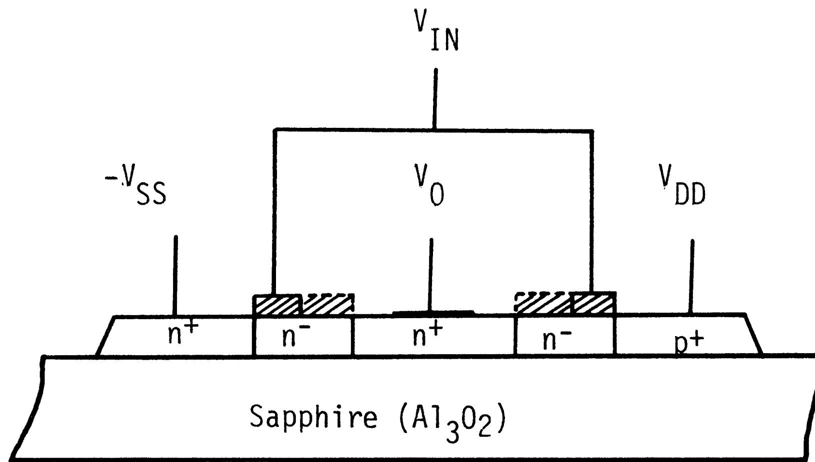
(b) Drain and gate closer.

Fig. 5.8 n^+p^- GFC-BARITT Device with Z = 125 μm, L_{SG} = 5 μm, L_G = 10 μm, L_{DS} = 30 μm, and 0.5 μm Thickness

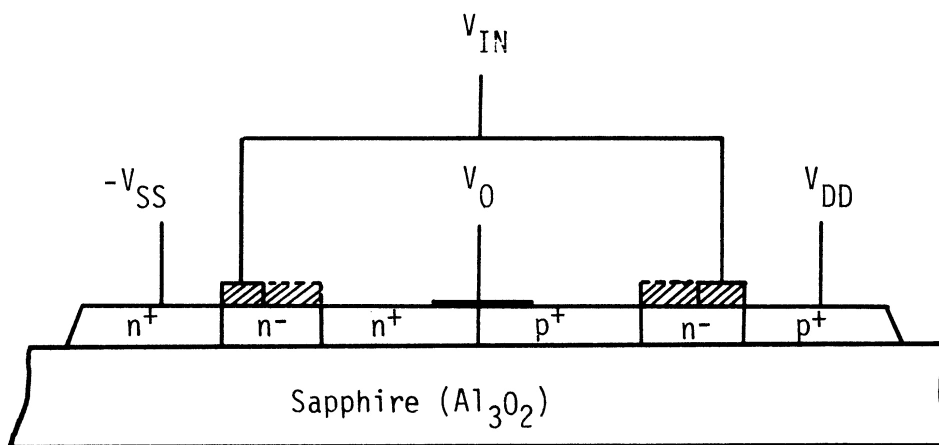
GFC-BARITT device/SOS inverters, fabrication of ring-oscillator circuits and an analysis of the experimental results are given.

5.5.1 Basic Structure and Principles of Operation. A new complementary logic scheme is illustrated in Fig. 5.9(a). An ICL inverter has two components which are: (i) an $n^+n^-n^+$ insulated gate field effect transistor (IGFET) and (ii) a $n^+n^-p^+$ gate field controlled diode (GFC-diode). The negative one of the two power supplied, $-V_{SS}$, is connected to the source of the IGFET, and the positive power supply is connected to the emitter of the GFC-diode. The insulated gates of both devices are joined together at the input terminal. The drain of the IGFET which is also the base of the GFC-diode is the output terminal. A basic ICL inverter is an $n^+n^-n^+n^-p^+$ structure with two insulated gates on the n^--regions as shown in Fig. 5.9(a). The drain of the IGFET and the base of the GFC-diode are common for both devices (common drain-base structure). A CMOS/SOS inverter is also given in Fig. 5.9(b) to compare with the ICL/SOS inverter.

The operation of an ICL inverter is as follows: If the input voltage, V_{in} is high (or positive) the $n^+n^-n^+$ IGFET is turned on and, it acts as a resistance. As a result, the output voltage, V_o, will charge up to the voltage level of the source of the IGFET, $(-V_{SS})$. If V_{in} is low (or negative), the IGFET is turned off, but the $n^+n^-p^+$ GFC-diode is turned on. A negative gate voltage will allow the carrier injection from p^+-emitter to n^+n^--base. Therefore, V_o, for this case, will charge up to the voltage level of the emitter of the GFC-diode $(+V_{DD})$. The V_o charges up to $+V_{DD}$ rather than



(a) Injection controlled logic.



(b) CMOS/SOS logic.

Fig. 5.9 Inverter Structures.

V_{DD}-V_B where V_B is the built-in voltage of the n^-p^+ junction, because V_B vanishes at the interface of the SiO_2 gate insulator and the n^--base. The GFC-diode is always forward biased, but the carrier injection is controlled through an insulated gate. If the gate voltage, V_{in} is negative, the GFC-diode will be turned on, and if V_{in} is positive, then the GFC-diode will be turned off.

The CMOS/SOS inverter structure is shown in Fig. 5.9(b). The dotted lines are for the overlapping gate structure which is necessary for the operation of the E-type p-channel MOSFET. The solid lines are for the narrow gate one which is the ideal GFC-BARITT for the SOS inverter. A CMOS/SOS inverter structure was used to fabricate a five-stage ring oscillator circuit. The switching speed of the conventional CMOS/SOS and the GFC-BARITT device (GFC-BARITT/SOS) inverter have been evaluated using the CMOS/SOS inverter ring oscillators. At low drain source bias conditions, the inverter structure shown in Fig. 5.9(b) operates as a CMOS inverter. When the applied voltage (V_{DD}) exceeds the punch-through voltage (V_{PT}) of the p-channel, the same structure operates as a GFC-BARITT/SOS inverter. More specifically, the p-MOSFET is replaced by the GFC-BARITT device at V_{DD} in excess of V_{PT}.

The operation of a GFC-BARITT/SOS is not as simple as the CMOS/SOS inverter. The principles of operation of a GFC-BARITT SOS inverter are as follows. When the input voltage is positive, the GFC-BARITT device will be turned off. Meanwhile the $n^+n^-n^+$ IGFET will be turned on. As a result, the output will charge up to $-V_{SS}$ voltage. If V_{in} becomes negative, the gate induced barrier against the carrier

injection in the GFC-BARITT device will vanish. Therefore the GFC-BARITT device will be conducting, while the IGFET is turned off. In an ideal GFC-BARITT/SOS structure, the output voltage of the inverter, V_o will charge up to $V_{DD} - V_{PT}$. However, in a GFC-BARITT/SOS structure with an overlapping gate, V_o will be charged up to $V_{DD} - V_{PT}$ by the GFC-BARITT device current. Beyond this level, V_o will be charged up to $V_{DD} - V_{TH}$ by the p-channel MOSFET, where V_{TH} is the threshold voltage of the enhancement type MOSFET.

5.5.2 Ring Oscillator Fabrication. Injection-controlled logic ring oscillator circuits have been fabricated on the 0.5 micrometer (μm) thick silicon on sapphire samples described previously. A simple four-mask fabrication process which was used to fabricate the ICL/SOS and CMOS/SOS ring oscillators, is described below. The n-type SOS samples which were describes in Section 5.2.1 were used to fabricate ring oscillator circuits.

The samples were cleaned, and active device areas were defined by using a 0.5 μm thick AZ1350B photoresist as a mask and etching the unprotected silicon in a plasma composed of 200 CF_4:25O_2 at 13.5 MHz frequency and 1.25 kW power. After plasma etching, the active device areas were oxidized in dry O_2 at 1000°C for 90 minutes to form 900 Å thick SiO_2 for the gate insulation. Immediately after the oxidation, 0.45 μm thick polysilicon is deposited at 668°C in the CVD reactor. The n^+-diffusion windows were defined by using AZ1350B photoresist as a mask and etching the polysilicon in a 200 CF_4:25O_2 plasma. Consequently, the 900 Å thick SiO_2 covering the n^+-diffusion windows was etched in a buffered HF solution. Prior to the diffusion the cleaned samples were phosphorus prediffused for four minutes.

Immediately after the diffusion, 0.3 μm thick SiO_2 was deposited at 810°C in the CVD reactor. This oxide layer was used as a mask to protect the n^+ diffusion and the n^+ polysilicon gate regions. The p^+-emitter windows are defined in a similar manner to the n^+-window formation. After the boron prediffusion at 950°C for five minutes, the 0.3 μm SiO_2 was removed completely.

The final step was the 0.3 μm thick aluminum evaporation and the definition of the metal connections. The processing sequence of the five-stage ring oscillators is shown in Fig. 5.10(a) through 5.10(f). The die microphotographs of the ring oscillator and some test circuits are shown in Fig. 5.11(a) and 5.11(b). This is a self-aligned gate process. The gate lengths of all the devices in the ICL/SOS and CMOS/SOS ring oscillators were 20 μm and the gate widths were 100 μm.

5.5.3 Results and Discussion. The fabricated ring oscillators with 20 μm gate lengths and 100 μm gate widths were biased at V_{DD} = 10 V and V_{SS} = -10 V. The output waveforms of an ICL/SOS ring oscillator and of a CMOS/SOS ring oscillator are shown in Figs. 5.12 and 5.13, respectively. The average delay time as a function of the power dissipation is calculated, and given in Fig. 5.14 for an ICL/SOS inverter and in Fig. 5.15 for a CMOS/SOS inverter. The average delay time is 19.6 ns for an ICL/SOS inverter and 30 ns for a CMOS/SOS inverter at ±15.0 V. However, the power dissipation is higher than the power dissipation of a CMOS/SOS inverter.

The symmetry of the output waveforms in Fig. 5.12 indicates that the $n^+n^-p^+$ GFC diode is as fast as the $n^+n^-n^+$ IGFET. If the

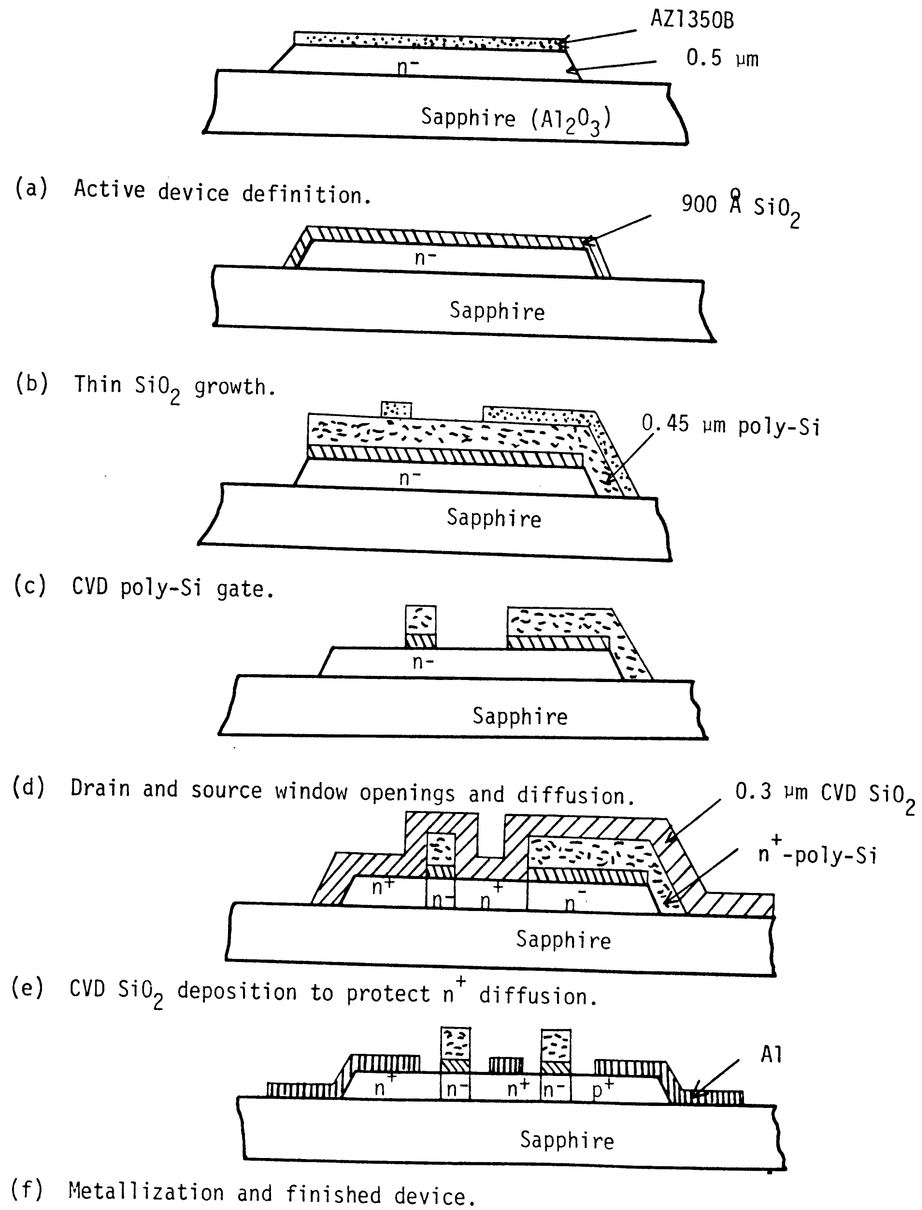
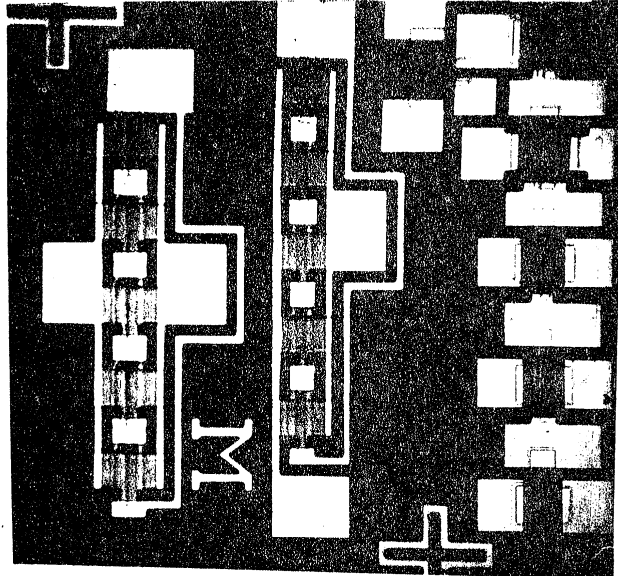
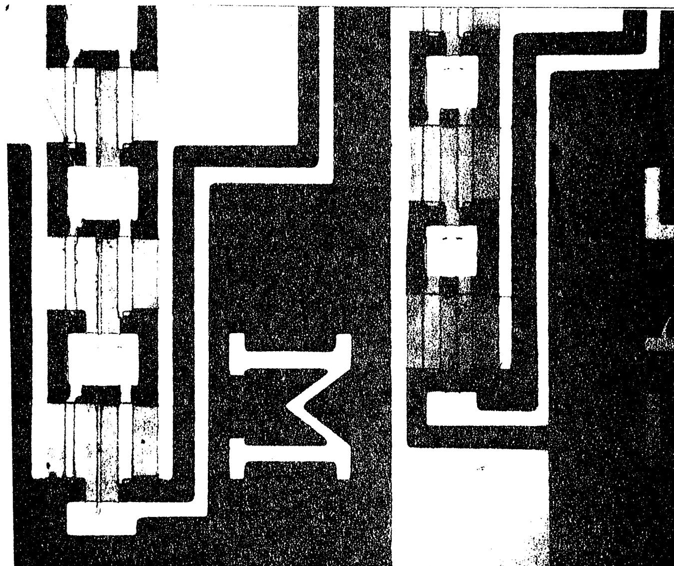


Fig. 5.10 Fabrication Steps.



(a) Die photomicrograph.



(b) Magnified photomicrograph of the oscillator circuits.

Fig. 5.11 Photomicrograph of the Five-Stage Ring Oscillators.

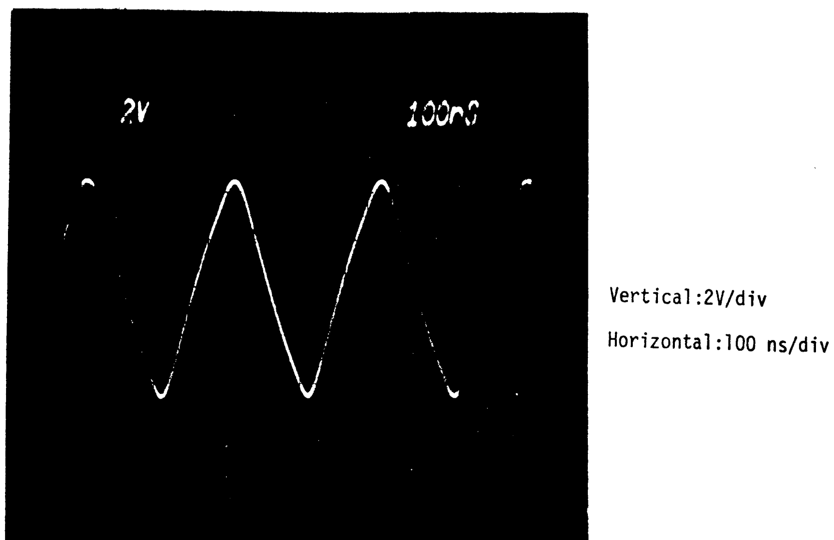
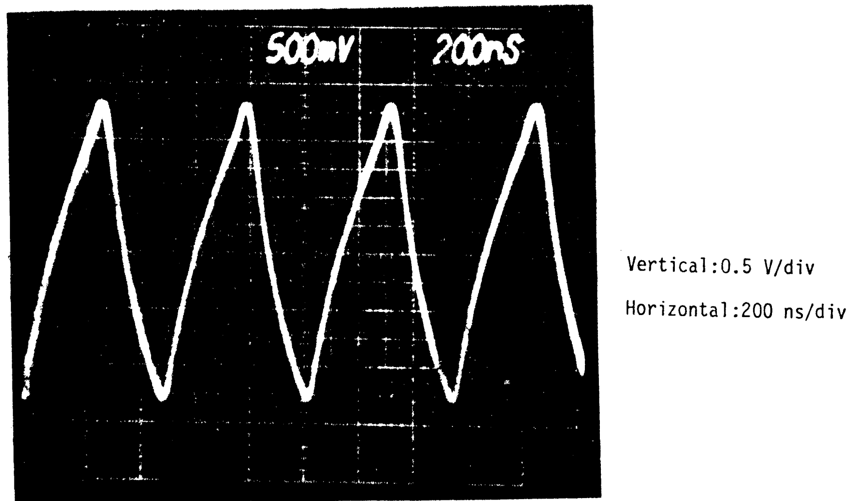


Fig. 5.12 Output Waveforms of the Complementary ICL Ring Oscillator.



Vertical:0.5 V/div

Horizontal:200 ns/div

Fig. 5.13 Output Waveforms of the CMOS/SOS Ring Oscillator.

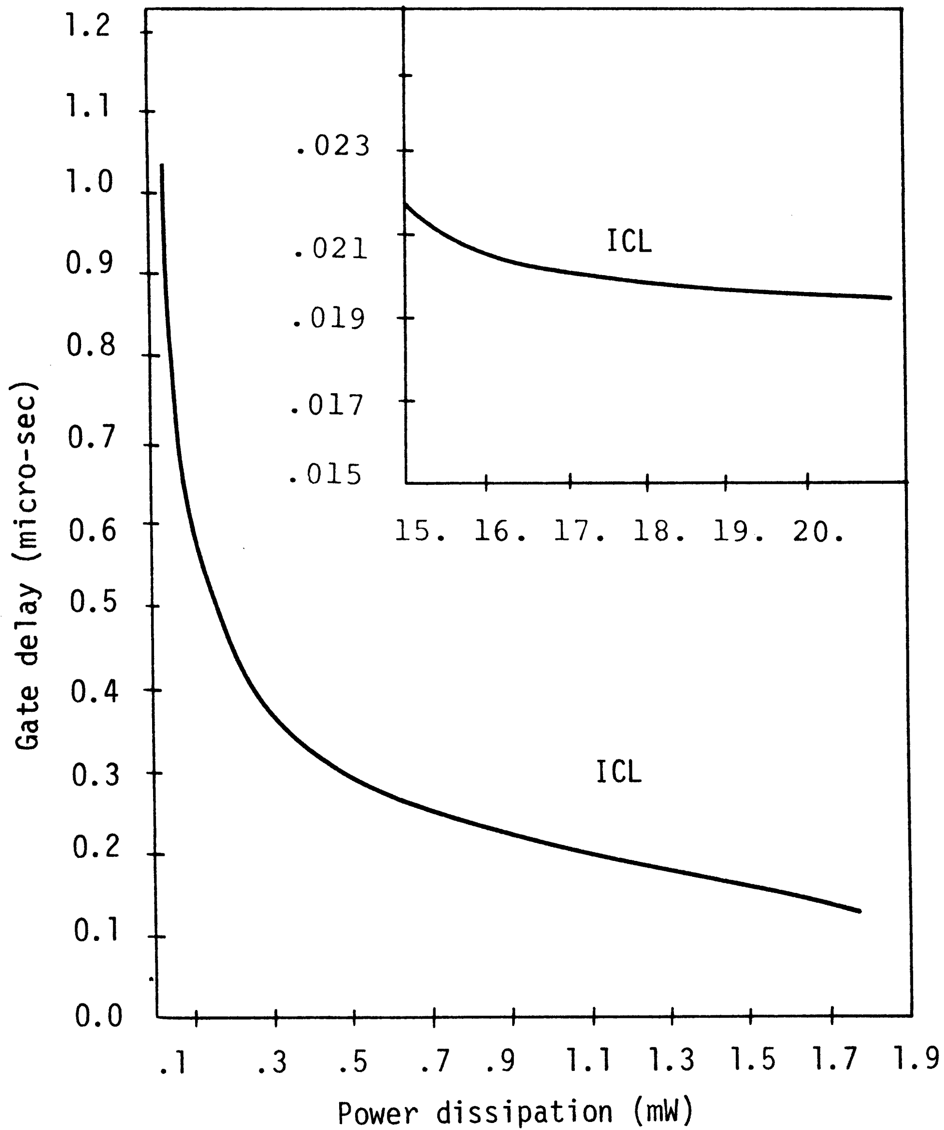


Fig. 5.14 Switching Speed of the Injection Controlled Logic Gate as a Function of the Power Dissipation.

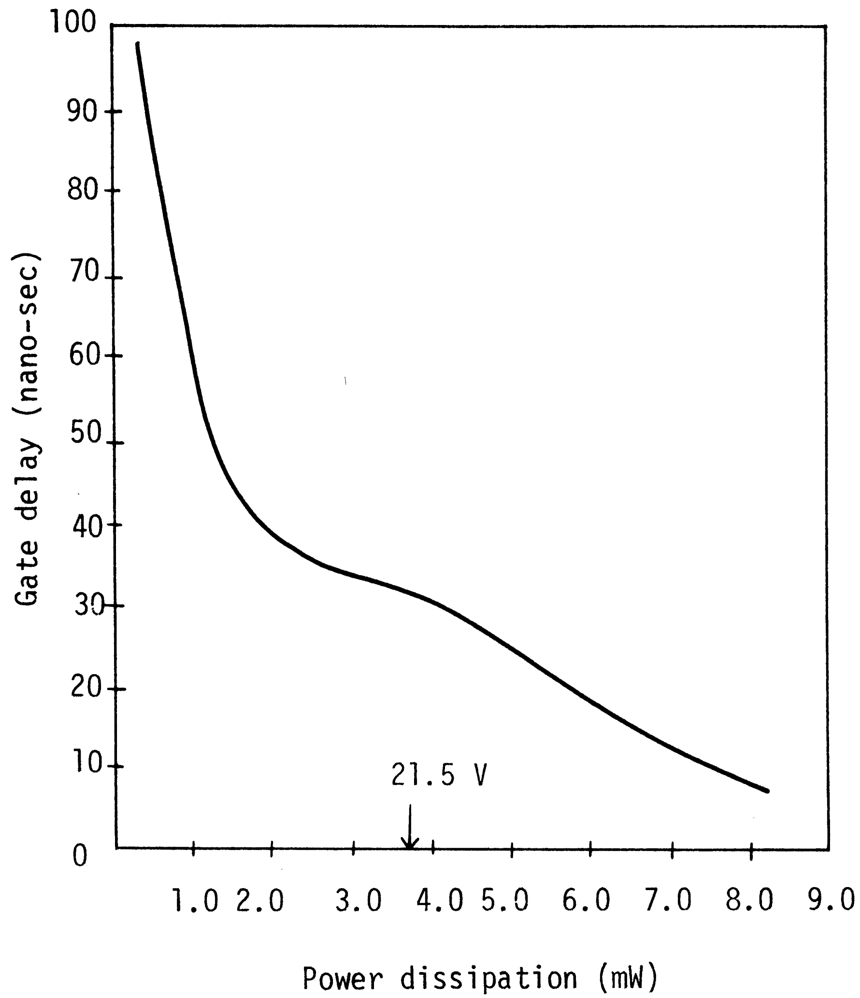


Fig. 5.15 Switching Speed of the Punch-Through Logic Gate as a Function of Power Dissipation.

switching speed of the one device is faster than the other, the resulting output waveform of the ring oscillator will be non-symmetrical, as in the case of CMOS/SOS ring oscillator shown in Fig. 5.13. In Fig. 5.13 , rise time of the output waveform is 1.5 times longer than the fall time which is an indication of an inverter with one fast and one slow switching device. Since the mobility of the holes is lower than the mobility of the electrons as given in [74], a $n^+n^-n^+$ IGFET will be faster than the same size p-channel MOSFET. As shown in this study, replacing the p-channel MOSFET in a CMOS/SOS with a faster device, GFC-diode, the average gate delay can be significantly reduced. In addition to the short gate delay time, the area consumed by this new, ICL/SOS inverter is also smaller than the area consumed by the CMOS/SOS.

Since an $n^+n^-n^+$ IGFET is common for SOS/CMOS and ICL logic, the difference in performance between these two logic circuits is due to the $p^+n^-p^+$ MOSFET and the $n^+n^-p^+$ GFC-diode. The current capability of an $n^+n^-p^+$ GFC-diode is higher than that of a thin p^- resistance of a $p^+n^-p^+$ MOSFET. In the $n^+n^-p^+$ GFC-diode, carriers are injected from the 0.5 μm thick diode, but in a $p^+n^-p^+$ MOSFET the current passes through only a few hundred Angstrom thick inversion layer. More current means faster charging of the output capacitance.

The GFC-diode circuits can switch faster than the MOSFET circuits because (i) the mobility of the injected carriers in the GFC-diode is high (bulk mobility of the silicon film) while the carrier mobility in an inversion layer of a MOSFET is lower than the bulk mobility, and (ii) the total current of a GFC-diode is higher

due to the larger injection area (film thickness) as opposed to a few 100 Å thick current path of a MOSFET.

Figure 5.15 shows the effect of the punch-through phenomenon on the switching characteristics of a logic gate. Beyond the indicated "21.5 volts" the n^- region of the $p^+n^-p^+$ MOSFET of the CMOS/SOS inverter is completely depleted. The p-channel MOSFET now operates as a GFC-BARITT device [76]. A current is provided through the $p^+n^-p^+$ GFC-BARITT device by the injection of the holes from the p^+ source into the depleted channel. Therefore, the GFC-BARITT device can supply a higher current than the same size MOSFET. This is the reason why Fig. 5.15 shows a sudden drop in the delay time (up to 10 ns) at a bias voltage in excess of the punch-through voltage. The delay time of a GFC-BARITT/SOS inverter can be further reduced by using a recessed gate. For instance, a GFC-BARITT device with 1 μm long gate and 20 μm drain-source distance, is expected to have a delay time of 500 ps. By reducing L_{DS} to 5 μm, the delay time is estimated to be less than 100 ps.

A delay time of 75 ps for a punch-through MOSFET inverter on a 10^{15} cm^{-3} doped p-Si has been reported [77]. It is possible to achieve even faster switching speeds with the scaled down GFC-BARITT device on SOS inverters. The distance between the drain and the source, L_{DS}, does not have to be in the micron or submicron range, it can be four or five μm. Only the gate length has to be in the micron or submicron range. In a GFC-BARITT device or in a MOSFET, the switching speed of the device is limited by the charging time of the output capacitance (including parasitics). L_{DS} determines the

transit time of the device which is much shorter than the switching (or gate delay) time. Therefore, for a short switching time, any device should have a high current capability and a small output capacitance. The inverter structure in Fig. 5.9(b) has recessed gates (dotted lines) for the small output capacitance, insulator substrate for small parasitic capacitances, and punch-through operation for high currents. Such a structure with a submicron gate length can be a fast logic gate, much faster than a MOSFET of the same size. Assuming a 0.5 μm thick SOS is used to fabricate a 5 μm drain source length and 1 μm gate length GFC-BARITT device and 5 μm gate length MOSFET, the speed fo the GFC-BARITT device is estimated to be 100 times faster than that of a MOSFET. A qualitative expression for the ratio of switching speeds of these devices is given by Eq. (5.2) :

$$\text{Switching speed of } \frac{\text{GFC-BARITT device}}{\text{MOSFET device}} = \frac{\text{Length of drain source}}{\text{Length of offset gate}} \; \frac{\mu_{\text{thin film}}}{\mu_{\text{surface}}} \; \frac{\text{Active layer thickness}}{\text{Inversion layer thickness}} \; . \tag{5.2}$$

Using an insulator substrate, sapphire in this case, has some disadvantages. If the processing parameters are not carefully chosen, such as the depths of the n^+ and especially the injecting junctions, p^+, the leakage currents will be high which results in high power dissipation. The reason for the high power dissipation of the ICL inverters in Fig. 5.14, is the high leakage current. If the depths of the n^+ and p^+ diffusions are shorter than the thickness of the

silicon film on sapphire, the leakage current will be increased with the increase of the applied bias voltage. This is, however, a relatively simple technological problem.

As shown in Section 5.5.5 the switching time of a logic gate (inverter) is determined by the average current of the individual devices, and the output capacitance. Therefore either inverter structure can be used to fabricate digital integrated circuits on III-V compound semiconductors. The GFC-diode in the ICL inverter and the GFC-BARITT device in the GFC-BARITT inverter are injection type devices and not gate-controlled resistances (FETs). In a FET, the current is directly proportional to the carrier mobility. The low mobility effect in injection devices (GFC-diode and -BARITT device) can be compensated for easily by the increase of the forward bias voltage. This means that the low mobility semiconductors can be used to fabricate high-speed switching devices. The role of the insulated gate in injection type devices is to deplete the channel, not to invert it. Therefore, it can be concluded that the two inverter schemes (ICL and GFC-BARITT) device inverters satisfy all the necessary physical and technological requirements to realize III-V compound semiconductor digital integrated circuits.

5.5.4 Delay Time. A simple approach is given below to calculate the delay time of an inverter with a capacitive load. The common delay time approximation is to find the charging or discharging times of the output capacitance with an average device current [78].

5.5.4.1 A GFC-BARITT Device Inverter. An inverter circuit with a capacitive load is shown in Fig. 5.16. The turn-on time, T_{ON},

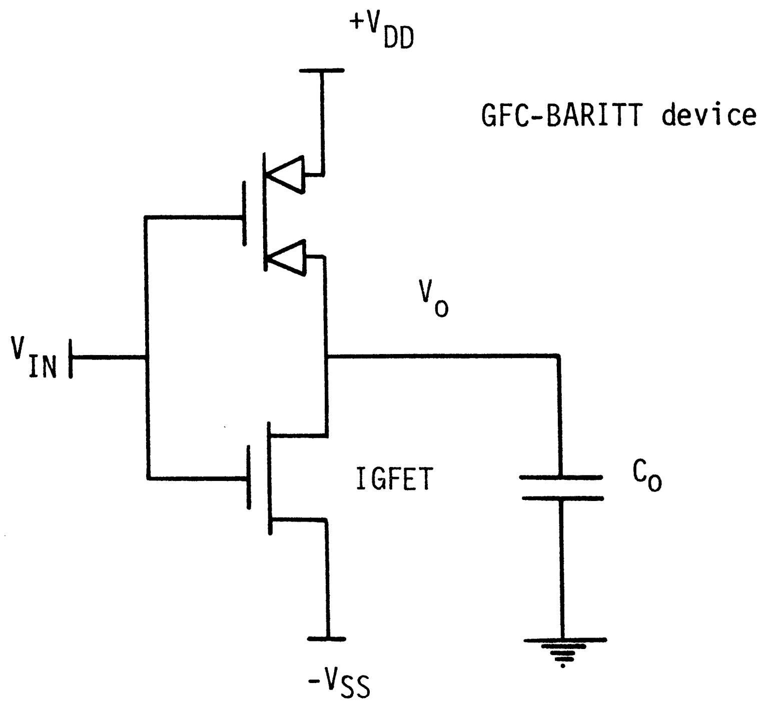


Fig. 5.16 GFC-BARITT Device Inverter Circuit with a Capacitive Load.

is defined as the charging time of the output capacitance, C_O, through the GFC-BARITT device:

$$T_{ON} = \frac{C_O V_O}{I_1} , \tag{5.3}$$

where V_O is the output voltage and I_1 is the average current which charges C_O and can be expressed as

$$I_1 = \frac{\int_{V_{O1}}^{V_{O2}} I_O \cdot DEXP[k_1(V_{DD} - V_O) - k_2 V_{IN}] dV_O}{\int_{V_{O1}}^{V_{O2}} dV_O} , \tag{5.4}$$

where V_{O1} is the initial output voltage and V_{O2} is the final output voltage which is less than V_{DD}. I_O, k_1 and k_2 are constants. If the gate length L_G is less than the distance between the source and the drain, L_{DS}, the maximum output voltage, V_{O2} is equal to the difference between V_{DD} and V_{PTG} (punch-through voltage for the distance of $L_{DS} - L_G$). Therefore,

$$V_{O2} = V_{DD} - V_{PTG} , \tag{5.5}$$

where

$$V_{PTG} = \frac{qN_D}{2\varepsilon_S} (L_{DS} - L_G)^2 .$$

If the gate extends from the source to the drain electrode, the capacitance is initially charged by a GFC-BARITT device when the output reaches $V_{DD} - V_{PT}$. In this case, the GFC-BARITT device operates in a MOSFET mode and it will charge the output capacitance up to $V_{DD} - V_{TH}$.

The main advantage of the GFC-BARITT device logic over a MOSFET logic is that initially the GFC-BARITT can supply a higher current than a MOSFET, which results in a shorter switching time. When the GFC-BARITT is turned on by applying a gate voltage in addition to the punch-through barrier lowering effect, the gate voltage further lowers the barrier against carrier injection.

The output level of a GFC-BARITT device inverter is lower than that of a MOSFET inverter.

5.5.4.2 Injection Control Logic. The delay time of the ICL can be estimated from the average charging and discharging time of the output capacitance also:

$$T_{ON} = \frac{C_O V_O}{I_1} , \qquad (5.6)$$

where I_1 the average current of the controlled diode can be expressed as

$$I_1 = \frac{\int_0^{V_O - V_{BB}} I_0 \exp(k_1 V'_{DS} k_2 V_{GS}) dV_O}{\int_0^{V_O} dV_O} . \qquad (5.7)$$

The turn-off time can be calculated by considering the discharging of the IGFET in the ICL circuit shown in Fig. 5.17. It is given by

$$T_{OFF} = \frac{C_o V_o}{I_2} , \qquad (5.8)$$

where I_2 is the average current of the IGFET and can be expressed as

$$I_2 = \frac{\int_{V_o}^{-V_{o1}} I_{DS} \, dV_o}{\int_{V_o}^{-V_{o1}} dV_o} . \qquad (5.9)$$

Both of these logic structures GFC-BARITT/SOS and ICL/SOS have the common $n^+n^-n^+$ IGFET as an active load. The turn-off or switching-off time for these two logic inverters is the same and is determined by the discharge time of the IGFET. There will be however a small difference in discharge time due to the difference of the output voltage levels in the ICL/SOS and GFC-BARITT/SOS. inverters.

5.5.5 Conclusion. A new ICL inverter scheme has been proposed and its principle of operation has been demonstrated. An ICL/SOS inverter with 19.6 ns and a CMOS/SOS conventional inverter of the same size with 30 ns gate delay time were fabricated. The ICL/SOS inverter is not only 1.5 times faster, but is also smaller than the CMOS/SOS inverter. On the other hand, a GFC-BARITT device inverter is even faster, 10 ns delay time, then an ICL. The reason

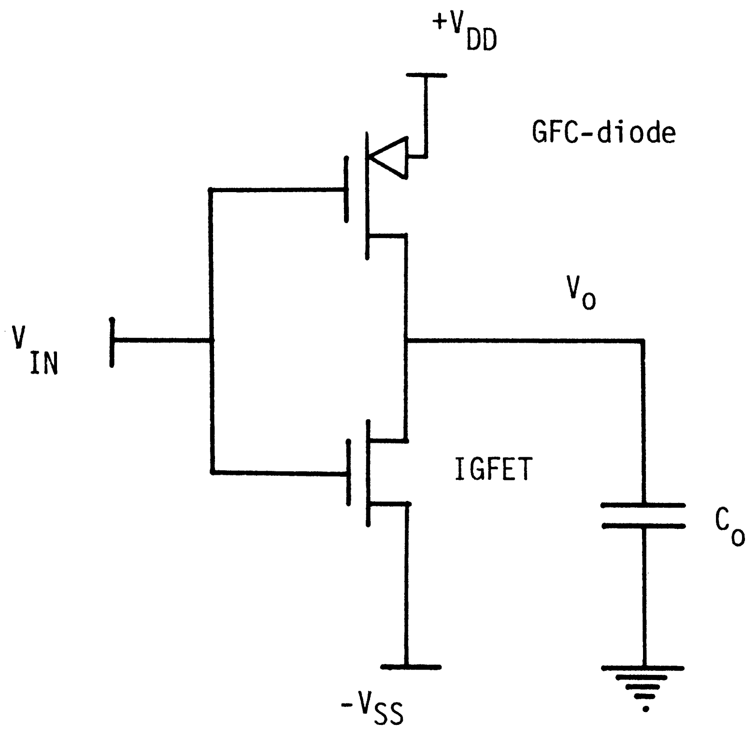
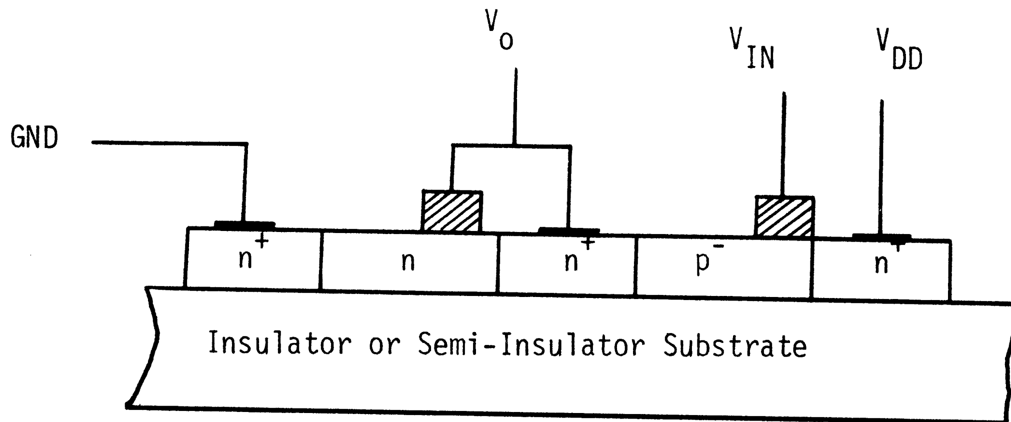


Fig. 5.17 ICL Inverter Circuit with a Capacitive Load.

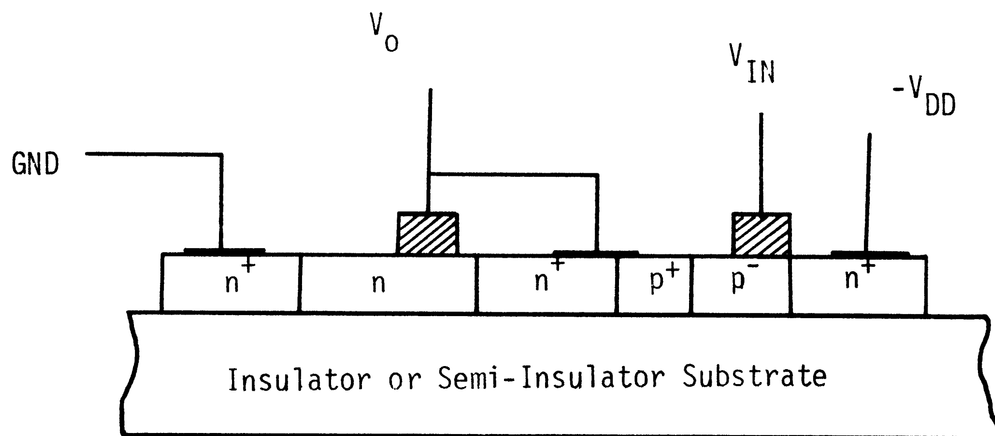
for the high power dissipation of the ICL/SOS inverter is the high leakage current at the silicon and sapphire interface. The leakage can be significantly reduced by making certain that the depths of the n^+ and p^+ regions are not shorter than the thickness of the silicon film on sapphire. As it is demonstrated in this study, there are two other possible high speed logic schemes other than a CMOS/SOS which are (i) an ICL/SOS and (ii) a GFC-BARITT/SOS.

The feasibility of ICL and GFC-BARITT device digital integrated circuits on III-V compound semiconductors was discussed, and it is concluded that it is possible to realize III-V compound semiconductor digital circuits with existing technologies simply by replacing the enhancement type MISFET with either GFC-BARITT devices or a GFC diode as shown in Fig. 5.18(a) and (b), respectively. These suggested logic schemes operate in a similar manner to a depletion/enhancement MOS logic. The reason for using the logic schemes shown in Fig. 5.18(a) and (b) is to utilize the high mobility electrons of III-V compound semiconductors. In Fig. 5.18(a) and (b), the $n^+n^-n^+$ IGFET must not be turned off at any time for the proper functioning of the inverter. As a result of this normally on $n^+n^-n^+$ IGFET, power dissipation will be high. Figure 5.18(a) and (b) represent a compromise between speed and power dissipation.

Even though the switching speed of a complementary logic structure from III-V compound semiconductors which is similar to the structure in Fig. 5.9, are not expected to be as fast as the one in Fig. 5.18 due to the low hole mobility. The power delay product of a complementary logic structure



(a) GFC-BARITT device logic.



(b) GFC diode logic.

Fig. 5.18 Inverter Structure for Semiconductors with High Electron Mobilities.

may be better than that of a structure shown in Fig. 5.18. Since GFC-BARITT device and GFC-diode can supply high hole current with a small gate-source capacitance, a III-V complementary structure which consists of one $n^+n^-n^+$ IGFET and one GFC-BARITT device or one GFC-diode, can switch μ_n (III-V)/μ_n (Si) times faster than their Si counterparts.

The advantages of using an insulated gate III-V compound semiconductor logic circuit over a MESFET logic are summarized as follows:

(i) For a small scale circuit GaAs MESFET logic circuits result in very impressive switching speeds, but MESFET circuits are not tolerant of process parameter variations [79]. Insulated gate structures have high tolerances against active layer thickness and the non-uniformity of the gate insulator.

(ii) Due to the forward-biasing problem of a Schottky gate, the logic swing of a MESFET logic is limited, but for insulated gate logic it is not.

(iii) It is not possible to fabricate a complementary low power MESFET logic circuit. The high power will limit the level of integration of the MESFET logic. On the other hand, GFC-BARITT devices or GFC-diode logic circuits can easily be coupled and the unit cell can be much smaller, therefore GFC-BARITT device or GFC-diode logic circuits can be integrated on a large scale easily.

(iv) The MESFET logic is limited to GaAs because it is much harder to form a Schottky gate on other III-V compound semiconductors with smaller energy band gap such as InP and $In_{1-x}Ga_xAs$. However, in the case of insulated gate devices there is no such limitation.

It can be concluded that the GFC-BARITT device and GFC-diode have some very promising digital circuits for high speed and low power circuit applications.

5.6 Comparison of the Theoretical and Experimental Results

All of the experimentally observed device characteristics were qualitatively predicted by the device theory, such as the mixed FET and punch-through operation of a SIT device, negative resistance in III-V compound semiconductor FETs and the geometry dependence of the device characteristics of all of the TTPT devices. In addition to the prediction of the experimental results, the effects of the various material parameters on the device performance have been studied. A simple and inexpensive simulation program, SIM-GFC, given in Chapter IV was proven to be a good tool for understanding the various punch-through devices. It is possible to predict the device performance under various operating conditions such as different temperatures, and also to evaluate the effect of the different material parameters before fabricating the device.

In Chapter IV the results of the computer simulation have indicated that the distance between the source and the gate is critical in controlling the injection of the carriers. If the gate is far from the source, the drain-source current cannot be modulated through a gate electrode. The experimental results of the GFC-BARITT device support the theoretical prediction. In Fig. 5.18, it is shown that a gate that is far from the source cannot control I_{DS}.

The experimental studies that were published about SIT devices can be explained theoretically. For instance, the field effect and the exponential characteristics of a SIT device are correctly predicted by the device theory and the results of the computer simulation are given in Chapter IV. The negative resistance in the I-V characteristics of the III-V compound semiconductor FET is an experimentally well-known fact. The impurity dependence of the mobility has been included in the theoretical calculations. As a result, the effect of the negative resistance on the I-V characteristics of the FETs with highly doped channels becomes negligible. In other words, the negative resistance effect is more pronounced for the lightly doped FETs. It is also known that the negative resistance in GaAs power MESFETs can be reduced using a highly doped material.

In addition to the study of the device physics, an accurate modeling of the device is also provided in SIM-GFC programs. The first three levels of the simulation program are devoted to the study of the basic device properties. The fourth level, however, is devoted to the accurate device modeling. To eliminate the errors in the calculation of the device parameter due to the simplifying assumptions, the critical variables such as forward bias voltage, V_F, is obtained from the measured dc I-V characteristics and used in the expressions for the small and large signal circuit elements. The approximated V_F values even with a small error, will induce, unacceptably large errors to the values of the calculated device parameters (C_{gs}, g_m, g_{ds}, C_{gd}). Because the device parameters

are exponentially dependent on the forward bias voltage. The most critical parameter is V_F. The extraction of this parameter from the measured dc I-V characteristic improves the device modelling and avoids the large discrepancies between the measured and the calculated device performance.

It can be concluded that the device theory predicts all the observed device properties conceptually. To avoid unacceptable errors in calculations of the equivalent-circuit parameters of the TTPT devices, the most critical parameter, V_F, is obtained from the measured dc I-V characteristics. The computer program SIN-GFC contains the solution of a very general and flexible analytical device expression, and also an accurate model of the TTPT devices.

CHAPTER VI. CONCLUSIONS AND SUGGESTIONS FOR FURTHER STUDY

In the course of this dissertation the following conclusions have been reached:

1. The principles of the operation of minority and the majority carrier TTPT devices are similar. They all involve control of the injected carriers via a junction, an ohmic or an insulated gate electrode.

2. Common device expressions can be used to calculate various TTPT device characteristics (Chapter II).

3. The barrier height of the injecting junctions is nonuniform across the source-channel junction. As a result of the non-uniform V_F, the current density is also non-uniform across the device thickness. This is true for all TTPT devices.

4. The level of the carrier injection in the GFC-BARITT devices is material dependent. At the same bias conditions, the carrier injection in the same size GFC-BARITT device made of a semiconductor with a smaller energy band gap such as Si is higher than that made of a larger energy band gap material such as InP and GaAs. The carrier injection in SIT devices is not energy band gap dependent.

5. The TTPT devices utilize the saturation velocity, therefore using semiconductors other than silicon to fabricate a TTPT device is not significant.

6. FETs were considered as a special mode of operation of SITs. At low bias voltages, GaAs FETs give the best performance,

highest g_m and cut-off frequency, but at high bias voltages, InP FETs can operate at the highest frequency and gain due to its higher peak velocity and saturation velocity than those of GaAs FETs.

7. The most critical geometrical parameter in TTPT devices is the source-gate spacing, W_{GS}. If W_{GS} is large, the drain-source current cannot be modulated through the gate voltage.

8. An increase in channel doping concentration decreases the drain-source current, I_{DS}, and the breakdown voltages in GFC-BARITT devices. At high channel doping concentrations, the SIT device operates as a conventional FET. In any mode of operation of a SIT device, increased channel doping reduces the drain-gate and source-gate breakdown voltages.

9. A small signal model for TTPT devices was developed including the noise figure.

10. A simple non-iterative large signal model was also proposed and demonstrated for the conventional FET device.

11. The principles of operation of various GFC-BARITT devices such as junction and Schottky barrier drain-source type GFC-BARITT devices on Silicon on Sapphire (SOS) have been proven (Chapter V). It was also shown that the GFC-BARITT devices are better than other TTPT devices for digital IC applications.

12. The switching speed if GFC-BARITT devices on SOS was shown to be faster than that of the same size MOSFET, due to its high current capability.

In this study, the understanding of the various TTPT and FET device characteristics have been accomplished and their use in high-speed digital circuit applications was proposed and demonstrated.

There are, however, several additional topics which need further exploration. Some of these topics are:

1. A full two-dimensional simulation program to study the potential and also the carrier distribution in TTPT devices.

2. Experimental study of the small and large signal properties of TTPT devices.

3. Fabrication of the same size GaAs, InP and Si TTPT devices to compare their performances.

4. Development of a practical large signal model to use as a design tool for microwave circuit design.

5. Fabrication of small size devices to determine the maximum switching speed of the GFC-BARITT device.

6. Application of III-V compound semiconductor TTPT devices in various high-frequency and high-speed circuits.

7. Study of a GFC-BARITT device as a gate-controlled negative resistance device.

APPENDIX A. FACR METHOD

The Fourier Analysis/Cyclic Reduction (FACR) direct method is based on performing a Fourier analysis in one direction (say the x-direction) followed by the solution of the harmonic equations in the other direction, using cyclic reduction [16]. If the boundary conditions are simple enough, then sines and cosines are the eignefunctions of the operator and the harmonic equations are uncoupled. The harmonic equations can then be solved separately and rapidly. Hence, the algorithm is as follows: The harmonic components of the charge are obtained from Fourier analysis of the given charge. Given the harmonic components of the charge, the harmonic equations for the harmonic components of the potential can be solved. The desired potential is then obtained by Fourier synthesis.

The simplest finite-difference approximation to Poisson's equation in two dimensions is that obtained from the "five-point" difference formula, namely,

$$\frac{(\phi_{s-1,t} - 2\phi_{s,t} + \phi_{s+1,t})}{Hx} + \frac{(\phi_{s,t-1} - 2\phi_{s,t} + \phi_{s,t+1})}{Hy} = \rho_{s,t}/\varepsilon_s \quad , \tag{A.1}$$

$$0 < s < Nx \quad , \quad 0 < t < Ny \quad ,$$

where Hx is the mesh spacing along the x-axis, and Hy is the mesh spacing along the y-axis, $\phi_{s,t}$ is the potential, and $\rho_{s,t}$ is the charge at each mesh point.

To simplify the mathematical description of the method, it is assumed that the mesh is a square (Hx = Hy), and the boundary conditions are periodic in the x-direction and given values in the y-direction. The original difference equations may then be written as

$$\phi_{t-1} + A\phi_t + \phi_{t+1} = q_t \quad , \qquad 0 < t < Ny \quad , \tag{A.2}$$

where the vectors ϕ_t and q_t are the potential and right-hand side for the 'row t' of the mesh:

$$\phi_t = \begin{bmatrix} \phi_{ot} \\ \phi_{1t} \\ \phi_{Nx-1,t} \end{bmatrix} \quad , \qquad q_t = \begin{bmatrix} q_{ot} \\ q_{1t} \\ q_{Nx-1,t} \end{bmatrix} \quad .$$

The steps of the FACR algorithm are:

(i) odd/even reduction,

(ii) Fourier analysis on even lines,

(iii) recursive cyclic reduction

(iv) Fourier synthesis on even lines and

(v) solution on the odd lines.

FORTRAN programs written by Hockney, POT1 uses FACR to solve the two-dimensional Poisson's equation.

1. Odd/even reduction:

Consider the three neighboring equations

$$\phi_{t-2} + A\phi_{t-1} + \phi_t = q_{t-1} ,$$

$$\phi_{t-1} + A\phi_t + \phi_{t+1} = q_t \qquad t \text{ even} , \qquad (A.3)$$

$$\phi_t + A\phi_{t+1} + \phi_{t+2} = q_{t+1} .$$

From the above equations odd lines can be omitted and formulas in Eq. (A.3) is reduced to a single one as in Eq. (A.4):

$$\phi_{t-2} + (2I - A^2) \cdot \phi_t + \phi_{t+2} = q_t^* , \qquad (A.4)$$

where A is the "five-point" difference operator. The modification is performed by the subroutine RHSE in POT1.

2. Fourier analysis on even lines:

A real finite Fourier analysis is performed on the even-line equations according to the transformation:

$$\phi_{s,t} = \frac{1}{2}\phi^c_{o,t} + \frac{1}{2}\phi^c_{Nx,2,t}(-1)^s + \sum_{k=1}^{Nx/2-1} \phi^c_{k,t} \cdot \cos\frac{2\pi k \cdot s}{Nx}$$

$$+ \phi^s_{k,t} \cdot \sin\frac{2\pi \cdot k \cdot s}{Nx} , \qquad (A.5)$$

where the harmonic components are given by

$$\phi^{c}_{k,t} = \frac{2}{Nx} \sum_{s=0}^{Nx-1} \phi_{s,t} \cos\left(\frac{2\ \pi\ k \cdot s}{Nx}\right)$$

and

$$\phi^{s}_{k,t} = \frac{2}{Nx} \sum_{s=0}^{Nx-1} \phi_{s,t} \sin \frac{2\ \ ks}{Nx} \quad .$$

This is a linear matrix transformation on the original data.

Substituting (A.5) into the even-line equations (A.4) and using the finite orthogonality relations of the harmonics one obtains

$$\phi_{k,t-2} + \lambda_k \phi_{k,t} + \phi_{k,t+2} = q^{*}_{k,t} \qquad t \text{ even} \ , \qquad (A.6)$$

where ϕ and q^{*} refer to either the sine or cosine harmonic and

$$\lambda_k = -2(8 - 8 \ \cos \frac{2\pi k}{Nx} + \cos \frac{4\pi k}{Nx}) \ .$$

Ny and Nx are the numbers of mesh points along the y-axis. This step is performed by the subroutine FOUR67.

3. Recursive cyclic reduction.

The equation (A.6) forms a tridiagonal system and can be solved by the recursive application of the process of cyclic reduction. The cyclic reduction method is better that the Gaussian elimination method for the periodic boundary conditions (less storage). Subroutine CRED does the cyclic reduction in POT1.

4. Fourier synthesis on even lines.

The recursive cyclic reduction determines the value of all the harmonic amplitudes of the potential on the even lines of

the mesh. A Fourier synthesis is performed on the even lines to obtain the values of the potential on those lines. Subroutine FOUR67 does the Fourier synthesis.

5. Solution on the odd lines.

The solution for the potential on the odd lines can be found from the original odd-line equations in Eq. (A.1) by putting the known values of the neighboring even lines on the right-hand side. Subroutine RHSO rearranges (A.1) by putting known values to the right-hand side and CRED cyclic reduction subroutine is used to solve the potentials on even lines.

The program POT1 calculates the two-dimensional potential distribution on a rectangular (x,y) mesh ($N_x \neq N_y$) where the mesh spacing may be unequal ($H_x \neq H_y$). The number of points computed may be either $(N - 1)$, N or $(N + 1)$, depending on the boundary conditions. In any case, N is restricted to a power of two ($N_x = 2^{IQX}$, $N_y = 2^{IQY}$.

The boundary conditions are

(i) IBCX = 1. The potential has given values placed on $\phi_{o,f}$ and $\phi_{Nx,t}$ before calling to subroutine POT1.

(ii) IBCX = 2. The field is zero at s = 0 and s = Nx. It converts the charges $q_{o,t}$ to $q_{Nx-1,t}$ on mesh points zero to Nx-1, to values of potential.

(iii) IBCX = 3. All variables are periodic in x, $\phi_{-s,t} = \phi_{Nx-s,t}$. The routine converts the charges $q_{o,t}$ to $q_{Nx-1,t}$, initially given on mesh points zero to Nx-1, to values of potential.

There are similar definitions for IBCY = 1,2,3. The required inputs to the program are values of IQX, IQY, Hx, Hy, IBCX, IBCY and the charge distribution.

APPENDIX B. SIM-GFC PROGRAM

The SIM-GFC program can be used to study the various properties of TTPT devices and FETs.

SIM-GFC program can simulate:

(A) Different devices;

- (i) GFC-BARITT device
- (ii) SIT and
- (iii) FET.

(B) Different device structures;

- (i) Geometry
- (ii) Doping
- (iii) Junction type
- (iv) Gate type, and
- (v) Gate insulator type in GFC-BARITT device

(C) Different semiconductor devices

- (i) Silicon
- (ii) GaAs
- (iii) InP, and
- (iv) Others

(D) Doping effect on device

- (i) Performance (mobility and velocity)
- (ii) Breakdown voltage
- (iii) Mobility and velocity

(E) Different operation temperature effect on

(i) Intrinsic carrier density

(ii) Energy band gap

(iii) Mobility and velocity

(F) Dc and small signal equivalent circuit

(i) I_{ds} vs V_{DS} of a function of V_{GD}

(ii) G_M, G_{DS}

(iii) C_{GS}, C_{GD}, C_{DS}

(G) Small signal device performance

(i) Maximum available gain

(ii) Maximum unilateral gain

(iii) Cut-off frequency ($g_m/\omega \cdot C_{gs}$)

(iv) 360 degrees phase difference in frequency

(v) Noise figure

(vi) Noise measurement

(H) Large-signal circuit elements

(i) Average ac current in one RF cycle

(ii) Average GM, GDS

(iii) Average CGS, CGD, CDS

(I) Large signal device performance

(i) Collector efficiency

(ii) Added power efficiency

(iii) Power gain

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