Maskless Laser-Write Lithography of a-Si:H TFT Passive Pixel Sensor for Hemispherical Imager

by

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Chapter 1

Introduction

1.1 Motivation/Overview

Recently there has been growing interest in solid-state image sensors due to enormous demands for mobile-imaging, digital and video cameras, surveillance, and medical imaging applications. Charge-coupled devices (CCDs), invented 1969, dominated the market due to a great quality of images. In addition to a high cost, the CCDs have a major drawback: incompatibility with the complementary metal oxide semiconductor (CMOS) technology [1]. So the recent advances of CMOS processing drive the development of image sensor in combination with the CMOS technologies. Today's CMOS image sensor is based on the work done from the mid 1980s at VLSI Vision Ltd. and the Jet Propulsion Lab (JPL) [1]. Until the early 1990s, the passive pixel sensor (PPS) was the first choice due to the feature size limitation of CMOS technologies [2]. In mid-1990s active pixel sensor (APS) technology became mature, and APS architecture becomes the key of CMOS image sensor with a high speed, less image lag, and a low power-consumption in comparison to CCDs [3]. Today this technology has been adopted in most of commercial products requiring compact and light-weight image sensors.

For a large area application such as security and medical imaging, the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) flat panel imagers based on a passive pixel sensor (PPS) concept have been used [4, 5]. Indeed a-Si:H TFT is a well proven technology for fabricating electronics over a large area that is widely used for flat panel displays and x-ray

sensors [5-7]. Although it is possible to realize a large area high performance imager by tiling a number of CCDs and/or CMOS image sensors [8], the cost benefit of a large area a-Si:H TFT fabrication process makes a-Si:H TFT flat panel imager much more attractive than other approaches. So far, all the current state-of-the-art image sensor technologies have been developed on flat surfaces because CMOS and TFT technology are developed either for a rigid silicon wafer or glass substrate.

Image sensors on flat surfaces have a planar focal plane array (FPA); FPA is an array of light-sensing pixels at the area where light is focused (focal plane). The planar FPA induces optical aberrations, which are deviations of the performance of an optical system from the prediction of optics [9], consequently leading to a distorted and blurred image compared to an original image. To correct this problem, additional optical elements and shaped lenses are necessary, resulting in the complicated and expensive optical system. Recently, there has been increasing research activities on unique advantages of image sensor to be fabricated on a spherical surface: a wide field-of-view (FOV), low optical aberrations with less optical components in the system, compact, and light weight [10-13], resulting in a lower cost. The low optical aberrations are attributed to that the surfaces of a spherical imager as well as ball-shaped lens are spherical and symmetric to the center of an optical system. This allows that all points on the imager are on-axis points without additional lenses, consequently contributing to simplify the optical system [14].

Figure 1.1 compares the performance of three camera systems that consists of different shaped-lenses and curved or planar FPAs in modulation-transfer-function (MTF) plots. MTF represents how accurately the lens transfers contrast of the object to the image produced by the lens; basically, the higher MTF number, the more accurate image. In Figure 1.1 (a-c), MTFs of diffraction limited systems (black dotted lines), image points on axis (red), tangential image point (solid lines) at 0.4 field (green) and 0.7 field (blue) and satittal image points (dashed dots) at both 0.4 and 0.7 fields are shown [13].

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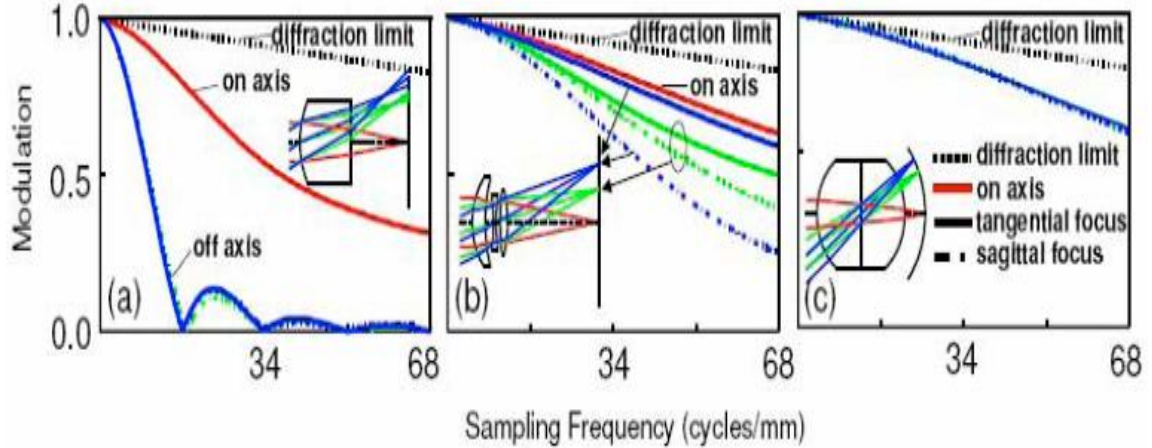
Figure 1.1 Modulation transfer functions (MTFs) of (a) a simple plano-convex lens with planar FPA, (b) Cooke triplet lens with planar FPA, (c) a ball-shaped lens with curved FPA (Adopt from [13]).

Aforementioned advantages demand the implementation of electronic and optoelectronic systems on non-planar or hemispherical surfaces. As illustrated in Figure 1.2, therefore, various approaches have been proposed to realize functional devices on those surfaces: a) transfer-based fabrications, b) self-assembly, c) interconnection of device tiles, and d) contact patterning methods.

a. Transfer-based fabrication: i) devices are fabricated on flexible substrates and then transferred by deformation onto curved substrates [15, 16]. ii) contact-transfer printing has been applied to transfer only functional devices, not the entire flexible substrate [17].

b. Self-assembly: functional devices are fabricated and prepared as individual components. Solder-based or complementary shape recognition assembly with the aid of capillary and/or gravitational force is used to integrate the components onto flexible substrates [18-20].

c. Interconnection of device tiles: standard fabrication process is conducted on silicon wafer. The processed wafer is diced by dry-etching on the back side, and the formed "tiles" are bridged by metal leads. Finally the wafer of the tiles is curved using an elastomeric mold [21].

d. Contact patterning method: soft-lithography is a representative example. First step is to build patterned stamps and molds as pattern transfer elements. A printing method with the prepared stamps/molds is used to form patterns on curved surfaces. It has advantages of being adaptable to substrate shape and generating conformal contact with the contour of curved substrates [22- 24].

Although the proposed methods have demonstrated feasibility of the fabrication of functional devices on non-planar surfaces, they are not desirable to realize complex device structures and circuits for high-resolution pixel arrays with various components. These strategies are limited by the following: difficulty with the preparation of transferable functional devices or individual components (a, b) due to the limitation of process temperature and strain associated with local deformation; lack of scaling capability (a, c, d); poor registration accuracy and layer-to-layer alignment accuracy (a, d); difficulty with interconnection to readout electronics (a, b). The pixel circuit's dimensional changes with the curvature should be considered in the fabrication of the hemispherical image.
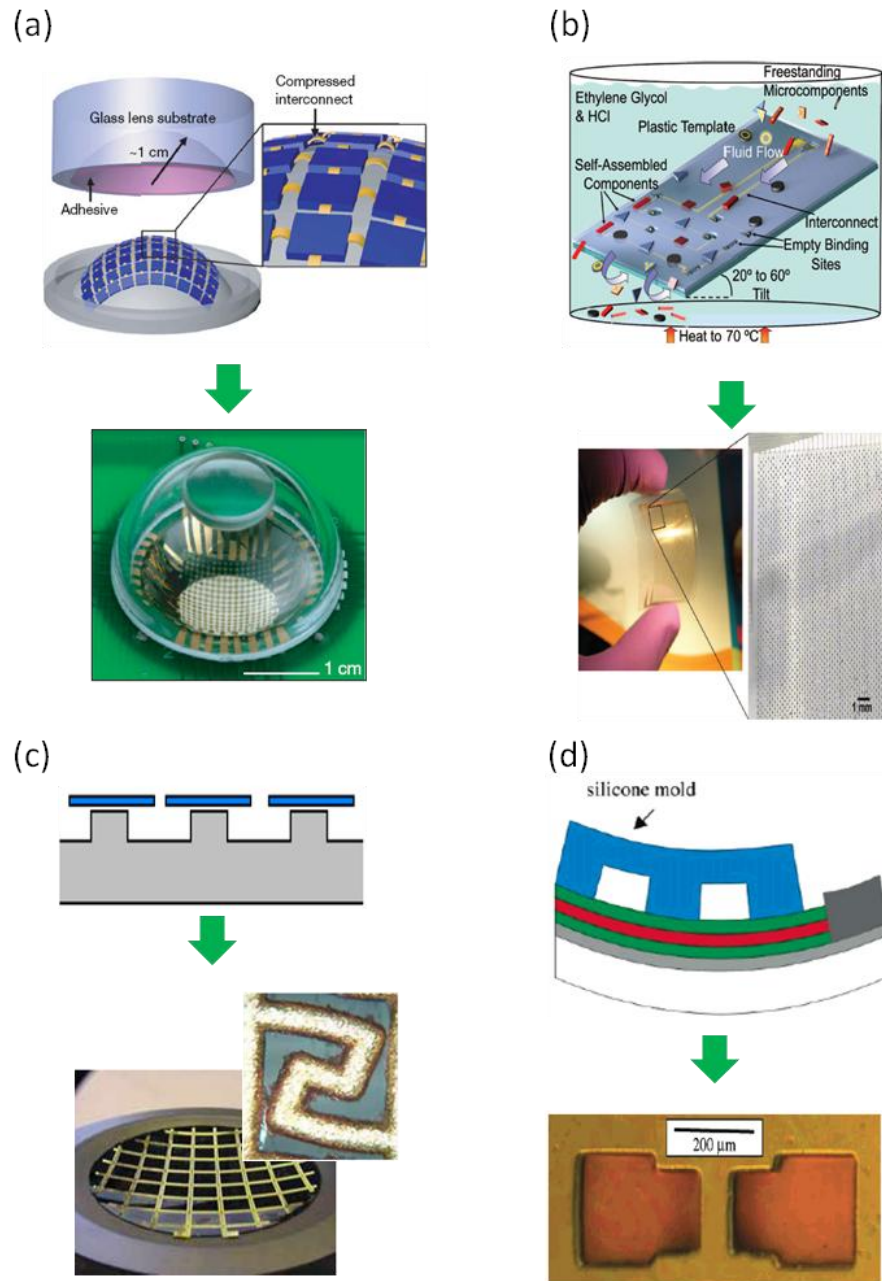
Figure 1.2 Various approaches proposed to realize functional devices on non-planar surfaces: (a) transfer-based fabrication [15] (b) Self-assembly [20] (c) Interconnection of devices tiles [21] (d) Contact patterning method [24].

The standard photolithography obviously cannot be used for non-planar surfaces because of the substrate curvature. To circumvent aforementioned difficulties and limitations, we need a direct fabrication method based on non-contact patterning. The maskless laser-write lithography (LWL) can be an alternative approach; the LWL is a direct fabrication method free from the stress and/or deformation issues which are inevitably involved in the transfer-based fabrication; the LWL can provide a submicron feature size with a very accurate registration and alignment capability. With extensive modification, the capability of LWL process on curved substrates has been demonstrated at a single-level mask step [25, 26], and can be extended for multi-level alignment and process. Therefore, it can be a very attractive and promising approach to fabricate high-performance functional devices and circuits on a non-planar surface.

1.2   Organization of Dissertation

This dissertation commences in **chapter 2** by introducing and discussing electrical properties and instability of advanced a-Si:H TFT structures for sensor application. The asymmetric electrical properties and instability of fork TFTs are investigated in depth. The instability of single and multiple HEX-TFTs is discussed, and their relationship is established. In **chapter 3**, we demonstrate the feasibility of using the LWL system with accurate level-to-level alignment in the fabrication of a-Si:H TFTs on a planar surface. Furthermore we describe what modification should be made for the expansion of the proposed LWL method into non-planar fabrication processing. We evaluate the modified LWL system in structuring on a curved surface. In **chapter 4**, we successfully demonstrate the fabrication of a-Si:H TFTs on a curved surface. The extensively modified LWL system is used, and the fabrication steps are described in detail. The fabricated TFTs show good enough electrical performance for application such as high-resolution and large-array devices. In **chapter 5**, electrical stability of a-Si:H TFTs fabricated on a curved

surface with enhanced field of view is studied in depth under various and prolonged bias-temperature stress. Furthermore we compare the obtained results with a-Si:H TFT fabricated on a flat surface using the same fabrication steps. In **chapter 6**, we fabricate a-Si:H TFT passive pixel sensor (PPS) circuits on a curved surface, and characterize their electrical instability and properties. SPICE model is developed and used for a comparison between measured and simulated data. In **chapter 7**, 50 µm pitch 128 x 128 a-Si:H TFT PPS is fabricated, and mask design and fabrication process are described in detail. Electrical characteristics and instability of the a-Si:H TFT pixel switch are characterized and discussed. Lastly expected opto-electronic properties of the organic photodiode to be integrated and PPS imager are elaborated. My dissertation is concluded and future research works are recommended for realizing a-Si:H TFT hemispherical imager in **chapter 8**.

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Chapter 2

Advanced a-Si:H Thin-Film Transistor Structures for Sensor Application

2.1 Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been extensively used in pixel circuits for large-area flat-panel displays and x-ray imagers due to excellent spatial uniformity and low fabrication cost [1, 2]. To use such devices for analog amplifiers, switches, and active-matrix organic light-emitting diodes (AM-OLEDs), a higher drain current and/or better electrical stability under prolonged bias stress are required [3,4]. For given channel length of a standard TFT, a higher drain current can be achieved by increasing TFT channel width using advanced TFT structures; fork, Corbino, and hexagonal (HEX) a-Si:H TFT [5-7]. *Lee et. al* proposed Corbino and hexagonal (HEX) a-Si:H TFTs to achieve large channel width without scarifying device electrical stability [6,7].

Such device designs provide a larger pixel aperture ratio (e.g. less pixel area occupation) and smaller parasitic gate-to-source capacitance compared to a standard TFT's for given channel width; in other words, they can provide more space for a storage capacitor and larger gate-to-drain capacitance, which are comprising and leading to a larger pixel capacitance. Furthermore, it is known that TFTs with the asymmetric source-drain electrode have better electrical stability (e.g. less threshold voltage shift) compared to the standard TFT for the same channel width to length (*W/L*) ratio at proper bias conditions [8]. These are promising characteristics for a high-resolution

sensor array application, requiring larger pixel capacitance to accumulate more signal charges and less threshold voltage shift.

With aforementioned advantages, it is essential to study electrical properties and to evaluate electrical instability of fork and HEX-TFTs in depth. In this chapter, we present asymmetric electrical properties and instability of fork a-Si:H TFT depending on drain bias polarity. We also report on geometrical effects of TFT on the extraction of key device electrical parameters. Then we study in detail current-temperature-stress (CTS) induced electrical instability of single and multiple HEX-TFTs. We measure threshold voltage shift (ΔV_{th}) of single HEX-TFTs and investigate their contribution to overall ΔV_{th} of multiple HEX-TFTs. Asymmetric electrical properties of HEX-TFTs were described by *H.Lee et. al.* elsewhere in details [7].

2.2   Fabrication of Fork and Hexagonal a-Si:H TFT

The fork and HEX a-Si:H TFTs were fabricated using the normal AM-LCD 5-photomask process steps (Figure 2.1 and 2.2). More specifically, on the Corning Eagle2000 glass substrate, bi-layer of molybdenum (Mo, 500Å) and aluminum-neodymium alloy (AlNd, 2000Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet-etching (Mask #1). Following gate electrode definition, hydrogenated amorphous silicon nitride (a-SiN$_X$:H, 4000Å)/a-Si:H (1700Å)/phosphor-doped a-Si:H (n$^+$ a-Si:H, 300Å) tri-layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form gate insulator and active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (Mask #2), a chromium (Cr, 1200Å) layer was deposited by sputtering, and source/drain (S/D) electrodes were patterned by wet-etching (Mask #3). Using S/D metal and photo resist as masks, the back-channel-etching by RIE was performed. Then, we deposited a-SiN$_X$:H (3000Å) as a

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passivation (PVX) layer by PECVD at 300 ℃. To realize an electrical contact to electrodes (source/drain and gate), vias were formed through the PVX layer by RIE (Mask #4). After contact vias definition, ITO (500Å) was deposited by a sputtering method at room temperature, and then pixel electrodes and probing pads were patterned by wet-etching (Mask #5). As a final step, the thermal annealing was performed for an hour at 235 ℃.
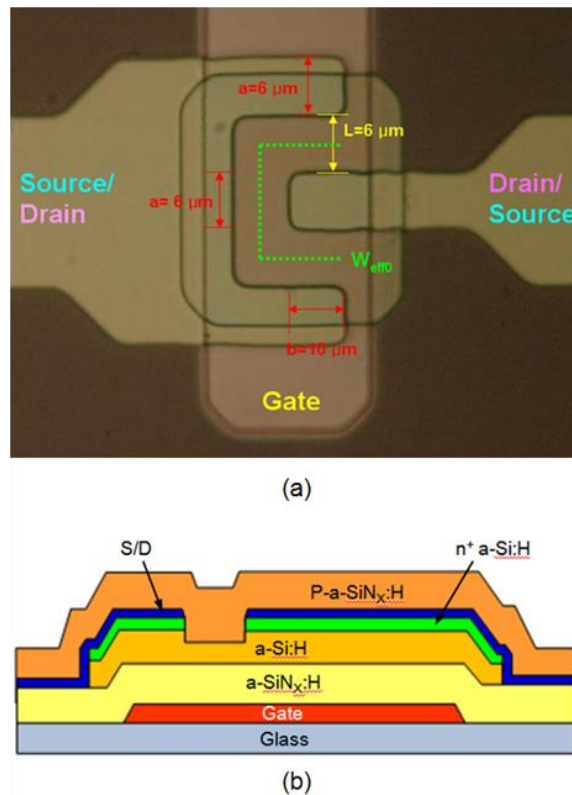
Figure 2.1 The fork TFT: (a) optical photograph of top view and (b) schematic of cross-sectional view.
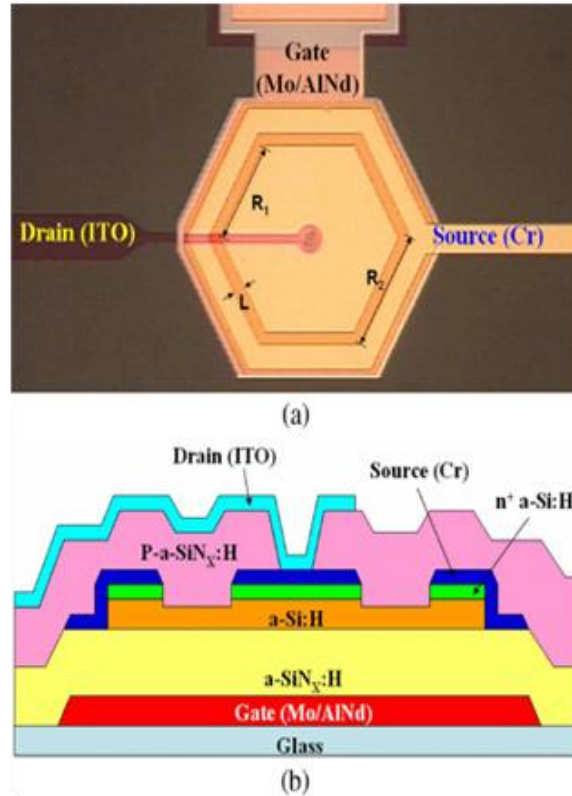
Figure 2.2 The HEX TFT: (a) optical photograph of top view and (b) schematic of cross-section view.

2.3 Electrical Properties and Instability of Fork a-Si:H TFT

2.3.1 Experimental results

To characterize the electronic properties of fork a-Si:H TFT, we first measured the transfer characteristics of fork a-Si:H TFT; we swept the gate bias from 25 to 0 V, and swept again from 0 to 25 V for various drain voltages (0.1, 1, 10, and 20 V). As shown in Figure 2.3, at low drain voltage (V_{DS}<1V), the ON-currents are identical for both cases. However, at high V_{DS} (> 10V), the ON-currents for case (1) are higher than for case (2). Therefore, regardless of gate bias and direction of drain bias applied, the ON-currents would be the same for a low drain bias. However,

when we apply a high drain bias, the ON-current levels can be increased significantly depending on the drain-bias direction. However, at the same time, as the drain bias is increased from 0.1 to 10V, the OFF-currents for both case (1) and (2) showed identical behavior regardless of drain biases; they increased from $\sim 10^{-13}$ to $\sim 10^{-12}$ A. During gate bias sweeping, no significant hysteresis (ΔV_{GS}) in current-voltage characteristics was observed for both cases; at V_{DS}=10V and I_{DS}=0.1nA, both cases showed ΔV_{GS}= 0.5V $_{case(1)}$ and 0.46V $_{case(2)}$.
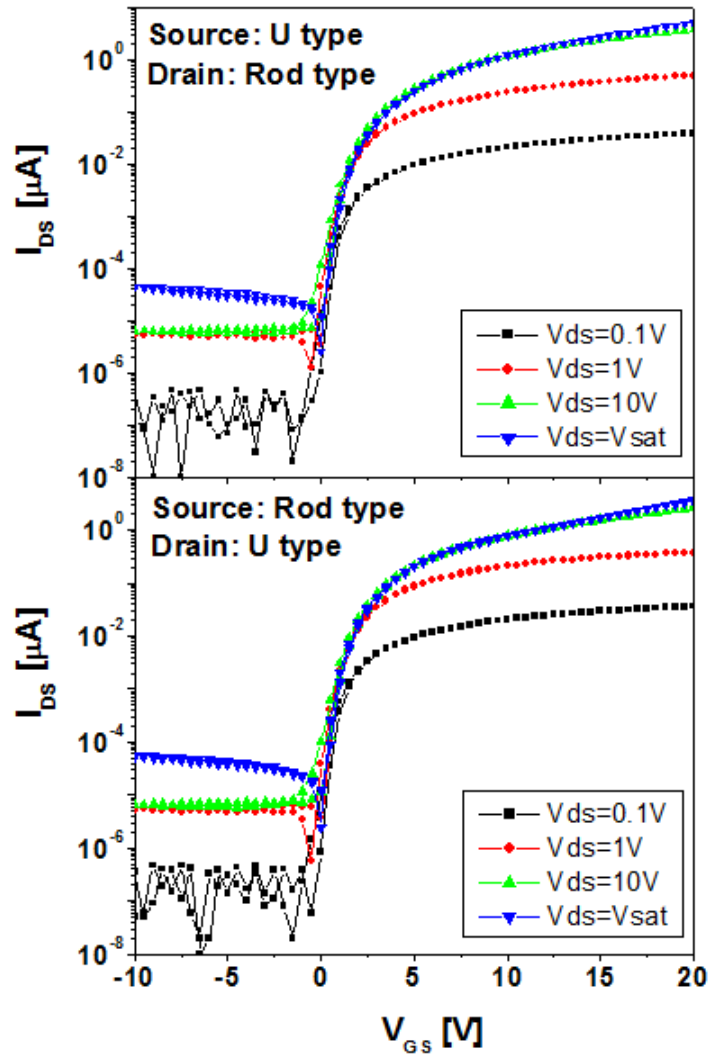
Figure 2.3 Transfer characteristics of fork a-Si:H TFT for various V_{DS}.
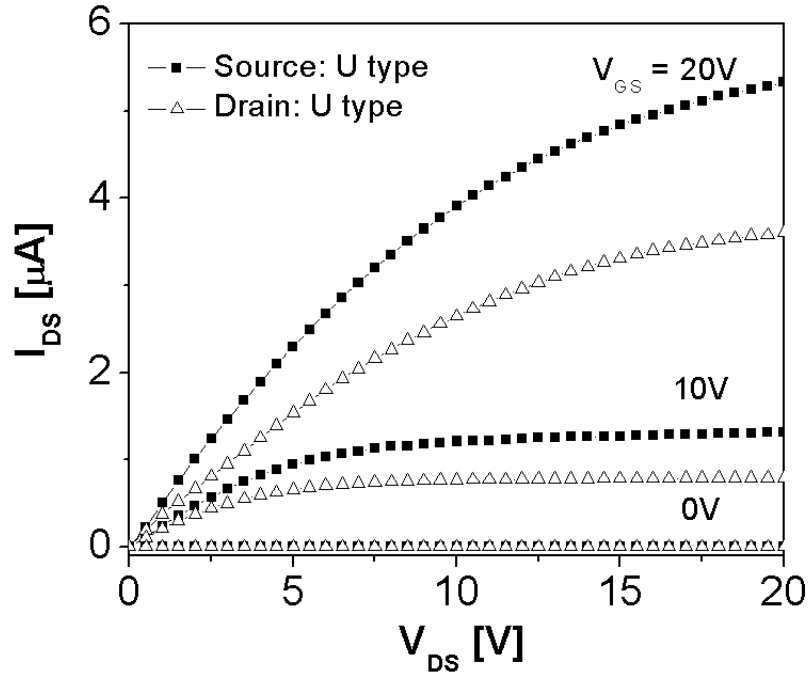
Figure 2.4 Output characteristics of fork a-Si:H TFT for various V_{GS}.

Next, we measured output characteristics (Figure 2.4) by applying the drain bias under following conditions: (1) ground was applied on the outer U-shaped source electrode and drain voltage was applied on the inner rod-shaped drain electrode; (2) drain voltage was applied on the outer U-shaped drain electrode and ground was applied on the inner rod-shaped source electrode. We swept the drain bias from 0 to 20 V for various gate voltages (0, 10, and 20 V). As shown in the Figure 2.4, at V_{DS}=20 V and V_{GS}=20 V, the output current for case (1) (= 5.3 μA) is 1.5 times higher than for case (2) (= 3.6 μA).

2.3.2 Discussion of fork a-Si:H TFT geometry effect

The asymmetric behaviors of fork a-Si:H TFT described above can be explained as follow. As the gate bias increases, a channel is formed in the active a-Si:H layer at the interface with the

gate insulator. At low V_{DS} (~1V), since the channel is not affected by the drain voltage, the whole channel remains as the accumulation layer. Hence, effectively the shape and length of the channel would be the same for both drain bias polarities, and we can define the device effective width W_{eff0} (= a + 2b + 2L) as the peripheral line of the middle of the channel between source and drain electrodes as shown in Figure 2.1(a), where a is the width of rod electrode, b is the overlapping distance between source and drain electrode, and L is the channel length. This effective width can be used in both cases to extract the device field-effect mobility at low V_{DS} (linear regime) based on the ideal MOSFET model. The drain current is assumed to be constant at distance y from the drain electrode and can be expressed as $I_{DS} = W_{eff0}J_y$, where the current density J_y is a function of electric field E_y and potential V_y: $J_y = \sigma E_y = \sigma dV_y/dy$. The resulting differential equation for the potential is expressed as

$$dV = \frac{I_{DS}}{W_{eff0}\sigma}dy \tag{2.1}$$

where the conductivity $\sigma = \mu_{FE}C_{OX}[(V_{GS}-V_{TH})-V_y]$, C_{OX} is the oxide capacitance, μ_{FE} is the field-effect mobility, V_{GS} is the gate bias, and V_{TH} is the threshold voltage of TFT. The integration of (2.1) from 0 to L yields the potential drop between the source and drain electrodes as

$$\int_o^{V_{DS}} [(V_{GS} - V_{TH}) - V_y]dV_y = \frac{I_{DS}}{W_{eff0}\mu_{FE}C_{OX}}\int_0^L dy \tag{2.2}$$

Hence, the drain current for both-bias polarity can be expressed as

$$I_{DS} = \frac{W_{eff0}C_{OX}\mu_{FE}}{L}\left[(V_{GS} - V_{TH})V_{DS} - V_{DS}^2/2\right] \tag{2.3}$$

However, output and transfer characteristics at high V_{DS} (>10V) are quite different from those measured at a low V_{DS}. As discussed above, at high V_{DS}, ON-current is higher for drain bias

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condition (1) than drain bias condition (2). Assuming the device is ideal crystalline silicon MOSFET and field-effect mobility remains identical for both conditions, the current flowing through TFT can only be strongly dependant on the value of channel width and length. Therefore, at high V_{DS}, we need to define different geometrical factor f_g for each drain bias condition to accommodate for differences in device electrical properties. When TFT is operating in the saturation regime at high V_{DS}, we can assume the channel depletion region at the drain electrode would be increased by a certain value. This change is referred to as channel length modulation factor (ΔL). However, in fork a-Si:H TFT, due to the unique device geometry, we can expect that ΔL would be different depending on the drain bias condition; the position of drain and source electrodes [9]. If the drain bias fully depletes the channel by ΔL from the edge of drain electrode, the electric field at the depletion region edge of drain electrode can be expressed by the gauss' law; the charge contained in a volume (ρ) equals to the permittivity ($\varepsilon_{a\text{-}Si}$) of a-Si:H times the electric field emanating from the volume:

$$\oint \rho dV = \varepsilon_{a-Si} E \tag{2.4}$$

If the drain bias creates the same number of the depletion-region charge per unit volume (Q_d) for both drain bias conditions, the electric field for each condition can be expressed by,

$$E_1 \cong \frac{Q_d \times x_i \times (a + 2\Delta L_1) \times (b + \Delta L_1)}{\varepsilon_{a-Si}} \tag{2.5a}$$

$$E_2 \cong \frac{Q_d \times x_i \times [2(a + 2\Delta L_2) \times (b + \Delta L_2) + (a + 2L - 2\Delta L_2)\Delta L_2]}{\varepsilon_{a-Si}} \tag{2.5b}$$

where x_i is the depletion width of drain depletion region and W_R is the width of the outer ring electrode. Therefore, if the electric field at drain depletion region would be same for both conditions ($E_1=E_2$), since the size of drain electrode is larger for condition (2) than for condition

(1), the depletion region at drain side for condition (1) is expected to be larger than for condition (2) ($\Delta L_1 > \Delta L_2$) as shown in Figure 2.5 (a) and (b). It should be noted that due to the unique bottom-gate fork TFT structure, the formed channel is expected to extend even below the source electrode as shown in Figure 2.5.
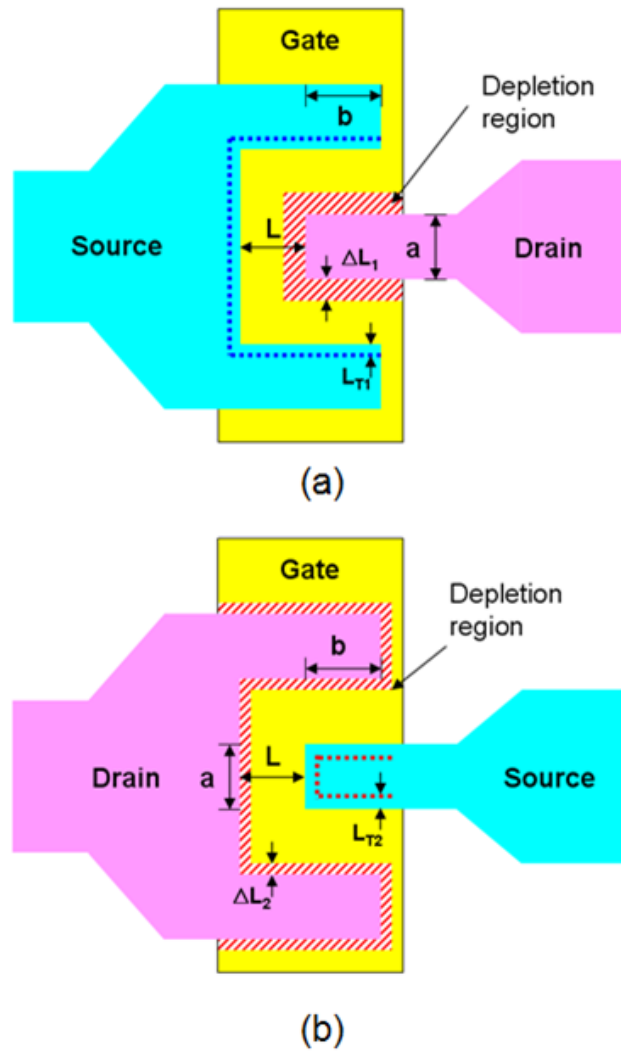
Figure 2.5 The schematic top views of depletion regions in fork a-Si:H TFT; case (1) where source is applied on U-shaped electrode and case (2) where source is applied on rod-shaped electrode.

However, it is well known that in a-Si:H TFT, the drain current does not flow through the whole source electrode length but is rather limited to a specific length, so-called TFT characteristic length (L_T) [10] near the electrode edge. Therefore, the characteristic length for each drain bias condition can be defined as L_{T1} and L_{T2}, respectively. To estimate L_{T1} and L_{T2}, we measured the channel resistance (r_{ch}) and source/drain contact resistance ($R_{S/D}$) for four fork TFTs with different channel lengths for each drain bias condition. From the measurements, TFT characteristic length ($=R_{S/D}/r_{ch}$) was calculated as 1.5 μm ($=L_{T2}$) and 1.0 μm ($=L_{T1}$) at V_{GS}=15V, respectively. From the experimental results, we can speculate that L_{T2} is larger than L_{T1} because the size of the electrode acting as an electron source is smaller for drain bias condition (2) than for drain bias condition (1).

Based on these assumptions, to derive the equation for the drain current in the saturation regime, the same methodology was applied here as one used for derivation of eq. (2.1); the integration of eq. (2.2) from ΔL_1 to $L+L_{T1}$ for drain bias condition (1) and from $-L_{T2}$ to $L-\Delta L_2$ for drain bias condition (2) yields the potential drop between the source and drain electrodes for each case, respectively. At the same time, the effective channel width also changes due to different depletion regions for different bias conditions. It should be noted that electrons are assumed to move along the shortest path, the channel length (L) only, not at the corner of U-shape electrode for both bias condition (1) and (2).

$$\int_{o}^{V_{DS}} [(V_{GS}-V_{TH})-V_y]dV_y = \frac{I_{DS}}{W_{eff1}\mu_{FE}C_{OX}} \int_{\Delta L_1}^{L+L_{T1}} dy, \tag{2.6a}$$

where $W_{eff1} = a + 2\Delta L_1 + 2(b+\Delta L_1)$.

$$\int_{o}^{V_{DS}} [(V_{GS}-V_{TH})-V_y]dV_y = \frac{I_{DS}}{W_{eff2}\mu_{FE}C_{OX}} \int_{-L_{T2}}^{L-\Delta L_2} dy, \tag{2.6b}$$

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$$\text{where } W_{eff2} = a + 2(b + \Delta L_2).$$

To find the values for ΔL_1 and ΔL_2 and corresponding equations for the asymmetric drain current, we do the asymmetric current calculation of fork a-Si:H TFT based on the standard TFT with the same length as reference width (W) = 20 μm and length (L) = 6 μm. Output drain current of conventional standard TFT was measured at V_{GS}=20V, and then normalized with its width over length ratio (W/2L), to be used as a reference value for the current calculation. Since both fork and standard a-Si:H TFT have been fabricated over the same substrate at the same time, we expect that their normalized electrical properties are equivalent and only geometries are different. Using normalized output drain current of standard TFT, we calculated the output drain current of fork TFT for each bias condition, by multiplying the normalized standard TFT characteristic by geometric factors defined in eq. (2.7) (output current of fork TFT= normalized output current of standard TFT × geometrical factor). By fitting several different values of ΔL_1 and ΔL_2 onto integrations above, we could find proper values for the channel length modulation factors empirically as $\Delta L_1 = L/4$ for condition (1) and $\Delta L_2 = L/10$ for condition (2), respectively. Hence, since $V_{DS} = (V_{GS}-V_{TH})$ in the saturation regime, the drain current for each condition can be expressed with corresponding geometrical factor f_{g1} and f_{g2}.

$$I_{DS}^{Condition\ (1)} = f_{g1}\mu_{FE}C_{OX}(V_{GS} - V_{TH})^2, \text{ where } f_{g1} = \frac{a + 2\Delta L_1 + 2(b + \Delta L_1)}{L + L_{T1} - \Delta L_1} \qquad (2.7a)$$

$$I_{DS}^{Condition\ (2)} = f_{g2}\mu_{FE}C_{OX}(V_{GS} - V_{TH})^2, \text{ where } f_{g2} = \frac{a + 2(b + \Delta L_2)}{L + L_{T2} - \Delta L_2} \qquad (2.7b)$$

As shown in eq. (2.7), in the saturation regime, values of geometrical factor can have direct impact on drain current values. When a and b in eq. (2.7) are replaced with the actual measured values (a=6 μm and b=10 μm), the geometrical factor in condition (1) turns out to be larger than

in condition (2) by about 1.5 times. Therefore, the ON-current for drain bias condition (1) is expected to be larger than for drain bias condition (2) by the difference in the geometrical factors.
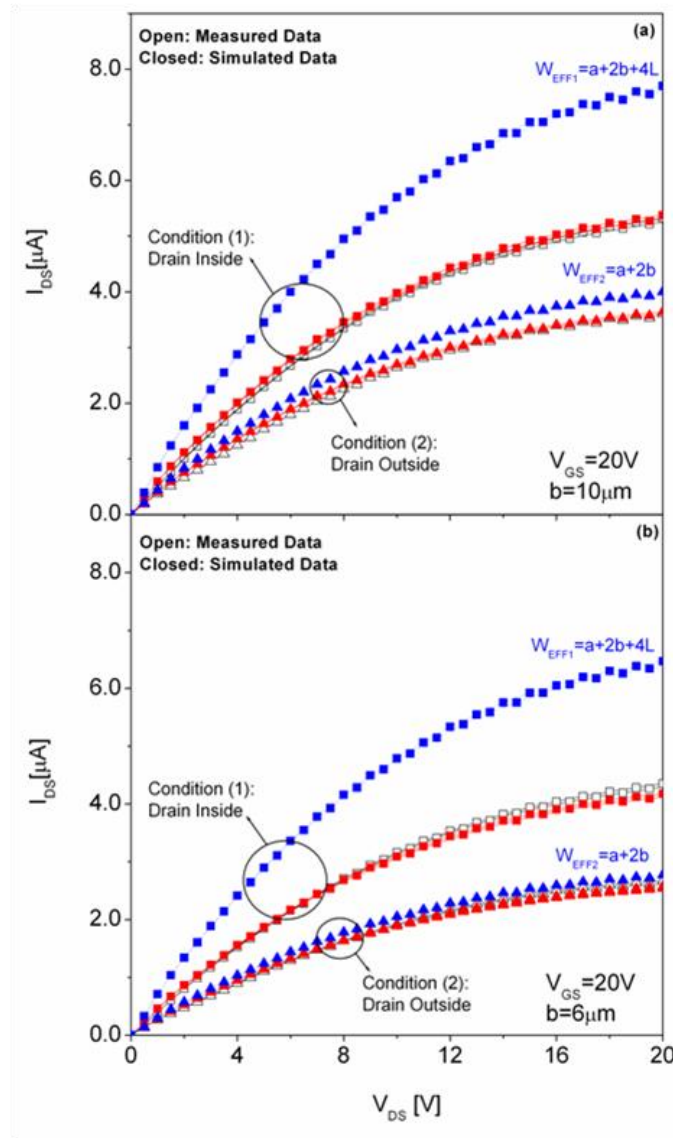
Figure 2.6 Measured (open symbol) and calculated (closed symbol) output characteristics of fork a-Si:H TFTs. (a) a = 6 µm and b =10 µm. (b) a = 6 µm and b = 6 µm.

As shown in the Figure 2.6, we could exactly match the measured output drain current of Fork TFT for each drain bias condition. It should be noted that when the intuitive channel width (W_{EFF1}= a + 2b + 4L for condition (1) and W_{EFF2}= a + 2b for condition (2)) is used as the circumference of source electrode instead of the geometrical factors given by eq. (2.7), the calculated drain current values are much larger than experimental values, Figure 2.6 (a). To validate these equations of geometrical factor, we measured another set of Fork TFT with different dimensions; a = 6μm and b = 6μm for smaller fork TFT. Again, the standard TFT is normalized by W/2L to be used as a reference for the calculated drain current. As shown in Figure 2.6 (b), though there is a little deviation observed for drain bias condition (1), the measured output drain current of fork TFT could only be exactly matched when the normalized drain current of standard TFT is multiplied for each bias condition by the defined geometrical factor as defined in eq. (2.7). Again, when the intuitive channel width (W_{EFF1}= a + 2b + 4L for condition (1) and W_{EFF2}= a + 2b for condition (2)) is used instead of the geometrical factor, the calculated output drain current of fork TFT shows huge difference from the measured values especially for bias condition (1).

The OFF-current in a-Si:H TFT is originated from carriers generated in the depletion region on drain side (at high V_{DS}) when negative gate bias is applied. Under V_{GS}<0, the a-Si:H is fully depleted and hole accumulation will take place near the a-Si:H / a-SiN$_X$:H interface creating a hole current. The current level is limited by the n[+]-a-Si:H source/drain contact regions (these are hole blocking contacts). If we assume that two quasi n[+]-p junctions are formed between the drain and source n[+]-regions and hole (p) conduction channel, the drain n[+]-p junction is under reverse bias (V_{DS}>0), which is similar to a n[+]-p junction in the OFF-state. Indeed, in a regular n[+]-p junction, the OFF-current is carried by minority carrier generated in depletion region. The OFF-current (J_g) in this region can be limited by the generation rate of carriers and the depletion width x_i as shown in following equation:

$$J_g = \frac{q n_i x_i}{2\tau_o},$$ (2.8)

where q is electron charge, n_i is the maximum generation rate, and τ_0 is the life time of excess carrier in the depletion region. If we assume that the width of the depletion region and the generation rate are identical for both drain bias conditions at high V_{DS}, the OFF-current can depend only on the volume of the depletion region (= the area of drain electrode × the depletion width, x_i) for each bias condition. Therefore, since the area of drain electrode is larger in drain bias condition (2) and in drain bias condition (1), the OFF-current of condition (2) is expected to be higher than for condition (1). For image sensor application, drain bias condition (1) is more promising because the OFF-current limits the lowest detectable signal level of image sensor. So the lower OFF-current is, the better.

2.3.3 Fork TFT parameters extraction

From TFT data shown in Figures 2.3, 2.4, and 2.7, we can extract sub-threshold slope (S), threshold voltage, and field-effect mobility values. We chose the center position (at $I_{DS} = 10^{-10}$A) in the transfer curve of log (I_{DS}) vs. V_{GS}, and use the linear fitting by taking two log (I_D) values around the center point to extract S-value. Field-effect mobility (μ_{FE}) and threshold voltage can be calculated as follow: from the transfer curve of I_D vs. V_{GS}, we chose a specific value of I_D at V_{GS}=15V. By taking 10 and 90% of this selected I_D value, we define the fitting range in I_D vs. V_{GS} experimental characteristics. From the slope and x-axis intercept of the calculated curve, the field-effect mobility and threshold voltage have been extracted using eq. (2.3) and (2.7) with different geometrical factors. Calculated device parameters are summarized in Table 1 for linear (low V_{DS}) and saturation (high V_{DS}) region, respectively.
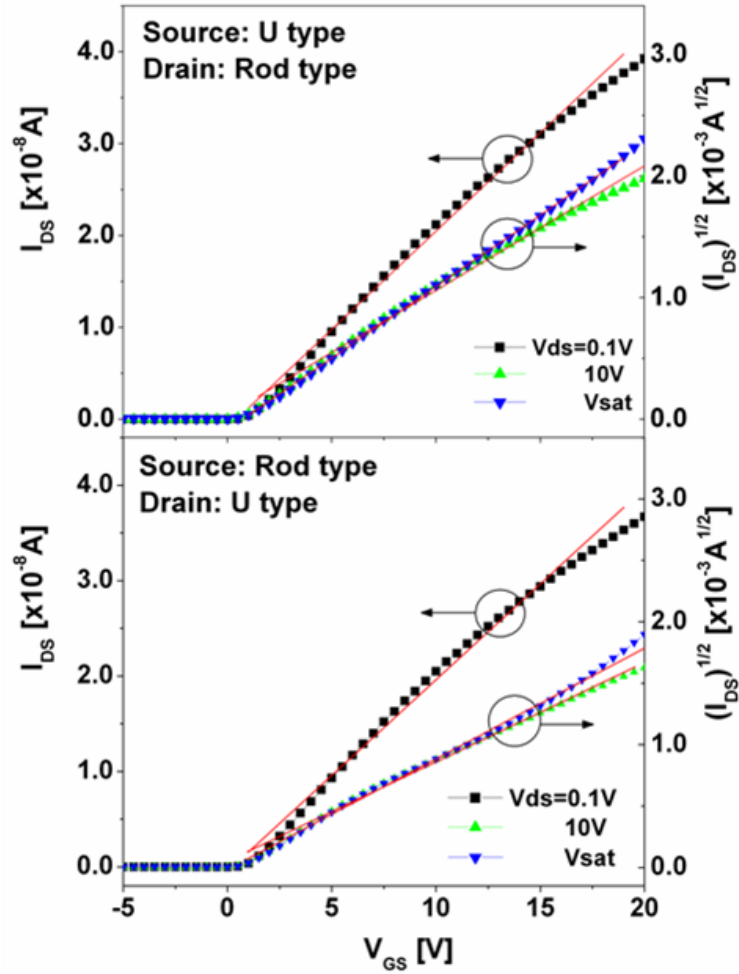
Figure 2.7 Transfer characteristics of fork a-Si:H TFT. Solid lines used for extraction of the threshold voltage and mobility are also shown (10-90% method used).

For the comparison, we also calculated field-effect mobility (μ_{FE}) and threshold voltage by using the maximum slope method which is usually used for crystalline silicon devices. The field-effect mobility is calculated from transconductance maximum (g_m) value using following equations:

$$\mu_{Linear} = \frac{L \cdot g_{m-Linear}}{W_{eff0} C_{OX} V_{DS}}, \tag{2.9a}$$

$$\mu_{Saturation} = \frac{g_{m-Saturation}^2}{f_{g1,2} C_{OX}}, \tag{2.9b}$$

where $g_{m-linear}$ is the maximum transconductace at $V_{DS}=0.1V$, and $g_{m-saturation}$ is the maximum transconductance at $V_{DS}=V_{SAT}$. From the V_{GS} value of the maximum g_m as a reference, two closest points are chosen for straight line fitting through the three points on the transfer curve of I_D-V_{GS}. The threshold voltage can be estimated from x-axis intercept of this extrapolated line for each drain bias condition. Resulting extracted parameters are summarized in Table 2.1. It is clear from this table that those two calculation methods provide very similar mobility and threshold voltage values for fork a-Si:H TFTs (within experimental error).

TFT Parameter	$V_{DS}=0.1V$		$V_{DS}=V_{sat}$	
Case	(1)	(2)	(1)	(2)
S [mV/Dec]	386	375	485	494
V_{th} [V]	0.73	0.66	0.61	0.84
I_{OFF} at V_{GS} = -5V [A]	1.00×10^{-13}	3.00×10^{-13}	3.59×10^{-11}	3.77×10^{-11}
μ_{FE} [cm^2/V·s]	0.32[a]	0.34[a]	0.35[b]	0.39[c]

Table 2.1 Extracted parameters of fork TFT; case (1) where source is applied on U-shaped electrode and case (2) where source is applied on rod-shaped electrode. Geometrical factor a) W_{eff0}/L b) f_{g1} and c) f_{g2} is used to extract the parameter

2.3.4 Electrical instability of fork a-Si:H TFT

The electrical instability of fork TFT as a switch in sensor application is important in that it affects ON-state resistance (R_{ON}), charge transfer time and eventually degrades the switching capability. To evaluate electrical instability of fork TFT, a series of current temperature stress (CTS) measurements of fork TFTs were performed by using a semiconductor parameter analyzer (HP 4156A) under an accelerated stress condition by setting the stress temperature (T_{STR}) at 80 ℃. During the CTS measurements, we connected the gate and drain bias together and continuously applied the current through the drain to the TFTs. Source of the TFT was grounded. So the TFTs operated in the saturation regime. We applied various drain current values: I_{STR} of 1, 2, and 4 µA corresponds to J_{STR} of 263, 527, and 1053 A/cm², respectively. The total stress time (t_{STR}) was 10,000 sec, and we only interrupted the applied stress for 60 sec to measure the transfer characteristics. We measured and collected results for both case (1) and (2).

Figure 2.8 shows the asymmetric threshold voltage shift (ΔV_{th}) of fork TFT depending on source-drain bias connection under CTS measurement. ΔV_{th} of case (1) is less than that of case (2). Although at low current stress ($I_{STR} = 1$ µA) their discrepancy is about 0.03 V, it increases to 0.14 V at $I_{STR} = 4$ µA. The results imply that the discrepancy will become larger for higher stress current density and larger asymmetricity of source-drain electrode. When the fork TFT is used as a switch, source and drain bias connection may depend on its application and design. So understanding of this asymmetric electrical instability will be helpful: case (1) where source is applied on U-shaped electrode is preferred for less threshold voltage shift. Asymmetric biasing of the fork TFT can change the ON-current characteristics while other TFT parameters such as OFF-current, field-effect mobility and threshold voltage remain the same regardless of bias conditions as shown in the Table 2.1. Along with larger pixel aperture ratio compared to normal TFT, these unperturbed characteristics can be very advantageous when device is used as a switching device in passive pixel sensor application.
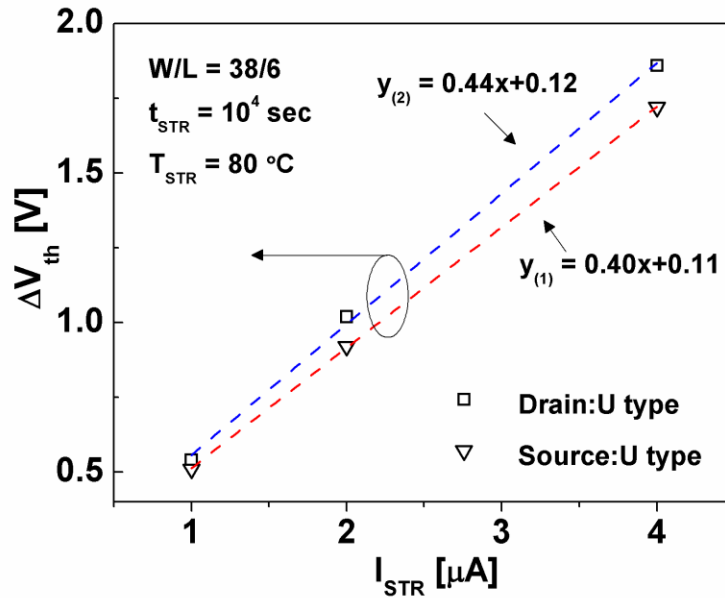
Figure 2.8 Source-drain bias connection dependence of threshold voltage shift (ΔV_{th}) of fork TFT for various stress current densities; (dash-line) linear fitting results.

2.4 Electrical Instability of Hexagonal a-Si:H TFT

2.4.1 Experiments

The electrical properties of hexagonal (HEX) a-Si:H TFT were described previously [7]. In this section, a series of current temperature stress (CTS) measurements of the single and multiple HEX-TFTs were performed by using a semiconductor parameter analyzer (HP 4156A) under an accelerated stress condition by setting the stress temperature (T_{STR}) at 80 ℃. During the CTS measurements, we connected the gate and drain bias (inner-electrode) together and continuously applied the current through the drain to the TFTs. Source (outer-electrode) of the TFT was grounded. So the TFTs operate in the saturation regime. We applied different drain current values

depending on the channel width to maintain the same stress current density (J_{STR} = 1667 A/cm^2). For example, drain currents of 50, 100 and 167 µA were applied to HEX-1 (*W/L* = 300/5), HEX-2 (*W/L* = 600/5) and standard (*W/L* = 1000/6) a-Si:H TFTs, respectively. The total stress time (t_{STR}) was 10,000 sec, and we only interrupted the applied stress for 60 sec to measure the transfer characteristics. Using the same condition, we also measured independently all HEX-TFT basic
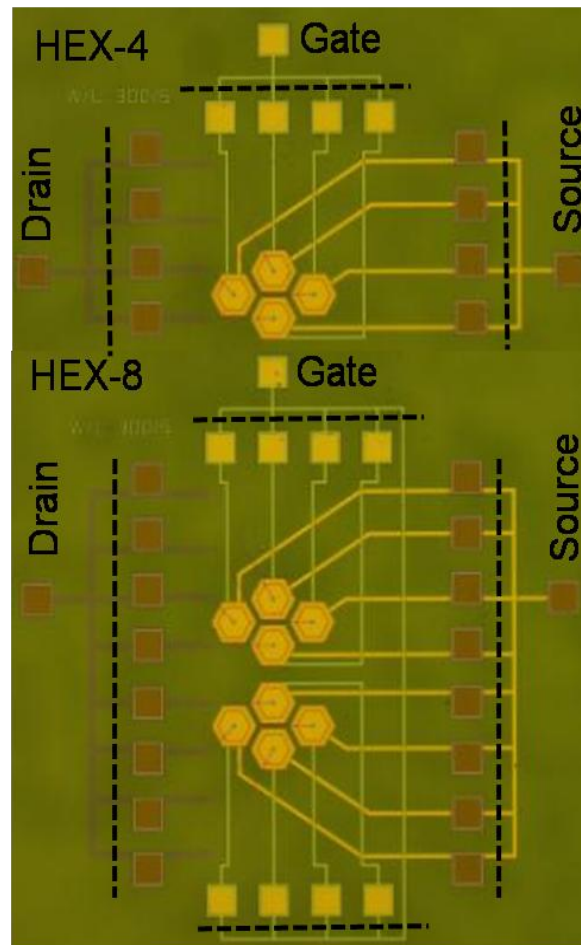
Figure 2.9 The photographs of multiple HEX-TFTs (e.g. HEX-4 and HEX-8 TFTs). Dashed lines show the cutting lines to separate and measure individual HEX-TFT unit.

units by cutting the parallel connection lines (Figure 2.9). A standard TFT ($W/L = 1000/6$) was measured as well for comparison. We performed thermal annealing at 200 °C for 2 hour to ensure the consistent initial properties of the a-Si:H TFTs before each CTS measurement. Figure 2.10 represents that the CTS induced stress could be fully recovered after each thermal annealing. Using the effective channel width calculated by *H.Lee et al.* [7], we extracted the threshold voltages using the maximum slope method over the stress time. The threshold voltage shift (ΔV_{th}) is defined as follows

$$\Delta V_{th}(t) = V_{th}\ (t = t_{STR}) - V_{th}(t = 0). \tag{2.10}$$
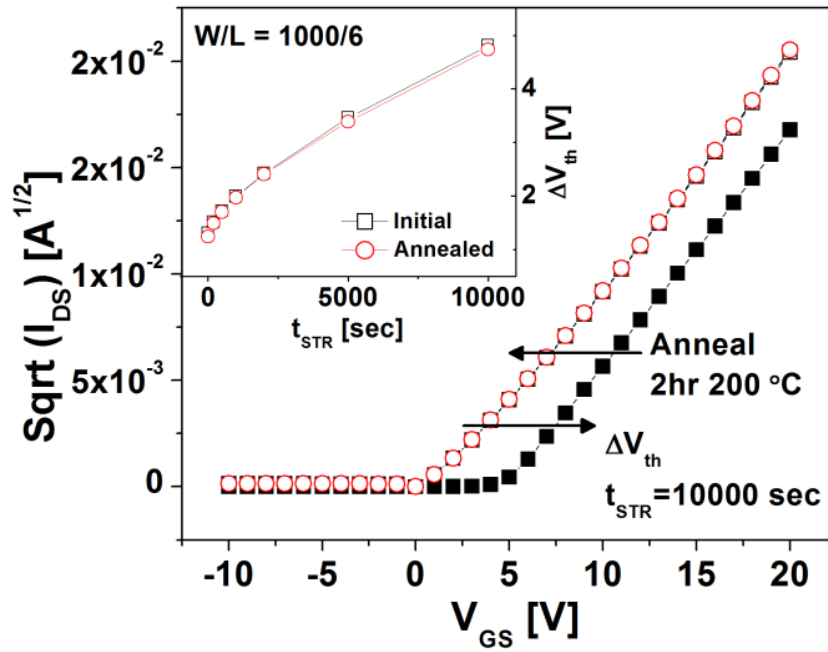
Figure 2.10 The recovery of the CTS-induced stress after thermal annealing. The transfer characteristics are restored to the initial state after the annealing. The inset shows the threshold voltage shift as a function of stress time. Squares and circles represent the CTS results of the initial and annealed TFTs, respectively.

2.4.2 Experimental results and discussion

Figure 2.11 shows the ΔV_{th} variation as a function of stress time (t_{STR}) for different TFTs studied in this work. The ΔV_{th} of HEX-2 ($W/L = 600/5$), HEX-4 ($W/L = 1200/5$) and HEX-8 ($W/L = 2400/5$) are 3.26 V, 3.56 V and 3.82 V, respectively. ΔV_{th} increases with W/L ratio: larger width results in larger ΔV_{th} for a given channel length (L = 5 µm). Because HEX-4 with even higher W/L ratio exhibited similar ΔV_{th} to standard TFT (W/L= 1000/6, ΔV_{th} = 3.55 V), parallel-connected multiple HEX-TFTs appear to have a better electrical stability (less ΔV_{th}) for the same W/L ratio in comparison to a standard TFT. Field-effect mobility (μ_{eff}) was also extracted from the transfer characteristics. The amount of μ_{eff} change ($\Delta\mu_{eff}$) after the CTS measurement for the standard TFT, HEX-2, HEX-4 and HEX-8 are 0.06, 0.07, 0.09 and 0.12 cm^2/(V·s), respectively.
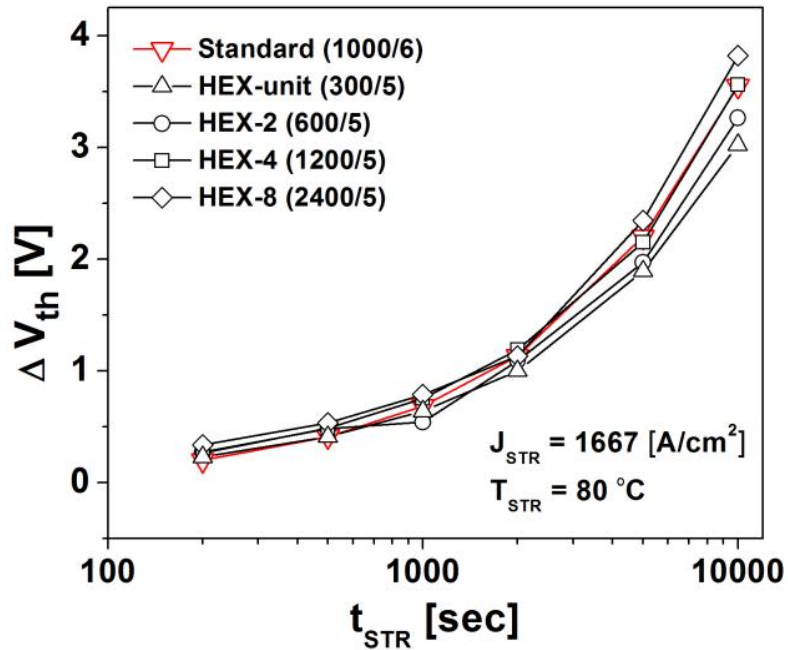
Figure 2.11 Threshold voltage shifts of the single HEXT-TFT, HEX-2, HEX-4, and HEX-8 as a function of stress time in a semi-log scale. The result of standard TFT is shown for comparison.

The influence of the ΔV_{th} of a single HEX-TFT on ΔV_{th} of multiple HEX-TFTs was also investigated. The ΔV_{th} of all single HEX-TFTs for both HEX-4 and HEX-8 is 3.04 V ± 0.06. No specific single HEX-TFT dominates the overall circuit electrical instability due to adequate a-Si:H TFT process spatial uniformity.

We also estimated ΔV_{th} of parallel-connected multiple HEX-TFTs based on their unit device. ΔV_{th} of HEX-2^N TFT (*N*, integer) can be described by $\Delta V_{th\_N} = \Delta V_{th\_u} + N \times 0.27$, where ΔV_{th_u} is ΔV_{th} of unit HEX-TFT and N is from HEX-2^N TFT (Figure 2.12). The linear relation between ΔV_{th} and number of unit TFTs can be explained as follows: for this specific experimental bias condition, ΔV_{th} is dominated by a combination of defect creation or/and charge trapping; indeed Figure 2.11 shows power-law dependence between ΔV_{th} and the stress time (t_{STR}) as disclosed in previous works by other groups [8, 11]. We observed $\Delta V_{th} \propto t_{STR}{}^{\beta}$, and β is extracted to be 0.65 ± 0.02. For a-Si;H TFT, the total channel charge (Q_{ch}) in the saturation region is given by

$$Q_{ch} = \frac{2}{3} C_G \cdot W \cdot L \left(V_{GS} - V_{th} \right), \tag{2.11}$$

where C_G is the gate capacitance per unit area, *W* the channel width, *L* the channel length, V_{GS} the gate-source bias [12]. The channel width increases with the number of parallel-connected HEX TFTs, and so does the total channel charge. For larger Q_{ch} we expect that a larger number of carriers are available for either to be trapped at the silicon nitride/a-Si:H interface or/and to participate in breaking of Si-Si weak bonds to create charged Si defects. Both mechanisms will produce ΔV_{th} that is proportional to number of trapped charges. In other words, a larger number of trapped charges will result in a larger threshold voltage shift in agreement with the experiments.
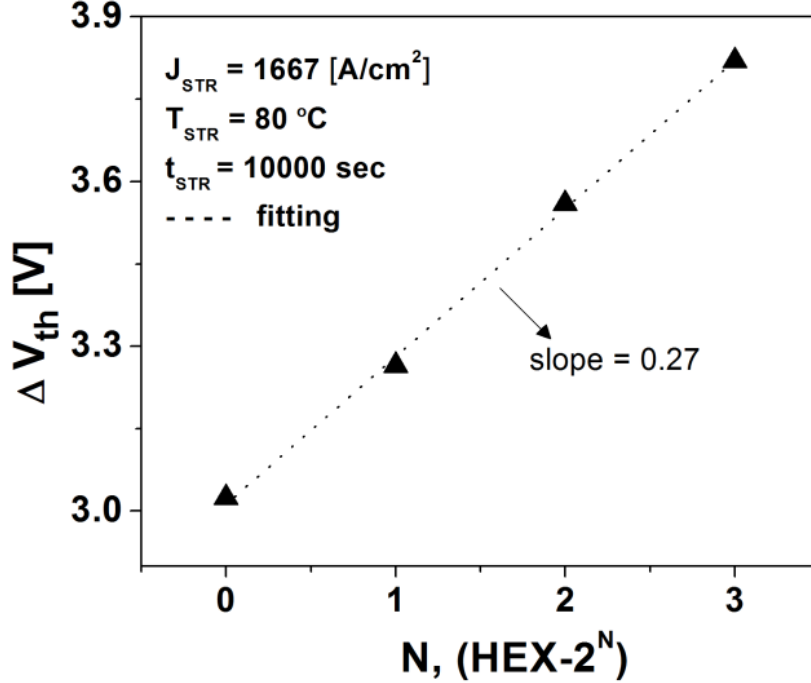
Figure 2.12 CTS-induced threshold voltage shift as a function of integer N of HEX-2^N.

2.5   Conclusion

We studied the asymmetric electrical characteristics of fork a-Si:H TFTs under different drain bias connections. Due to the unique fork device geometry, when source is connected to outer U-shaped electrode, ON-current is 1.5 times higher than when source is applied to inner rod-shaped electrode at high drain voltages (>10 V) while OFF-current remains the same for both cases. Asymmetric electrical instability of fork TFT under the current-temperature-stress is also attributed to this unique fork-shape. We studied in depth the electrical stability of single and multiple HEX-TFTs under the current-temperature-stress as well. The multiple HEX-TFTs show a better electrical stability compared to the standard TFT for a similar *W/L* ratio. It is also found that one specific HEX unit in the multiple HEX-TFT does not dominate or/and affect the

electrical instability of the overall TFT. Furthermore, we established the relationship between the threshold voltage shift and number of units in the multiple HEX-TFT. The improved electrical stability (i.e. less threshold voltage shift, ΔV_{th}) of fork and HEX-TFTs is promising characteristics since ΔV_{th} degrades the switching capability. Both fork and HEX-TFT occupy less pixel area so they provide a larger pixel aperture ratio for given channel width. The demonstrated electrical properties and instability shows that fork and HEX-TFT structures can be a good candidate as a switching TFT for high-resolution passive pixel sensor application.

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Chapter 3

Maskless Laser-Write Lithography

3.1 Introduction

Maskless lithography technology, which was introduced in 1989 for photo-mask making and structuring of specific materials [1], has drawn increasing attention in recent years for patterning fine features over a large area. It provides advantages such as fast turn-around time, no cost associated with mask-making process, flexibility in lithographic process, and capability for a large area exposure [2-4]. When a low-volume and a fast run are necessary, mask-based lithographic process is not a best option. In flat panel display and solar-cell panel processing, as substrate sizes increase, the cost of mask fabrication rapidly increases with its size. To reduce the fabrication cost of photo-masks, a laser direct patterning technology of thin-film has been investigated [4, 5]. It was recently reported that the laser direct patterning of ITO thin-film can compete with the typical photolithography process [6]. At the same time, there have been increasing efforts to develop optical maskless lithography technology for CMOS industry. As the chip design becomes more complex with a smaller critical dimension, the cost and time of mask-making increases tremendously [7].

In this chapter, we describe the feasibility of using the maskless laser-write lithography (LWL) system of Heidelberg Instruments (DWL 4000) together with the level-to-level alignment capability in the fabrication of the a-Si:H TFTs on a planar surface. The maskless laser-write lithography (LWL) system has been a workhorse for mask-making process in large area

applications. Also electrical performances of fabricated a-Si:H TFTs are discussed. Lastly, the extensively modified LWL system is described and evaluated in details, which will be used for the fabrication of the a-Si:H TFT and circuits on a non-planar surface.

3.2   Maskless a-Si:H TFT Processing using a Standard LWL on a Flat Surface

3.2.1   Fabrication of a-Si:H TFTs

The LWL system (DWL 4000) shown in Figure 3.1 is capable of creating two and three dimensional structures on up to 400 mm x 400 mm substrate using the binary and gray-scale exposure, respectively [8]. In binary exposure, intensity of light source is selected so that the resist is exposed completely or unexposed. The exposed areas are gone after resist development. Gray scale exposure is performed by directly modulating the intensity to expose partially

Figure 3.1 Whole view of DWL 4000 System used in this work

the resist with variable doses. Figure 3.2 illustrate write-strategy of the system; the acousto-optic modulator (AOM) modulates the laser beam intensity, and the acousto-optic deflector (AOD) deflects the laser beam and performs a scan. The substrate stage holds a substrate and moves it in x-y plane, which is monitored by an interferometer system with a resolution of 10 nm. During the exposure, it is critical for a good and constant structure quality that the system keeps the beam focused since the depth of focus is low and little variation can lead to non-uniform exposure. The auto-focusing is done by an air-gauge. Stripes are exposed by laser scanning with programmed width, and the entire area is exposed by stitching multiple exposed stripes. Modified optical set-ups can provide various write-modes with different writing speeds and resolutions as shown in Table 3.1 [8].
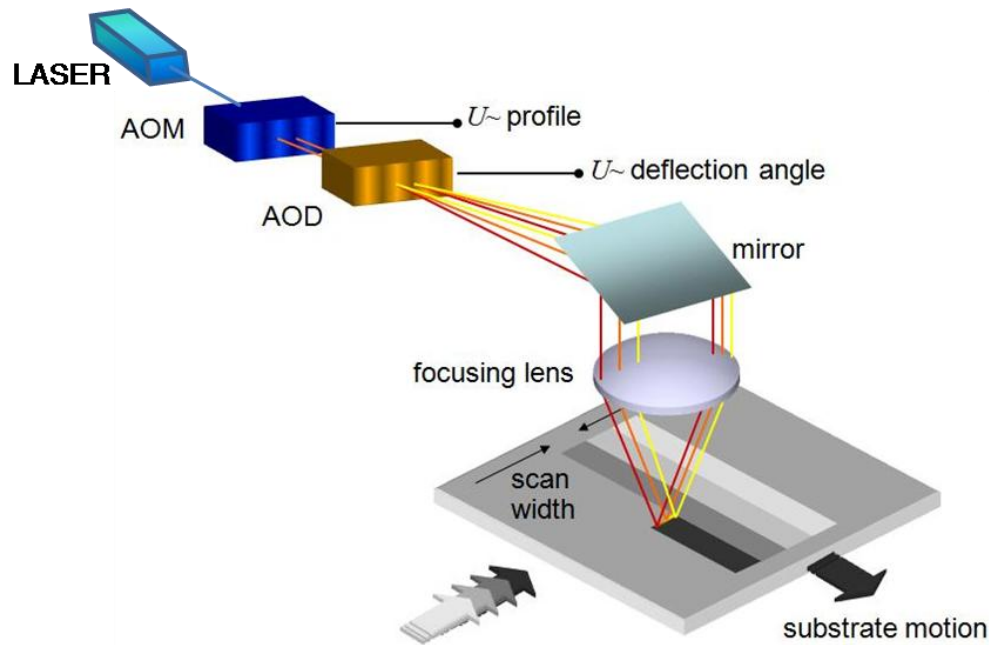
Figure 3.2 The illustration of the optical design and writing strategy. The substrate moves in the x-y plane during the exposure (Adopt from [8]).

Write Mode	I	II	III	IV
Address Grid [nm]	10	20	25	50
Minimum Feature Size [µm]	0.6	0.7	0.8	1.6
Write Speed [mm^2/min]	26	101	155	560
Exposure Time [min/4″wafer]	300	75	50	15
Edge Roughness [3σ, nm]	60	80	100	120

Table 3.1 The specification of the LWL system for different write modes.

The performance specifications of the adopted write-mode (II) was used for the present study: the minimum feature size of 0.7 µm can be achieved with an address grid of 20 nm. The focal length of the write lens is 4 mm and the writing speed is 101 mm^2/min. The alignment accuracy is 0.25 µm. Helium-Cadmium (He-Cd) laser with a wavelength of 442 nm was used as a laser source. The LWL system was used to expose all device layers before each development and following etching processing step. The photoresist (S1805) is spin-coated at 2000 rpm and soft-baking is performed over a hotplate at 100 ℃ for 1 min. Then LWL exposure is conducted, which is followed by development process in AZ 726 MIF developer and hard-baking on a hotplate at 110 ℃ for 5 min.

In this work, we fabricated inverted-staggered a-Si:H TFTs using four masks process step. Figure 3.3 (a) shows the fabricated a-Si:H TFT. First, Cr of 200 nm was deposited by a sputtering method and then the Cr gate electrode was patterned by wet-etching using CR-14 etchant (layer #1). Next, PECVD was used to deposit a tri-layer of gate silicon nitride (a-SiN$_X$:H, 400 nm) forming a gate insulator together with amorphous silicon (a-Si:H, 170 nm) and phosphorous-doped (n+) a-Si:H (70 nm) forming an active channel layer. The active island was
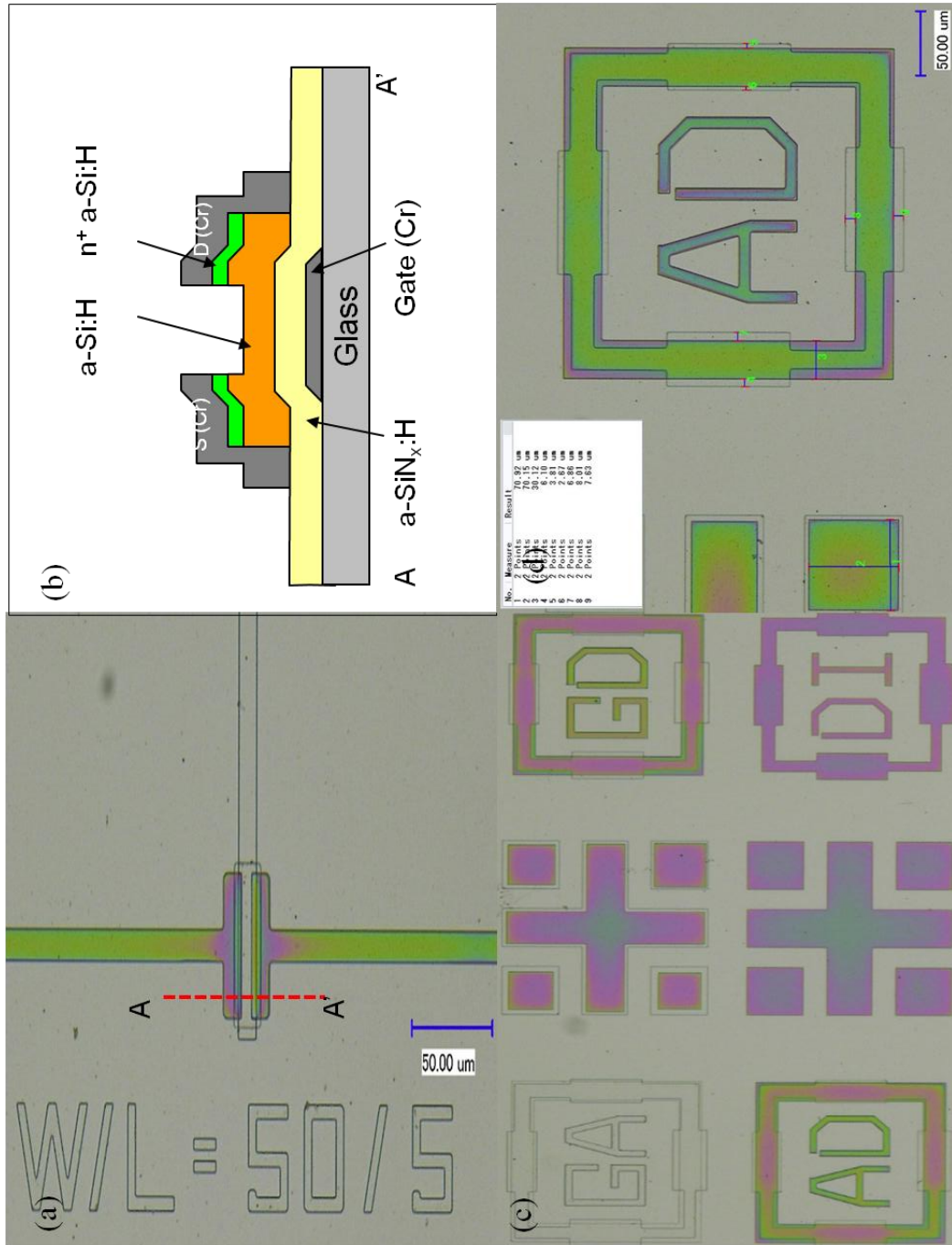
Figure 3.3 (a) Optical microscope images of fabricated a-Si:H TFT (*W/L* = 50/5) using LWL (b) A schematic of cross section view (c) Alignment marks (resist not removed for a clear picture) (d) Example of alignment mark used for calculation of alignment error.

defined by RIE dry-etching of the a-Si:H and n+a-Si:H using a gas mixture of SF_6 and O_2 (layer #2). We subsequently defined contact via to the gate electrode using buffered hydrofluoric acid (BHF) (layer #3). Following a deposition of a source/drain (S/D) metal Cr layer (200 nm) by a sputtering method, wet-etching using CR-14 etchant was done to form S/D contacts (layer #4). Then to remove the n+ a-Si:H layer from the channel region, back-channel etching is performed by RIE dry-etching with a gas mixture of SF_6 and O_2 using the S/D metal and a photoresist as a mask. As a final step, thermal annealing was performed at 200 ℃ for two hours to improve electrical properties of each film layer.

Level-to-level alignment with high accuracy is the central critical issue for fabricating fully functional devices and circuits. It was performed here in the following manner: the optical and metrology system in the LWL are equipped with two camera systems. One camera with a large field of view is used to locate alignment marks and another camera with high resolution is intended for aligning these marks. Figure 3.3 (c) shows part of the alignment marks used in this experiment. The level-to-level alignment error is defined as the relative position deviation of the alignment marks within the two following layers. We derive vertical and horizontal deviation from the measurement of the distance of the borders on four sides in the bar alignment mark as shown in Figure 3.3 (d) for instance. The measured error was less than 1 µm for TFT with a 5 µm channel length and up to 300 µm channel width.

The evaluation of the LWL exposure accuracy was performed by measuring dimensions of various exposed and developed structures as shown Figure 3.4. We then compared the measured results with electronics design. The discrepancy between exposed structures and electronics design was less than about 5.79 %, which is acceptable for fabricating functional electronic devices; 5.67% for interdigitated TFT in Figure 3.4 (a), 3.45% for contact pad in Figure 3.4(b), and 7.46% for normal TFT in Figure 3.4 (c).

No.	Measure	Result
1	2 Points	10.80 um
2	2 Points	11.12 um
3	2 Points	51.47 um
4	2 Points	12.07 um

No.	Measure	Result
1	2 Points	291.66 um
2	2 Points	289.75 um

50.00 um

No.	Measure	Result
1	2 Points	5.72 um
2	2 Points	11.06 um
3	2 Points	49.57 um
4	2 Points	49.75 um
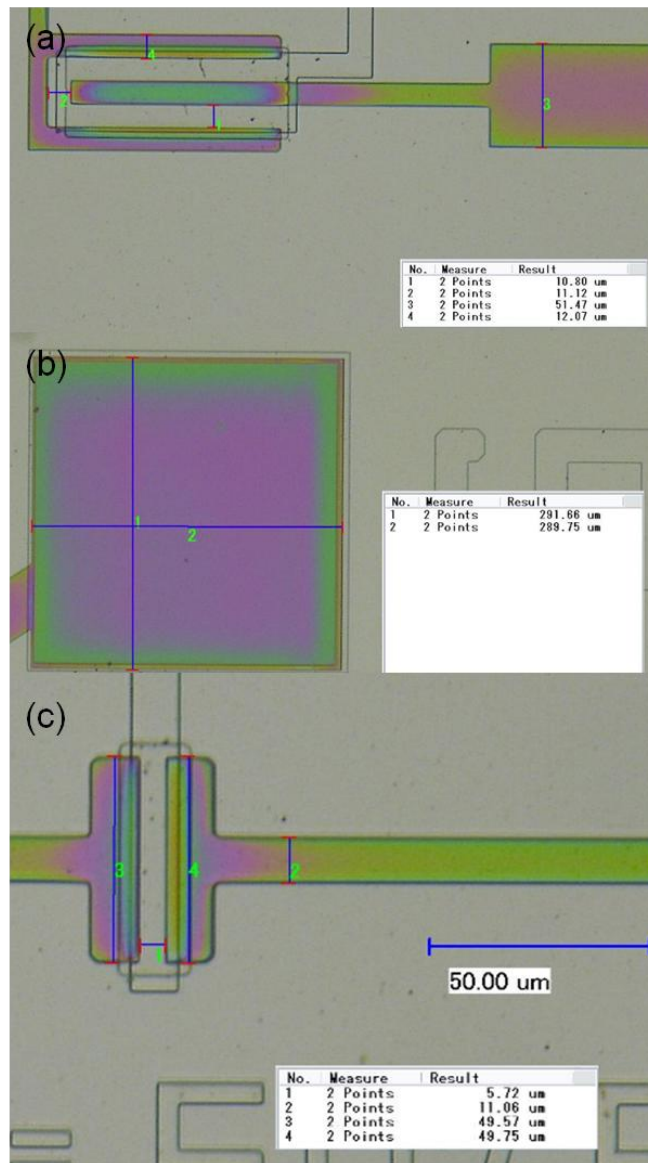
Figure 3.4 Examples of exposed structures using LWL after photoresist development: (a) interdigitated TFT (W/L =200/10), (b) contact pad, and (c) normal TFT (W/L =50/5).

3.2.2 Experimental results and discussions

Electrical measurements of the fabricated a-Si:H TFT (W/L = 50/5) were conducted and analyzed using a probe station in combination with HP 4156 at room temperature in a dark

condition. We first measured the output characteristics of the TFT for various gate voltages (V_{GS}) (Figure 3.5). Then the transfer characteristics for drain-to-source voltage (V_{DS}) of 0.1 V and 10 V were measured (Figure 3.6). We extracted the field-effect mobility (μ_{FE}) and threshold voltage (V_{th}) by using the maximum slope method [9]. The subthreshold swing (S) is defined as the steepest slope of the I_{DS}-V_{GS} plot in log scale, and extracted using the following equation:

$$S = \left(\frac{d\log(I_D)}{dV_{GS}} \right)^{-1} \tag{3.1}$$

Table 3.2 shows the summary of the extracted TFT parameters: In this process S is slightly larger in comparison to reported values for a-Si:H TFTs. The S is related to bulk and/or interface state density (N_{SS}) through the following equation [10]:

$$N_{ss} = \left(\frac{S\log(e)}{kT/q} - 1 \right)\frac{C_i}{q} \tag{3.2}$$

where q is the electron charge, k is the Boltzman constant, C_i is insulator capacitance per unit area, and T is the temperature. From this equation we calculated the value of N_{ss} (1.08 x 10^{12} for $V_{DS} = 0.1$V), which is slightly larger than value published for normal TFT [11].
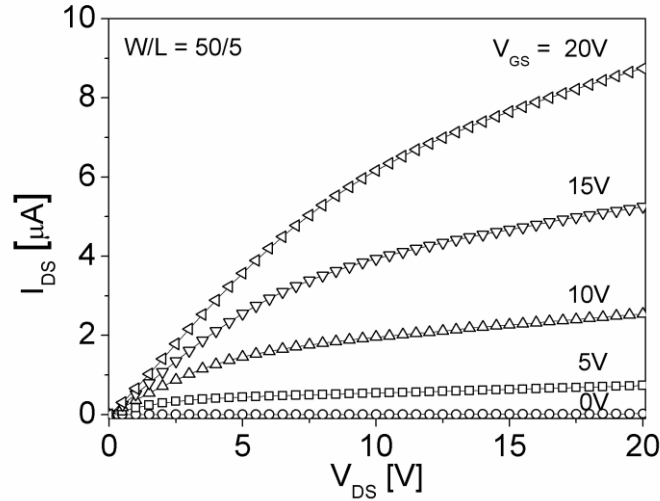
Figure 3.5 Output characteristics of fabricated a-Si:H TFT using LWL process ($W/L = 50/5$).
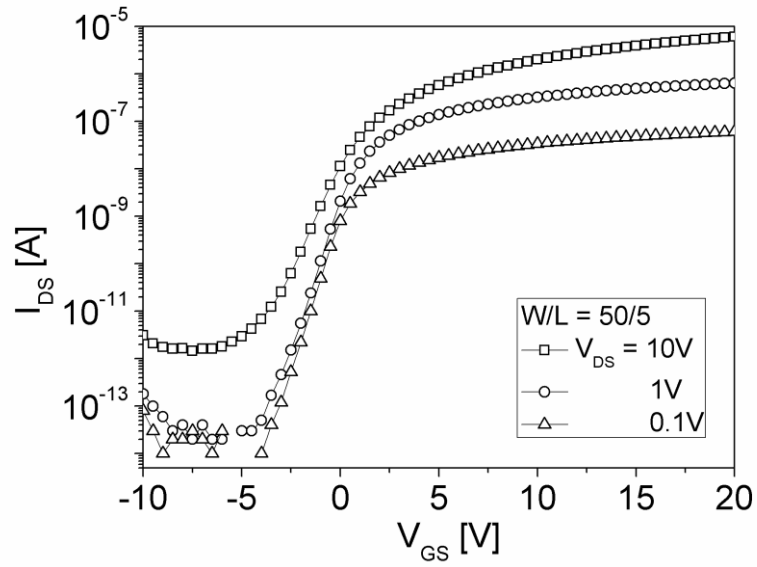
Figure 3.6 Transfer characteristics of fabricated a-Si:H TFT using LWL process in saturation regime. Inset shows the result in a log scale.

Parameters	$V_{DS} = 0.1$ V	$V_{DS} = 10$ V
V_{th} [V]	0.17	1.5
μ_{FE} [cm^2/V·s]	0.22	0.24
On/Off Current Ratio	1.6×10^6	2.7×10^6
I_{OFF} at $V_{GS} = -7.5$V [A]	3×10^{-14}	1.46×10^{-12}
S [V/dec]	0.76	1.07

Table 3.2 Summary of the extracted TFT (*W/L* = 50/5) parameters.
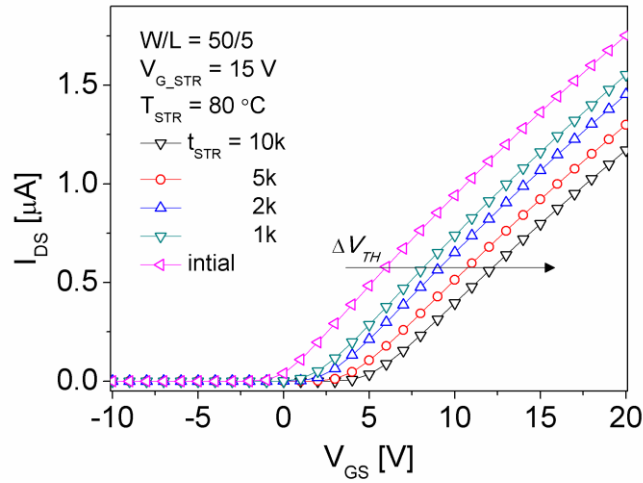
Figure 3.7 The change of the fabricated TFT transfer characteristics at $V_{DS} = 1$V for $t_{STR} = 10^4$ sec under BTS condition.

The low leakage current ($I_{OFF} < 1.5$ pA) for both low (0.1 V) and high drain bias (10 V), and large On/Off current ratio (~ 10^6) are desirable characteristics for a pixel switch in passive pixel sensor application.

To evaluate electrical instability of the fabricated TFT ($W/L = 50/5$) for a prolonged gate-bias condition, we conducted a bias-temperature stress (BTS) experiment. During the BTS, a constant gate stress voltage ($V_{G\_STR} = 15$ V) is applied, and the drain bias is grounded to source bias. We set the stress temperature (T_{STR}) and stress time (t_{STR}) as 80 ℃ and 10^4 sec, respectively. In Figure 3.7, all I_{DS} -V_{GS} characteristics were measured at $V_{DS} = 1$V by interrupting constant bias stress for 60 sec at predetermined time steps. The threshold voltage (V_{th}) and its shift ($\varDelta V_{th}$) over t_{STR} were extracted and calculated using the same method described in Chapter 2. The threshold voltage shift ($\varDelta V_{th}$) for the stress time and condition was about 5.18 V, which is comparable to $\varDelta V_{th} = $ 4.76 V of a-Si:H TFT ($W/L = 50/5$) fabricated by same process conditions (e.g. tri-layer deposition, dry-, and wet-etch) except conventional photolithography (MA-6).

3.2.3 Summary

In this experiment, a-Si:H TFTs with 5 µm channel length were fabricated using the maskless laser-write lithography (LWL) in combination with the well-established a-Si:H TFT processing technology. By using LWL, it is very easy to modify the device and circuit designs during process development since the lithography process is performed directly from an electronic design rather than from photo-masks. This fabrication method using the LWL can be an alternative to conventional photolithography for a rapid and a low-volume prototyping by reducing the turn-around time and cost of mask fabrication. The proposed fabrication technique can be extended from research to development and fabrication of large area electronics including flat panel displays, x-ray imager, and solar panels.

3.3 Modified LWL System for TFT Processing on a Non-Planar Surface

To perform LWL process on a non-planar surface, we need extensive modification of the standard system to meet special requirements. Figure 3.8 shows pictures of the modified system used in this work. Technical details regarding the modified LWL system have been published by our collaborator, *D. Radtke et. al* [12]. To accommodate non-planar substrate, we need following tool modifications: capability to tilt substrate table; optical and metrology system including optical autofocus system; special data preparation and exposure control. Finally we will describe modified LWL system for processing of curved substrate with enhanced field of view (*FOV*).
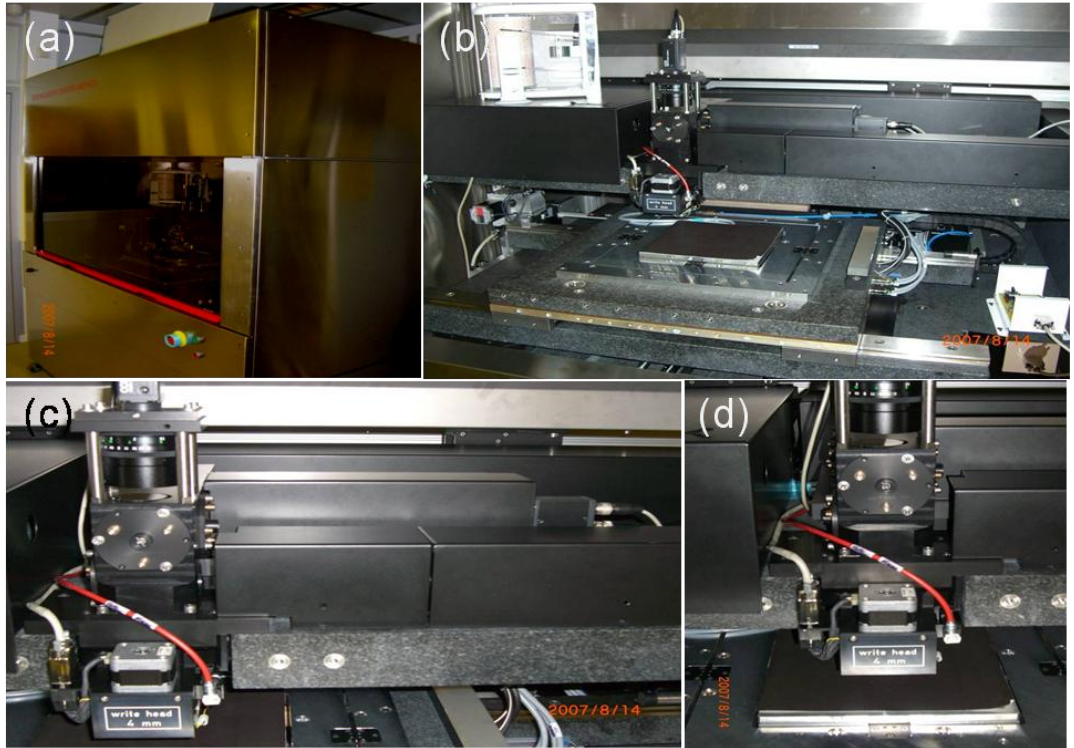
Figure 3.8 The modified Heidelberg laser write lithography system (a) general view of LWL system (b) main functional components (c) optics plate (d) write head & substrate table.
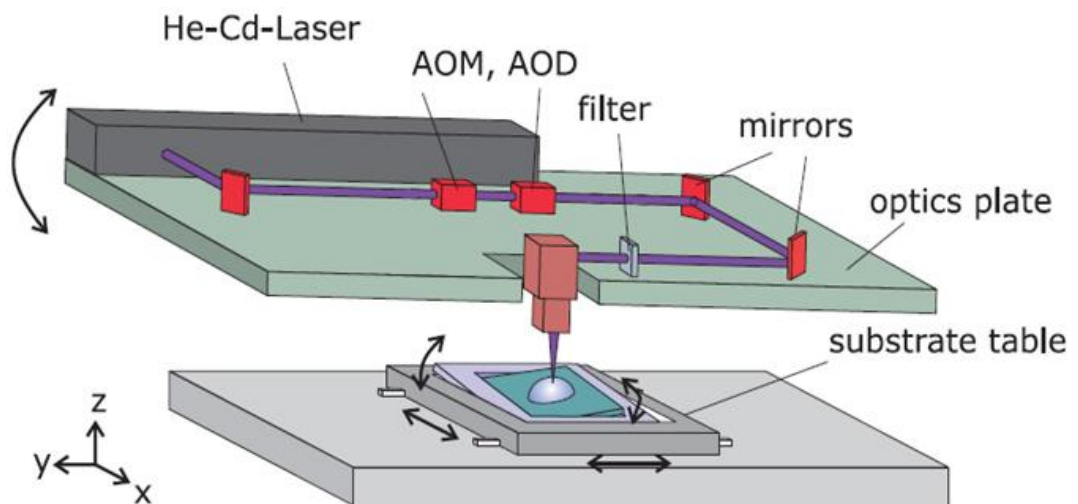
Figure 3.9 Illustration of a main function part of the modified LWL systems [10]

3.3.1 Laser source

Helium-Cadmium (He-Cd) laser with a wavelength of 442 nm is used as a laser source. A spot size of laser beam determining minimum feature size depends on writing lenses, and for the modified system ~ 1 μm minimum feature size can be achieved by using writing lens of 4 mm focal length.

3.3.2 Substrate table

The exact position of the incident writing beam on a non-planar surface is mandatory. This requires capability of tilting a substrate stage to make an exposed area to be always perpendicular to the writing beam as illustrated in Figure 3.9. In addition to x-y motion, the modified substrate stage can be tilted up to ± 10 ° along x and y direction, which is limiting field-of-view (*FOV*) of a curved substrate to 20 °; *FOV,* describing the curved area of a substrate, is a degree. The optics plate carrying the laser source and modulating optics can be tilted as well. These tilting units are precisely controlled by interferometer in 10 nm resolution. To prevent variation of exposed structures, it is crucial to focus the incident beam onto planar and non-planar substrates during the exposure. Instead of the standard air-pressure-controlled autofocus system, an optical autofocus is implemented, which will work correctly on non-planar surface.

3.3.3 Optical and metrology system

The optical and metrology system in the modified LWL system are equipped with two cameras: one camera with a large field of view is used to locate alignment marks, and another camera with a high resolution is intended to align these marks. Level-to-level alignment is performed in the following manner. To begin with, leveling of the substrate is required due to the tilted optics plate and/or un-leveled substrate table. This can be done by focusing the beam on flat

areas. Then the compensation of theta of the stage should be done to set the origin for the alignment determining the degree of misalignment. Finally the alignment of new layers to existing layers is performed manually.

3.3.4   Data preparation/conversion and exposure

The conversion software of the LWL system takes multiple design formats (i.e. DXF, GDSII, CIF, etc.) and converts them to the system format (LIC) ready for exposure. So various design software can be used for data preparation. Input data to be exposed can be prepared on a flat surface (two dimensional) using commercial CAD programs, Design Workshop, Cadence Virtuoso, and etc. Dimensional deformation, however, cannot be avoided after the input data is projected onto non-planar surface. As shown in Figure 3.10, the extent of deformation depends on a curvature of the substrate. Figure 3.10 (a) shows schematics of the curved substrate used for the experiment as well as how to estimate the deformation for various *FOV*. *R* is the radius of curvature of a curved substrate; *Θ* is a half of *FOV*; *L* and *L'* represent the dimension drawn on flat surface and projected onto curved surface, respectively. The relationship between *L* and *L'* is derived below:

$$L' = L \times \sec\theta, \ where \ \theta = \frac{FOV}{2}. \tag{3.3}$$

The expected extent of deformation depending on the curvature of substrate (i.e. *FOV*) is shown in Figure 3.10 (b); for a curved substrate with *FOV* of 33.5°, 40.5°, and 120°, the deformation are 2%, 6%, and 100%, respectively, by calculating *(L' - L)/L* using MATLAB. Properties of our customized glass (BK-7) substrates are summarized in Table 3.3, and Figure 3.11 shows the details of our substrates design.

(a)

(b)
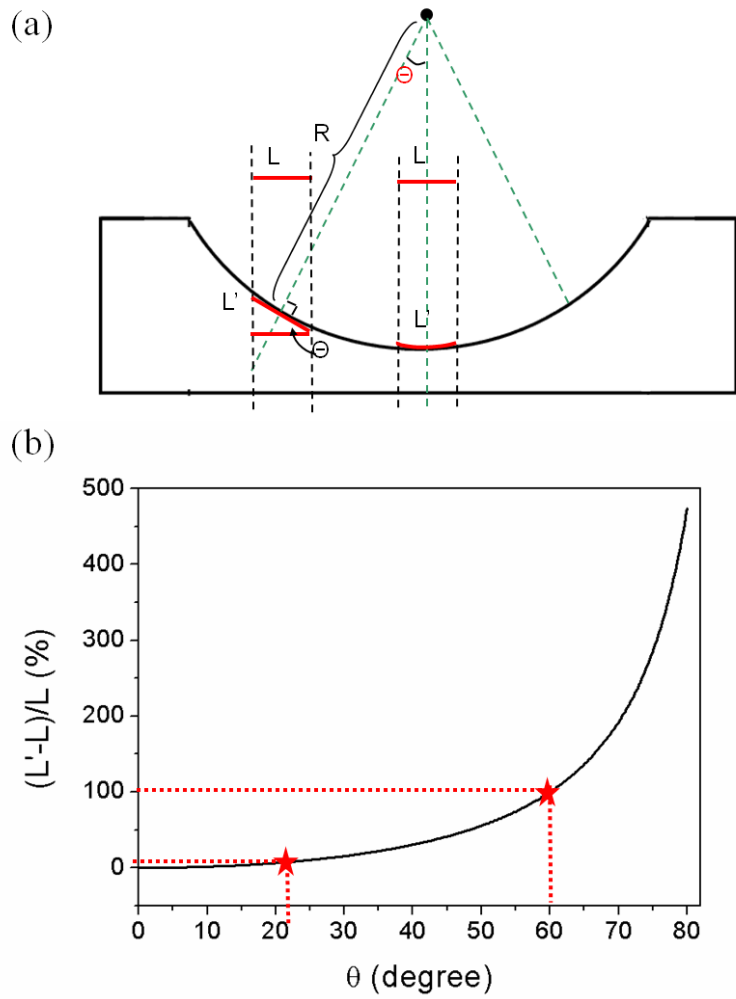
Figure 3.10 (a) Schematics of a customized substrate (b) Expected extent of the dimensional deformation vs. the degree; for *FOV* of 33.5 °, ~2 %; for *FOV* of 40.5 °, ~ 6 %; and for *FOV* of 120 °, ~100 %.

Table 3.3 Properties of BK-7 optical material

Max Temperature	350 ℃
Thermal conductivity	0.0026 cal·cm/cm^2/sec/℃
Coefficient of Thermal Expansion	86 x 10^{-7} cm/cm·℃
Optical Transmission Range (> 90%)	350 nm ~ 2.0 µm
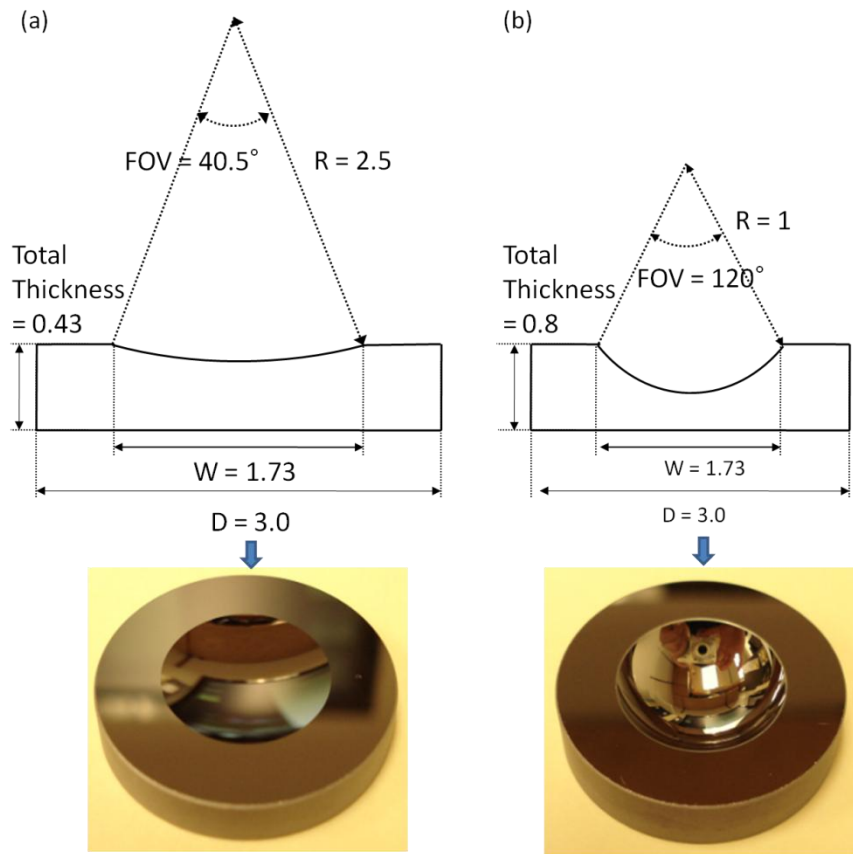
Figure 3.11 Customized BK-7 concave glass substrates with *FOV* of (a) 40.5 ° and (b) 120 °; 2000Å Cr was deposited for a clear picture. Unit is [cm].

To prevent aforementioned dimensional deformation, input data need to be created directly on the non-planar surface. First the same non-planar surface on which the input data to be projected should be generated using commercial CAD programs. Dimensional parameters of the non-planar substrate should be collected very accurately (i.e. radius of curvature, diameter of the curved area, and etc), and provided for this purpose. The input design is created directly on the generated virtual surface, projected onto a planar surface, and saved as one of the aforementioned data formats. Then the design is converted to the system format (LIC), projected onto the real curved surface, divided into sub-fields, and fitted onto the curved surface by the conversion software of the LWL system. The moving and tilting substrate stage makes each sub-field perpendicular to the incident writing beam to prevent deformation of exposed structures on each sub-field. The sub-fields are exposed individually and stitched together.

3.3.5 Subfield and stitching

When the active area where we want to fabricate devices or circuits is larger than the spot size of exposing light, decomposition of input data into small areas, which is so called *subfields*, is mandatory. However, during individual exposure of each subfield, the amount of exposed light between adjacent subfields is not exactly the same because error exists in positioning the substrate and incident light can be reflected from the curved surface. As a consequence of unequal light dose, the exposure is not uniform producing mismatches. Therefore, stitching problem appears after photoresist development and it gets worse toward the edge of curved area (e.g. high curvature area). Resist left, as shown in Figure 3.12 (a), causes unexpected connections, and distorted structure in Figure 3.12 (b) leads to misalignment and thus device failure. The stitching problem leading to unexpected connections and distortion/variation of structures can be corrected and minimized by optimizing the intensity of exposing light and reducing its difference

between subfields. Thus, we can successfully demonstrated working TFTs and circuits using LWL in the following chapter 4 and 5, respectively.
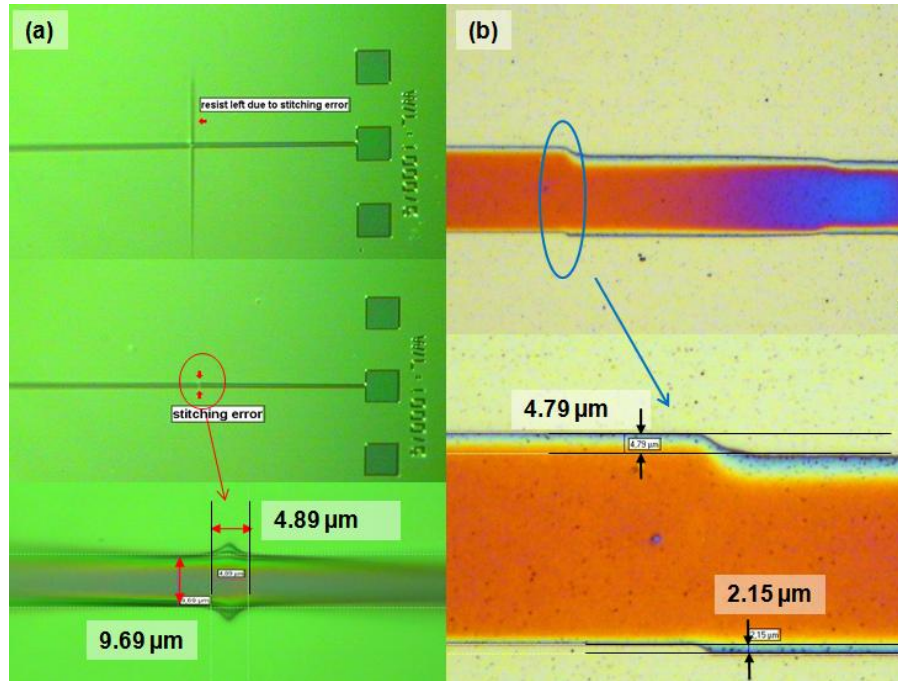
Figure 3.12 Stitching problem after photoresist development caused structure variation.

3.3.6   Structuring accuracy of LWL on a curved surface

To evaluate the influence of the substrate curvature on LWL exposure accuracies, we measured dimensions of patterned structures from various locations over a curved surface using special 3D digital microscope (Keyence VHX-600) as shown in Figure 3.13 (a). Source-drain structure in Figure 3.13 (b) was prepared; Cr of 2000 Å was deposited on a curved substrate by a sputtering method and then the Cr source-drain electrode was patterned by LWL and wet-etch. Typical microscope has a problem with focusing and measurement on a curved surface due to the substrate curvature. However, the Keyence microscope has a capability of observation at all angle

with a swivelable stage. Figure 3.13 (b) shows clearly such an advantage of using Keyence microscope on a curved surface.
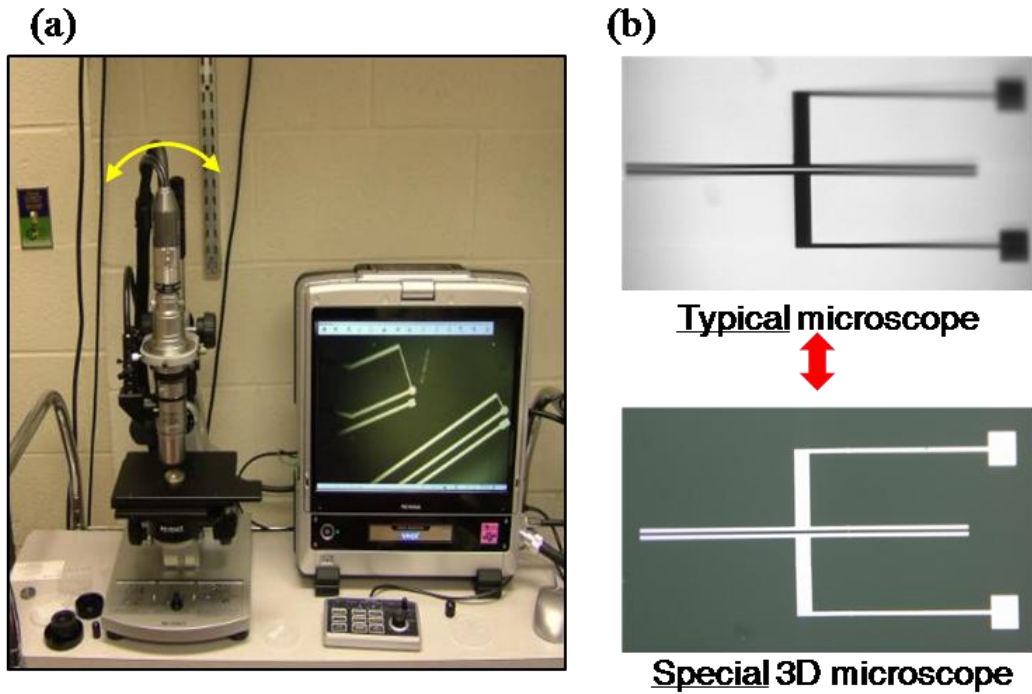
Figure 3.13 (a) Photography of Keyence VHX-600 microscope (b) comparison of 3D microscope to typical microscope providing blurred image due to losing focus.
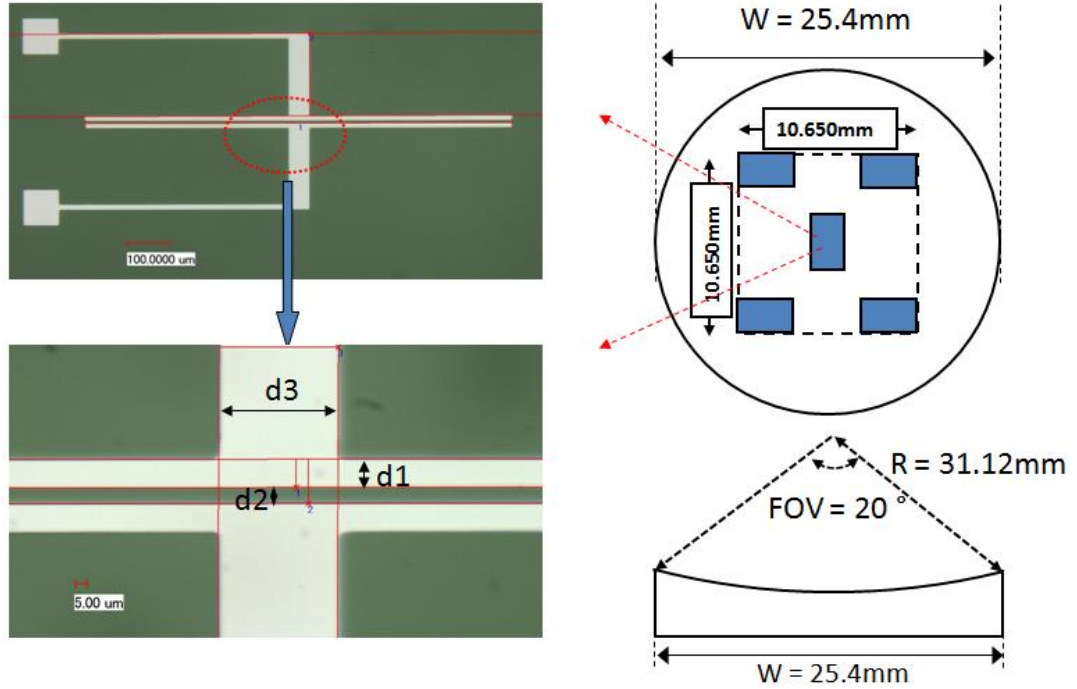
Figure 3.14 Pictures of test structure and its location over the curved surface; illustration of top and cross section view of the substrate.

	Error [%]				Error [%]		
Before Etching	d1	d2	d3	After Etching	d3	d4	d5
Center	6.36	1.67	3.54	Center	0.91	6.67	2.50
Lower Left	5.45	3.33	3.54	Lower Left	3.63	6.67	3.33
Upper Left	1.81	8.33	2.92	Upper Left	0.91	8.33	2.50
Lower Right	4.54	5.00	6.67	Lower Right	0.91	5.00	3.33
Upper Right	~ 0	6.67	3.54	Upper Right	2.72	13.3	3.12

Table 3.4 Summarized discrepancy of dimension between measured structure (d1,d2, and d3) and its electronic design.

A test structure of source-drain layer of standard TFT was patterned over a curved substrate that has a radius-of-curvature of 3.1 cm but smaller *FOV* of 20 °. We measured patterned structures (d1, d2 and d3 of) and calculated averaged discrepancies in comparison to electronic design from five different locations after both photoresist development ('before etching') and etching ('after etching') as shown in Figure 3.14. As summarized in Table 3.4, before etching, the average error in center area and curved area were 3.86 % and 4.30 %, respectively; after etching, the average error in center area and curved area were 3.36 % and 4.48 %, respectively. There was no significant discrepancy of dimension between the fabricated and electronic design on the curved substrate, which is in agreement with the theoretically investigated results described in the previous section.

3.3.7 Advanced LWL system for device/circuit fabrication processing on a curved surface with FOV = 120 °

The modified system described in previous sections is capable of performing exposure on a curved substrate of *FOV* up to 20° because the substrate table can only be tilted up to ± 10°. To implement LWL processing on a substrate with larger *FOV* (e.g. 120°), we developed in collaboration with the Heidelberg Instruments a special unique LWL system. Most of all, in this tool the substrate table is modified for tilting as well as rotating the substrate to accommodate larger *FOV* substrate up to 120°. Instead of horizontal mounting shown in Figure 3.8, vertical mounting of substrate was used to reduce substrate table positioning error and inefficiency from not perfect rotating. Figure 3.15 shows our advanced LWL system, and Table 3.5 summarizes its specification. Unfortunately, this advanced LWL system was placed at the CBrite, Inc. location due to DARPA project termination, and therefore we did not have a chance to conduct an experiment using this system.
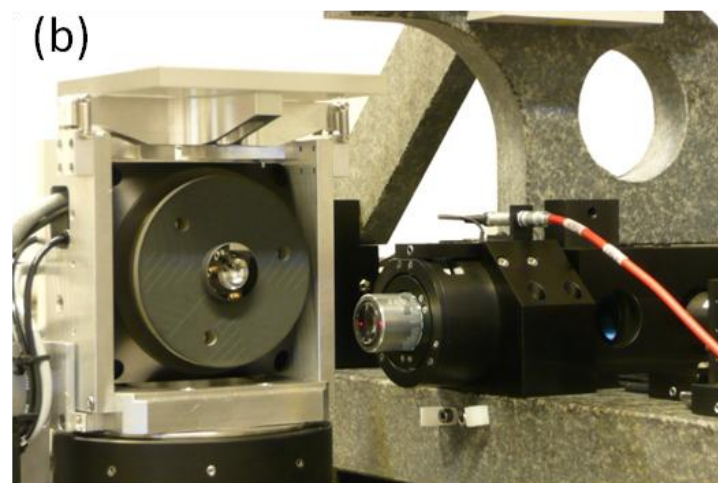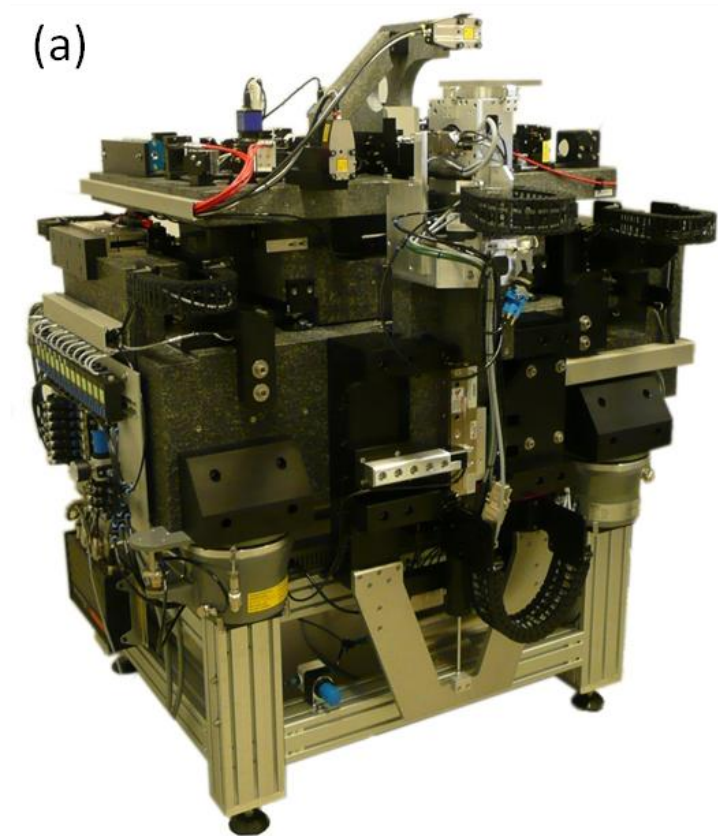
Figure 3.15 (a) System overview of our proposed LWL system for *FOV* up to
120 ° (b) Substrate chuck and write head.

Address Grid [nm]	50
Focal Length of Laser Beam [mm]	10
Minimum Feature Size [µm]	1.5
Write Speed	6 hours per our substrate (design III)
Registration Accuracy [3σ,nm]	600
Overlay accuracy [3σ,nm]	450

Table 3.5 Specification of our proposed LWL system for a substrate with *FOV* of 120° (design III)

3.4   Conclusion

In this chapter, we demonstrated the feasibility of using the LWL system together with level-to-level alignment in the fabrication of the a-Si:H TFTs on a planar surface; 5 µm channel length TFTs were fabricated successfully. The unique advantage of the LWL process is the easy access to modify design during process development since lithography process is performed directly from electronic design rather than from photo-masks. This LWL fabrication method using the LWL can be an alternative to conventional photolithography for a rapid and a low-volume prototyping by reducing turn-around time and cost of the mask fabrication process. The proposed fabrication technique can be extended from the research to the development and fabrication of large area electronics including flat panel displays, x-ray imager, and solar panels.

We further described and discussed what kinds of requirements should be met to realize the LWL process on a non-planar surface based on the extensively modified LWL system: tilting substrate table, optical and metrology setup, and special data preparation/exposure using conversion software were described. To correct stitching problem occurring between subfields, the exposure condition should be optimized. The investigated results of the structuring accuracy over a curved surface using the modified LWL system was in agreement with the theoretical

study and showed about 5 % deviation in comparison to electronic design for the substrate with FOV of 20 °. Finally, we developed in collaboration with Heidelberg Instruments LWL system for processing a substrate with the FOV up to 120 °.

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Chapter 4

Maskless Processing of a-Si:H TFT on a Curved Surface

4.1 Introduction

There is increasing demands for the implementation of electronic and optoelectronic systems on non-planar surfaces for their diverse and unique applications: biometrics [1], artificial retina [2], imaging sensors [3] and non-flat display [4]. Various approaches, therefore, have been proposed to realize functional devices on non-planar or hemispherical surfaces: transfer-based fabrications [3, 5, 6], self-assembly [4, 8, 9], interconnection of device tiles [10], and contact patterning methods [11, 12]. Although all the proposed methods have demonstrated feasibility, they are not desirable to realize highly integrated and complex device structures and circuits with an acceptable fabrication yield. These strategies are limited by strain due to deformation [5-7], lack of scaling capability [3, 4, 8, 9, 10] and poor level-to-level alignment accuracy [11, 12]. Also normal contact photolithography cannot be used for non-planar surfaces due to the substrate curvature. To circumvent these limitations, we used a combination of proven maskless laser-write lithography (LWL) [13, 14] initially developed for flat surfaces and hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) technology developed for flat-panel display to realize a-Si:H TFTs on a concave substrate. This direct LWL fabrication method is free from stress or deformation induced by transfer-based approaches. High-resolution interferometer monitoring (< 10 nm) and precisely controlled tilting-stage in the LWL system can provide a high level-to-level

alignment accuracy as discussed in chapter 3. In this chapter, we describe the maskless fabrication of the a-Si:H TFTs with various channel widths and channel length of 10 µm on a concave surface. The electrical characteristics and the impacts of the curvature on both TFT fabrication and electrical performance are also described.

4.2 Fabrication of a-Si:H TFTs on a Curved Surface using Maskless LWL

4.2.1 Customized curved glass substrate

Figure 4.1(a) illustrates our customized BK-7 concave glass substrate used in this work. BK-7 (Table 4.1) is a borosilicate crown optical glass used in standard optical glass component. For uniform film deposition and coating, the surface is highly polished to scratch-dig of 20-10, which permits a scratch width of 0.02 mm and a dig diameter of 0.1 mm. Since various layers of materials need to be processed for fabricating TFTs and circuits, precise alignment between layers should be performed. Level-to-level alignment marks are placed on a flat area as indicated by gray crosses. The radius-of-curvature (ROC) is 3cm, the field of view (FOV) is 33.5°, and the total diameter including a flat area is 3cm.

Table 4.1 Properties of BK-7 optical materials

Max Temperature	350 ℃
Thermal conductivity	0.0026 cal·cm/cm^2/sec/℃
Coefficient of Thermal Expansion	86 x 10^{-7} cm/cm·℃
Optical Transmission Range (> 90%)	350 nm ~ 2.0 µm
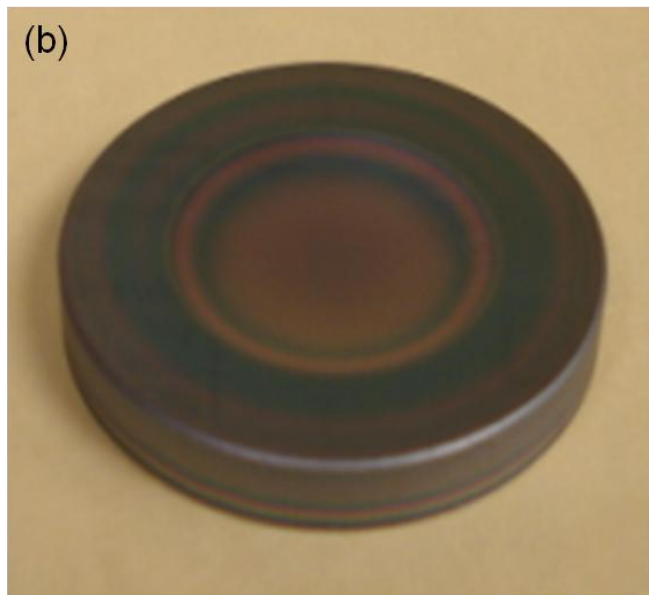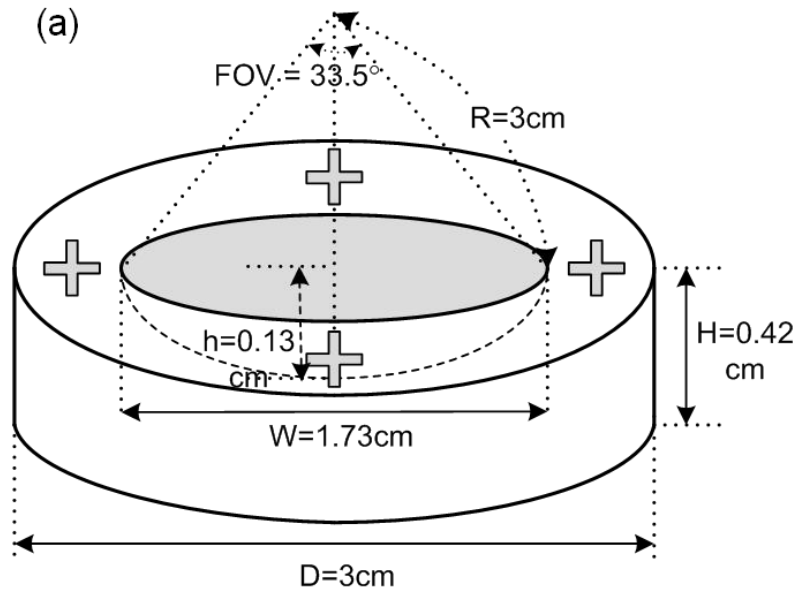
Figure 4.1 (a) an illustration of the customized concave glass substrate; crosses represent alignment marks on the flat area. (b) a picture of customized substrate coated with thin-film materials.

4.2.2 Thin-film deposition and etching on curved surfaces

Uniformity evaluation of thin-films deposited by plasma-enhanced chemical vapor deposition (PECVD) and etched by reactive-ion etching (RIE) was conducted by acquiring and analyzing scanning electronic microscope (SEM) images. As illustrated in Figure 4.2(a), after cleaving the concave substrate through the center, we took pictures of the cross section from the vertex to the edge of the curved surface with 1mm distance between images. Figure 4.2(b) shows
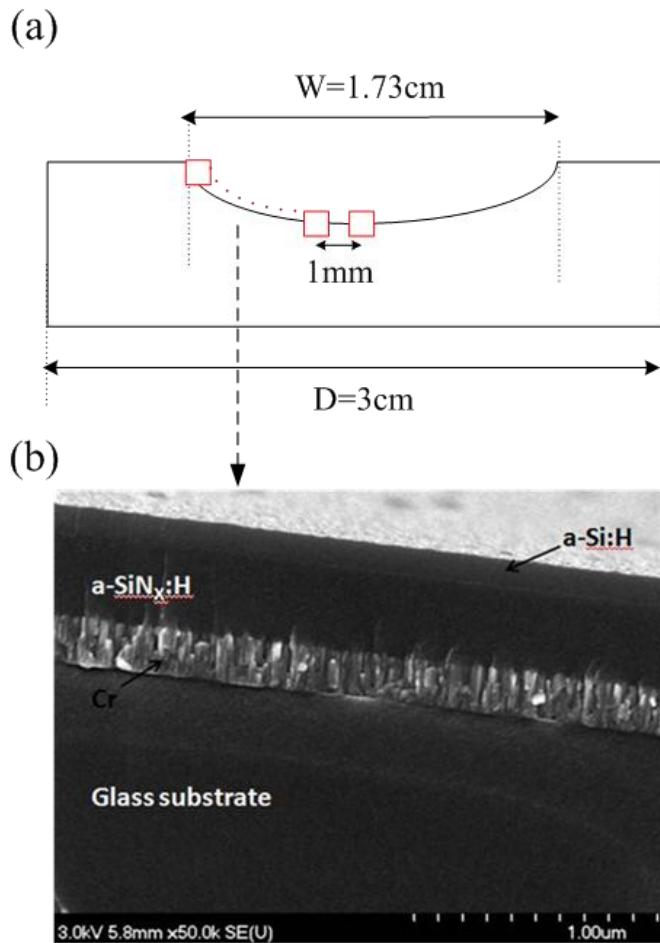
Figure 4.2 (a) Illustration of the method used to get cross-sectional images of the curved surface. (b) Scanning Electronic Microscope (SEM) image captured in the middle of curved area.

an image taken in the middle of the concave surface. We then collected nine data points of thickness distribution for each layer. The thickness variations of each layer are as follows: chromium (Cr) of the gate electrode (203nm ±8), the tri-layer deposition of hydrogenated amorphous silicon nitride (a-SiN$_X$:H) / a-Si:H / P-doped a-Si:H (n+ a-Si:H) (634nm ±70), and the etched thickness of the active channel layer by RIE (118nm ±14). Although the sputtered Cr layer showed a low deviation due to the benefit of physical vapor deposition, thin-film deposition and etching by PECVD and RIE method, respectively, showed relatively higher deviation that can be due to a non-uniform flow of gas mixtures over flat and curved surfaces.

4.2.3   Spin-coat of photo-resist on curved surface

Prior to each LWL exposure step, the photoresist (AZ 1505) was spin-coated to form a uniform coating over the curved surface. For uniform resist coat, the following mathematical condition should be met;

$$r < 0.816 \cdot R \text{ given that } 0.816 \cdot R < \sqrt{R^2 - \frac{g^2}{\rho^2 \cdot \omega^4}}, \tag{4.1}$$

where r is the radius of substrate, R is radius of curvature, g is acceleration of gravity, ρ is the fluid density, and ω is the angular velocity [16]. In other words, with proper photoresist viscosity and spin speed, a concave substrate with W (diameter of concave area) < 1.632R can be spin-coated with a uniform photoresist. For instance, the highest FOV to be successfully spin-coated is ~109 °. So an alternative resist coating method (e.g. spray-coat) needs to be investigated for a curved substrate with a FOV larger than ~109 °. The forecast on feasibility of spin-coat method on various substrates is shown in Table 4.2.

Substrate	Substrate Conditions				Spin-Coat Feasible?
	R [cm]	W [cm]	W/R	FOV [°]	
I*	3	1.73	0.577	33.5	Yes
II	2.5	1.73	0.692	40.5	Yes
III	1	1.73	1.73	120	No**

Table 4.2 The feasibility of photoresist spin-coating on various substrates; * used in this work; ** alternative resist coating method needs to be investigated.

The ratio of our customized substrate-radius ($r = 0.865$ cm) to radius-of-curvature ($R = 3$ cm) is below 0.816, which guarantees the spin-coated film is nearly homogeneous over the curved surface. To evaluate the thickness difference of spin-coated photoresist between curved and flat areas, we partly removed the resist and measured the thickness across the sample using a mechanical profiler. The thickness of the photoresist on a flat area (594 nm $\pm$ 20) was slightly thicker than that of a curved surface (575 nm $\pm$ 20) at 4000 rpm. This difference does not have any impact on LWL exposure conditions.

However, larger film-inhomogeneity was observed over the transition area between curved and flat areas, and it was found to be due to the edge-bead formation. The measured width and height of the formed edge-bead using the mechanical profiler were in the range of 100 - 250 µm and 200 - 500 nm, respectively (Figure 4.3(a)). These edge beads can cause additional connection, distortion of the structure size and/or breakup of the patterns lying over the transition area (Figure 4.3(b)). This is due to the remained non-exposed photoresist after development process, which will affect the subsequent etching process step.
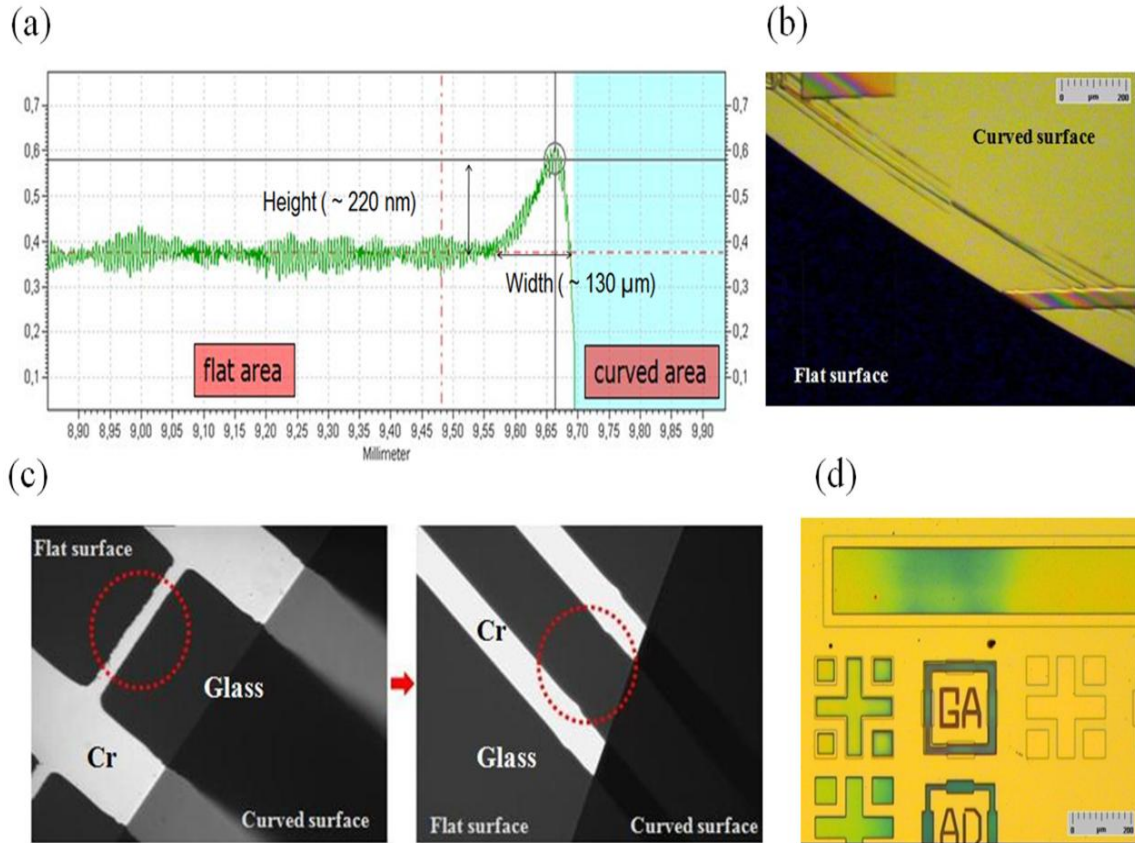
Figure 4.3 (a) Thickness profile of the spin-coated photoresist over the transition area. Measured height and width of the edge-bead shown. (b) Distortion and additional connection of patterns due to edge-bead formation over the transition area between a curved and flat area. (c) Additional connection (red circle area) formed by edge-bead of the photoresist was removed by the local double exposure (d) Optical microscope image of the alignment marks after Gate electrode to Active island layer exposure; Photoresist was not removed to capture clear images.

To correct the edge-bead formation, we used the local double LWL exposure method, consisting of double exposure of the edge-bead formed areas with different light doses. Such local-double exposure will allow full removal of the exposed areas during the development process in AZ 726 MIF developer for 35 sec. Hard-baking was performed in an oven at 110 ℃ for 10 min after each photolithography development process step. Figure 4.3(c) shows the results before and after the local-double exposure treatment. To perform the local-double exposure

precisely, it was found that the substrate dimension must be very well defined ($\pm$ 0.1 mm) to provide the reference dimension of the curved areas.

The spray-coat method was investigated for the substrate III (FOV = 120°), on which a photoresist could not be spin-coated. We explored spray-coaters from Special Coating System (SCS) and SUSS MicroTec; the photoresist (AZ1505) film was coated by spraying technique followed by soft-baking at 90 ℃ for 5 mins. To evaluate thickness difference of spray-coated photoresist across the substrate, we partly removed the resist and measured the thicknesses using a mechanical profiler. Thickness variations of the spray-coated resist were about 474 nm $\pm$ 90 for SCS tool and 319 nm $\pm$ 225 for SUSS system (Figure 4.4). The aforementioned edge-bead problem was even worse in the investigated spray-coat method because of the steeper angle near the transition between the flat and curved area; there was significant variation of the measured dimensions of the formed edge-beads depending on their location on the substrate. For SCS tool the width and was the height were 45 – 345 µm and 120 – 935 nm, respectively; for SUSS system the width and the height were 115 – 420 µm and 190 – 2485 nm, respectively. Such a large variation makes it impossible to correct problems (i.e. additional connections and distortion of structures) induced by the edge-bead formation. The poor inhomogeneity of the film together with the large variation of edge-bead dimension indicates that the spray-coat method is not eligible for LWL processing on the substrate III at the moment. Possible improvements could be expected after full optimization of spray-coating tool is done. However other thin film deposition methods should also be investigated
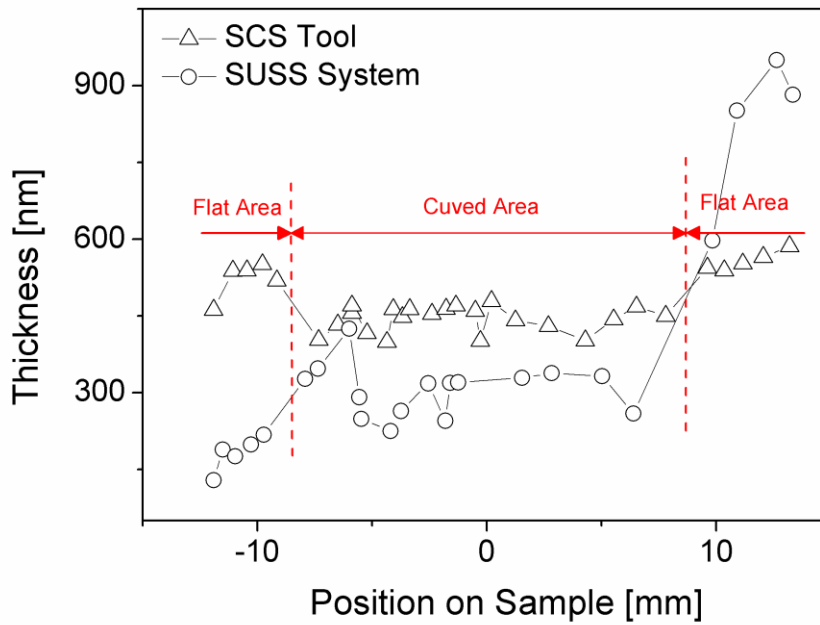
Figure 4.4 Thickness distribution of spray-coated photoresist (AZ1505) across the substrate III

4.2.4 Level-to-level alignment on a curved surface

Level-to-level alignment with a high accuracy is the central critical issue for fabricating fully functional devices and circuits. The optical and metrology system in the LWL is equipped with two camera systems. One camera with a large field of view is used to find alignment marks located on the flat area of the substrate, and another camera with a high resolution is intended for aligning these marks. Figure 4.3(d) shows part of the alignment marks used in this experiment. It was performed in the following manner: to begin with leveling of the substrate is required due to the tilted optics plate and/or un-leveled substrate stage. This can be done by focusing the beam on flat area. Then the compensation of theta (ɵ) of the stage should be done to set the origin for the

alignment, which determining the degree of misalignment. Finally the alignment of a new layer to existing layers is performed.

The level-to-level alignment error is defined as the relative position deviation of the alignment marks within the two following layers, and we derive vertical and horizontal deviation from the measurement of the distance of the borders on four sides in the bar alignment mark. The measured error was less than 2 µm for TFT with a 10 µm channel length and up to 300 µm channel width. The procedure for level-to-level alignment described here will not be affected by the substrate curvature (e.g. $FOV = 120$ °) because alignment marks are placed on flat areas.

4.2.5 Concentric exposure strategy

Following the photoresist spin-coating and soft-baking in an oven at 90 ℃ for 5 min, LWL was used to expose all device layers before each processing step. In our experiment, a concentric-circle exposure-strategy similar to what *Y. Xie et al* demonstrated [13] was used instead of a conventional exposure method [14] which would decompose the electronic design data into square subfields. This alternative is developed because 33.5° FOV of our substrate exceeds the maximum mechanical tilt angle (20°) of the substrate table in the present LWL configuration [14], i.e. the area to be exposed cannot be perpendicular to the incident light and therefore a uniform pattern of photoresist would have been difficult to achieve. Our strategy [15] takes advantage of the nonzero depth of focus of the writing laser beam and capability of the LWL system to tilt the optics plate, not of rotating substrate stage; this tilting capability of optics plate was implemented to allow for a variety of substrate thickness and to enable focusing on the subfields during the conventional exposures.

The idea is to decompose the electronic design into circular subfields, and some optical facts need to be considered. Most of all, the depth of focus should not be exceeded. By assuming the laser-write beam as Gaussian beam, the Rayleigh length (Z_0) is given by

$$Z_0 = \frac{\pi \cdot w_0^2}{\lambda}, \tag{4.2}$$

where λ is the wavelength and w_0 is the radius of the beam. In Figure 4.5 (a), the radius of the

beam can be expressed as

$$w(z) = w_0 \cdot \sqrt{\frac{\Delta z^2}{z_0^2} + 1}. \tag{4.3}$$

For a maximum allowed spot size after defocusing, $w_{max} = m \cdot w_0$, we get the maximum height

of circular subfields, $\Delta z(w_{max})$. With the given $\Delta z(w_{max})$ and radius of the curvature, R, the

width of the subfield rings for equal Δz is given by

$$\Delta x(\Delta z) = \sqrt{R^2 - \left(z + \Delta z\left(w_{\max}\right) - R\right)^2} - \sqrt{R^2 - \left(z - R\right)^2}. \tag{4.4}$$
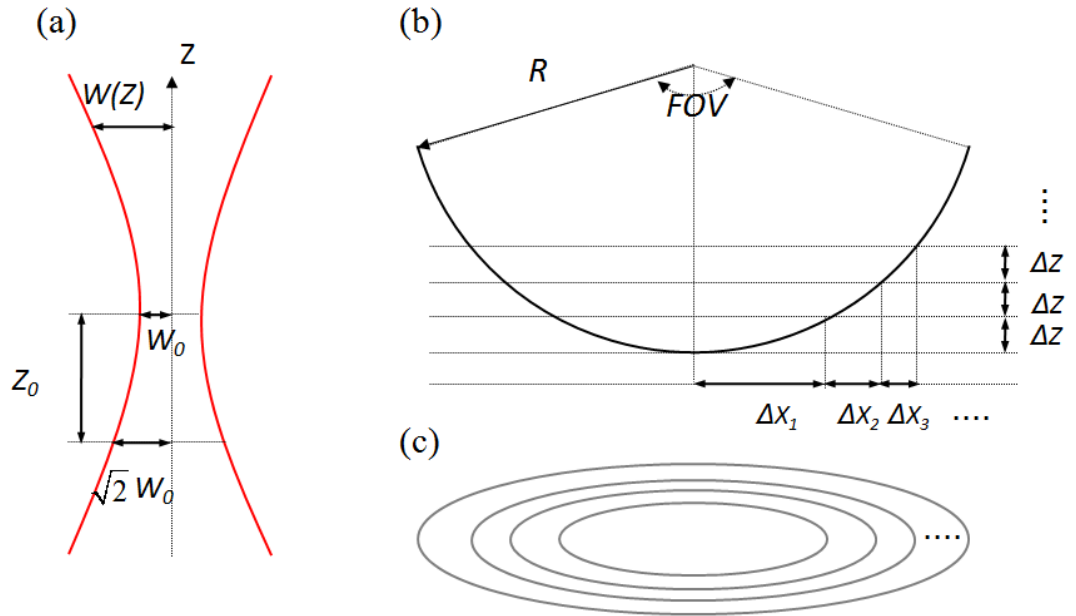
Figure 4.5 (a) Gaussian beam width w(z) as a function of the axial distance z. (b) Geometry
of circular subfields for spherical surface. (c) Illustration of the decomposition of design
into the subfields.

70

For our data preparation, we use $w_{max} = \sqrt{2} \cdot w_0$, where the spot area gets double and Δz is equal to the Rayleigh length. We count the number circular subfields and divide the data into those rings having width of Δx as illustrated in Figure 4.5 (b-c). Finally the respective area is converted to a format that is readable to the LWL system. Since the defocusing gets severe for larger FOV and/or too many rings are required for a smaller feature size causing increased exposure time and data conversion efforts, this concentric exposure strategy may not be the best approach. With this concentric exposure strategy, the minimum feature size of 5µm can be achieved. So we fabricated a-Si:H TFTs with 10 µm channel length in this work. A specially customized LWL tool is necessary for exposing concave/convex substrates of higher FOV with a smaller feature size as discussed in chapter 3.

4.2.6 Maskless LWL TFT fabrication process sequence on a curved surface

First, Cr of 200nm was deposited by a sputtering method and then the Cr gate electrode was patterned by wet-etching using CR-14 (CH_3COOH: $Ce(NH_4)_2(NO_3)_6$: H_2O in 9:22:69) etchant (layer #1). Next, PECVD was used to deposit a tri-layer of gate silicon nitride (a-SiN$_X$:H, 400nm) forming a gate insulator together with amorphous silicon (a-Si:H, 170nm) and phosphorous-doped (n+) a-Si:H (70nm) forming an active channel layer. The active island was defined by RIE dry-etching of a-Si:H and n+a-Si:H using a gas mixture of SF_6 and O_2 (layer #2). Following a deposition of a source/drain (S/D) metal Cr layer (130nm) by a sputtering method, wet-etching using CR-14 etchant was done to form S/D contacts (layer #3). Then to remove the n+ a-Si:H layer from the channel region, back-channel etching is performed by RIE dry-etching with a gas mixture of SF_6 and O_2 using the S/D metal and a photoresist as a mask. We subsequently defined contact via to the gate electrode using buffered hydrofluoric acid (BHF) (layer #4).
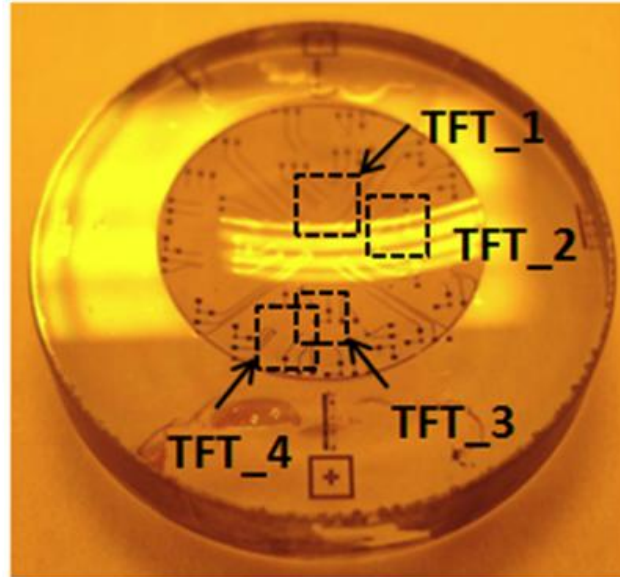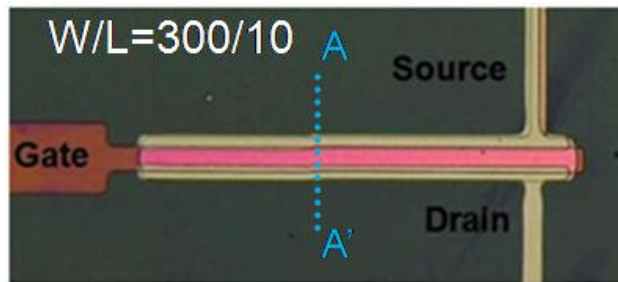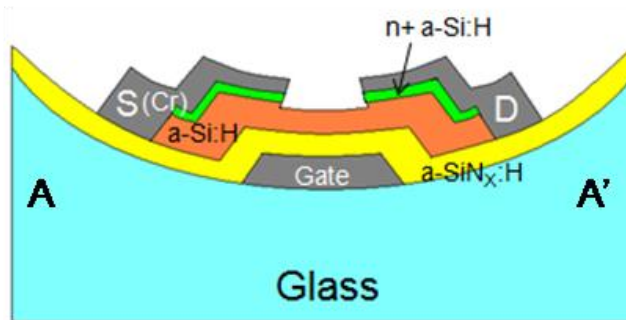
Figure 4.6 (a) Photograph of the fabricated substrate. Dashed squares show the measured a-Si:H TFTs. (b) Optical microscope image of the fabricated a-Si:H TFT (*W/L*=300/10) from the edge of curved surface. (c) Schematic of cross section view of fabricated TFT. The substrate curvature is exaggerated.

As a final step, thermal annealing was performed at 250℃ for an hour to improve electrical properties of each film layer [17]. Figure 4.6(a) and (b) show photographs of the fabricated substrate and a-Si:H TFT (*W/L*=300/10, 'TFT_2'), respectively. We note that for each processing step photoresist (AZ1505) was first spin-coated over deposited layers, and then exposed using LWL to realize level-to-level alignments. Finally, the photoresist was stripped using PRS-2000. Electrical measurements were conducted and analyzed using probe station in combination with HP 4156 at room temperature in dark condition.

4.3   Electrical Properties of a-Si:H TFT on a Curved Surface

4.3.1   Experimental results and discussion

To begin with, using the same procedure described in Chapter 3.3.5, we verified the accuracy of LWL exposure using concentric exposure strategy. We measured dimensions of channel length, width and gate electrode line width from 'TFT_1' and 'TFT_4' in Figure 4.6(a). The discrepancies of dimensions between fabricated structures and electronic design were calculated to be 4.16% for 'TFT_1' and 4.88% for 'TFT_4'. No significant dependency of patterned-structures accuracy on substrate curvature was observed by virtue of the optical auto-focus system, the high resolution interferometer monitoring and precise control of the substrate table of the LWL system [14].
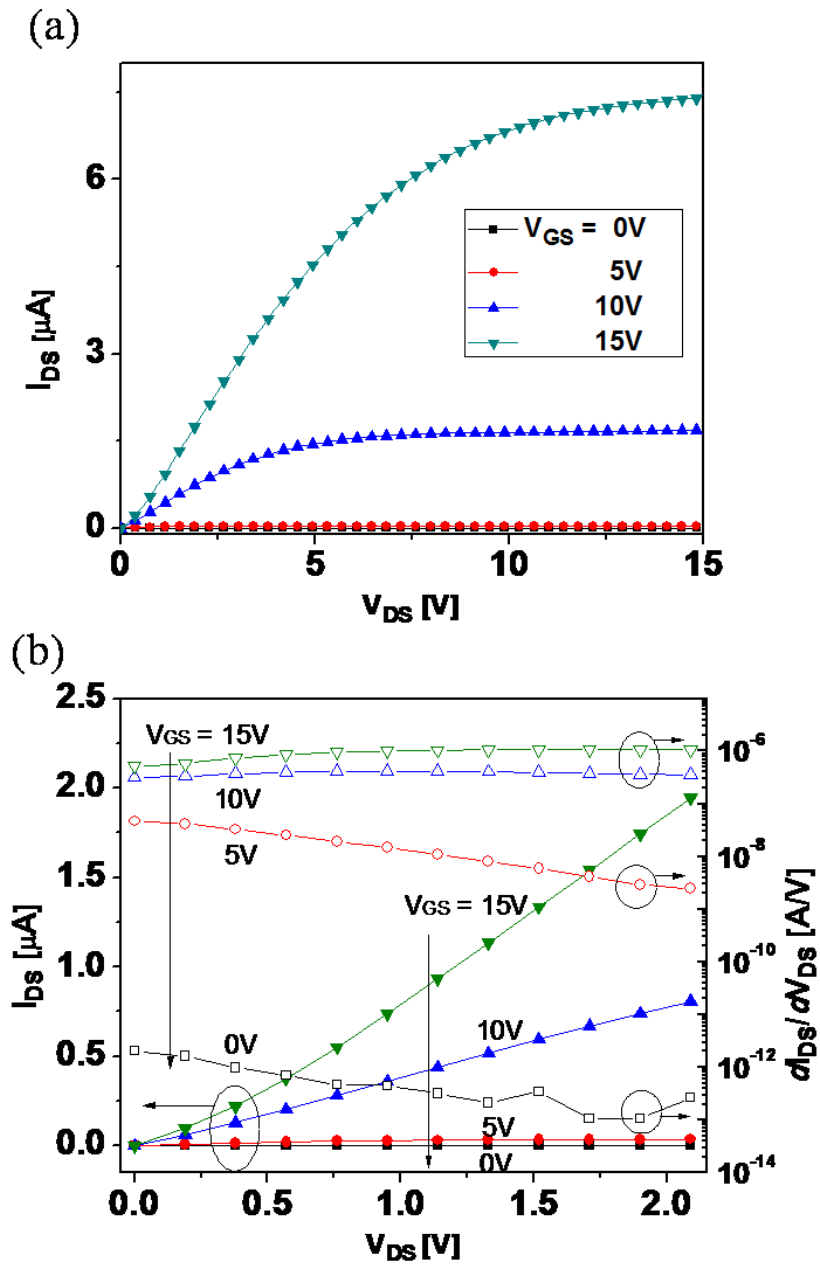
Figure 4.7 Electrical properties of the fabricated a-Si:H TFT (W/L=300/10, 'TFT_2') on a curved surface. (a) Output characteristics. (b) Output characteristics and output conductance in low V_{DS} bias region (0 ~ 2V).
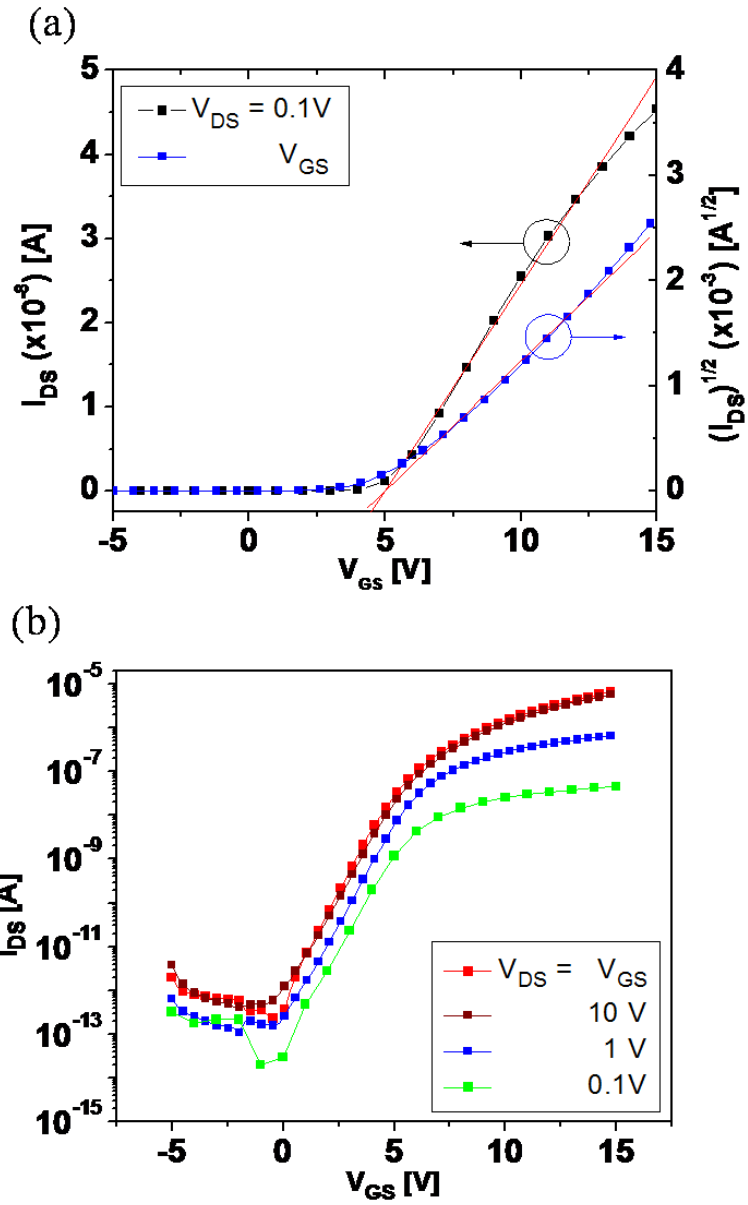
Figure 4.8 Electrical properties of the fabricated a-Si:H TFT (W/L=300/10, 'TFT_2') on a curved surface. (a) Transfer characteristics with fitting lines used for extraction of threshold voltage and mobility. (b) Transfer characteristics in a semi-log scale.

As indicated in Figure 4.6(a), output and transfer characteristics of a-Si:H TFTs at different locations were measured to evaluate the impacts of the substrate curvature on the device electrical properties. We first measured the output characteristics of TFTs for various gate voltages, V_{GS} = 0, 5, 10 and 15V (Figure 4.7 (a)). For the low V_{DS} bias (0 – 2V), Figure 4.7(b) shows the output characteristics and its output conductance defined as the derivative of the drain-to-source current (I_{DS}) with respect to drain voltage (V_{DS}). We swept V_{DS} from 0 to 15V and I_{DS} exhibits typical output characteristics. In Figure 4.8, the transfer characteristics for various drain voltages (V_{DS} = 0.1, 1, 10 V and V_{GS}) were measured. The data at V_{DS} of 0.1V and V_{GS} correspond to a linear and saturation operating regime, respectively. We used the 10-90% range data of the maximum I_{DS} for the extraction of threshold voltage (V_{th}) and field-effect mobility (μ_{FE}) in Figure 4.8(a). OFF-current (I_{OFF}) was extracted at V_{GS} = -5 V, and subthreshold swing (SS) was derived from the inverse of maximum slope in subthreshold region (Figure 4.8(b)). Other a-Si:H TFTs (i.e. TFT_1,TFT_3, and TFT_4) were measured and analyzed using the same approach. The variations of all TFTs' extracted parameter are calculated and summarized in Table 4.3.

Parameters	V_{DS} = 0.1V	V_{DS} = V_{GS}
I_{OFF} [A] at V_{GS} = -5V	$3.2 \times 10^{-13} \pm 1 \times 10^{-13}$	$5.5 \times 10^{-12} \pm 4.5 \times 10^{-12}$
V_{th} [V]	6.9 ± 1.8	5.7 ± 2
SS [V/dec]	1.21 ± 0.14	1.04 ± 0.2
μ_{FE} [cm2/Vs]	0.1 ± 0.02	0.21 ± 0.07

Table 4.3 Variation of the extracted parameters for all fabricated a-Si:H TFTs

For a linear (V_{DS} = 0.1 V) and saturation (V_{DS} = V_{GS}) regimes, the variations in V_{th} of all fabricated TFTs were ± 26 % and ±35 %, respectively; the variations in μ_{FE} of all fabricated TFTs were ± 20 % and ± 33 %, respectively; the variations in I_{OFF} of all fabricated TFTs were ± 31 % and ± 80 %, respectively; the variations in SS of all fabricated TFTs were ± 12 % and ± 19 %, respectively. These variations can be associated with the variation of the a-Si:H thickness (t_{si}) over the curved surface (153 nm ± 39 nm, ± 25 %) after back-channel dry-etching [18]. With an increase of the t_{si} in the dry-etched a-Si:H TFT, it is observed that V_{th}, SS and μ_{FE} tend to decrease [19, 20]. The variation of the t_{si} can be resolved by further optimizing dry-etch conditions or adopting isotropic wet-etching methods which are independent from the surface curvature.

The leakage current was less than 10 pA even in saturation operation regime, and the ON/OFF ratios of both linear and saturation regime are in the order of 5 and 6, respectively. As shown in Figure 4.8 (b), the linear behavior at low V_{DS} indicates good ohmic contact between source-drain electrode and n+ a-Si:H/a-Si:H layer. The smaller SS is, the better to make the TFT turned-off near V_{th} and to have less leakage current. Although SS of fabricated TFT on a curved surface is higher than other TFT fabricated in our lab (~ 0.6 V/dec), the electrical characteristics of fabricated TFTs is promising to be used as a pixel switch in passive pixel sensor application.

4.4   Conclusion

In this chapter, we described the LWL process development on a curved surface and addressed confronted issues related to thin-film deposition/etching and spin-coat of photoresist. a-Si:H TFTs with 10 µm channel length on the concave surface were fabricated using the maskless laser write lithography (LWL); a high level-to-level alignment accuracy (± 2µm or less) was also demonstrated for fabricated devices. The electrical performance of the fabricated a-Si:H TFTs

was characterized over the curved surface. Due to the thickness variation of the dry-etched a-Si:H layer over the curved surface, changes in OFF-current, field-effect mobility, subthreshold swing and threshold voltage were observed. These variations are acceptable for development of passive pixel sensor on a non-planar surface. The LWL fabrication of a-Si:H TFTs described in this chapter is suitable for the fabrication of a high-resolution TFT pixel arrays and circuits on a curved surface for passive pixel sensor application.

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Chapter 5

Electrical Instability of the a-Si:H TFTs on a Curved Surface

5.1   Introduction

There is increasing interest in implementing electronic and optoelectronic systems on non-planar surfaces for their unique application in image sensors; it allows for a larger field-of-view (*FOV*) and induces lower aberrations with less optical components [1-3]. Various approaches, therefore, have been proposed to realize functional devices on non-planar or hemispherical surfaces [2-5]. Although the proposed methods have demonstrated feasibility, they are not desirable to realize highly integrated and complex device structures and circuits. As an alternative, we have used a combination of maskless laser-write lithography (LWL) and hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) technology to demonstrate a-Si:H TFTs and circuits on a concave substrate as demonstrated in the previous chapters. Those devices fabricated on a spherical surface are free of mechanical stress induced by film deformation. It is still important to investigate the electrical characteristics and instability of those devices under prolonged bias-temperature stress (BTS) conditions.

In this chapter, we fabricated a-Si:H TFTs with a channel length of 10 µm on a concave substrate having enhanced *FOV* (40.5 °) and smaller radius of curvature (*ROC*, 2.5 cm) compared to the work in chapter 4. Furthermore, fully functional metal interconnect lines over the transition between curved and flat areas of a single substrate are demonstrated, for the first time, using a

local-multiple exposure approach. This method is an essential requirement for placing contact pads on the flat area and fabricating a large pixel array within the curved area. Finally we characterize and discuss the electrical properties and threshold voltage shift (ΔV_{th}) of the TFT fabricated on a spherical surface under various and prolonged BTS conditions in comparison with the a-Si:H TFT fabricated on a flat surface using the same LWL fabrication steps.

5.2 Experiments

Fig. 5.1(a) illustrates the customized concave glass (BK-7) substrate used in this chapter; level-to-level alignment marks were placed on a flat area as indicated by crosses. In order to be able to perform level-to-level alignment on a curved surface, the flat area has to be added at the edge of the substrate. The *ROC* is 2.5 cm; the *FOV* is 40.5 °; the diameter of the concave area (*W*) is 1.73 cm; the total diameter (*D*) is 3cm. Fig. 5.1(b) shows the fabricated devices and circuits on this concave substrate; inverted stagger a-Si:H TFTs were fabricated using six LWL exposure processes. For each device/circuit processing step, photoresist (AZ 1505) was first spin-coated over deposited thin-film layers and then exposed. More details about LWL processing of the a-Si:H TFTs on both flat and spherical surfaces can be found in chapter 3 and 4, respectively.

First, Cr of 200nm thickness was deposited by a sputtering method and then the Cr gate electrode was patterned by wet-etching using CR-14 (CH_3COOH: $Ce(NH_4)_2(NO_3)_6$: H_2O in 9:22:69) etchant (layer #1). Next, plasma enhanced chemical vapor deposition (PECVD) was used to deposit a tri-layer of gate silicon nitride (a-SiN_X:H, 400nm) forming a gate insulator together with a-Si:H (170 nm) and phosphorous-doped (n+) a-Si:H (70 nm) forming an active channel layer. A multiple-layer PECVD approach by *Kuo et. al.* [6] was used in this work. The active island was defined by RIE dry-etching of a-Si:H and n+ a-Si:H using a gas mixture of SF_6 and O_2 (layer #2). We subsequently defined gate contact-via to the gate electrode using buffered
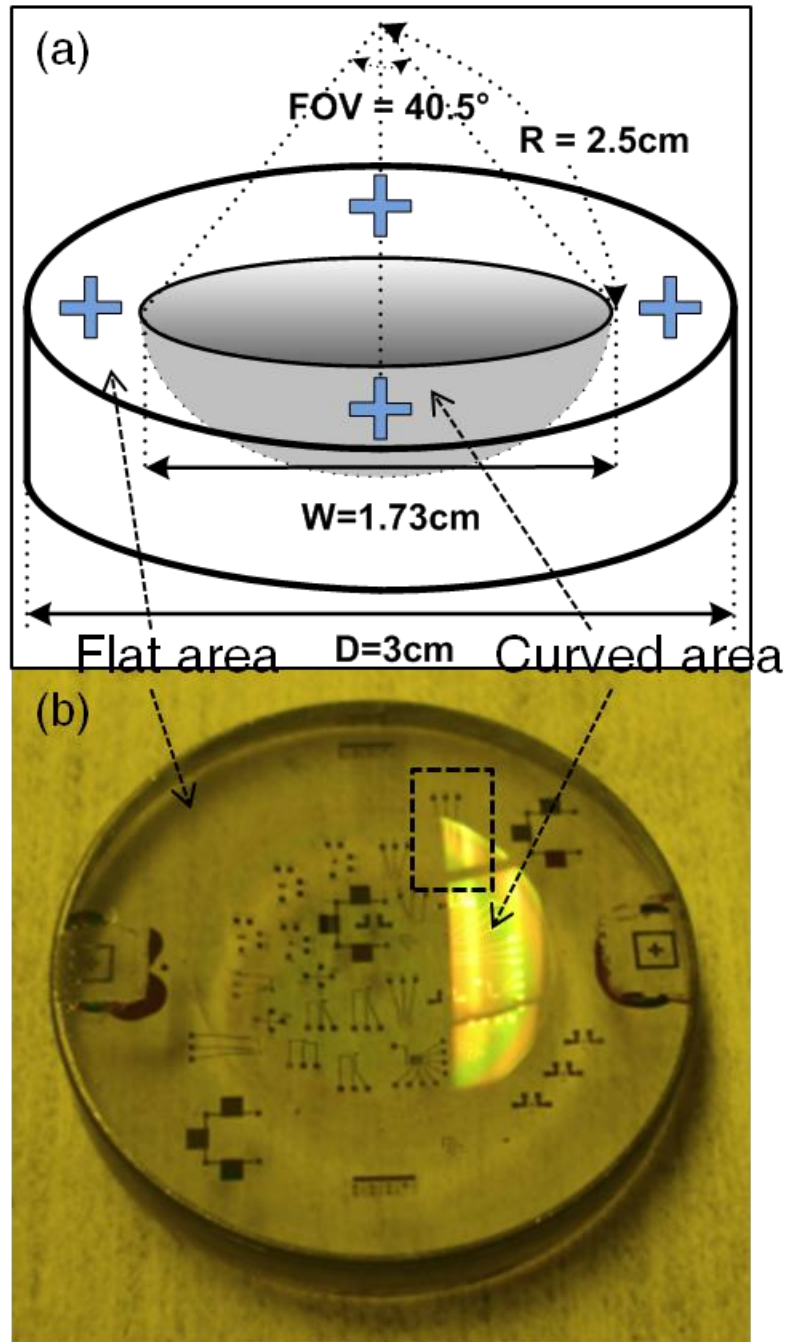
Figure 5.1(a) Illustration of the customized BK-7 concave glass substrate; crosses represent alignment marks placed on the flat area. (b) Photograph of the fabricated devices and circuits on the substrate. A dashed-box indicates the location of the a-Si:H TFT studied in this chapter.

hydrofluoric acid (BHF) (layer #3). Following a deposition of a source/drain (S/D) metal layer (200 nm of Cr) by a sputtering method, CR-14 was used to form S/D contacts (layer #4). Then to remove the n+ a-Si:H layer from the channel region, back-channel etching was performed by RIE with a gas mixture of SF_6 and O_2. As a passivation layer, we deposited 400 nm of a-SiN$_X$:H using PECVD and defined contact-via to electrodes by BHF (layer #5). Finally we deposited a Cr layer (200 nm) by sputtering and patterned it using CR-14 (layer #6). The fabricated TFT (W/L = 50/10) and a schematic of its cross-section view are shown in Fig. 5.2. Its location on the substrate is indicated by a dashed-box in Fig. 5.1. Thermal annealing was performed at 200℃ for two hours. Electrical measurements were conducted using a probe station in combination with HP 4156 semiconductor parameter analyzer at room temperature in dark condition.

For switch applications, only gate bias is applied externally and a certain voltage is present at a drain terminal due to, for example, storage capacitance charging-up. In analog circuits (e.g. amplifier and active load), however, both gate and drain bias are applied. In order to predict ΔV_{th} of the fabricated TFTs in such applications, BTS experiments were conducted for various V_{DS} (= 0, 5, 10, 15 V) at V_{GS} = 15 V that was slightly higher than the turn-on voltage of the TFT switch in passive pixel sensor operation (to be discussed in the next chapter). The total stress time (t_{STR}) was 10^4 sec, stress temperature (T_{STR}) was set to 80 ℃, and we only interrupted the applied stress for 60 sec to measure the transfer characteristics at V_{DS} = 1 V. We performed thermal annealing at 200 ℃ for two hours between the experiments to ensure the consistent initial properties of the TFT. The V_{th} was extracted using maximum slope method [7], and ΔV_{th} over t_{STR} is defined as follows

$$\Delta V_{th}(t) = V_{th} \ (t = t_{STR}) - V_{th}(t = 0). \tag{5.1}$$
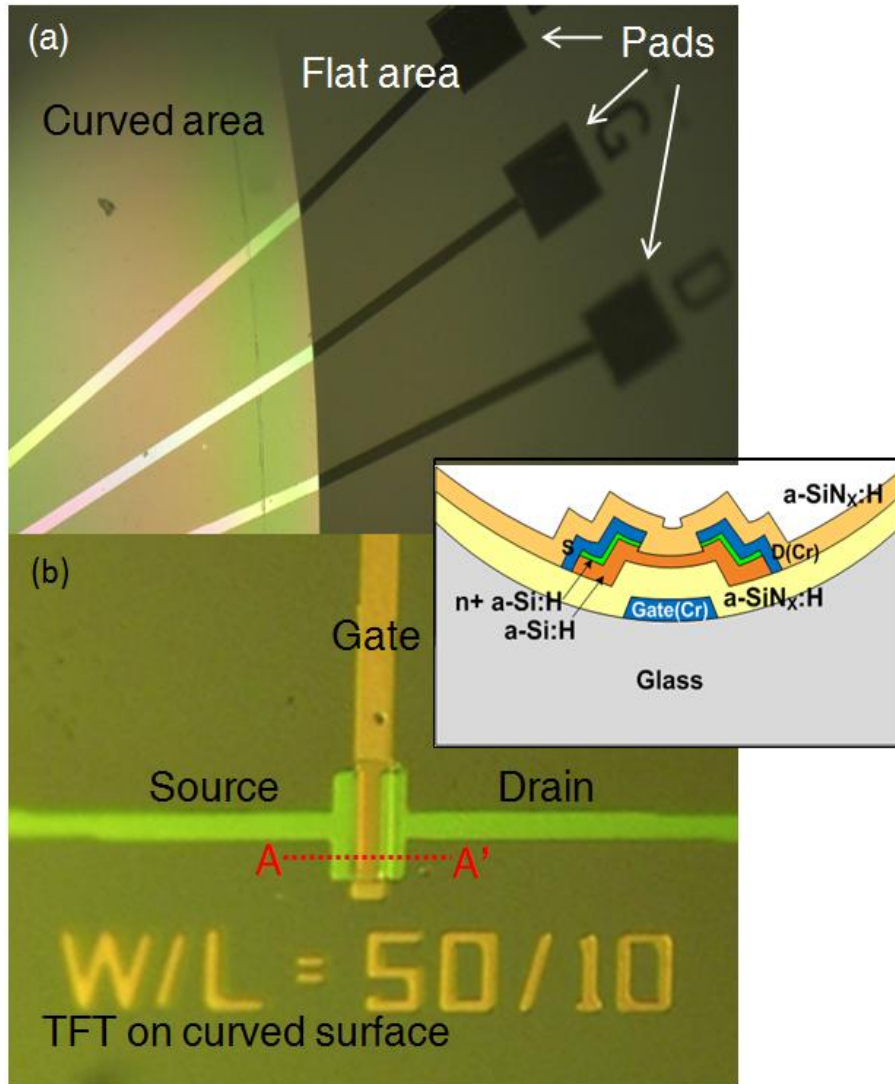
Figure 5.2 Optical microscope image of one of the fabricated a-Si:H TFTs. (a) The contact pads are placed on the flat area, and metal interconnect lines over the transition area leading to the fabricated device can be seen. (b) Enlarged image of the a-Si:H TFT (W/L = 50/10). The blurred image is induced by substrate curvature. The inset illustrates a cross-section view of the fabricated TFT.

5.3   Results and Discussions

Fig. 5.2 shows the fabricated TFT and metal interconnect lines over the transition area between curved and flat surface to the contact pads placed on a flat surface. It was initially found that edge-bead is formed due to large film inhomogeneity of spin-coated resist over the transition area, which was responsible for the distortion of structures and additional connections between lines. The edge-bead formation becomes worse for the substrate with a larger curvature due to the enhanced *FOV* and smaller *ROC*. To circumvent this issue, we adopted local-multiple LWL exposure method proposed in chapter 4; the transition area where the edge-bead formed was exposed three times. This approach allows us to successfully fabricate the metal interconnect lines without any shorts or distortion (Fig. 5.2(a)).

We measured at room temperature the transfer and output characteristics of the TFT fabricated on a spherical surface for various drain voltages (V_{DS}) and gate voltages (V_{GS}), respectively (Fig. 5.3). The maximum slope method [7] was used to extract threshold voltage (V_{th}) and field-effect mobility (μ_{FE}). OFF-current (I_{OFF}) was extracted at $V_{GS} = -5$ V, and subthreshold slope (*S*) was calculated from an inverse value of the steepest slope in an I_{DS}-V_{GS} semi-log plot. The extracted device electrical parameters are summarized in Table 5.1, and are acceptable for pixel switch applications in active-matrix liquid crystal displays (AM-LCDs), passive pixel sensor arrays, and analog circuits.
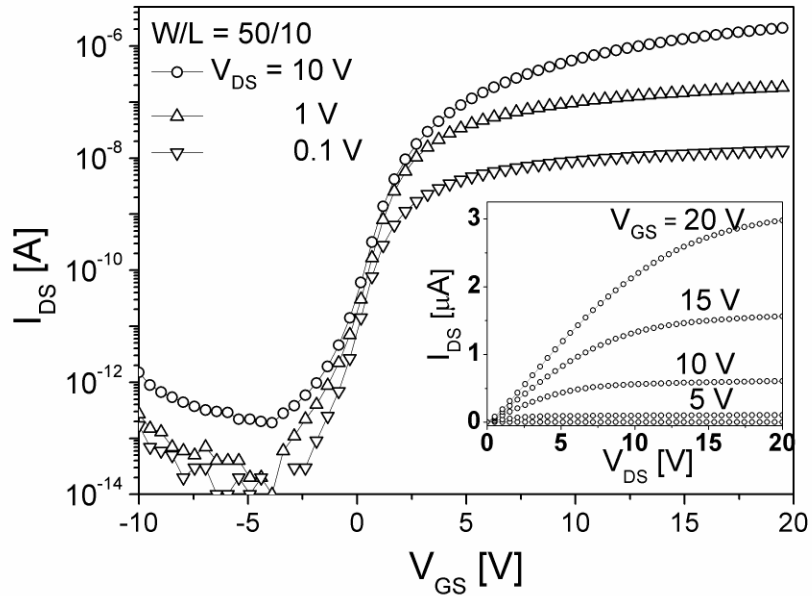
Figure 5.3 Transfer and output characteristics of the fabricated a-Si:H TFT ($W/L = 50/10$) for various V_{DS} (= 0.1 V, 1 V, and 10 V) and V_{GS} =(0 V, 5 V, 10 V, 15 V, 20 V), respectively.

Parameters	$V_{DS} = 0.1$ V	$V_{DS} = 10$ V
Threshold voltage (V_{th}) [V]	1.31	1.39
Sub-threshold slope (S) [V/dec]	0.70	0.75
Field-effect mobility (μ_{FE}) [cm2/Vs]	0.16	0.21
Off current (I_{OFF}) at V_{GS} = -5 V [A]	2×10^{-14}	2.2×10^{-13}
ON/OFF current ratio	2×10^{5}	5.4×10^{6}

Table 5.1 Extracted electrical parameters of a-Si:H TFT ($W/L = 50/10$) fabricated on a spherical surface

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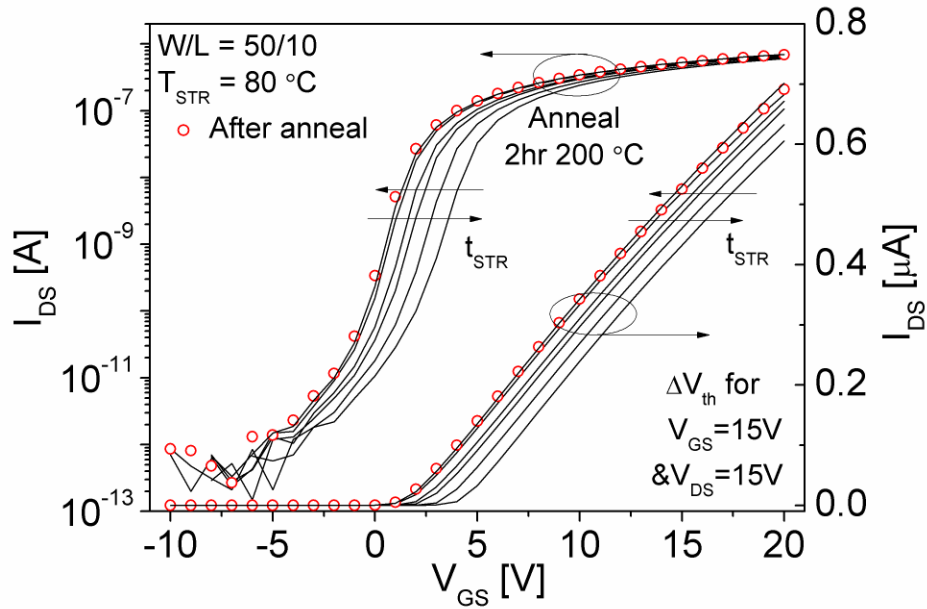
Figure 5.4 Evolution of the transfer characteristics of the a-Si:H TFT fabricated on a spherical surface for BTS (V_{GS} = 15 V and V_{DS} = 15 V) and its recovery to the initial state after thermal annealing.

Fig. 5.4 shows changes of the $I_{DS} - V_{GS}$ characteristics with t_{STR} for BTS condition of V_{GS} = 15 V and V_{DS} = 15 V at 80 °C. ΔV_{th} as a function of t_{STR} for various V_{DS} bias during the BTS experiment is shown in Fig. 5.5. The BTS induced ΔV_{th} of the TFT fabricated on a spherical surface can be described by the well known stretched-exponential equation [8]

$$\left| \Delta V_{th} \right| = \left| V_{GS} - V_{th\_i} \right| \left\{ 1 - \exp\left[-\left(\frac{t_{STR}}{\tau} \right)^{\beta} \right] \right\}, \tag{5.2}$$

where V_{th_i} is a initial threshold voltage of each BTS experiment, τ is a characteristic time constant, and β is the stretched-exponential exponent. For a limited stress time of 10^4 sec, eq. (5.2) can be simplified as

$$\left| \Delta V_{th} \left(t_{STR} \right) \right| \cong \left| V_{GS} - V_{th\_i} \right| \tau^{-\beta} t_{STR}{}^{\beta}. \qquad (5.3)$$

This power-law dependence on t_{STR} can be observed in Fig. 5.5 where the extracted β for each V_{DS} is summarized as well; no significant variation of β (< 9 %) was observed, indicating that the power-law time dependence of ΔV_{th} on t_{STR} is similar regardless of the V_{DS} bias stress condition.
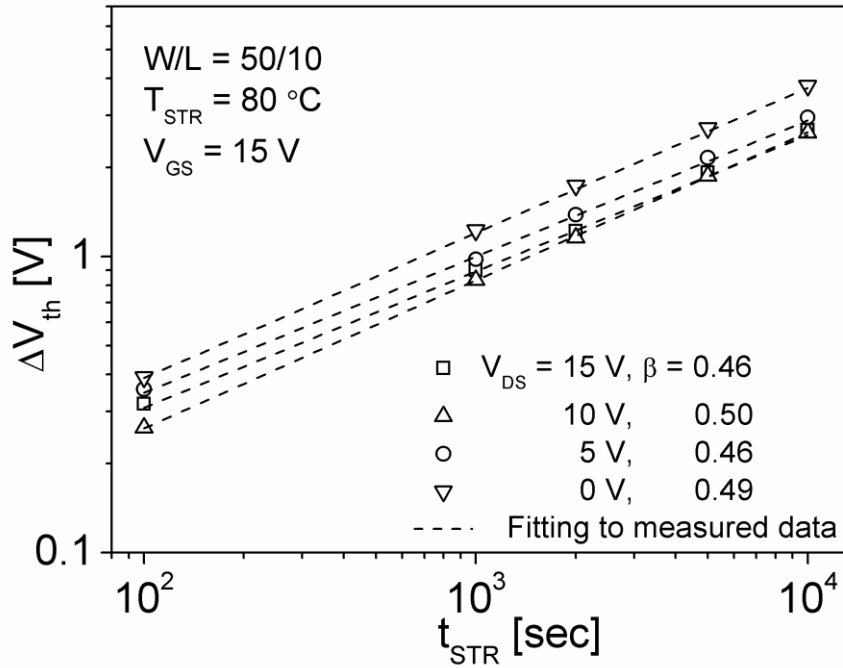
Figure 5.5 Threshold voltage shift (ΔV_{th}) as a function of the stress time (t_{STR}) for different stress bias of V_{DS} bias; V_{GS} was kept to 15 V. The stretched-exponential exponent (β) is extracted and summarized for each V_{DS} bias. Dashed lines are the linear fit to the experimental data.
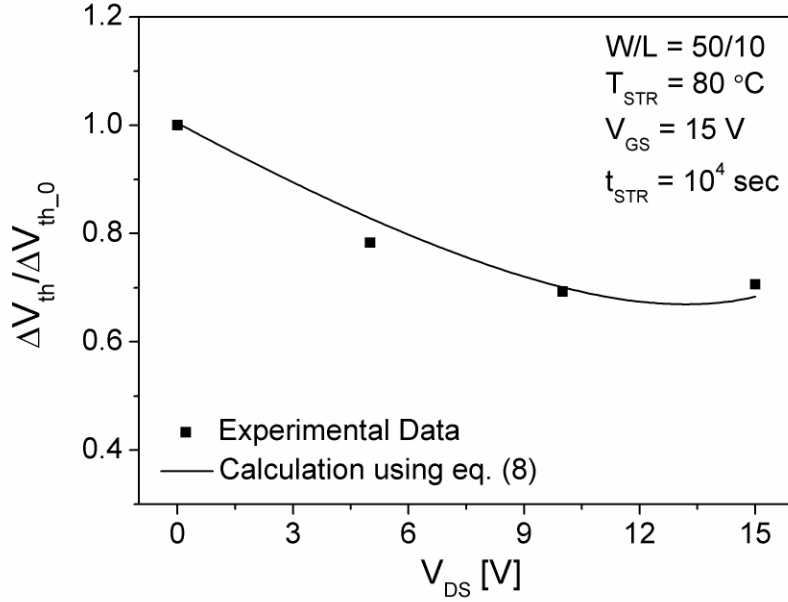
Figure 5.6 ΔV_{th} normalized to its maximum value (ΔV_{th_0} at $V_{DS} = 0$ V) as a function of V_{DS} bias; experimental data from Fig. 5.5 at $t_{STR} = 10^4$ sec. The solid line shows the calculation result of eq. (8) for the same V_{DS} range (0 V ~ 15 V) using MATLAB.

ΔV_{th} normalized to its maximum value (ΔV_{th_0}) at $V_{DS} = 0$ V as a function of V_{DS} bias is plotted in Fig. 5.6; the larger V_{DS} bias is, the smaller ΔV_{th} is observed. This can be explained as follows: in general, ΔV_{th} is induced by a combination of charge trapping and/or defect state creation [8]. If defect creation mechanism dominates, ΔV_{th} is proportional to the number of charges in the channel [9]. Considering the observed V_{DS} dependence of ΔV_{th}, eq. (5.3) can be modified to [10]

$$\left| \Delta V_{th}\left(t_{STR}\right) \right| = \left(\frac{Q_G}{Q_{G0}} \right) \left| V_{GS} - V_{th\_i} \right| \tau^{-\beta} t_{STR}^{\ \beta}, \tag{5.4}$$

where Q_{G0} is the maximum channel charge in a linear regime and can be expressed as

$$Q_{G0} = C_G \cdot W \cdot L \cdot \left(V_{GS} - V_{th\_i} \right), \tag{5.5}$$

and Q_G is the channel charge depending on V_{DS} bias and can be written as

$$Q_G = \frac{2}{3} C_G \cdot W \cdot L \cdot \frac{\left(V_{GS} - V_{th\_i} \right)^3 - \left(V_{GD} - V_{th\_i} \right)^3}{\left(V_{GS} - V_{th\_i} \right)^2 - \left(V_{GD} - V_{th\_i} \right)^2}, \quad V_{GD} = V_{GS} - V_{DS}. \tag{5.6}$$

The larger V_{DS} bias results in a higher electric field at the drain electrode, depleting more charges in the channel near the drain (i.e. smaller Q_G) and consequently inducing lower ΔV_{th}. To better describe the dependence of ΔV_{th} on V_{DS} bias, we compared the experimental data with calculated values in Fig. 5.6. By substituting eq. (5.5) and (5.6) into eq. (5.4), ΔV_{th} can be written as

$$\left| \Delta V_{th} \left(t_{STR} \right) \right| = \frac{2}{3} \left(V_{GS} - V_{th\_i} \right)^{-1} \frac{\left(V_{GS} - V_{th\_i} \right)^3 - \left(V_{GS} - V_{DS} - V_{th\_i} \right)^3}{\left(V_{GS} - V_{th\_i} \right)^2 - \left(V_{GS} - V_{DS} - V_{th\_i} \right)^2} \left| V_{GS} - V_{th\_i} \right| \tau^{-\beta} t_{STR}^{\ \beta}.$$

$$\tag{5.7}$$

After inserting the extracted parameters and the BTS experiment conditions into eq. (5.7), we can simplify eq. (5.7) to,

$$\left| \Delta V_{th} \left(V_{DS} \right) \right| = A \frac{13.2^3 - \left(13.2 - V_{DS} \right)^3}{13.2^2 - \left(13.2 - V_{DS} \right)^2}, \quad \text{A is a constant.} \tag{5.8}$$

As shown in Fig. 5.6 where the calculation result normalized to its maximum value at $V_{DS} = 0$ V is plotted, eq. (5.8) can describe well our experimental data. For the change of V_{DS} bias from 0 V to 15 V, ΔV_{th} decreases from 1 to ~ 0.69 (~ 29 %). For $V_{DS} = 15$ V corresponding to a saturation regime we observed similar ΔV_{th} to ΔV_{th} for $V_{DS} = 10$ V, which is in agreement with the results reported by *Karim et. al* [10].
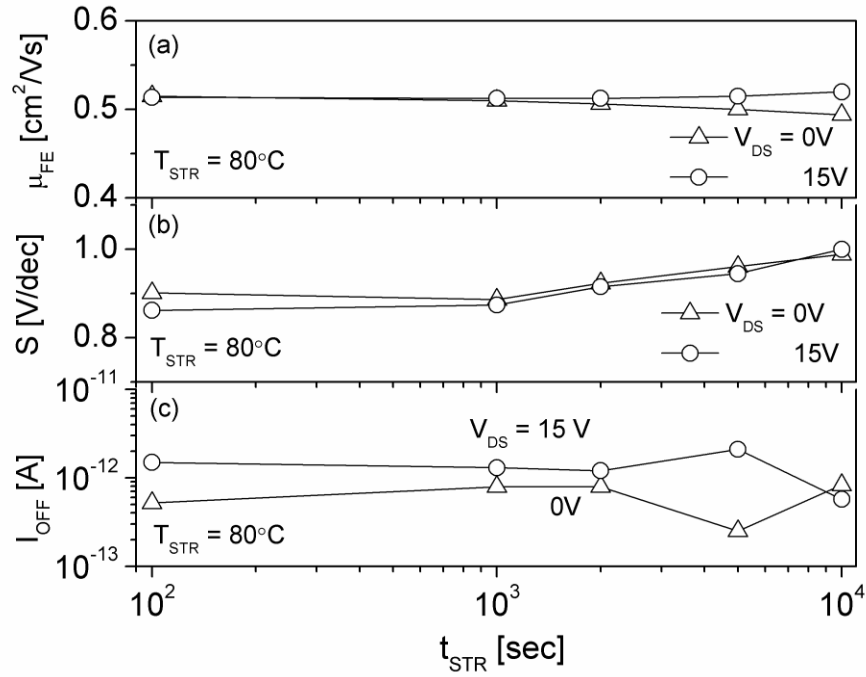
Figure 5.7 (a) μ_{FE} (b) S and (c) I_{OFF} as a function of stress time (t_{STR}) of the a-Si:H TFT (W/L = 50/10) fabricated on a spherical surface for BTS conditions of both i) V_{GS} = 15 V, V_{DS} = 0 V and ii) V_{GS} = 15 V, V_{DS} = 15 V BTS conditions. Symbols represent the measured data and lines are for aid of eye.

The evolution of other key parameters such as μ_{FE}, S, and I_{OFF} is plotted as a function of stress time (t_{STR}) in Fig. 5.7. The change of I_{OFF} is negligible, and μ_{FE} varies within ~ 4 %; S increases over t_{STR} up to ~19 % in agreement with the defect creation model. The observed results indicate that during circuit operation with or without V_{DS} bias, the a-Si:H TFTs fabricated on a spherical surface will experience some changes in electrical parameters as well as threshold voltage shift.

To compare ΔV_{th} of the a-Si:H TFT fabricated on a spherical surface with ΔV_{th} of the TFT fabricated on a flat surface, a-Si:H TFTs with the same dimension (W/L = 50/10) were fabricated on a 4″ glass wafer using the same LWL fabrication steps. The BTS experiments were performed
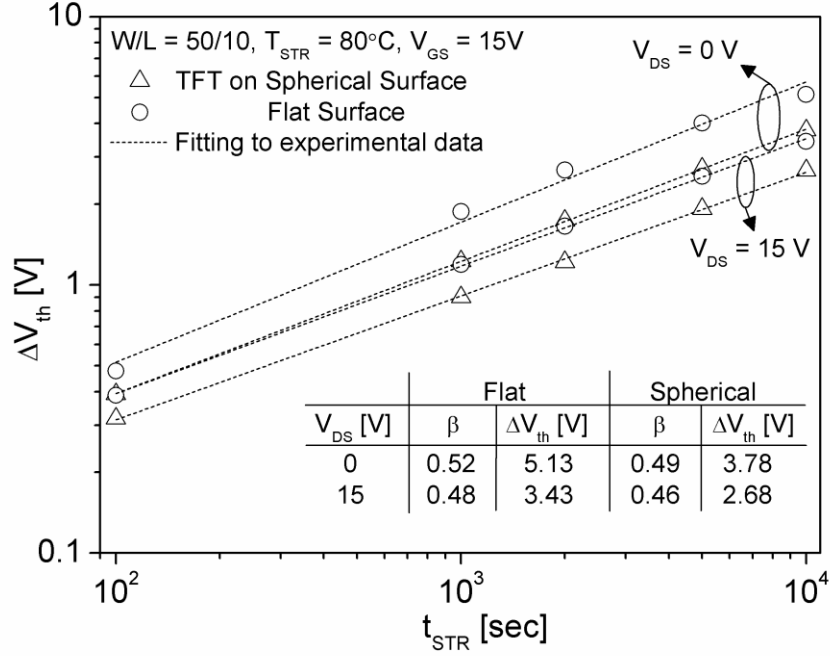
Figure 5.8 ΔV_{th} versus stress time (t_{STR}) of the a-Si:H TFTs fabricated on both flat and spherical surfaces for different BTS conditions of both i) $V_{GS} = 15$ V, $V_{DS} = 0$ V and ii) $V_{GS} = 15$ V, $V_{DS} = 15$ V. The corresponding final ΔV_{th} and stretched-exponential exponent (β) are summarized in the inset. Symbols represent the measured data, and dashed lines are the linear fit to the experimental data.

under the same conditions, and $\boldsymbol{\Delta V_{th}}$ and other parameters were extracted following the same approach as described in the experiment part (Sec. 5.2). The stretched-exponential exponent (β) in eq. (5.4) is extracted and summarized in Fig. 5.8 for both flat and spherical surfaces. A small variation (< 7 %) of the β, which is within experimental error range, is observed between the data of both surface types under different V_{DS} bias conditions. The observed ΔV_{th} of the a-Si:H TFT on a spherical surface, as shown in Fig. 5.8, is smaller than that of the a-Si:H TFT on a flat surface; for $V_{DS} = 0$ V, the difference is 1.35 V, and for $V_{DS} = 15$ V, it is 0.75 V. Although the same process steps were used for the fabrication of a-Si:H TFT on both surface types, the actual

conditions (e.g. active layer deposition and back-channel etch) might be changing due to the surface height and shape of the curved substrate. Also extraction method could introduce small error. Difference in the V_{th_i} between the flat and spherical surface was observed; for the TFT on a spherical surface, V_{th_i} is ~ 1.7 V, and for the TFT on a flat surface, it is ~ 1.33 V. The smaller ΔV_{th} of the TFT on a spherical surface can be attributed in part to a larger V_{th_i} and therefore a smaller $|V_{GS} - V_{th\_i}|$ in eq. (5.3).

5.4 Conclusion

In this chapter, we describe the electrical performance as well as the threshold voltage instability under the prolonged BTS conditions of the a-Si:H TFT fabricated on a spherical surface using LWL. We demonstrated that it is possible to fabricate the metal interconnect lines over the transition area between curved and flat surfaces of a single substrate allowing for fabrication of both high density TFT pixel arrays on the curved area and contact pads for interconnects on the flat area. The a-Si:H TFT fabricated on a spherical surface shows ΔV_{th} that is comparable to the devices fabricated on a flat surface. The extracted electrical parameters and comparable ΔV_{th} ensure the a-Si:H TFT fabricated by LWL method can be used as pixel switches in AM-LCDs and passive pixel image sensor arrays, and analog circuits on a non-planar or spherical surface.

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Chapter 6

Maskless processing of a-Si:H TFT Passive Pixel Sensors on a Curved Surface

6.1 Introduction

Complementary metal oxide semiconductor (CMOS) image sensor based on the active pixel sensor (APS) architecture is used in mobile-imaging, digital and video cameras. They provide a high speed, wide dynamic range and low power-consumption [1]. For large area applications such as security scanning and medical imaging, the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) flat panel imager based on passive pixel sensor (PPS) concept are used [2-4]. So far, all current state-of-the-art image sensor technology has been developed on flat surfaces. Recently, due to the unique advantages of the hemispherical image sensor such as wide field of view (*FOV*) and low aberrations with less optical and mechanical components in the system [5], various strategies have been proposed to implement optoelectronic devices on non-planar surfaces. They are crucial to realize imaging system on a hemispherical surface [6-13]. Although all the proposed methods have demonstrated feasibility and a working hemispherical sensor [6], they are not adequate to realize active-matrix high resolution pixel-arrays. These strategies are limited by the lack of scaling capability [6, 9, 10, 11], strain by deformation [7, 8] and a poor level-to-level alignment accuracy [12, 13]. As an alternative to circumvent these limitations, a direct fabrication method using optical lithography has been considered [6]. In the past the maskless laser-write lithography (LWL) system was used to fabricate the micro-optical elements

on both concave and convex glass lenses at a single-mask level [14, 15]. In this chapter, we demonstrate the feasibility of using the Maskless LWL with level-to-level alignment capability to fabricate a high performance a-Si:H TFT PPS on a curved surface. We then describe the electrical performance and stability of the fabricated PPS circuits. SPICE model is developed to perform simulation and compare simulated data with experimental results.

6.2   Passive Pixel Sensor and its Operation

Passive pixel sensor consists of a photodiode, storage capacitor and switching TFT as shown in Figure 6.1. There are three operation modes for PPS (*integration, readout/reset*), and each operation mode is described below with characteristic functions.

a) *Integration* mode: photo-induced charges accumulated on pixel capacitance and switching TFT is OFF.

b) *Readout* mode: switching TFT is ON, and the accumulated charges are transferred from pixel capacitance to the external readout circuit.

c) *Reset mode*: pixel capacitance is reset to an initial value prior to integration mode.
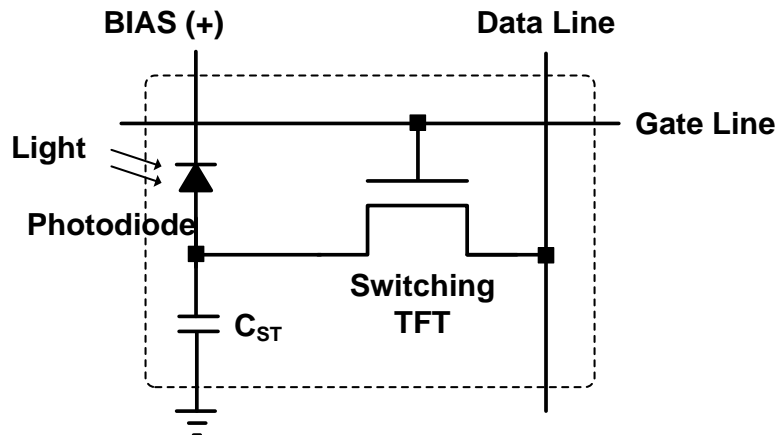
Figure 6.1 Schematic of passive pixel sensor circuit
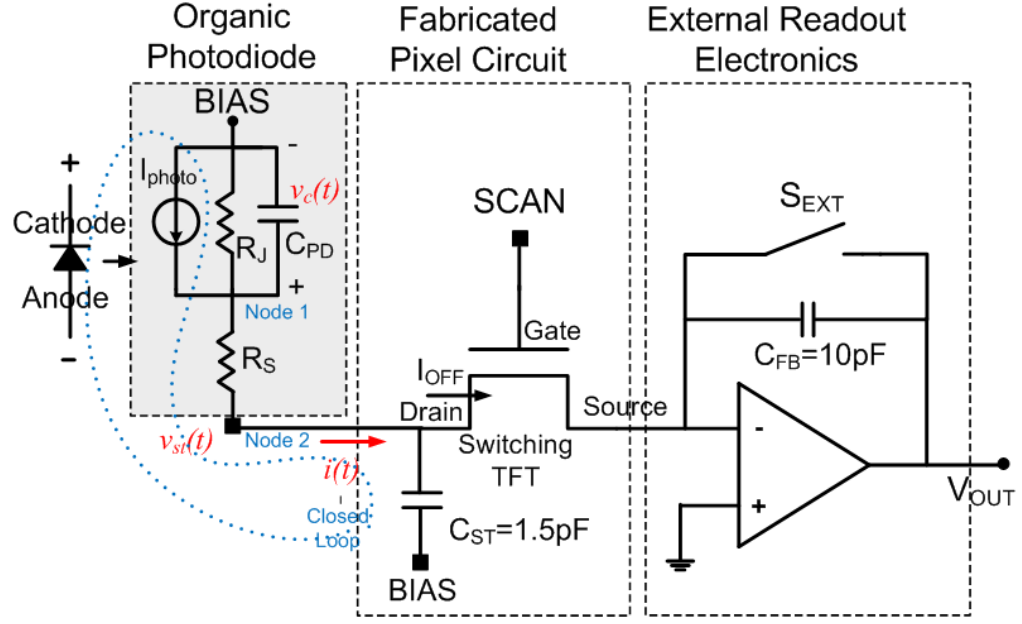
Figure 6.2 The circuit diagram of PPS connected to the external charge amplifier. The gray box indicates the organic photodiode which is not integrated in this experiment.

PPS operates in two steps since readout and reset modes operate concurrently. The equivalent circuit diagram of organic photodiode (OPD) [16] is shown in Figure 6.2. During *integration* mode, the switching TFT (SCAN) is OFF, and light-modulated current from the OPD is integrated over C_{PIXEL} during the signal integration time (T_{INT}). The pixel capacitance (C_{PIXEL}), which is the sum of photodiode capacitance (C_{PD}), storage capacitance (C_{ST}) and parasitic gate-drain capacitance of a-Si:H TFT (C_{GD}). Using basic circuit analysis for the closed loop and node 1 and 2, we can derive voltage change, *Vst(t)* at node 2 as follows:

$$-v_c(t) + i(t)R_S + v_{st}(t) = 0, \tag{6.1}$$

$$-C_{PD}\frac{dv_c}{dt} - \frac{v_c(t)}{R_J} + I_{ph} = i(t), \tag{6.2}$$

$$i(t) = C_{ST}\frac{dv_{st}}{dt} + I_{OFF}, \tag{6.3}$$

where $I_{photo} = I_{ph}$, and I_{OFF} is TFT's dark leakage current. Eq. (6.1) is derived from mesh analysis of the closed loop, and Eq. (6.2) and (6.3) are from nodal analysis for node1 and 2, respectively. By substituting Eq. (6.3) into Eq. (6.1) then plugging the result into Eq. (6.2), we get the following equation:

$$a\frac{d^2v_{st}}{dt^2} + b\frac{dv_{st}}{dt} + cv_{st}(t) + d = 0, \tag{6.4}$$

$$where \ a = C_{PD}C_{ST}R_S, \ b = C_{PD} + \frac{R_S C_{ST}}{R_J} + C_{ST}, \ c = \frac{1}{R_J}, \ d = \frac{R_S}{R_J}I_{OFF} + I_{OFF} - I_{ph}.$$

The second order non-homogeneous differential Eq. (6.4) was solved separately for homogeneous and non-homogeneous part. The homogeneous solution was found as below:

$$v_{st\_h}(t) = Ae^{r_1 \cdot t} + Be^{r_2 \cdot t}, \tag{6.5}$$

$$where \ r_1, r_2 = \frac{-\left[C_{PD} + (R_S C_{ST}/R_J) + C_{ST}\right] \pm \sqrt{\left[C_{PD} + (R_S C_{ST}/R_J) + C_{St}\right]^2 - 4(C_{PD}C_{St}R_S)/R_J}}{2(C_{PD}C_{ST}R_S)}.$$

The r_1 and r_2 are solution of complementary function of Eq. (6.4). The A and B are constants to be determined by initial boundary conditions. Non-homogeneous solution is derived as below:

$$v_{st\_nh}(t) = R_J I_{Ph} - (R_J + R_S)I_{OFF}. \tag{6.6}$$

Finally the voltage change, *Vst(t)* within integration mode can be expressed as below:

$$v_{st}(t) = v_{st\_h}(t) + v_{st\_nh}(t) = R_J I_{Ph} - (R_J + R_S)I_{OFF} + Ae^{r_1 \cdot t} + Be^{r_2 \cdot t} \text{ for } 0 \leq t \leq T_{INT}. \tag{6.7}$$

Following the integration mode, SCAN is turned ON and the accumulated charges of the light-modulated current flow through SCAN during the read time (T_{READ}). Charge integration on feedback capacitor (C_{FB}) of external readout electronics is then conducted by home-made external readout electronics during the external integration time (T_{EXT}). At the same time, the pixel capacitance is reset to its initial state (*Readout/Reset* mode), and the pixel is ready for next charge integration. The characteristic equation of output voltage $V_{OUT}(t)$ can be derived as following. The switching TFT (SCAN) operates in linear regime, and is simply modeled by drain-source resistance (R_{ON}),

$$\mathrm{R}_{ON} = \left[\frac{W}{L} \mu_{FE} C_{OX} \left(V_{GS} - V_{th} \right) \right]^{-1}. \tag{6.8}$$

And as current keeps flowing through SCAN, *Vst(t)* during readout mode can be expressed as

$$C_{PIXEL} \frac{dv_{st}(t)}{dt} + \frac{v_{st}(t)}{R_{ON}} = 0 \rightarrow v_{st}(t) = v_{st}(T_{INT}) \cdot e^{-t/\tau_1}, \text{ where } \tau_1 = R_{ON} C_{PIXEL}. \tag{6.9}$$

Following the direction of current flow, we apply nodal analysis to the input of OP-amp and

derive the $V_{OUT}(t)$ during readout/reset mode as below,

$$\frac{v_{st}(t)}{R_{ON}} = -C_{FB} \frac{dv_{out}(t)}{dt} \tag{6.10}$$

$$\rightarrow \int_{vo}^{v} dv_{out}(t) = -\int_{0}^{t} \frac{v_{st}(t)}{R_{ON} C_{FB}} dt, \ \tau_2 = R_{ON} C_{FB}$$

$$\rightarrow v_{out}(t) = v_o + \frac{\tau_1}{\tau_2} v_{st}(T_{INT}) \left(e^{-t/\tau_1} - 1 \right)$$

$$\therefore v_{out}(t) = v_o - \frac{C_{PIXEL} \cdot v_{st}(T_{INT})}{C_{FB}} \left(1 - e^{-t/\tau_1} \right), \ v_o = v_{out}(0) \text{ for } 0 \le t \le T_{READ}. \tag{6.11}$$

We compared the analytical and simulated results for a given set of parameters, respectively:

$C_{PD} = 6$ pF, $R_J = 10$ MΩ, $I_{photo} = 0.1$ μA, $C_{ST} = 0.1$ pF, $R_S = 1$ kΩ, $C_{FB} = 6$ pF, *W/L* of TFT = 100/6

with $V_{th} = 4$ V, $T_{INT} = 250$ μS, $T_{READ} = 50$ μS, $T_{EXT} = 50$ μS. For calculated results of analytical

solutions, MATLAB was used to calculate and generate waveforms of $V_{st}(t)$ and $V_{OUT}(t)$ for a

period of operation (300 μS) as shown in Figure 6.3. We used Synopsis HSPICE and RPI a-Si

TFT model for a simulation, and Figure 6.4 shows the simulated results in comparison to the

results by MATLAB. Discrepancy between simulated and calculation results was observed

because we could not take into account all parasitic effects (e.g. resistance, capacitance) of TFT

and a switch in external readout electronics. Overall, both results show a good agreement that can

be used to understand the PPS operation.
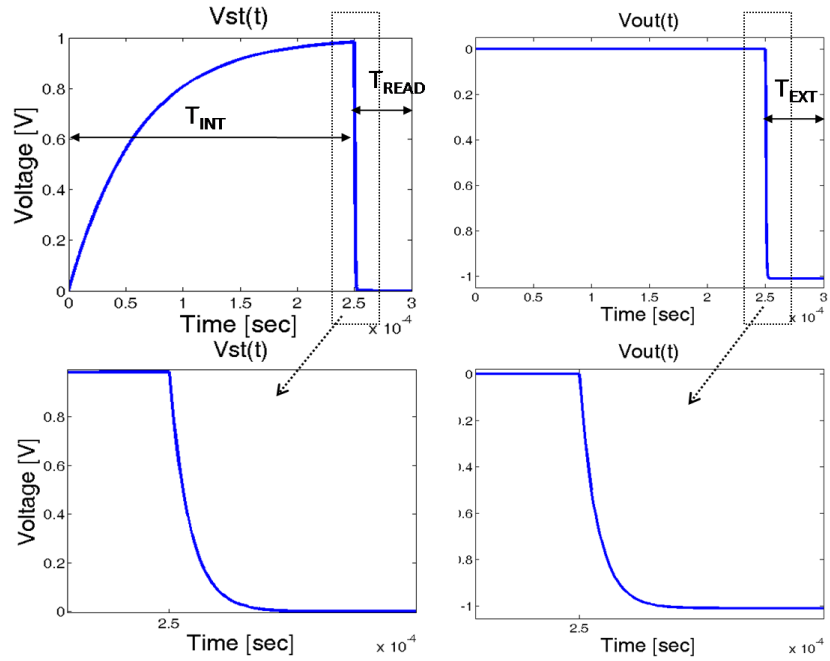
Figure 6.3 Calculation results of analytical solution by MATLAB
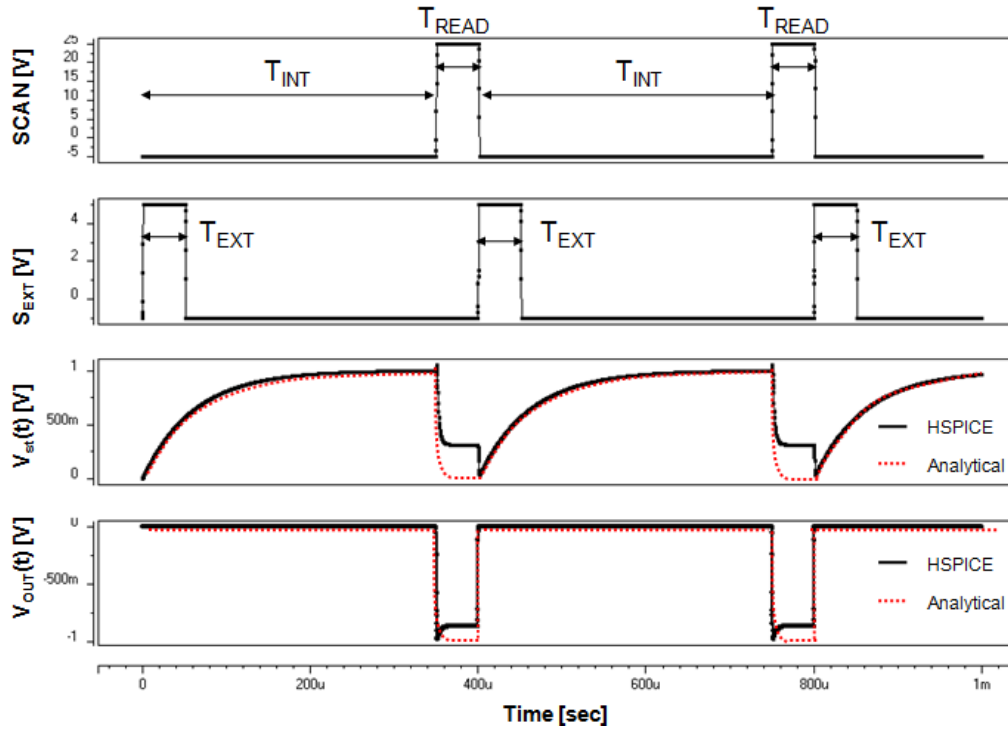
Figure 6.4 HSPICE simulation results

6.3 Fabrication of a-Si:H TFT PPS on a Curved Surface using LWL

Figure 6.5 shows a picture of the fabricated PPS circuits consisted of the bottom-gate structure a-Si:H TFT-switch (SCAN) and a storage capacitor (C_{ST}) on the concave substrate (*FOV* = 33.5°). The elongated connection lines among the TFT, capacitor and contact pads were intended for checking the uniformity of TFT circuit fabricated over the curved surface. Prior to the LWL exposure step for each level, the photoresist (AZ 1505) was spin-coated to form a uniform coating over the curved surface; the ratio of substrate-radius (0.865 cm) to radius-of-curvature (3 cm) is below 0.816, which guarantees for the spin-coated film to be in nearly homogeneous composition over the curved surface [17]. As evaluated in chapter 3, the thickness
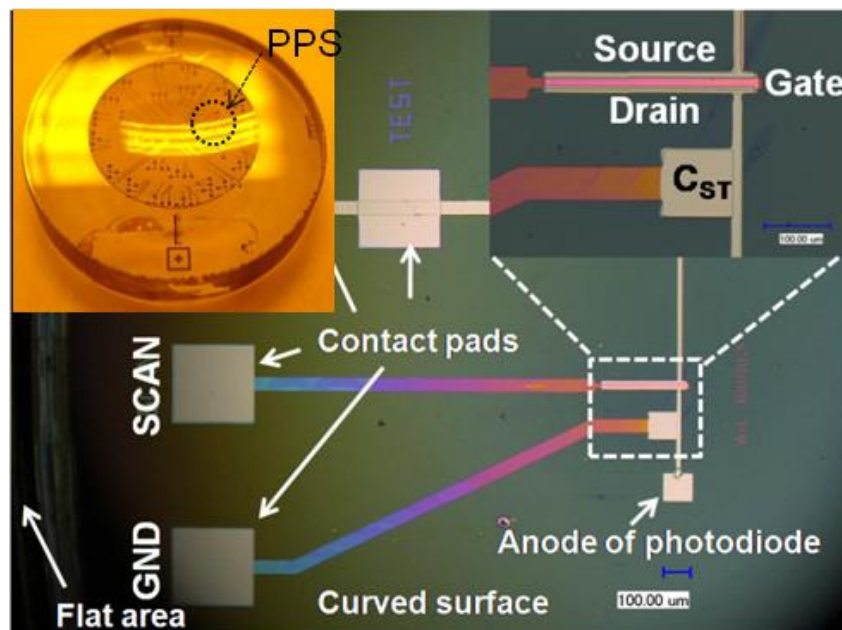
Figure 6.5 Photograph of the fabricated substrate and optical micrograph of the pixel sensor circuit at the edge of the curved surface. (Inset) Detailed micrograph of the a-Si:H TFT and C_{ST}. A dashed-circle indicates a location of the PPS studied in this chapter.

of spin-coated photoresist on a flat area (594 nm ± 20) was slightly thicker than that of a curved surface (575 nm ± 20) at 4000 rpm. This difference does not have any impact on LWL exposure conditions. However, this spin-coating method is not applicable to a curved substrate with larger *FOV*; the largest *FOV* to be spin-coated for a given radius-of-curvature of 3 cm is ~109°. For realizing hemispherical image sensor, alternative resist coating method such as spray-coat needs to be investigated. More details about the fabrication using the LWL on a curved surface can be found in chapter 4.

6.4   Experimental and Testing Set-up

Figure 6.6 shows testing set-up and schematics of PPS circuit that is electrically tested using home-made external readout electronics consisted of a Burr-Brown 102 charge amplifier with a feedback capacitor (C_{FB}) of 10 pF. Electrical measurements of the TFT were conducted and analyzed using a HP 4156 semiconductor parameter analyzer. To evaluate the electrical performance of the PPS, we used a Keithley 6221 DC/AC current source to apply test current (I_{TEST}). This current is used to mimic the light-modulated current, which will be generated from the organic photodiode (see gray box of Figure 6.2.)

The schematics of the driving waveforms are shown in the Figure 6.7. A typical frame of imaging devices is usually within 30 ~ 60 Hz. Considering a frame rate of 60 Hz and 100 x 100 pixel arrays, we set the integration time (T_{INT}) and the read time (T_{READ}) to ~16 ms and 128 µs, respectively. The switch in the external readout circuits (S_{EXT}) is open for a period of external integration time (T_{EXT}) of 160 µs; we added a 10% offset (16 µs) into the T_{EXT} to fully open the S_{EXT} before SCAN is closed so that no signal is lost. A 10% offset (16 µs) is also included into the T_{EXT} after SCAN is open to measure stable V_{OUT}.
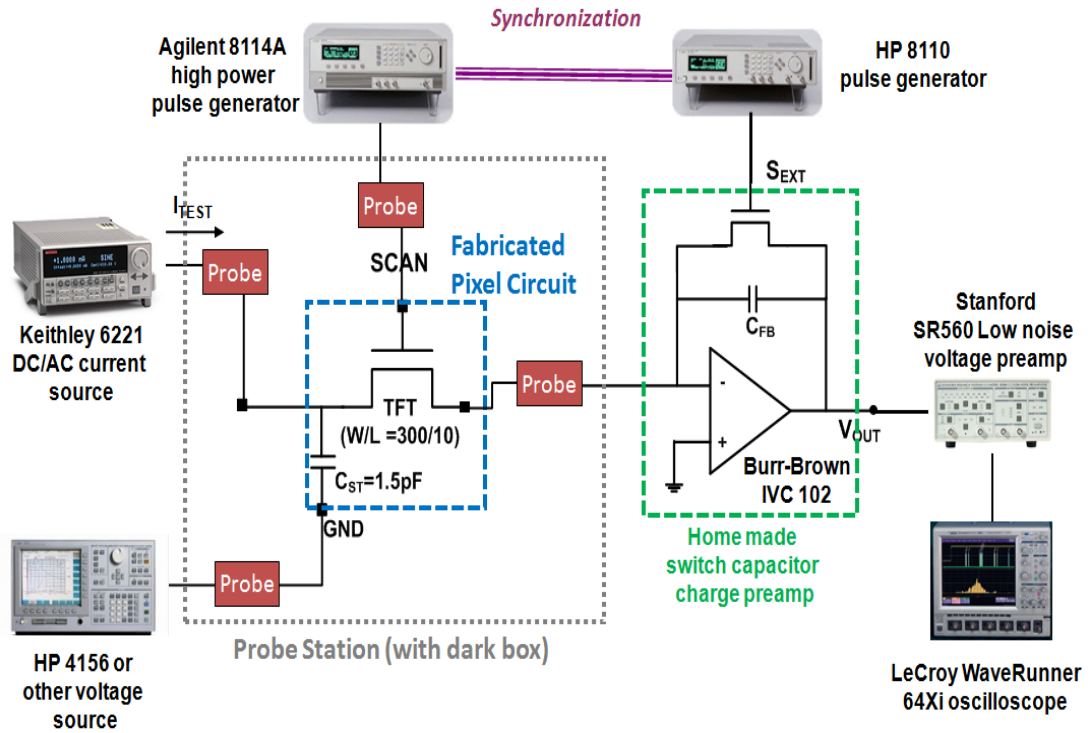
Figure 6.6 The experimental set-up for PPS AC testing.
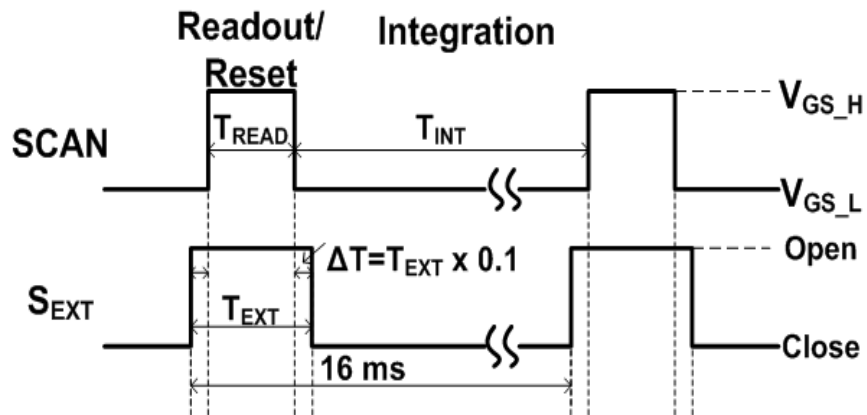
Figure 6.7 Schematic drawing of the driving waveforms to SCAN and S_{EXT}

We would like to discuss briefly about the feasibility of photodiode fabrication on the curved surface. An inorganic photodiode layer, e.g. a-Si photodiode [3], can be formed on top of the PPS circuit by PECVD and then be patterned using the same LWL method. An alternative approach, as demonstrated by *Tedde et al.* [18], is using a solution-processable organic photodetector (OPD) that will allow us to fabricate photodiode on the curved surface using spin-coat method. OPD integration enables us to achieve a high fill factor close to 100%. However, for a high resolution array processing, this continuous sensor design may bring about undesirable issues such as parasitic capacitance and lateral cross-talk between pixels [19]. The light-modulated current from the photodiode is given by the equation:

$$I_{TEST} = I_{photo} = \frac{(P_{in} \times \eta_{ext} \times e)}{hv}, \tag{6.12}$$

where e is unit charge, η_{ext} is external quantum efficiency and hv is the light photon energy. Assuming the organic photodetector is integrated on top of the PPS [18], for a range of the light intensity from 0 to 0.36 mW/cm^2 we estimated corresponding I_{TEST} (= I_{photo}) range from 0 to 2.1 nA. But we could not perform actual optical illumination of the fabricated PPS.

The charge transfer time (τ) through SCAN is given by $\tau = C_{PIXEL} \times R_{ON}$, where C_{PIXEL} is the sum of C_{GD}, C_{ST} and photodiode capacitance (C_{PD}). By integrating the organic photodiode [18] on top of 150 µm pixel pitch PPS, we estimated the C_{PD} to be about 3.8 pF for corresponding C_{PIXEL}=5.4 pF. Finally, τ is calculated to be ~ 22 µs. For 99.3% charge readout on C_{PIXEL}, five time constant of τ (~110 µs) is sufficient [20]. The calculation result shows that 100 x 100 pixel arrays with 60 Hz frame based on column-parallel readout can be realized. To realize higher resolution arrays (e.g. 1000 x 1000) with the same pixel pitch and frame rate, we need smaller R_{ON} (e.g. 0.47 MΩ) to achieve shorter τ (e.g. ~2.5 µs). So the a-Si:H active layer needs to be replaced with a thin-film channel material having higher field-effect mobility (e.g. ~10 cm^2/Vs) such as amorphous indium gallium zinc oxide (a-IGZO) [21].

6.5　Experimental Results and Discussion

6.5.1　Electrical characteristics and instability of the switching TFT

We first extracted electrical parameters of the switching TFT (*W/L*=300/10) based on 10-90% data range of the maximum drain-to-source current. Figure 6.8 shows the transfer characteristics of the switching TFT, and the extracted parameters in a linear operation regime are as follows: field effect mobility (μ_{FE}) ~ 0.11 cm^2/Vs, threshold voltage (V_{th}) ~ 5.06 V, OFF-current (I_{OFF}) at V_{GS} = -5 V ~ 0.32 pA, and subthreshold swing (*SS*) ~ 1.07 V/dec. The ON/OFF current ratio was ~10^6, and the ON-state resistance of switching TFT (R_{ON}) was calculated to be 4.1 MΩ at V_{GS} = 10 V using the following equation:

$$R_{ON} = \left[\left(\frac{W}{L} \right) \mu_{FE} C_{OX} \left(V_{GS} - V_{th} \right) \right]^{-1}, \tag{6.13}$$

where C_{OX} is gate insulator capacitance per unit area, V_{GS} is gate bias to the switching TFT. C_{GD} and C_{GS} were calculated to be 112 fF (W/L= 300/10) for an overlap of 4 µm between the gate and drain electrodes, and between the gate and source electrodes, respectively.

To accurately predict electrical performance (e.g. *dynamic range*) of the fabricated PPS on the curved surface, SPICE model of the switching TFT is required. This model is also needed for active-matrix array design. We fitted semi-empirically the measured data into LEVEL 61 RPI a-Si TFT model [22] and then extracted all needed SPICE TFT parameters. Synopsys HSPICE was used for simulation, and the comparison between measured and simulated TFT characteristics is shown in Figure 6.9. We can see that the SPICE model with appropriately extracted TFT parameters can produce well our measured device characteristics. Although the leakage current of simulation at high drain bias (V_{DS} = 10 V) deviated from the measured data by one order so

further optimization is required, it does not affect much simulated results of PPS dynamic range since the switching TFT operates usually in linear regime.
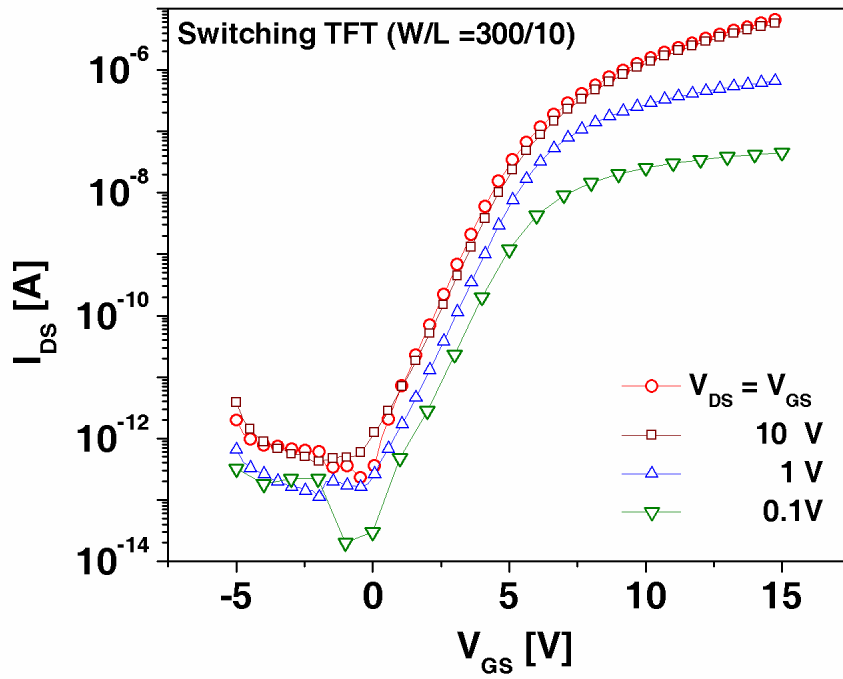
Figure 6.8 Transfer characteristics of the switching TFT for various V_{DS}
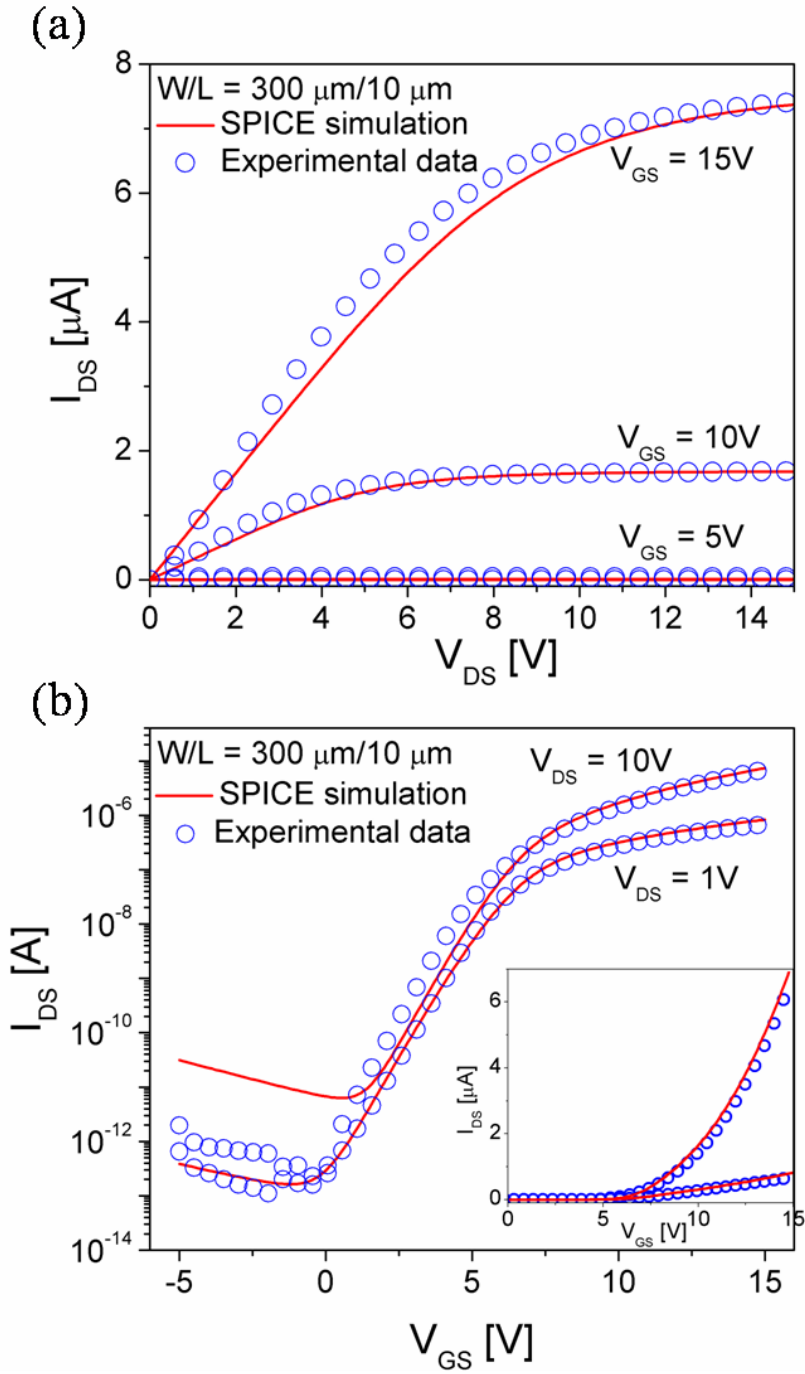
Figure 6.9 Measured and simulated (a) output and (b) transfer characteristics of the switching TFT. (Inset) transfer characteristics in linear scale.
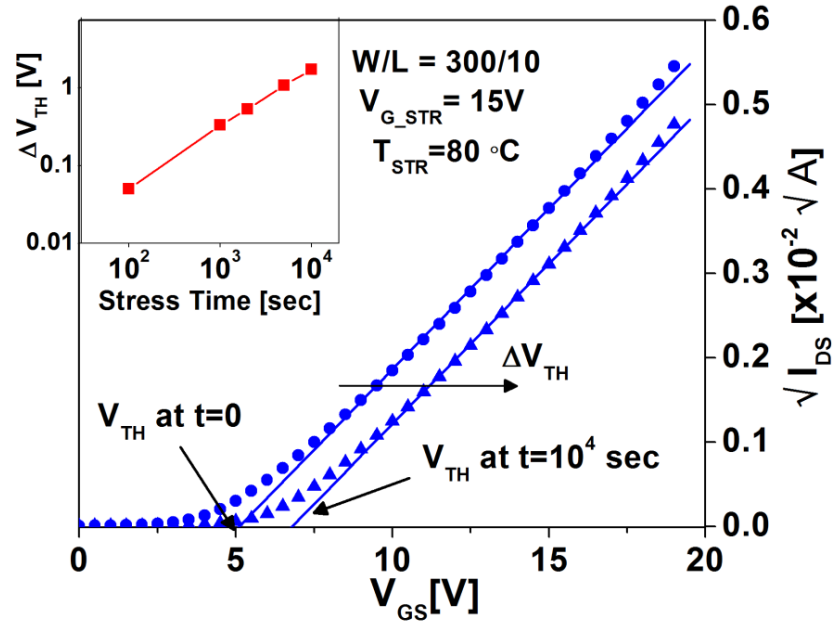
Figure 6.10 The change of TFT switch transfer characteristics at saturation operation regime for BTS (V_{G_STR} = 15V, V_{DS} =0V, T_{STR} = 80 ℃. (Inset) ΔV_{TH} as a function of stress time.

The threshold voltage shift of the switching TFT is important characteristics to be investigated since it can affect R_{ON}, charge transfer time and eventually degrade the switching capability. To evaluate threshold voltage shift of the switching TFT for a prolonged bias condition, we conducted a bias-temperature stress (BTS) experiment. During the BTS, a constant gate stress voltage (V_{G_STR} = 15 V) was applied and the drain bias was grounded to source bias. We set the stress temperature (T_{STR}) and time as 80 ℃ and 10^4 sec, respectively. All I_{DS} -V_{GS} characteristics were measured by interrupting constant bias stress for 60 sec at predetermined time steps. The threshold voltage shift (ΔV_{TH}) for the stress time was ~1.71 V (Figure 6.10). We can estimate the R_{ON} shift induced by ΔV_{TH} , based on the following equation:

$$R_{ON}\left(\Delta V_{th}\right) = \left[\left(\frac{W}{L}\right)\mu_{FE}C_{OX}\left(V_{GS} - V_{th} - \Delta V_{th}\right)\right]^{-1}. \qquad (6.14)$$

The predicted shift of R_{ON} and charge transfer time (τ) is calculated to be 6.3 MΩ and 34.02 μs, respectively. About 53% increment of both parameters makes the switching TFT insufficient to realize 100 x 100 PPS array because full transfer of the accumulated charges through the switching TFT becomes impractical of the requirement ($5\tau > T_{READ}$) discussed in the previous section 6.4. Five times of the charge transfer time ($5\tau = 170$ μs) becomes larger than readout time ($T_{READ} = 128$ μs).

6.5.2   Transient response and dynamic range of fabricated PPS

Oscilloscope traces of V_{OUT} for various I_{TEST} are shown in Figure 6.11. $I_{TEST} = 0$ nA corresponds to no light-modulated current, and V_{OUT} starts to saturate at $I_{TEST} = 1.9$ nA due to the complete discharge of C_{ST} (1.5 pF) during the readout. Furthermore, to characterize the dynamic range (DR) which quantifies sensor's ability to image scenes with the wide spatial variations in illumination [23], we evaluated the linearity of V_{OUT} in response to I_{TEST} for the range of 0.01 nA – 2.1 nA by sampling the stabilized V_{OUT} at 158 μs (Figure 6.11). The dynamic range is given by the equation:

$$Dynamic\ Range\ (DR) = 20 \times \log\left(\frac{I_{max}}{I_{min}}\right), \qquad (6.15)$$

where I_{max} is a maximum non-saturated signal and I_{min} is a minimum detectable signal. Figure 6.12 shows the saturation effect for the I_{TEST} corresponding to high light intensities. I_{max} and I_{min} were measured to be 1.9 nA and 0.02 nA, respectively, and DR was calculated to be about 40 dB for the fabricated PPS.

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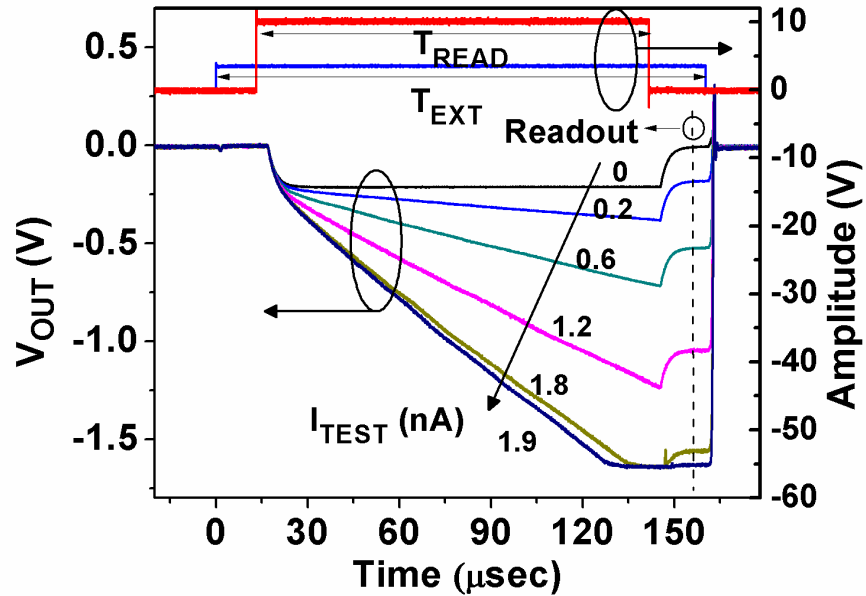
Figure 6.11 Oscilloscope traces of V_{OUT} for different I_{TEST}

6.5.3 Comparison between experimental and simulated results

Simulated result of *DR* using HSPICE is also shown in Figure 6.12; SPICE model with extracted parameters described in the previous section (6.5.1) was used for the simulation. Simulated V_{OUT} is slightly higher than measured values because an ideal Op-amp is used in the simulation and there is no current loss by flowing into the input of the Op-amp. For simulated data *DR* is calculated to be about 60 dB. The low end of V_{OUT} (I_{TEST_min}) is affected by the leakage current of SCAN (I_{OFF}, 0.32 pA) and reset noise (~1.2 pA) [23]. Since the simulation result using HSPICE does not include noises from SCAN and DC/AC current source, lower I_{TEST} (~5 pA) can be detected. The high end of V_{OUT} (I_{TEST_max}) is limited by C_{PIXEL} for given T_{INT} [23]. Designed capacitances of C_{ST} and C_{GD} constituting C_{PIXEL} are subject to insulator and active layer thickness control. Consequently, the thickness variation of the layers over the curved surface after plasma-

enhanced chemical vapor deposition ($\pm$ 11%) and reactive-ion etching ($\pm$ 12%) presented in chapter 3 can cause capacitance discrepancies that affects the amount of the accumulated charges on C_{PIXEL} and drain voltage (V_{DS}) during integration ($V_{DS} = Q_{PIXEL}/C_{PIXEL}$). V_{DS} should be less than V_{GS_H} -V_{th}, where V_{GS_H} is gate voltage during readout. In this experimental condition, V_{DS} for I_{TEST_max} is calculated to be ~ 5.6 V, which is less than V_{GS_H} of 10 V. Thus SCAN could operate in a linear regime for both a quick readout by reducing R_{ON} and a linear behavior of drain-to-source current depending on V_{DS}. Without changing the operation regime of SCAN, larger C_{PIXEL} could increase Q_{PIXEL}, non-saturated I_{TEST} value, and the high end of *DR*.
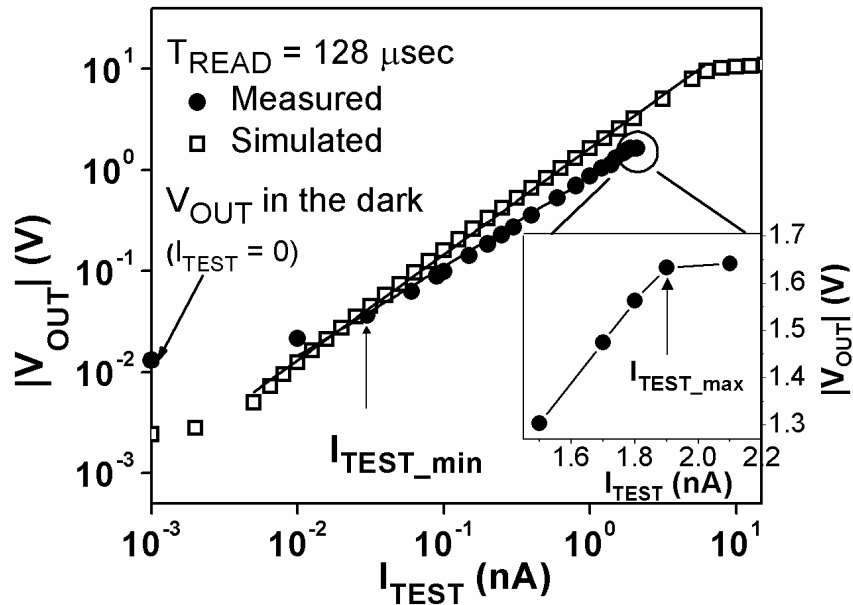
Figure 6.12 Solid circles show the linearity plot of the measured V_{OUT} vs. I_{TEST} by sampling V_{OUT} at 158μs. (Inset) Non-linearity is shown at high values of I_{TEST}. Squares show the simulated results.

A compromise between the charge transfer time and the dynamic range must be realized because C_{PIXEL} increases along with the charge transfer time. The pixel pitch and aperture ratio also need to be taken into consideration, which is a controlling factor in the size optimization of C_{PIXEL}. Basically, the larger pixel pitch is, the more space is available to C_{ST} contributing total C_{PIXEL}. For high-resolution image sensor, however, the required pixel pitch is very small so the aperture ratio needs to be maximized. The pixel aperture ratio is a ratio between the transmissive portion of a pixel and its surrounding opaque components (e.g. thin-film transistors); in our PPS, the transmissive portion corresponds to the area for C_{ST}. Therefore advanced TFT structures studied in chapter 2 can be used as alternative device structure for increasing C_{PIXEL} and consequently dynamic range (*DR*) in high-resolution active-matrix sensor array.

6.6   Conclusion

In summary, we demonstrated that LWL with a high level-to-level alignment accuracy can be used to fabricate a-Si:H TFT PPS on a curved surface. We also reported electrical performance of the fabricated PPS circuits: electrical stability, transient response and dynamic range. We developed SPICE model to perform a simulation and compare the simulated results with the experimental results. The obtained results clearly show that we can realize high resolution a-Si:H TFT active-matrix PPS; a pixel pitch of 150 µm and a dynamic range of about 40 dB were realized in this work. Further integration of the proven solution-processable organic photodiode will allow realizing a high resolution passive pixel image sensor on a curved surface.

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Chapter 7

50 µm pixel pitch 128 x 128 a-Si:H TFT PPS Imager

7.1   Introduction

In addition to flat panel displays, the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) can also be used for active-matrix flat panel imagers [1]. The passive pixel sensor (PPS) employing TFT as a pixel switch is the most simple and compact pixel architecture for imager, and has been the choice for x-ray detector [2]. This PPS architecture allows fine pixel size for a high resolution, and the finest pixel pitch reported so far was 64 µm [3]. A fill factor, which is defined by a sensor area divided by a pixel area, is another issue to be addressed to achieve a high resolution pixel array. Conventional PPS design places a photodiode next to a switching TFT and other bus lines. This isolated sensor design has a low fill factor, which is usually less than 50 % for ~ 100 µm pitch [4]. More advanced design adopted a continuous sensor layer on top of the TFT to increase the fill factor, and the effective fill factor reported was ~ 90 % [5]. Various inorganic photodiodes for a pixel and its array have been studied for the continuous sensor layer: amorphous selenium (a-Se) photoconductor [6], a-Si PIN photodiode [7], and Si photogate (CMOS process) [8].

A solution-processable organic photodiode (OPD) is an alternative and promising candidate for a large area and a low fabrication cost imager due to a relatively simple fabrication and integration process in comparison to the inorganic photodiodes [5, 9-11]. Proper selection of organic photodiode materials makes possible a large spectral response for such device [11].

Moreover, the simple fabrication process (i.e. spin-coating doctor-balding, spray-coating, and inkjet printing) makes OPD a good candidate for flexible and/or non-planar imager applications.

In this chapter, we fabricate the highest resolution 128 x 128 50 µm pitch a-Si:H TFT PPS array to be integrated with the continuous sensor layer integration to maximize a pixel fill factor. A bulk heterojunction OPD will be used as the light-sensing layer, which is deposited on top of the pixel electrode serving as a bottom electrode of the OPD. Our pixel circuit consists of fork-shaped a-Si:H TFT (W/L = 40/5) and a storage capacitor (C_{ST}, 0.1 pF); TFT operates as a switch, and a storage capacitor is added to accumulate more charges since the junction capacitance of OPD is rather small. A light shield layer is integrated in order to prevent light-induced leakage current in a-Si:H TFTs. Detailed fabrication steps including mask design and electrical characterization of the fabricated switch TFT are presented and described. Finally expected results of the OPD to be integrated and opto-electronic properties of PPS imager are elaborated.

7.2 Fabrication of 50 µm pixel pitch 128 x 128 a-Si:H TFT PPS array

Figure 7.1 shows a whole view of our mask design and a schematic of top and cross section view of the pixel architecture. Eight photo-mask process steps are designed to fabricate a complete passive pixel and bottom electrode of an organic photodiode. Table 7.1 provides detailed description of each photo-mask. Active protection (Mask #2) is defined at the intersection between gate-bias and source/drain bus line to reduce parasitic capacitance between them and to prevent electrical shorts caused by defects (e.g. pinholes) in a passivation and/or gate dielectric layer. This active protection can eventually increase array process yield. The light shield layer (Mask #6) is embedded to prevent the active island from being exposed to illuminated and ambient light. Unlike inorganic photodiode structures (e.g. thick a-Si or a-Se p-i-

n), light passing through OPD is not completely absorbed. So the illuminated and/or ambient light can penetrate into the channel region of a-Si:H TFT beneath the OPD and consequently induce leakage current. The increased leakage current reduces a dynamic range of imagers. Although the light shield layer requires additional passivation layer and via-definition, it allows leakage current to be kept lower under imager operating conditions. The complete fabrication process steps are illustrated with top and cross section views as follows. Mask #3 step is only for contact pads so it is not reflected in an enlarged view of a single pixel.
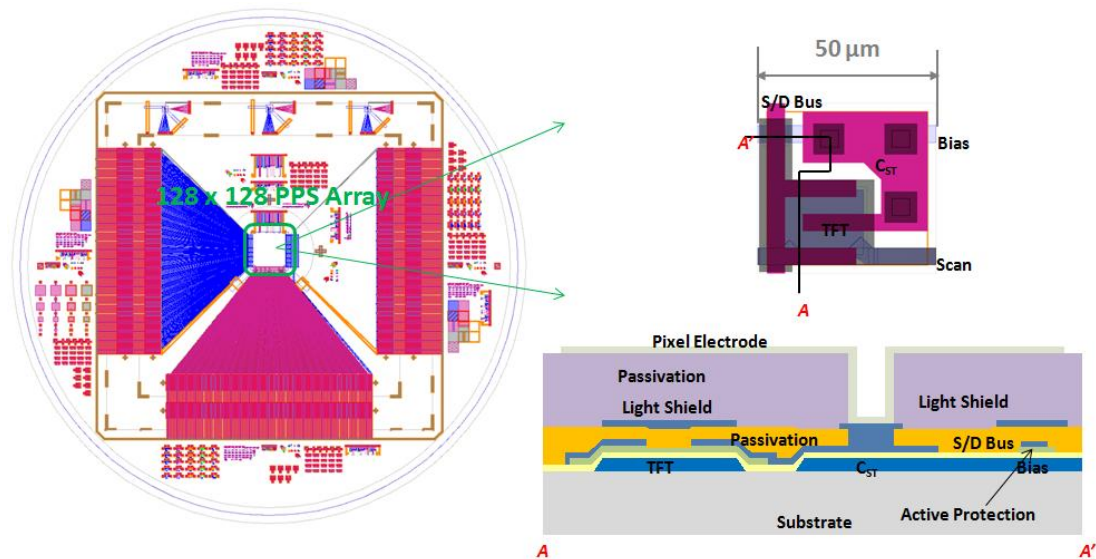
Figure 7.1 Whole view of the mask design (left) and enlarged single pixel from 128 x 128 PPS array with its cross section view (right).

Table 7.1 Descriptions of the eight photo-masks

Mask Number	Purpose	Description
#1	Gate Metallization	-TFT gate metals, and bottom electrode of C_{ST}
#2	Active Island Formation	-Tri-layer deposition and its active area formation
#3	Gate Contact Via	-Making via through gate insulator to gate level metal layer
#4	Source/Drain Metallization	-TFT source/drain metal and its bus line, and top electrode of C_{ST} -Back-channel etch performed
#5	Contact Via	- Making via through passivation layer to S/D metal
#6	Light Shield Metallization	-Light shield metal, and external ground bus line
#7	Shield Layer Via	-Making via through top passivation layer to light shield metal
#8	Pixel Electrode Patterning	-Formation of bottom electrode of OPD
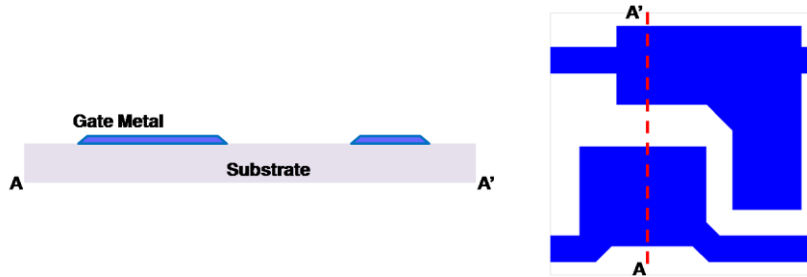
Figure 7.2 Mask #1 (Gate Metallization): Sputtered Chromium, 2000 $\overset{\circ}{A}$, and wet-etch method (CR-14) used.
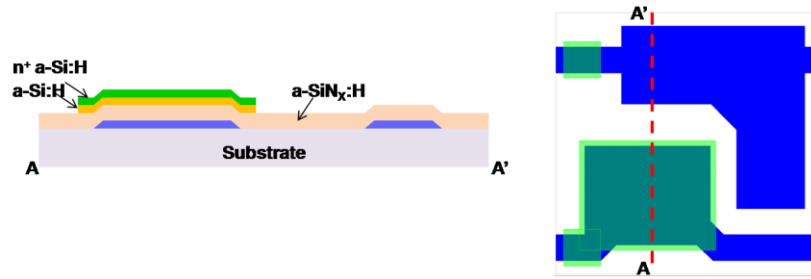
Figure 7.3 Mask #2 (Active Island Formation): Tri-layer of a-SiN$_x$ (4000 Å) / a-Si:H (1700 Å) / n$^+$ a-Si:H (700Å) by PECVD, and active island formation using RIE (SF$_6$/O$_2$).
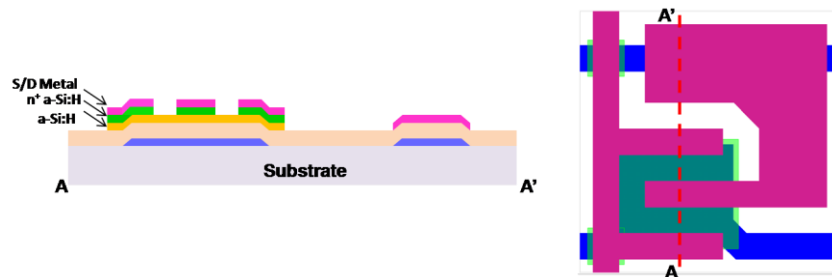
Figure 7.4 Mask #4 (Source/Drain Metallization): Sputtered Cr (2000 Å), and back-channel etch using RIE (SF$_6$/O$_2$).
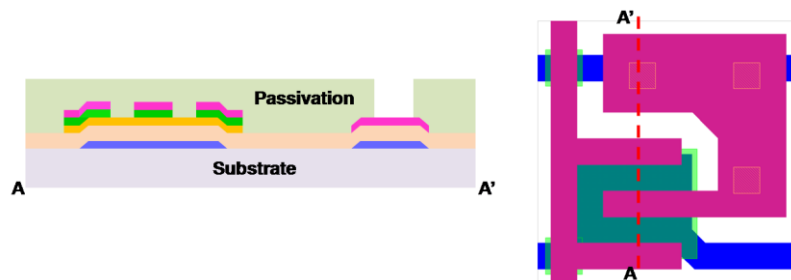
Figure 7.5 Mask #5 (Contact Via): Passivation using a-SiN$_X$:H (4000 Å) by PECVD, and via definition by RIE (CF$_4$/O$_2$).
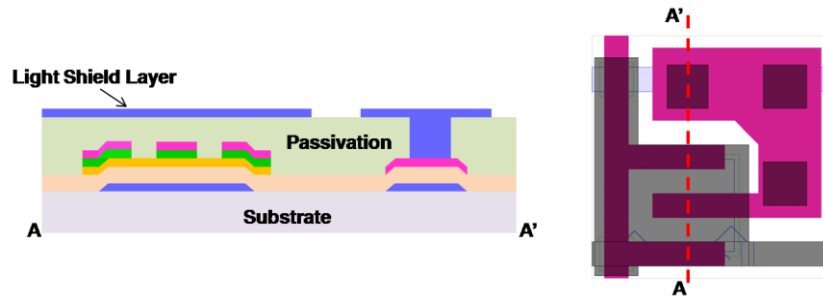
Figure 7.6 Mask #6 (Light Shield Metallization): Sputtered Cr (2000 Å), and wet-etch method (CR-14) used.
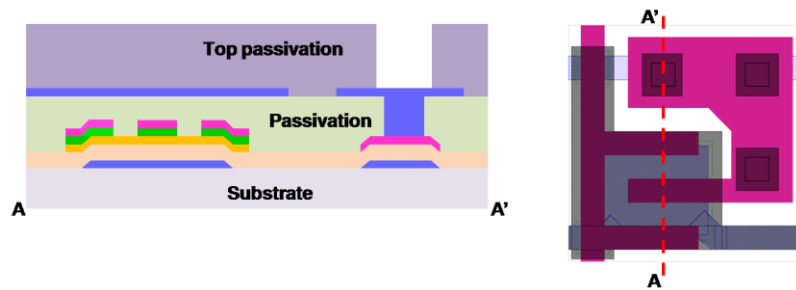
Figure 7.7 Mask #7 (Shield Layer Via): Top passivation using a-SiN$_X$:H (6000 Å) by PECVD, and via definition by RIE (CF$_4$/O$_2$) used.
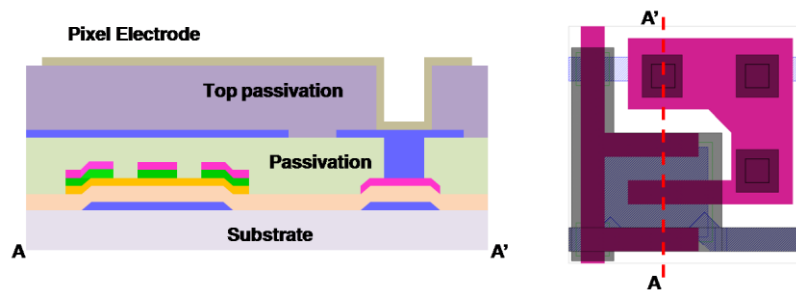
Figure 7.8 Mask #8 (Pixel Electrode Patterning): Sputtered Cr (1500 Å), and wet-etch method (CR-14) used.

Figure 7.9 (a) shows the fabricated 128x128 PPS array with 50 µm pixel pitch on a 4″ silicon wafer with 1 µm thick thermal oxide. White dash-lines indicate the position of dicing guidance lines. Enlarged photographs of the part near the PPS array and itself are shown in Figure 7.9 (b), (c). Lastly, thermal annealing was conducted at 200 ℃ for 2 hours. Afterwards we performed electrical characterization of a process-control-monitor (PCM) device, as shown in Figure 7.9 (d), using HP 4156 in dark condition. PCM devices have exactly the same pixel structure as a pixel in the PPS array. Electrical characteristics and instability of the switching a-Si:H TFT ($W/L = 40/5$) is described and discussed in a following section 7.3.
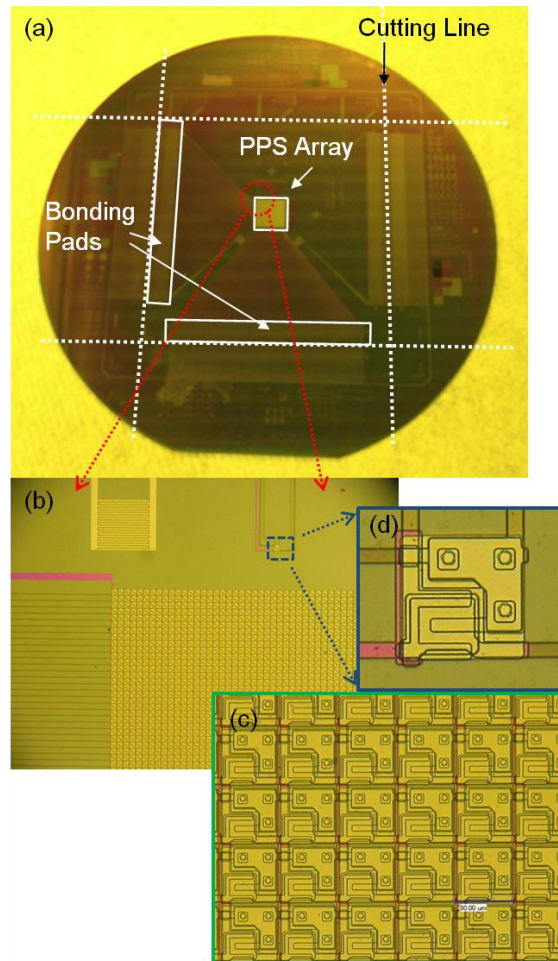
Figure 7.9 (a) Fabricated 128x128 PPS array on a 4" Silicon wafer. White dash-lines indicate the cutting line for dicing (b) Photograph from the upper left corner near the PPS array (from Red circle) (c) Enlarged photo of the part of the PPS array (d) Photograph of a PCM device.

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7.3 Electrical characteristics of the fabricated switch a-Si:H TFTs

Electrical characterization of the a-Si:H TFT (W/L = 40/5) as a pixel switch was performed as follows. As indicated in Figure 7.9 (d), we tested one of process-control-monitor (PCM) devices located close to the PPS array; PCM devices have the same architecture as the pixels in the array. Six out of nine PCMs around the array, which is about 67 %, showed adequate electrical properties. The remaining devices did not work. The dry etch optimization will be needed to increase the yield of working devices. To begin with, we measured the transfer characteristics for drain voltage (V_{DS}) of 0.1 V and 10 V as shown in Figure 7.10 (a). The comparison of electrical characteristics between grounded (GND) and floated (Float) light-shield metal layer (Shield) was studied as well; no significant difference between the two light-shield bias conditions was observed for the transfer characteristics. Detailed comparison will be presented and discussed in the following Table 7.2. Picture in the inset of Figure 7.10 (a) shows the fabricated PCM device, and its schematic is shown in Figure 7.10 (b).
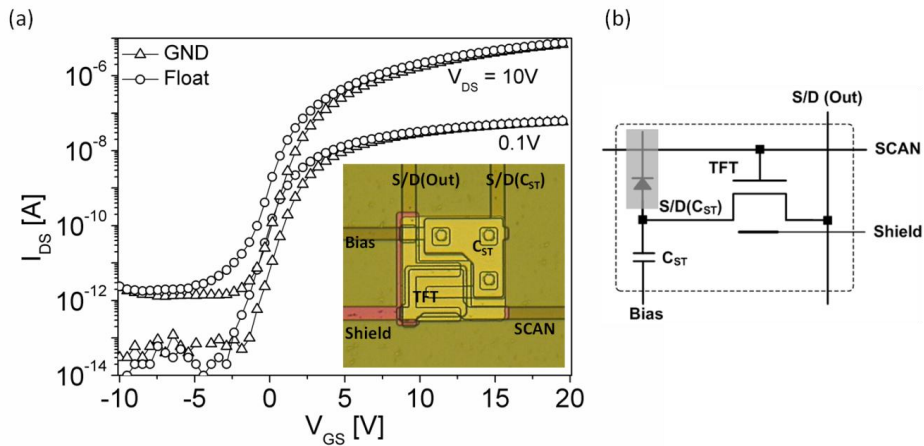
Figure 7.10 (a) Transfer characteristics of the fabricated switching TFT (W/L = 40/5) in semi-log scale. Inset shows the fabricated PCM device (b) Schematic of the PCM device; OPD indicated by gray-box is not integrated.
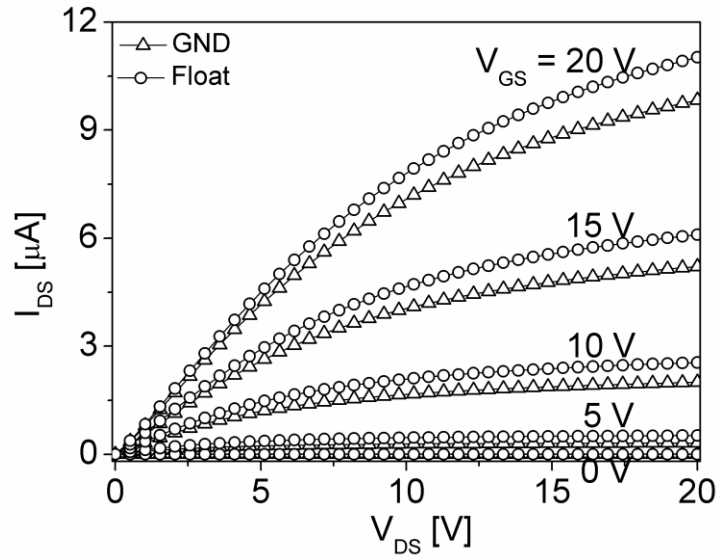
Figure 7.11 Output characteristics of the fabricated switching TFT (*W/L* = 40/5) for various V_{GS} bias.

Figure 7.11 shows the output characteristics for various gate voltages (V_{GS} = 0, 5, 10, 15, 20 V); higher I_{DS} was observed in floated light-shield layer bias condition (~10% at V_{DS} = 20 V & V_{GS} = 20 V). We calculated field-effect mobility (μ_{FE}) and threshold voltage (V_{th}) using the maximum slope method. Off-current (I_{OFF}) was extracted at V_{GS} = -5 V, and sub-threshold slope (S) was derived from the inverse of maximum slope in subthreshold region. The extracted electrical parameters for both bias conditions of light-shield layer are summarized in Table 7.2. There was not much difference in device electrical parameters between grounded (GND) and floated (Float) light-shield layer except threshold voltage (V_{th}); for both low and high V_{DS} conditions, V_{th} of grounded light-shield metal layer was higher by ~ 1 V. So the floated light-shield metal layer will be a better choice for PPS array application since a higher V_{th} induces a larger on-resistance (R_{ON}) of a switching TFT and accordingly causes increased charge transfer time (τ) as discussed in chapter 6. With a high On/Off ratio (> ~10^6) and low leakage current

(< 3 pA in both linear and saturation regime), the fabricated switching a-Si:H TFT is acceptable for being used as a pixel switch in passive pixel sensor array.

Parameters	V_{DS} = 0.1 V		V_{DS} = 10 V	
	Float	GND	Float	GND
V_{th} [V]	1.57	2.51	0.59	1.51
μ_{FE} [cm^2/V·s]	0.30	0.30	0.38	0.36
On/Off Ratio	2.44 x 10^6	6.54 x 10^5	1.82 x 10^6	2.93 x 10^6
I_{OFF} at V_{GS} = -5V [A]	2 x 10^{-14}	7 x 10^{-14}	2.56 x 10^{-12}	1.38 x 10^{-12}
S [V/dec]	0.73	0.74	0.82	0.73

Table 7.2 Extracted electrical parameters of the fabricated switching TFT (W/L = 40/5) for both grounded and floated light-shield metal layer.
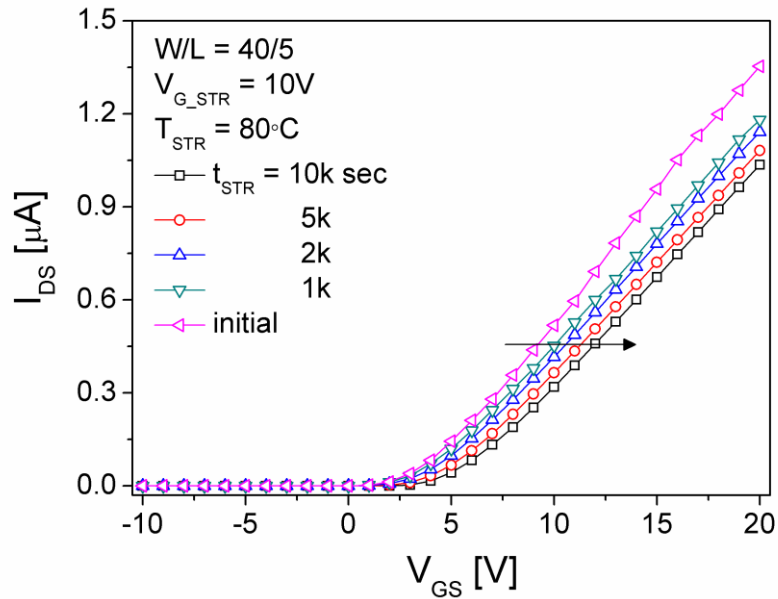
Figure 7.12 Evolution of the transfer characteristics of the fabricated switching TFT in linear operation regime for BTS (V_{G_STR} = 10 V, V_{DS} = 0 V, T_{STR} = 80 ℃).

Electrical instability (i.e. threshold voltage shift) of the fabricated switching TFT in PCM devices was evaluated by performing the bias-temperature stress (BTS) experiment as described in the previous chapters. During the BTS, a constant gate stress voltage (V_{G_STR} = 10 V) was applied and the drain bias (V_{DS}) was grounded to source bias. We set the stress temperature (T_{STR}) and time (t_{STR}) as 80 °C and 10^4 sec, respectively. All I_{DS} -V_{GS} characteristics shown in Figure 7.12 were measured in linear operation regime (V_{DS} = 1 V) by interrupting constant bias stress for 60 sec at predetermined time steps. The extraction of V_{th} and ΔV_{th} over t_{STR} was performed using the same method described in chapter 5. The threshold voltage shift (ΔV_{th}) for the stress time was about 1.18 V (from 4.60 V to 5.78 V), which is acceptable for being used as a pixel switch in the present imager.

The organic photodiode, its integration over the fabricated PPS array, and expected opto-electronic properties of the imager are discussed in the following sections. Only expected results are presented due to a delay in integration by our collaborators.

7.4 Organic photodiode structure and its expected opto-electronic properties

A bulk heterojunction organic photodiode (OPD) consists of a blend of poly-3-hexy-thiophene (P3HT) and [6, 6]-phenyl C_{61} butyric acid methylester (PCBM). The layer stack of the OPD is illustrated in Figure 7.13 (a); Cr pixel electrode as anode; PEDOT: PSS as hole conductor layer; P3HT as electron donor; PCBM as electron acceptor material; lastly semitransparent top electrode of Ca/Al as cathode of the OPD. The conversion of light into current can be explained as following [11, 12]; when an incident photon with energy larger than an energy gap between a Lowest Unoccupied Molecular Orbital (LUMO) and a Highest Occupied Molecular Orbital
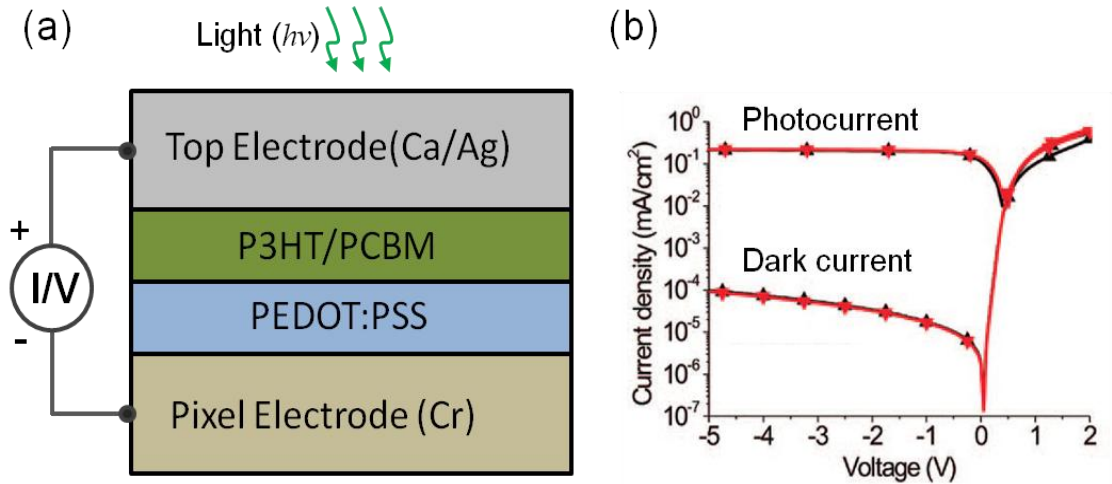
Figure 7.13 (a) The layer stack of a bulk heterojunction organic photodiode (OPD) (b) Expected I-V characteristics of OPD to be fabricated using spray-coating (adopted from [10])

(HOMO) of P3HT is absorbed, an exciton will be formed and hop between molecules to PCBM; the electron is attracted to PCBM since the LUMO of the PCBM is lower than P3HT's, and finally collected to cathode (Ca/Ag) electrode by the applied electric field; a dissociated hole from the exciton is pulled to P3HT and extracted via anode (Cr).

Figure 7.13 (b) shows the I-V characteristics of the OPD expected to be fabricated using the spray-coating method; dark current density of around 7×10^{-5} mA/cm^2 was measured at 5 V reverse bias; photocurrent was measured under illumination at a wavelength of 532nm with intensity of 780 μW/cm^2 [10]. The OPD is intended to operate at 5 V or less reverse bias at room temperature to reduce its response time. High external quantum efficiency (*EQE*) up to 71% over a large part of visible spectrum was achieved. Considering the transmission of the top electrode as a cathode is approximately 60 % at 550 nm, the high *EQE* reflects high internal quantum efficiency close to 100% for this OPD material [13].

7.5 Integration of the organic photodiode with the a-Si:H TFT PPS array

After cleaning and oxygen plasma treatment of the fabricated PPS array, the OPD will be deposited from the bottom; On top of pixel electrode of sputtered Cr (1500 Å), conductive poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT: PSS) for hole injection layer
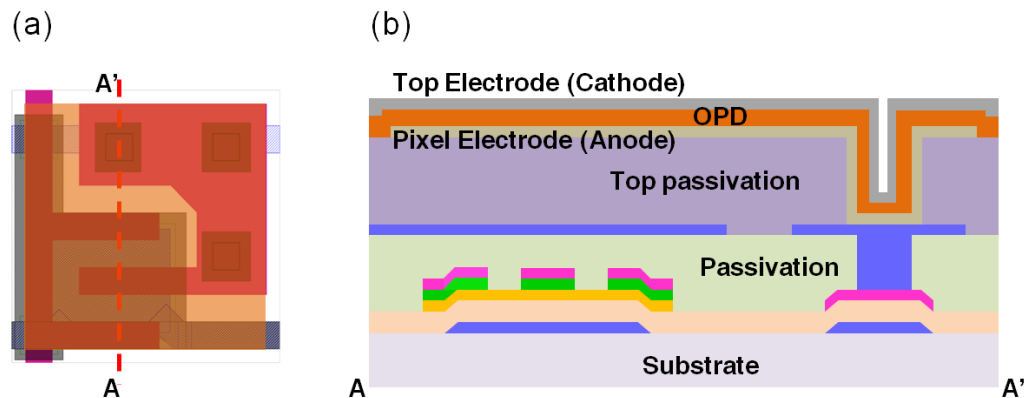
Figure 7.14 Illustration of top (a) and cross section (b) view of a pixel after OPD integration

is spray-coated with a thickness of 300 Å, and then P3HT: PCBM blend (weight percent ratio = 1: 0.75 in xylene) heterojunction layer (5000 Å) is also spray-coated on the substrate covered with a metal shadow mask to define the PPS imager area. Spray-coating is performed with a house-built setup using a computer-controlled *xy*-stage and a pneumatic spraying valve working at a compressed air pressure of 4 bar [10]. Afterward top semitransparent cathode layer of Ca/Ag (30 Å /100 Å) is thermally evaporated through a shadow mask, followed by encapsulation of the whole OPD with solvent-free epoxy resin and glass coverslips to prevent the OPD from degradation. With this encapsulation, OPD lifetime was longer than 1000 hours in a climate

chamber at 85 °C and 85 % relative humidity [13]. For the overlapped configuration shown in Figure 7.14, a fill factor for 50 µm pixel pitch PPS array is calculated to be 81 % in eq. 7.1.

$$Fill\ Factor = \frac{\text{Area of OPD Pixel Electrode}}{\text{Area of a Pixel}} = \frac{45\mu m \times 45\mu m}{50\mu m \times 50\mu m} = 81\% \qquad (7.1)$$

7.6 Expected opto-electronic properties of the fabricated 128 x 128 PPS imager

For illumination on OPD, a green light emitting diode at a wavelength of about 520 nm with a light intensity of 10 µW/cm^2 will be used. The imager size is about 6.4 x 6.4 mm^2; a picture printed on a foil will be put above the imager area, and illumination through the foil forms an image on the imager. The read-out of the imager will be performed by using in-house built *Active-Matrix Array Tester* in the following manner. By opening all switch TFTs in one row, all pixels in one row are read out simultaneously. The stored information in the pixels is read out via highly integrated chips with 128 input charge integrator and analog to digital converting (16 bit). Figure 7.15 shows a schematic of the experimental setup to be used for measurements. Following are the fabricated OPD and PPS imager's parameters to be measured with the tester.

- Dark current: as one of important figure of the OPD, it represents current flow in the absence of light. Dark current includes background-light generated photocurrent and at the junction under reverse bias.
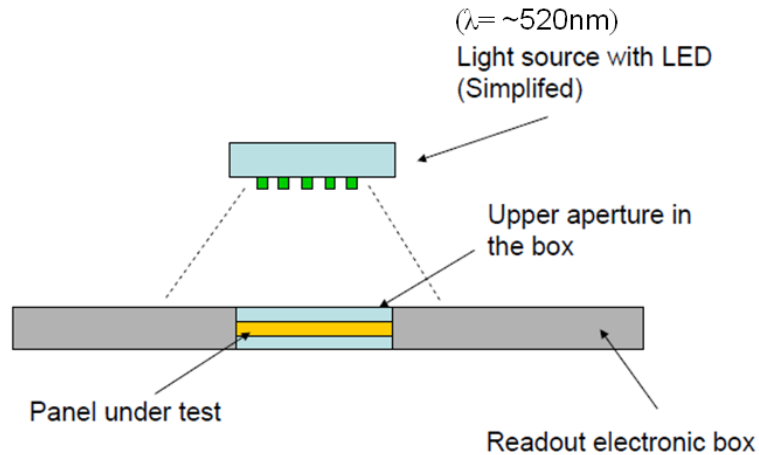
Figure 7.15 A schematic of the experimental setup for measurement.

- External quantum efficiency (*EQE*): ratio of the number of extracted charges to the number of incident photons on the OPD, resulting in the difference of reverse current between 'under illumination' and 'in the dark'.

- Spectral response: imager output per incident light energy per wavelength in the range of spectrum where the incident light's wavelength is distributed [14].

- Life time: operational life time of the OPD under elevated temperature and various light intensities.

- Conversion factor: ratio of the amount of charge collected in a pixel to a converted output in the imager; imager ouput can be a voltage or current/charge.

- Dynamic range (*DR*): as discussed in chapter 6, *DR* quantifies imager's capability of imaging scenes with the wide spatial variations in illumination.

- Crosstalk: due to the high resolution pixel pitch and non-pixelated continuous OPD layer, a high crosstalk can be introduced. Light induced charges in an area can travel to neighbor pixels and cause 'smeared' images [13].

- Image lag: signals from one frame may contribute to the next frame. Therefore a fast response of imager is necessary for capturing rapidly changing scenes. A pixel's

130

response between frames can be characterized by the image lag value, which could be caused by incomplete charge transfer from the photodiodes to the pixel circuit [15].

- Fixed pattern noise (FPN): a temporally constant lateral non-uniformity in imager due to difference among individual responsivity of array pixels.

- Noise power spectrum (NPS): defined as a Fourier transform of noisy images and providing the means of characterizing level of image noise [16].

7.7 Conclusion

In this chapter, we demonstrate the fabrication of the highest resolution 128 x 128 50 µm pitch a-Si:H TFT PPS array with the pixel structure for the continuous sensor layer integration to maximize a pixel fill factor. The fork-shaped a-Si:H TFT (W/L = 40/5) pixel switch shows promising electrical characteristics and stability under the prolonged BTS experiment. Different bias conditions applied to the light-shield layer were tested, and floated light-shield layer is preferred by providing lower V_{th} that will induce smaller on-resistance (R_{ON}) of a switching TFT and accordingly will achieve fast charge transfer time (τ). Considering that one of the biggest obstacles to fabrication of this PPS array in our laboratory was back-channel uniformity, we need to develop optimized process condition and/or reliable RIE system to extend this array process to more dense array (i.e. 1000 x 1000). The organic photodiode to be integrated is described, and its expected properties of dark current density and external quantum efficiency are speculated. Finally PPS imager's opto-electronic parameters to be measured are elaborated.

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Chapter 8
Conclusions and Future Work

8.1   Conclusions

In this dissertation, the inverted stagger fork-shaped a-Si:H TFTs were fabricated, and their asymmetric electrical characteristics were studied. To extract the electrical parameters of the TFTs, we developed asymmetric geometrical factors. The ON/OFF current ratio of fork TFT can be enhanced significantly by choosing the outer electrode as the drain, while the field-effect mobility and threshold voltage have the identical value regardless of drain bias condition. Asymmetric electrical instability of fork TFT is also attributed to the unique fork-shape. We also studied electrical stability of single and multiple HEX-TFTs; HEX-TFTs have improved electrical stability compared to the standard TFT for a similar *W/L* ratio and linear dependence of threshold voltage shift on the number of connected HEX-TFT units. The improved electrical stability of fork and HEX-TFTs is promising characteristics as a pixel switch. Both fork and HEX-TFT occupy less pixel area so they provide a larger pixel aperture ratio for given channel width. Demonstrated electrical properties and stability shows that fork and HEX-TFT structures can be a good candidate as a switching TFT for high-resolution passive pixel sensor application.

Maskless laser-write lithography (LWL) was proposed and described for fabrication of a-Si:H TFTs with 5 µm channel length, which is cost-effective and fast turn-around since it is maskless technology. The unique advantage of LWL process is the easy access to the design for modification during fabrication process because lithography is performed directly from an

electronic design. This fabrication method using LWL can be an alternative to conventional photolithography for rapid and low-volume prototyping, and be extended to process development and prototyping of large area electronics including flat panel displays, x-ray imager, and solar panels. We further described and discussed in detail the requirements of the modified LWL system to realize the process on a non-planar surface. Finally we proposed LWL system for processing a curved substrate having FOV up to 120°.

We reported on the design and fabrication methods for a-Si:H TFTs with 10 µm channel length on a spherical surface using the modified LWL system. Level-to-level alignment with high accuracy (± 2µm or less) was also demonstrated. The electrical performances of the fabricated a-Si:H TFTs were characterized over the curved surface: field-effect mobility of 0.27 cm^2/Vs, threshold voltage of 4.9 V and on/off current ratio of ~6x10^6 in a saturation regime. Due to the thickness variation of the dry-etched a-Si:H layer over the curved surface, variations in OFF-current, field-effect mobility, subthreshold swing and threshold voltage were observed. The LWL fabrication of a-Si:H TFTs is suitable to realize a high-resolution TFT pixel arrays on a curved surface for passive pixel sensor application.

Electrical characteristics and instability of the fabricated a-Si:H TFTs on a spherical surface were investigated under prolonged bias-temperature stress conditions; the spherical surface has enhanced FOV (40.5 °) and smaller radius of curvature (2.5 cm). We also demonstrated that it is possible to fabricate the metal interconnect lines over the transition area between curved and flat surfaces of a single substrate allowing for fabrication of both high density TFT pixel arrays on the curved area and contact pads for interconnects on the flat area. The a-Si:H TFT fabricated on the spherical surface shows ΔV_{th} that is comparable to the devices fabricated on a flat surface. The extracted electrical parameters and comparable ΔV_{th} ensure the a-Si:H TFT can be used as pixel switches in passive pixel image sensor arrays on a non-planar or spherical surface.

Using the LWL system together with a high level-to-level alignment accuracy, a-Si:H TFT PPS on a curved surface was fabricated, and electrical performance of the fabricated PPS circuits was discussed: electrical stability, transient response and dynamic range. We developed SPICE model to perform a simulation and compare it with the experimental results. The obtained results clearly show that we can realize a high resolution a-Si:H TFT active-matrix PPS; a pixel pitch of 150 µm and a dynamic range of about 40 dB were realized in this work. Further integration of the proven solution-processable organic photodiode will allow realizing a high resolution image sensor.

Finally, we demonstrated the fabrication of 128 x 128 50 µm pitch a-Si:H TFT PPS array with the pixel structure for the continuous sensor layer integration to maximize fill factor. The fork-shaped a-Si:H TFT (W/L= 40/5) pixel switch showed promising electrical characteristics and stability under the prolonged BTS experiment. Different bias conditions to the light-shield layer were tested, and floated light-shield layer is preferred since that gives lower V_{th} that will induce smaller on-resistance (R_{ON}) of a switching TFT and accordingly will achieve fast charge transfer time (τ). The organic photodiode to be integrated was described, and its dark current density and external quantum efficiency were speculated. Finally PPS imager's opto-electronic parameters to be measured were elaborated.

8.2   Recommendations for future work

Two directions are suggested for eventually realizing active-matrix high resolution hemispherical imager using LWL process.

- a-Si:H TFT PPS array fabrication on a spherical surface: A single pixel circuit of a-Si:H TFT PPS was successfully demonstrated on a spherical surface. High density and resolution active-matrix backplane on a spherical surface is necessary. First, further optimization of

thin-film deposition and dry etch condition is needed since a variation in such processes can cause discrepancy of electrical property between adjacent pixels. LWL process on a spherical surface for highly dense structures with fine feature should be further investigated; optimization on stitch issue and structuring over the transition area between a flat and curved surface is also inevitable. Bonding and testing methodology for active-matrix backplane on a non-planar surface should be explored.

- Organic photodiode integration on a spherical surface: Organic photodiode (OPD) has held great potential for a flexible substrate due to its simple and low temperature fabrication process. OPD, which can be spin-coated, is a good candidate for process on a spherical surface. Proper viscosity of organic blends and spin speed of a spinner should be investigated for a uniform coat over the curved area while maintaining high sensitivity. Moreover, proper shadow mask needs to be developed for selectively spin-coat on the active areas. Lastly, encapsulation method on a non-planar surface is necessary to prevent the imager from degradation.

Appendix – List of Publications

Journal Papers:

J1. H. Lee, <u>G. Yoo</u>, J.-S Yoo, and J. Kanicki, "Asymmetric electrical properties of fork a-Si:H thin-film transistor and its application to flat panel displays," *Journal of Applied Physics*, vol. 105, pp. 124522 – 124522-7, 2009.

J2. <u>G. Yoo,</u> H. Lee, D. Radtke, M. Stumpf, U. Zeitner, and J. Kanicki, "A maskless laser-write lithography processing of thin-film transistors on a hemispherical surface," *Microelectronic Engineering*, vol. 87, pp. 83 - 87, 2010.

J3. <u>G. Yoo</u>, H. Lee, and J. Kanicki, "Electrical stability of hexagonal a-Si:H TFTs," *IEEE Electron Device Letter*, vol. 31, no 1, pp. 53-55, 2010.

J4. <u>G. Yoo,</u> T.-Z. Fung, D. Radtke, M. Stumpf, U. Zeitner, and J. Kanicki, "Hemispherical Thin-Film Transistor Passive Pixel Sensors," *Sensor and Actuator A: Physical*, vol. 158, pp. 280-283, 2010.

J5. <u>G. Yoo</u>, D. Radtke, G. Baek, U. Zeitner, and J. Kanicki, "Electrical instability of the a-Si:H TFTs fabricated by maskless laser-write lithography on a spherical surface," *IEEE Transaction on Electron Device*, in press.

Conference Papers:

C1. <u>G. Yoo,</u> W. Salewski, J. Herrmann, T.-K. Won, and J. Kanicki, "A maskless laser-write lithography processing thin-film transistors," *Proc. of 29th International Display Research Conference*, pp.277 - 279, 2009.

C2. <u>G. Yoo,</u> H. Lee, and J. Kanicki, "Electrical stability of hexagonal a-Si:H TFTs," *Proc. of 29th International Display Research Conference*, pp.280 – 282, 2009.

C3. <u>G. Yoo</u>, H. Lee, and J. Kanicki, "Electrical stability of advanced a-Si:H TFT structures," *Proc. of 6th International Thin-Film Transistor Conference*, 2010. (Invited)