ZnO thin-film transistors with polycrystalline (Ba,Sr)TiO_3 gate insulators

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The electrical characteristics of ZnO thin-film transistors with high-k (Ba,Sr)TiO_3 gate dielectrics are presented. The ZnO and (Ba,Sr)TiO_3 thin films were deposited on Pt, exhibiting polycrystalline characteristics. The thin-film devices demonstrated transistor behavior over the range of 0–10 V with a stable threshold voltage of approximately 1.2 V. The field effect mobility, subthreshold slope, and on/off ratio were measured to be 2.3 $cm^2\ V^{-1}\ s^{-1}$, 0.25 V/decade, and 1.5×10^8, respectively. The measured transistor performance characteristics suggest that ZnO/(Ba,Sr)TiO_3 structures are well suited for both polycrystalline thin-film transistors for display applications and future higher performance transistors based on single crystal ZnO. © *2006 American Institute of Physics*.
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ZnO thin-film transistors (TFTs) have become the topic of much research in the recent past. Overcoming various limitations of a:Si used in many of today's display technologies, the visible transparency and low growth temperatures associated with wide-band-gap ZnO are highly attractive for display applications. Limitations of a:Si include visible light sensitivity, which reduces the aperture ratio for active matrix arrays,[1] and low channel mobility ($<1\ cm^2\ V^{-1}\ s^{-1}$), which limits drive current and device speed. Effective channel mobilities and on/off ratios of ZnO transparent TFTs grown at low temperatures have been reported in the $0.2–3\ cm^2\ V^{-1}\ s^{-1}$ range and 10^7, respectively.[2] While even higher carrier mobilities can be achieved for single crystal ZnO under higher growth temperature,[3] good ZnO TFT performance may be achieved for ZnO deposition at low temperatures via rf sputtering,[4] pulsed laser deposition,[5] and spin-coating[6] techniques. One drawback to many of the ZnO TFTs reported is large threshold and operating voltages in comparison to a:Si TFTs.[4–7] To reduce the operating voltage of a transistor, one must increase the coupling of the gate electric field to the channel layer. This is often done by reducing the gate dielectric thickness or using gate dielectric material with a higher relative permittivity[8] (high-k gate dielectric). The fact that ZnO is a semiconducting oxide provides a unique opportunity for the integration of oxide high-k gate dielectrics, where deleterious chemical interactions at the dielectric/semiconductor interface are predicted to be suppressed relative to nonoxide semiconductors. In this work, the properties of ZnO TFTs incorporating polycrystalline (Ba,Sr)TiO_3 (BST) high-k gate dielectrics are studied. The properties of BST/ZnO structures are studied for their potential in future TFT devices, as well as future electronic devices based on single crystal ZnO or perovskite oxide/ZnO heterojunctions.

ZnO and BST thin films were deposited by pulsed laser deposition (PLD). The ZnO thin films were deposited at a substrate temperature of 350 °C, oxygen partial pressure of 30 mTorr, and laser pulse energy of 350 mJ. The BST thin films were deposited at a substrate temperature of 500 °C, oxygen partial pressure of 30 mTorr, and laser pulse energy of 350 mJ. The deposition temperatures used in this work are higher than those traditionally used for TFT applications but were used primarily for the purpose of examining BST/ZnO structures where higher crystalline quality may be achieved. Thin-film transistor structures consisted of ZnO and BST thin films deposited on Pt/TiO_2/SiO_2/Si substrates as illustrated in Fig. 1. Transistor devices consisted of a uniform Pt blanket gate electrode and Ohmic source/drain contacts deposited on the ZnO layers (Fig. 1). The transistor gate length (L) and width (W) were 5 and 100 μm, respectively. The primary layer structure reported in this work employed a 60 nm ZnO layer thickness and 740 nm BST layer thickness. Devices were fabricated using metal evaporation and lift-off processes for source and drain contacts. Photolithography and wet chemical etching were used for device isolation and contact definition for the gate electrode. Separate Pt/BST/Pt test capacitors were fabricated to evaluate the dielectric properties of the BST thin films. The crystalline properties of the thin films were measured by x-ray diffraction for samples deposited separately under similar deposition conditions to the transistor layer structure. The capacitance-voltage characteristics of the BST thin films were measured using a Boonton 72 capacitance meter. The frequency dependent capacitance-voltage characteristics of Pt/BST/ZnO structures were measured using a Hewlett Packard 4284A Precision *LCR* meter. Transistor characteristics were measured using a Keithley 4200 parameter analyzer.

The crystalline characteristics of ZnO thin films deposited on glass or crystalline dielectric materials using our de-

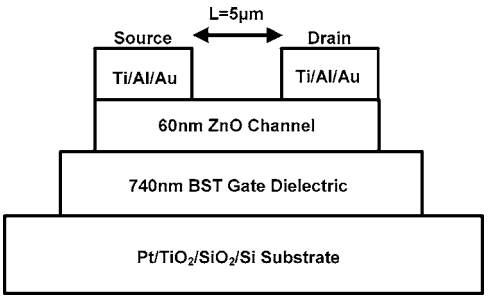

FIG. 1. Schematic illustration of the ZnO/BST thin-film transistor device under study.

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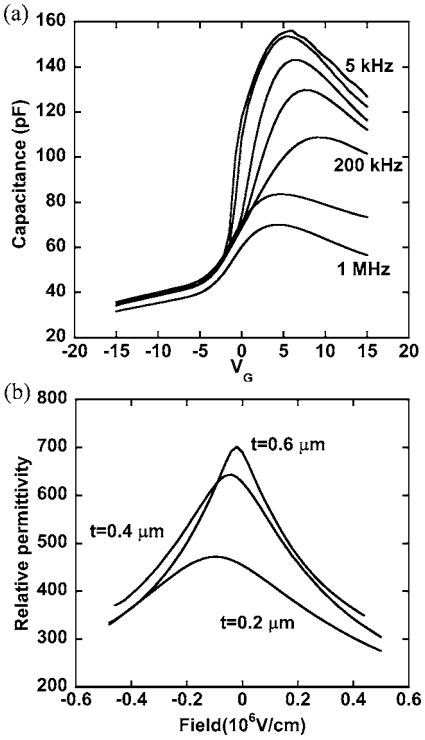

FIG. 2. Results of capacitance-voltage measurements of (a) Pt/BST/ZnO structures at variable frequency and (b) Pt/BST/ZnO structures showing relative permittivity with varying BST thickness.

scribed growth process routinely demonstrate (0002) and (0004) x-ray diffraction peaks, suggesting a strong degree of crystallinity and a preferred *c*-axis orientation. X-ray diffraction characteristics of BST thin films deposited on Pt substrates show a number of diffraction peaks resembling a powder diffraction scan, indicating some degree of crystallinity with no preferred crystalline orientation. In separate experiments we have studied the dependence of BST crystallinity on deposition temperature. We have observed that crystallinity degrades significantly for substrate temperatures below ~400 °C based on the absence of diffraction peaks.

Capacitance-voltage (*C-V*) characteristics of a representative Pt/BST/ZnO structure are shown in Fig. 2(a). The *C-V* data show a clear metal-insulator-semiconductor characteristic with a transition between depletion and accumulation in the ZnO layer occurring in the bias range between 0 and 5 V. There is a clear increase in the maximum capacitance for decreasing measurement frequency. We believe that this frequency dependence may be a result of traps at the BST/ZnO interface and/or defects within the BST where charge density is reduced at higher frequency due to a slow carrier trapping and emission process. For large negative bias, there is no clear surface inversion down to −15 V. We believe that the lack of surface inversion is also due to defects at the BST/ZnO interface. For positive bias beyond 5 V, the capacitance is observed to decrease. The decreased capacitance at increasing forward bias is not typical for a metal-insulator-semiconductor structure and may be attributed to unique properties of the BST material described in the following. The composition of BST used in this study was $Ba_{0.5}Sr_{0.5}TiO_3$, with a Curie temperature below room temperature and expected paraelectric behavior. The electric field dependence of the dielectric constant of paraelectric BST thin films may be described by the Landau theory.[9] The

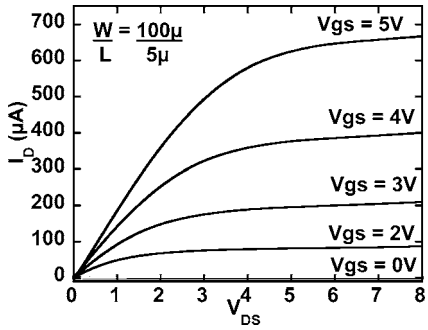

FIG. 3. Output characteristics (I_D-V_{DS}) of a representative ZnO/BST thin-film transistor.

measured electric field dependence of the relative permittivity of several BST thin films deposited under similar conditions with varying thickness is shown in Fig. 2(b). A clear variation in dielectric constant is observed with respect to electric field. The thickness dependence observed is believed to be a result of the "dead layer" commonly observed in ferroelectric and paraelectric thin films.[10] We believe that the electric field dependence of dielectric constant is the cause of the capacitance decrease at increasing positive bias for the Pt/BST/ZnO capacitors in Fig. 2(a). The net *C-V* characteristics of the Pt/BST/ZnO capacitors are believed to be a superposition of the field-dependent dielectric constant of the BST insulator and the depletion to accumulation properties of the metal-insulator-semiconductor structure.

The output characteristics of a representative ZnO/BST thin-film transistor are shown in Fig. 3. The device shows clear transistor operation in the range of V_{DS}=0–8 V. The drain current shows a flat saturation characteristic (large output impedance) and clear gate modulation for V_{GS}=0–5 V. The control of drain current by the gate in these devices is excellent given the large thickness of the gate insulator (740 nm) and may be attributed to the large dielectric constant of the BST material. The transfer (I_D-V_{GS}) characteristics of the representative thin-film transistor are shown in Fig. 4. The channel mobility (μ_{sat}) and threshold voltage

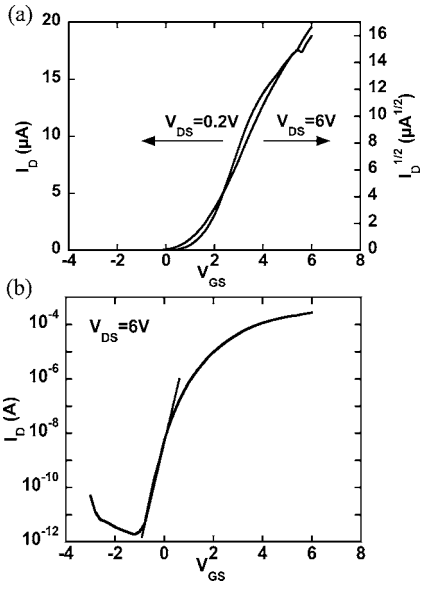

FIG. 4. Gate characteristics (I_D-V_{GS}) of a representative ZnO/BST thin-film transistor (a) in linear and saturation modes and (b) log scale in saturation mode.

(V_{th}) were calculated by a linear fit of the $I_{DS}^{1/2}$ vs V_{GS} curve of the transistor operating in the saturation region and applying the saturation region expression for a field effect transistor,

$$I_{DS} = \left(\frac{\varepsilon_0 \varepsilon_r \mu_{sat} W}{t_{ins} 2L} \right) (V_{GS} - V_{th})^2 \quad \text{for } V_{DS} \geqslant V_{GS} - V_{th}, \tag{1}$$

where ε_r is the relative permittivity and t_{ins} is the BST thickness. A relative dielectric constant of $\varepsilon_r = 500$ was used for BST, measured at 1 MHz. The threshold voltage of the device was determined to be $V_{th} = 1.2$ V. No clear variation in threshold voltage was observed with varying V_{DS}. The channel mobility for the device was determined to be 2.3 $cm^2\ V^{-1}\ s^{-1}$. This value for mobility is consistent with ZnO thin films we have previously deposited on glass substrates under similar deposition conditions where Hall effect measurements indicated electron mobility in the range of 1–5 $cm^2\ V^{-1}\ s^{-1}$. The on/off ratio, off current, and subthreshold slope were measured using the $\log(I_{DS})$ vs V_{GS} curve of the transistor in the saturation region. The on/off ratio was measured to be $I_D^{on}/I_D^{off} = 1.5 \times 10^8$ for operation in the saturation region, with an off current of $I_D^{off} = 1.8$ pA, as shown in Fig. 4(b). The subthreshold slope was determined to be $S = 0.25$ V/decade by fitting a straight line to the curve about the region that has a maximum slope over a 500 mV range. In our *C-V* characteristics we observed clear frequency dependence [Fig. 2(a)] suggesting the presence of traps at the BST/ZnO interface. Despite this observation, we observe no detectable hysteretic behavior in the dc gate characteristics when sweeping V_{GS} in forward and reverse directions (Using Keithley 4200's voltage list sweep option). In addition, the reduction in BST dielectric constant at increasing V_{GS} does not appear to have a negative effect on transistor performance.

In conclusion, the electrical characteristics of ZnO thin-film transistors with BST gate dielectrics were presented. Capacitance-voltage characteristics show a unique behavior combining the field-dependent dielectric constant of the BST insulator and the depletion-accumulation characteristic of the metal-insulator-ZnO structure. Transistors utilizing a thick BST gate insulator demonstrate good operating characteristics with a low and stable threshold voltage of ~1.2 V, high output conductance, operating voltage in the 0–8 V range, high on/off ratio of $\sim 10^8$, and low off current of <2 pA. The results obtained for the ZnO/BST transistors suggest that ZnO/BST structures may be a viable technology for transparent electronics or future electronics based on single crystal ZnO.

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[1] E. M. C. Fortunato, P. M. C. Barquinha, Ana C. M. B. G. Pimentel, A. M. F. Goncalves, A. J. S. Marques, R. F. P. Martins, and L. M. N. Pereira, Appl. Phys. Lett. **85**, 2541 (2004).
[2] R. L. Hoffman, B. J. Norris, and J. F. Wager, Appl. Phys. Lett. **82**, 733 (2003).
[3] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, Science **300**, 1269 (2003).
[4] P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes, Jr., Appl. Phys. Lett. **82**, 1117 (2003).
[5] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, J. Appl. Phys. **93**, 1624 (2003).
[6] B. J. Norris, J. Anderson, J. F. Wager, and D. A. Keszler, J. Phys. D **36**, L105 (2003).
[7] H. S. Bae, M. H. Yoon, J. H. Kim, and S. Im, Appl. Phys. Lett. **83**, 5313 (2003).
[8] I. Kim, Y. Choi, and H. Tuller, Appl. Phys. Lett. **87**, 043509 (2005).
[9] A. K. Tagantsev, V. O. Sherman, K. F. Astafiev, J. Venkatesh, and N. Setter, J. Electroceram. **11**, 5 (2003).
[10] L. J. Sinnamon, R. M. Bowman, and J. M. Gregg, Appl. Phys. Lett. **78**, 1724 (2001).