INTEGRATION OF BULK PIEZOELECTRIC MATERIALS INTO MICROSYSTEMS

by

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To my dearest family:
Your unyielding love, support and dedication made this possible

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ABSTRACT

INTEGRATION OF BULK PIEZOELECTRIC MATERIALS INTO MICROSYSTEMS

by

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Bulk piezoelectric ceramics, compared to deposited piezoelectric thin-films, provide greater electromechanical coupling and charge capacity, which are highly desirable in many MEMS applications. In this thesis, a technology platform is developed for wafer-level integration of bulk piezoelectric substrates on silicon, with a final film thickness of 5-100μm. The characterized processes include reliable low-temperature (200˚C) AuIn diffusion bonding and parylene bonding of bulk-PZT on silicon, wafer-level lapping of bulk-PZT with high-uniformity (±0.5μm), and low-damage micro-machining of PZT films via dicing-saw patterning, laser ablation, and wet-etching. Preservation of ferroelectric and piezoelectric properties is confirmed with hysteresis and piezo-response measurements. The introduced technology offers higher material quality and unique advantages in fabrication flexibility over existing piezoelectric film deposition methods.

In order to confirm the preserved bulk properties in the final film, diaphragm and cantilever beam actuators operating in the transverse-mode are designed, fabricated and tested. The diaphragm structure and electrode shapes/sizes are optimized for maximum deflection through finite-element simulations. During tests of fabricated devices, greater than $12\mu m_{PP}$ displacement is obtained by actuation of a $1mm^2$ diaphragm at 111kHz with <7mW power consumption. The close match between test data and simulation results suggests that the piezoelectric properties of bulk-PZT5A are mostly preserved without any necessity of repolarization.

Three generations of resonant vibration energy harvesters are designed, simulated and fabricated to demonstrate the competitive performance of the new fabrication process over traditional piezoelectric deposition systems. An unpackaged PZT/Si unimorph harvester with $27mm^3$ active device volume produces up to 205µW at 1.5g/154Hz. The prototypes have achieved the highest figure-of-merits (normalized-power-density × bandwidth) amongst previously reported inertial energy harvesters.

The fabricated energy harvester is utilized to create an autonomous energy generation platform in $0.3cm^3$ by system-level integration of a 50-80% efficient power management IC, which incorporates a supply-independent bias circuitry, an active diode for low-dropout rectification, a bias-flip system for higher efficiency, and a trickle battery charger. The overall system does not require a pre-charged battery, and has power consumption of <1µW in active-mode (measured) and <5pA in sleep-mode (simulated). Under 1g vibration at 155Hz, a 70mF ultra-capacitor is charged from 0V to 1.85V in 50 minutes.

Chapter 1

Introduction

The rapid advances in solid-state electronics have opened a new era in human history and continue to change on how we interact with our environment. One leg of this development is the increasing computational performance at smaller scales for automated and fast data processing, transferring and storing. Another leg is the physical interfaces & transducers. Transducers enable the interaction of an electronic device with the physical world around it, and functionalize it to sense, transfer or respond to environmental or user data inputs from different physical domains. In this regard, micro-fabricated transducers, or micro-electro-mechanical systems (MEMS), have seen significant progress over the past three decades since the commercialization of the first MEMS products, pressure sensors, in 1980s [Wise98]. Compared to macro-scale transducers, these miniaturized devices can provide higher precision and efficiency in compact volumes while lowering the fabrication/assembly costs by leveraging, adapting and improving the batch production process techniques that have been initially developed for the integrated circuits industry. As MEMS researchers and engineers around the world strive to develop new devices with higher performance and increased functionality, they are looking into incorporating new sensing/actuation mechanisms into existing micro-fabrication process technologies. In this sense, an increasingly popularized and unique electromechanical energy transduction mechanism is provided by piezoelectric materials, which enable direct conversion of energy between mechanical and electrical domains due to their inherent or engineered molecular structure. Although these materials are readily in use by a variety of macro-scale devices, their integration into microsystems have been challenging due to shortcomings of existing additive microfilm deposition techniques. As an alternative, a new piezoelectric MEMS technology is described in this thesis, based on subtractive micro-machining and processing of bulk piezoelectric ceramics on silicon.

1.1. Piezoelectricity and Ferroelectricity Phenomenon

Piezoelectric materials produce electrical charge displacement due to a mechanical strain input (direct piezoelectric effect), or conversely produce a mechanical strain due to application of an electric field (inverse piezoelectric effect), in an amount proportional to the input strain or electric field respectively. The piezoelectric effect is reversible, i.e. the produced electric field or mechanical strain goes back to its original condition when the input mechanical or electrical input on the material is removed. The piezoelectric effect is first experimentally demonstrated by Pierre and Jacques Curie in 1880 [Manbachi11], who experimentally demonstrated electrical charge generation in quartz. The inverse piezoelectric effect was predicted within just a year through mathematical formulation by G. Lippman [Lippman1881].

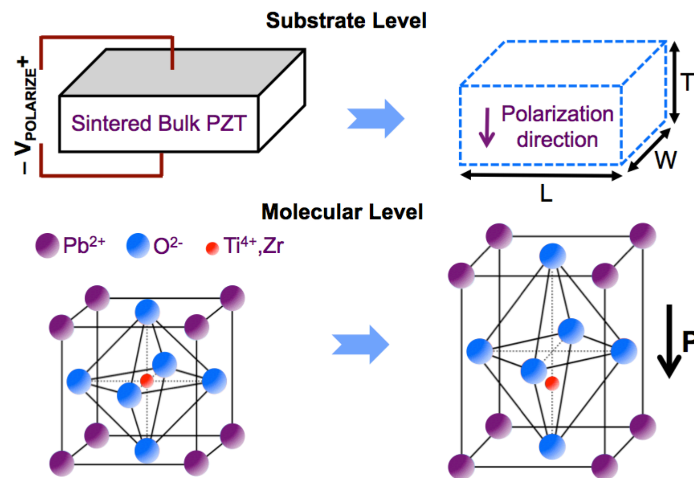


Fig.1.1 – Poling process of a PZT substrate and the change in its unit cell from cubic to tetragonal shape

Some piezoelectric materials, pyroelectrics, are known to form permanent dipoles in their crystal unit cells and they possess a spontaneous polarization as a result of their crystal orientation and phase [Webster99]. This inherent polarization changes with temperature. A subgroup of the pyroelectric materials, which are called ferroelectric, possess a spontaneous dipole moment that can be set in a defined direction with application of a high electric field (1500-3000 V/mm) less than the material's dielectric breakdown limit. In the electro-ceramics industry, this polarization process is usually performed using the Corona charging method at an elevated temperature (100-150°C) on the newly sintered bulk piezoelectric ceramics, such as PZT, PMN-PT, etc., where the quality of poling determines the final piezoelectric properties of the ferroelectric ceramic

[Damjanovic98]. During the poling process, the previously misaligned dipole domains are aligned with the applied electric field, and locked into a permanent polarization when the electric field is finally removed (remnant polarization).

Due to the reversible spontaneous polarization effect, ferroelectric properties show unique electrical and mechanical hysteresis [Lines79] (*Fig.1.2*). A common theory on the cause of this hysteresis is the energy dissipation due to domain wall motion and internal sliding and friction effects within the polycrystalline body [Smith99]. Depending on the direction and magnitude of the electric field, the remnant polarization of the material can be reversed. The electrical hysteresis of the ferroelectric materials can be leveraged in special applications such as tunable capacitors or memory devices (e.g. FeRAM [Buck52]). As it is seen in the mechanical butterfly hysteresis, an initially depolarized ferroelectric material can only expand and not contract with respect to its original strain condition upon application of an external electric field. However, a certain mechanical strain (i.e. a permanent expansion) remains within the material after the poling treatment, and hereafter the material deforms in both ways (expansion or contraction) according to the direction of the electric field.

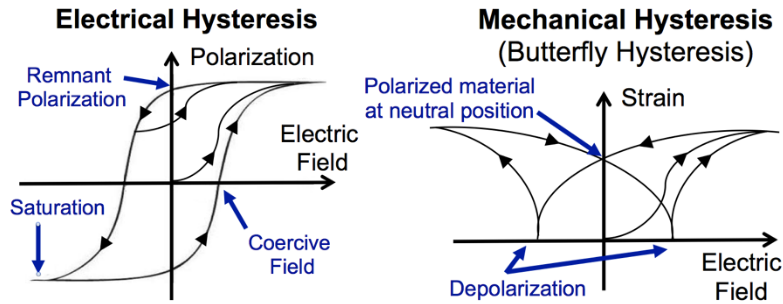


Fig.1.2 – Electrical and mechanical hysteresis effects on a ferroelectric material

The constitutive equations that describe the piezoelectric effects can be written in different expressions according to the chosen independent variables (stress, strain, polarization or electric field), although these expressions all route from the same energy forms. For this reason, there are a number of piezoelectric coefficient expressions (d_{ij}, e_{ij}, g_{ij}, and h_{ij}) that are used to define the piezoelectric coupling between different variables, although the values of these constants are all related to each other [Ballato96].

$$d = \varepsilon^T.g = e.s^E = \text{piezoelectric strain coefficient (m/V or C/N)} \quad (1.1)$$

$$e = \varepsilon^S.h = d.c^E = \text{piezoelectric charge coefficient (C/m}^2\text{ or N/Vm)} \quad (1.2)$$

$$g = \beta^T.d = h.s^D = \text{piezoelectric voltage coefficient (Vm/N or m}^2\text{/C)} \quad (1.3)$$

$$h = \beta^S.e = g.c^D = \text{piezoelectric stress coefficient (V/m or N/C)} \quad (1.4)$$

$$\varepsilon = 1/\beta = \text{permittivity} = \text{relative dielectric constant} \times \text{permittivity of air (F/m)} \quad (1.5)$$

The choice of stress (T) and electric field (E) as the independent variables is a common method to describe the constitutive equations, and especially to formulate the actuation modes. In this case, the constitutive equations are [IEEE87]:

$$Converse\ Piezoelectric\ Effect \rightarrow Strain = S_i = s_{ij}^E T_j + d_{mi} E_m \quad (1.6)$$

$$Direct\ Piezoelectric\ Effect \rightarrow Dielectric\ Displacement = D_m = d_{mi} T_i + \varepsilon_{mk}^T E_k \quad (1.7)$$

The superscripts in the notations are used to indicate the quantity held constant during measurement, and the subscripts *(ij)* indicate the electrical and mechanical directions, where the first subscript *(i)* represents the excitation direction, and the second value *(j)* represents the response direction. For instance, s^E is the compliance of the material at a constant electric field (i.e. the electrodes are short circuited), and d_{31} is the piezoelectric strain coefficient relating the strain response in the 1-direction to the electric field applied in the 3-direction.

Since piezoelectric materials typically exhibit anisotropic characteristics, their material properties including the stress-strain response (i.e. resultant deformation under an applied stress) are defined in matrix forms. The elastic constants determining the stress-strain mechanical relation can be defined in terms of either stiffness coefficients (c_{ij}) with a dimension unit of Pa, or compliance coefficients (s_{ij}) with a unit of Pa^{-1}. Thus, the constitutive equations can be expanded as follows [Seitz57].

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & s_{14} & s_{15} & s_{16} \\ s_{21} & s_{22} & s_{23} & s_{24} & s_{25} & s_{26} \\ s_{31} & s_{32} & s_{33} & s_{34} & s_{35} & s_{36} \\ s_{41} & s_{42} & s_{43} & s_{44} & s_{45} & s_{46} \\ s_{51} & s_{52} & s_{53} & s_{54} & s_{55} & s_{56} \\ s_{61} & s_{62} & s_{63} & s_{64} & s_{65} & s_{66} \end{bmatrix} . \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \\ d_{31} & d_{32} & d_{33} \\ d_{41} & d_{42} & s_{43} \\ d_{51} & d_{52} & s_{53} \\ d_{61} & d_{62} & s_{63} \end{bmatrix} . \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \quad (1.8)$$

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & d_{13} & d_{14} & d_{15} & d_{16} \\ d_{21} & d_{22} & d_{23} & d_{24} & d_{25} & d_{26} \\ d_{31} & d_{32} & d_{33} & d_{34} & d_{35} & d_{36} \end{bmatrix} . \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon_{33} \end{bmatrix} . \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \quad (1.9)$$

As most of the piezoelectric materials are orthotropic, the elasticity and permittivity matrices can be simplified to more manageable forms with fewer independent variables.

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & 0 & 0 & 0 \\ s_{12} & s_{22} & s_{23} & 0 & 0 & 0 \\ s_{13} & s_{23} & s_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{66} \end{bmatrix} \cdot \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \\ d_{31} & d_{32} & d_{33} \\ d_{41} & d_{42} & s_{43} \\ d_{51} & d_{52} & s_{53} \\ d_{61} & d_{62} & s_{63} \end{bmatrix} \cdot \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \quad (1.10)$$

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & d_{13} & d_{14} & d_{15} & d_{16} \\ d_{21} & d_{22} & d_{23} & d_{24} & d_{25} & d_{26} \\ d_{31} & d_{32} & d_{33} & d_{34} & d_{35} & d_{36} \end{bmatrix} \cdot \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} \varepsilon_{11} & 0 & 0 \\ 0 & \varepsilon_{22} & 0 \\ 0 & 0 & \varepsilon_{33} \end{bmatrix} \cdot \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \quad (1.11)$$

The symmetry within a piezoelectric crystal structure limits its coupling to only a subset of directions. These favored operation modes are determined specifically for each piezoelectric material, depending on its polarization direction, crystal structure, and material phase. For instance, for lead zirconium titanate (PZT) the most efficient operating modes are 33 and 31, where the direction of applied electric field or strain is parallel or perpendicular with the resultant strain or electric field, while for quartz, the most favored operation is in 12-mode. Therefore, for PZT material, the matrix of piezoelectric strain coefficients can be simplified as follows [Kholkin08].

$$d = \begin{bmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{15} & 0 & 0 \\ d_{31} & d_{31} & d_{33} & 0 & 0 & 0 \end{bmatrix} \quad (1.12)$$

In *Fig.1.3-4*, the common operating modes of a PZT substrate are displayed, and simplified constitutive relations are provided to formulate the sensing or actuation mode. In these figures, the total displacement on the material is shown as unidirectional for sake of visual simplicity, however the actual expansion/contraction occurs in a bidirectional manner. As it is seen, the generated displacements and electric fields are linearly proportional to the piezoelectric strain coefficient of that specific mode. Although the piezoelectric coefficients of PZT are commonly higher in the 33-mode, it is generally more favorable to use this material in the 31-mode, due to the mechanics of bending structures and large lateral/vertical dimension ratios in practical devices. Therefore, 31-mode bending beam and diaphragm sensors and actuators are the most frequently used structures in literature, and they are shown to provide a very effective electromechanical conversion mechanism providing either high actuation range or high sensitivity.

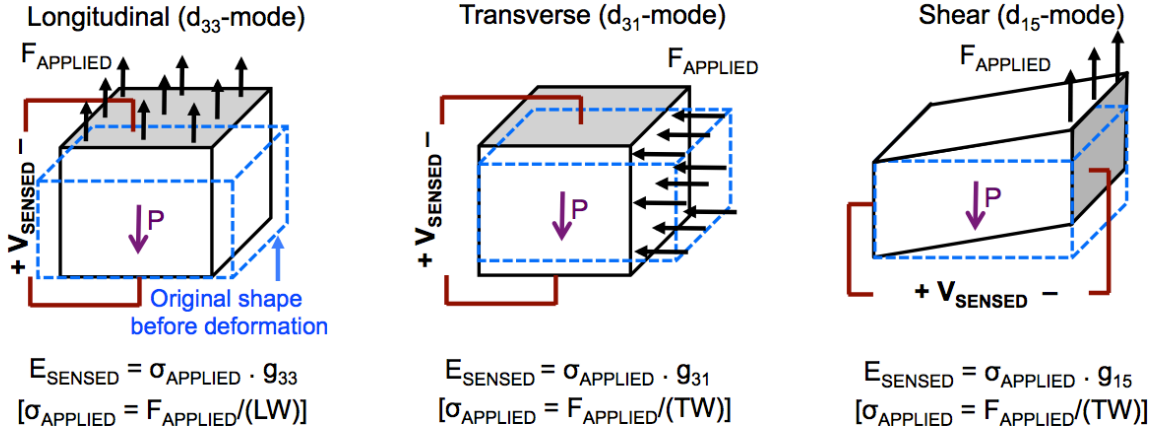


Fig.1.3 – The direct piezoelectric modes in a PZT material that can be used for sensing

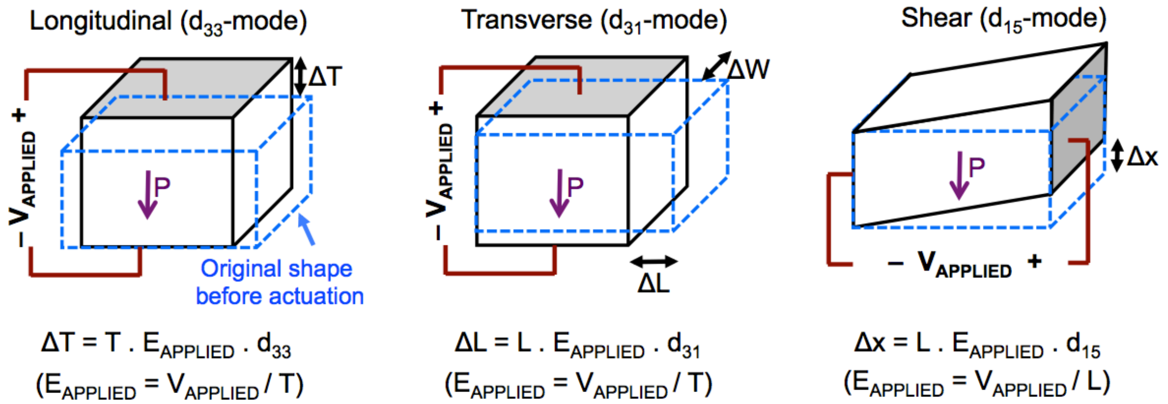


Fig.1.4 – The inverse piezoelectric modes in a PZT material that can be used for actuation

A significant characterization property of the piezoelectric materials is the electromechanical coupling coefficient, k_{ij}^2. This dimensionless term describes the ability of a material to transform energy between electrical and mechanical domains [Uchino03].

$$k^2 = \frac{\text{Stored mechanical energy}}{\text{Supplied electrical energy}} = \frac{\text{Stored electrical energy}}{\text{Supplied mechanical energy}} \qquad (0 < k^2 < 1) \qquad (1.13)$$

Since most piezoelectric transducers operate in the 31-mode, the transverse piezoelectric coupling factor in these directions is a useful term for comparison of different materials in terms of their energy transduction ability [Jiang03]:

$$k_{31}{}^2 = \frac{d_{31}{}^2}{\varepsilon_{33}^T s_{11}^E} \qquad (1.14)$$

Since the piezoelectric transduction phenomenon is fairly simple and efficient, it provides several advantages over electromagnetic or electrostatic conversion. Compared to electrostatic devices, piezoelectric actuators are not limited in their displacement range by a pulling voltage, the generated force values are higher, the actuation amplitude changes linearly with the applied voltage, and the required actuation voltages are

considerably lower and can be provided by a CMOS chip easily. Compared to electromagnetic devices, they do not require a bulk heavy permanent magnet in the design, the designs are easily scalable with micro-fabrication technologies, and also the voltage-based control of piezoelectric devices is simpler to implement in circuits, compared with current-based electromagnetic devices.

There is a wide range of application fields for piezoelectric materials in the micro-fabrication world. Some of the recent devices from literature and expected future applications are listed below:

- *Microfluidics:* micro-pumps, micro valves, fluidic mixers, droplet generators
- *Optical:* micro mirrors, micro scanners
- *Mechanical Sensors:* accelerometers, bio-sensors, touch sensors, atomic microscopy
- *Resonators:* surface acoustic wave filters, bulk acoustic filters, delay lines
- *Solid-state:* tunable capacitors, memory devices
- *Energy:* vibration/force/shock energy harvesters, pyroelectric energy harvesters
- *Sound:* microphones, micro-speakers, hearing aids, hydrophones, alarms, buzzers
- *Ultrasonic generators*: sonar, atomizers, jet-propulsion, ultrasonic imaging
- *High-voltage:* micro-switches, relays, transformers
- *Mechanical actuators:* micro motors, vibration isolation, precision positioning

1.2. Existing Piezoelectric Deposition Processes for Microsystems

There have been several methods studied previously for fabrication of piezoelectric layers on silicon substrate. Some of the main deposition techniques and materials used in these studies for development of MEMS devices are:

- Sol-gel or composite sol spin-coating of PZT
- Direct writing (ink-jet printing) of PZT sol
- Screen printing of PZT
- Sputtering of PZT, PZNT, PMN-PT, AlN or ZnO
- Electro-phoretic deposition of PZT
- Epitaxial growth of PZT, AlN or GaN
- Hydrothermal deposition of PZT
- Aerosol deposition of PZT

Some of these deposition methods are described in the following subsections.

1.2.1. ZnO Sputtering

Deposition of ZnO thin-films (<1-2 μm) by conventional DC and RF-magnetron sputtering tools and pulsed laser deposition was one of the first studied methods for fabrication of piezoelectric micro sensors and actuators on silicon due to the ease of deposition process. This material can be sputtered at room temperature, does not require a seed layer unlike AlN, and has a self-poling capability without a subsequent electrical-thermal poling procedure. On the other hand, the fast diffusion rate of Zn into silicon makes challenging the integration of this material on CMOS and its long-term reliability, although ZnO surface acoustic wave devices have been combined with standard IC processes [Vellekoop94]. In addition, the commonly encountered low resistivity (high DC leakage) in ZnO films impedes operation in the low frequency range. The film resistance can be improved by PECVD deposition of thin SiO_2 as top and bottom insulation layers [Kuoni02], however this can also decrease the effective piezoelectric properties. The deposition of ZnO at low temperatures is known to result in high compressive residual stress, due to the lack of energy in atoms to arrange themselves into their lowest energy state. A variety of deposition parameters can affect the film stress, including deposition power, sputtering rate, gas mixture, chamber pressure, and substrate temperature [Hickernell83] [Zesch91]. The intrinsic stress in the film can be relaxed by either increasing the deposition temperature up to 225-375°C, or adding an annealing step at 300-500°C after the deposition process. The heat treatment eliminates boundary defects and improves the preferred c-axis orientation of the poly-crystalline film [Cimpoiasu96].

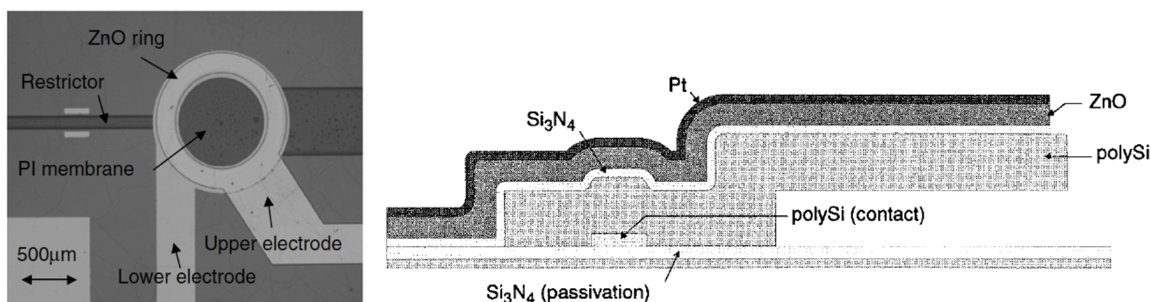


Fig.1.5 – a-) Top view of a liquid flow pressure sensor fabricated by deposition of ZnO on a polyimide sheet [Kuoni03]; b-) A surface-micromachined ZnO cantilever beam actuator [DeVoe97].

Previously, sputtering of ZnO has been demonstrated on polyimide membranes on silicon for liquid flow pressure sensors [Kuoni03], and on surface-micromachined poly-

silicon layers for cantilever beam actuators [DeVoe97] (*Fig.1.5a-b*). Furthermore, the fabrication of free-standing individual ZnO nanowires/nano-belts has been demonstrated in [Kong03]. The effective piezoelectric strain coefficient d_{33} of nano-belts is measured to vary between 14.3 to 26.7 pm/V depending on frequency [Zhao04], which is much higher than that of the bulk (001) ZnO, 9.3 pm/V. Even though ZnO is a non-ferroelectric material, the frequency-dependent properties are hypothesized to be caused by pinning of spontaneous polarization and surface charging, as a result of the high surface-to-volume ratio of the nanowires. These ZnO nano-belts are leveraged in fabrication of field effect transistors [Arnold03] and nano-cantilevers [Hughes03].

1.2.2. PZT Sol-gel Spin-Coating

For incorporation of PZT on silicon, initially sol-gel deposition has been one of the most popular and widely investigated methods, since it offers a fast and low cost fabrication process. The process is as simple as basic spin-coating technology, but it also provides some ability to control homogeneity and composition of the deposited film over a large surface area [Li94]. The fabrication can be usually summarized in four main steps [Nakao95]. First, a small drop of liquid precursor solution, including suspended nano-scale PZT particles, is squeezed over silicon substrate. Then, spin coating is performed at a defined rotation speed depending on the desired target film thickness, and the viscosity, surface adhesion, drying rate, and sol composition of the PZT sol-gel. The wafer spin rate is usually increased gradually to avoid bubble formation in the film, which is also a common method for photo-resist coating. After spin-coating, the first annealing step, called as pyrolysis, is performed at a relatively low temperature (300˚-400˚C) for a few minutes. During this drying process, the liquid phase (organic solvents) is removed from the gel, and a porous material is left behind. At this early stage, there is still enough fluid for particle reorientation, and this allows relief of film stress due to shrinkage. After pyrolysis, this one cycle of spin coating process can be repeated multiple times in order to increase the final film thickness up to 1-2 μm [Mitsubishi02] (*Fig.1.6*). Finally, crystallization, commonly achieved by a rapid thermal annealing step around 700˚C, is performed to form perovskite phase in the PZT film. In some cases, an additional annealing step can be used to densify and sinter the film by exposure to higher temperatures for a prolonged time. However, a higher annealing temperature comes also

with more thermal stress, larger mechanical deformation in the film, and Pb out-diffusion from the film, which means a degradation in the piezoelectric properties [Dai04]. It has been shown that performing the annealing step in a PbO rich environment can counter the Pb out-diffusion from the film [Kosec99].

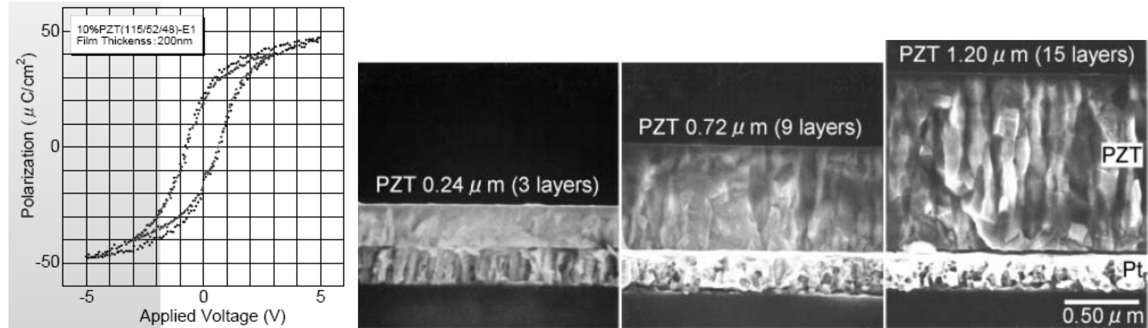


Fig.1.6 – Spin-coated and annealed sol-gel PZT films by Mitsubishi Materials Inc. [Mitsubishi02]

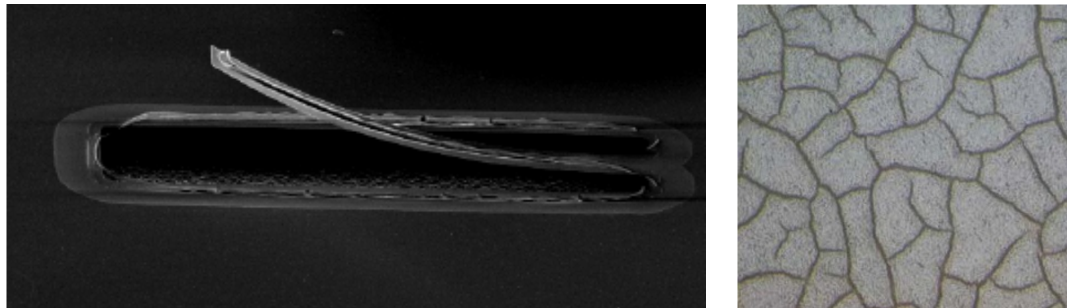


Fig.1.7 – a-) Curving due to residual stress [Frederick06]; b-) Cracking during annealing [Dauchy07]

Although, the process seems to be simple, it includes several fabrication issues due to required high temperature annealing steps. One of the problems is due to the volatility and reactivity of Pb. Silicon dioxide or silicon nitride layers are not effective against diffusion of lead, since lead silicate formation occurs at PZT interface. So, there is a need for thin and effective diffusion barrier with good adhesion. Several diffusion barriers are used in previous studies, such as ZrO_2 [Dorey03], $SiO_2/TiO_2/Pt$ [Glynne-Jones00], MgO [Jeon00], YSZ [Hren92], or YSZ/TiO_2 [Kim01]. Another crucial problem is the stress in the final deposited film. Film shrinkage occurs during pyrolysis and sintering due to drying and burning out of solvents and binders in the mixture. Therefore, these high temperature processes are the main causes for in-plane tensile stress, which may lead to a variable density profile through the thickness, micro-cracks, and even delamination of the deposited layer during processing. *Fig.1.7a* shows a curved PZT cantilever beam due to high thermal stress, while *Fig.1.7b* gives an example of cracking issues during pyrolysis. In order to improve the thermal expansion mismatch between the film and substrate, a

thin ZrO_2 ceramic layer can be used as interface film, since its thermal expansion coefficient has a value similar to that of PZT [Brooks96]. Also, the bottom electrode used in the process should withstand the high processing temperature without peeling off. In the previous studies, generally Pt or conductive ceramic RuO_2 is used for this purpose. Pt electrode can withstand up to 850˚C without degradation, and Ti or TiO_2 layer can be used for adhesion.

As it is stated before, high temperature sintering is necessary to obtain perovskite phase in PZT. Although bulk PZT sintering temperature is around 1100-1300˚C, several types of sintering aids are generally used in a sol-gel to lower the sintering temperature down to 700-850˚C for integration into silicon processing. Some of the common materials for this purpose, and their melting temperatures are PbO (886˚C) [Futakutchi00] and $Pb_5Ge_3O_{11}$ (738˚C) [Tran01]. These sintering aids are very beneficial, since they allow shear stress relaxation by providing particle reflow. Although these additives increase the density of final film and lower the porous profile, the piezoelectric property might degrade due to atomic mixing. Other additives can also be used in a sol-gel composition to release stress, enhance compliance or increase single-spin film thickness. For instance, PVP (polyvinyl pyrrolidine) or PVB (polyvinyl butral) can break down polymeric gel network and increase flexibility [Kozuka02] [Takahashi00]. However, these additional organic materials in the film also cause inhomogeneity during crystal growth and lower functionality of the film.

1.2.3. PZT Sputtering

Since sputtering is a fairly well known deposition technique for thin film fabrication in MEMS field, a good amount of effort has been given in previous studies to obtain a high quality film by this method. In addition, the films fabricated by this method are typically oriented appropriately as deposited, and they do not require a poling procedure. The substrate temperature during PZT deposition is usually in the 450-650˚C range, and as temperature increases larger crystal particle diameter can be obtained, which results in higher piezoelectric properties in the final thin film. However, due to the high substrate temperature and rapid cooling at the end of the process, the final film may suffer from thermal stress issues. Additionally, pinholes have been reported in some depositions due to low melting temperature (327˚C) and high vapor pressure of lead [Tsuchiya06].

For a high quality film it is necessary to optimize several deposition parameters, including the target composition, substrate material, buffer layer on the substrate, substrate temperature, chamber pressure, substrate position and angle, input power, sputtering time, gas pressure and flow ratio, and other sputtering related variables. A figure of RF-magnetron sputtering chamber used for PZT deposition is illustrated in *Fig.1.8a*. One of the fabrication challenges related to sputtering is to obtain a uniform crystal orientation throughout the film thickness and over the whole wafer area. Having a mixture of orientations in the film is known to degrade the piezoelectric property due to cancellation of overall effective coupling by different crystal grain polarizations.

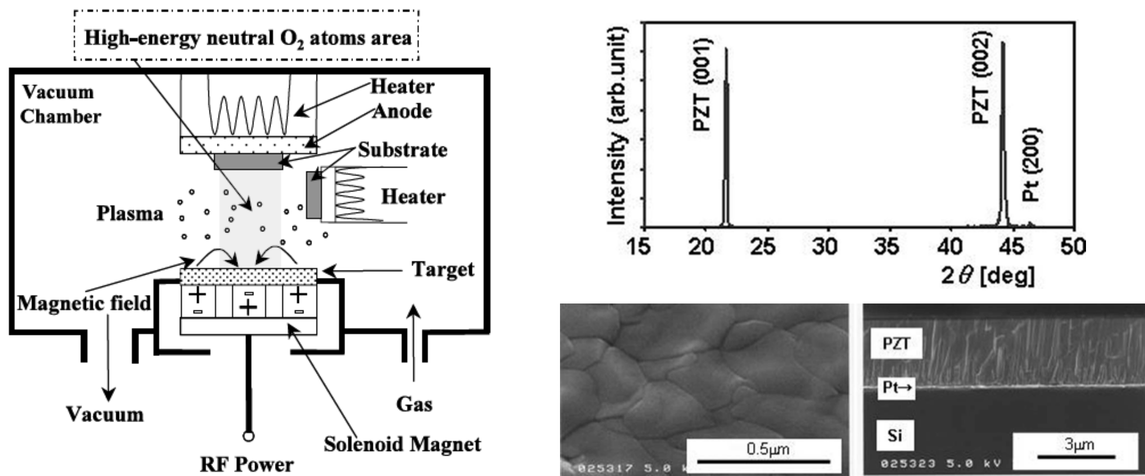


Fig.1.8 – a-) The RF-magnetron sputtering chamber used for deposition of PZT in [Tsuchiya06; b-) 3-μm thick (001) oriented sputtered PZT film on Pt/Ti coated silicon substrate [Fujii07].

The initial studies in this field have reported that (111) oriented PZT films are expected to have higher piezoelectric coefficients than (001) oriented films, although experiments done in [Tsuchiya06] have indicated problems associated with sputtering a pure (111) oriented thin film. In this work, a pure perovskite crystal structure is deposited on a $PbTiO_3$/Pt/Ti buffer layer at 630˚C substrate temperature, with a deposition rate of 0.2 nm/sec at 100 W. The particle diameter is measured as 250 nm, and the piezoelectric strain coefficient d_{31} of the sputtered film is measured as -28 pm/V. More recently, deposition of (001) oriented PZT films with composition near a morphotropic phase boundary around a Zr/Ti ratio of 53/47 is demonstrated to provide superior piezoelectric properties than that of (111) oriented films [Fujii07]. In this work, 3 μm thick PZT film is sputtered from a sintered $[(PbZr_{0.53}Ti_{0.47}O_3)_{0.8}+(PbO)_{0.2}]$ ceramic target on a silicon substrate at 600˚C, which has a Pt/Ti coating with an additional MgO buffer layer on

some of the samples (*Fig.1.8b*). The measured d_{31} values are very large, with values between -100 pm/V to -150 pm/V, compared to previously reported thin film properties, and the dielectric loss of the film is measured as 2%.

1.2.4. AlN Sputtering

The use of AlN in microelectronics started to be investigated by late 1960s due to its relatively high thermal conductivity (as high as 285 W/m/K) and high temperature durability as an electrically insulating ceramic [Noreika68]. With recent advancements in its standardized thin film deposition process, AlN is also demonstrated to be a beneficial piezoelectric material for a variety of microsystem applications, especially thin film sensors and high-Q resonators. This material is perfectly IC compatible, and has large resistivity and more stable characteristics compared to ZnO when exposed to humidity and temperature variance. In addition, AlN does not require poling unlike ferroelectric materials, and it has larger yield strength (300 MPa) than the PZT material (<80 MPa). Also, its high acoustic velocity (~11000 m/s) has found utilization in high-frequency bulk-acoustic mode and counter-mode resonators [Zuo08]. On the other hand, although AlN (and GaN) has the highest piezoelectric coupling among other nitrides and can demonstrate comparable piezoelectric charge coefficient (e_{31}) with respect to some of the deposited PZT thin films, at the end it still incorporates a lower electromechanical coupling (k_{ij}^2) compared to bulk PZT and other lead-based materials. While the low dielectric loss (~0.2%) and high mechanical quality factor of this material can favor its use in low-noise sensors and micro/nano high-Q filters, it is more favorable to utilize PZT to realize high-force, high-deflection actuators, and wide-bandwidth high-efficiency energy harvesters.

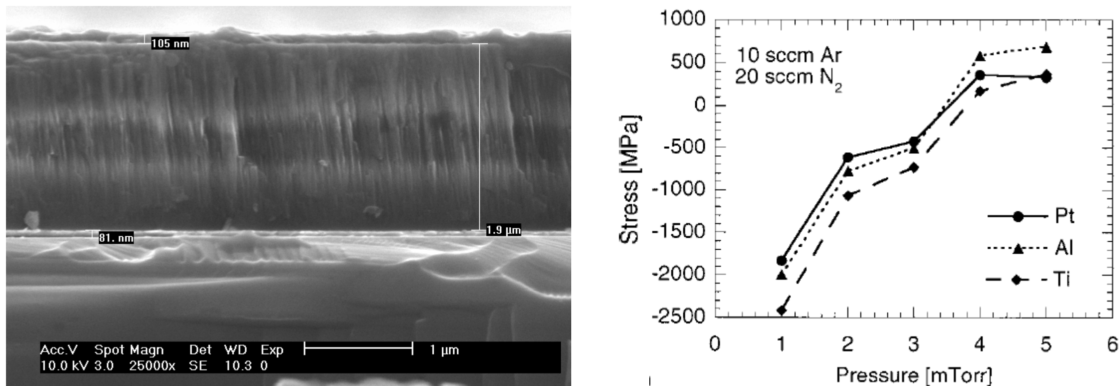


Fig.1.9 – a-) SEM cross-section of 1.9 µm thick AlN deposited at 450˚C by DC magnetron sputtering [Chen06]; b-) Dependence of film stress to chamber pressure in a AlN DC-sputtering system [Dubois01]

AlN thin films can be obtained by a wide range of deposition methods, such as chemical vapor deposition (CVD) [Kung95], plasma enhanced CVD [Young97], and molecular beam epitaxy (MBE) [Henlein98], and pulsed laser deposition [Bathe01]. The reactive sputtering is the most popular method because of its low-cost and low-temperature deposition. In order to obtain good piezoelectric properties, the AlN film should have a c-axis wurtzite crystalline structure oriented perpendicular to the substrate [Conrad09]. Therefore, sputtered Pt (111) is usually used as a buffer layer to facilitate growth of c-axis textured AlN film [Dubois99]. Molybdenum is also a preferred material as a buffer layer due to its low resistivity and high acoustic impedance [Ueda05]. In addition, a chemical-mechanical-polishing (CMP) step can be performed initially on the substrate in order to have a very smooth surface prior to the film stack deposition [Wang06]. The initial substrate surface roughness is an important parameter to achieve columnar AlN growth perpendicular to the substrate [Ruby02]. The AlN deposition can be performed via either DC [Chen06] or RF reactive magnetron sputtering in an Ar/N_2 environment (*Fig.1.9a*). The intrinsic stress of the deposited films can show a large variance from strong compression to high tension sensitively depending on the chamber pressure, Ar/N2 flow rate, and the induced substrate potential (*Fig.1.9b*) [Dubois01]. Since existing native oxides on a substrate and an oxygen environment during deposition can degrade the piezoelectric properties of AlN severely, the sputtering is usually performed at a low base pressure after an RF sputter cleaning process [Marvell11]. Also, in order to prevent contamination of the sputter target, usually there are many restrictions in terms of allowed materials into the process chambers. Some of the restricted materials are substrates with high vapor pressure, substrates with mobile-ion content, photoresist, and materials that have low melting temperatures. In most of the cases, the fabrication facilities restrict allowable materials to only Si, SiO_2, Pt, Mo, and a few other exceptions.

1.3. Motivation for a New Piezoelectric MEMS Process

As described in the previous section, various thin/thick film deposition techniques have been developed for integration of piezoelectric materials on silicon, such as screen printing, sol-gel spin coating, and sputtering (*Table.1.1)*. However, these deposition techniques have their own fabrication challenges, including high-temperature processing, and issues related to film uniformity and process reliability. Although there have been

recent improvements in some of these processes for increased reliability, most of these technologies require sophisticated deposition tools and/or hard-to-tune process recipes. Thus, replicating the same film quality between different process runs is accepted as challenging by several experts in the field, even with the same exact process recipe and at the same fabrication facility. Furthermore, the deposited films are limited in maximum film thickness to few micrometers. In spite of the fact that this film thickness is sufficient and may be even preferred in many nano/micro resonator applications, there are many other micro transducers that can benefit from a thicker piezoelectric microfilm. Finally, despite the recent progress and promising efforts in the piezoelectric deposition systems, the fabricated thin films still show relatively less piezoelectric coupling compared to commercially available bulk ceramics, which can provide greater electro-mechanical coupling and charge capacity. The aim of this thesis work is to integrate these materials into MEMS by developing a standard, reliable and flexible fabrication method, in order to take advantage of their properties in a variety of film thicknesses.

Table.1.1 – Comparison of available fabrication processes for piezoelectric MEMS devices

Reference	Material	Transverse Coupling k_{31}^2	Strain Coeff. d_{31} (pm/V)	Material Thickness	Process Temperature
[Piezo08] [APC11]	**Bulk Ceramics** (PZT, PMN-PT, etc.)	0.09 – 0.65	100-1200	> 130 µm	–
[Wasa08] [Fujii09] [Fujii11]	Sputtered PMN-PZT / PNZT	0.09 - 0.33	83-259	< 3-5 µm	500-650˚C
[Kanno97] [Nistorica04] [Muralt05]	Sputtered PZT	0.07 – 0.15	28-150	< 2-4 µm	450–650˚C
[Morimoto10] [Isarakorn10]	Epitaxial PZT	0.09 - 0.15	49-140	< 3 µm	600-650˚C
[Jeon00] [Stamos08] [Hindrichsen10]	Screen Printed PZT	0.05 - 0.10	60-130	10-100 µm	650–900˚C
[Tadigadapa09] [Kobayashi08] [Pardo10]	Sol-gel PZT / Composite-Sol PZT	0.04 – 0.09	16-100	< 2-5 µm	400–800˚C
[Mortet04] [Clement04] [Karakaya08]	Sputtered AlN	0.02 - 0.04	1.9-2.3	< 2 µm	20–400˚C
[Devoe97] [Johnson05]	Sputtered ZnO	0.01 - 0.05	5.4-7.0	< 2 µm	20–500˚C

1.4. Thesis Goal

This thesis work seeks to advance the state-of-the-art in piezoelectric out-of-plane actuators and vibration energy harvesters, by enabling the use of high-performance piezoelectric substrates in microsystems. With this aim, a new wafer-level fabrication process is introduced to integrate bulk piezoelectric substrates on silicon, in a thickness range of 5 to 100 μm (*Fig.1.10*). The technology offers an advantageous flexibility for rapid adaptation of other existing and future bulk electro-ceramic materials, and a straightforward process, which utilizes traditional cleanroom tools instead of sophisticated and hard-to-tune deposition systems. While existing piezoelectric thin-film deposition methods are expected to remain useful for many micro/nano applications, the introduced technology will find its use in several microsystem applications as well, such as micro-speakers, micro-pumps, micro-motors, micro-thrusters, where high-force, high-deflection actuators are desired (*Fig.1.11*).

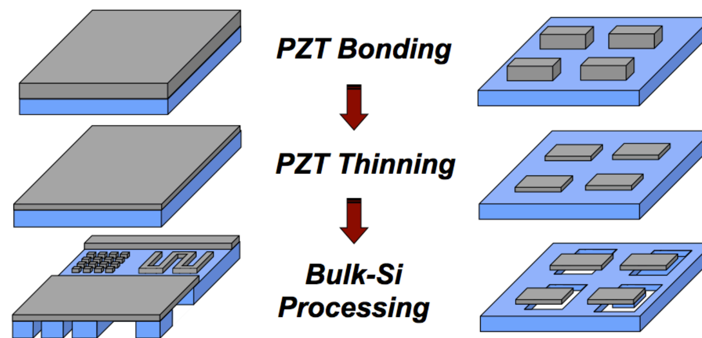


Fig.1.10 – General overview of the developed technology for bulk-PZT integration on silicon

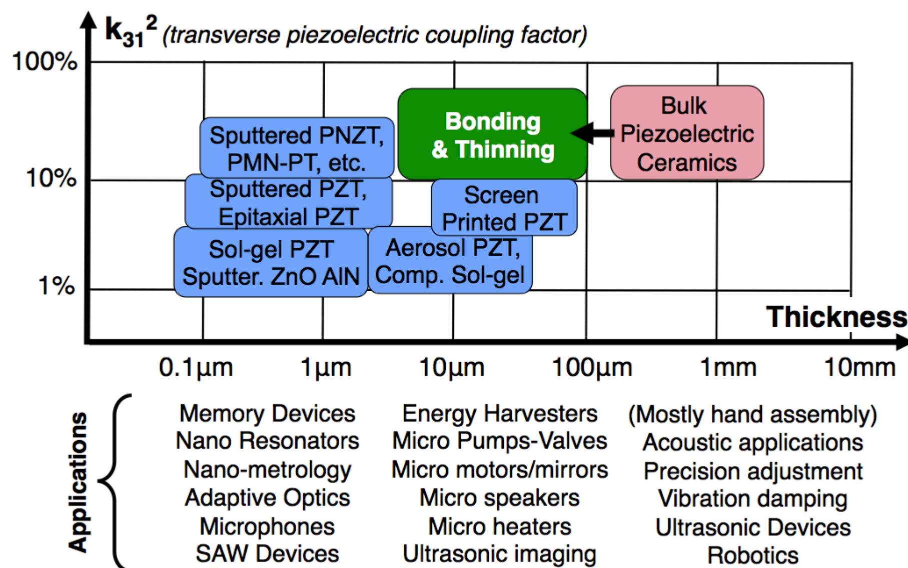


Fig.1.11 – Position of the developed process in the existing technology and application field

1.5. Thesis Contributions

The main scientific and technological contributions of this thesis are summarized as follows, while the detailed achievements can be found in the conclusion chapter.

1-) A CMOS-compatible wafer-level process technology is introduced for integration of bulk piezoelectric ceramics into microsystems in order to take advantage of their high piezoelectric properties in a thickness range of 5-100 μm for a wide range of applications, and associated bonding, thinning and patterning processes are characterized for increased reliability and process control.

2-) Surface micromachining capability and multi-layer deposition capability of this new process is explored by development of PZT diaphragms on pre-patterned silicon surface, and by development of a bimorph-PZT energy harvester, respectively.

3-) High-deflection and high-stroke out-of-plane piezoelectric micro-actuators are developed with state-of-the-art performance results, and the effects of layer-thickness ratio, piezoelectric actuation-mode, electrode dimensions, and residual stress to the actuator performance are extensively studied through analytical/simulation models.

4-) Resonant vibration energy harvesters are designed with optimized structural dimensions, decreased residual stress and structural damping, and three generations of devices are micro-fabricated with the developed bulk piezoelectric MEMS technology to result in record figure of merit values (power density times bandwidth) among state-of-the-art vibration energy harvesters.

5-) An autonomous energy harvesting platform is implemented in a compact volume to harvest the ambient vibration energy efficiently and charge a fully/partially depleted energy reservoir up to its regulated potential, while being self-supplied by the harvested energy with minimized active-mode and sleep-mode power consumptions.

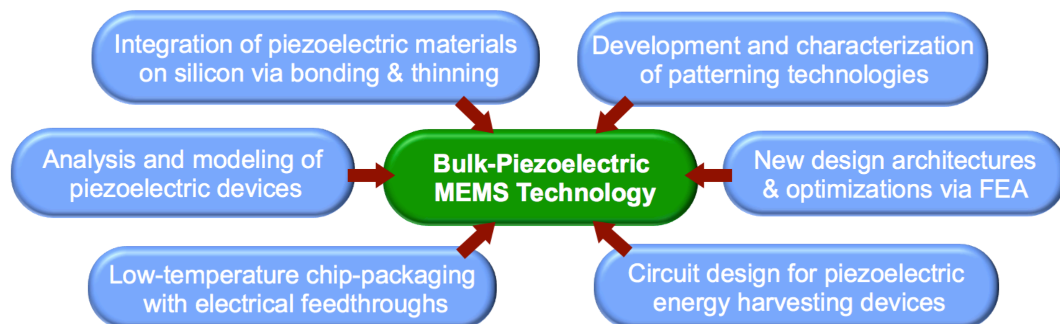


Fig.1.12 – Base elements of this thesis work for development of a new bulk-piezoelectric MEMS technology

1.6. Thesis Organization

This thesis is organized into six chapters. Chapter II introduces a CMOS-compatible bulk piezoelectric MEMS technology, and the characterization of associated fabrication processes, including AuIn transient-liquid-phase bonding, parylene bonding, loose and fixed abrasive lapping, lapping over pre-patterned structures, dicing-saw patterning, nano/femto-second laser micromachining, and wet-etching. The piezoelectric coupling in the final thinned bulk-PZT films is measured with piezo-response microscopy. This section also includes a discussion on the capabilities and limitations of the developed technology compared to traditional piezoelectric thin-film deposition approaches.

Chapter III presents design, optimization, and testing of out-of-plane diaphragm and cantilever beam actuators that are fabricated with the introduced process technology. The effects of layer-thickness ratio, piezoelectric actuation-mode, electrode dimensions, and residual stress on the diaphragm performance are analyzed. This section also provides a new piezoelectric diaphragm design that actuates in shear mode, which could be useful to minimize nonlinearities due to stress generation. Finally, loading capacity and actuation efficiency of transverse-mode diaphragms are characterized, and possible methods to increase the performance are experimented, such as addition of a isolation layer between PZT and electrodes, or confinement of PZT only at the actuation regions.

Chapter IV starts with an overview of the required specifications, target applications and recent developments in the vibration energy harvesting field. The piezoelectric energy transduction mechanism is analyzed, and finite element modeling is performed to optimize design variables of cantilever beam harvesters. In this section, the fabrication process and test results of micro-fabricated unimorph/bimorph piezoelectric prototypes are presented, and the device performance is compared with the state-of-the-art.

Chapter V provides a discussion on different power management architectures for piezoelectric harvesters, and details the design and implementation of a power management IC to realize an autonomous vibration energy harvesting platform. In addition, the system-level packaging and interconnection of the harvester, power management circuitry and surface-mount components are presented.

Chapter VI summarizes the milestones and achievements of this thesis, and presents suggestions for future work on technology improvement and device development.

Appendix A summarizes the first attempt to scavenge energy with non-resonant devices from live flying insects, in order to power an implanted neural control system. In this section, recent progress in the micro air vehicles and cyborg insects are discussed, and theoretical considerations on non-resonant piezoelectric energy harvesting are provided. Design, micro-fabrication, and test results of cantilever beam and spiral beam non-resonant energy harvesters are explained, and compared in performance with other possible energy transduction methods for hybrid insects.

In Appendix B, a meso-scale piezoelectric frequency increased generator with its design, fabrication, and test results is presented for harvesting low-frequency non-periodic vibrations. The generator incorporates bulk piezoelectric ceramics that are micro-machined into a FEA-optimized clamped-clamped spiral shape using femtosecond laser ablation. The test results are analyzed to determine the effectiveness of this generator and how to improve its performance in the future.

Appendices C and D include the calculation of residual stress in fabricated PZT/AuIn unimorph cantilever beams, and a list of piezoelectric and physical properties of materials used in the modeling of the fabricated devices, respectively.

Chapter 2

Thinned-PZT on Silicon Process

2.1. Overview of the Developed Process Technology

In place of additive piezoelectric microfilm deposition techniques, this thesis project has its focus on developing a subtractive fabrication process, so that the original properties of high-quality bulk piezoelectric materials can be preserved. The process involves bonding of commercially available piezoelectric substrates on silicon, and mechanical thinning to obtain the desired thickness (*Fig.2.1*).

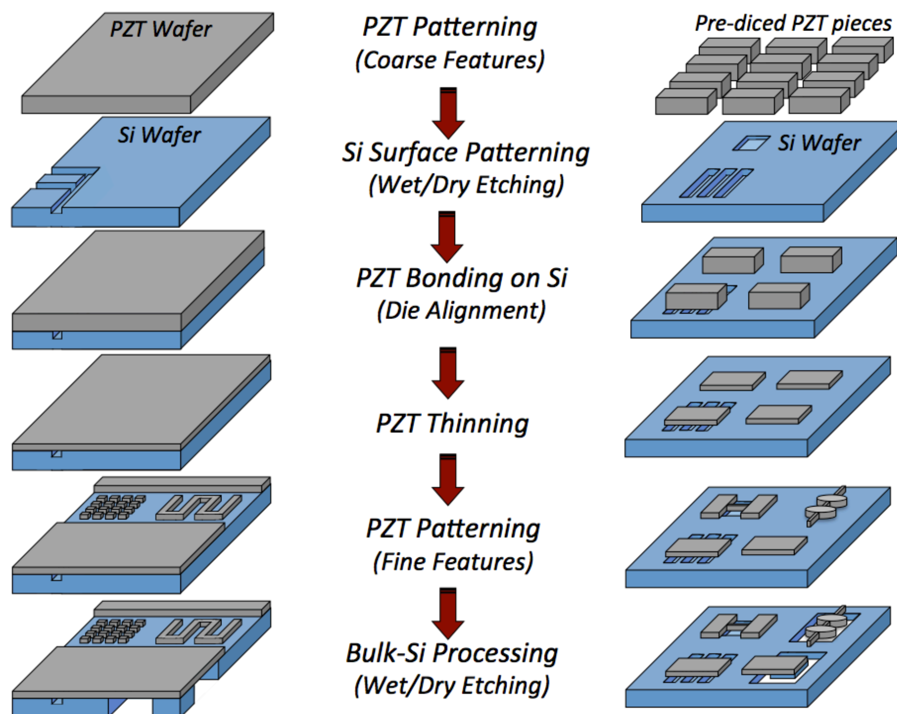


Fig.2.1 – Simplified overview of the developed process technology for integration of bulk PZT on Si.

The bonding can be performed at wafer-scale with a 4-6 inch bulk piezoelectric substrate, followed by subsequent PZT thinning and patterning. Alternatively, dicing can be used for initial patterning of simple PZT structures prior to bonding, so that chemical patterning can be avoided or simplified in the subsequent process steps. In order to

release the piezoelectric film from the silicon substrate to form mechanical structures, one can either use traditional bulk-silicon micro-machining techniques at the end of the whole process, or take advantage of silicon features that are patterned on the wafer surface prior to the bonding step. For patterning of the thin/thick piezoelectric layers for a wide variety of applications, various techniques are studied such as dicing saw patterning, laser ablation, and wet etching.

2.2. Bonding of Bulk Piezoelectric Substrates on Silicon

Previous studies for bonding of bulk piezoelectric ceramics on silicon or glass substrates have focused on bonding by surface activation [Takagi99], hydrophilic conditioning [Eda95], epoxy-resin [Xu08], Cytop [Wang08], AuSn [Turner02], or InSn [Cheong05]. However, these manufacturing techniques have faced significant process issues such as non-patternable bond layers, low bond strength due to high stress, voids in the bond layer, or out-diffusion of lead and re-polarization issues due to high temperature processing (*Table.2.1*).

Table.2.1 – Overview of piezoelectric substrate and Si bonding technologies studied in literature

Reference	Bond Layer Material	Bonding Temperature	Challenges
[Eda95]	Direct bonding by hydrophilic conditioning	350˚C-450˚C	Highly stressed bond layer No electrical connection
[Xu08]	Ag-epoxy resin	40˚C - 100˚C	Not patternable by lithography Poorly defined bond layer thickness
[Wang08]	Cytop	160˚C	Requires electrical feed-through Voids in the bond layer
[Tanaka05]	Au Eutectic	450˚C - 550˚C	Stressed bond layer Re-polarization issues
[Hucker07]	BCB	250˚C	Requires electrical feed-through

Typically, bonding of bulk PZT layers can be challenging because of the highly rough surface of commercial PZT substrates, high thermal mismatch between the bond interface and substrates, and morphological changes at high temperatures. In this study, we have developed low-temperature, fluxless, patternable, and reliable AuIn (conductive) and Parylene (non-conductive) bonding of bulk PZT-5A on Si wafers at both die-level (down to 200 μm) and wafer level (70 mm × 70 mm), and have demonstrated that bonding interfaces are strong enough to allow wafer-level mechanical thinning of the bulk PZT down to a thickness of less than 10 μm.

2.2.1. Bonding Setup and Profile

Both AuIn solder and parylene bonding processes are performed with a bonding pressure of 0.75 MPa to 1.5 MPa at 200˚C for 30-60 min (*Fig.2.2*). In addition, both bonding processes require a vacuum environment for decreased O_2(g) concentration in the medium, since parylene can degrade above 120˚C in air [Noh04a], and indium quickly forms a hard and thick oxide layer at elevated temperatures. Either of these cases would prevent a reliable bonding. During the bonding process, as the temperature increases, the intermediate bonding layer (either liquefied indium over its melting temperature, or softened parylene over its glass-transition temperature) re-flows over any bumpy surface profile and planarizes the surface roughness. Since both bonding processes are performed at 200˚C, depolarization (loss of permanent electric polarization, which is a characteristic property of ferroelectric materials) and subsequent degradation of piezoelectric properties due to bonding is not an issue for materials with high Curie temperatures such as PZT-5A. However, for low Curie temperature materials such as PZT-5H (T_C=200-250˚C) or lead-based single crystalline materials (T_C=100-175˚C) an electric field may need to be applied across the piezoelectric layer either during or after the bonding process in order to maintain the polarization or re-polarize the layer.

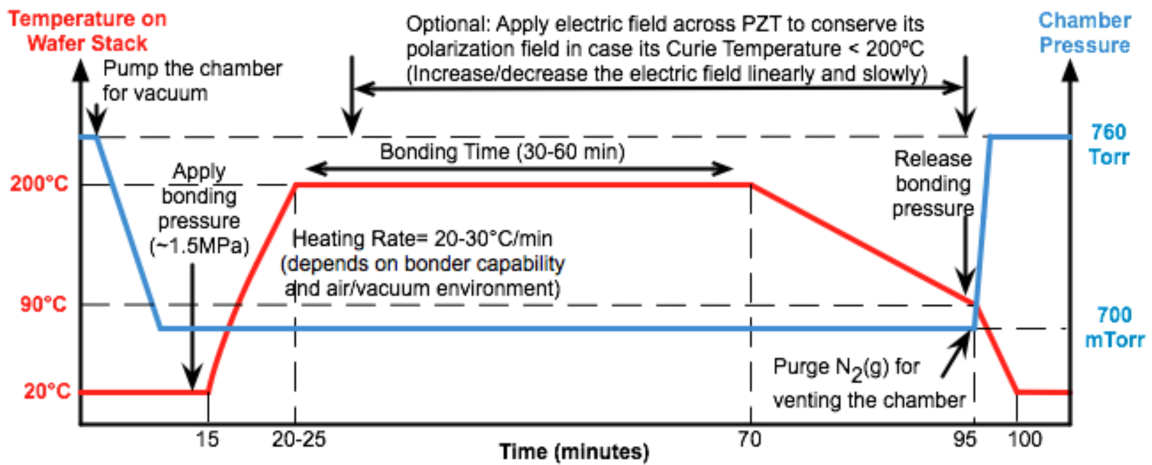


Fig.2.2 – Process profile for a typical parylene or AuIn bonding process

Any standard commercial 4-6 inch wafer bonder can be leveraged as a bonding setup for the required thermo-compression process (*Fig.2.3*). At the time of this study, polymer bonding was allowed only in specific equipment in the employed clean-room facility due to possible contamination concerns. Therefore, different commercial bonders are used for parylene and solder bonding experiments, EVG-501s bonder and Suss SB6-E or EVG-

510 bonders, respectively. For gold-indium bonding process, an important parameter of the bonder is its maximum heating rate, since it effects the formation of intermetallic compounds and the final bond layer strength. During a typical bonding process performed under vacuum, the measured maximum heating rates are ~30-40˚C/sec in Suss SB6-E and EVG-510 bonders, and 20-30˚C/sec in EVG-501s bonder.

In a typical bonding setup, a thick graphite chuck and a thin aluminum/carbon sheet are placed on the very top of the bonding stack, so that the applied force is distributed equally over the bonding samples and the detrimental effect of slight non-uniformities in the height profile, such as local hillocks, is avoided. Since large sheets (70mm on a side) or wafers (4-6 inch in diameter) of various bulk piezoelectric materials are commercially available, the bonding can be performed at either wafer-level or at die-level. For bonding at die-level, a silicon process wafer should be aligned to a DRIE-patterned silicon shadow mask on an alignment bond chuck, so that the diced PZT pieces can be precisely placed on the process wafer.

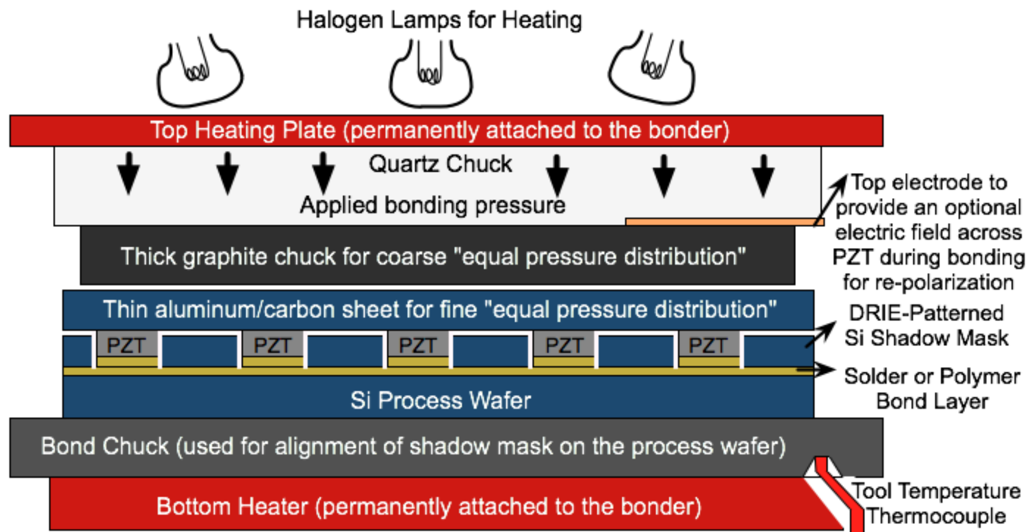


Fig.2.3 – Bonding setup used with a standard commercial wafer bonder

2.2.2. Gold-Indium Transient-Liquid-Phase Bonding

Transient Liquid Phase (TLP) solder bonding (or "diffusion soldering") is a different bonding technique than eutectic solder bonding, although both bonding processes may utilize the same materials in the bond layer composition. For the formation of a TLP bond, a low melting point interlayer metal (e.g. indium) is sandwiched in between two parent metals (e.g. gold) [Humpston04]. As the temperature increases, the molten interlayer conforms over the surface topology, and diffuses into and reacts with the parent

metals on both sides. Unlike in standard eutectic solder bonding, the solder exists in the liquid phase only temporarily, hence the name *transient liquid phase*. Depending on its composition, the final inter-metallic compound can have a re-melting point considerably higher than the bonding temperature. This characteristic feature differentiates a TLP solder bond from a standard eutectic solder joint, which still incorporates low melting point phases in its final form. This is because a standard solder alloy has an already established mix ratio of metals even before the bonding process, which only involves the melting and cooling of the solder joint without a change in its composition. In contrast, a low weight ratio of interlayer metal to parent metal is formed in a TLP bond during the bonding process, which is initiated at the low melting temperature of a pure interlayer metal that has not yet reacted with the parent metal to form the solder.

In the bond stack deposition to form a TLP bond, some additional layers are used in this study other than the parent and interlayer metals including (*Fig.2.4a*):

- Isolation layer to prevent an electrical short of the bond layer to the Si substrate,
- Adhesion layer between noble parent metals and the PZT/Si substrate,
- Barrier layer to prevent diffusion of solder into the adhesion layer,
- Protection layer against oxidation of the interlayer before the bonding process.

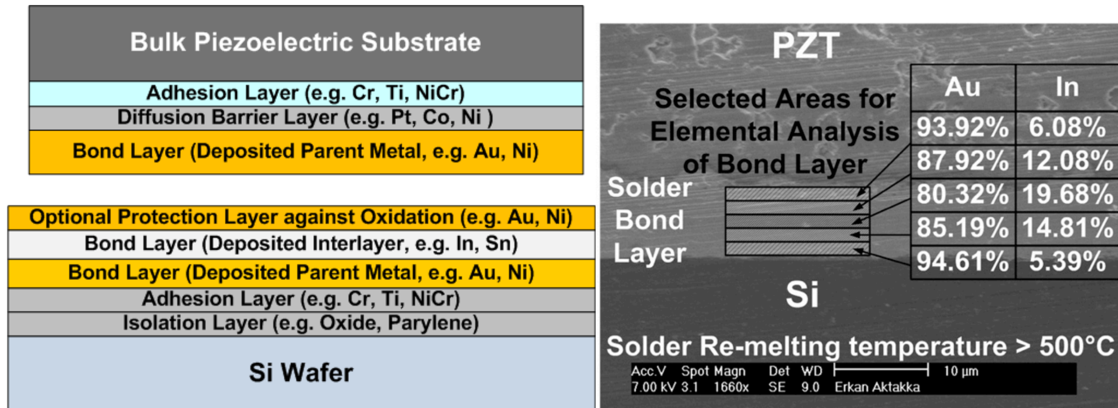


Fig.2.4 – a-) Deposited solder stack prior to bonding; b-) Elemental analysis of the final bond layer.

The same TLP bonding principle can be applied via different material compositions, such as Ag-In [Chuang02], Au-Sn [Welch04], Ni-Sn [Welch04], Ag-Sn [Humpston94], Cu-Sn [Bosco04] or Cu-In [Chen96], although the bonding temperature and the challenges related to form a void-free bond joint differ. In this thesis, AuIn TLP solder is studied for bonding of bulk PZT on silicon, since it offers both a low bonding temperature (200˚C) and also a strong void-free bond joint at the end (*Fig.2.5*). By proper

adjustment of deposited metal thicknesses, the AuIn interface between PZT and Si can be formed to have less than 20% indium existence by weight percentage in its final composition (*Fig.2.4b*). According to the Au-In inter-metallic phase diagram, this suggests a re-melting temperature greater than 500˚C [Welch07], which allows further high temperature processing of the wafer in the subsequent fabrication steps. This feature enables multiple bonding processes on the same wafer, for example for the formation of bimorph piezoelectric layers or wafer/die packaging, without compromising the integrity of the initial bond layer.

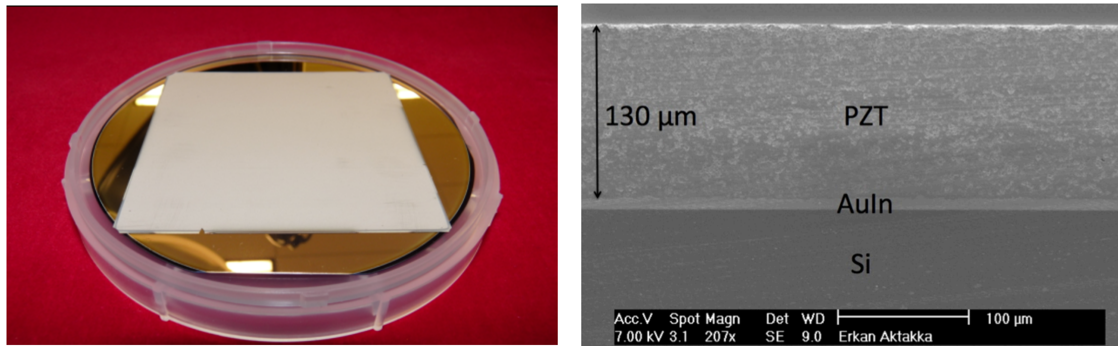


Fig.2.5 – Wafer-level solder bonding of a bulk PZT substrate on 4-inch silicon wafer.

Various bonding parameters and their effects on the formation of a strong AuIn TLP solder are discussed in *Table.2.2*.

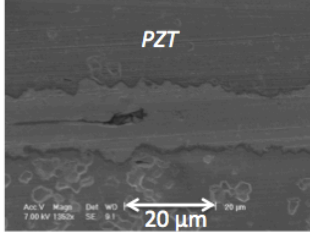
Table.2.2 – AuIn bonding parameters and their effects on bond formation

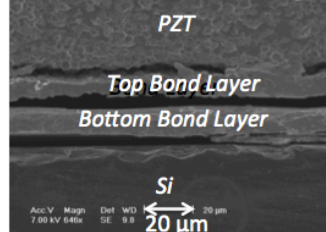
Variable	Value	Effect of the variable
Bonding Temperature	200˚C to 300˚C	An overshoot in bonding temperature enables increased wetting force in liquefied indium and thus allows better coverage over the rough PZT surface. In addition, it becomes easier to melt/crack the undesired intermetallic compounds, which are readily formed between indium and its protective thin Au layer prior to bonding. On the other hand, increased bonding temperature means higher residual stress at the end.
Bonding Time	30min to 60 min	Longer time for solid-state diffusion of In into Au will result in higher and homogenized Au/In ratio in the final bond layer, and increase the bonding strength and the re-melting temperature. However, excessive bonding time can result in diffusion of indium through the barrier and adhesion layers, de-wetting of the substrate surfaces, causing the bond joint to peel off from either or both of the substrates.

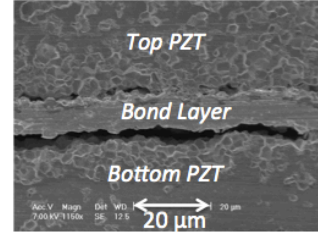
Bonding Pressure	1-2 MPa	The already-formed intermetallic compound between the deposited indium and its protective thin gold coating should be cracked with a high enough pressure in order to allow the spreading and diffusion of the liquefied indium on the bottom counter parent metal.
Atmospheric Medium	Vacuum or N_2 (g) ambient	Vacuum guarantees less O_2 (g) in the environment. However, this causes an uncharacterized offset in the temperature measurements done via thermocouples in the bonder due to the decreased thermal conduction.
In thickness (Interlayer Solder)	1 µm to 2 µm	It is desirable to have a high Au/In ratio in the final bond composition. However there is a minimum indium thickness required to slow down the intermetallic compound (IMC) formation during the initial temperature rise. Otherwise, pre-mature bonding occurs before the molten indium covers the whole surface, and thus voids remain at the interface.
Au thickness (Parent Solder)	0.5 µm to 5 µm	The Au thickness can be used to determine the final Au/In weight ratio to have a higher re-melting temperature. In addition, it can be used to define the bond layer thickness, which can also be exploited as a structural layer in the final device.
Pt thickness (Barrier Layer)	0 to 1000Å	Pt can be used as a diffusion barrier on the bulk PZT against diffusion of indium through the adhesion layer, and also to prevent possible out-diffusion of Pb from PZT into the bond joint. Both cases can cause de-wetting on the surface, which eventually results in the bond layer peeling off from the substrate.
Au thickness (Protection layer on top of the interlayer to avoid oxidation)	0 to 1000Å	Increasing the thickness ensures better coverage over the rough indium surface, and prevents oxidation of it. Meanwhile, an undesired intermetallic compound layer starts to form at this interface even at room temperature via solid-state diffusion prior to bonding, and it requires an increased force to break this layer during initial phase of the bonding process.
Vendor deposited nickel or gold layer on the PZT surface	Preserved / Etched away	There is a typically a deposited ~0.5 µm thick nickel layer on the PZT sheets purchased from Piezo Inc. Other companies also readily deposit either Ni or Au as the surface electrode. As observed during the bond strength experiments, weak points in the bond layer can occur at this interface due to poor adhesion.

Throughout the initial experimentations with AuIn solder bonding, various types of bonding failures are encountered. Their suggested causes and proposed solutions are listed in *Fig.2.6*.

Some of the encountered bonding failures during initial AuIn bonding experiments and possible solutions



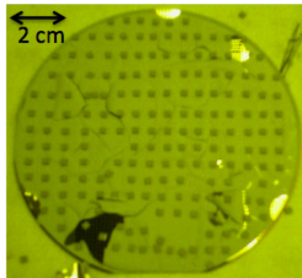


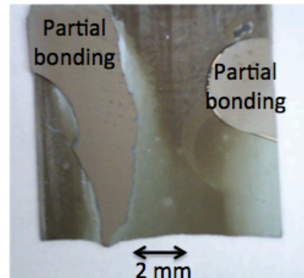


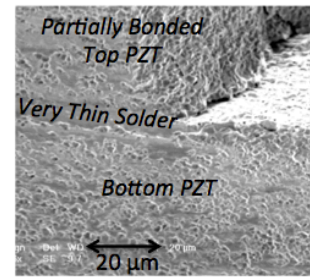
Voids or trapped dirt/particles in between the bonded samples
(1) O_2 plasma & pressurized N_2 flow on wafers before bonding
(2) Increase bonding pressure to break through IMC and InO_2

Bad adhesion of metals on Si/PZT
No bonding between layers at all
(1) Initial organic cleaning
(2) Adjust barrier thickness to prevent thru-diffusion of indium
(3) Increase bonding pressure

Cracking between PZT grains at surface close to the bond layer
(1) Soft scrubbing/cleaning of new wafers to remove loose grains,
(2) Decrease the bonding pressure,
(3) Polish the PZT wafer initially







Cracking of the AuIn stack on the silicon wafer due to high stress
(1) Decrease thickness of metal layers causing the high-stress
(2) Use electroplating instead of evaporation if thick Au needed
(3) Slower Cr deposition at low vac.

Oxidation of In before/during bonding,
De-wetting due to out-diffusion of Pb
(1) Perform bonding at vacuum,
(2) Decrease waiting time after indium deposition to prevent its oxidation,
(3) Use barrier to prevent possible Pb out-diffusion from PZT into bond joint

Non-conformal coverage of the bond layer on the rough PZT surface
(1) Increase the bond layer thickness,
(2) Increase heating rate or bonding temp. for conformal reflow of indium,
(3) Polish the PZT wafer initially to decrease the surface roughness

Fig.2.6 – Addressed bonding failures encountered during initial AuIn TLP solder bonding experiments. Possible causes of failure are typed in regular black font; possible solutions are typed in italic blue font.

2.2.3. Parylene Bonding

Previously, low temperature parylene bonding of two silicon wafers by microwave heating [Noh04b] and by thermo-compression 230˚C [Kim05] has been investigated. Parylene bonding can be achieved at a temperature between the material's glass transition temperature (110˚C) and melting temperature (290˚C), through the entanglement of softened polymer chains with an applied pressure. Due to its chemical inertness, parylene bonding interface has been shown to endure in various chemical solutions for very long times (>100 hours), in solvents such as photoresist-developers (MF319, AZ400K), alcohols used for organic cleaning (IPA, acetone), or even some acidic solutions (BHF) [Kim05]. In addition, compared to other polymer bonding techniques, parylene is

deposited as a solid at room temperature. Since there is no solvent involved in the deposition process, no voids occur in the bond layer due to out-gassing.

In this thesis, a parylene bonding process for integration of bulk PZT on silicon is developed at 200˚C with an applied pressure of 0.75 MPa, for possible applications that require a non-conductive bond layer as an alternative to soldering (*Fig.2.7*). Moreover, one can take advantage of the very low Young's modulus value of parylene (~1 GPa) in order to fabricate highly flexible piezoelectric resonators. Additionally, parylene's conformal deposition allows planarization of the rough PZT surface to a certain extent before bonding. In this study, different values between 2-4 μm have been used for the thickness of evaporated parylene on each bonding substrate, resulting in a bond layer with a thickness range of 4-8 μm, while no significant change is observed in the bond strength due to interface thickness. One can attain a thinner bond interface by planarizing the bulk PZT bonding surface via polishing prior to parylene evaporation. An increased bonding strength and reliability is observed on samples when the bonding temperature is raised to 300˚C (over the melting temperature of Parylene-C), although this causes an overflow of the excessive liquefied parylene layer towards the sides of the bonded sample, and a possible variation in the chemical and physical properties due to hypothetical change in cross-linking of polymer chains.

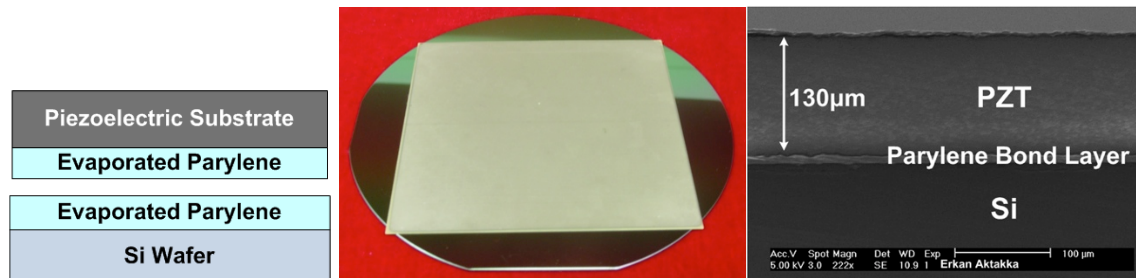


Fig.2.7 – Cross-sections of a 130-μm thick 70x70 mm^2 PZT wafer bonded on Si.

2.2.4. Bond Strength

The shear strength of the AuIn and parylene bond interfaces between bulk PZT and silicon substrates bonded at 200˚C is measured by applying an increasing lateral shear force on the bond layer until it fails (*Fig.2.8*), and the test results are summarized in *Table.2.3*. During the shear tests, more than 50% of the AuIn samples failed not at the bond interface, but due to a cracking that occurred either in the PZT or in the silicon substrate, which indicates that in these samples the bond layer had greater strength than

the bonded material itself. The average shear strength of AuIn is measured as 4.5 MPa, with a maximum value of 10 MPa on some samples. As expected, the parylene bond layer is observed to be not as strong as the solder bond, with a 1.5 MPa average shear strength. This value is in close proximity with strength (1-3 MPa) of thin (0.6 µm) parylene bond interfaces between bonded silicon wafers studied in [Kim05]. The measured bond strengths have proved to be high enough for the purpose of the processes as described in this thesis, since in the following sections the bond layers are demonstrated to endure during subsequent lapping or dicing-saw patterning of the top piezoelectric layer (*Fig.2.9*).

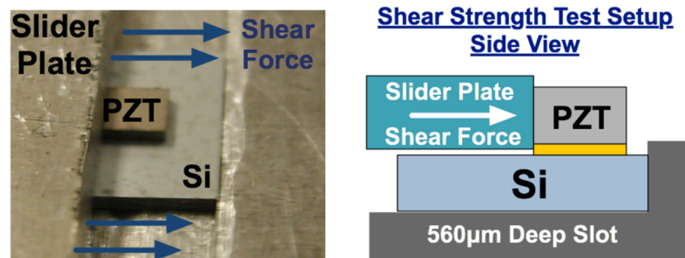


Fig.2.8 – An angled-view photo of the shear strength test setup and its side-view illustration

Table.2.3: Shear strength test results of PZT pieces bonded on Si.

	AuIn Bonding	Parylene Bonding
Number of test samples	112	43
Bond area	2 mm × 2 mm	3 mm × 3 mm
Average shear strength	4.44 MPa	1.47 MPa
Standard deviation	2.01 MPa	0.81 MPa
Max shear strength	10.05 MPa	3.40 MPa
Dominant failure mode during tests	Cracking in either PZT or Si (>50% of samples)	Peeling off of the bond joint from PZT or silicon

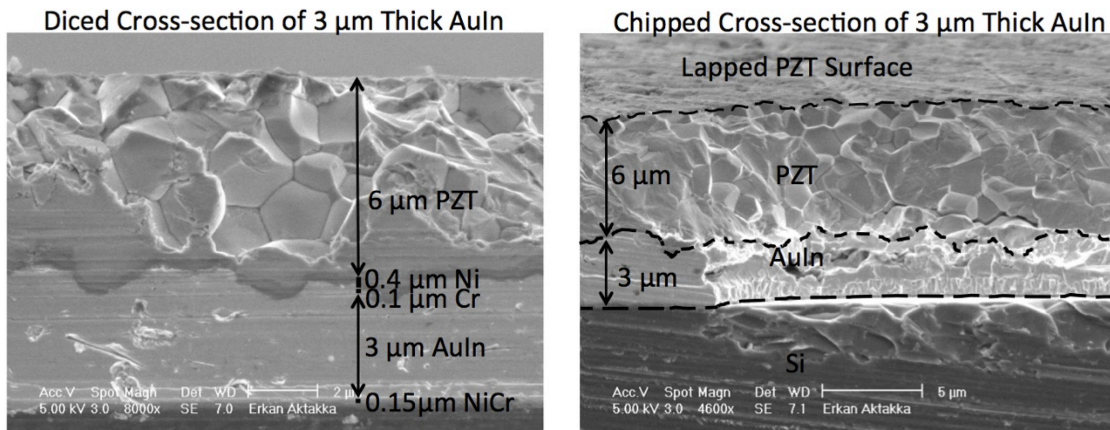


Fig.2.9 – Thinned-down PZT layers on Si with no mechanical damage at the bond interface

2.3. Wafer-level Thinning of Bulk Piezoelectric Substrates on Silicon

2.3.1. Loose and Fixed Abrasive Grinding

For realization of MEMS sensors and actuators out of bulk piezoelectric materials, it is essential to fabricate mechanically flexible thin structures at the required miniaturized scale. Therefore, it is highly desirable to thin a bulk piezoelectric ceramic, which is already bonded on silicon at either wafer or die level, from a thickness value of hundreds of microns down to 5-50 μm. The required subtractive machining can be achieved by purely chemical means such as isotropic dry and wet etching, by purely physical means such as water jet cutting, sand ablation and ultrasonic machining, or by a combination of physical and chemical reactions such as directional plasma etching (RIE) and chemical mechanical polishing (CMP). In this study, abrasive lapping/grinding is the preferred physical machining technology, since it provides a fast, wafer-scale, parallel processing capability with no chemical damage on the final thinned film. A simple description of lapping is the rubbing of a brittle work piece against a surface with an abrasive in between them. An enhanced lapping/polishing process is developed in this work, and it is characterized to yield highly uniform bulk piezoelectric layers with thickness values of down to 5 μm on a silicon wafer (*Fig.2.10*).

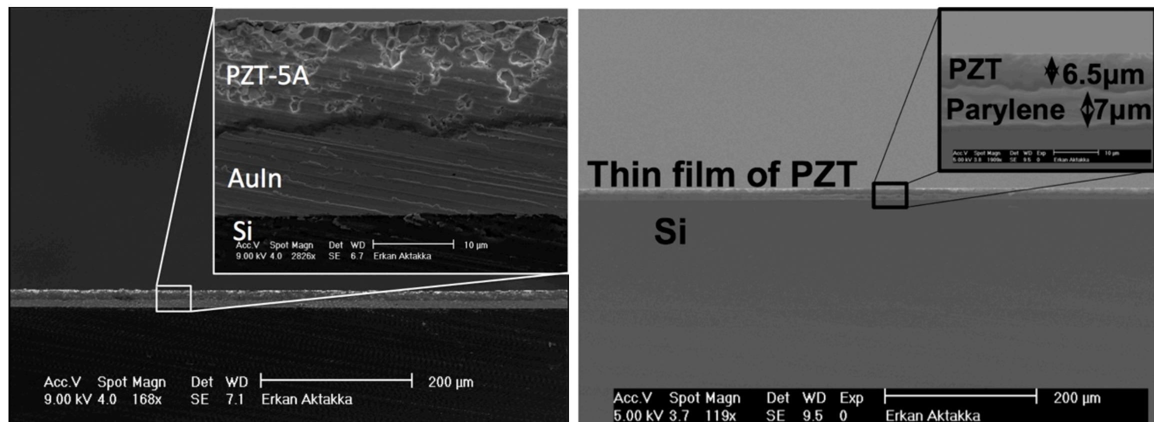


Fig.2.10 – Thinned PZT films on silicon with AuIn and parylene bond layers

For the initial thinning experiments, a *loose abrasive grinding (slurry lapping)* process is tested with a Logitech lapping/polishing tool, which consists of a copper lapping-wheel with diamond-steel cylinders for groove-conditioning, a wafer-retention jig with a vacuum chuck and a variable load piston, a control box for the wheel rotation speed, and a timing box to define the duration and interval of spraying slurry on the lapping wheel (*Fig.2.11a*). During the thinning process, water-based diamond slurry with

a particle size of 3 μm is supplied between the sample and the wheel, and a lapping rate of 4 μm/min is achieved.

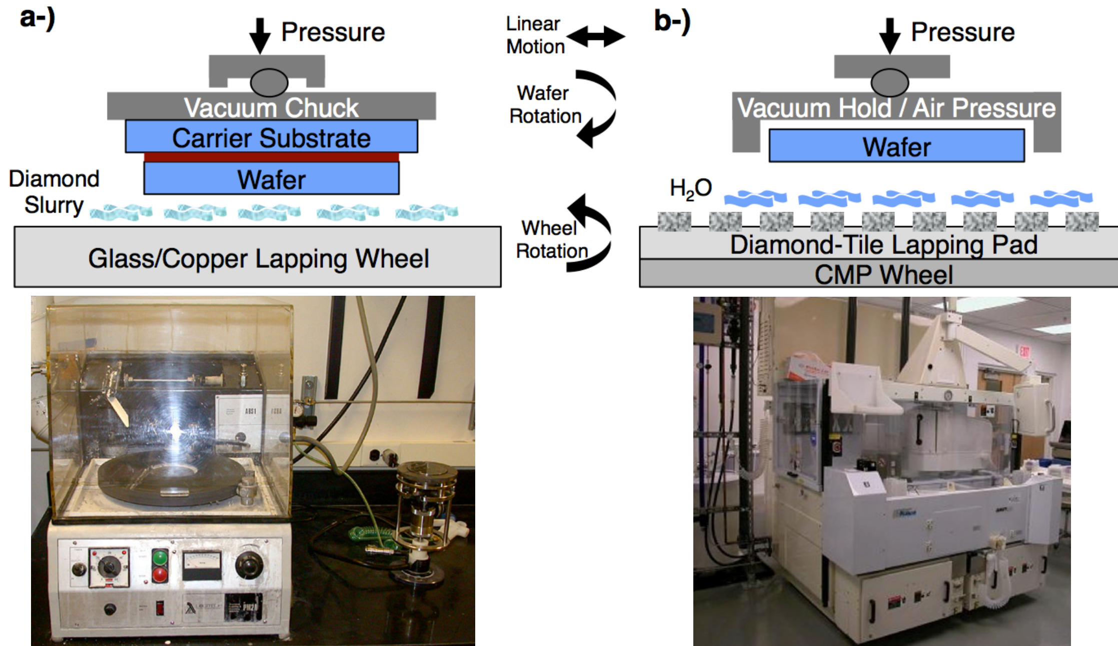


Fig.2.11 – a-) Loose abrasive grinding tool; b-) IPEC-472 CMP tool modified for fixed abrasive grinding.

In these initial lapping experiments, the uniformity of PZT film thickness is measured to vary between +/–4 μm to +/–15 μm on a 4-inch silicon wafer, and the lapping rate was found to be rather inconsistent due to the unsteady rotation-speed of the retention jig and non-uniform lapping pressure caused by imperfect surface flatness. These values can be possibly improved by checking/maintaining the flatness of the lapping wheel regularly, by using a high-quality retention jig to apply uniform pressure on the process wafer, and by keeping the rotation speed of the retention jig constant through some additional equipment. However, an important tool limitation on the surface flatness still arises from the lapper's wafer-handling capability. The slurry can often leak to in-between the process wafer and the vacuum chuck it is attached to, resulting in decreased flatness or detachment and slipping off of the wafer from the retention jig in the worst case. To prevent this situation, a 2-mm thick 4.5-inch glass substrate can be used as a wafer-carrier, where the process wafer is attached to one face of the glass carrier with a water/alcohol soluble wax and the opposing face of the glass carrier is mounted on the vacuum chuck. However, in this case, the non-uniform wax thickness and trapped air bubbles between the process wafer and the glass carrier will still have a detrimental effect on the wafer flatness.

After these initial experiments with the described standard *slurry-lapping* tool, a CMP tool (IPEC-472) is modified to utilize a 3M™ Trixact™ Diamond Tile pad (677XA SP520T) for *fixed-abrasive lapping*, in order to improve the PZT thickness uniformity, and lapping-rate consistency (*Fig.2.11b)*. In this setup, the composite pad is formed of structured small pellets incorporating 3 µm sized diamond particles embedded within a polymeric binder. Grooves between the pellets provide a means for the removal of the polishing debris and the distribution of excessive lubricant [Fletcher03]. During lapping, only de-ionized water is supplied to the pad in order to act as an aqueous lubricant and coolant with no external addition of any other abrasive mineral or chemical. Advantages of this lapping system are the highly uniform distribution of the abrasive particles, fine adjustment of the lapping pressure, the ability to apply backside air pressure on the wafer for fine pressure distribution and wafer-bowing correction, and a high level of control over the individual rotation speeds of the lapping pad and the process wafer.

2.3.2. Lapping Rate

The applied pressure and the rotation speeds on the modified CMP tool can be adjusted for faster lapping rates and higher lapping uniformity. For minimum physical damage on the final surface while keeping a high lapping rate, the optimum total pressure applied on a wafer is determined experimentally to be 1.5 psi for PZT-5A and PZT-5H polycrystalline, and 0.5 psi for PMN-PT single-crystalline ceramic substrates (*Fig.2.12*).

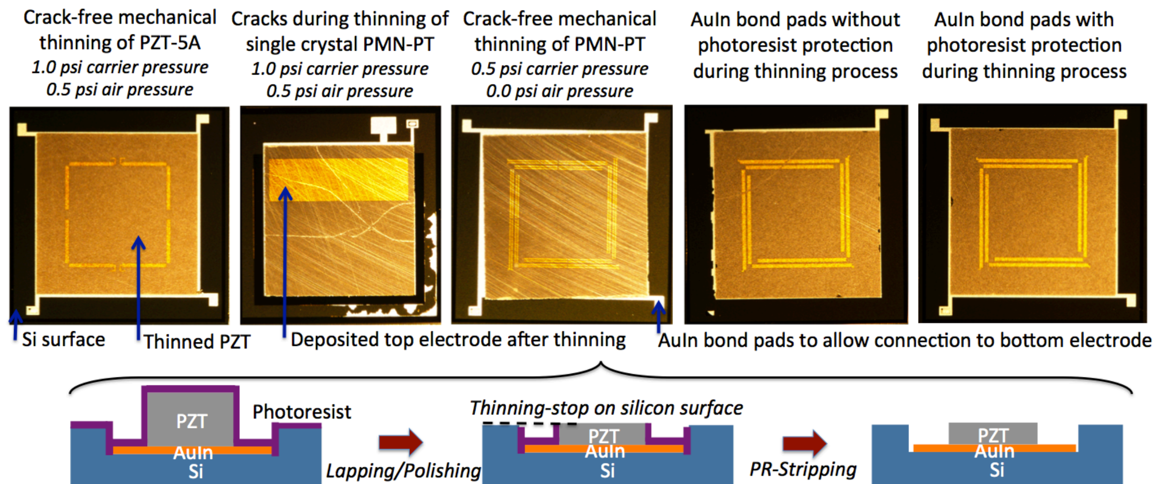
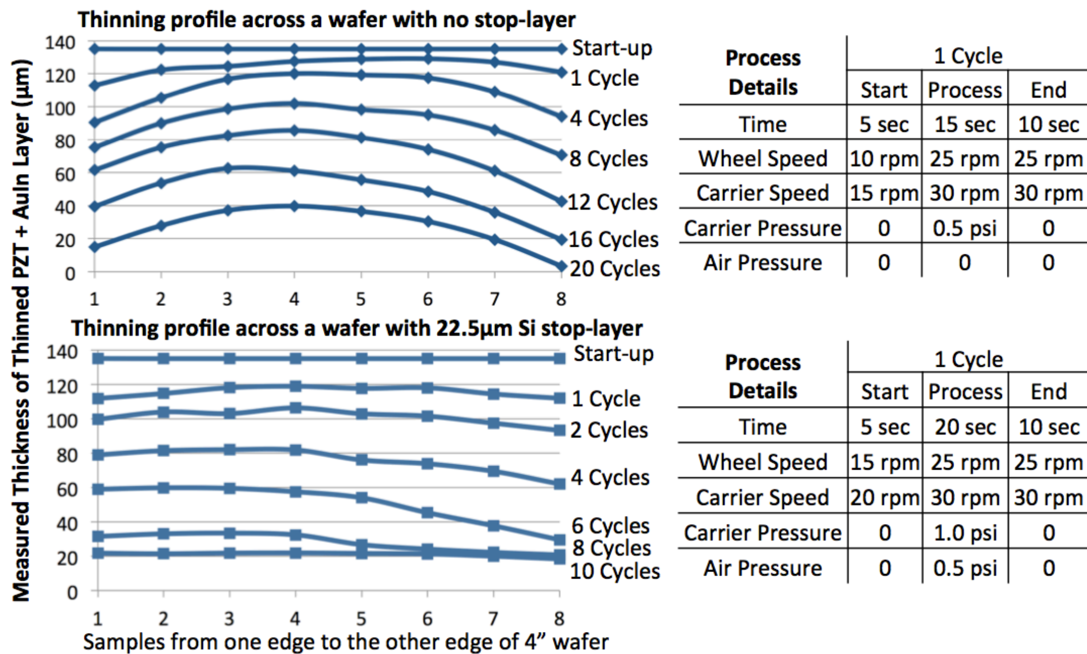


Fig.2.12 – Effect of applied pressure and protective photoresist coating in the lapping process.

A thin-layer (1-2 µm thick) of spin-coated photoresist helps to protect the substrate surface that is facedown against the lapping pad. If this measure is not taken, it is highly

possible to have some damage on the soft AuIn pads that provide electrical contact to the bottom electrode underneath the piezoelectric layer.

In order to improve the wafer-scale thinning uniformity, a new method is developed to precisely define the final PZT thickness on the wafer, by using the surrounding silicon-wafer surface (or any other deposited hard material on the wafer surface) as a thinning-stop layer. In this process, mm-scale diced PZT pieces are bonded inside cavities, which are previously patterned by dry etching of the silicon surface. During the lapping process, as the thinned-PZT thickness is reduced so that its top surface is level with the silicon surface, which is utilized as the thinning-stop layer in this process, there is an abrupt decrease in the lapping rate due to both increased lapping surface area and also increased hardness of the lapped material. This method can be leveraged to overcome the variation of thinning rate at different locations of the wafer, provide an effective method to achieve the target PZT thickness, and also improve the final wafer-level thickness uniformity.



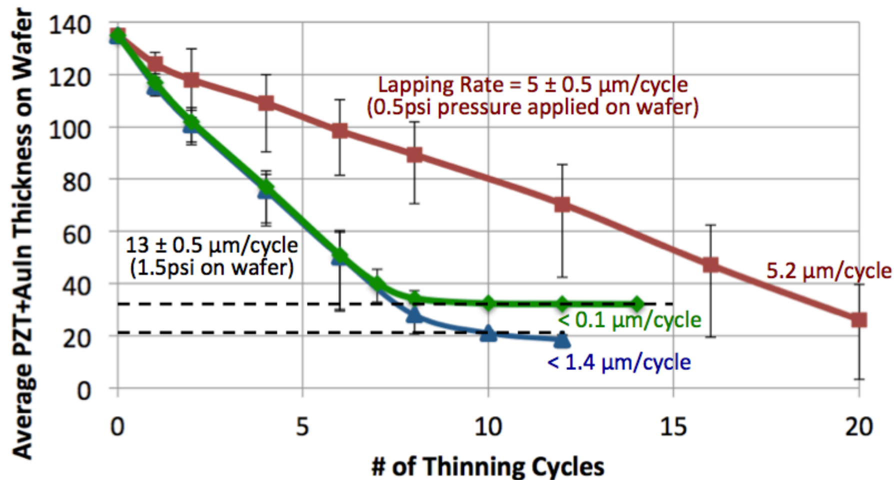
Process Details	1 Cycle		
	Start	Process	End
Time	5 sec	15 sec	10 sec
Wheel Speed	10 rpm	25 rpm	25 rpm
Carrier Speed	15 rpm	30 rpm	30 rpm
Carrier Pressure	0	0.5 psi	0
Air Pressure	0	0	0

Process Details	1 Cycle		
	Start	Process	End
Time	5 sec	20 sec	10 sec
Wheel Speed	15 rpm	25 rpm	25 rpm
Carrier Speed	20 rpm	30 rpm	30 rpm
Carrier Pressure	0	1.0 psi	0
Air Pressure	0	0.5 psi	0

Fig.2.13 – Effect of using the silicon surface as the lapping stop layer on wafer-level thickness uniformity

The effectiveness of the use of silicon wafer surface as a thinning stop layer is demonstrated in *Fig.2.13*. During the thinning process, a start phase and an end phase with zero lapping pressure is engaged for each lapping cycle to provide a low-acceleration smooth start-up, and to remove some of the final lapping debris from the wafer surface, respectively. The variation of the thinned PZT thickness on a typical wafer with no thinning-stop layer is observed to be as high as +/-18 μm, often due to an

increasing lapping rate towards the edges of the wafer. However, the use of the silicon surface as the thinning-stop layer decreases this non-uniformity 10-fold down to +/-1.8 µm. This stop-layer effect can be improved even further by incorporating a thin coating of a harder material on top of the silicon surface. A layer of 0.5-µm thick thermally grown silicon oxide on top of the silicon can decrease the lapping rate very effectively upon leveling of the PZT height with the Si/SiO_2 surface, and a ~100x reduction in the lapping rate compared to the initial value is attainable (*Fig.2.14*).



Wafer #	Stop layer	Height of the stop layer	Decrease in lapping rate when reaching stop layer	Wafer-level thickness uniformity	
				Max Deviation	Standard Dev.
■ 1	N/A	-	-	+/- 17.2 µm	11.8 µm
▲ 2	Si	22.5 µm	91.3%	+/- 1.8 µm	1.1 µm
◆ 3	Si/SiO_2	32.5 µm	99.2%	+/- 0.55 µm	0.28 µm

Fig.2.14 – Change in the lapping rates when the thinning stop layer is reached

2.3.3. Thickness Uniformity and Flatness

The final thickness of each thinned-PZT layer from all (52) dies out of a wafer, where the Si/SiO_2 wafer surface is used as the thinning stop-layer, is measured by a surface profilometer (Dektak™ 6M) with a linear scanning resolution of 0.1 µm (*Fig.2.15*). The standard population deviation is calculated as 0.28 µm, while the maximum deviation is measured as +/-0.55 µm. For further improvement of thickness uniformity, in addition to the lapping parameters one should also pay attention to the wafer-level variation in the depth of DRIE cavity and the flatness of the silicon substrate.

A single die from the thinned-PZT on silicon wafer shown in *Fig.2.1* is examined for the flatness of the piezoelectric layer across the length of the whole die (*Fig.2.16*). The average surface roughness (R_a) along a 4 mm scanning line on the PZT die is measured as

48 nm, with +/-200 nm maximum height/depth of hillocks on the PZT surface. A more accurate surface analysis over a 2D surface area is described in the next section.

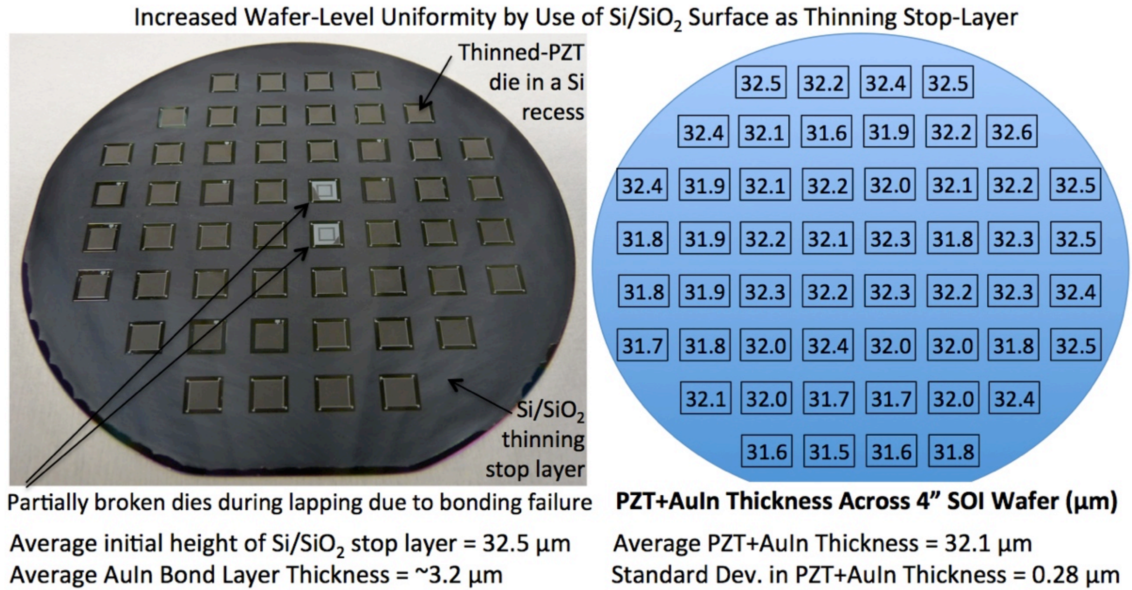


Fig.2.15 – Wafer-level PZT thickness uniformity measured with a Dektak-6M profilometer

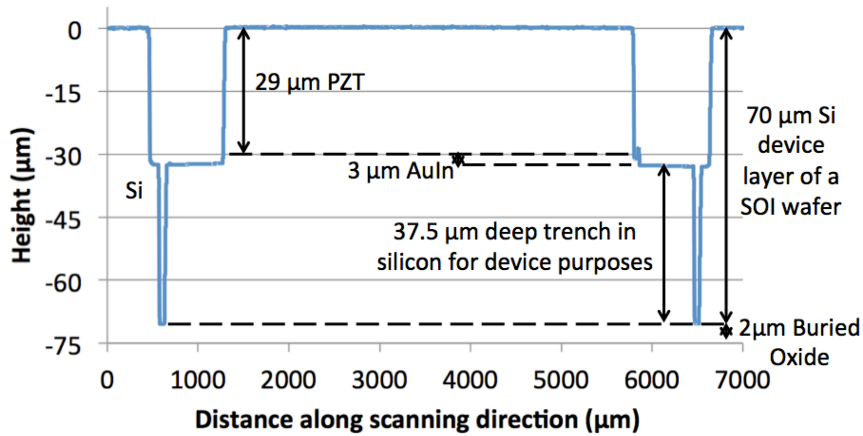


Fig.2.16 – Thickness profile over a single thinned-PZT die from a 4-inch wafer

2.3.4. Surface Roughness

A scanning white light interferometer is used over a thinned PZT film that is lapped with the slurry-lapping system. The arithmetic average surface roughness (S_a) is measured as 56 nm over 100 μm x 100 μm sample area with a profile range (S_t) of 356 nm (*Fig.2.17a*). Although this value is acceptable for most MEMS processes, it can be improved further if needed, by using a slurry with finer particle size. Still, the feasibility of obtaining an optically smooth surface (<20 nm roughness) is questionable due to the grainy structure of the original bulk PZT ceramic (*Fig.2.17b*).

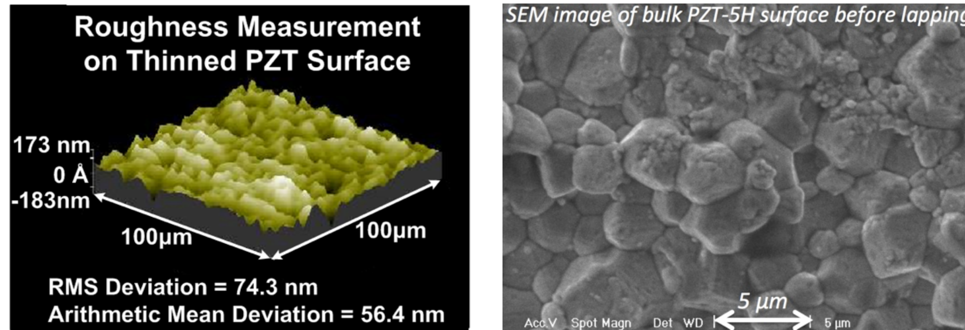
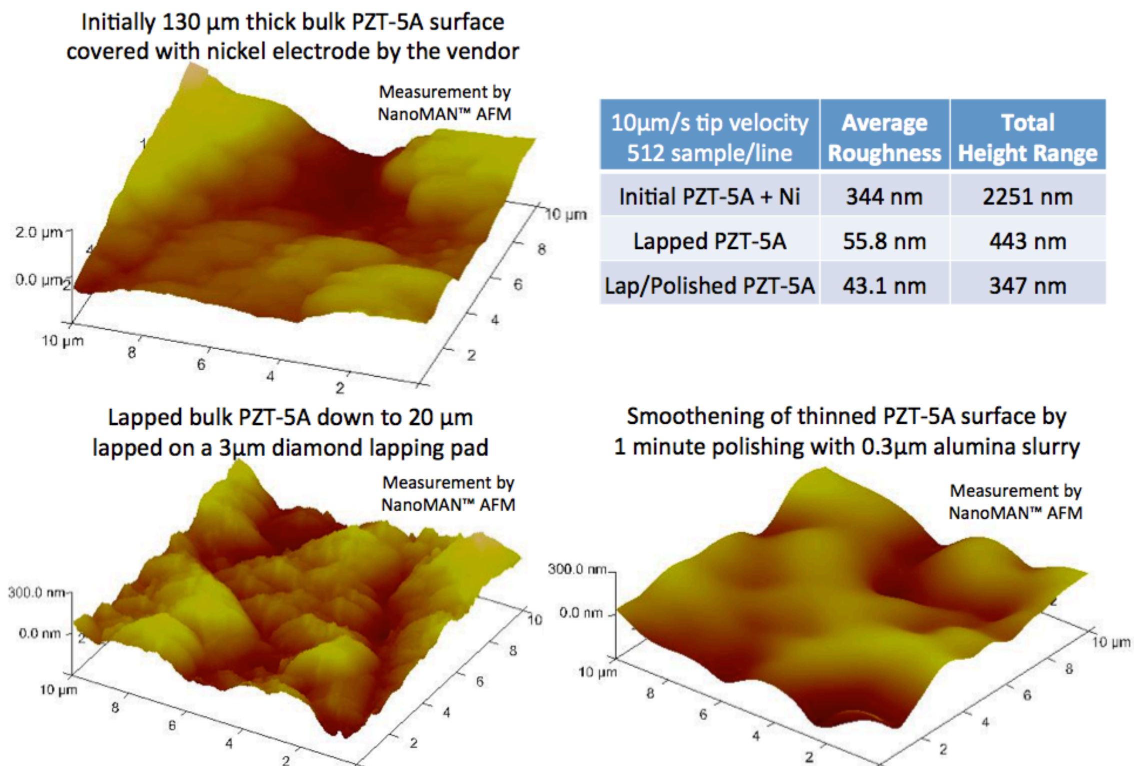


Fig.2.17 – a-) Surface roughness of lapped PZT-film by 3µm diamond slurry (interferometer measurement) b-) SEM image of the surface of a new purchased bulk PZT substrate indicating 3-4 µm grain size

In *Fig.2.18*, the measured surface roughness values are given for the original 130-µm thick bulk PZT substrate, a 20-µm thick PZT film obtained with the new fixed abrasive lapping system, and a 20-µm thick PZT sample that is polished with slurry lapping tool for 1 minute after the lapping process. The measurements are performed over 10 µm x 10 µm sample areas with an atomic force microscopy tool (NanoMAN™ AFM) operating in tapping mode. The use of AFM for surface roughness measurements is preferred over light interferometry due to measurement errors with the latter when sub-wavelength accuracy is demanded over high surface gradients [Gao08]. To obtain a smoother surface, one can lengthen the polishing process and use even a finer slurry size (0.1 µm).



10µm/s tip velocity 512 sample/line	Average Roughness	Total Height Range
Initial PZT-5A + Ni	344 nm	2251 nm
Lapped PZT-5A	55.8 nm	443 nm
Lap/Polished PZT-5A	43.1 nm	347 nm

Fig.2.18 – Measured surface profiles by tapping-mode AFM over 10 µm x 10 µm sample areas

2.3.5. Thinning Over Cavities

In order to form suspended structures such as beams or diaphragms out of the bonded and thinned piezoelectric layer, one needs to free the device layer from its bottom silicon substrate. One way to achieve this can be backside wet or dry etching through the whole silicon wafer. This method may not be preferable for all applications since deep wet etching requires precise process-timing, high alignment accuracy, and a protective coating on the front-side, while wafer-through DRIE is an expensive and time-consuming option for a production line. Alternatively, at the very beginning of the process one can wet or dry etch shallow cavities (with a depth of 1-100 μm depending on the application) on the front-side of the silicon wafer, and perform the bonding and thinning of the bulk piezoelectric layer on these pre-patterned features (*Fig.2.19*). In addition to the minimized etching time and increased patterning accuracy of the bulk-silicon, this method also facilitates easier packaging of the final device in the subsequent process steps since there is no need for extra coverage below the PZT layer.

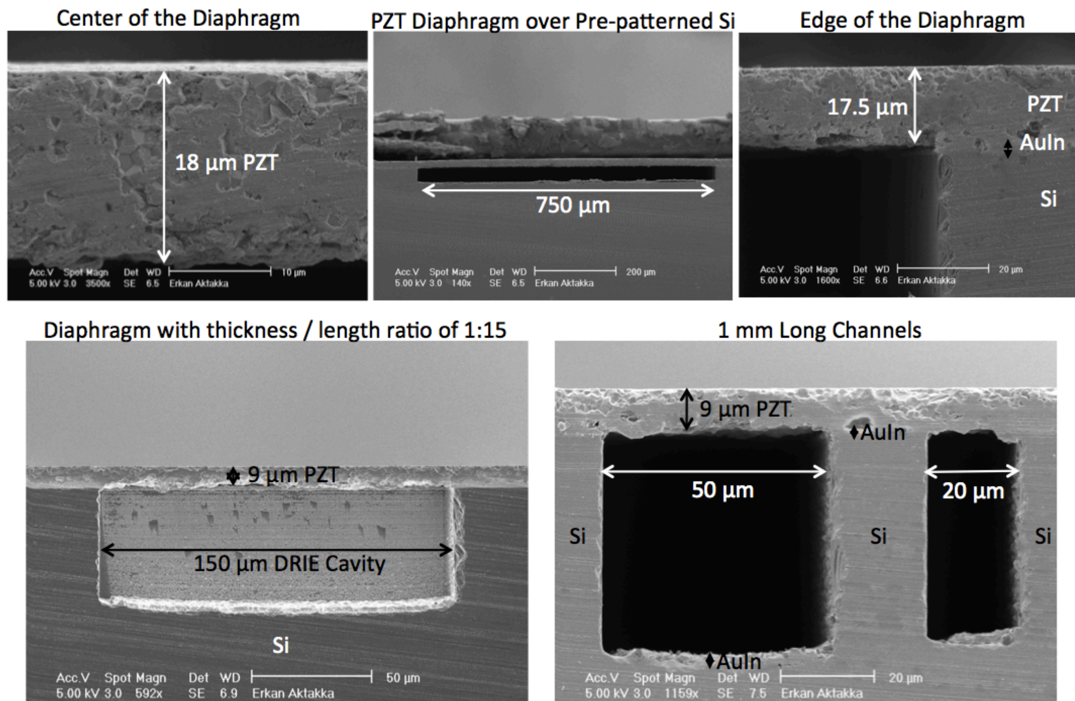


Fig.2.19 – Square diaphragms and micro-channels formed by bonding & thinning over pre-patterned Si.

In order to characterize the minimum diaphragm thickness and so the maximum aspect ratio (width/thickness) that can be obtained on a suspended structure fabricated with this method, 50 μm deep square cavities with different side lengths are DRIE patterned on a silicon wafer, and diced PZT dies are bonded and thinned down to various

thickness values on these pre-patterned silicon features. The minimum PZT thickness required for a crack/hole free diaphragm is noted for different diaphragm diameters (*Fig.2.20*). The main cause for cracking of a diaphragm is predicted to be the large bending of the diaphragm beyond its yield-point during the thinning process due to the applied lapping pressure and the size of slurry particles and lapping debris. Another cause can be the atmospheric pressure difference between the two faces of a diaphragm, since the AuIn bonding is performed under vacuum.

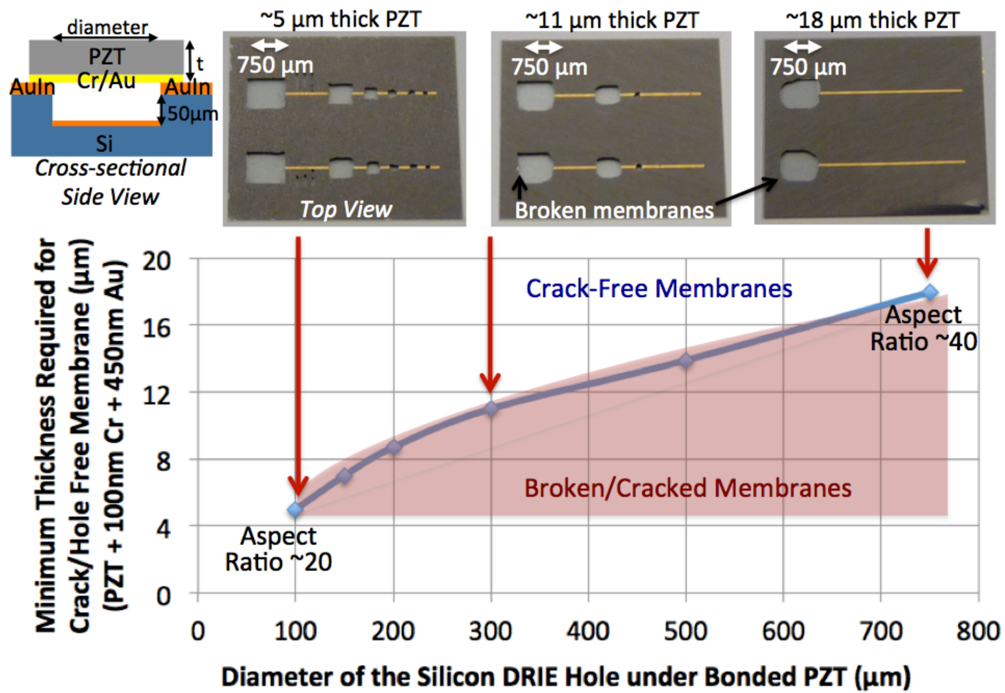


Fig.2.20 – Minimum PZT thickness that can be obtained over pre-patterned square cavities with different side lengths, by bonding and thinning the PZT substrate over 50 µm deep DRIE-machined Si features.

2.4. Patterning of Thin/Thick Film PZT Structures

2.4.1. Dicing and Piece-wise Bonding

Compared to wafer bonding, piece-wise bonding of a bulk PZT substrate on silicon can be beneficial not only for utilization of the surrounding silicon surface as the stop-layer during the subsequent thinning process, but it can also facilitate device fabrication at mm-scales without further patterning. The bonded and thinned rectangular structures can be easily shaped into diaphragms, bridge structures, or cantilever beams by subsequent bulk-Si micromachining (*Fig.2.21*). In this study, the cutting of the PZT wafer into mm-scale rectangular shapes is performed with a 110 µm thick nickel-hubbed dicing blade (Micro Automation 42525), and the dicing blade and the target material is

cooled with pressurized water flow during the process. The alignment of the diced pieces on the process wafer is achieved by using a silicon shadow mask, which incorporates DRIE-etched wafer-through holes having lateral dimensions of the corresponding PZT pieces with an additional 25-50 µm tolerance on both width and length.

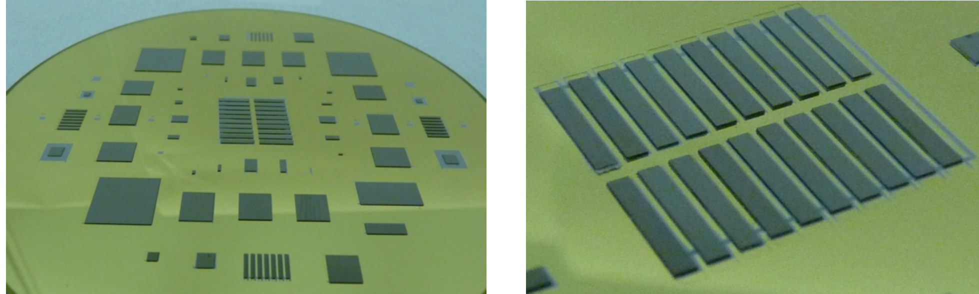


Fig.2.21 – Bonding of mm-scale PZT pieces on 4-inch Si wafer via alignment through a shadow mask

Previous studies to pattern thick PZT films for fabrication of piezoelectric devices include ultrasonic machining [Li05], laser ablation [Desbiens07], FIB milling [Marshall04], reactive-ion-etching [Jung01], and wet-etching [Wang01]. However, each of these methods has its own drawbacks such as micro-cracks due to mechanical machining, unintentional v-shaped cutting, impractically long processing time, or intolerable under-cutting. In contrast, the fabrication of simple rectangular structures with a feature size > 200 µm can be enabled by precision dicing before bonding, which eliminates the necessity of further chemical/thermal patterning of PZT on silicon. Aligned bonding and thinning of 200-500 µm wide and 130 µm thick PZT samples on a Si wafer is demonstrated (*Fig.2.22)*. Although the manual handling of the diced samples at this scale is challenging, it is possible to perform the alignment of these pieces on the shadow mask by either an automated pick-and-place equipment [Weck04] or a parallel micro-assembly technique by leveraging electrostatic force fields [Bohringer98] and non-contact levitation between the pieces and the process wafer [Vandaele05].

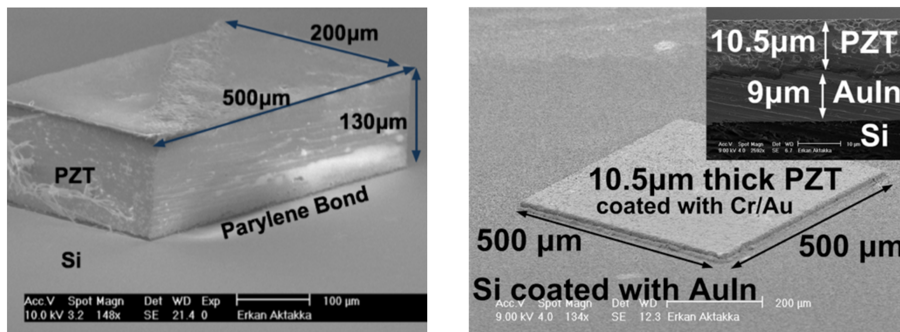


Fig.2.22 – Aligned bonding and thinning of 500µm×500µm PZT pieces on silicon

In addition, the dicing saw patterning of a bulk piezoelectric substrate can also be achieved after the bonding process on silicon, in order to obtain arrays of micrometer-scale rectangular structures (*Fig.2.23*). During the characterization runs, a 35-μm thick dicing-blade with 6-μm sized diamond particles embedded in its nickel-alloy matrix is used for minimum mechanical damage and higher resolution, and the optimum linear cutting speed is found to be 2.5–5.0 mm/sec with a spindle speed of 34,000 rpm. The minimum feature size is limited not only by the blade thickness and the stage accuracy, but also by the cutting depth since the mechanical susceptibility of the patterned structures increases with their aspect ratio. A 130-μm thick PZT layer can be patterned into 40-μm wide columns or 70-μm wide pillars, and these experimentally determined dimension limits are expected to go even lower for thinner PZT structures, as mechanical wobbling and vulnerability of the columns/pillars during dicing become less of a problem at low aspect ratios. Although this patterning technique brings its own subsequent processing challenges (e.g. deposition/ patterning of top/side electrodes, or possible disconnection of the bottom electrode due to unintentional cutting into the bottom substrate), it can still find good use in certain applications. For instance, the illustrated high aspect-ratio PZT micro-channels can be utilized in drop-on-demand ink-jet heads for multiple droplet generation/steering/ dispensing through actuation of PZT walls, while PZT pillar arrays can be used in high-resolution ultrasonic applications.

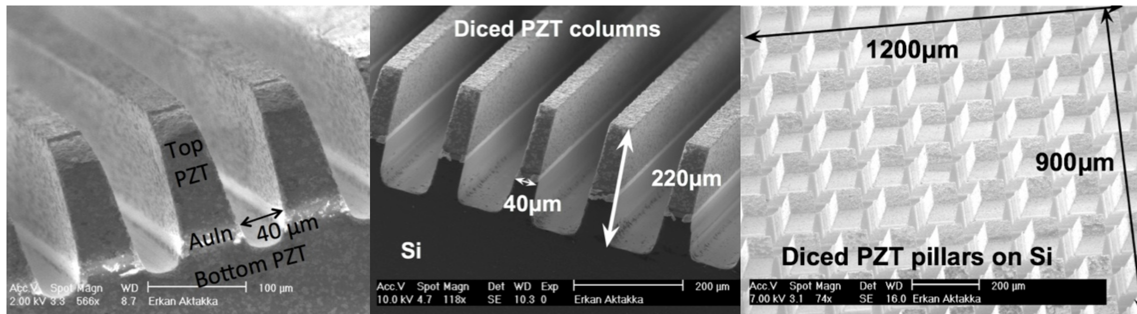


Fig.2.23 – Dicing saw patterning of thick PZT structures such as rectangular columns or pillar arrays.

2.4.2. Laser Micro-machining

In order to realize fabrication of piezoelectric devices with complex shapes, nano-second and femto-second laser ablation experiments are performed on bulk PZT. Laser ablation enables the removal of the target material from a solid/liquid interface by evaporation/sublimation due to the absorbed laser energy. Compared to RIE, milling, and ultrasonic machining of PZT, laser ablation is beneficial due to fast prototyping, ability to

cut through thick substrates, and minimized mechanical/thermal damage, which can degrade piezoelectric properties.

Initial experiments are performed with an Nd:YAG nano-second laser (λ = 1064 nm) with Gaussian spatial beam intensity profile. PZT bimorph samples of thickness 270 and 380 μm are tested, with the aim of cutting a spiral cantilever beam with straight sidewalls. During these experiments, the linear scan speed is kept at 4-6 mm/s with 60-65 passes, and laser power at 350-750 mW with a 30 μm spot size, corresponding to a laser fluence of 180-380 mJ/cm^2. The laser fluence defines the energy delivered to the work material per unit area per laser pulse, and it is generally used for characterization of the ablation effect on the work material per absorbed energy (*Fig.2.24*).

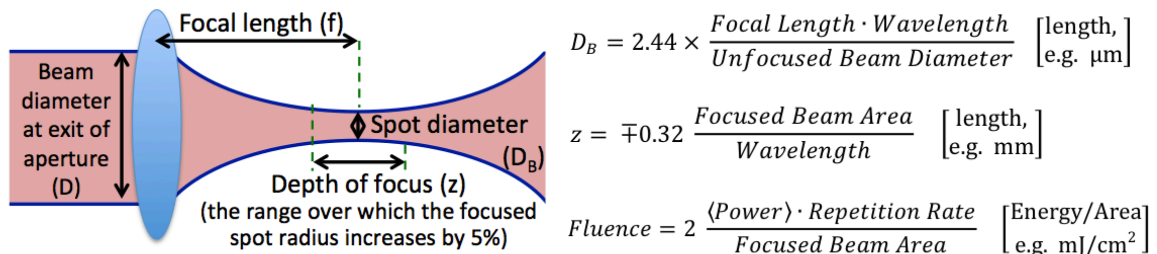


Fig.2.24 – Definition of basic important parameters used in laser machining of materials

Because of the observed large melt-zone area and *recast layer* built on the side-walls in the nano-second laser cuts, the rest of the experiments are completed using a Ti-Sapphire femto-second laser (λ=780 nm) with 150 fs pulse duration, 1 kHz pulse repetition rate, and an average power output up to ~800 mW (*Fig.2.25*). With this setup, the shorter pulse duration minimizes the thermal conduction to the surrounding material while the maximum peak power is applied to the ablated region. In addition, the high pulse repetition rate prevents cooling of the ablated region, so that more of the incident radiation is used for material removal instead of thermal conduction to the surroundings. Therefore, the combined effect of short pulses with high repetition rate enables more efficient ablation with a minimized melt-zone area compared to a nanosecond pulse laser. During the ablation, the products of the chemical reaction produce a plasma-like substance, which scatters the incident beam causing a larger ablation region than intended, and also deposits over the surrounding work material forming a recast layer. In this study, to minimize these effects, this plume is cleared from the work area by vacuum and pressurized air flow (preferably nitrogen gas).

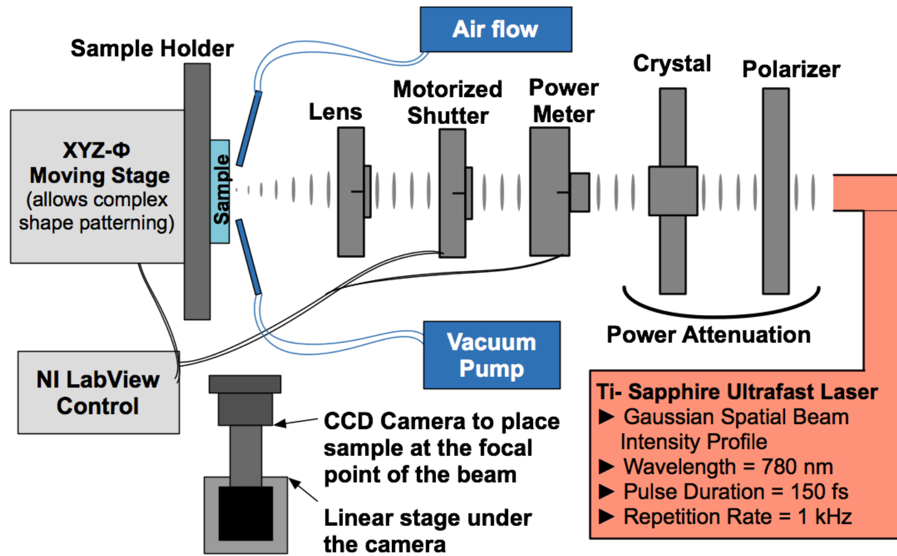


Fig.2.25 – The femto-second laser setup used for complex-shape patterning of PZT.

In order to define the range of applicable power values on the work material, an ablation threshold test is performed at 20 mm/sec linear scanning speed, and the effect of individual laser pulses on the surface of bulk PZT-5A is observed (*Fig.2.26*). Over ~300 mW, there is a clear increase in the diameter of the ablation region and an optically observable damage towards the sides of the cut line, while under ~20 mW no ablation is observed with both optical and scanning electron microscopes.

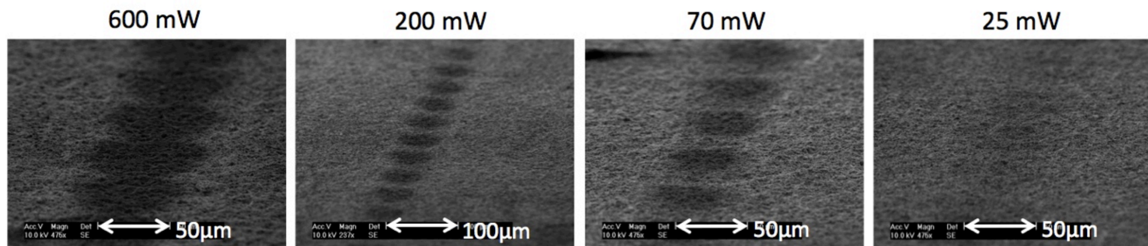


Fig.2.26 – SEM images from the laser ablation threshold test on bulk PZT-5A surface.

In order to cut complex shapes other than linear cuts, to maintain a constant scanning speed throughout the entire trajectory path, and to have a control over the shutter opening/closing times on the trajectory, a LabVIEW program is created by leveraging the vendor-defined LabVIEW commands for the XYZ-ϕ motion stage, on which the sample is mounted. This program also provides the capability for automated cuts of any complex-shaped pattern in a 2D array over a 4-inch wafer area, and enables automated focus adjustment during ablation of thick substrates to prevent excessive slope on the sidewalls.

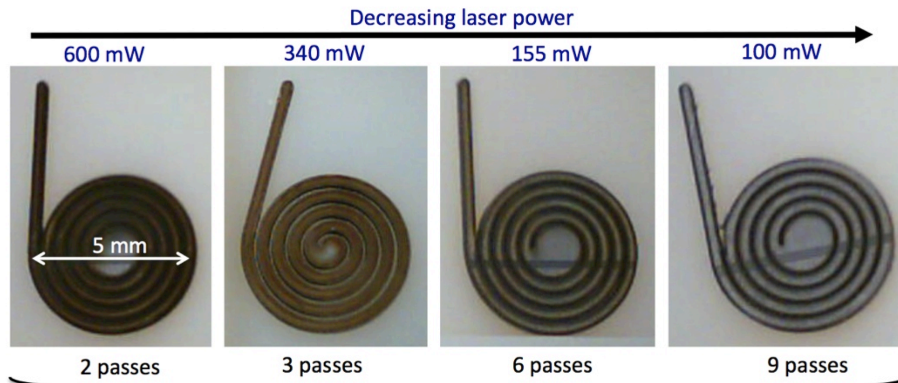


Fig.2.27 – Thick bimorph PZT spirals cut at varying power levels

Laser fluence and linear scan speed along the pattern trajectory are optimized for minimum damage of the material surface and for an acceptable processing time, while the beam spot size is kept at 55 µm (*Fig.2.27*). The best ablation profile is obtained by using low laser fluence (125 mJ/cm^2) close to the PZT-ablation threshold level (~25 mJ/cm^2) at low linear scanning speed (100 µm/sec) for fewer passes (3-4 passes) over the same cutting path on a 270 µm thick sample. Depending on the required ablation depth, a lower laser fluence and a faster scanning speed can also be preferred for bonded & thinned PZT films with smaller thickness values than the ones tested here.

Minimum number of passes along the same trajectory to cut through 270 µm thick PZT substrate **(passes)**
Required processing time to cut 270µm thick spiral beam with 42.5 mm trajectory length **(min)**

	Laser Power (mW)	291	145	102	73	44	Ablation Threshold 29
	Laser Fluence (mJ/cm²)	250	125	88	63	38	25
Linear Scanning Speed (µm/s)	800	10 passes 9 min	17 passes 15 min	25 passes 19 min	40 passes 35 min	120 passes 106 min	—
	400	4 passes 7 min	9 passes 16 min	12 passes 21 min	19 passes 34 min	55 passes 97 min	—
	200	2 passes 7 min	5 passes 18 min	7 passes 25 min	11 passes 39 min	26 passes 92 min	—
	100	2 passes 14 min	3 passes 21 min	4 passes 28 min	6 passes 42 min	13 passes 92 min	—
	50	2 passes 28 min	2 passes 28 min	2 passes 28 min	3 passes 42 min	7 passes 99 min	25 passes 353 min
	25	—	—	—	2 passes 57 min	5 passes 141 min	17 passes 481 min
	13	—	—	—	1 passes 57 min	3 passes 170 min	21 passes 1188 min
	7	—	—	—	1 passes 101 min	2 passes 202 min	8 passes 808 min

Replication rate of laser pulses = 1 kHz
Focal length = 20 cm (depth of focus = 1.9 mm)
Diffraction limited beam diameter = 55 µm (spot size)

Decreasing observed surface damage
Increasing required processing time

None or very slow ablation of the material

Fig.2.28 – Effect of the laser power and scanning speed on the required processing time.

With the optimized parameters, 380-μm thick bimorph PZT/Brass/PZT spiral cantilever beams are machined via the described femto-second laser setup, causing much less thermal damage on the material surface, minimizing the recast-layer formation and providing straighter wall edges compared to the best profile obtained during initial nano-second laser tests (*Fig.2.29*). These spiral cantilever beams are used for non-resonant energy harvesting from flying insects as part of a collaboration project with other research groups aiming to hijack the neural systems of insects and build energy-autonomous locomotion control systems for them (see Appendix-A). Additionally, clamped-clamped spiral beams are designed, simulated, optimized and fabricated to build a piezoelectric Parametric Frequency Increased Generator (PFIG), in order to harvest low-frequency, high-amplitude vibration for wearable electronics (see Appendix-B).

In addition to thick PZT substrate machining, the developed laser-cutting technology can also be applied to thinned-PZT films on silicon. In this case, the decreased ablation-depth due to thinned-PZT thickness, e.g. 5-10 μm compared to >100 μm for a bulk-PZT substrate, would lower the required processing time, and also result in less thermal damage of the surrounding material. In addition, the spot size of the laser can be decreased down to <10 μm depending on the design requirements, by using a combination of differently sized focal lenses.

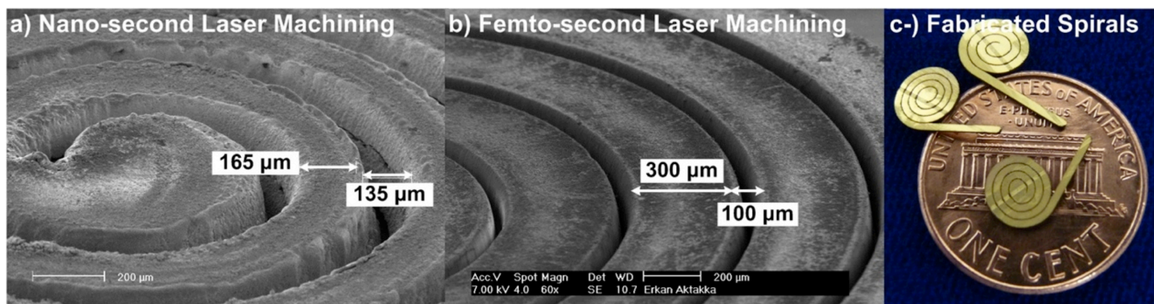


Fig.2.29 – Complex shape and high-aspect ratio laser-cut of 380μm thick PZT by laser ablation

2.4.3. Wet Etching

Although complex patterning of bulk PZT is possible with the developed laser machining technique, it is also desirable to have a patterning method that uses a parallel process to increase the throughput in bulk manufacturing. Wet etching is one of the most preferred patterning methods in the micro-machining industry for various materials, since it is a very cost-effective and fast process, and also enables lithographically-defined features. Wet etch patterning of thin PZT structures have been studied throughout the last

decade, especially on sol-gel spin coated 1-2 μm thick films, by use of different mixes and ratios of acidic solutions, such as HF, HCl, CH_3COOH, and HNO_3 (*Table.2.4*).

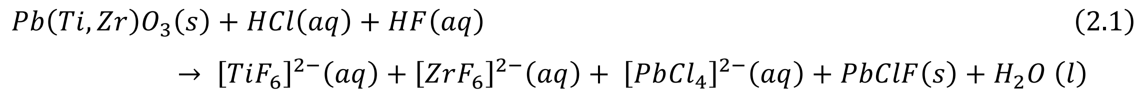
Table.2.4 – Selected literature on wet-etch patterning of thin/thick PZT films

Reference	***Etching Solution, Mix Ratio & Temperature***	***Etched PZT Thickness***	***Etch-rate (μm/min)***	***Undercut Ratio***	***Residues or Mask Delamination***
[Wang01]	HCl at 45°C	2 μm (sol-gel)	1	10:1	Masking
	HF at 25°C	1 μm (sol-gel)	0.15	2:1	Masking / Residue
	0.34%HF 5%HCl 94.7%H_2O	2 μm (sol-gel)	0.20	3:1	Masking / Residue
	BOE (+ 30sec dip in HCl)	2-5 μm (sol-gel)	0.13	2:1	Residues removed at the second step
[Zheng04]	BHF : 2HCl : 4H_2O (+ 15sec dip in 2HNO_3:H_2O)	1 μm (sol-gel)	0.78	5.5:1	Residues removed at the second step
	BHF : 2HCl : 4NH_4Cl : 4H_2O (+ 15sec dip in 2HNO_3:H_2O)		0.96	1.5:1	Residues removed at the second step
[Jeon04]	4BHF : 25HCl : 50H_2O	0.5 μm (sol-gel)	0.25	2.5:1	N/A
[Dauchy07]	0.5%HF 5%HCl 95%H_2O at 60°C (+ final ultrasonic cleaning)	20-30 μm sol composite	2.5-4.2	1-2:1	N/A
[Cai10]	34ml mix of 5HCl : 5HAc : 20H_2O : HF : 2H_2O_2 : HNO_3 + 0.5g EDTA + 0.5g NH_4F	0.2 μm (sol-gel)	0.2-0.5	0.9:1	N/A
[Che11]	BHF : CH3COOH : 8H_2O	1 μm (sol-gel)	-	-	Dense residue
	BHF : 4HCl : 4H_2O		> 2	-	Residue
	BHF : 28HCl : 70H_2O		> 2	3.5:1	N/A
	BHF : HNO_3 : 20H_2O		3.3	1.1:1	N/A

Minimizing the undercut distance during wet etching is especially important for the presented bulk-PZT technology since the piezoelectric thickness values are relatively high compared to previously studied sol-gel layers, mostly in the 5 to 25 μm range. As a way to avoid resist-mask delamination during etching, a common reason for large undercuts, it is advisable to use thick photoresist-masks (>10 μm), and also employ diluted and buffered acids, e.g. using buffered HF instead of straight HF, or in an analogous manner adding NH_4Cl to HCl to control Cl^- ion concentration. In addition, one can perform the process at a higher solution-temperature, in order to benefit from increased vertical/lateral etch rate ratio and a higher etching rate overall [Cai10].

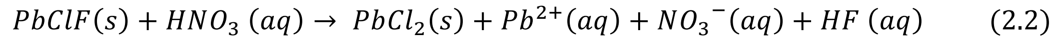
From the analysis of previous literature, it is concluded that using a single chemical reagent is not viable for etching through the complex composition of PZT, since it causes

unreliable etching rates, increased undercuts and residues on the exposed surface. For instance, the use of HF as the only reagent in the etching solution results in Pb_5ZrF_{14} and other lead halide residue formation on the etched surface [Wang01]. Although a second step for final surface cleaning by brief HCl or HNO_3 dips can be added into the process, this is not a suitable method for thick film patterning due to the persistent problems of non-uniform etching and the resulting large undercut. Instead, a mix of reagents is necessary to establish uniform etching rates on the different components of the material, such as using HF for ZrO_2 and TiO_2 etching while counting on HCl for TiO_2 and PbO etching [Zheng04].



$$Pb(Ti,Zr)O_3(s) + HCl(aq) + HF(aq) \rightarrow [TiF_6]^{2-}(aq) + [ZrF_6]^{2-}(aq) + [PbCl_4]^{2-}(aq) + PbClF(s) + H_2O\ (l) \quad (2.1)$$

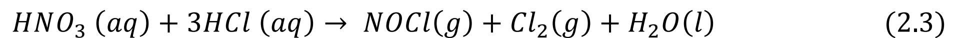
In this case, the mix ratio of the solution can effect whether PbClF(s) residue precipitates or not on the exposed regions during the reaction. Consequently, a final surface cleaning with HNO_3 might still be required. This cleaning step has been cited as conversion of the non-soluble PbClF(s) into the slightly soluble $PbCl_2$ (10 g/L at 20°C).



$$PbClF(s) + HNO_3\ (aq) \rightarrow PbCl_2(s) + Pb^{2+}(aq) + NO_3^{-}(aq) + HF\ (aq) \quad (2.2)$$

In this study, the wet etching of 5-20 μm thick bonded and thinned bulk PZT substrate is studied with a dilute acid mix, incorporating 100 ml BHF : 100 ml HNO_3 (67%) : 100 ml HCl (38%) : 1800 ml H_2O. Despite the dilution, this solution can etch away a wide-variety of metals on the exposed regions, but in this case the bottom electrode is still safely preserved after the PZT etching process due to the > 3 μm thick AuIn layer.

The mix of nitric and hydrochloric acids form a diluted *aqua regia* solution, which has an equilibrium-limited self-decomposition. Thus, the mixture should be freshly mixed, as the volatile reaction products escape from the solution, and the reactive ion concentration decreases in time.



$$HNO_3\ (aq) + 3HCl\ (aq) \rightarrow NOCl(g) + Cl_2(g) + H_2O(l) \quad (2.3)$$

The freshly prepared solution is heated to 35-40°C in order to increase the etching efficiency, and also to yield a better undercut profile by increasing the vertical/lateral etching ratio. *Fig.2.30* shows measurements done via a Olympus LEXT Interferometer on the etching profile of an 8-μm thick bulk-PZT square capacitor with 400 μm width. The

measured undercut ratio is more than 1.5:1 (lateral undercut to etch depth ratio), due to the fast lateral travel of solution through the grain boundaries, and the over-etching time.

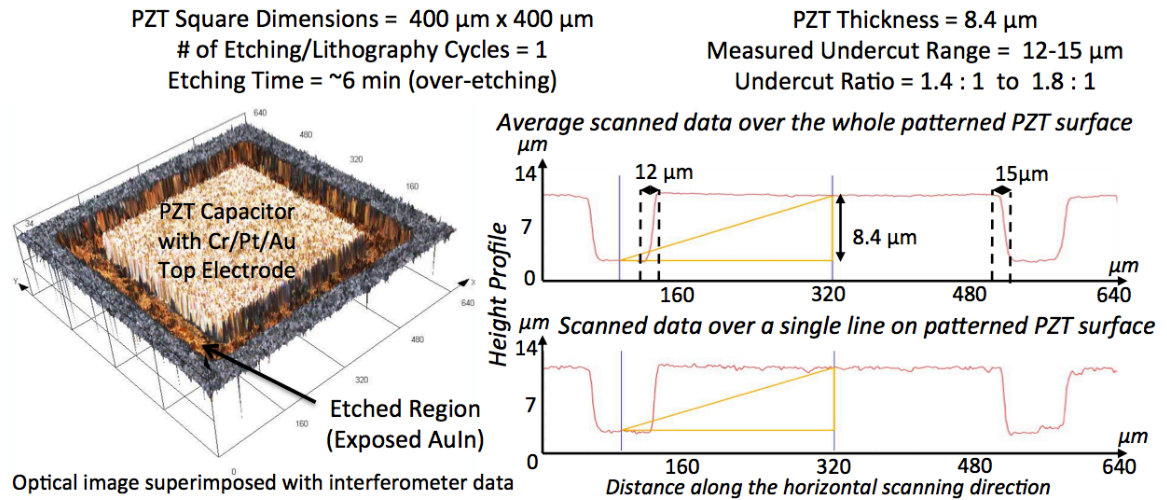


Fig.2.30 – Measured height profile of a 8-µm thick PZT capacitor wet-etch patterned in a single step.

In addition to optimizing the process time to avoid excessive etching, another possible method for minimizing the undercut ratio is to divide the process into multiple steps of lithography and wet etching (*Fig.2.31*). In this case, only a portion of the total PZT thickness is etched in one of these cycles, the used photoresist mask is then stripped off, and a new layer of photoresist is used to mask the next etching step, over-coating and protecting the previously created undercut region. Overall, at the end of several lithography and etching cycles, the total undercut is limited to the maximum undercut obtained at one of these cycles. The number of etching cycles and minimum feature size obtainable with this method depend on the etched PZT thickness and the repeatable lithographic accuracy over steep features.

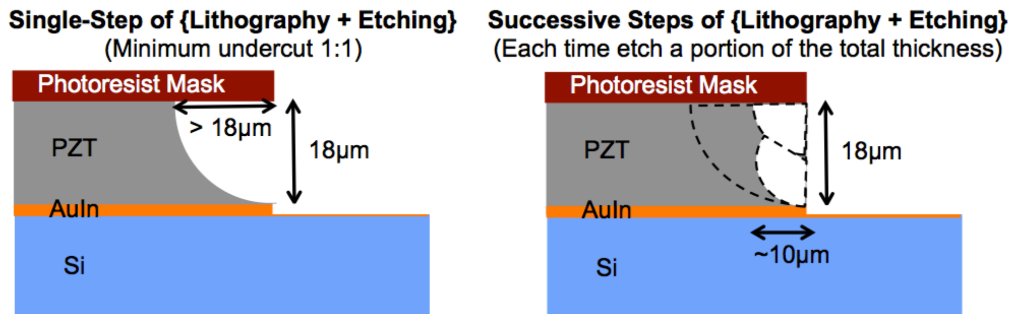


Fig.2.31 – A possible method to decrease the effective undercut during wet-etching of thick PZT layers.

Using this new multi-step wet-etching method, 18 µm thick PZT is patterned within two cycles, to provide an undercut ratio less than 0.6 : 1 (*Fig.2.32*). A tolerance of 15 µm

is provided between the edge of the top Cr/Pt/Au electrode and the edge of the etching mask, since the utilized acidic solution can also attack these metal layers.

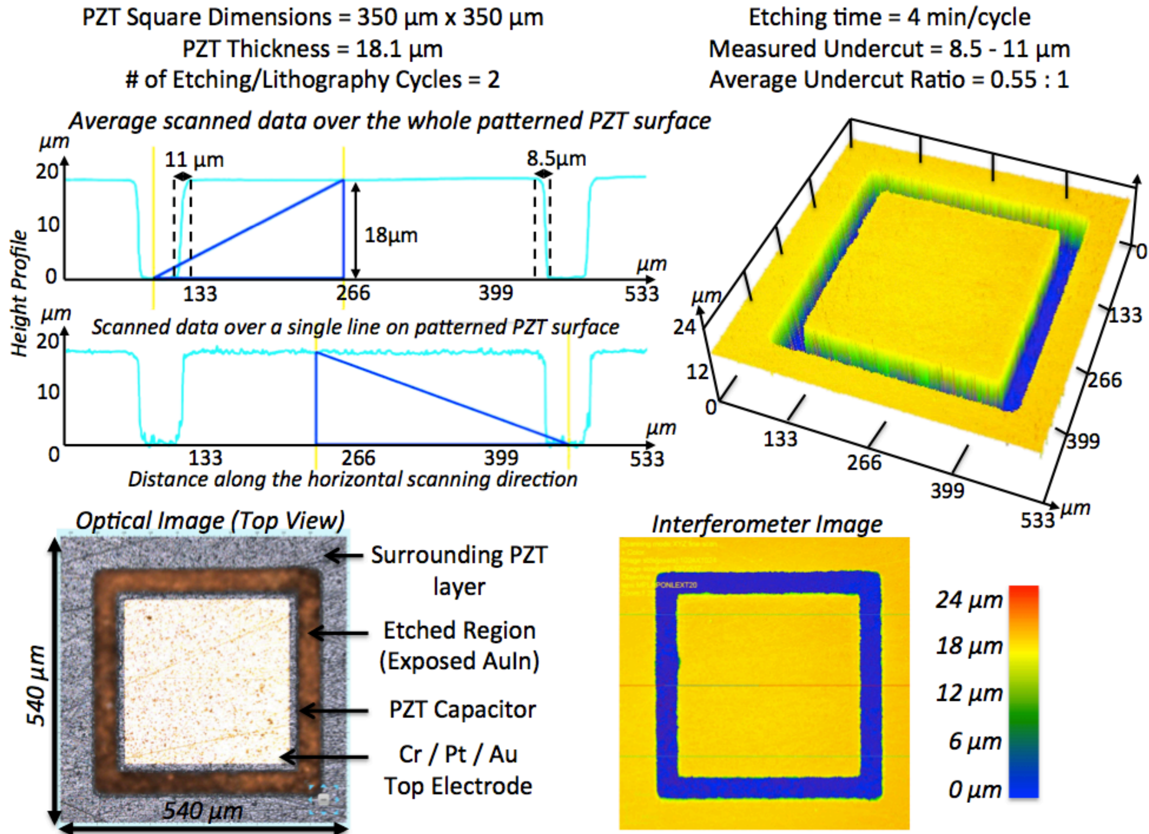


Fig.2.32 – Measured height profile of an 18-µm thick PZT capacitor wet-etch patterned in two steps.

2.5. Electrical Characterization of the Final Film

Preservation of ferroelectric properties in PZT after the bonding process is confirmed via measurement of the remnant polarization (37.7 µC/cm^2) and the coercive field (1.9-2 kV/mm) by use of a Radiant^{TM} ferroelectric test system in an external foundry *(Fig.2.33)*. The aim of this measurement is to observe any shift in the electrical characteristics due to a possible stoichiometric or morphological change at high temperatures, such as out-diffusion of Pb or other vendor-specific dopants. The measurement results closely match the original values provided by the piezoelectric ceramic vendor. Due to our limited access to the testing setup, no further data was obtained for the PZT films that are mechanically thinned after bonding. However, we can assume a minimal change, since the thinning process is performed at room temperature. Still, effects of possible local micro-cracks in the final film due to the mechanical thinning process may require further investigation in order to enable fabrication of high-resolution structures.

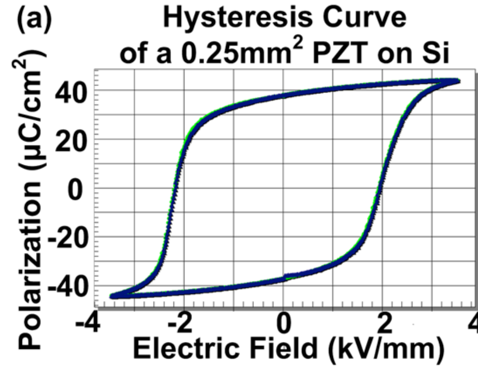


Fig.2.33 – Polarization curve of a 500µm×500µm PZT piece after bonding on silicon

In order to confirm that the piezoelectric properties are preserved in the final bonded and thinned PZT films, an atomic force microscope, NanoMAN AFM with Veeco Nanoscope controller, is utilized in its piezo-response mode (PFM) [Veeco08]. During these measurements, the AFM is operated in contact mode where the tip touches the PZT surface with a constant deflection to ensure good contact (*Fig.2.34*). An AC electric field is applied between the tip and sample, and as the piezoelectric sample locally expands and contracts, a four-quadrant photodiode detector measures the vertical deflection of the cantilever beam. Since the measured deflections are on order of a few picometers, a lock-in amplifier is used, which uses the applied electric field as its reference input. Most often, the measurement limitations are set by photodetector sensitivity, background thermal/vibration noise and shot noise. In addition to these, the surface roughness on the sample can also result in noisy measurements. Although piezo-response force microscopy is used in this study only to measure the effective direct piezoelectric coupling (d_{33eff}), it is also possible to leverage this tool for gathering information on the domain structures and polarization switching mechanisms.

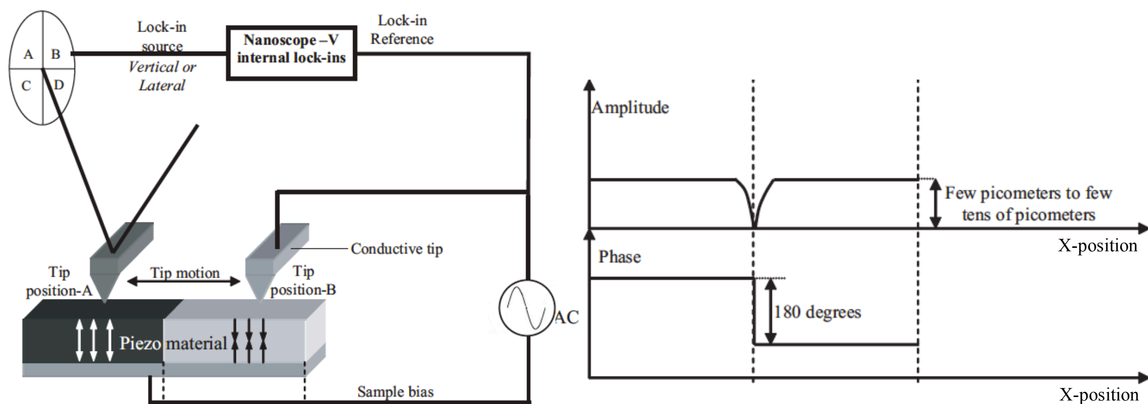


Fig.2.34 – Piezo-response force microscopy (PFM) setup used for the tests [Veeco08]

During the PFM tests, Veeco SCM-PIT Ti/Pt coated conductive tips with 250 μm cantilever length and <10 nm tip diameter are used. For proper characterization of the cantilever beam employed in these tests, its spring constant (2.55 N/m), resonance frequency (62.9 kHz) and deflection sensitivity (77.8 nm/V) are measured initially. In order to minimize the effect of noise in the measurements, the AC voltage amplitude applied on the sample is not kept at a constant value but swept from 0 V to 10 V and back to 0 V in a total duration of 10 seconds, and the change in deflection response from the sample is recorded. The drive frequency is kept at 10 kHz, away from the resonance frequency of the AFM tip so as not to be affected by its quality factor.

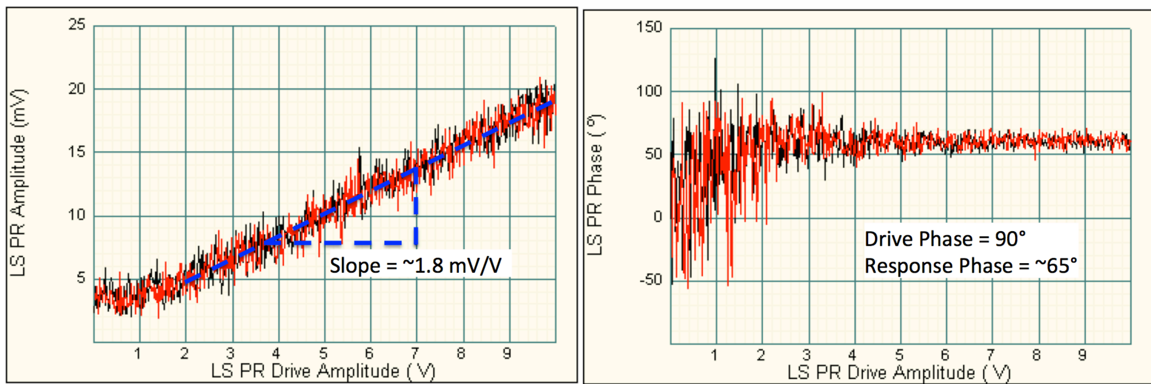


Fig.2.35 – Piezo-response measurement on bonded and thinned ~16 μm thick PZT-5A film

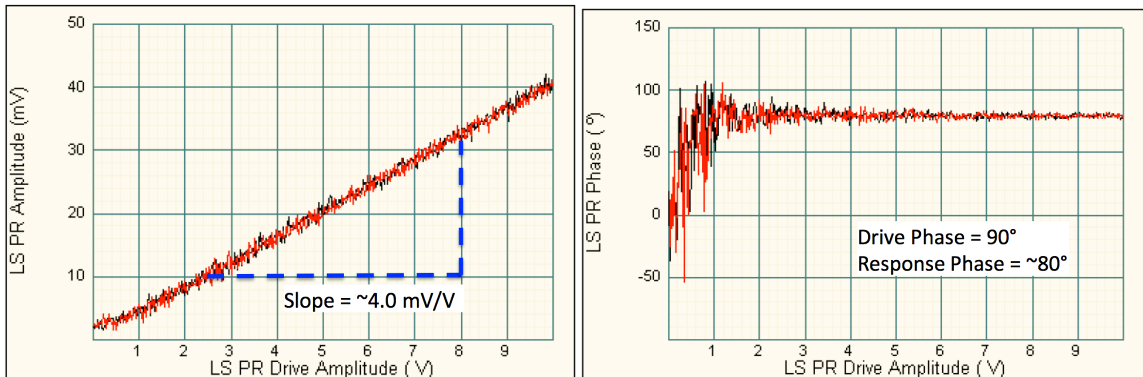


Fig.2.36 – Piezo-response measurement on bonded and thinned ~16 μm thick PZT-5H film

Measurements are performed on 300 μm x 300 μm sized Cr/Pt/Au top electrodes on ~16 μm thick PZT-5A and PZT-5H films, which are bonded on silicon via ~3 μm thick AuIn solder (*Fig.2.35 & Fig.2.36*). The use of a top electrode allows the application of a more uniform electric field through the PZT, and facilitates higher measurement accuracy. It has been previously reported that reducing the dimension of a top electrode from 1 mm to 0.05 mm can result in a decrease in the d_{33eff} measurements up to 50%, due

to the increased influence of imperfect film-clamping, thermal pre-stress and unintended actuation of the surrounding PZT layer [Prume04].

From these PFM measurements, the tip deflection can be calculated by using the initially measured deflection sensitivity of the cantilever beam.

$$Tip\ Deflection\ (pm) = Deflect.\ Sensitivity\ (pm/mV)\ x\ Measured\ Response\ (mV) \quad (2.4)$$

Although no DC bias is applied on the sample, the measurements include a static tip deflection, which is a result of initial hard positioning of the tip to ensure good contact on the sample surface. Since d_{33eff} is calculated by taking the ratio of the change in actuation response to the change in applied AC voltage, this static deflection can be neglected.

$$Tip\ Deflection = z(t) = d_{33eff}V_{DC} + d_{33eff}V_{AC}.\cos(\omega t + \Delta\phi) \quad (2.5)$$

$$d_{33eff} = \frac{\text{S}_3\ \text{(Out-of-Plane Strain)}}{\text{E}_3\ \text{(Vertical Electric Field)}} = \frac{\Delta z_{Amplitude}}{\Delta V_{AC-Amplitude}} \quad (2.6)$$

As expected, the measured effective piezoelectric couplings are lower than the values obtained from unconstrained bulk materials, because clamping of the piezoelectric thin film by the thick bottom silicon substrate changes its boundary conditions. In the case of a perfect lateral clamping by a totally rigid substrate, one can assume that under a vertically applied electric field the in-plane strains stay at zero while the generated in-plane stresses degrade the out-of-plane strain [Lefki94].

$$\text{In-plane Strain} = S_2 = S_1 = ({s_{11}}^E + {s_{12}}^E)T_1 + d_{31}E_3 = 0 \quad (2.7)$$

$$\text{Out-of-plane Strain} = S_3 = 2{s_{13}}^E T_1 + d_{33}E_3 = 0 \quad (2.8)$$

From these equations, the relation between the original material coefficient and the measured effective coefficient can be easily calculated [Prume07].

$$d_{33eff} = d_{33} - 2\left(\frac{d_{31}.{s_{13}}^E}{{s_{11}}^E + {s_{12}}^E}\right) \quad (2.9)$$

In *Table.2.1*, the measured d_{33eff} and calculated d_{33} values of thinned PZT-5A and PZT-5H films are compared with the values from vendor provided datasheets of the bulk materials. The slight mismatch in values are assumed to be associated with the perfect clamping assumption in the calculations, and the effect of additional static in-plane stresses on the piezoelectric layer from the 3 μm thick AuIn bond layer. Nevertheless, the results indicate that the high piezoelectric coefficients of the bulk PZT are preserved in final thinned PZT films.

Table.2.5 – Measured piezoelectric strain coefficients on PZT-5A and PZT-5H thin films

	d_{33eff} (Measured)	d_{33} (Calculated)	d_{33} (Vendor Datasheet)
PZT-5A	140 pm/V	398 pm/V	390 pm/V
PZT-5H	311 pm/V	772 pm/V	650 pm/V

2.6. Advantages of the Developed Thinned-PZT Process

- *High piezoelectric coupling:* As described in the introduction section, commercial bulk piezoelectric ceramics can provide much higher electromechanical coupling compared to many thin-film deposition techniques. This results in realization of devices with higher sensitivity or larger actuation range.
- *Piezoelectric layer thickness:* The developed technology allows a wide range of thickness values for the piezoelectric layer from 5 μm to 100 μm, while most of the other deposition technologies such as sol-gel deposition, sputtering or epitaxial growth are limited in thickness to a few μm. Furthermore, in these traditional deposition methods, it can be challenging to modify the deposition thickness for different applications due to frequently required successive multi-layer deposition, variation of built-in stress with thickness, and the required modification of existing process recipes, such as new spin-coating/hydrolysis/annealing/sintering temperature and times.
- *Wide range of piezoelectric material choice:* The developed technology is not limited to deposition of a certain kind of PZT material, but rather can take advantage of a variety of bulk piezoelectric materials that are commercially available. In addition, there is no need for an extensive process modification to change the work material such as development, purchase or characterization of a new deposition tool, and the required R&D time for a new product using a new piezoelectric material is shortened. Some of the commercial piezoelectric substrates that can be utilized with the developed bonding & thinning process are:
    - Variety of soft/hard lead-based ferroelectric poly crystalline materials (PZT-5A, PZT-5H, PZT-8, PZT-4, etc.)
    - Single crystalline piezoelectric ceramics (PMN-PT, PZN-PT, etc.)
    - Conventional lead-free bulk piezoelectric materials ($BaTiO_3$, $LiTaO_3$, etc.)
    - Emerging lead-free bulk piezoelectric materials (KNN, LF3T, LF4T, etc.)
    - Other emerging bulk materials from several electro-ceramics vendors

- *The use of standard clean-room tools:* The use of standard cleanroom tools (a standard thermo-compression wafer bonder and a good quality wafer lapping tool) instead of sophisticated equipment for deposition of specific materials, which can be expensive but still hard-to-tune for reliable operation, decreases the fabrication cost and allows easy adaptation by other micro-fabrication facilities.
- *Characterized and repeatable material properties:* Unlike many thin-film deposited materials, most of the commercial bulk piezoelectric substrates are already highly characterized for their material coefficients including the piezoelectric properties, elastic properties, temperature response, pyroelectric properties, etc. This allows accurate and fast analysis and simulation of the designed piezoelectric device. Furthermore, many vendors claim to provide high uniformity in the material properties from wafer to wafer, which results in high repeatability in end products. In contrast, repeatability issues have been reported in the past for several thin-film deposition methods. For example, the PZT sol-gel can change its properties in the stored chemical solution even during its shelf time.
- *Low temperature processing:* The maximum process temperature required for the thinned-PZT process is 200°C, while the utilized AuIn diffusion bonding allows for further processing temperatures of up to 500°C depending on the requirements of a specific application. However, if the process temperature exceeds the Curie temperature of the leveraged bulk piezoelectric material, a repolarization step should be performed at the end. Some of the benefits of low temperature processing are:
    - Use of piezoelectric substrates (e.g. PZT-5A), which have high Curie temperatures (>300°C) *eliminates the necessity of re-polarization*, since the polarization and bulk piezoelectric properties can be still preserved at the end of the whole fabrication process.
    - The developed process is *post-CMOS compatible*, and this feature can be leveraged to fabricate a bulk piezoelectric MEMS device with integrated circuitry on the same chip in a future project.
    - Compared to many other bonding methods, the low process temperature of solder and parylene bonding also results in *lower residual stress*.

- *Multi-layer deposition for bimorph structures:* Bonding and thinning of two piezoelectric layers by use of the same or different bulk materials can be utilized to fabricate bimorph structures for increased sensitivity or actuation capability. Although this fabrication capability is possible in a limited number of the existing deposition methods too such as screen-printing, others lack this option due to the required repetition of a high temperature step for deposition/annealing/sintering of the piezoelectric layers, which results in cracking of the initially deposited film.
- *Formation of suspended flat structures on pre-patterned silicon features:* This unique surface micro-machining capability is not attainable with the thin-film deposition methods, since they require a flat deposition surface.

2.7. Process Corners, Challenges and Limitations

- *Minimum piezoelectric layer thickness:* The minimum PZT thickness that can be obtained with this process is limited to ~5 μm due to the large grain sizes (~3 μm) in the original bulk material. Although, a higher tolerance at this minimum limit is possible with single crystalline ceramics and other bulk piezoelectric materials, still the final wafer-level thickness uniformity (+/- 0.5 μm currently) at the end of the thinning process limits the application fields where this process can be utilized. For instance, nano-resonators, ferroelectric memory devices, and microphones often require much thinner piezoelectric layers, 0.1 μm to 3 μm.
- *Minimum lateral patterning resolution:* The minimum patterning resolution that can be obtained with the bulk PZT process is limited by the undercut of the thick film in wet-etching case, and by slope of the side-walls in dry-etching or laser ablation cases.
- *Minimum bond layer thickness:* The minimum AuIn bond layer thickness that has been studied in this work is 3 μm. A thinner bond layer is foreseen to be possible through a decrease of the required indium thickness in the bond layer, which can be enabled by initial polishing of the highly rough PZT surface, and by a slight increase in the bonding temperature (250-300°C) to overcome the formation of undesired intermetallic compounds during the temperature rise in the TLP bonding process.
- *Increased processing steps:* The number of required processing steps is higher compared to a single-step deposition system such as sputtering. However, many thin-film deposition methods actually require additional steps that are usually overlooked,

such as deposition of certain metals (e.g. sputtered Pt or Mo) for controlled growth, surface preparation, and extended furnace annealing.

- *Indium as an expensive material:* Since indium is an expensive metal with its price/weight close to silver, the use of 1-2 µm thick evaporated indium in the required AuIn bond layer can be rather unfavorable compared to other bonding techniques, such as those using spin-coated polymers. However, different options to decrease the deposition cost can be investigated, including the use of electroplating instead of e-beam evaporation for deposition of indium, or investigation into other TLP solder compositions such as AuSn, which has still a low bonding temperature of 300°C.
- *Stress engineering:* Despite of the close match in the thermal expansion coefficients of silicon and bulk PZT substrates, because of high thermal expansion/shrinkage of both AuIn and parylene bonding layers a careful attention should be given to the device design in order to avoid any structural deformation or reduced piezoelectric coupling due to this residual stress.
- *Fabrication of 3-D structures:* Unlike sputtering, which allows conformal deposition over 3-D surfaces such as a wineglass structure for resonators, currently the developed process technology only allows the fabrication of 2-D planar structures.
- *General issues related to ferroelectric materials:* Unlike AlN or ZnO, most of the bulk piezoelectric materials are ferroelectric at the same time, which brings some limitations and requires special care during their operation.
    - *De-polarization:* A ferroelectric material typically lose its spontaneous electric polarization and its characteristic polarization hysteresis over a phase transition temperature, called the Curie temperature, above which it starts to behave as a paraelectric material. The Curie temperature is commonly in the range of 100-150°C for single crystalline lead-based ceramics, 200-350°C for polycrystalline lead-based ceramics, 610°C for lithium niobate, and 1150°C for lithium tantalate. Thus, the operation temperature of a ferroelectric device is often limited up to ~50°C below to its Curie temperature, where a permanent reduction occurs in its piezoelectric properties. Depolarization can also be an issue if the material is exposed to high dynamic/static mechanical stress or electric field.

- *Electrical non-linearity:* The polarization hysteresis in ferroelectric materials causes them to behave slightly different under increasing and decreasing electric fields or mechanical stresses. This can result in a small nonlinearity in the actuation or sensing characteristics of a MEMS device. However, it is possible to engineer an axial static compressive stress into the piezoelectric layer on purpose, which has been previously shown in literature to decrease this nonlinearity.