

A Low Power Wireless Multichannel Microsystem For Reliable Neural Recording

by

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This dissertation is dedicated to my mother
Dr. Shahnaz Atabak for her endless love and support

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ABSTRACT

This thesis reports on the development of a *reliable*, single-chip, multichannel wireless biotelemetry microsystem intended for extracellular neural recording from awake, mobile, and small animal models. The inherently conflicting requirements of low power and *reliability* are addressed in the proposed microsystem at architectural and circuit levels. Through employing the preliminary microsystems in various in-vivo experiments, the system requirements for reliable neural recording are identified and addressed at architectural level through the analytical tool: signal path co-optimization.

The 2.85mm×3.84mm, mixed-signal ASIC integrates a low-noise front-end, programmable digital controller, an RF modulator, and an RF power amplifier (PA) at the ISM band of 433MHz on a single-chip; and is fabricated using a 0.5μm double-poly triple-metal n-well standard CMOS process.

The proposed microsystem, incorporating the ASIC, is a 9-channel (8-neural, 1-audio) user programmable reliable wireless neural telemetry microsystem with a weight of 2.2g (including two 1.5V batteries) and size of 2.2×1.1×0.5cm³. The electrical characteristics of this microsystem are extensively characterized via benchtop tests. The transmitter consumes 5mW and has a measured total input referred voltage noise of 4.74μV_{rms}, 6.47μV_{rms}, and 8.27μV_{rms} at transmission distances of 3m, 10m, and 20m, respectively. The measured inter-channel crosstalk is less than 3.5% and battery life is about an hour. To compare the wireless neural telemetry systems, a figure of merit (FoM)

is defined as the reciprocal of the power spent on broadcasting one channel over one meter distance. The proposed microsystem's FoM is an order of magnitude larger compared to all other research and commercial systems.

The proposed biotelemetry system has been successfully used in two in-vivo neural recording experiments: *i*) from a freely roaming South-American cockroach, and *ii*) from an awake and mobile rat. In recording from the cockroach's antennas, the small amplitude action potentials ($100\mu V_{pp}$) on left and right antennas sensory inputs were captured wirelessly from the freely roaming subject. In recording from the Femur sections of the cockroach rear legs a variety of biopotential signals from small amplitude action potentials ($100\mu V_{pp}$) to large amplitude intramuscular EMG signals ($2mV_{pp}$) were recorded wirelessly and could be attributed to state of the cockroach, i.e. walking versus standing. In recording from the hippocampus of an awake and mobile rat, the extracellular neural action potentials on eight channels were received and recovered wirelessly.

CHAPTER 1

INTRODUCTION

The term biotelemetry refers to the measurement of biological data over a distance. As an example the simplest device applying the biotelemetry principle is stethoscope, in which the heart beats are amplified acoustically, transmitted through a hollow tube and picked up by the physician's ear [1.1]. The quantities measured by the biotelemetry devices can be divided into two categories: *i*) bioelectrical (or biopotentials) variables such as ECG, EMG, EEG, LFP, neural action potentials, and *ii*) physiological parameters such as blood pressure, gastrointestinal pressure, blood flow, and body temperature. The biotelemetry systems have two broad applications: health care and neuroscience community. In health care applications, the patient's physiological parameters such as ECG and blood pressure are of interest whereas in neuroscience experiments the bioelectrical signals of the test subject (EMG, EEG, LFP, and neural action potentials) are collected by the biotelemetry system.

The field of biotelemetry was pioneered by Professor Willem Einthoven who is also the father of electrocardiography. To analyze the heart's electrical activity, in 1903, Einthoven transmitted ECG signals from a hospital to his laboratory many miles away (figure 1-1). In this experiment Einthoven used the telephone lines to relay the biological information and immersion electrodes for sensing the patient's ECG signals; at the other end of the telephone line (laboratory) Einthoven employed galvanometer to restore the remotely sensed ECG signals [1.1].

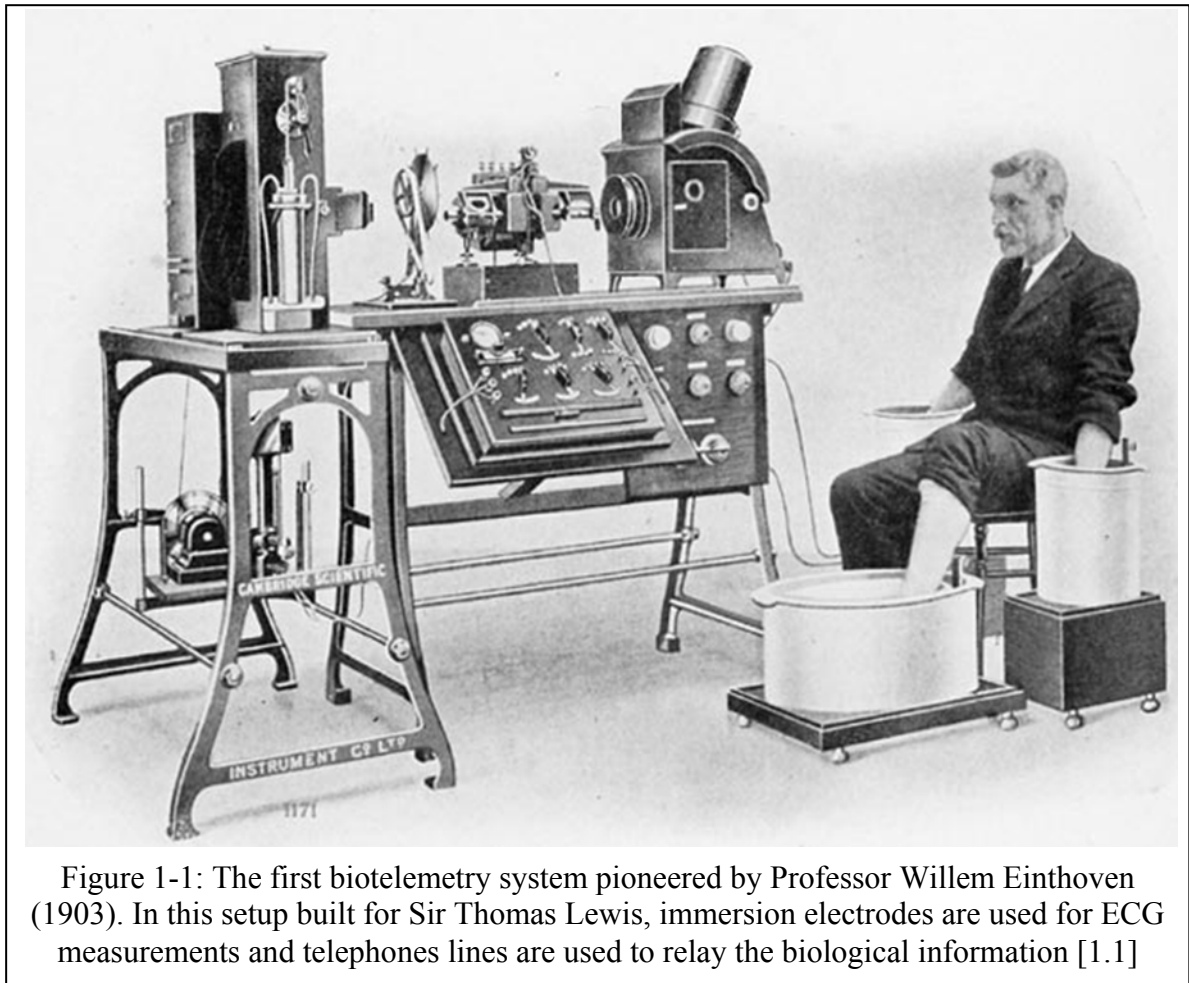


Figure 1-1: The first biotelemetry system pioneered by Professor Willem Einthoven (1903). In this setup built for Sir Thomas Lewis, immersion electrodes are used for ECG measurements and telephones lines are used to relay the biological information [1.1]

Since 1903, advancements in many fields of engineering and science, including integrated circuits, micro-electro-mechanical-systems (MEMS), radio frequency (RF) engineering, and signal processing have made it possible to develop light weight, small size, low power, low noise, multichannel, wireless biotelemetry systems. The MEMS technology has facilitated the fabrication of sub-millimeter, multi-site neural recording electrodes which conceptually replace the immersion electrodes in Einthoven's biotelemetry system (figure 1-1). The advancements in integrated circuits and RF engineering have enabled the integration of all the transmitter circuit blocks on a single, low power, application specific integrated circuit (ASIC) with sub-centimeter dimensions; furthermore, high frequency wireless links have replaced the telephones

lines (in Einthoven's biotelemetry system) for back telemetry of biological information. As a result of this high level of integration and low power consumption, today's ASIC-based biotelemetry transmitters have dimensions on order of few centimeter cubic (cm^3), weigh only a few grams, and have power consumptions less than few milliwatts.

Recent advancements in behavioral neuroscience have shown that the test subject responses to stimuli are heavily dependent on the animals' state (sedated, restrained, isolated) [1.2] and social context [1.3]. While tethered recording provides the neuroscience community with the opportunity of employing reliable data acquisition systems, it inevitably skews the experiment's outcomes since the animal has to be restrained and/or sedated [1.2, 1.3]. Therefore, there is an increasing demand for light weight, small size, and reliable wireless neural telemetry microsystems which facilitate studying the underlying principles of neural activity in small animal models. Using such systems the test subject can freely interact with other colony members in a semi-natural environment as it is being studied and presented with various stimuli. On the other hand, in order to decode the wirelessly received extracellular neural activities correctly, the wireless microsystem should be as reliable as the tethered recording setups.

In brief, a reliable wireless neural telemetry system is one in which no extracellular action potential is lost, or falsely flagged as it is being transmitted over a reasonable distance for the whole duration of the in-vivo experiment. Specifically the reliability requirements for wireless multichannel neural recording systems are: *i*) low inter-channel crosstalk levels ($XT < 5\%$), *ii*) small input referred noise of the entire system including the biotelemeter, wireless link and the external electronics ($V_{noise} < 30\mu V_{rms}$), *iii*) back telemetry over a reasonable distance ($>3m$), *iv*) continuous neural

recordings, and v) long recording sessions ($>1hr$). Also to record from freely moving small animals the biotelemetry has to be limited in weight ($<1g$) and size ($<1cm^3$). These physical specifications put stringent constraints on the transmitter's power consumption which is inherently in conflict with the reliability and robustness of the overall system. Therefore, the key challenge of designing these systems is to meet the conflicting requirements of low power and reliability.

The work presented in this thesis is focused on biotelemetry systems aimed at the needs of neuroscience community and designed specifically for reliable multichannel wireless recoding of neural action potentials generated in the central nervous system (CNS) of small animals. Low power, small-size/light-weight and reliability are conflicting requirements, and addressing them is the main challenge of the presented work.

1.1 The Specific Application

The goal of the presented work is to develop wireless microsystems and technologies which facilitate studying the neural circuits involved in vocal exchange of small songbirds and specifically zebra finches. This vocal exchange is an auditory interaction between different birds in a colony much like conversation of humans. And as in the human case, vocal exchange of songbirds is heavily dependent on social context and behavior state of the birds [1.2-1.6]. Here, social context refers to the situation the bird is in, relative to other colony members; the behavioral state refers to the bird's state, e.g., stressed, sedated, mating mode, etc.

Many recent observations have proved that vocal based communication is dependent on the social context. The technology needed to study the neural bases of vocal communication in small song birds while interacting freely in a semi-natural habitat is not available yet. Therefore, in most experiments published today, the test subject's state is altered (sedated, restrained, isolated, etc.), which will skew the experiment's outcomes. The same principle holds true in vocal communication because producing an auditory response is a response to an auditory stimulus which is



Figure 1-2:
Tethered recording
from a zebra finch
(courtesy of Prof.
Marc F. Schmidt)

processed differently in different social and behavior state contexts [1.7-1.9]. Figure 1-2 shows the currently used tethered setup for neural recording from zebra finches.

There are a number of requirements for wireless biotelemetry microsystems employed in reliable wireless neural recordings. The weight of the developed wireless biotelemetry microsystem needs to be limited ($<1\text{g}$) so that the small zebra finch (an adult zebra finch weighs about 12g) can carry it in a colony. The size of the transmit unit should also be limited to $<1\text{cm}^3$; it is likely that birds with foreign objects attached to their head are not involved in social interactions with other colony members; the small size of the device makes it possible to encapsulate the microsystem so that it is invisible and inaccessible to other colony members.

Other than the constraints on weight and size, the experiments must be conducted continuously for few hours, during which the animal subject is presented with various stimuli. The system must be robust and reliable; during the experiment the transmitter

unit should send the multichannel neural data to the receiver with minimum system-introduced noise, no interruption and ideally no crosstalk. Neuroscientists need to observe individual neural spike events; therefore a low noise system is required so that the neural spikes can be distinguished from the background noise. An interruption in the communication channel, between the transmitter and the receiver, leads to loss of a population of neural spikes which can result in misleading conclusions. And finally, in systems with large crosstalk ($XT > 5\%$) false spike events will be reported which contribute to misleading conclusions as well.

1.2. The Concept of Reliability in Wireless Biotelemetry Systems

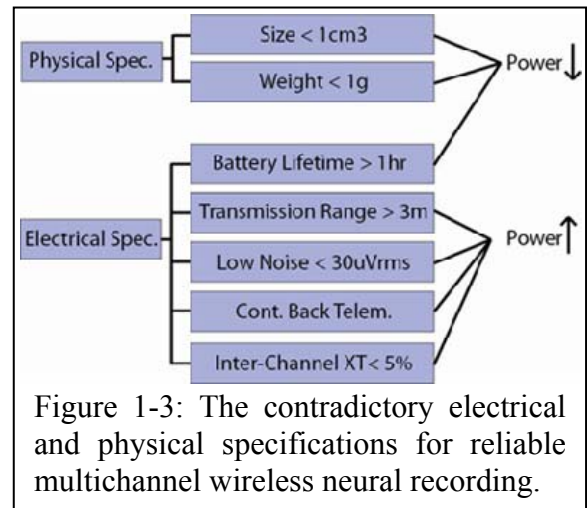
A reliable wireless neural telemetry system is one in which no extracellular action potential is lost, or falsely flagged as it is being transmitted over a reasonable distance for the whole duration of the in-vivo experiment. The system requirements for reliable neural recording from small animal subjects can be divided into physical specifications and electrical specifications. The physical specifications are: *i*) low weight ($<1\text{g}$), and *ii*) small size ($<1\text{cm}^3$). The physical specifications stem from the small size and limited carrying capabilities of the adult zebra finches and similar small animal subjects. These physical specifications put stringent constraints on the transmitter's power consumption which inherently are in conflict with the reliability and robustness of the overall system. Electrical specifications are related to signal quality and the overall system reliability. The electrical specifications required for reliable wireless multichannel neural recordings are: *i*) low inter-channel crosstalk levels ($XT < 5\%$), *ii*) small input referred noise of the entire system including the biotelemetry, wireless link and the external electronics (V_{noise}

$< 30\mu V_{rms}$), *iii*) back telemetry over a reasonable distance ($>3m$), *iv*) continuous neural recordings, and *v*) long recording sessions ($>1hr$).

Biotelemetry systems with large inter-channel crosstalk levels ($XT > 5\%$), flag false spike events, which lead to misleading conclusions about the brain circuits. Therefore, the inter-channel crosstalk level of the system should be kept well below 5%. The accumulative noise of the entire signal path from the implanted extracellular electrodes to the host computer's quantization noise should be below $30\mu V_{rms}$ so that the small-amplitude neural signals ($50\mu V_{pp}$ - $500\mu V_{pp}$) can be distinguished from the background noise. The neural transmitter should be capable of transmitting the multichannel neural data over a distance of at least 3m to cover the medium sized cage of small animal colony under study. The neural data telemetry should not be terminated at anytime during the neural recording experiment; this phenomenon has been observed in systems where the transmitter's antenna is directly coupled to the RF-modulator [1.16, 1.25]. Other than the wireless link the front-end can also terminate the neural data telemetry; in Fully-Analog, Time-Division-Multiplexing, Frequency Modulation (FA-TDM-FM) systems with an analog front-end that suffers from large offsets, the frequency spectrum of the wirelessly received RF signal can be excessively wide; due to limited available receiver bandwidth, the individual neural channels cannot be recovered and there would be a loss of neural data in such systems. Even if the required bandwidth can be supported by the receiver, the wide bandwidth increases the receiver noise; the increased receiver noise reduces the SNR of the recovered individual neural channels and consequently limits the transmission range for a fixed emitted RF power. Therefore it is essential to have the front-end output offset less than $1mV_{DC}$. The continuous back

telemetry can also be impacted by large low frequency noise signals; low-frequency (<500Hz) suppression is required to remove the Flicker (1/f) noise, Local Field Potentials (LFP), movement artifacts and 60Hz noise from the neural signal before reaching the multiplexing stage. These low frequency signals can saturate the front-end and/or the wireless link, resulting in loss of the neural data. And finally, the battery-powered transmitter should run for a few hours without the need to battery replacement. The specific implementation of these specifications depends on the employed architecture and will be discussed in more detail in chapter 2.

Figure 1-3 shows the contradictory nature of the electrical and physical specifications. The electrical and physical specifications are partly inter-related and partly contradictory; therefore to design a robust and reliable low power system, the various block parameters should be optimized with regard to others. To meet these conflicting requirements, at the circuit level various low power, low noise and robust circuit blocks are implemented;

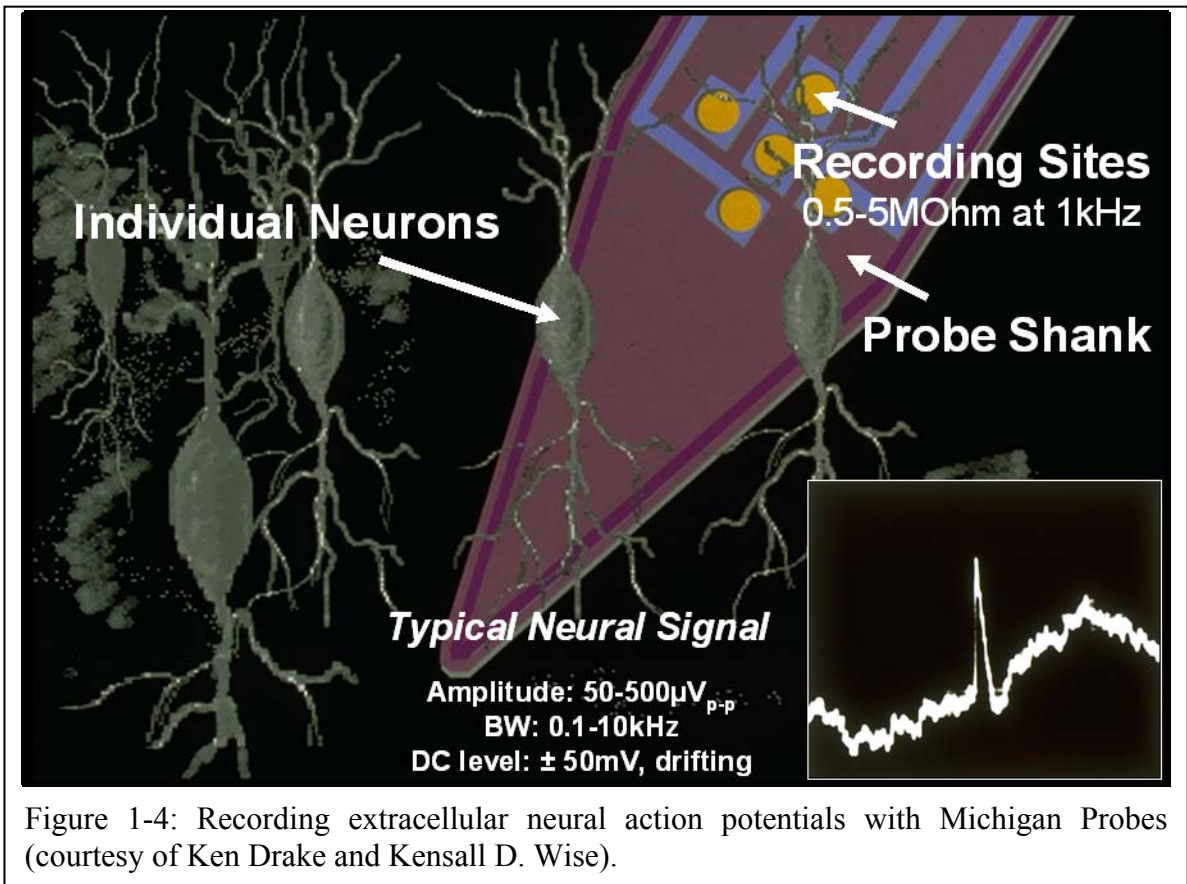


furthermore in this project an analytical tool (SPCO) is developed which attacks the problem at the system level. Signal-Path-Co-Optimization, SPCO (chapter 2), derives the formulas for performance metrics of interest based on high level parameters. SPCO takes in the high level system parameters (noise densities, distance, number of channels, etc.) and provides the user with a boundary for block parameters (front-end gain, VCO's

oscillator gain, etc.) within which, *i*) the system is reliable, and *ii*) signal to noise ratio (SNR) of the recovered neural channel is maximized.

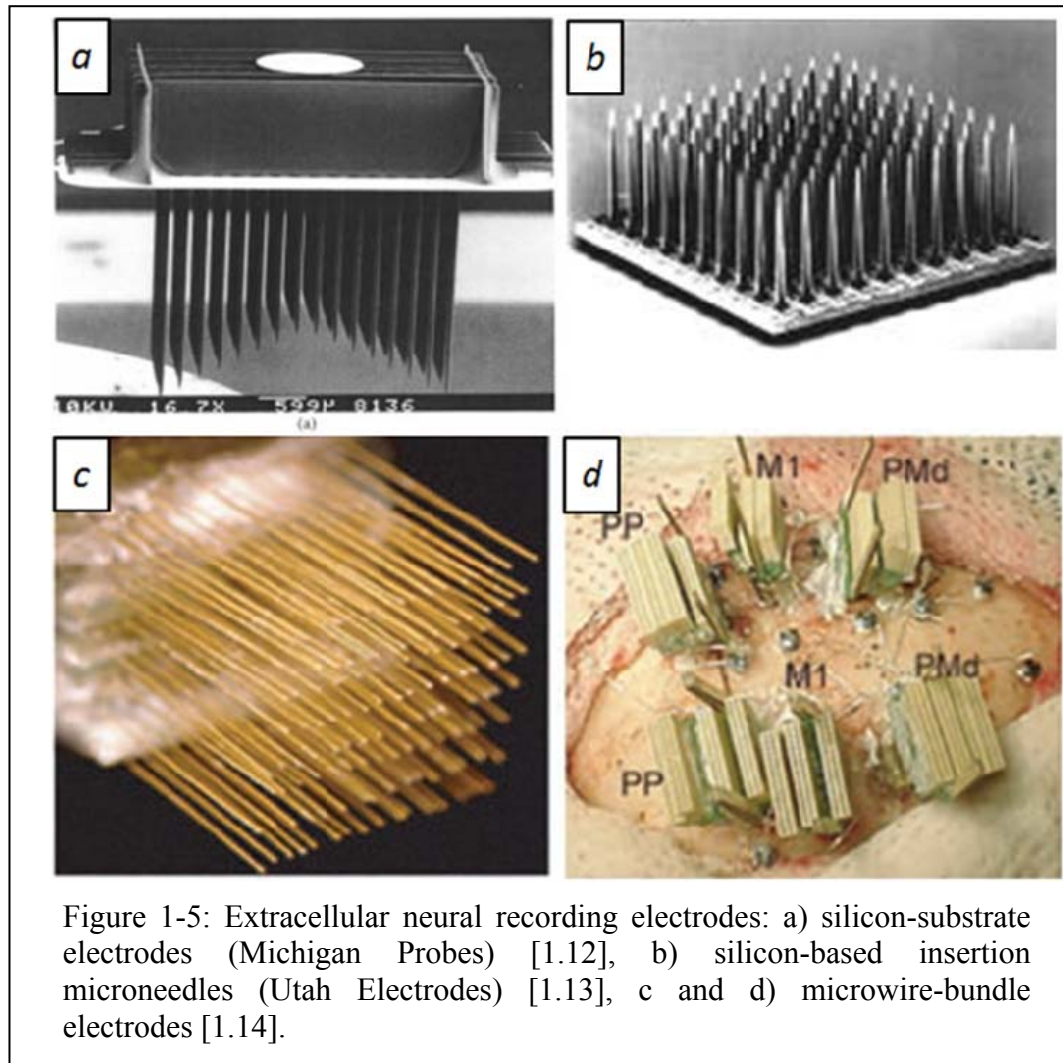
1.3. Wireless Biotelemetry Microsystems: *Previous Work*

The neural action potentials generated in the central nervous systems and sensed by extracellular electrodes have amplitudes between $50\mu\text{V}_{\text{pp}}$ and $500\mu\text{V}_{\text{pp}}$ in the frequency band of 500Hz-10KHz [1.10]. In extracellular neural recording, the electrodes



are inserted outside the neuron's body (soma) in an electrically conductive fluid which surrounds the neurons: extracellular fluid (ECF). Extracellular neural recording with silicon-based (Michigan) probes is shown in figure 1-4. The ionic current flow of the firing (excited) neurons in the extracellular fluid and the ECF's finite resistance create a

small transient potential difference ($50\mu V_{pp}$ - $500\mu V_{pp}$) between the working electrode, located in close proximity of the active neurons, and the reference electrode, which is



located in the ECF far from the recorded neuron populations. This transient voltage potential difference is what sensed by the electronics [1.11].

In today's neurophysiology laboratories there are three main categories of electrodes used for recording extracellular neural action potentials: *i*) silicon-substrate electrodes, e.g., Michigan probes [1.12], *ii*) silicon-based insertion microneedles, e.g., Utah Microelectrode Array (UEA) (the UEA is a 10×10 array of platinum-tipped silicon extracellular electrodes on a silicon substrate [1.13]), and *iii*) microwire-bundle

electrodes [1.14] which are an array of S-isonel (or Teflon)-coated tungsten (or stainless steel) microwire electrodes. These electrodes are shown in figure 1-5. The biotelemetry device is directly connected to the other end of the implanted extracellular neural recording electrodes usually through, so called, neuro-connectors [1.15].

Regardless of the specific architecture, all the biotelemetry devices have to amplify and condition the sensed, small-amplitude neural action potentials. Depending on the techniques used for multichannel multiplexing (TDM [1.16], FDM [1.17], TDM-PWM [1.18], etc.) and telemetry wireless link (FM [1.16], FSK [1.19], UWB [1.20], IR [1.21], etc.) various architectures are used to implement the multichannel wireless neural recording devices.

1.3.1. Research on Wireless Biotelemetry Systems

Mohseni *et al.* have demonstrated a single chip ASIC capable of transmitting 3-Ch of neural signal through the 94MHz-98MHz band with a maximum transmission range of ~ 0.5 m. The transmitter is composed of the ASIC, fabricated in a $1.5\mu\text{m}$ 2P2M CMOS process, along with only 3 off-chip SMD LC-Tank components. This device dissipates 2.2mW of power from two 1.5V miniature batteries, weighs 1.1g including the batteries and has dimensions of $17\text{mm}\times 12\text{mm}\times 1.6\text{mm}$ [1.16]. This an example of Fully Analog TDMA-FM architecture based on which the proposed work is implemented. There are three shortcomings with this system: *i)* the front-end implementation of electrode-DC offset rejection, does not allow for recording more than one neural channel in wireless in-vivo neural recordings due to inter-channel offset, and *ii)* the VCO-antenna

direct coupling and the lack of PA results in center frequency fluctuations and termination of back telemetry both of which prevent reliable wireless neural recording.

Seung Bae Lee, *et al.* demonstrated a 32-Ch wireless neural recording device which employs Pulse Width Modulation (PWM) of Time Division Multiplexed (TDM) signals [1.18]. The core of this prototype is an ASIC implemented in 0.5 μ m 2P3M CMOS and dissipates 5.8mW. The RF transmitter is a voltage controlled oscillator (VCO) which implements Frequency Shift Keying (FSK) with frequencies of 845.5MHz/915MHz and has a maximum transmission range of \sim 1.5m. The required receiver bandwidth varies between 36MHz-75MHz depending on the number of channels. This ASIC is not assembled in a standalone wireless biotelemetry microsystem.

In [1.19], Harrison *et al.* have developed a digital 4-Ch wireless neural recording system. It dedicates two channels to action potentials (300Hz-5.2KHz) and two channels are assigned for EMG (20Hz-280Hz) signals. The neural transmitter incorporates a COTS MEMS accelerometer with its data sent out along with the neural channels. Each neural channel has a gain of 1000 \times with an input referred noise of 2.3 μ V_{rms}. The back telemetry uses a VCO implementing FSK at 920MHz with a transmission range of 2m. The entire device measures 9mm \times 13mm and weighs 0.79g including the batteries. The ASIC consumes 2.64mW and the MEMS accelerometer burns 0.96mW for a total of 3.6mW. This system fits all the requirements of the intended application of this work except the number of neural channels. This is a digital transmitter and the number of neural channels cannot be extended without increasing the required bandwidth

Sung-Chae *et al.* reported a 128-Ch wireless neural recording IC consuming 6mW of power from a \pm 1.65V battery [1.20]. This chip employs impulse radio based Ultra

Wide Band (IR-UWB) RF transmitter centered at 4Ghz. The required bandwidth is 1GHz which is dedicated to sending out the raw neural data for all the 128 channels. Each channel is sampled with 6 to 9-bits of resolution resulting in a maximum data rate of 90Mbps. The chip area is of $8.8mm \times 7.2mm$ fabricated in a $0.35\mu m$ 2P4M CMOS process. The UWB antenna occupies $10mm \times 10mm \times 0.8mm$. This chip is not assembled in a standalone microsystem yet and not verified for in-vivo functionality. In this work the transmission range is not reported.

Song *et al.* have presented a hybrid (ASIC + COTS components), 16-Ch, transcutaneous device powered through RF link and transmitting the digital data through an Infra Red (IR) link [1.21]. Power consumption is 12mW which is provided by the RF forward wireless link. All the components are assembled on a flexible polymer substrate. Due to RF power link, the distance b/w the transmitter and the external coil is restricted to $< 1cm$. Even if powered by battery, the transmission range has to be limited to at most few centimeters due to IR back telemetry; furthermore due to large power consumption of 12mW the battery will dominate the size and weight of the transmitter making it unattractive for the application of the proposed work.

Schregardus *et al.* presented a fully analog, single-channel, light-weight telemetry system specifically designed for recording neural spikes from small zebra finches [1.22]. For neural data back telemetry this transmitter utilizes frequency modulation at 480MHz. The transmitter is assembled using commercial-off-the-shelf (COTS) components, measures $12mm \times 5mm \times 8mm$ and weighs 1.1g with batteries. Transmission range is $\sim 6m$ and the battery lifetime is 20hrs for continuous operation. The main drawback of this work is the single-channel signal path; due to the COTS based design, it cannot be

extended to a multichannel architecture without increasing the weight/size significantly. The most size/weight efficient way to have multichannel device using COTS component is to use a commercially available multichannel analog front-end. To the best of author's knowledge, there is only one company providing such a component: Intan Technologies, LLC [1.23]. The RHA2000-series products are integrated neural amplifier arrays from Intan Technologies containing 16 or 32 amplifiers with programmable bandwidths and on-chip time division multiplexing (TDM). These products consume $500\mu\text{W}$ per channel for a total of 7mW (RHA2116) and 14mW (RHA2132). The large power consumption of these microchips, would force the designer to employ heavy and bulky batteries.

Sodagar *et al.* reported a 64-Ch wireless neural recording microsystem which weighs 275mg , measures $14\text{mm}\times 15\text{mm}$, and dissipates 14.4mW from a 1.8V supply [1.24]. This system receives power and setup commands via a forward telemetry link which employs Amplitude Shift Keying (ASK) at $4\text{MHz}/8\text{MHz}$. For back telemetry it employs On-Off-Keying (OOK) with programmable frequencies of $70\text{-}200\text{MHz}$. This device can detect spike events on all the 64 channels or can continuously monitor a single channel with 8-bits of resolution. Due to inductive powering method, the distance between receiver antenna and the transmitter antenna has been tested for a range of 1cm and is limited to few centimeters. For two reasons this system is not suitable for the application of the proposed work: *i)* single channel continuous monitoring; due to the employed FSK communication link, the number of continuously monitored channels cannot be extended further without increasing the required bandwidth significantly, and *ii)* limited telemetry distance due to inductive powering; and even if the transmitter

operates on the battery due to 14.4mW of power dissipation, the battery size and weight will be prohibitive.

Harrison *et al.* have demonstrated a wireless neural recording microsystem to interface with the 100-site UTAH electrode array. The main component of the system is an ASIC which receives power and command data through a RF link, dissipates 8mW and sends out the spike events on all the channels by employing on-chip analog spike detection circuitry; it also can monitor one channel continuously with a input referred noise of $23\mu V_{\text{rms}}$. This ASIC is manufactured in a $0.6\mu\text{m}$ 2P3M BiCMOS process and measures of $4.6\text{mm}\times 5.4\text{mm}$. The forward RF link operates at 2.765MHz and the distance between the external coil and the integrated coil has to be less than 34mm . The reverse telemetry employs FSK at 902MHz/928MHz. The overall transmitter dimensions including the power coil are $7.6\text{mm}\times 8.0\text{mm}\times 2.5\text{mm}$ [1.25]. Like the previous system, due to single channel monitoring and limited telemetry distance this system is not suitable for the intended application of the proposed work. Also 8mW of power dissipation does not allow using miniaturized batteries.

Yeager *et al.* have demonstrated a single-channel system which only transmits the neural spike counts [1.26]; the novelty of this design is its power harvesting method; the transmitter is powered from the far-field RF energy provided by a RF Identification (RFID) reader up to a distance of 1m. The ASIC contains the neural amplifier, while the circuitry for spike detection and spike counting is provided by a general purpose microcontroller. Power harvesting and passive back telemetry are implemented by COTS RFID. The entire neural transmitter dissipates $36\mu\text{W}$ from the harvested 1.8V supply,

measures $2.2 \times 1.5 \text{cm}^2$, and weighs 1.6g. It should be noted that this system has only one channel and only transmits the spike counts not the continuously recorded neural channel.

Rai *et al.* have developed a passive wireless system which continuously broadcast a digitized, single neural channel over 15m of distance [1.27]. The neural channel is amplified with a variable gain from 42 to 78dB, digitized with 8-bits at 9.1kS/s, and sent out using FSK modulation scheme at 400MHz carrier frequency. Similar to [1.26] this system too is supplied from the far-field RF energy. The reported transmission range and power consumption are 15m and $500 \mu\text{W}$ respectively. This system is not integrated in a standalone microsystem and there is no in-vivo verification of its functionality.

In [1.28], Linderman *et al* have demonstrated a new class of neural recording microsystems. This is a discrete board-level design which uses commercial-off-the-shelf (COTS) components; it has 16 channels of data from which 2 can be simultaneously recorded from. The selected two channels are digitized by 12-bits and saved in a 6GB compact flash card capable of recording up to 48hrs of data. The microsystem weighs 220g and measures $60 \times 70 \times 45 \text{mm}^3$. Using a 1600mAh battery, the battery lifetime is 19hrs. The main advantage of this system is its small input referred noise ($3.5 \mu\text{V}_{\text{rms}}$) which is independent of the test subject's location. The main disadvantage is its large weight and power consumption.

Takeuchi *et al* have reported a discrete board level single-channel neural transmitter intended for recording from small insects [1.29]. The entire transmitter weighs 0.1g (without the batteries), measures $15 \text{mm} \times \text{mm}$ and is assembled using COTS components. The power consumption of the transmitter unit is 10mW for a transmission range of 16m. Similar to [1.22] this a fully analog FM transmitter in which the channel

count cannot be expanded further without significant compromise to size, weight and power consumption.

1.3.2. Commercial-Off-the-Shelf (COTS) Systems

There are several commercial companies (TBSI, Alpha Omega, etc) providing wireless multichannel neural transceivers. The most distinguished product in the market is from Triangle BioSystems, Inc.

(TBSI) [1.30]. TBSI products are 5, 15, 31 and 63-Channels unidirectional wireless neural recording systems. Figure 1-6 demonstrates TBSI 15-Ch neural transmitter. The input referred

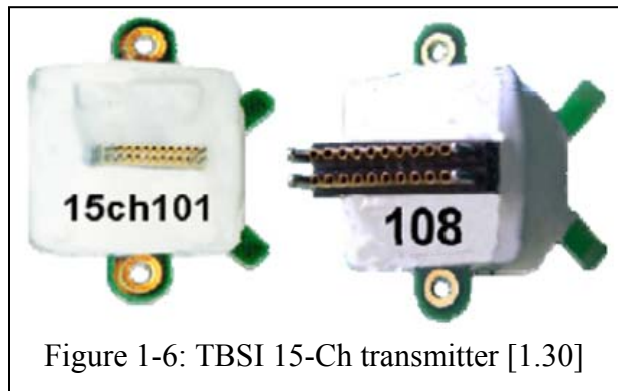


Figure 1-6: TBSI 15-Ch transmitter [1.30]

noise of the 15-Ch transmitter is $10\mu V_{rms}$, channel gain is $600\times$ with a pass band from 0.9Hz to 6KHz, its dimensions are $16mm\times 17.2mm\times 8mm$, and weighs 4.0g including the

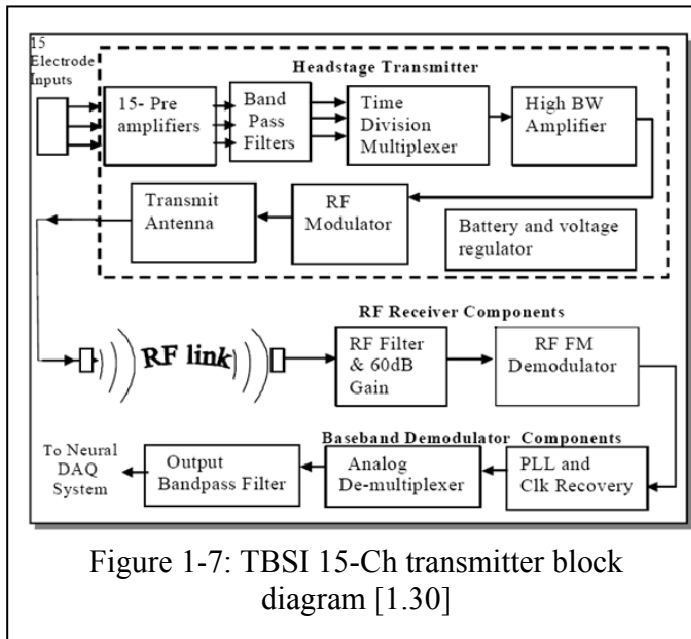


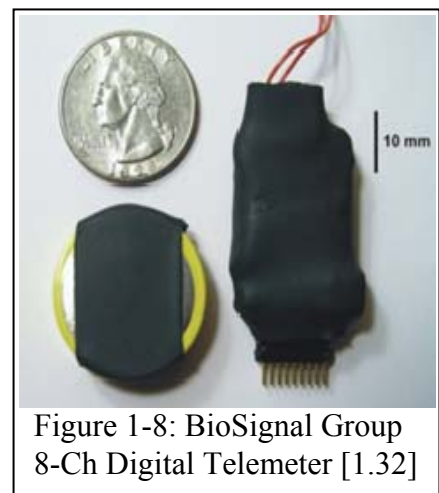
Figure 1-7: TBSI 15-Ch transmitter block diagram [1.30]

custom rechargeable battery. Transmission range is 3m and it lasts for 5.5hrs on its custom made rechargeable 3V battery. The system is based on a Fully Analog TDM-FM architecture in which the channels are multiplexed in time and sent out using Frequency Modulation as

shown in figure 1-7. Due to weight of TBSI transmitters they cannot be used for wireless neural recording from small animals.

Telespike from AlphaOmega [1.31] is an example of commercial digital wireless biotelemetry devices. TeleSpike can monitor neural and LFP signals from 8/16 electrodes, transmitting only one continuous channel or spike events on all the channels to the host computer that can be located up to 3m away at 2.4GHz frequency range. Its dimensions are $57\text{mm}\times 39\text{mm}\times 18\text{mm}$; operates up to 3.5 hours from a custom rechargeable 3V battery and weighs 34g including the battery. Other than signal conditioning, TeleSpike contains an onboard Digital Signal Processor (400MIPS), on-chip memory, and USB interface which allows the implementation of various neural signal detection, sorting and analysis algorithms. This device sends out only one channel in continuous mode; alternatively TeleSpike can transmit spike events on all the channels to the receiver. Due to the large weight (34g) and limited number of continuously transmitted neural channels (1-Ch), TeleSpike cannot be employed in the intended applications of the proposed work.

Finally Digital Telemeter from BioSignal Group [1.32] transmits 2, 4, 8 or 16 channels of respectively 24, 24, 16, or 8-bit-digitized neural spikes over a distance of 8m, weighs 16g including the rechargeable 3V coin cell battery, and operates up to 2 hours with dimension of $23\text{mm}\times 35\text{mm}\times 7.5\text{mm}$ (figure 1-8). The power consumption of the

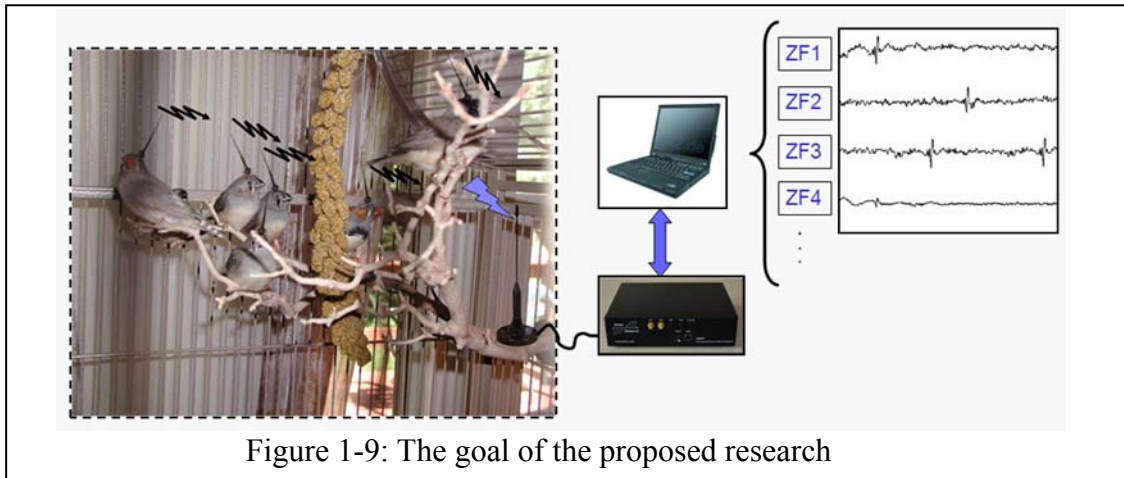


transmitter unit is 360mW. Due to size and weight constraints none of BioSignal Group

wireless biotelemetry products are suitable for wireless neural recording from small animals.

1.4. Proposed Research

Figure 1-9 depicts the goal of the proposed research in which the multichannel neural data from the animal subject's central nervous system (CNS) are sent out by the



neural transmitter, received wirelessly and demodulated by a single receiver controlled through the host computer. Finally, the recovered neural channels are processed, displayed and recorded in realtime by the host computer.

During the course of this project various fully-analog, time-division-multiplexing, frequency-modulation (FA-TDM-FM), multichannel wireless neural recording transmitters were designed and assembled as shown in figure 1-10. Through employing these systems in various in-vivo experiments, the requirements for reliable wireless neural recording are identified and the conflicting requirements of power/reliability are addressed in the proposed wireless biotelemetry microsystem: *NC_V3*.

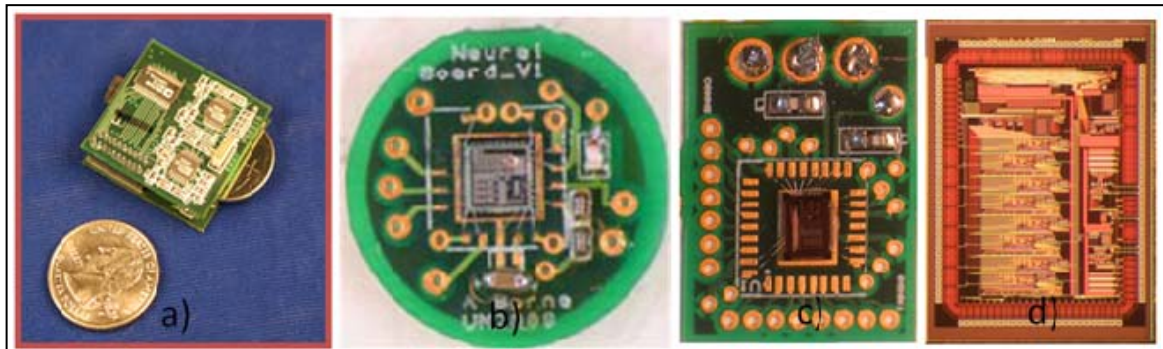


Figure 1-10: The FA-TDM-FM wireless biotelemetry devices developed during the course of this project: a) *FMT_V1*: the discrete 15-ch, b) *NC_V1*: the 3-ch ASIC, c) *NC_V2*: the 9-ch ASIC, and d) *NC_V3*: the 9-ch ASIC.

The latest neural transmitter, *NC_V3*, is implemented using a fully-analog, time-division-multiplexing, frequency-modulation (FA-TDM-FM) architecture and is demonstrated in figure 1-11. In this transmitter eight channels are dedicated to the neural signals and one channel is dedicated to the audio channel. The transmitter is optimized at the block level using the analytical tool Signal-Path-Co-Optimization (SPCO) discussed in chapter 2.

NC_V3 is a 9-channel (8 neural channels, 1 audio channel), user programmable, reliable wireless neural telemetry microsystem with a weight of 2.2g including the 2×1.5V silver-oxide batteries (Energizer-337 [1.33]), and dimensions of 2.2×1.1×0.5cm³. The transmitter consumes 4.2mW-5mW and has a total input referred noise of 4.74μV_{rms}, 6.47μV_{rms}, and 8.27μV_{rms} at transmission distances of 3m, 10m, and 20m, respectively. The inter-channel crosstalk is less than 3.5%. This ASIC has an area of 2.85×3.84mm² and is fabricated in a 0.5μm 2P2M n-well CMOS process. As shown in figure 1-11, the microsystem is composed of 2 vertically stacked boards; the bottom board contains the ASIC, the two RF inductors, and the batteries; the top board houses the antenna. The electrode signals are amplified by 40dB through the analog front-end which employs

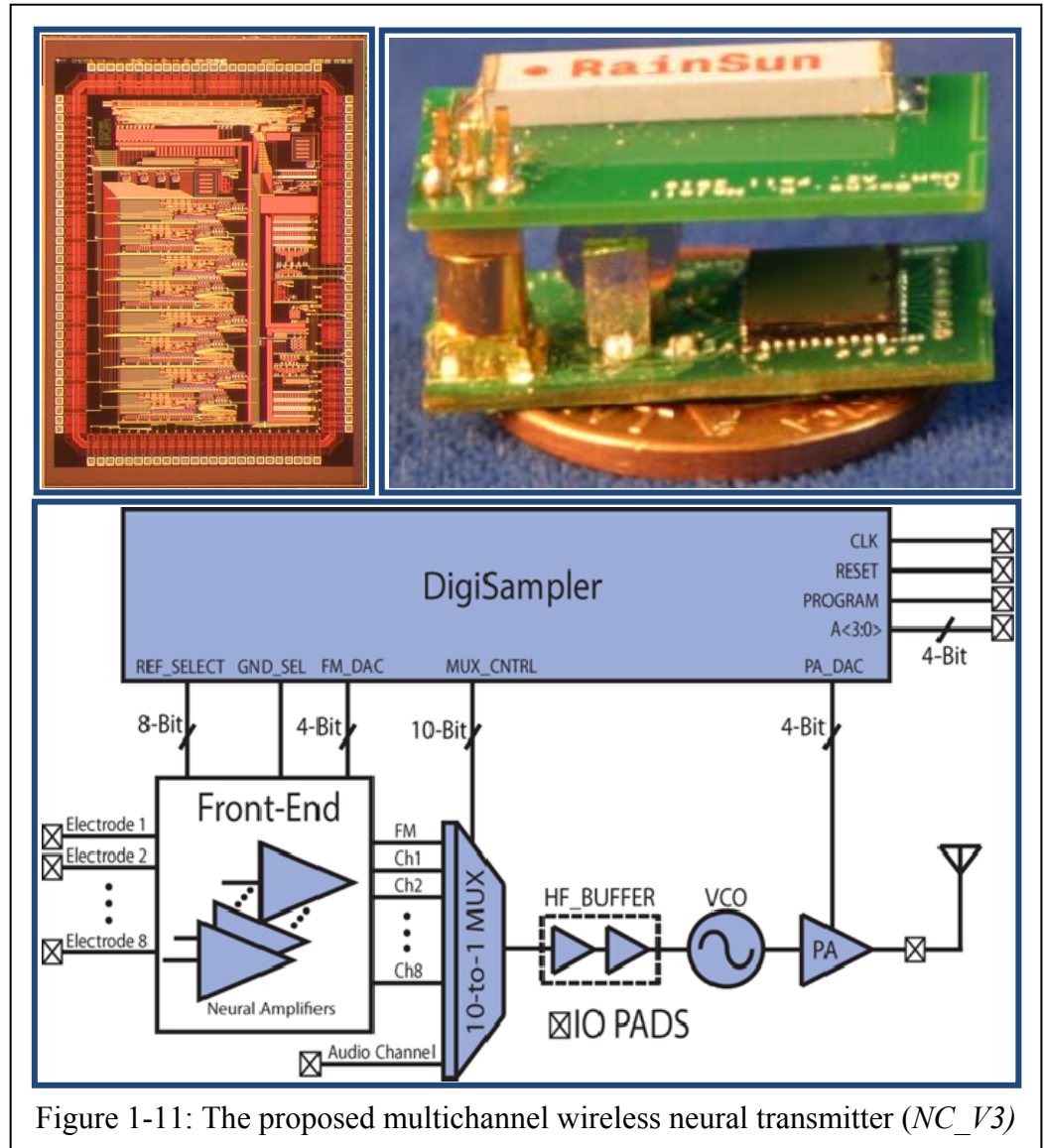


Figure 1-11: The proposed multichannel wireless neural transmitter (*NC_V3*)

local-bias-voltage, global-reference-current scheme. The global bias currents ($1\mu\text{A}$) are generated by 4 adjustable V_{th} referenced current sources and routed to individual neural amplifiers. A user programmable subset of the 8 available neural channels is multiplexed in time, and the resulting TDM signal is frequency modulated in the ISM band of 433MHz. The FM modulated RF signal is sent to a commercial 50Ω chip antenna by a class-C RF PA. The digital section (DigiSampler) is composed of a synthesized core, and

full custom designed peripheral blocks dissipating $24\mu\text{W}$ from the bottom 1.5V battery. DigiSampler adds flexibility to the microsystem by: *i)* generating the user-adjustable on-chip sampling CLK, *ii)* selecting any subset of neural channels for TDM, *iii)* configuring the front-end's signal path for common noise rejection, and *iv)* setting the transmitter's emitted RF power.

The analog front-end of the transmitter consists of: *i)* a bank of eight neural amplifiers, *ii)* the reference-channel circuitry, and *iii)* frame marker generator. The front-end amplifies the extracellular action potentials in the frequency band of 200Hz-8.5KHz by 40dB and generates the frame marker. The front-end's signal path is user-adjustable through 9-bits; having a flexible signal path helps in removing the common mode noise sources, e.g. 60Hz. The neural amplifiers of the front-end are implemented using a novel active-low-frequency-suppression (ALFS) architecture with micro-volt (μV) input referred offset. The ALFS dynamically suppresses all the low frequency noise components (amplifier's intrinsic offset, local field potentials, Flicker noise, and muscle movement artifacts), and amplifies the input signal of interest. This is done by extracting the low frequency signal components from the amplifiers output node using the miller integrator, and feeding them back to the gain stage's input differential pair. The neural amplifier once configured for BPF has a measured input referred voltage noise of $2.4\mu\text{V}_{\text{rms}}$ and $3\mu\text{V}_{\text{rms}}$ for power consumptions of $28\mu\text{W}$ and $14\mu\text{W}$, respectively. In ALFS configuration it has a measured input referred voltage noise of $5.2\mu\text{V}_{\text{rms}}$ and $5.86\mu\text{V}_{\text{rms}}$ at power consumptions of $31.5\mu\text{W}$ and $17\mu\text{W}$, respectively.

The RF front-end, reported in [1.34], is composed of a FM modulator followed by a class-C RF PA driving an off-chip commercial chip-antenna. The RF modulator is a

single-transistor Colpitts VCO with 2 on-chip capacitors, 1 off-chip inductor and an array of 12 PMOS varactors. The oscillator gain is adjustable and is set to 9.67MHz/V. To prolong the battery lifetime, the load of the VCO is on the bottom 1.5V battery while the PA is powered from the top 1.5V battery. The VCO's power consumption is set by an array of current mirrors from 495 μ W to 1.485mW. The VCO's generated wideband FM signal (~2MHz) in the ISM frequency band of 433MHz is amplified by a class-C PA. To meet the low power requirements, the RF PA is eliminated in some works [1.16, 1.25]; other than limiting the transmission range, the elimination of the PA terminates the back telemetry. The presented PA has 2 on-chip capacitors and one off-chip inductor. The LC-tank capacitor forms a tapped resonator up-converting the antenna impedance for power saving. In recording setups where the wireless biotelemeter is located close to the receiver's antenna ($d < 1\text{m}$), the antenna's emitted power can be reduced to trade transmission distance for battery lifetime. To change the emitted power, the PA's gate DC bias is adjusted through a 4-bit DAC. The PA has a maximum measured drain efficiency of 33% and a maximum measured antenna power of 1.457mW. The audio signal is provided by the low power COTS microphones (SPM0408HE5H) [1.35] and routed directly to the on-chip TDM multiplexer. The programmable architecture of NC_V3 allows the user to optimize the performance metrics of interest (battery lifetime, recovered neural channel SNR, etc.) based on the requirements of the specific experiment.

On the receiver side, the received wideband frequency-modulated (WBFM) RF signal is demodulated using software defined radios controlled by the host computer. Other than demodulation the host computer is also responsible for neural channel

recovery which consists of: *i*) time division demultiplexing, and *ii*) filtering. FM demodulation, time-division-demultiplexing, and neural channel filtering are integrated in a user friendly GUI program implemented in the Windows based Matlab environment.

Table 1-1 summarizes the wireless neural recording systems. The colored rows pertain to metrics vital for multichannel wireless neural recordings from small animals. The blue color is satisfactory, yellow is mediocre and red is unsatisfactory. A system which has all its columns in blue is the suitable one for the proposed application. To compare the performance metrics of the wireless neural telemetry systems, a figure-of-merit (FOM) is defined as the reciprocal of the power spent on broadcasting one channel over one meter distance. The state-of-the-art wireless multichannel neural transmitters are compared in table 1-1 and as shown the presented microsystem has the highest FOM compared to all research and commercial systems.

Table 1-1: Wireless Neural Recording Microsystems Performance Comparison

	Harrison, [1.19] (2010)	Shregardus, [1.22] (2006)	Bae Lee, [1.18] (2010)	TBSI, W5 [1.30]	TBSI, W16 [1.30]	TBSI, W32 [1.30]	TBSI, W64 [1.30]	Presented Work
Number of Channels	2/4	1	32	5	15	31	62	8/9
Standalone Microsystem	yes	yes	no	yes	yes	yes	Yes	yes
Weight	0.79g	1.1g	NA	2.7g	4g	4.8g	4.8g	2.2g
Dimensions (cm³)	0.9×1.3×0.5	1.2×0.5×0.8	NA	1.5×1.1×0.5	1.6×1.7×0.8	1.7×1.9×0.8	1.5×2×1.2	1.1×2.2×0.5
Microsystem Lifetime (hrs)	2hrs	20hrs	NA	3.5hrs	5.5hrs	5hrs	5hrs	1hr
Transmission Range	2m	6m	1.5m	4m	4m	4m	4m	20m
Power Consumption	2.64mW	14mW	5.8mW	32.45mW	32.45mW	32.45mW	32.45mW	5mW
FOM $\left(\frac{Power}{N_{ch} \times R_{TX}}\right)^{-1}$	0.152×10^4	0.029×10^4	0.827×10^4	0.062×10^4	0.185×10^4	0.382×10^4	0.764×10^4	3.2×10^4
Back Telemetry Frequency	920MHz	482.3MHz	845MHz/915MHz	3.05GHz	3.05GHz	3.05GHz	3.05GHz	433MHz
Supply Voltage	±1.5V	±1.4V	±1.5V	3V	3V	3V	3V	±1.5V
Process	0.5µm CMOS	NA	0.5µm CMOS	NA	NA	NA	NA	0.5µm CMOS
Implementation	Single Chip	Discrete	Single Chip	NA	NA	NA	NA	Single Chip
Communication Scheme	FSK	FM	TDM-PWM-FSK	NA	NA	NA	NA	TDM-FM

The specific contributions of the proposed research are:

- Design and assembling of a 9-Ch (8 neural channels + one audio channel), light weight (2.2g), small size ($1.1 \times 2.2 \times 0.5 \text{cm}^3$), long range ($>20\text{m}$), low power ($< 5\text{mW}$) fully analog, time-division-multiplexing, frequency-modulation wireless biotelemetry microsystem intended for reliable neural recording from small animal models.
- Identifying the requirements for reliable wireless neural recording and addressing the conflicting issues of reliability and low power at both the circuit and architectural levels in the proposed wireless biotelemetry microsystem (*NC_V3*)
- Formulating the reliability criteria and optimization of the microsystem's signal path through the analytical tool so called Signal Path Co-Optimization which provides the designer with the insight to optimize performance metrics of a generic FA-TDM-FM wireless transmitter given a limited power and bandwidth budget.
- Introducing a novel front-end which employs active-low-frequency-suppression in a user-adjustable signal path, to cancel Flicker ($1/f$), process and temperature variation induced random inter-channel offsets, dynamic offset drifts, movement artifacts, 60Hz noise, and low frequency signals, e.g. local field potentials, Montecarlo simulations and measured data have proved that the proposed front-end is very robust in face of extreme process and temperature variations.
- Introducing a low power, unidirectional, user-adjustable wireless interface for back telemetry of biological data in reliable multichannel wireless systems. This RF front-end operates in the industrial, scientific, and medical band of 433MHz and is composed of: *i*) a low power ($495\mu\text{W}$), low voltage (1.5V) voltage controlled oscillator with an oscillator gain of 9.67MHz/V , and *ii*) a user-adjustable, low voltage (1.5V) RF power

amplifier which trades power consumption for transmission range; the PA has a maximum measured drain efficiency of 33% and a maximum measured antenna power of 1.457mW.

- System integration for the developed wireless biotelemetry microsystem and employing software defined radios (SDR) for demodulation of the received WBFM RF signal.

Consequently the outcome of this research will provide the neuroscience community with reliable, low cost, wireless biotelemetry systems.

The remainder of this thesis is organized as:

Chapter 2: introduces the concept of reliability with regards to the FA-TDM-FM architecture; circuit-level techniques to meet the electrical specification pertaining to reliability are presented. The Signal-Path-Co-Optimization (SPCO), the analytical tool needed to meet the conflicting requirements of low power and reliability, is introduced; and high level design choices affecting the system's electrical and physical specifications are discussed in details through using SPCO.

Chapter 3: presents the preliminary microsystems, developed during the early phase of this project, which served as the test vehicle to identify the system's reliability requirements.

Chapter 4: reports on the design and performance characterization of the individual analog/digital/RF circuit blocks employed in the latest multichannel wireless neural recording transmitter: *NC_V3*.

Chapter 5: discusses the external electronics used to recover the wirelessly received neural channels.

Chapter 6: reports on the overall system performance characterization and in-vivo test results on South Americano cockroach.

Chapter 7: concludes the work of this thesis, underlines the major contributions of the presented research, and proposes further opportunities for research in this field.

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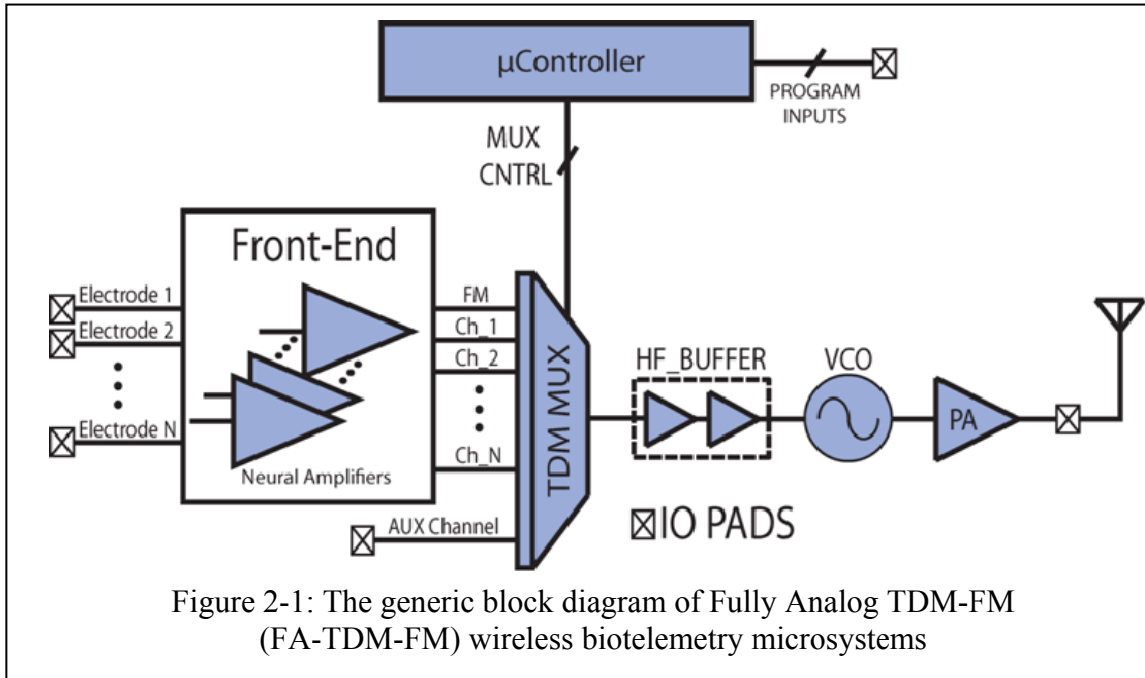
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CHAPTER 2

SYSTEM LEVEL ANALYSIS AND OPTIMIZATION

2.1. The Fully Analog TDM-FM Architecture

The work in this thesis focuses on a low power, light weight, multichannel time-division-multiplexing, frequency-modulation (FA-TDM-FM) wireless biotelemetry system intended for reliable neural recordings. FA-TDM-FM wireless biotelemetry systems have been developed and employed in neural recordings by quite a few groups [2.1, 2.2, and 2.3]. A generic block diagram of this architecture is shown in figure 2-1. In the intended application of this work, extracellular single-unit neural spikes, with amplitude of $50\mu\text{V}_{\text{pp}}$ - $500\mu\text{V}_{\text{pp}}$ and frequency content of 500Hz-10kHz, are sensed by electrodes (with an impedance of $\sim 1\text{M}\Omega$ at 1kHz) implanted in the extracellular space of the central nervous system (CNS). The small amplitude neural signals are amplified by a bank of neural amplifiers; the neural amplifiers provide gain to signals in the frequency band of 500Hz-10KHz and must have less than $10\mu\text{V}_{\text{rms}}$ of input referred noise. Other than amplification, the front-end is responsible for electrode-ECF (extracellular fluid) interface offset rejection, which can be as large as $\pm 0.5\text{V}_{\text{DC}}$ at the amplifier input; furthermore the amplifiers band pass filter the channels to prevent aliasing in the subsequent sampling stage. The amplified channels are then multiplexed into a continuous stream of data using time division multiplexing (TDM). The frame marker channel (FM) is used at the receiver for demultiplexing. The TDM is implemented by an analog multiplexer controlled by the



digital block. The digital block generates the on-chip sampling clock to eliminate the need for bulky off-chip components. The multiplexed data stream is buffered by a wide bandwidth unity gain buffer which preserves the sharp discontinuities introduced by the TDM process. The buffer drives the frequency modulator (FM) implemented by a Colpitts voltage controlled oscillator (VCO). The VCO output can be directly coupled to the antenna [2.1], or a power amplifier (PA) can be used to enhance the transmission range and decouple the antenna from the *LC*-tank of the RF modulator.

One should note that reliability and low power are two conflicting requirements and to achieve both, the system performance has been optimized through an analytical tool called signal path co-optimization (SPCO), developed in this work. SPCO is an analytical tool which provides the designer with the insight to choose various system level parameters given a limited power and bandwidth budget. The microsystem is assembled in a miniaturized package and applied in various wireless neural recordings from small, awake, and freely moving subjects.

2.2 Reliability in Wireless Biotelemetry Systems

The system requirements for reliable neural recording from small subjects can be divided into physical specifications and electrical specifications. The physical specifications are: *i*) light weight ($<1\text{g}$), and *ii*) small size ($<1\text{cm}^3$). Limited carrying capability of the small subjects necessitates the total weight of the wireless neural transmitter to be less than 1g. Furthermore since the transmitter is to be installed on the skull of the test subject, the size of the transmitter should be about 1cm^3 to facilitate the device encapsulation. These physical specifications put stringent constraints on the transmitter's power which inherently is in conflict with the reliability and robustness of the overall system.

Electrical specifications are related to signal quality and the overall system reliability. The reliability can be defined as the characteristic of a biotelemetry system employing which no extracellular action potential is lost, or falsely flagged as it is being transmitted over a reasonable distance for the whole duration of the in-vivo experiment. Specifically the reliability requirements for wireless multichannel neural recording systems are: *i*) low inter-channel crosstalk levels ($XT < 5\%$), *ii*) small input referred noise of the entire system including the biotelemeter, wireless link and the external electronics ($V_{noise} < 30\mu V_{rms}$), *iii*) back telemetry over a reasonable distance ($>3\text{m}$), *iv*) continuous neural recordings, and *v*) long recording sessions ($>1\text{hr}$). The electrical specifications related to system reliability are discussed in details:

***i*) Crosstalk (XT):** In multichannel neural recording systems, inter-channel crosstalk is an important performance metric affecting the overall system reliability. Inter-channel crosstalk refers to any phenomenon by which a signal on one neural

channel creates an undesired effect in another neural channel. As mentioned earlier the purpose of this work is to develop systems which enable neuroscientists to decode the brain circuits. Having a false action potential flagged on one of the electrode sites, due to crosstalk, can lead to misunderstanding of the brain circuits. The source of crosstalk depends on the signal path. Regarding the system proposed in this work, in one end is the electrode implanted in the host's CNS and at the other end is the host computer processing and displaying electrodes' waveforms in real time. In fully analog, TDM-FM systems the eight possible sources of crosstalk, in the order of neural signal propagation, are:

- 1) **Adjacent Electrode Sites:** in an in-vivo neural recording experiment where electrodes are implanted in one of brain circuits, e.g., the auditory cortex, the distance between electrodes can be as short as few tens of micrometers. A population of neurons can be equidistant from multiple electrode sites and once the neurons fire, the action potentials will be sensed by all the nearby electrode sites; these action potentials are all sensed almost at the same time on the nearby electrodes and the user might interpret some of the electrodes neural spikes as crosstalk from other channels. This type of crosstalk can be recognized by applying offline spike sorting algorithms to the recorded channel waveforms and is not of concern to circuit designer.
- 2) **Electrodes' Interconnects:** the exposed electrode sites are connected to electronics through interconnects and wirebonds. These closely packed interconnects and wirebonds are prone to capacitive and inductive couplings which can lead to crosstalk. However considering the frequency spectrum ($<10\text{KHz}$) and amplitude ($<500\mu\text{V}_{\text{pp}}$) of neural spikes, the crosstalk level contributed by electrodes'

interconnects is negligible and can be avoided with proper design of the electrode interconnects.

- 3) **Power Supply:** Wireless biotelemetry microsystem ASICs with inefficient power grid and poor Power-Supply-Rejection-Ratio (PSRR) of neural amplifiers (e.g., open-loop designs) may exhibit a significant crosstalk level; in the proposed work this source of crosstalk is avoided by employing closed-loop neural amplifiers with large PSRR; furthermore the power supply rails are laid out with star-topology and have proper width regarding the number of neural channels and power consumption per channel.
- 4) **Front-End Layout:** The front-end output wires carry the amplified neural spikes which can be hundreds of millivolts in amplitude. If the front-end output wires are not laid out properly, the capacitive coupling among interconnects can lead to significant inter-channel crosstalk level. The crosstalk level contributed by capacitive coupling is proportional to the ratio of capacitance among the adjacent wires to the output resistance of the victim channel. In the presented work this type of error is minimized by guarding the front-end output wires with ground shields to separate them electrically from adjacent wires; also the output wires are driven by buffers with low output impedance to further reduce the inter-channel crosstalk.
- 5) **TDM Multiplexer:** During the sampling window of each channel, the TDM multiplexer output is driven by the channel's neural amplifier. The TDM multiplexer output capacitance (in the range of pF) along with the output resistance of the selected neural amplifier, in the range of few $K\Omega$, creates a first order RC circuit. The transient time it takes the multiplexer output to settle down to its steady state should

be less than 5% of the sampling window. As the number of channel increases and so does the sampling frequency, the transient time stays constant and therefore the transient time becomes a significant portion of the sampling window; this phenomenon can be a significant contributor to the total system's crosstalk. In the proposed work, this type of crosstalk is avoided by designing multiplexer's output capacitance and neural amplifiers' output resistance according to the required maximum sampling frequency.

- 6) **TDM Buffer:** the unity-gain buffer inserted between the TDM multiplexer and the RF modulator plays an important role in total inter-channel crosstalk level. As the bandwidth of the buffer reduces, the transitions between adjacent sampling windows become smoother, as opposed to sharp discontinuities observed at the output of TDM multiplexer, leading to crosstalk among sequenced channels. To minimize the crosstalk from this source, a wide bandwidth buffer with adjustable bandwidth is employed. This is an example of trading power for signal integrity.
- 7) **VCO:** the response time of VCO also affects the overall system's crosstalk level; the abrupt voltage difference between the sampled channels, requires the VCO to settle down to the steady state frequency within at most 5% of sampling window. It should be noted that this criterion is different from VCO's start-up time, which is irrelevant in FA-TDM-FM architecture as the VCO runs continuously. The proposed VCO's response time is not measured, however noting the overall system crosstalk (<5%) the VCO's response time is adequate for the intended application.
- 8) **Receiver Bandwidth:** the most important source of crosstalk in FA-TDM-FM systems is the limited receiver bandwidth. In the proposed work, to enhance the

neural channels signal-to-noise-ratio (SNR) at the receiver, the on-chip VCO has an adjustable large oscillator gain (1-14MHz/V), and consequently the modulation is wideband-FM (WBFM). In WBFM modulation, the occupied spectrum is a function of modulating input amplitude, oscillator gain and frequency contents of the modulating input. If the available receiver bandwidth is narrower than the received signal spectrum, inter-channel crosstalk can be observed (section 2.3.1.3). Therefore there is a tradeoff between receiver's bandwidth, VCO's oscillator gain, number of sampled channels, and front-end gain. These inter-related parameters have been optimized through signal-path-co-optimization (SPCO) for a given receiver's bandwidth (6MHz).

ii) Input Referred Noise: the neural spikes vary in amplitude from $50\mu V_{pp}$ - $500\mu V_{pp}$; therefore as a rule of thumb the total system's input referred noise must be less than $30\mu V_{rms}$. There are various sources contributing to system's total noise:

- 1) **Front-End:** the neural amplifiers play the most important role in noise reduction. As a rule of thumb the neural amplifiers input referred noise must be less than electrode's thermal noise which is about $10\mu V_{rms}$ in the frequency band of interest (500Hz-10kHz) [2.10]. This issue is addressed by the proposed front-end which has a measured input referred voltage noise of $1.8\mu V_{rm}$ in the frequency range of 100mHz-50KHz.
- 2) **Mixed Signal Noise:** the ASIC, other than the analog front-end, includes the RF and digital blocks. In the proposed ASIC, to reduce the RF/digital noise on the sensitive signal path the following technique have been used: *i)* a separate power/ground lines are assigned to each block, *ii)* amplitude of RF/digital signals are limited to half the

- rail-to-rail supply voltage to minimize the noise injected into the substrate, *iii*) noisy RF/digital blocks are surrounded by guard rings to collect the charge carriers injected into substrate, *iv*) the sensitive front-end blocks are guarded with guard rings to prevent the stray substrate carriers from reaching the sensitive front-end nodes.
- 3) **VCO's Phase Noise:** the phase noise of the VCO will be down converted into the baseband and contribute to the total noise. Harmonic oscillators have better phase noise performance than relaxation oscillators; among the harmonic oscillators the LC-tank Colpitts oscillators have the best phase noise performance [2.11] and therefore in the proposed work a low power ($495\mu\text{W}$) LC-tank Colpitts VCO with a simulated phase noise of -76dBc/Hz at an offset of 10KHz from the 433MHz center frequency is used. Furthermore, in section 2.3 it is shown that in FA-TDM-FM systems the VCO's phase noise is not a major contributor to the total noise compared to other noise sources, e.g. the front-end and receiver thermal noise.
 - 4) **RF Interference:** RF interferences are always present in the back telemetry wireless link; as a rule of thumb the higher the RF transmission frequency the lower the RF interference. However due to large power consumption of RF blocks at high transmission frequencies some intermediate band should be selected for the wireless link. The best solution to reduce the RF interference is to have the test subject's cage electromagnetically shielded. In the proposed work the ISM band of 433MHz is utilized for back telemetry of neural data.
 - 5) **Receiver Bandwidth:** receiver bandwidth should be large enough to capture the wide spectrum of the WBFM signal emitted by the microsystem; however if it is larger than the received signal spectrum, the input referred noise of the total system

increases. Therefore the receiver bandwidth should be adjusted according to the transmitter's frequency spectrum which in turn is a function of oscillator gain, front-end gain, number of channels and the desired inter-channel crosstalk level. In the proposed work the receiver bandwidth can be adjusted from 500KHz to 6MHz.

iii) Transmission Range: to have a minimum transmission distance of 3m, the antenna must be driven by a RF power amplifier (PA). Furthermore active antenna can be used in the receiver to enhance the minimum detectable signal [2.12, 2.13]. In recording setups where the wireless microsystem is located close to the receiver's antenna ($d < 1\text{m}$), the antenna's emitted power can be reduced to increase battery life. In the proposed microsystem, to change the emitted power, the PA's gate DC bias is adjusted through a 4-bit DAC. The PA has a maximum measured drain efficiency of 33%, a maximum measured antenna power of 1.457mW, and drives a 50Ω , off-chip, miniaturized chip-antenna (ANT1603-433) [2.14]. Consequently the presented neural transmitter has a measured transmission distance of more than 20m.

iv) Continuous Neural Recording: It is essential that the employed biotelemetry system recovers the input neural activities during the in-vivo experiment with no loss. The recovery of the wirelessly transmitted neural data may be interrupted due to several sources:

1) **Power Supply Disconnect:** battery holders must be robust to provide the supply voltage to the microsystem despite the perturbations induced by the subject's movements; the off the shelf battery holders are robust but their weight and size make them unattractive for light-weight microsystems. A light-weight and custom made battery holder is used in the presented microsystem.

- 2) **RF Antenna Coupling:** in transmitters where antenna is directly coupled to the VCO's *LC*-tank, signal transmission can be terminated as the antenna gets in contact with nearby objects; this phenomena is observed in some systems [2.1]; to avoid this problem, in the presented work, the antenna is driven by the PA which technically decouples the antenna from the RF modulator; therefore the back telemetry of neural data is not terminated when the antenna is in contact with non-conductive objects.
- 3) **Front-End Offset:** in a Fully Analog TDM-FM (FA-TDM-FM) wireless biotelemetry microsystem, the front-end's output offset is one of the most important factors affecting system reliability and functionality. The front-end offset stems from the electrode-ECF (extracellular fluid) interface offset and the front-end's intrinsic offset. The electrode-ECF interface offset can be as large as $\pm 0.5V_{DC}$; this offset should be rejected by the neural amplifier such that the output offset is a small fraction of the amplified neural signal. The front-end intrinsic offset alone can be detrimental in FA-TDM-FM systems. The work presented in [2.4] has a measured input referred offset of $550\mu V$ which for a gain of $100\times$ leads to $55mV_{DC}$ offset at the front-end output; such random inter-channel offsets will saturate the wireless link due to the large oscillator gain of the VCO stage and limited receiver bandwidth. The same work once commercialized dissipates $40mW$ [2.5] for 16 neural channels. Therefore, there are two conflicting requirements for the front-end: on one hand the neural amplifier should be low power to suit the systems with large number of channels; on the other hand it should have low offset. Even if an infinite receiver bandwidth was available to capture the wide spectrum resulting from the inter-channel front-end offset, such large bandwidth would increase the receiver thermal

noise and degrade the overall noise performance of the system. In this thesis a new architecture for active low frequency suppression of the front-end offset is proposed. The proposed front-end is based on the work presented in [2.6]. Montecarlo simulation has shown that the new front-end is very robust in the face of extreme process and temperature variations (PTV). Other than process induced inter-channel offset, amplifier offsets drift over time, leading to random inter-channel offset which will saturate the wireless link and consequently make the microsystem dysfunctional. This phenomenon has been observed in some of FA-TDM-FM systems [2.1, and 2.2] and consequently the system fails after few weeks of operation. The proposed active low frequency suppression architecture cancels the front-end's offset drift over time as well.

- 4) **Low-Frequency Suppression:** large-amplitude low-frequency signals can saturate the front-end and/or wireless link leading to temporarily loss of the input neural activity. The transmitter devices Flicker ($1/f$) noise, the test subject's local field potentials (LFP), the test subject's movement artifacts and the 60Hz noise are the main signals to be filtered before reaching the multiplexing stage. The proposed active low frequency suppression front-end will filter out all these noise sources. Furthermore the front-end can be programmed by the user to select any of the electrode signals as the reference channel which will efficiently eliminate the common mode noise sources.
- 5) **Light Insensitivity:** In many neural amplifiers to filter out the low frequency signal components high-value resistors are needed; these high-value resistors are implemented with subthreshold PMOS transistors [2.1, 2.2, 2.7, 2.8, and 2.9]. The

problem encountered with this implementation technique is light sensitivity of the front-end; this is due to the fact that the input terminal of the large-gain amplification-stage connects to ASIC's ground through a high impedance path created by subthreshold PMOS pseudo-resistor. In this pseudo-resistor, electron-hole pairs are generated with light; this light-induced current multiplied by the resistance of the pseudo-resistor, creates a light-dependent offset at the input of the neural amplifier which once amplified by the front-end's gain will saturate the neural amplifier. The proposed active-low-frequency-suppression front-end does not require the high value resistor at the input of the amplification stage and is light insensitive.

v) **Long Recording Sessions:** duration of the wireless neural recording experiment depends on the microsystem power dissipation and the choice of the batteries.

Furthermore the battery choice is bounded by the transmitter's weight. For a 1g microsystem (including the batteries), with power consumption of less than 5mW, various COTS miniaturized silver-oxide batteries [2.15] can be used. After each recording session the batteries can be easily replaced. If the

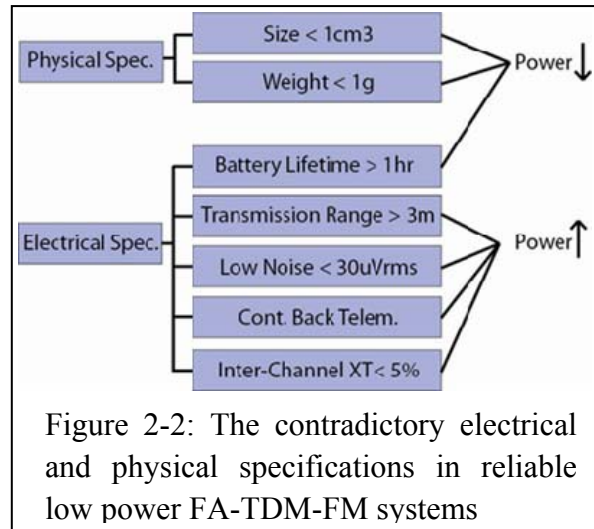


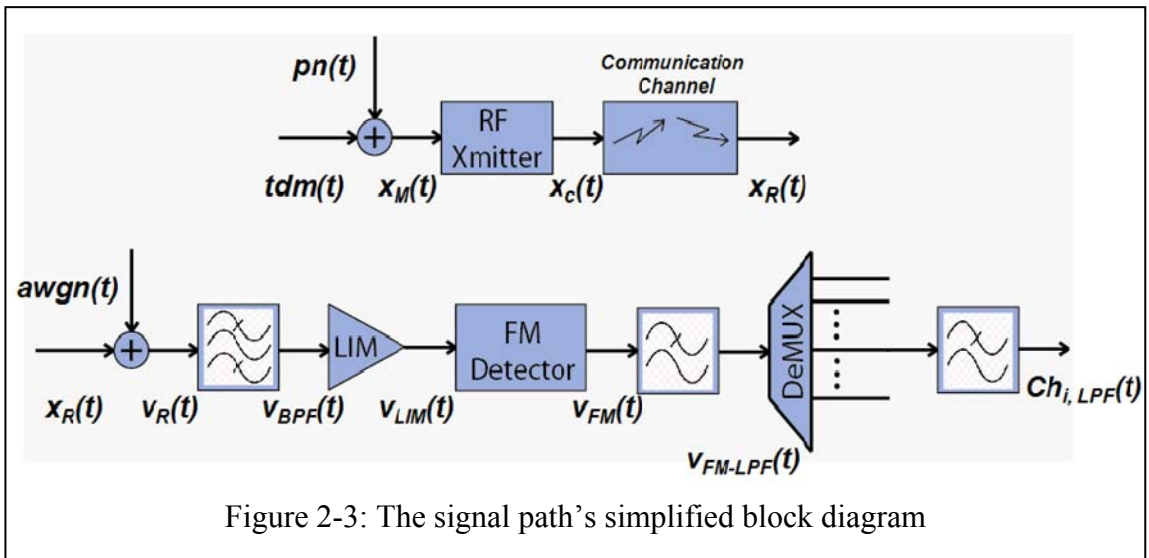
Figure 2-2: The contradictory electrical and physical specifications in reliable low power FA-TDM-FM systems

microsystem's power consumption is more than 6mW, miniaturized batteries are not an option and one has to employ large and bulky batteries. The proposed microsystem operates on two silver-oxide batteries (Energizer 337) with a total weight of 0.26g and is successfully applied in recording sessions conducted for one hour.

2.3 System Level Optimization: Signal Path Co-Optimization (SPCO)

As explained in section 2.2 and depicted in figure 2-2, the electrical and physical specifications are partly inter-related and partly contradictory; therefore to design a robust and reliable low power system, the various block parameters should be co-optimized. The signal path co-optimization (SPCO) is an analytical tool which derives the formulas for performance metrics of interest and allows the designer to choose a set of parameters to optimize performance metrics of interest while meeting a fixed power-bandwidth budget.

The signal-path-co-optimization (SPCO) optimizes the signal path, figure 2-3, according to the performance metric of interest. Due to small-amplitude nature of the neural spikes, the performance metric is defined as the signal to noise ratio (SNR) of the recovered neural channel at the receiver side.



2.3.1. The Transmitter Unit

2.3.1.1. Time Division Multiplexing: TDM

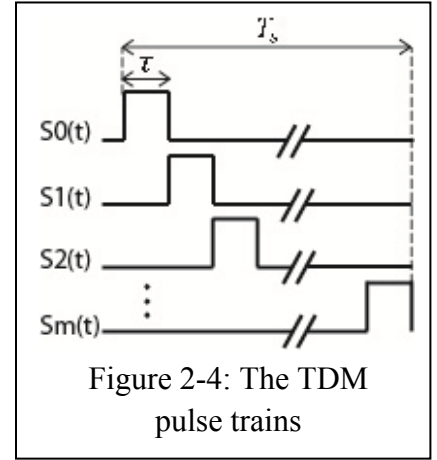
The amplified neural channels are noted as $x_1, x_2 \dots$ and x_m , while the frame marker ($F.M.$) is noted as x_0 . The bandwidth of each neural channel (x_i) is constant and equal to BW_{ch} (10KHz).

$$BW(x_1) = BW(x_2) = \dots = BW(x_m) = BW_{ch} \quad (2 - 1)$$

Each neural channel can be expressed in time domain as:

$$x_i(t) = FE_{gain} \times (v_{neural,i}(t) + n_{FE}(t)) + ch_{i,DC} \quad (2 - 2)$$

In 2-2, FE_{gain} is the front-end gain of the transmitter; $v_{neural,i}(t)$ is the neural signal sensed by the electrode; $n_{FE}(t)$ is the input referred noise of the channel, and $ch_{i,DC}$ is the channel's output offset. The time division multiplexed signal can be expressed in time domain, in terms of neural channels signals and the pulse trains (shown in figure 2-4). The non-overlapping pulse trains allow the time-division-multiplexed signal ($tdm(t)$) to be equal to one of the neural channels during each sampling window.



$$tdm(t) = x_0(t) \times s_0(t) + x_1(t) \times s_1(t) + \dots + x_m(t) \times s_m(t) \quad (2 - 3)$$

The sampling frequency per channel, f_s , is assumed to be constant at $2 \times BW_{ch}$ (20KHz) and has the following relationship with the sampling window (τ):

$$f_s = \frac{1}{T_s} > 2 \times BW_{ch} \rightarrow (m + 1) \times \tau < \frac{1}{2 \times BW_{ch}} \quad (2 - 4)$$

The Fourier transform of the non-periodic time division multiplexed signal, equation 2-3, can be calculated as:

$$\begin{aligned}
TDM(f) = & c_0 X_0(f) + c_1 [X_0(f - f_s) + X_0(f + f_s)] + c_2 [X_0(f - 2f_s) + X_0(f + 2f_s)] + \dots \\
& + c_0 X_1(f) + c_1 e^{-j\omega_s \tau} [X_1(f - f_s) + X_1(f + f_s)] + c_2 e^{-j\omega_s 2\tau} [X_1(f - 2f_s) + X_1(f + 2f_s)] + \dots \\
& + c_0 X_2(f) + c_1 e^{-j\omega_s 2\tau} [X_2(f - f_s) + X_2(f + f_s)] + c_2 e^{-j\omega_s 4\tau} [X_2(f - 2f_s) + X_2(f + 2f_s)] + \dots \\
& \vdots \\
& + c_0 X_m(f) + c_1 e^{-j\omega_s m\tau} [X_m(f - f_s) + X_m(f + f_s)] + c_2 e^{-j\omega_s 2m\tau} [X_m(f - 2f_s) + X_m(f + 2f_s)] + \dots \quad (2 - 5)
\end{aligned}$$

From 2-5, the neural channels are spread around the harmonics of the channel sampling frequency (f_s); the channel frequency spectrums are multiplied by the Fourier coefficients of the TDM pulse train (c_i) and each have a constant phase added. Also from 2-5, it can be concluded that the bandwidth of the $tdm(t)$ is infinite which is due to the abrupt discontinuity introduced in the time domain by the TDM process. However depending on the targeted level of crosstalk, the bandwidth can be reduced. The bandwidth of the time division multiplexed signal can be calculated based on the channel bandwidth and the sampling frequency per channel:

$$BW_{TDM} = p \times f_s + BW_{ch} \quad (2 - 6)$$

In 2-6, p is a positive integer number which should be calculated based on the targeted level of crosstalk. The crosstalk is defined in the time domain according to the figure 2-5 [2.16]:

$$k_{XT} = 10 \log\left(\frac{A_{xt}}{A}\right)^2 \quad (2 - 7)$$

In 2-7, A_{xt} is the residue of the previous channel voltage which is ideally zero; A is the voltage difference between the two consecutive sampled channels which is a function of the channels amplified action potentials and the channels output offsets as reflected in 2-8:

$$\begin{cases} Ch_{i-1}(t) = x_{i-1}(t) = x_{i-1,DC} + x_{i-1,AP}(t) \\ Ch_i(t) = x_i(t) = x_{i,DC} + x_{i,AP}(t) \end{cases} \Rightarrow A = (x_{i,DC} - x_{i-1,DC}) + (x_{i,AP}(t) - x_{i-1,AP}(t)) \quad (2-8)$$

From 2-8 and 2-7 it can be observed that the inter-channel offset variation also adds to the total crosstalk of the system; and therefore it is necessary to employ a small offset front-end to minimize the inter-channel crosstalk. The

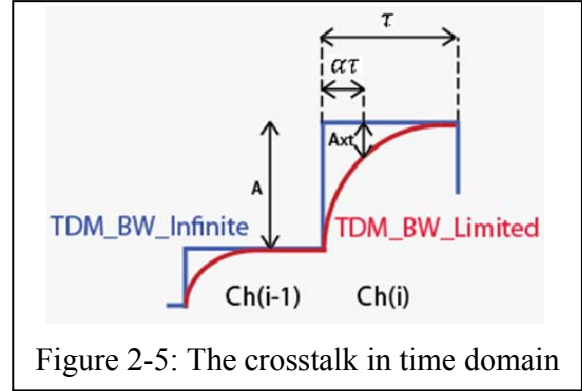


Figure 2-5: The crosstalk in time domain

sampling time is noted as t_{sample} and from figure 2-5 it is expressed as $\alpha\tau$:

$$t_{sample} = \alpha\tau = \frac{\alpha}{(m+1) \times f_s} \quad (2-9)$$

If the desired level of crosstalk is $XT \left(10 \log \left(\frac{A_{xt}}{A} \right)^2 < XT \right)$ the sampling time can be approximated:

$$t_{sample} \geq 0.0183 \times \left(-\frac{XT}{BW_{XT}} \right) \quad (2-10)$$

In 2-10, XT is the desired inter-channel crosstalk level in dB and BW_{XT} is the required bandwidth (Hz) to have XT level of crosstalk.

Substituting 2-10 into 2-9, the required bandwidth for XT level of crosstalk (dB) based on the channel sampling frequency and the number of channels can be calculated:

$$BW_{XT} = 0.0183 \times (m+1) \times f_s \times \frac{-XT}{\alpha} \quad (2-11)$$

The positive integer, p , introduced in 2-6 can be written as:

$$p > \left\lceil \frac{BW_{XT}}{f_s} \right\rceil \quad (2-12)$$

Substituting the 2-12 into 2-11, the positive integer, p , can be calculated as:

$$p > \left\lceil \frac{0.0183 \times (m + 1) \times f_s \times (-XT)}{\alpha f_s} \right\rceil \quad (2 - 13)$$

From 2-13 and 2-6 the bandwidth of the baseband TDM signal ($tdm(t)$) can be calculated based on the number of neural channels (m), the desired crosstalk level (XT), the sampling time ($\alpha\tau$), the sampling frequency per channel (f_s), and the channel bandwidth (BW_{ch}):

$$BW_{TDM} = \left\lceil \frac{0.0183 \times (m + 1) \times (-XT)}{\alpha} \right\rceil \times f_s + BW_{ch} \quad (2 - 14)$$

2.3.1.2. Frequency Modulation: *FM*

The time-division-multiplexed signal ($tdm(t)$) contains all the transmitter mixed signal noise except the RF transmitter's phase noise. As shown in figure 2-3, the RF transmitter's phase noise ($pn(t)$) is added to the ($tdm(t)$) and constructs the modulating input of the transmitter ($x_M(t)$).

On the transmitter the RF blocks apply the frequency modulation (FM) scheme to the modulating input. The output of the FM modulator is expressed as [2.16]:

$$x_c(t) = A_c \cos(\omega_c t + \phi(t)) \quad (2 - 15)$$

The neural channels data is embedded in the phase as:

$$\phi(t) = 2\pi f_\Delta \int_{-\infty}^t x_M(\lambda) d\lambda \quad (2 - 16)$$

In 2-16, f_Δ is the VCO's oscillator gain. The RF transmitter's modulating input is the superposition of the TDM signal and the VCO's phase noise which is referred to the VCO's modulating input:

$$x_M(t) = tdm(t) + pn(t) \quad (2 - 17)$$

Before calculating the power spectral density of $pn(t)$, the bandwidth of the frequency modulated TDM signal should be studied.

Like the TDM signal, the bandwidth of the frequency modulated signal is also infinite; by accepting some levels of distortion (<2%) this bandwidth can be estimated as [2.16]:

$$BW_{FM} = 2(A_m f_{\Delta} + 2BW_{TDM}) \quad (2 - 18)$$

In 2-18, f_{Δ} is the VCO's oscillator gain, A_m is the peak amplitude of the TDM signal, and BW_{TDM} is the bandwidth of the TDM signal.

The peak amplitude of the TDM signal can be expressed as:

$$2 \times A_m = F.M. - (Ch_{i,DC} + FE_{gain} \times V_{neural,i}) \quad (2 - 19)$$

In 2-19, the F.M. is the frame marker DC voltage, and $Ch_{i,DC}$ is the largest DC offset of the front-end channels. By inspecting 2-18 and 2-19 it can be seen that the inter-channel front-end offset increases the FM bandwidth; this effect is more pronounced in systems with large oscillator gain. Substituting the 2-19 and 2-14 into 2-18, the bandwidth of the FM signal emitted by the transmitter unit can be calculated based on the high level parameters of the transmitter:

$$BW_{FM} = f_{\Delta} \left(F.M. - (Ch_{i,DC} + FE_{gain} \times V_{neural,i}) \right) + 4 \left(\left[\frac{0.0183 \times (m+1) \times (-XT)}{\alpha} \right] \times f_s + W_{ch} \right) \quad (2 - 20)$$

2.3.1.3. The Receiver Limited Bandwidth

To demodulate the FM signal, the receiver needs to have a bandwidth of at least BW_{FM} calculated in 2-20. To understand the impacts of the receiver limited bandwidth on

the demodulated signal, the frequency spectrum of the TDM-FM signal should be inspected. Suppose the TDM signal is a normalized (peak amplitude of unity) pulse train with the mean of $\langle x(t) \rangle = m$ [2.16]. After removing the DC component from the pulse train, the instantaneous frequency of the FM signal and the resulting phase can be simply calculated. The instantaneous frequency is also a pulse train and the resulting phase is a saw tooth waveform. The frequency modulated signal can be calculated as:

$$x_c(t) = \text{Re}[A_c e^{j(\omega_c t + \phi(t))}] = A_c \text{Re}[e^{j\omega_c t} \times e^{j\phi(t)}] \quad (2 - 21)$$

But, $\phi(t)$ is periodic and so is $e^{j\phi(t)}$. Therefore $e^{j\phi(t)}$ can be expressed by a Fourier series:

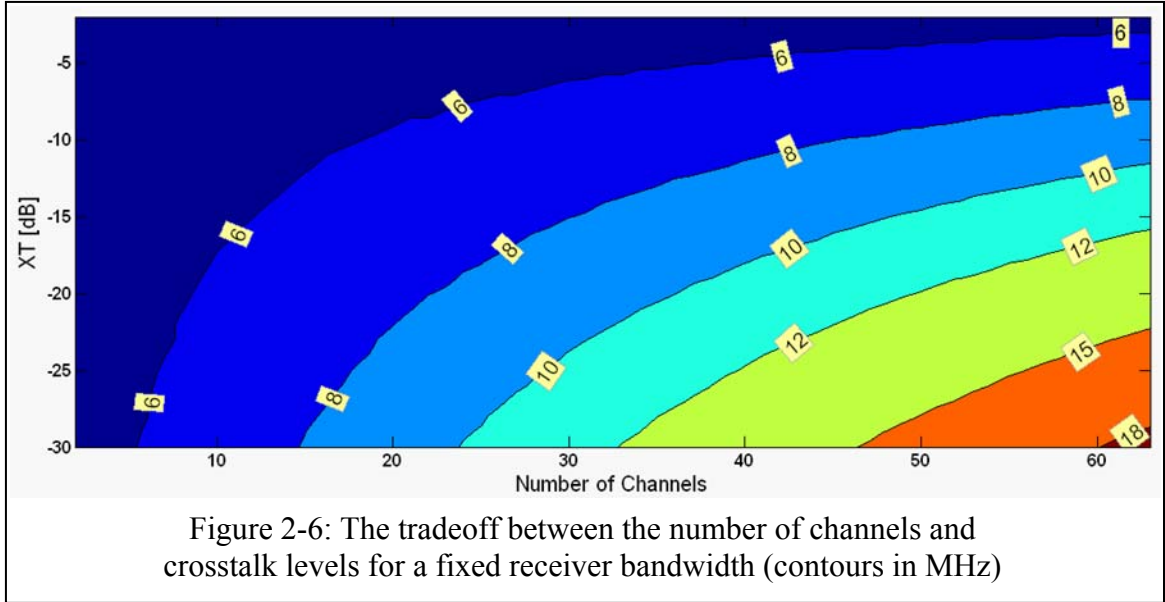
$$\left\{ \begin{array}{l} e^{j\phi(t)} = \sum_{n=-\infty}^{+\infty} c_n e^{jn\omega_0 t} \\ c_n = \frac{\beta m}{(\beta - n)m + n} \text{sinc}(\beta - n)m e^{j\pi(\beta+n)m} \end{array} \right. \quad (2 - 22)$$

Substituting 2-22 into 2-21, the frequency modulated signal is calculated:

$$x_c(t) = A_c \text{Re} \left[\sum_{n=-\infty}^{+\infty} c_n e^{j(\omega_c t + n\omega_0 t)} \right] \quad (2 - 23)$$

From 2-23 and 2-22 it can be proved that the spectrum peaks around $f_c + (1 - m)f_\Delta$ and $f_c - mf_\Delta$ which are the two instantaneous frequency originated from the voltage levels of the modulating train pulse [2.16].

The same principle holds true for the case of a TDM modulating input. In an ideal TDM-FM transmitter, the outputs offsets of the front-end channels are all zero and the only voltage fluctuation in the modulating TDM signal are due to the amplified action potentials. In such circumstances, the TDM-FM spectrum has two peaks: a smaller peak for the frame marker and a larger peak for the front-end signals. The difference in



spectrum peak amplitudes is due to the superposition of the Fourier coefficients in 2-23. If the receiver has enough bandwidth to capture the peaks in the frequency spectrum of the TDM-FM signal, but not enough to capture the tails, the demodulated TDM signal will have smoother transitions for adjacent channels. In this scenario, all the neural channels are recovered, however as explained in 2.3.1.1, the smooth channel to channel transitions increase the inter-channel crosstalk levels.

On the other hand if the front-end has large inter-channel offsets, the frequency spectrum of the TDM-FM signal peaks around the instantaneous frequencies of the channels, e.g. $f_c + Ch_{i,DC}f_{\Delta}$. In such a case, if the receiver does not have enough bandwidth to capture the whole spectrum, some neural channels will not be recovered. Furthermore during the sampling windows (τ) of the left out channels the time division demultiplexing process might be disturbed, which will result in the loss of action potentials of other properly demodulated channels on the receiver side; in a reliable system such a loss is not acceptable. Therefore to design a reliable FA-TDM-FM system, all the high level parameters in equation 2-20 should be co-optimized.

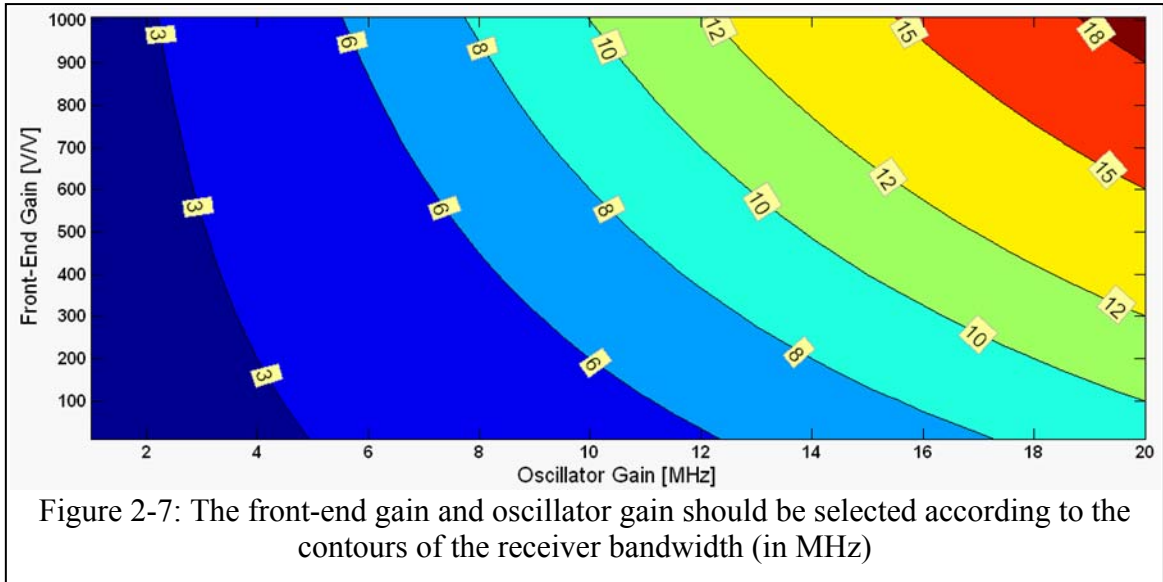


Figure 2-6, depicts the contours of fixed receiver bandwidth (in MHz) for varying crosstalk level and the transmitter's number of channels. For a fixed receiver bandwidth, as more channels are packed in one TDM stream, the inter channel crosstalk level increases. Figure 2-7, demonstrates the relation between the front-end gain and the oscillator gain for a fixed number of channels, crosstalk level, and receiver bandwidth (contours in MHz); according to the equation 2-20, both front-end gain and oscillator gain are determining factors in the required receiver bandwidth. Therefore these two parameters should be selected according to the contours of figure 2-7.

2.3.1.4. VCO's Phase Noise

On the transmitter side the digital noise and the front-end noise are lumped in $n_{FE}(t)$ (equation 2-2); the other source of noise in the transmitter unit is the VCO's induced noise. The finite-Q LC-tank, and the g_m device of the VCO introduce noise into the RF signal path which is referred to as phase noise. The phase noise of the VCO has been studied extensively by few authors [2.17, 2.18, and 2.19]. However in all these

models the impacts of device noise on the spectrum of the VCO's output voltage have been studied. In this analysis the approach introduced in [2.19] is modified to relate the VCO's phase noise to its modulating baseband input.

In a single-transistor Colpitts VCO, it can safely be assumed that the dominant noise source is the *gm*-device of the VCO. The excess phase can be expressed in time domain as [2.19]:

$$\phi_{pn}(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{+\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_c \tau) d\tau \right] \quad (2 - 24)$$

In 2-24, $i(\tau)$ is the noise of the VCO's *gm*-device and the Fourier coefficients (c_i) are from the impulse sensitivity function (ISF) [2.19].

From the Frequency Modulation theory, the instantaneous frequency can be calculated from the phase as:

$$f(t) = \frac{1}{2\pi} \dot{\phi}(t) = f_c + f_{\Delta} x(t) \quad (2 - 25)$$

In 2-25, the $x(t)$ is the VCO's modulating input and the f_{Δ} is the VCO's oscillator gain. Therefore the excess phase calculated in 2-24 can be related back to the modulating input:

$$x_{pn}(t) = \frac{1}{2\pi f_{\Delta}} \dot{\phi}(t) = \frac{I_m c_m \cos(\Delta\omega t)}{4\pi f_{\Delta} q_{max}} \quad (2 - 26)$$

The impacts of noise components around center frequency harmonics can be calculated as:

$$i_{pn,0}(t) = \sqrt{2} \sqrt{\frac{i_n^2}{\Delta f}} \cos(\Delta\omega t) \rightarrow x_{pn,0}(t) = \sqrt{2} \sqrt{\frac{i_n^2}{\Delta f}} \frac{c_0 \cos(\Delta\omega t)}{4\pi f_{\Delta} q_{max}} \quad (DC)$$

$$i_{pn,1\pm}(t) = \sqrt{2} \sqrt{\frac{\overline{i_n^2}}{\Delta f}} \cos((\omega_0 \pm \Delta\omega)t) \rightarrow x_{pn,1\pm}(t) = \sqrt{2} \sqrt{\frac{\overline{i_n^2}}{\Delta f}} \frac{c_1 \cos(\Delta\omega t)}{4\pi f_\Delta q_{max}} \text{ (First)}$$

⋮

$$i_{pn,n\pm}(t) = \sqrt{2} \sqrt{\frac{\overline{i_n^2}}{\Delta f}} \cos((n\omega_0 \pm \Delta\omega)t) \rightarrow x_{pn,n\pm}(t) = \sqrt{2} \sqrt{\frac{\overline{i_n^2}}{\Delta f}} \frac{c_n \cos(\Delta\omega t)}{4\pi f_\Delta q_{max}} \text{ (} n^{th} \text{)} \quad (2 - 27)$$

From 2-27, the noise power spectral density of the phase noise at the modulating input can be expressed as:

$$G_{pn}(f) = \frac{\overline{i_n^2}}{\Delta f} \frac{1}{16\pi^2 f_\Delta^2 q_{max}^2} (c_0^2 + 2c_1^2 + 2c_2^2 \dots) = \frac{\overline{i_n^2}}{\Delta f} \frac{\Gamma_{rms}^2}{4\pi^2 f_\Delta^2 q_{max}^2} \quad (2 - 28)$$

This is an additive noise which together with the time-division-multiplexed signal constitutes the modulating input to the transmitter's noise-less VCO. Also from 2-28, the impacts of VCO's phase noise is alleviated by:

- i) increasing q_{max} ; this can be achieved by increasing the supply voltage or the equivalent capacitance of the LC-tank both of which increase the power consumption, and
- ii) designing an efficient VCO with small Γ_{rms} .

2.3.2. The Receiver

2.3.2.1. The Received Signal

According to the Friis transmission formula, the received signal power can be calculated as [2.20]:

$$P_R = \frac{P_T G_T G_R \lambda^2}{4\pi R^2} = \frac{P_T}{L} = \frac{P_{PA} \times PA_{eff} \times G_T}{L} \quad (2 - 29)$$

In 2-29, R is the distance between the transmitter's and receiver's antennas; G_T and G_R are the transmitter's and receiver's antennas gains which also include the antenna efficiency. P_T is the RF power radiated from the transmitter's antenna which can be expressed as the power amplifier (PA) total power, PA's efficiency, and the transmitter antenna gain ($P_{PA} \times PA_{eff} \times G_T$). L is the free path space loss derived from the Friis transmission formula.

On the receiver side the received signal power can be related to the received signal amplitude as:

$$P_R = \frac{P_T}{L} = \frac{A_R^2}{2 \times R_{ANT,RX}} \rightarrow A_R = \sqrt{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L}} \times R_{ANT,RX} \quad (2 - 30)$$

In above equation, A_R is the received signal amplitude, and $R_{ANT,RX}$ is the impedance of the receiver antenna (50Ω).

From the received signal amplitude in 2-30, the received signal is:

$$x_R(t) = A_R \cos(\omega_c t + \phi(t)) \quad (2 - 31)$$

The total signal entering the demodulator is assumed to be the superposition of the received signal and the Additive White Gaussian Noise (AWGN):

$$v_R(t) = x_R(t) + n_{awgn}(t) = A_R \cos(\omega_c t + \phi(t)) + n_{awgn}(t) \quad (2 - 32)$$

In above formula, the RF interference has been ignored as it can be eliminated by the Faraday cage or shifting the VCO's center frequency to the quiet zone.

2.3.2.2. Signal Conditioning: *BPF+Limiter*

The received amplified signal enters the band pass filter. The assumption here is that the transmitter emitted signal passes without distortion through the band pass filter

and AWGN noise is shaped by the band pass filter to form the band passed noise. The impacts of receiver limited bandwidth on the demodulated signal are already discussed in the bandwidth estimation of TDM modulated FM signals in section 2.3.1.3.

$$v_{BPF}(t) = x_R(t) + n_{awgn,BPF}(t) = A_R \cos(\omega_c t + \phi(t)) + A_n(t) \cos(\omega_c t + \phi_n(t)) \quad (2 - 33)$$

The band passed noise results in a signal with time varying amplitude which also disturbs the received signal phase. Therefore the $v_{BPF}(t)$ can be written as:

$$v_{BPF}(t) = A_v(t) \cos(\omega_c t + \phi_v(t)) \quad (2 - 34)$$

After the band pass filter, there is a limiter block which eliminates the amplitude variation; furthermore in FM signals, the noise induced phase variation affects the SNR. The output of the limiter is:

$$v_{Limiter}(t) = A_R \cos(\omega_c t + \phi_v(t)) \quad (2 - 35)$$

The band pass noise in 2-33, can be written in terms of its quadrature baseband components as [2.16]:

$$n(t) \cong n_i(t) \cos(\omega_c t) - n_q(t) \sin(\omega_c t) \quad (2 - 36)$$

From 2-33 and 2-35, the total phase can be written as:

$$\phi_v(t) \cong \phi(t) + \psi(t) \quad (2 - 37)$$

In above equation $\psi(t)$ is the phase of the band passed white noise which can be calculated as:

$$\psi(t) = \frac{A_n \sin(\phi_n(t))}{A_R} = \frac{n_q(t)}{\sqrt{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}}} \quad (2 - 38)$$

Therefore it can be concluded that the phase from band passed white noise linearly disturbed the received signal phase, and increasing the transmitted power or

reducing the transmission distance reduces the disturbing phase from the band passed (colored) white noise.

The quadrature baseband components of band passed white noise have a power spectral density described by [2.16]:

$$G_{n_i}(f) = G_{n_q}(f) = N_{0,awgn} \Pi\left(\frac{f}{BW_{FM}}\right) \quad (2 - 39)$$

In above equation, $N_{0,awgn}$ is the power spectral density of the AWGN and BW_{FM} is the required bandwidth to demodulate the TDM-FM signal as calculated in 2-20.

2.3.2.3. FM Detection

To calculate the SNR of the demodulated-demultiplexed neural channel, the band passed white noise should be expressed in time domain. The FM demodulated band passed white noise is:

$$\xi(t) = \frac{1}{2\pi} \psi \dot{(t)} = \frac{n_q \dot{(t)}}{2\pi \sqrt{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}}} \quad (2 - 40)$$

The power spectral density of $n_q \dot{(t)}$ can be calculated as:

$$\begin{aligned} G_{\xi}(f) &= (2\pi f)^2 \frac{G_{n_q}(f)}{4\pi^2 \times \frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} \\ &= \frac{f^2 N_{0,awgn}}{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} \Pi\left(\frac{f}{BW_{FM}}\right) \end{aligned} \quad (2 - 41)$$

From the 2-25 and 2-35, the output of the FM detector is calculated:

$$v_{FM}(t) = \frac{1}{2\pi} \phi_v(t) = \frac{1}{2\pi} \dot{\phi}(t) + \xi(t) = f_{\Delta} x_M(t) + \xi(t) \quad (2 - 42)$$

The FM detector is followed by a low pass filter which filters out the noise and passes the TDM signal; the optimum bandwidth of this block is equal to TDM bandwidth calculated in equation 2-14. The output of the LPF is:

$$v_{FM_LPF}(t) = f_{\Delta}x_M(t) + \xi_{LPF}(t) \quad (2 - 43)$$

In above equation $x_M(t)$ is the modulating input of the transmitter's VCO introduced in 2-17; $\xi_{LPF}(t)$ is the low pass filtered $\xi(t)$ in 2-42. The $\xi_{LPF}(t)$ has a transfer function similar to that of $\xi(t)$ but limited in frequency to BW_{TDM} as opposed to BW_{FM} . The noise reduction advantage of the low pass filter block following the FM detector block is more pronounced in systems with large transmitter's oscillator gain (f_{Δ}). The power spectral density of $\xi_{LPF}(t)$ is calculated as:

$$G_{\xi_{LPF}}(f) = \frac{f^2 N_{0,awgn}}{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} \Pi\left(\frac{f}{2 \times BW_{TDM}}\right) \quad (2 - 44)$$

2.3.2.4. Time Division Demultiplexing

The TDM demultiplexer and the subsequent low pass filter blocks in figure 2-3, recover the neural channels. The demultiplexed, low pass filtered $\xi_{LPF}(t)$ forms the noise component on the neural channel: $\xi_{LP,DM,LP}(t)$. This is the result of AWGN passing through all the receiver blocks. $\xi_{LP,DM,LP}(t)$ has a power spectral density described by:

$$G_{\xi_{LP,DM,LP}}(f) = \frac{BW_{TDM}^2 N_{0,awgn}}{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} \Pi\left(\frac{f}{2 \times BW_{ch}}\right) \quad (2 - 45)$$

The advantage of the last low pass filter block (figure 2-3), manifest itself in limiting the $G_{\xi_{LP,DM,LP}}(f)$ in frequency domain to $2 \times BW_{ch}$. Without this block,

$G_{\xi_{LP,DM,LP}}(f)$ has a bandwidth of $2 \times BW_{TDM}$ which is substantially larger than the neural channel bandwidth as calculated in 2-14.

The recovered neural channel can be written in time domain as:

$$ch_i(t) = f_{\Delta}x_i(t) + f_{\Delta}pn(t) + \xi_{LP,DM,LP}(t) \quad (2 - 46)$$

Substituting for $x_i(t)$ (equation 2-2) and ignoring the front-end output offset:

$$ch_i(t) = f_{\Delta}FE_{gain}v_{neural,i}(t) + f_{\Delta}FE_{gain}n_{FE}(t) + f_{\Delta}pn(t) + \xi_{LP,DM,LP}(t) \quad (2 - 47)$$

The right hand side of 2-47, contains the neural channel signal and various noise components: the first term is the neural signal, the second term is from the mixed-signal noise of the transmitter, the third term is contributed by the transmitter VCO's phase noise, and the last term is the result of additive white Gaussian noise (AWGN) passing through all the receiver blocks.

2.3.2.5. SNR of the Recovered Neural Channel

To calculate the SNR of the recovered neural channel, one should note that the purpose of the system is to capture an action potential. Therefore the SNR should be calculated in time domain during the window when an action potential is present; if the window of calculation is increased to include more than one action potential, the firing rate of the neuronal populations also play a role in the calculated SNR, which is irrelevant from the circuit design point of view.

From 2-47, the average power of the recovered neural signal is calculated in time domain as:

$$S_x = f_{\Delta}^2 \times FE_{gain}^2 \times \langle v_{neural,i}^2(t) \rangle \quad (2 - 48)$$

The average power of the transmitter's mixed signal noise in time domain:

$$N_{FE} = f_{\Delta}^2 \times FE_{gain}^2 \times \langle n_{FE}^2(t) \rangle \quad (2-49)$$

The average power of the transmitter's VCO circuit noise in time domain:

$$N_{PN} = f_{\Delta}^2 \times \langle pn^2(t) \rangle \quad (2-50)$$

The average power of the additive white Gaussian noise (AWGN) in time domain:

$$N_{awgn} = \langle \xi_{LP,DM,LP}^2(t) \rangle \quad (2-51)$$

The SNR of the recovered neural channel can be calculated in time domain from 2-47:

$$(S/N)_{chi} = \frac{S_x}{N_{FE} + N_{PN} + N_{awgn}} \quad (2-52)$$

By substituting 2-48 through 2-51 into 2-52, the SNR of the recovered neural channel at the receiver is calculated as:

$$(S/N)_{chi} = \frac{f_{\Delta}^2 \times FE_{gain}^2 \times \langle v_{neural,i}^2(t) \rangle}{f_{\Delta}^2 \times FE_{gain}^2 \times \langle n_{FE}^2(t) \rangle + f_{\Delta}^2 \times \langle pn^2(t) \rangle + \langle \xi_{LP,DM,LP}^2(t) \rangle} \quad (2-53)$$

The average power of the various noise sources in 2-53 can be calculated in time domain:

$$\begin{aligned} \langle n_{FE}^2(t) \rangle &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{+T/2} n_{FE}^2(t) dt = R_{n_{FE}}(0) = \int_{-\infty}^{+\infty} G_{n_{FE}}(f) df \\ &= \int_{-BW_{ch}}^{+BW_{ch}} \frac{N_{0,FE}}{2} df = N_{0,FE} \times BW_{ch} \end{aligned} \quad (2-54)$$

$$\begin{aligned} \langle pn^2(t) \rangle &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{+T/2} pn^2(t) dt = R_{pn}(0) = \int_{-\infty}^{+\infty} G_{pn}(f) df \\ &= \int_{-BW_{ch}}^{+BW_{ch}} \frac{\overline{i_n^2}}{\Delta f} \frac{\Gamma_{rms}^2}{4\pi^2 f_{\Delta}^2 q_{max}^2} df = \frac{\overline{i_n^2}}{\Delta f} \frac{\Gamma_{rms}^2}{2\pi^2 f_{\Delta}^2 q_{max}^2} \times BW_{ch} \end{aligned} \quad (2-55)$$

$$\begin{aligned}
\langle \xi_{LP,DM,LP}^2(t) \rangle &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} \xi_{LP,DM,LP}^2(t) dt = R_{\xi_{LP,DM,LP}}(0) = \int_{-\infty}^{+\infty} G_{\xi_{LP,DM,LP}}(f) df \\
&= \int_{-BW_{ch}}^{+BW_{ch}} \frac{BW_{TDM}^2 N_{0,awgn}}{\frac{2 \times P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} df \\
&= \frac{BW_{TDM}^2 N_{0,awgn}}{\frac{P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} \times BW_{ch} \tag{2-56}
\end{aligned}$$

The average power of the neural signal can be calculated in time domain as:

$$\langle v_{neural,i}^2(t) \rangle = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{+T/2} v_{neural,i}^2(t) dt \approx \frac{1}{T_{AP}} \int_0^{T_{AP}} v_{neural,i}^2(t) dt \tag{2-57}$$

As explained earlier the integral limit of 2-57 should be limited to the time window when a single action potential is present (T_{AP}).

Substituting 2-54 through 2-57 into 2-53, the SNR of the recovered neural channel can be expressed as:

$$(S/N)_{ch_i} = \frac{f_{\Delta}^2 \times FE_{gain}^2 \times \langle v_{neural,i}^2(t) \rangle}{f_{\Delta}^2 \times FE_{gain}^2 \times N_{0,FE} \times BW_{ch} + \frac{\overline{i_n^2}}{\Delta f} \frac{\Gamma_{rms}^2}{2\pi^2 q_{max}^2} \times BW_{ch} + \frac{BW_{TDM}^2 N_{0,awgn}}{\frac{P_{PA} \times PA_{eff} \times G_T}{L} \times R_{ANT,RX}} \times BW_{ch}} \tag{2-58}$$

Where:

f_{Δ} : Transmitter VCO's oscillator gain

FE_{gain} : Transmitter front-end's gain

$N_{0,FE}$: Transmitter's input referred mixed signal noise spectral density

BW_{ch} : Neural channel bandwidth (fixed at 10KHz for neural channel)

$\frac{\overline{i_n^2}}{\Delta f}$: Spectral density of the transmitter VCO's current noise

Γ_{rms} : The RMS of the transmitter VCO's ISF

q_{max} : Maximum charge displacement of the transmitter LC-tank equivalent capacitance.

BW_{TDM} : The transmitter TDM bandwidth (equation 2-14)

$N_{0,\text{awgn}}$: The power spectral density of the AWGN

$P_{\text{PA}} \times PA_{\text{eff}} \times G_{\text{T}}$: The transmitted power

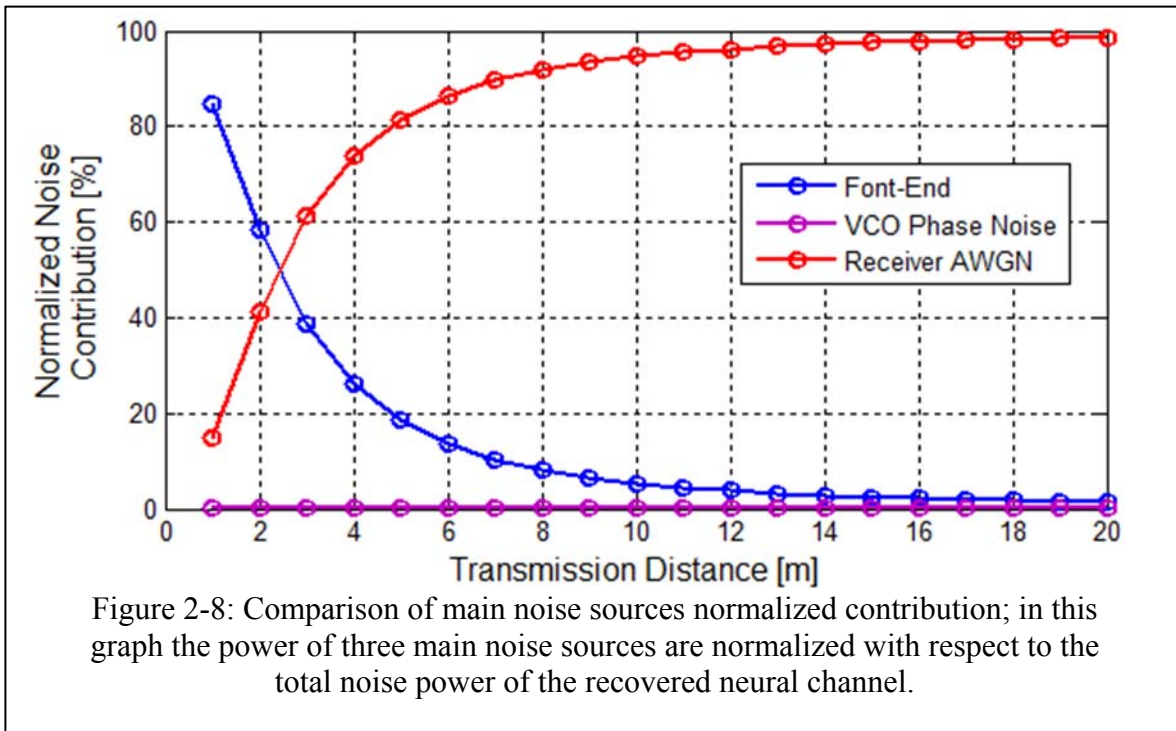
L : The free space path loss (equation 2-29)

$R_{\text{ANT,RX}}$: The receiver antenna impedance (50 Ω)

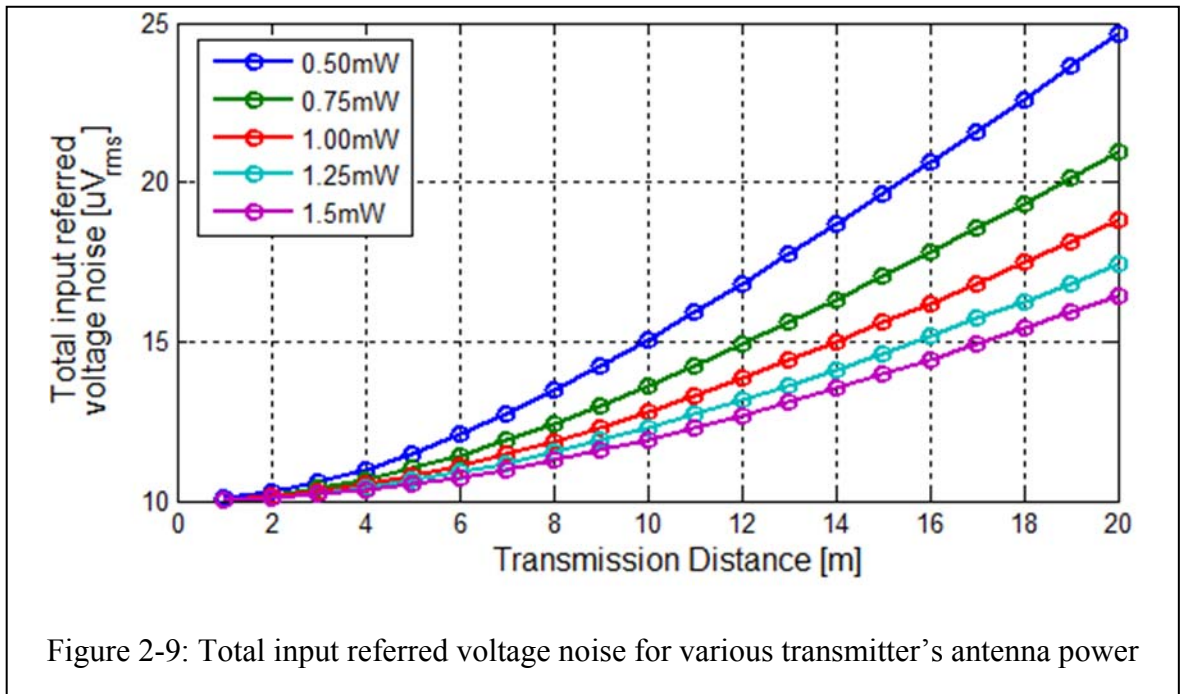
Equation 2-58, calculates the recovered neural channel SNR using all the high level system parameters and provides the designer with an insight to co-optimize the inter-related parameters of fully analog TDM-FM (FA-TDM-FM) systems. It should be noted that equation 2-58 calculates the SNR of a generic FA-TDM-FM system and does not include the parameters specific to neural recording devices, e.g. electrode noise and electrode impedance. The optimum electrode's parameters cannot be addressed at the architectural level; instead the front-end should be designed specifically for the target electrode.

2.3.3. Results and Discussions

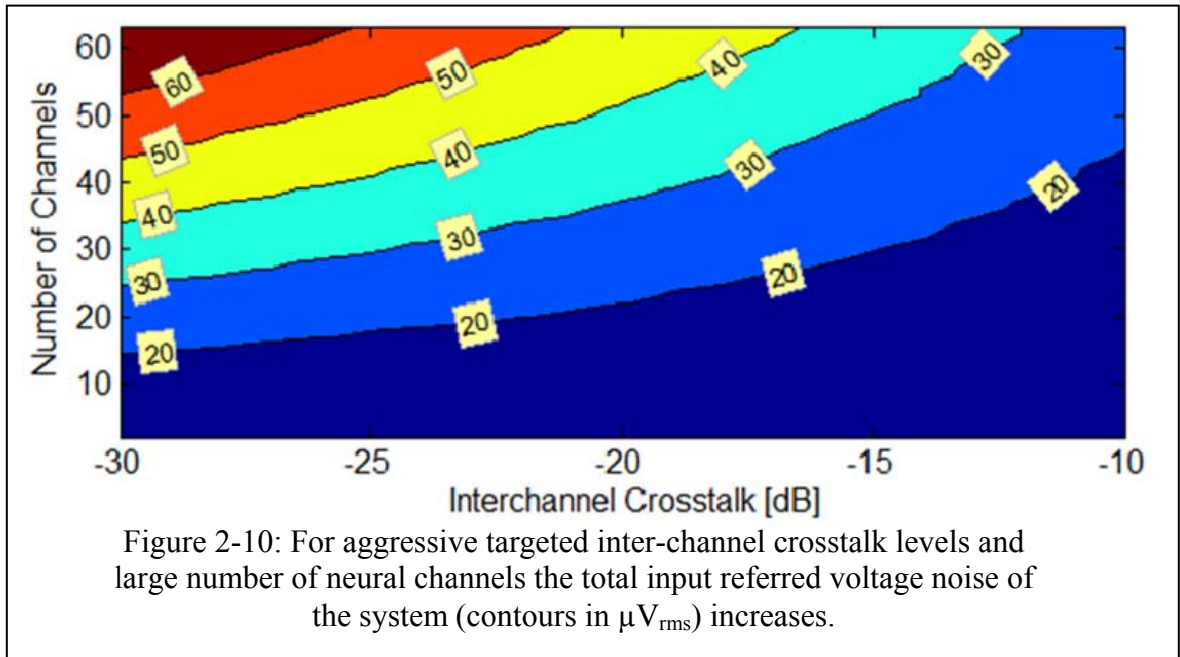
Several conclusions can be drawn from SNR of recovered neural channel calculated in equation 2-58 which serve as a guideline in designing a robust and reliable FA-TDM-FM system. As reflected in the nominator of equation 2-58, by increasing the oscillator gain (f_{Δ}) or front-end gain (FE_{gain}), the input signal's average power increases; but so does the contribution of the transmitter's mixed signal noise ($f_{\Delta}^2 \times FE_{gain}^2 \times N_{0,FE} \times BW_{ch}$). By increasing oscillator gain (f_{Δ}) and front-end gain (FE_{gain}), the bandwidth is traded for the signal quality as the first term in the denominator of equation 2-58 dominates others. However arbitrarily increasing these factors results in an increase of the TDM signal bandwidth (BW_{TDM}) which give rise to the contribution of the additive white Gaussian noise (last term of the denominator in 2-58). Based on the estimated (or measured) contributions of these noise sources the oscillator gain (f_{Δ}) and front-end gain



(FE_{gain}), should be selected accordingly. In figure 2-8 the normalized contribution of main noise sources are compared versus the transmission distance. For transmission distances over 2m, the receiver AWGN dominates other noise sources and as can be observed the phase noise contribution is negligible (<1%). The VCO's phase noise contribution to the recovered neural channel total noise is an order of magnitude smaller than that of other noise sources. The contribution of VCO's phase noise is minimized by increasing the VCO charge swing (q_{max}), and minimizing the RMS of VCO's impulse sensitivity function (Γ_{rms}). Increasing the VCO charge swing (q_{max}), is achieved by



increasing power consumption of the transmitter's RF blocks; and minimizing the RMS of VCO's impulse sensitivity function (Γ_{rms}) is achieved by efficient VCO design. Therefore in designing the VCO of FA-TDM-FM systems the focus should be on reducing the VCO's power consumption rather than achieving competitive phase noise.



Increasing the transmitted RF power ($P_{PA} \times PA_{eff} \times G_T$) reduces the contribution of the additive white Gaussian noise (AWGN) as shown by the last term of the denominator in equation 2-58; increasing the transmitted RF power can be achieved by: 1) designing efficient power amplifiers (large PA_{eff}), 2) increasing the PA power consumption (P_{PA}), and 3) employing efficient transmitter antennas (G_T close to unity); however employing an efficient antenna results in an increase in the transmitter size/weight assuming a fixed back telemetry transmission frequency. Figure 2-9, shows the input referred voltage noise versus transmission distance for various emitted transmitter's antenna power.

Another less obvious conclusion from equation 2-58 is the impact of desired crosstalk level and number of channels on the recovered neural channel SNR shown in figure 2-10. This is due to the required large receiver bandwidth for aggressive crosstalk levels and large number of channels which accentuates the impacts of additive white Gaussian noise.

2.4. Conclusion

The employed high level architecture of the developed wireless biotelemetry systems (FA-TDM-FM) is introduced. The physical and electrical specifications of the biotelemetry systems intended for reliable wireless neural recording from small animal subjects are discussed in details. The concept of reliability is explained along with the implemented design strategies to achieve a reliable system. The introduced reliability criteria is quantified mathematically and implemented in an analytical tool so called Signal Path Co-Optimization (SPCO) providing the designer with the insight to choose various block-level parameters given a limited power and bandwidth budget.

2.5. References for Chapter 2

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CHAPTER 3

THE PRELIMINARY MICROSYSTEMS: TEST VEHICLES

Two generations of fully analog, TDM-FM (FA-TDM-FM) systems were developed and applied in wireless neural recoding experiments from small animal models. Through field testing of these systems, the obstacles encountered in reliable multichannel wireless neural recording are identified. These systems served as the basis for derivation and quantification of the reliability concept explained in chapter 2.

3.1 The Discrete 15-Ch Neural Transmitter: *FMT_V1*

3.1.1. *FMT_V1*'s Block Diagram

The high-level architecture of the 15-Ch transmitter prototype is displayed in figure 3-1 [3.1]. The transmitter is comprised of two 62mil, custom-designed PCBs

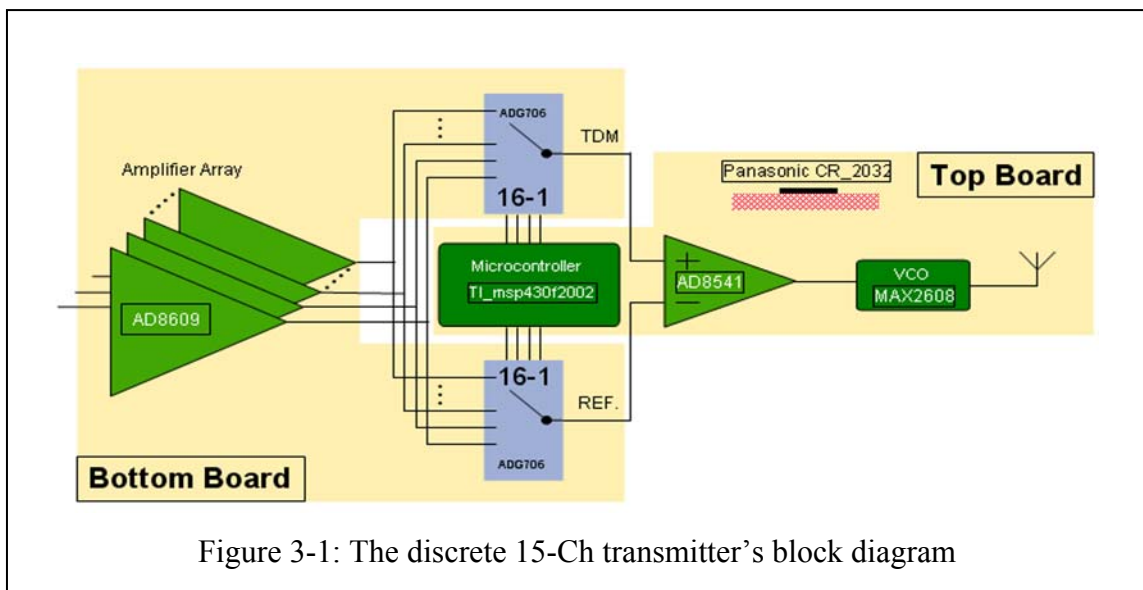


Figure 3-1: The discrete 15-Ch transmitter's block diagram

stacked vertically; the bottom board contains the sensitive analog front-end circuitry which includes the neural amplifiers and TDM multiplexers. The top board houses the microcontroller and RF transmitter. The potential difference between electrode-ECF (Extracellular Fluid) in equilibrium can be as large as $\pm 1V_{DC}$ which is imposed on the input node of neural amplifier leading to amplifiers saturation. Due to size constraints of the system and large number of channels, the non-Faradaic capacitance of the electrodes is used to cancel the DC offset which is similar to the approach taken in [3.2]; a 22M Ω resistor (SMD 0603) is added in parallel with the amplifier input which forms a high pass filter with the non-Faradaic capacitance of the electrode and at the same time forms a resistive divider with the Faradaic resistor of the electrode. This method of DC rejection has the advantage of being more compact, especially in discrete COTS-based systems. In-vivo experiments with this discrete device revealed the inadequacy of its DC cancellation approach for large number of channels due to inter-channel offsets. The validity of this architecture was verified first through the high-level Simulink model and emulated system; finally the low level verification was implemented in hspice in which all the estimated parasitics were modeled. The final assembled 15-Ch device is shown in figure 3-2; this is a lightweight (10.8g including the batteries, 6.7g no batteries), low power (3.7mA from a 3V battery, operates up to 24hrs from a Panasonic CR_2032), small size (30 \times 30 \times 8mm³), multichannel (up to 15-Ch) wireless biotelemetry transmitter. FMT_V1 has a transmission distance of 6m, and a crosstalk level of 2%.

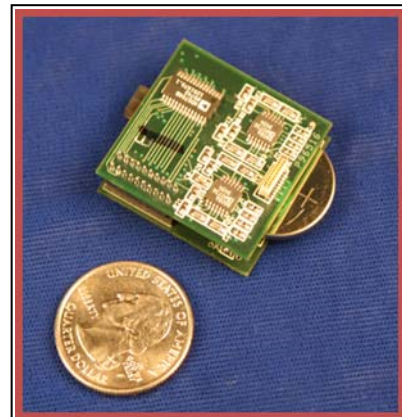


Figure 3-2: The discrete 15-Ch neural transmitter

3.1.2. Biological Test Results

In-vivo experiments were conducted on three different animal subjects: guinea pig, zebra finch and marmoset monkey. Guinea pigs were implanted with chronic 16-Ch

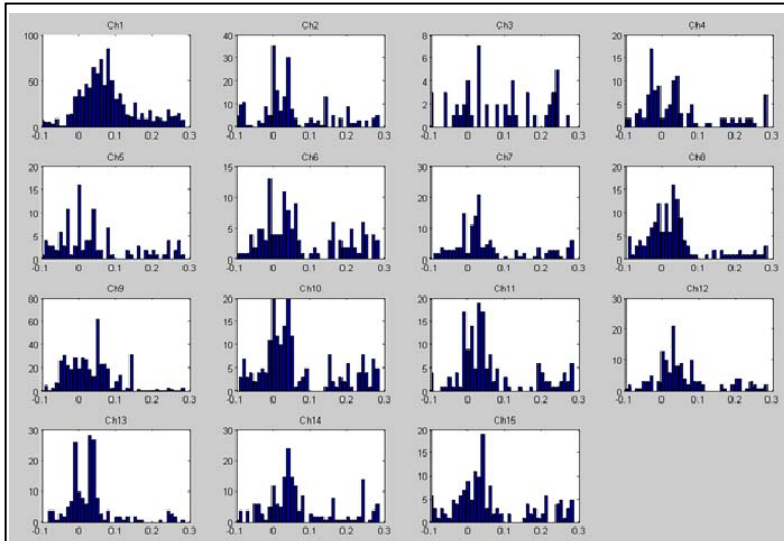


Figure 3-3: Histograms of neural channels from the guinea pig using the discrete 15-ch transmitter; Y axis is the number of spikes. X axis is time (in seconds) relative to audio stimulation.

wire bundle electrodes in their HVC nucleus. During the experiment the animal was awake, restrained and presented with audio stimulus. To have a point of reference for wirelessly received action potentials, tethered recording was conducted

prior to wireless recording; as it turned out the chronic implant on the tested animal did not have any good sites with high SNR but the spikes were present. To distinguish between noise and neural spikes, a basic neuroscience algorithm was adopted in the back-end software tool. In this algorithm, the subject is presented with a periodic audio stimulation while the neural spikes are being recorded. The HVC and RA neurons fire rate should increase with onset of stimulation. The recorded channels are divided into 5ms bins. For each bins the number of spikes are counted. The spikes are being recognized by their waveform characteristics. To justify the reliability of this recognition, the histogram of number of spikes versus the time of audio stimulation is calculated as illustrated in figure 3-3; in this figure, time 0 is the stimulation time. For a total duration

of 0.4 Seconds around the stimulation time, neural spikes are extracted and binned in time. As can be seen, in almost all the channels the firing rate of neurons increase around stimulation time which shows the counted spikes were in fact action potentials not noise.

The zebra finch (ZF) in the in-vivo experiment was implanted with wire bundle electrodes in their RA and HVC nucleus (both RA and HVC are part of auditory cortex). Due to small size of ZF's motor cortexes, only 2 working electrodes (WE) were implanted which among them only one sensed good action potentials. Also on top of ZF's head manual microdrivers are installed which can be used to change the position of individual

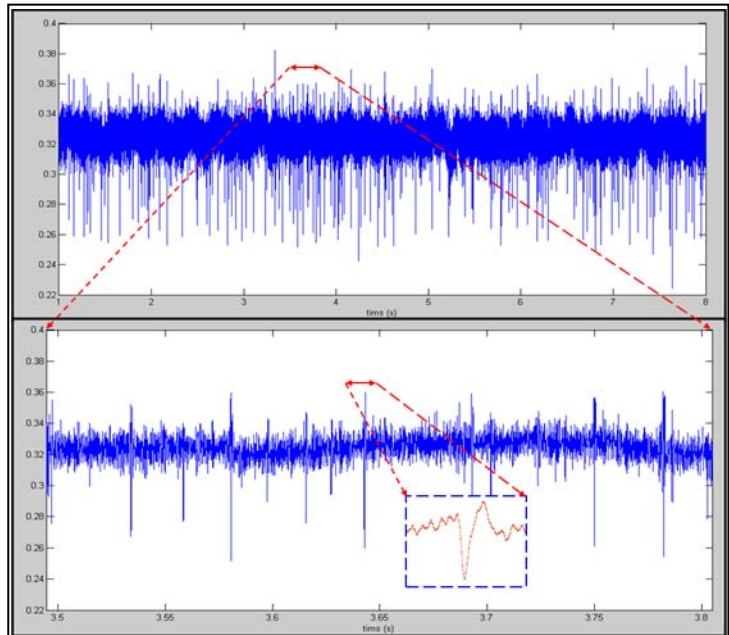


Figure 3-4: Recording wirelessly from RA nucleus of zebra finch using the discrete 15-ch transmitter

wire electrodes by a few of micrometers. The 15-Ch discrete prototype device was programmed to send out only 2 channels; among those, one had good action potentials comparable to tethered recording. Figure 3-4, is an example of neural activities recorded wirelessly with *FMT_VI* from RA nucleus of an anesthetized zebra finch.

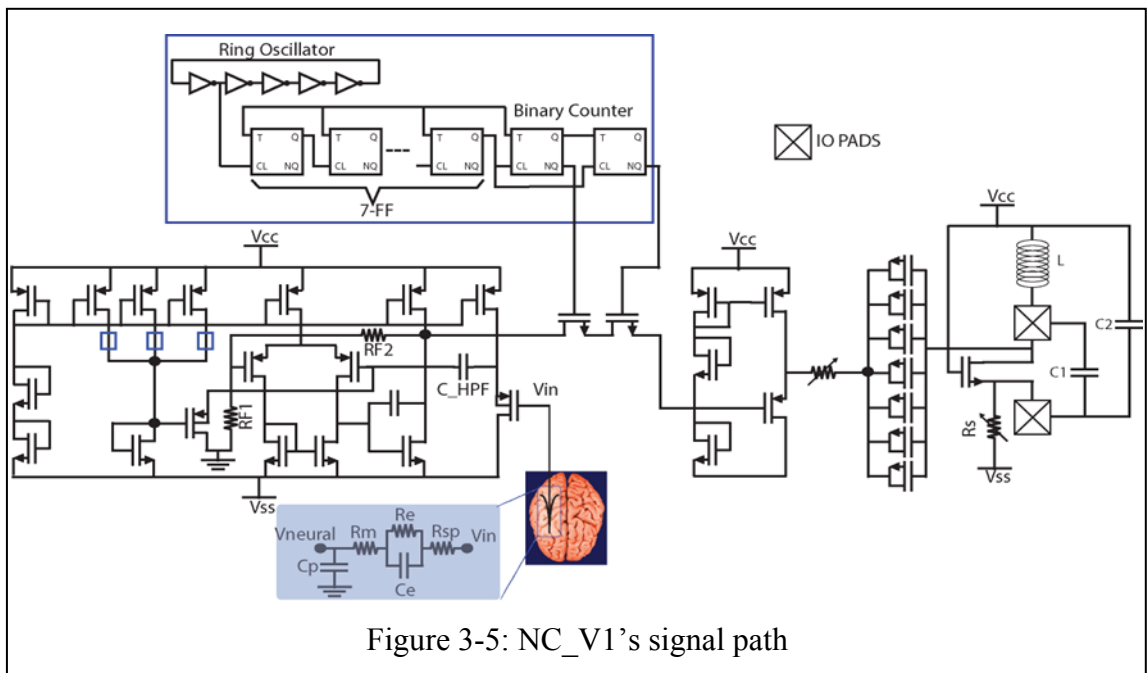
The marmoset monkey was implanted with wire bundle electrode as well; as a result of the discrete 15-Ch transmitter's DC cancellation method, large inter-electrode offsets and consequently large inter-channel offsets among channels were observed; as

explained in chapter 2, such large inter-channel offsets saturate the wireless link, making all the neural channels irrecoverable.

3.2 The Integrated 3-Ch Microsystem: NC_V1

3.2.1. NC_V1's Block Diagram

Figure 3-5 [3.3], shows the transmitter's signal path which can be divided into three categories: *i*) front-end circuitry (neural amplifiers) *ii*) sampling circuitry (digital



controller + TDM Multiplexer + buffer), and *iii*) RF modulator (VCO). The ASIC is fabricated in a 1.5 μ m 2P2M standard CMOS process. The preamplifier consists of a two-stage lead-compensated OTA with resistive feedback preceded by a high pass filter; front-end gain is set at 40dB. The HPF is composed of a PMOS source-follower driving an on-chip RC HPF; the capacitor of the HPF is a double-poly linear capacitor and its resistor is implemented with a subthreshold PMOS transistor. High pass cut-off

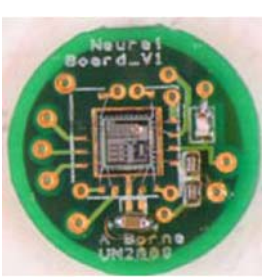


Figure 3-6: The assembled NC_V1, Weight < 1g, Volume < 1cm³

frequencies is laser trimmable from 10Hz to 200Hz. Using this method of DC rejection the channel's SNR was constant over a 1V_{DC} range of input offset (-500mV_{DC} to 500mV_{DC}). Even though this method rejects the Electrode-ECF offset potential successfully it created two additional problems: *i*) light sensitivity: the drain current of subthreshold PMOS pseudo resistor is light sensitive; this current flows into the high impedance node of the neural amplifier's input, which results in an light-dependent output offset in the front-end, *ii*) increased input referred noise of the front-end. NC_V1 can be configured to use one of two RF transmitters: *i*) an on-chip single-transistor Colpitts VCO with a center frequency of 440MHz, and *ii*) a COTS RF modulator, MAX2608, which consumes 2.7mA from 3V supply at 440MHz. The on-chip VCO was tested successfully, but for in-vivo experiments MAX2608 was used due to its superior range and stability. The assembled microsystem is displayed in figure 3-6.

3.2.2. Biological Test Results

Two test subjects were used for in-vivo experiments: cockroach and Long Evans rat; in recording from Long Evans rat (figure 3-7) electrodes were inserted in the forelimb area of the motor cortex (coordinates AP: 2.5 mm, ML: 2.5 mm from bregma). Anesthesia was maintained through intraperitoneal injections of a mixture of 50mg/ml ketamine, 5mg/ml xylazine, and 1mg/ml acepromazine at an injection volume of 0.125ml/100g body weight.

The connector used on the rat was FE-18 Omnetics connector [3.4]; to interface the FE-18 with the 3-channel neural board a custom made 3-channel connector was built which limits the functionality of the system to record from three adjacent sites at every recording. Figure 3-8 depicts the recordings; before the wireless recording experiment, all the 16-channels were

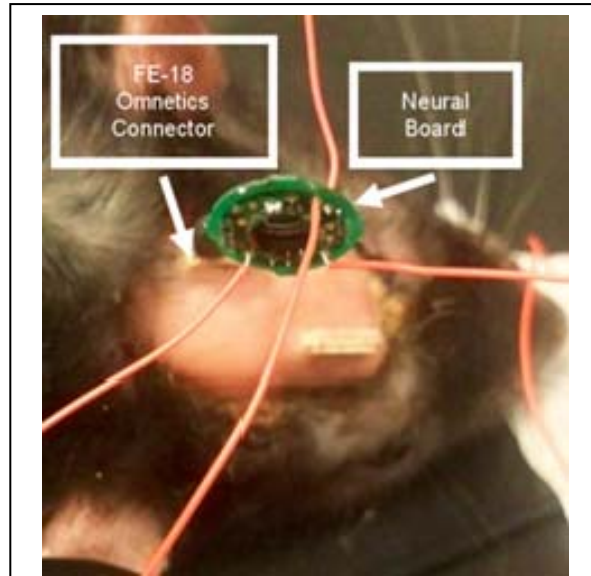


Figure 3-7: Recording from motor cortex of Long Evans rat using NC_V1

monitored through tethered setup and the wired recording waveforms were used as a reference. The wired recording results were in good agreement with wireless recording results in a sense that wired channels with good SNR maintained their high quality in wireless recording as well. The second in-vivo experiment was on an amputated cockroach leg. Cockroach leg contains sensory receptors and provides a stable platform

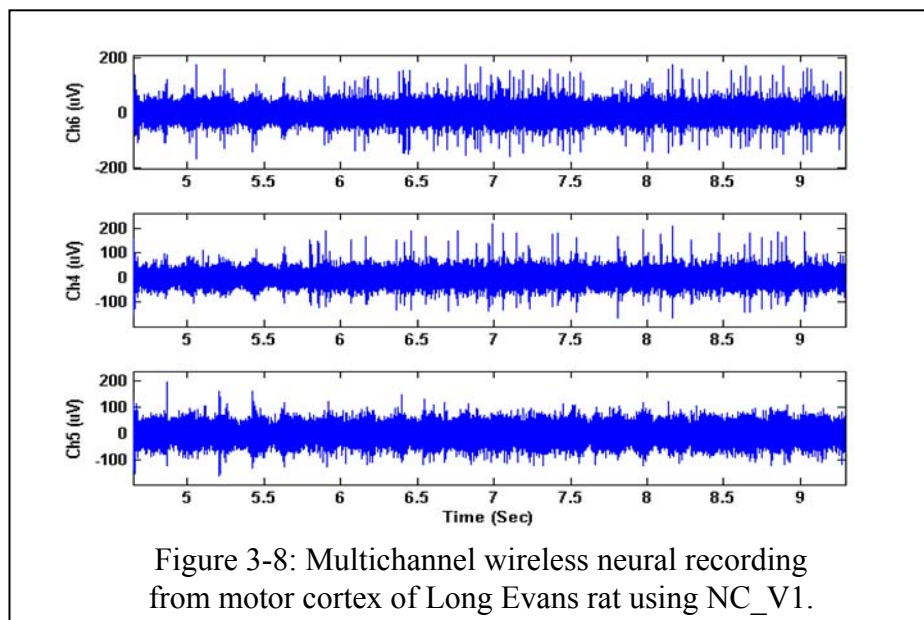
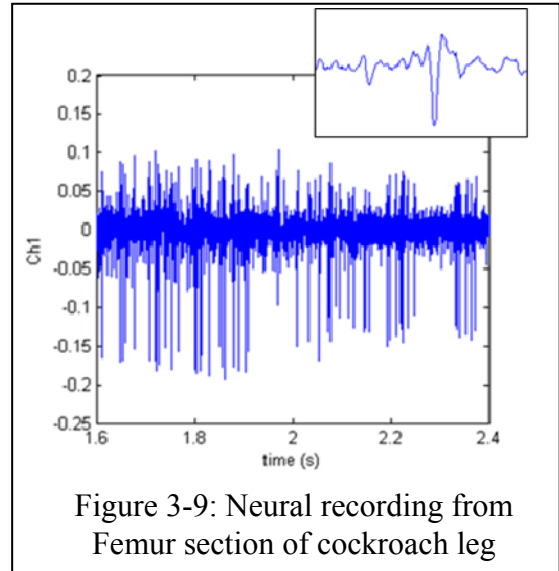


Figure 3-8: Multichannel wireless neural recording from motor cortex of Long Evans rat using NC_V1.

to record neural activity from, for the purpose of initial prototyping of a design [3.5]. In this test stainless steel pins were used as electrodes with the reference electrode (RE) inserted in Coxa and the working electrode (WE) put in Femur. The recorded action potentials are depicted in figure 3-9; the x-axis is the time in seconds



and the y-axis is the input-referred neural signal amplitude in mV. Several problems were observed when employing NC_V1 in in-vivo neural recordings: 1) over time large inter-channel offset was observed among the NC_V1 neural channels; and the front-end offset eventually saturated the wireless link, 2) the on-chip Colpitts VCO of NC_V1 was coupled to the off-chip monopole wire antenna directly; as mentioned before this strategy results in termination of neural data back telemetry and limited transmission range, 3) small VCO's oscillator gain, and 4) noisy front-end due to the buffer stage.

3.3. Conclusion

Two generations of fully analog, TDM-FM (FA-TDM-FM) wireless biotelemetry systems developed in early course of this project were presented: *i*) FMT_V1 (discrete 15-Ch), and *ii*) NC_V1 (ASIC, single-chip). These devices were used in wireless neural recordings from various animal subjects. Employing these preliminary systems the obstacles encountered in reliable multichannel wireless neural recording were identified, which provided the knowledge needed to quantify the reliability concept.

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CHAPTER 4

THE NEURAL TRANSMITTER: *CIRCUIT ANALYSIS*

In this chapter the design, implementation and characterization of the individual blocks employed in the proposed multichannel wireless neural recording microsystem are discussed. The conflicting criteria of reliability and low power are addressed in the proposed multichannel wireless neural recording microsystem: *NC_V3*. This microsystem is optimized at the system level through the analytical tool SPCO (chapter 2), to enhance the performance metrics pertaining to robustness and reliability while meeting a limited power and bandwidth budget. All the blocks presented in this chapter are fabricated in a 0.5 μm 2P3M n-well standard CMOS process.

4.1. The Transmitter's ASIC Architecture

The *NC_V3*'s ASIC and architecture are demonstrated in figures 4-1 and 4-2 respectively; the 2.85 \times 3.84mm² ASIC is fabricated in a 0.5 μm 2P2M n-well CMOS process. The architecture follows that of a FA-TDM-FM system. In *NC_V3*, 8-channels are dedicated to neural signals and one channel is dedicated to audio signals. The advantage of the audio channel is in applications where the auditory cortex of the test subject is under study, and the audio stimulation perceived and produced by the subject is of importance [4.1]. In other applications this auxiliary channel can be replaced with other signals, e.g. accelerometer [4.2], as needed.

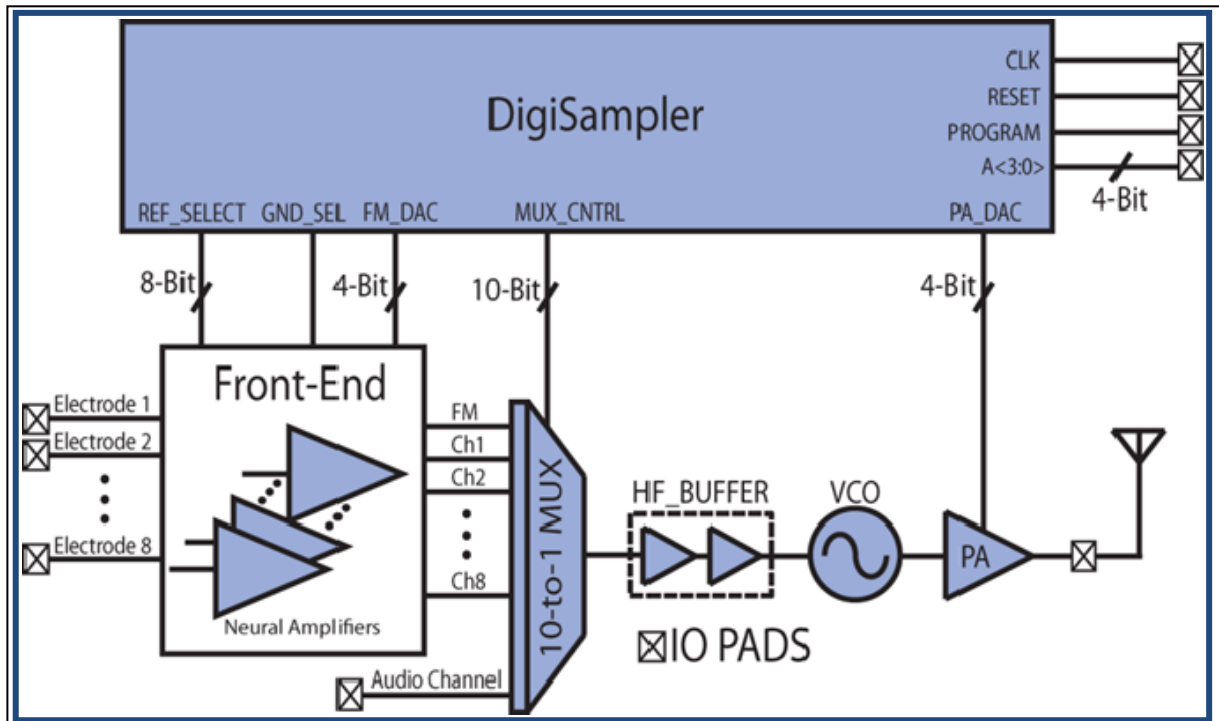


Figure 4-1: The FA-TDM-FM architecture of the proposed multichannel wireless neural transmitter (*NC_V3*)

The front-end consists of: *i*) a bank of eight neural amplifiers, *ii*) the reference channel circuitry, and *iii*) frame marker generator. The front-end amplifies the extracellular action potentials and generates the frame marker. The front-end's signal path is user-adjustable through 9-bits; the frame marker voltage level is also user-adjustable through 4-bits. Having a flexible signal path helps in removing the common mode noise sources, e.g. 60Hz. A user-adjustable frame marker is useful for trading off the recovered neural channel SNR and the demultiplexing procedure robustness at the receiver as explained by equation 2-58. The audio signal is provided by the low power COTS microphones (SPM0408HE5H) [4.3].

The 10 channels of continuous data (frame marker, 8-neural, 1-audio) are multiplexed in one continuous time division multiplexed (TDM) stream using the analog multiplexer. The analog multiplexer is controlled by the digital block so called

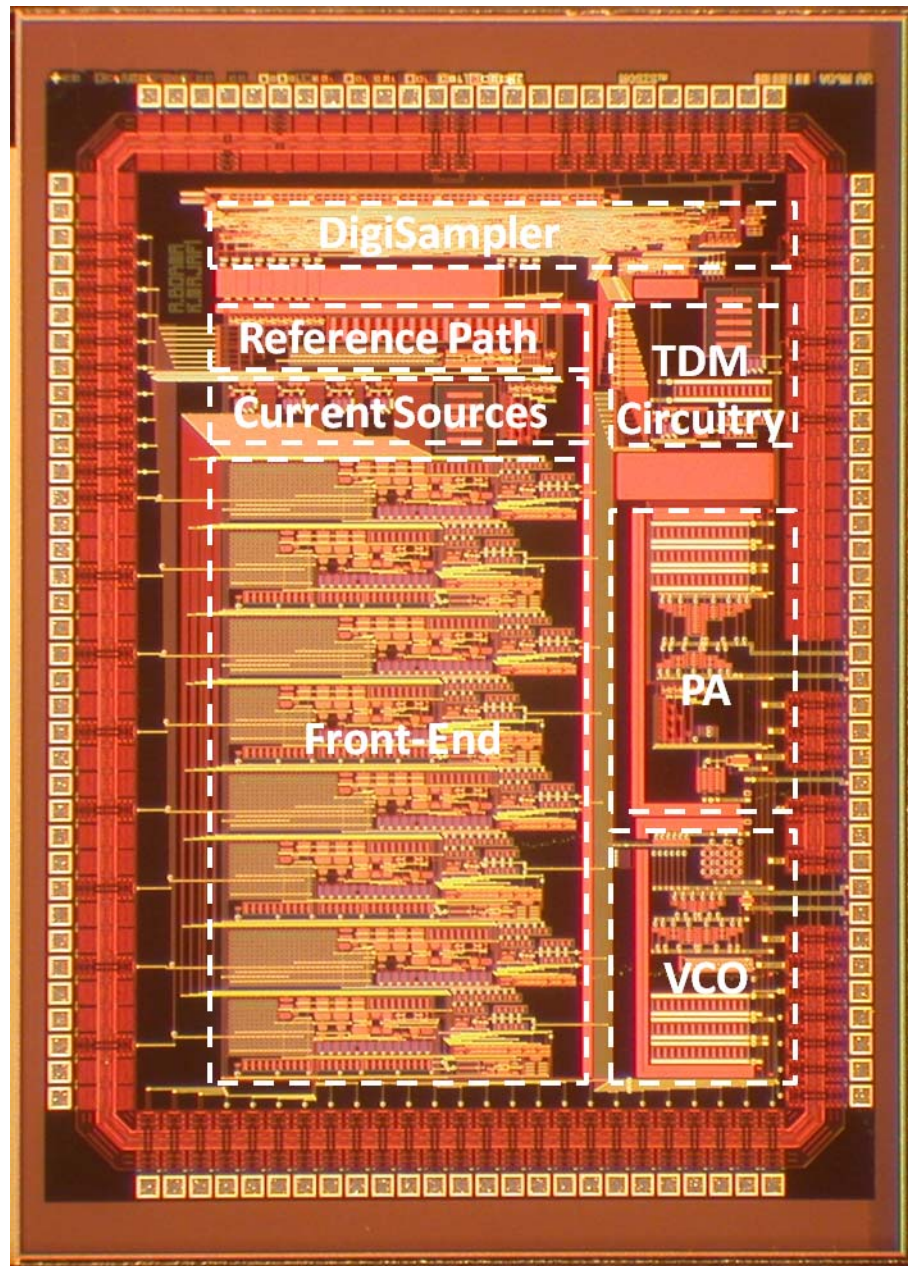


Figure 4-2: The proposed $2.85 \times 3.84 \text{mm}^2$ ASIC in $0.5 \mu\text{m}$ 2P3M n-well CMOS process

DigiSampler. The DigiSampler generates an on-chip clock, provides the user-programmability, and selects the channels for time division multiplexing. The TDM signal is buffered by a wide bandwidth buffer which drives the modulating input of the voltage controlled oscillator (VCO). The VCO's output (FM signal) is amplified by a class-C power amplifier (PA) which its emitted power is user-adjustable through 4-bits.

Having an adjustable emitted power is useful in trading transmission distance for battery life in recording setups where the transmitter is located in close proximity of the receiver. The programmable architecture of NC_V3 allows the user to optimize the performance metrics of interest depending on the specific requirement of the experiment (crosstalk level, transmission distance, SNR, etc.).

4.2. The Programmable Digital Controller: *DigiSampler*

The digital block, *DigiSampler*, serves as the brain of the ASIC. The digital block is included in all the multichannel wireless neural transmitters regardless of the architecture. The functionality of the digital block varies among various systems. This block can be as simple as a binary counter [4.4], implementing spike sorting algorithms [4.5], or compressing digital data [4.6]. The digital block employed in the presented system, *DigiSampler*, has the following functionalities: *i*) generates the on-chip sampling CLK with user-adjustable frequency, *ii*) selects any subset of neural/audio channels for time-division-multiplexing (TDM), *iii*) configures the front-end's signal path to use either ASIC's ground or any of the eight electrode signals as the reference, *iv*) sets the frame marker's voltage level, and *v*) sets the transmitter's emitted RF power. The *DigiSampler* has 3842 transistors and dissipates 24 μ W from a 1.5V_{DC} supply.

4.2.1. Modes of Operation

DigiSampler has two modes of operation:

i) RESET mode: in this mode the *DigiSampler* is not programmed by the user and all the programming inputs are floating. In the absence of external reset signal, about 120 μ s

after the power supply is connected, an internal RESET signal is generated which sets the DigiSampler to the default state. In this default state, all the eight neural channels are sampled with a sampling frequency of 20KHz per channel and the audio channel is left out. Frame marker is set to 200mV_{DC} ; and the class-C power amplifier is set to emit $300\mu\text{W}$ of RF power.

ii) PROGRAM mode: in this mode the DigiSampler is programmed externally by 7 programming inputs, e.g. CLK, RESET, PROGRAM, A_IN (4×), in 16 cycles. The programming interface is controlled by the host computer through a Matlab script. The Matlab script takes in the user specifications (multiplexed channels, sampling frequency, frame marker voltage level, emitted RF power, and front-end's configuration) and generates digital waveforms according to the DigiSampler's core programming protocol. The Matlab generated digital waveforms are sent to the NI-6534 DAQ card [4.7] which generates TTL level signals. These TTL signals are conditioned to the DigiSampler supply voltage (1.5V_{DC}) by the on-board resistive voltage divider.

4.2.2. Circuit Blocks

The block diagram of the DigiSampler is demonstrated in figure 4-3. It is composed of a synthesized core, and several full custom designed peripheral blocks:

i) clock generator, *ii)* reset signal generator, and *iii)* input latches.

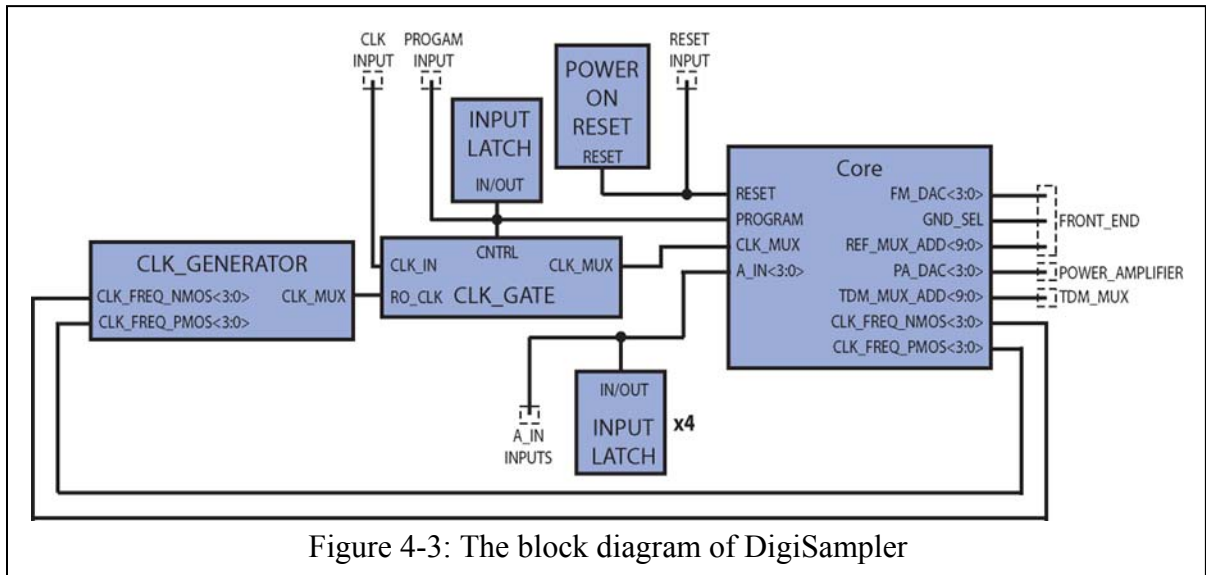


Figure 4-3: The block diagram of DigiSampler

4.2.2.1. The Core

The DigiSampler's core was synthesized with standard cell library; the core's register transfer level (RTL) Verilog code was optimized for power consumption. The core's RTL code, was synthesized in Design_Compiler (Synopsys) using an open-source standard cell library provided by OSU [4.8]. Encounter (Cadence) was used for cell placement and routing.

The DigiSampler's core is programmable through 7 external input pins, e.g. CLK, RESET, PROGRAM, and A_IN (4×). The programming sequence takes 16 cycles of external clock. As the PROGRAM bit is set high by the user, the core is detached from the on-chip clock generator and is clocked through the external CLK pin. The external RESET pin is an asynchronous reset signal which upon its arrival sets the core's internal registers to 0h. The core contains a Finite State Machine (FSM) which is activated during the programming cycle. The FSM state determines which of the core's 4-bit internal registers should take in the 4-bit data on the external pins A_IN<0:3>. At the end of the

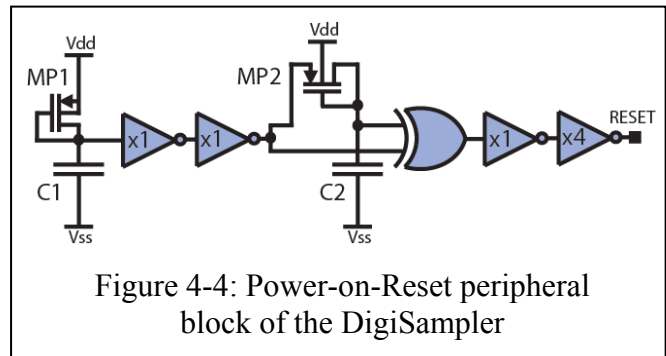
16 cycles the user should set the PROGRAM pin to 0, which detaches the core from the external clock (CLK) and connects the core to the on-chip clock generator. After the programming cycle, the user can disconnect the wireless neural transmitter from the programming board; the DigiSampler's peripherals retain the core's internal registers at the programmed state as long as the power supply stays connected to the transmitter.

4.2.2.2. Peripherals

The POWER-ON-RESET block has two functions: *i)* in the RESET operation mode, upon connection to the supply, it generates the RESET signal which sets the core's internal registers to 0h, and *ii)* during normal operation of the wireless neural transmitter, it holds the core's reset input at the ground level, despite the noise on the floating external RESET pin.

The circuit diagram of this block is shown in figure 4-4. This unit employs two RC networks to create an imbalanced path, similar to the mechanism of static hazard.

Each RC networks consist of a MOS-Bipolar pseudo resistors [4.9] and an on-chip double-poly 1pF capacitor. In figure 4-4, MP1 and C1 mark the arrival of the RESET signal; MP2 and C2 determine the



pulse width. About 120 μ s after power-on, this block creates an internal RESET signal with a pulse width of 11 μ s which puts the DigiSampler to the default state.

To ensure the functionality of the ASIC during the normal operation, the DigiSampler should maintain the internal registers at the programmed values. The DigiSampler's inputs are connected to IO-PADS which are driven by the user in PROGRAM mode; after programming, these high impedance input nodes are floating. In order to prevent the DigiSampler from latching in the noise

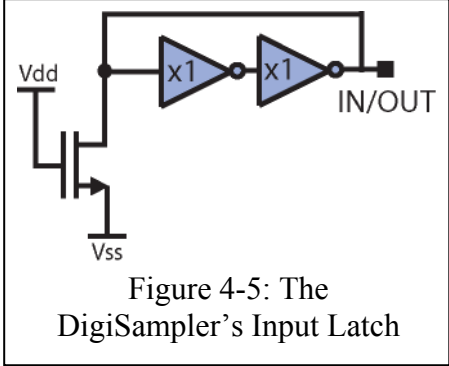


Figure 4-5: The DigiSampler's Input Latch

induced on the high impedance input nodes, the input latches shown in figure 4-5 retain the input nodes at the ground level regardless of the noise on these floating pins.

DigiSampler is capable of sampling any subset of neural/audio channels; this feature is useful in recording setups where there are less than eight implanted electrodes available or in cases where some of front-end channels malfunction and if selected can disturb the demultiplexing procedure at the receiver. As a consequence the sampling clock should be adjustable to provide a sampling frequency of about 20KHz per channel regardless of the number

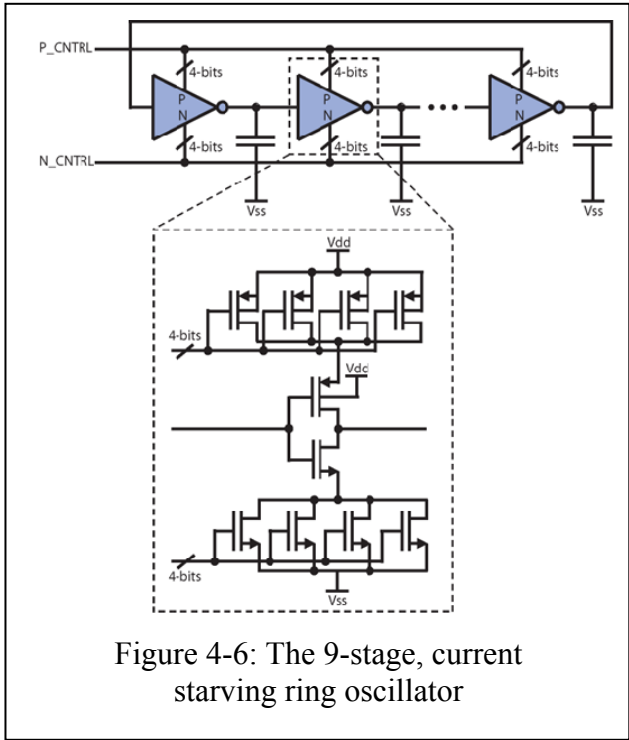


Figure 4-6: The 9-stage, current starving ring oscillator

of selected channels. The on-chip sampling clock frequency can be programmed in 16 steps from 200KHz to 716KHz.

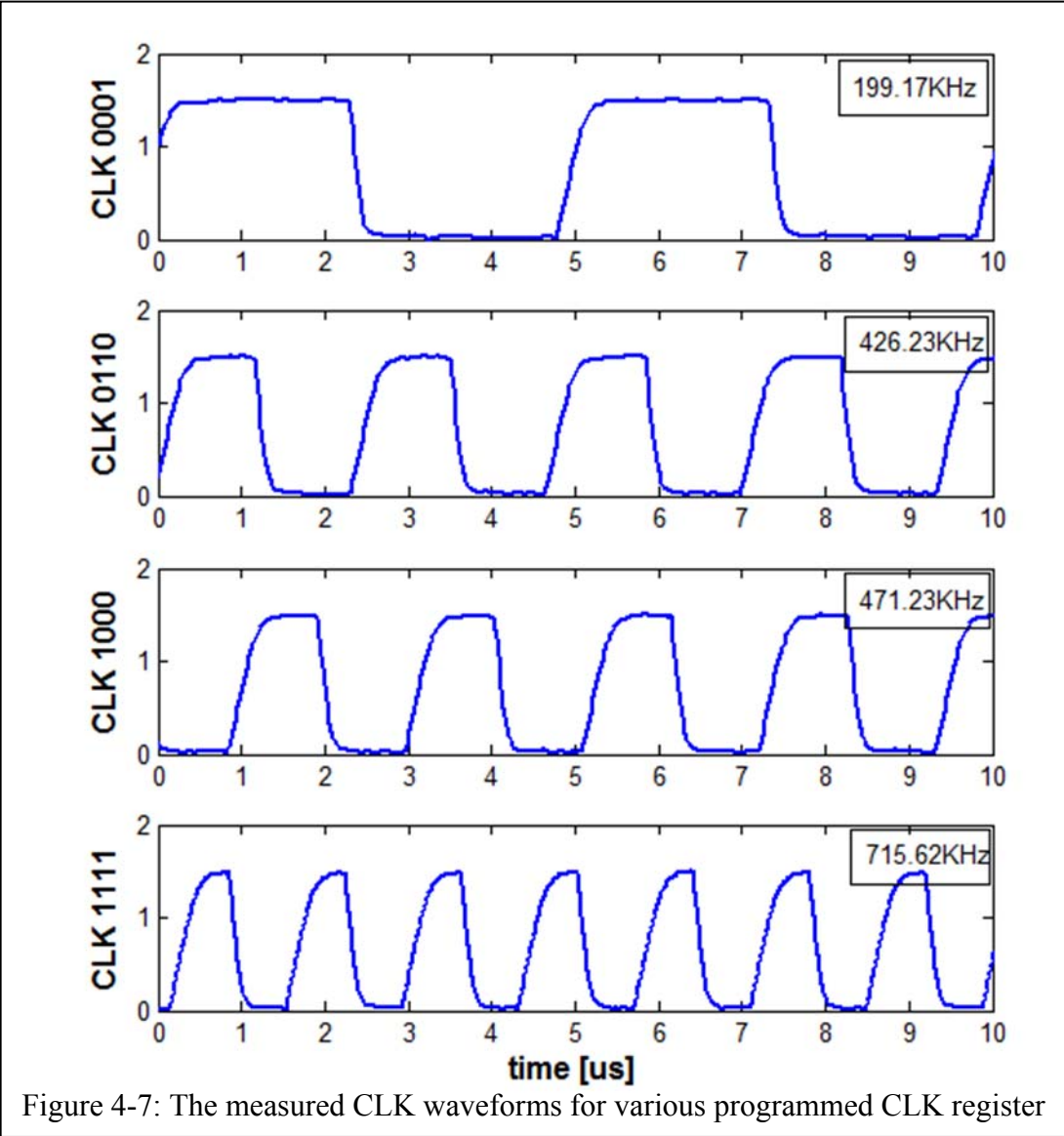


Figure 4-7: The measured CLK waveforms for various programmed CLK register

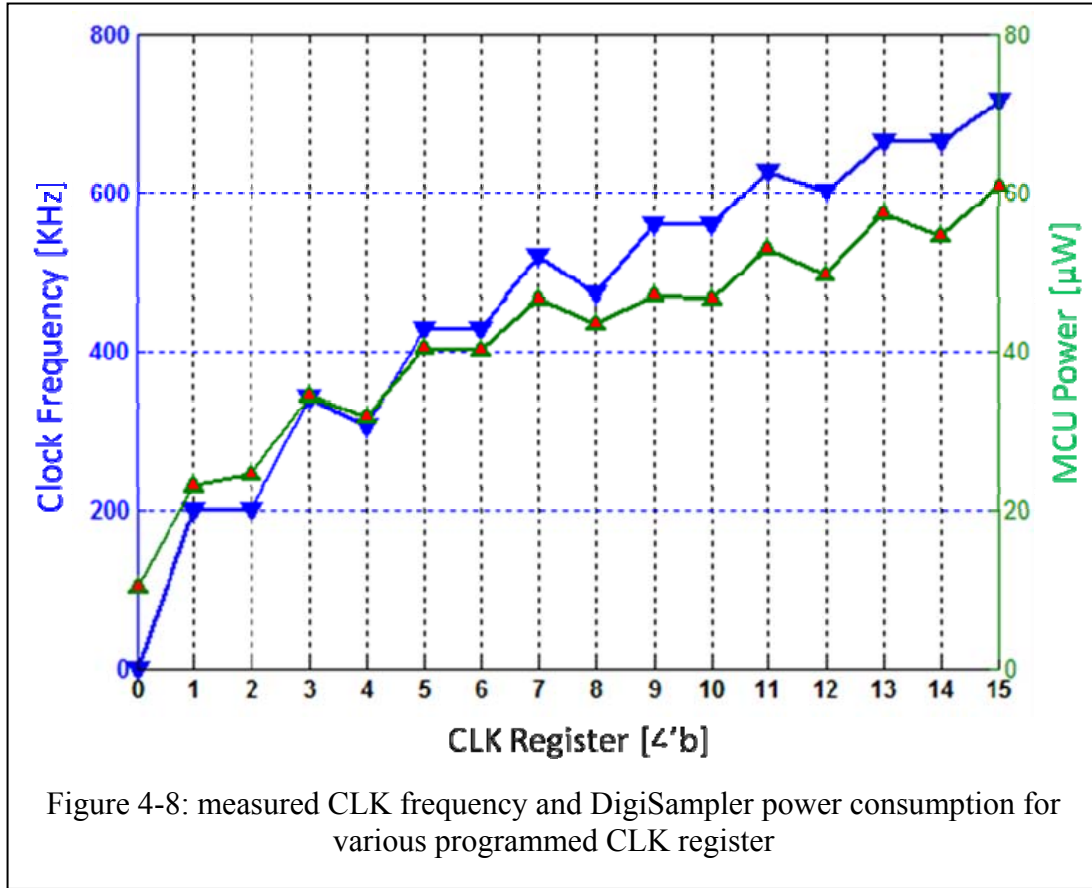
The clock generator, figure 4-6, is a 9-stage, current-starving ring oscillator followed by a frequency divider; the current-starving stages are controlled by four complementary signals (8-bits) from the DigiSampler’s core to generate a programmable clock frequency. Each stage is slowed down by a double-polysilicon 2.5pF on-chip capacitor. Figure 4-7 depicts the measured clock waveforms for various programmed clock register.

4.2.3. Power Consumption Reduction

Two $1.5V_{DC}$ silver-oxide batteries are used as the proposed neural transmitter's power supply. Even though a $3V_{DC}$ supply is available to the transmitter, due to low clock frequency of the DigiSampler, smaller supply voltages can be used to conserve energy. Dynamic voltage scaling (DVS) [4.10] was used to determine an optimum supply voltage for the DigiSampler. The advantage of using a supply voltage smaller than the available $3V_{DC}$ supply is double folded: *i)* it reduces the power consumption of the digital block, and *ii)* it reduces the digital noise in the mixed-signal ASIC. The optimum supply voltage was determined to be about $1.2V_{DC}$ however since a $1.5V_{DC}$ supply is already available on the chip, the entire digital block, DigiSampler, was supplied with $1.5V_{DC}$. Figure 4-8 shows the clock frequency and DigiSampler power consumption for various programmed clock register; the DigiSampler has a minimum clock frequency of 200KHz for a minimum power consumption of $24\mu W$.

To interface the DigiSampler to other blocks, level shifters should be used. These level shifters convert the $1.5V$ DigiSampler's bits to the $3V$ bits needed to set various digital to analog converters (DAC) and multiplexers.

There are two disadvantages to undervolting the supplies. The phase noise of the current starving ring oscillator is proportional to V_{DD}^{-2} and by halving the V_{DD} , the phase noise power spectrum quadruples. The main impact of the clock generator phase noise is on the TDM multiplexer. In time domain, the increased phase noise manifests in variation of the sampling frequency per channel; the time varying sampling frequency is however captured at the receiver side by the frame marker extraction algorithm. The other disadvantage of undervolting is the increased overlap time of the sampled channels



which potentially can lead to crosstalk among adjacent channels. Simulations show that for a V_{DD} of $1.5V_{DC}$ the channels overlap is less than 0.2% of the sampling window which does not contribute to the required system crosstalk ($\sim 5\%$)

4.3. The Front-End

The front-end connects directly to the implanted electrodes and has three major functions: *i*) amplifying the extracellular action potentials with amplitude of $50\mu V_{pp}$ - $500\mu V_{pp}$ and frequency contents of 500Hz-10KHz [4.11], *ii*) band pass filtering (BPF) the incoming signal for frequency range of 500Hz-10KHz to prevent aliasing in subsequent sampling stages, and *iii*) eliminating the electrode-ECF (Extracellular Fluid) interface offset which can be as large as $\pm 1V_{DC}$.

DC rejection method in bio-amplifiers intended for Local Field Potentials (LFP) can be different from DC rejection methods for neural amplifiers. LFP amplifier, due to their low frequency operation ($< 250\text{Hz}$), have the leverage of applying fancy techniques such as auto-zeroing (AZ) [4.13] and chopper modulation [4.14]; in neural amplifiers intended for extracellular action potentials, due to their frequency of operation auto-zeroing and chopper modulation result in prohibitively large power consumption. In neural amplifiers, there are three main methods for electrode-ECF DC rejection: *i)* in most neural amplifiers the electrode-ECF offset is eliminated by AC coupling the electrode to the amplifier through on-chip capacitors [4.15-4.19]. This capacitor along with an on-chip pseudo resistor provides a lower bound on the high pass frequency corner for the entire signal path, *ii)* direct coupling the electrode to the amplifier's input [4.20, 4.21]. In this method, DC rejection is achieved by a voltage divider composed of the electrode's Faradaic resistance and a pseudo resistor implemented by subthreshold PMOS transistor. The advantage of this method is the elimination of large input coupling capacitor and consequently preventing the signal degradation due to the capacitive divider between electrode-ECF's interface non-Faradaic capacitor and the input capacitor; this method works well in theory however it fails in practice as it has two major drawbacks: *a)* variation of high cutoff frequency: in different in-vivo experiments where different electrodes are implanted, the electrode-ECF (Extracellular Fluid) interface electrical model (C_{dl} and R_e) can be quite different depending on the type of implanted electrodes, the implanted region and the duration of implantation (chronic vs. acute). Variation of C_{dl} results in variation of high pass cutoff frequency in different in-vivo experiments, and *b)* inter-electrode DC offset: variation of R_e is more detrimental to

reliability than variation of C_{dl} as it affects the DC offset applied to the input of high gain neural amplifiers. And finally the third method of electrode-ECF (Extracellular Fluid) interface offset rejection is, *iii*) active DC rejection [4.22], where the low frequency contents of the amplifier's output is sensed and fed back into the signal path to remove the low frequency contents including the DC offset.

All the neural amplifiers employ some forms of high value resistor (HVR) due to their small high pass frequency corners ($<500\text{Hz}$). An important choice in neural amplifier design is the implementation of high value resistors (HVR). There are two major methods for implementing on-chip high value resistors: *i*) using subthreshold PMOS pseudo-resistors [4.12, 4.18, 4.21, 4.23], or *ii*) employing MOS-Bipolar elements [4.15, 4.16]. The latter has gained more attention recently due to its simple biasing mechanism.

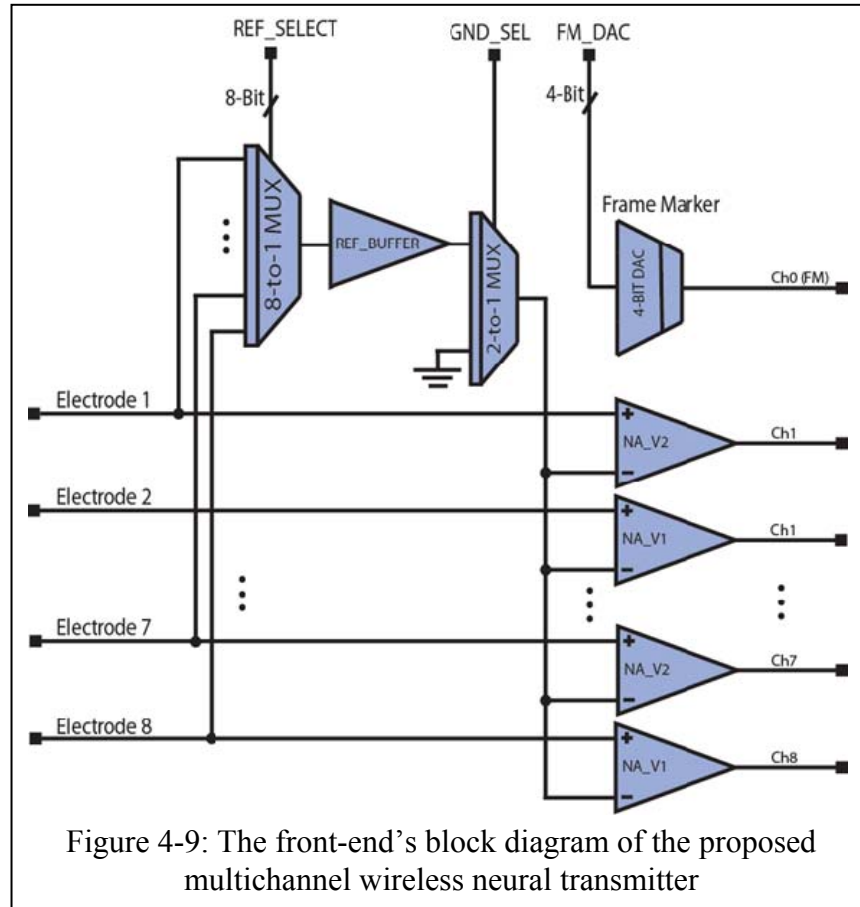
The amplification stage can have either open-loop [4.17, 4.22] or closed-loop [4.12, 4.15, 4.16, 4.18, and 4.21] configurations. The advantage of open-loop configuration is its inherent low power consumption; the disadvantage is its vulnerability to process and temperature variation (PTV) and poor power supply rejection ratio (PSRR); the PTV induced parameter fluctuations not only affects the IC yield but in WBFM multichannel systems the PTV induced inter-channel offset variation can make the entire IC dysfunctional by saturating the wireless link; this phenomenon is quantified in chapter 2. Table 4-1 compares performance metrics of neural amplifiers with their key implementation techniques.

	Harrison, [4.16] (2003)	Mohseni, [4.21] (2004)	Perlin, [4.18] 2006	Wattanapanitch, [4.15] 2007	Holleman, [4.17] 2007	Yin, [4.23] 2007	Gosselin, [4.22] 2007
Gain	39.5 dB	39.3 dB	59.5dB	40.85dB	36.1dB	39.3 dB	49.52dB
Power Consumption	80 μ W	115 μ W	75 μ W	7.56 μ W	805nW	27.2 μ W	8.6 μ W
Area (mm²)	0.160	0.107	0.072	0.16	.046	0.201	0.05
Supply Voltage	\pm 2.5	\pm 1.5	\pm 1.5V	2.8V	1V	\pm 1.7	1.8
Input Referred Offset	550 μ V	811 μ V	1mV	NA	NA	700 μ V	NA
Input Referred Noise	2.2 μ V _{rms} (0.5Hz-50KHz)	7.8 μ V _{rms} (0.1Hz-10KHz)	8 μ V _{rms} (10Hz-10KHz)	3.06 μ V _{rms} (45Hz-5.32KHz)	3.6 μ V _{rms} (.3Hz-4.7KHz)	3.6 μ V _{rms} (20Hz-10 KHz)	5.6 μ V _{rms} (98Hz-9.1KHz)
Process	1.5 μ m CMOS	1.5 μ m CMOS	0.5 μ m CMOS	0.5 μ m CMOS	0.5 μ m CMOS	1.5 μ m CMOS	0.18 μ m CMOS
Bandwidth	0.025Hz-7.2KHz	DC-9.1KHz	10Hz-9.1KHz	45Hz-5.32KHz	.3Hz-4.7KHz	0.015Hz-4KHz	98Hz-9.1KHz
Configuration	Closed Loop	Closed Loop	Closed Loop	Closed Loop	Open Loop	Closed Loop	Open Loop
DC Rejection	AC Coupling	Direct Coupling	AC Coupling	AC Coupling	AC Coupling	AC Coupling	Active DC Suppression

Table 4-1: Comparison of Neural Amplifiers

4.3.1. User Adjustable Signal Path

The front-end of the proposed multichannel wireless neural transmitter is shown in figure 4-9; the front-end has an adjustable signal path which its configuration is programmed by the user. The voltage difference between the eight electrodes and the reference voltage is amplified by eight neural amplifiers. The reference voltage can be selected from any of the eight neural channels or the ASIC's ground. The 1-bit GND_SEL from the DigiSampler selects the ground or one of the neural channels as the reference. The 8-bit REF_SELECT chooses one of the eight electrodes as the reference.



The reference signal is buffered by the “Reference Buffer” which drives the large parasitic capacitance from wires and NMOS inputs of the eight neural amplifiers. For in-vivo recordings, where a reference electrode is provided, having the reference voltage selected from the electrodes signals eliminates the common mode noise; among common mode noise sources, movement artifacts and 60Hz noise are of more importance as they can destabilize the system, e.g. wireless link saturation, leading to termination of back telemetry.

The front-end is composed of: *i*) reference circuitry, *ii*) eight neural amplifiers ($4 \times \text{NA_V1}$, $4 \times \text{NA_V2}$), and *iii*) user-adjustable frame marker.

4.3.1.1. The Reference Path

The reference circuitry configures the front-end's signal path to use either ASIC's ground or any of the eight electrode signals as the reference; it is composed of: *i*) an 8-to-1 channel-select (analog) multiplexer which selects one of eight electrodes signals as the reference, *ii*) a unity gain buffer which buffers the selected electrode signal, and *iii*) a 2-to-1 ground (analog) multiplexer which selects either the buffered selected electrode signal or the ASIC's ground as the reference voltage. The 2-to-1 analog multiplexer is shown in figure 4-10; all the blocks interfacing with the DigiSampler employ a level shifter for each bit which boosts the bit's high level voltage from V_{DD} (1.5V) to V_{cc} (3V). The interfacing level shifter is needed to keep the effective resistance of the multiplexer's on-resistance small. As shown in figure 4-10, the GND multiplexer uses

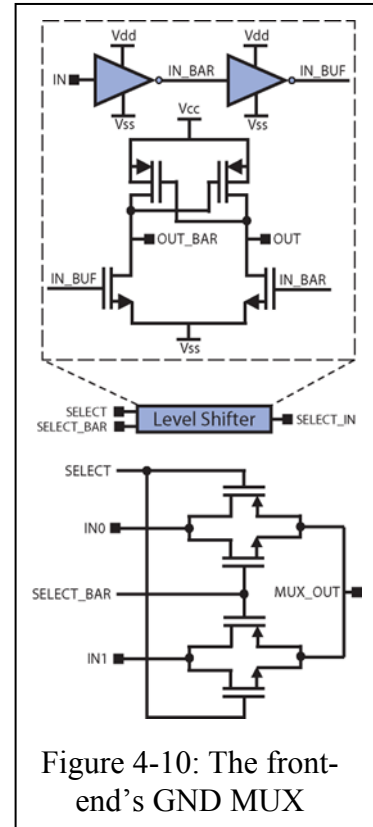


Figure 4-10: The front-end's GND MUX

CMOS pass gates instead of NMOS pass gates to further reduce the effective on-resistance of the pass gates; also the CMOS pass gates show smaller on-resistance for large noise signals, e.g. 60Hz and movement artifacts. The same design principles apply to the 8-to-1 channel-select multiplexer.

If an electrode signal is selected as the reference, its signal must be buffered to drive the large capacitive parasitics of the wires and input transistors of the neural amplifiers. The reference buffer shown in figure 4-11, is composed of an on-chip RC high pass filter, preceded by a standard 2-stage lead compensated OTA with unity-gain

configuration. The reference buffer dissipates $70\mu\text{W}$ from a $\pm 1.5\text{V}$ supply and has an open loop gain of 90dB .

In figure 4-11, C_1 is a capacitor composed of an array of $118\times$ double-polysilicon, 120fF capacitors. C_2 is a 120fF capacitor of the same type as in the array of C_1 . The capacitor C_2 is added to keep the capacitive loading on the reference buffer OTA's terminals the same as

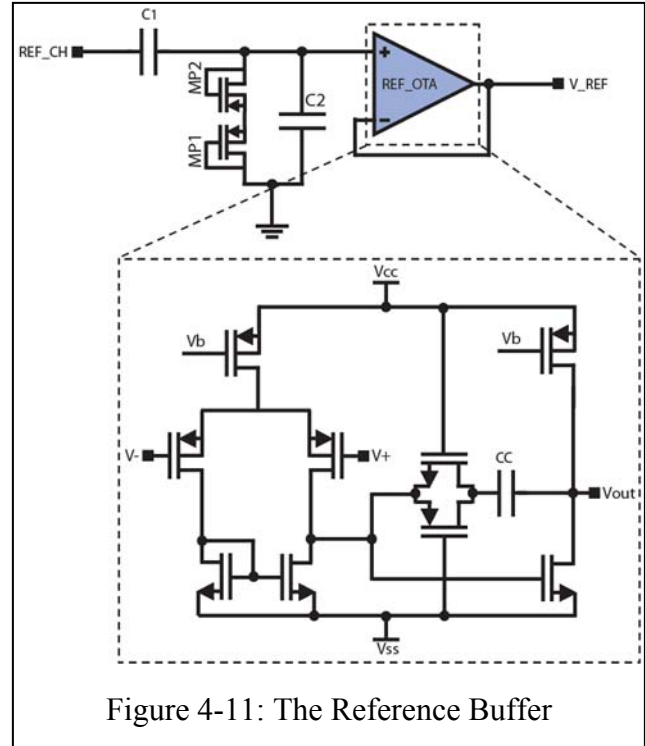


Figure 4-11: The Reference Buffer

that of neural amplifiers. The series combination of MP_1 and MP_2 provides a high impedance DC path between the OTA's input terminal and ground for biasing; these elements are back-to-back MOS-Bipolar pseudo resistors [4.9] which extends the dynamic range of high impedance path. The DC resistance of MOS-Bipolar pseudo resistors is in the order of $10\text{T}\Omega$ [4.16]; however their impedance drops for frequencies higher than 1Hz due to the stray capacitive elements of the device. The array capacitor, C_1 , AC-couples the reference buffer from the electrode which is the most efficient way of eliminating the electrode-ECF interface offset. Furthermore the series resistance of MP_1 and MP_2 forms a high pass filter with the array capacitor C_1 with sub-mHz cut off frequency. The neural amplifiers of the front-end which are responsible for action potentials amplifications, band pass filter the input signal from 500Hz to 10KHz . The reference circuitry however is supposed to buffer the common mode signal with all the

noise sources which vary from 60Hz to movement artifacts; therefore the sub-mHz high pass filter formed at the buffer's input is suitable for buffering large, low-frequency noise components of the common mode signal.

4.3.1.2. User Programmable Frame Marker

The frame marker is essentially a 4-bit resistive DAC with interfacing level shifters. The same design is used for all the DACs employed in the proposed ASIC. The power consumption of the frame marker is $70\mu\text{W}$.

There are $45 \times 3\text{K}\Omega$ polysilicon resistors between V_{CC} (1.5V_{DC}) and V_{SS} (-1.5V_{DC}) which adjust the frame marker voltage level between -500mV_{DC} and $+500\text{mV}_{DC}$ in 16 steps. During normal operation, the DAC of the frame marker is set at a constant value. However frame marker output drives the TDM multiplexer output to the set value during

its sampling window. The sampling window can be as narrow as $5\mu\text{s}$ when all the 9-channels are sampled; therefore frame marker output should settle down during the $5\mu\text{s}$ sampling window. Unlike other channels, the crosstalk level on the frame marker is not of importance as long as its

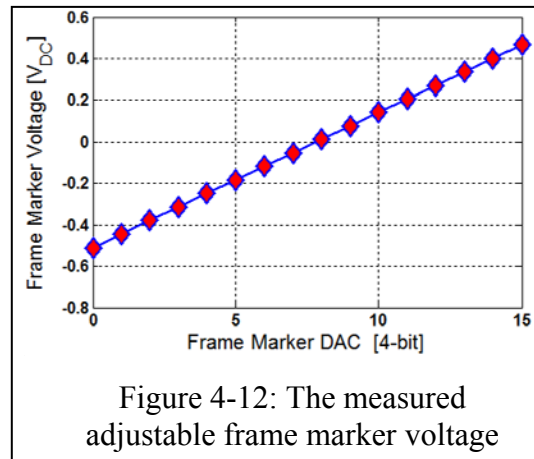


Figure 4-12: The measured adjustable frame marker voltage

voltage level stands substantially higher than other channels. Therefore the frame marker crosstalk can be traded with power consumption. The frame marker in this system is not buffered and its output resistance is designed to achieve a worst case 20% settling time. The advantage of having an adjustable frame marker is discussed in chapter 6.

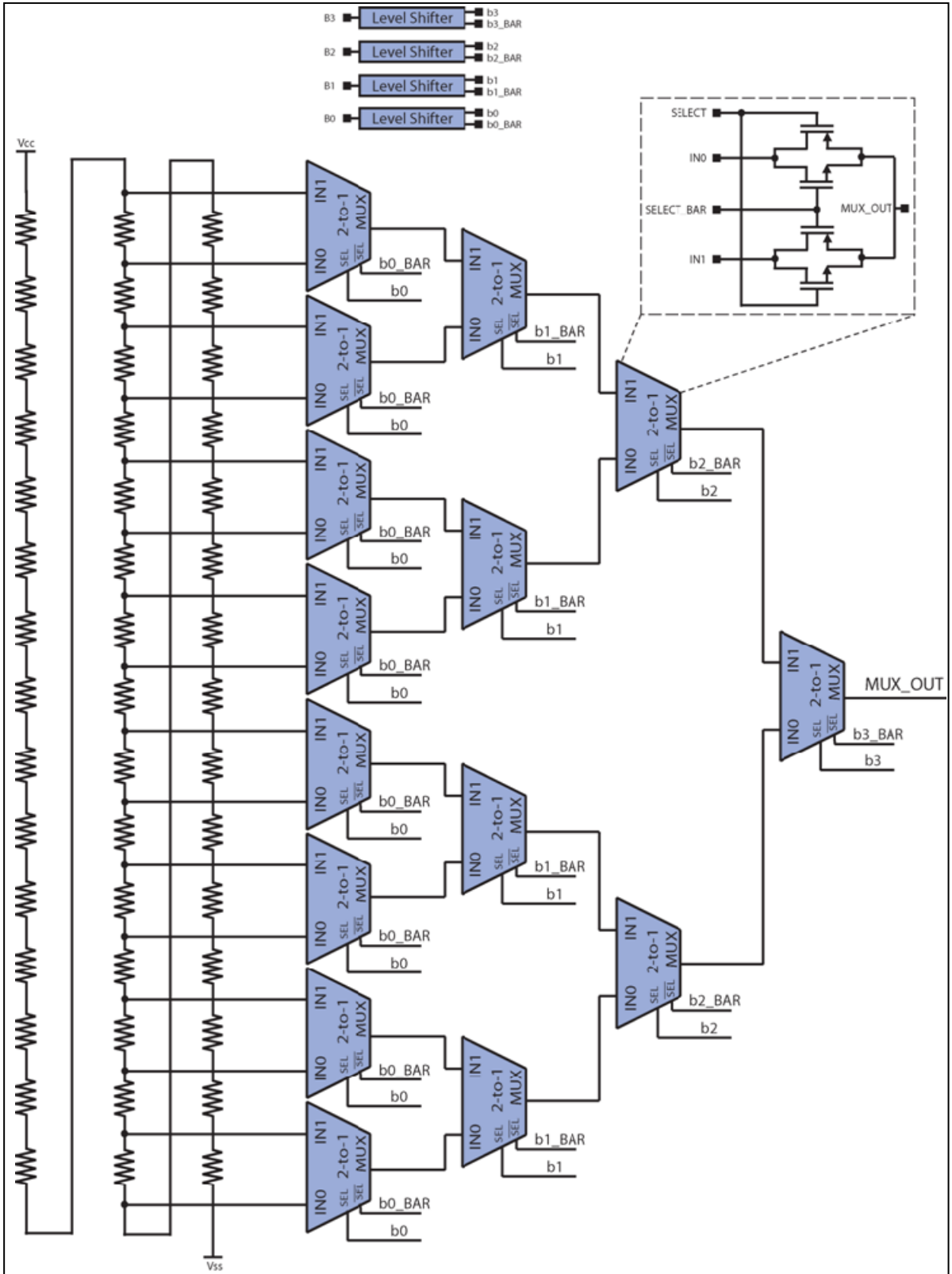


Figure 4-13: The user adjustable frame marker circuit diagram

Figure 4-12 depicts the measured frame marker voltage for various programmed frame marker register and figure 4-13 shows the circuit diagram of the frame marker.

4.3.2. Neural Amplifiers

The neural amplifiers: *i)* amplify neural action potentials with minimum noise addition, *ii)* band pass filter the input signals from 500Hz to 10KHz, (the low pass filtering at 10KHz eliminates the aliasing in subsequent sampling stages, and high pass filtering at 500Hz reduces the large-amplitude, low-frequency noise components) and *iii)* reject the electrode-ECF interface offset. In fully analog TDM-FM systems there is an additional requirement for the neural amplifiers of the front-end: having small inter-channel output offset ($<10\text{mV}_{\text{DC}}$).

All the amplifiers referenced in table 4-1, are not suitable for a fully analog TDM-FM system (except the last column [4.22]) due to their large input referred offset. The 2-stage lead compensated amplifier in [4.18], has an input referred offset of 1mV_{DC} and a passband gain of 60dB; such input referred offset translates into 1V_{DC} of front-end offset variation; in a fully analog TDM-FM system employing a voltage controlled oscillator (VCO) with a oscillator gain of 10MHz/V , the 1V_{DC} offset, spreads the channels frequency spectrum by at least 10MHz; an FM signal with such large bandwidth cannot be demodulated by the available FM receivers. Even if the resulting spectrum can be captured by a custom made wideband FM receiver, the SNR of the recovered neural channel reduces significantly as reflected in equation 2-58. Furthermore other than front-end offset any large, low-frequency noise component, e.g. 60Hz and movement artifacts, has the same detrimental impacts on the fully analog TDM-FM system as well.

To reduce the output offset of the front-end, the neural amplifiers in the proposed wireless multichannel neural transmitter (NC_V3), employ a technique so called active-low-frequency-suppression discussed in next section.

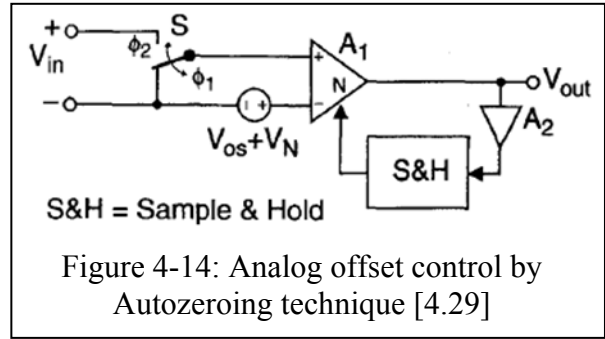
4.3.2.1. Low Frequency Noise Suppression

Any large, low-frequency noise component (60Hz, intrinsic offset, temperature-dependent offset drifts, movement artifacts, etc.) is detrimental for a neural amplifier employed in a fully analog TDM-FM system as quantified in chapter 2 (equation 2-58). The low-frequency noise components are related to various sources; they can be from the test subject (movement artifacts), the test setup (60Hz), the environment (temperature-dependent offset drifts), or the ASIC fabrication process (intrinsic offset).

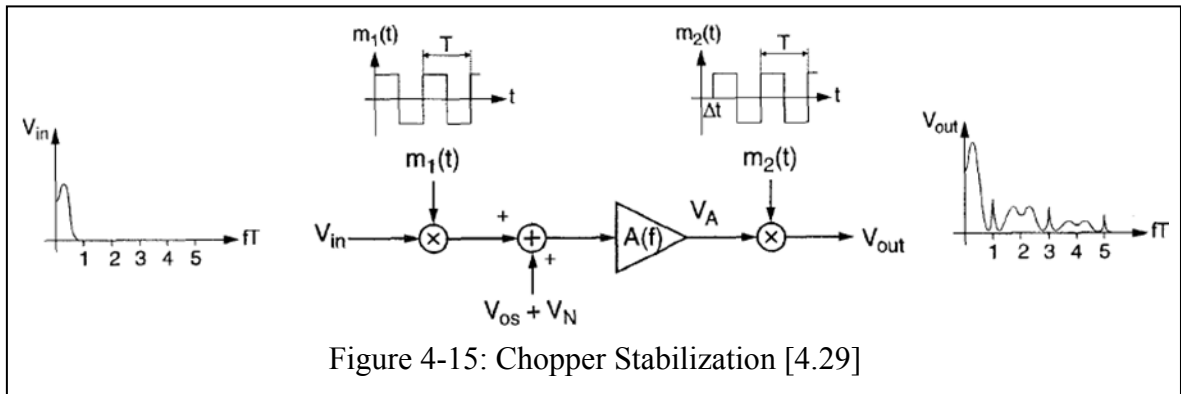
Among the low-frequency noise components, the neural amplifier's intrinsic offset can be minimized by proper design. The amplifier's intrinsic offset tends to worsen with CMOS process scaling. Aggressive scaling of the channel length, leads to reduction of supply voltage to prevent oxide breakdown and transistor's aging; however since the threshold voltage does not scale at the same rate, the analog designer has to bias some of the transistors in subthreshold regime. Therefore as a result of threshold voltage mismatch [4.24], lithographic induced perturbations [4.25, 4.26], and temperature dependent effects the offset voltage of neural amplifiers fabricated in submicron technologies tend to increase with technology. Some of these factors can be minimized by design/layout strategies; as an example threshold voltage mismatch reduces by employing large area devices [4.24], and the lithographic defect can be alleviated by layout techniques such as common centroid and the use of dummy devices [4.27].

There are some common architectural techniques to compensate for amplifier's offset [4.28]: *i)* autozeroing/correlated-double-sampling, *ii)* chopper stabilization, *iii)* ping pong, *iv)* post-fabrication laser trimming, and *v)* digitally assisted current adjustments.

Autozeroing (AZ) [4.29], figure 4-14, and correlated-double-sampling (CDS) are suitable for sampled data systems; there are two phases of operation: *i)* sampling phase in which the offset and low frequency components are sampled and stored, and *ii)* signal processing phase in which the input signal is amplified while offset and low frequency noise are subtracted. There are



some disadvantages to AZ and CDS; specifically high power consumptions, low operation speed, switching noise and charge injection, and an increase in the overall



amplifier's white noise due to aliasing, prevent using AZ and CDS in neural amplifiers. CDS is a particular case of AZ and will not be discussed further.

In Chopper Stabilization (CHS) technique, figure 4-15, the input signal is modulated to a higher intermediate frequency where there is no 1/f or DC offset present; after the amplification of the transposed signal, the amplified-modulated signal is

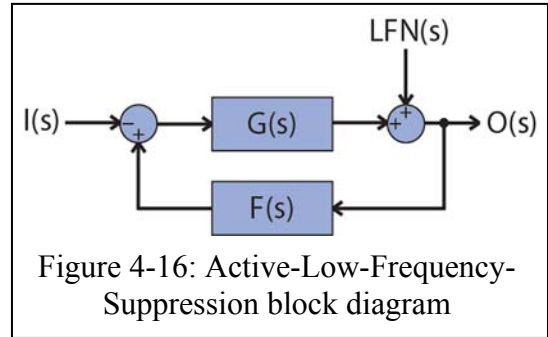
transposed to baseband. Unlike AZ and CDS, CHS can be used for continuous time operation. CHS also increases the overall amplifier's white noise [4.29], has large power consumption, and is limited to low frequency signals.

Ping pong amplifiers due to their redundant structures and employing AZ as part of their operations have large power consumption as well [4.30]. In post fabrication trimming technique, the amplifier has an adjustable element (resistors, or current sources); the fabricated amplifier is tested for its offset and the adjustable element is laser-trimmed to minimize the output offset. This technique is expensive and complex in implementation, in addition it does not compensate for dynamic offset and large, low-frequency noise components. And finally, some amplifiers take advantage of digital blocks and DACs to adjust the amplifier's load current for offset compensation [4.28]; in essence digitally assisted current adjustments is similar to the post fabrication trimming technique and poses the same problems.

To compensate for large, low-frequency noise components of the front-end, the neural amplifiers of the proposed work employ active-low-frequency-suppression (ALFS). The active-low-frequency-suppression is a technique in which the amplifier's output signal is sensed and its low frequency contents are fed back to the amplifier's input. Unlike AZ and CDS, ALFS is a continuous time operation and does not require high power consumption. Other than intrinsic offset, ALFS compensates for any large, low-frequency noise component, (60Hz, temperature-dependent offset drifts and movement artifacts). Furthermore since it does not sample the signal, the problem of increased white noise level due to aliasing (like in AZ and CHS) is resolved in neural amplifiers using ALFS.

4.3.2.1.1 The Concept of Active Low Frequency Suppression

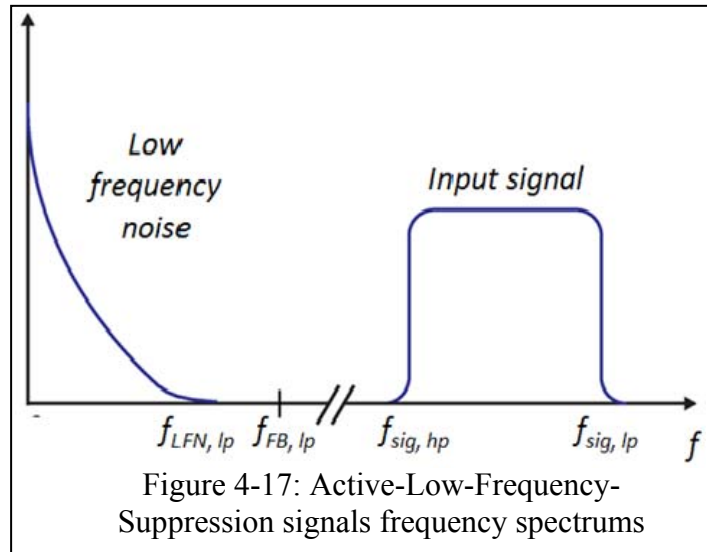
The block diagram of active low frequency suppression is shown in figure 4-16; in this figure LFN is the low-frequency-noise components of the entire circuits including that of the input signal which is manifested at the output of the amplifier; G is the main amplification block; F is the feedback network; I is the input signal and O is the output of the compensated amplifier.



By Laplace analysis of the circuit, the compensated output can be written in terms of the input and low frequency noise component as:

$$O(s) = \frac{-G(s)}{1 - G(s)F(s)} I(s) + \frac{1}{1 - G(s)F(s)} LFN(s) \quad (4 - 1)$$

It can safely be assumed that $LFN(s)$ has its frequency contents located at lower frequencies compared to the input signal $I(s)$ as shown in figure 4-17. In the case of neural amplifiers the inputs are action potentials with frequency contents between 500Hz and 10KHz where as the low frequency noise components have $f < 300Hz$.



If the feedback network ($F(s)$) has a low pass characteristic such that below certain frequency ($f_{FB,lp}$), the loop gain ($G(s)F(s)$), is much larger than unity, then for $f < f_{FB,lp}$ the output can be written as:

$$O(s) \cong \frac{1}{F(s)} I(s) - \frac{1}{G(s)F(s)} LFN(s) \quad (4 - 2)$$

Since the input, $I(s)$, does not have information in frequencies $f < f_{FB,lp}$, in 4-2, the first term of the right hand side does not contribute to the output signal; however the power spectrum of the large, low-frequency noise components, $LFN(s)$, is located at $f < f_{LFN,lp} < f_{FB,lp}$ and will be attenuated by the loop gain, $G(s)F(s)$.

If the magnitude of the feedback network's transfer function ($F(s)$) is small for the frequency band of input signal, $f_{sig,hp} < f < f_{sig,lp}$, such that loop gain, $G(s)F(s)$, is much smaller than unity the output can be written as:

$$O(s) \cong -G(s)I(s) + LFN(s) \quad (4 - 3)$$

In 4-3, the second term of the right hand side relates to the large-amplitude, low-frequency noise components which does not contribute to the output since its frequency contents are located at $f < f_{LFN,lp} \ll f_{sig,hp}$. However the first term of the right hand side in 4-3, is the input signal amplified. Investigating 4-2 and 4-3 it can be concluded that active-low-frequency-suppression, suppresses all the large low-frequency noise components including amplifier's dynamic and intrinsic offset and amplifies the input signal.

There are two different types of neural amplifiers used in the proposed system: NA_V1 and NA_V2; both share the same building blocks with the difference that

NA_V1 employs active-low-frequency-suppression and NA_V2 is configured as band pass amplifier.

In NA_V1, the feedback network is implemented by a continuous time Miller integrator with the transfer function: $F(s) = \frac{-1}{s\tau}$ where $\tau = R \times C$ is the time RC constant of the integrator. The amplification stage, $G(s)$, can be assumed to have a low pass characteristic with bandwidth, BW , and passband gain of $A0$: $G(s) = \frac{A0}{1+\frac{s}{BW}}$.

Rewriting the general active-low-frequency-suppression transfer function (4-1) for input-output, and substituting for $F(s)$ and $G(s)$:

$$H(s) = (-A0) \times \frac{BW}{\xi_1 \times \xi_2} \times \frac{s}{\left(1 - \frac{s}{\xi_1}\right) \times \left(1 - \frac{s}{\xi_2}\right)} \quad (4-4)$$

Equation 4-4, describes a bandpass filter with the high pass cut off frequency $\left(\frac{\xi_1}{2\pi}\right)$, and low pass cut off frequency $\left(\frac{\xi_2}{2\pi}\right)$:

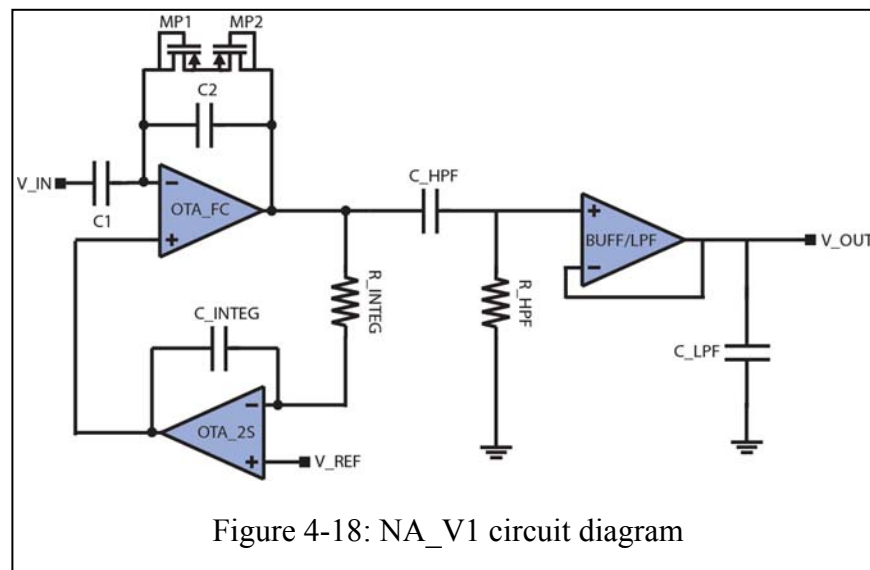
$$\begin{cases} \xi_1 = \frac{-BW + \sqrt{BW^2 - 4 \times A0 \times BW/\tau}}{2} \\ \xi_2 = \frac{-BW - \sqrt{BW^2 - 4 \times A0 \times BW/\tau}}{2} \end{cases} \quad (4-5)$$

The inequality, $BW^2 > 4 \times A0 \times BW/\tau$, should be satisfied to have a stable frequency response. Assuming $4 \times A0 \ll BW \times \tau$, the passband gain (A_{PB}), high pass cut-off frequency (f_{hp}) and low pass cut-off frequency (f_{lp}) of the overall active-low-frequency-suppression core can be calculated as:

$$\left\{ \begin{array}{l} A_{PB} \cong \frac{-A0}{1 - \frac{A0}{BW \times \tau}} \cong -A0 \\ f_{hp} = \frac{|\xi_1|}{2\pi} \cong \frac{A0}{2\pi \times \tau} = \frac{A0}{2\pi \times RC} \\ f_{lp} = \frac{|\xi_2|}{2\pi} \cong \frac{BW - \frac{A0}{\tau}}{2\pi} = \frac{BW - \frac{A0}{RC}}{2\pi} \end{array} \right. \quad (4-6)$$

4.3.2.2. NA_V1

The circuit diagram of NA_V1 is shown in figure 4-18; it is composed of an active-low-frequency-suppression core followed by a high pass filter and a buffer/LPF stage. A similar active-low-frequency-suppression core is implemented in [4.22]. However the neural amplifier introduced in [4.22], uses on an open-loop gain stage and has MOS-Bipolar pseudo resistor implementing the Miller integrator's large time



constant; such design choices pose several problems: *i*) poor Power Supply Rejection Ratio (PSRR) due to open-loop topology, *ii*) inter-channel high pass cut-off frequency variation, due to open-loop topology and MOS-Bipolar pseudo resistor (equation 4-6), and *iii*) inter-channel gain variations due to open-loop topology. The inter-channel gain

variation is addressed in the presented neural amplifier by employing a closed-loop folded cascode OTA which also resolves the poor PSRR issue. Inter-channel high pass cut-off frequency variation is solved by using an adjustable high value pseudo resistor (R_{INTEG}) as opposed to using MOS-Bipolar element for implementing the high value resistor of the Miller integrator.

The amplification of the neural action potential is achieved by a subset of active-low-frequency-suppression core: OTA_{FC} , C_1 , C_2 , MP_1 and MP_2 . OTA_{FC} is a low noise, low power folded-cascode operational transconductance amplifier (OTA) employed in a capacitive feedback configuration formed by C_1 and C_2 ; the passband gain of the overall neural amplifier is the capacitive ratio ($-C_1/C_2$). C_1 is composed of an array of 117×120 fF double-polysilicon capacitors and C_2 is a single element of the capacitor array. C_1 is directly connected to the implanted electrodes; there are two main advantages to this configuration: *i*) the ac-coupling technique effectively rejects the electrode-ECF interface offset, and *ii*) electrostatic discharge (ESD) immunity; in assembling process and transmitter handling, electro-static-discharge does not directly impact the threshold voltage of the input differential, which is important to keep the neural amplifier DC offset small. The value of C_1 is optimized for interfacing with $1M\Omega$ electrodes, e.g. Michigan probes.

MP_1 and MP_2 are MOS-Bipolar pseudo resistors [4.9] biasing the negative (-) terminal of the folded-cascode OTA. The high pass cut off frequency created by the MOS-Bipolar elements (MP_1 and MP_2) and the feedback capacitor (C_2) is sub-mHz and will not affect the band pass characteristic of the overall neural amplifier. Therefore as derived in 4-6, the low pass cut-off frequency of the active-low-frequency-suppression

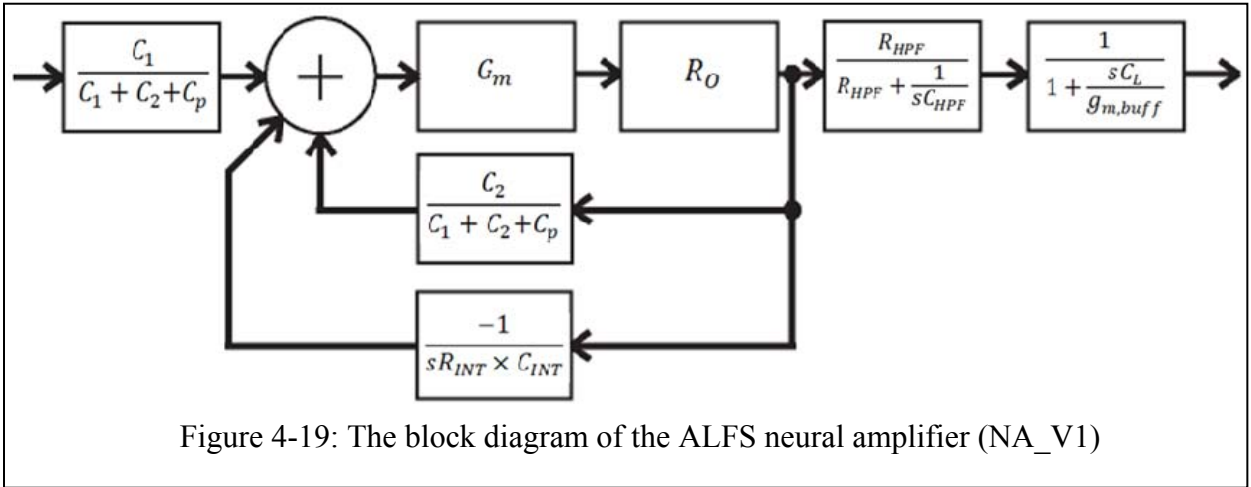


Figure 4-19: The block diagram of the ALFS neural amplifier (NA_V1)

core ($\frac{\xi_2}{2\pi}$) is determined by the dominant pole of the folded cascode OTA located at its output (10KHz). From equation 4-6, the high pass cut-off frequency of the overall neural amplifier ($\frac{\xi_1}{2\pi}$) can be approximated as:

$$f_{hp} = \frac{\xi_1}{2\pi} \cong \frac{C_1/C_2}{2\pi \times R_{INTEG} \times C_{INTEG}} \quad (4-7)$$

The f_{hp} is set to 500Hz by adjusting the Miller integrator's time constant, τ , to be 31.8ms.

By comparing the active-low-frequency-suppression circuitry of figures 4-18 and 4-16, it can be observed that the amplification stage ($G(s)$) is implemented with the folded cascode OTA in a capacitive feedback configuration, while the feedback network is formed by a continuous-time Miller-integrator. The RC high pass filter following the amplification stage, adds the second high pass cut off frequency at 500Hz to further remove the large-amplitude, low-frequency noise components; and finally the buffer stage is needed to drive the large capacitive load of wires and the TDM multiplexer. The noise contribution of the last two blocks is negligible due to the large gain of the

amplification stage; therefore in all the noise analysis only the folded cascode OTA is considered.

The block diagram of the neural amplifier, NA_V1, is shown in figure 4-19. As can be seen the overall neural amplifier, NA_V1, has a double feedback and its stability should be guaranteed by adjusting the parameters in equation 4-5. Furthermore the noise of the overall neural amplifier is determined by the input referred noise of the active-low-frequency-suppression circuitry and multiplied by the factor $\frac{C_1+C_2+C_p}{C_1}$; to lower the input referred noise of the overall neural amplifier this factor should be very close to unity by choosing the C_1 and C_2 according to size of the input differential pair transistors. The last two blocks of the NA_V1, are high pass filter and low pass filter respectively; they add poles at the same location as the poles of the active-low-frequency-suppression core.

From figure 4-19, the transfer function of the NA_V1 can be written as:

$$H(s) = \frac{-C_1}{C_2} \times \frac{s \times BW}{s^2 + BW \times s + \frac{C_1}{C_2} \times \frac{BW}{\tau}} \times \frac{R_{HPF}}{R_{HPF} + \frac{1}{sC_{HPF}}} \times \frac{1}{1 + \frac{sC_L}{g_{m,buf}}} \quad (4 - 8)$$

In 4-8, $\frac{BW}{2\pi}$ is the low pass cut off frequency of the gain stage folded cascode OTA; τ is the time constant of the continuous time Miller integrator; R_{HPF} is the on-chip adjustable high value pseudo resistor of the high pass filter and C_{HPF} is the double-polysilicon, on-chip capacitor of the high pass filter; C_L is the load of the neural amplifier; and $g_{m,buf}$ is the transconductance of the buffer/LPF. The circuit topologies of neural amplifier's building blocks will be explained in following sections.

4.3.2.2.1. The Folded Cascode OTA

The operational transconductance amplifier (OTA) used in the amplification stage of the neural amplifier ($G(s)$ in figure 4-16) is the most important building block which dictates the noise performance and power consumption of the front-end. Among the common OTA topologies, folded cascode is implemented since folded it trades output-swing for large open-loop gain for the same power consumption [4.27]; the topology choice is justified by noting that in the frequency band of interest, 500Hz-10KHz, the neural action potentials have a maximum amplitude of $500\mu V_{pp}$ which with a closed-loop gain of $100\times$ results in a maximum output swing of $50mV_{pp}$.

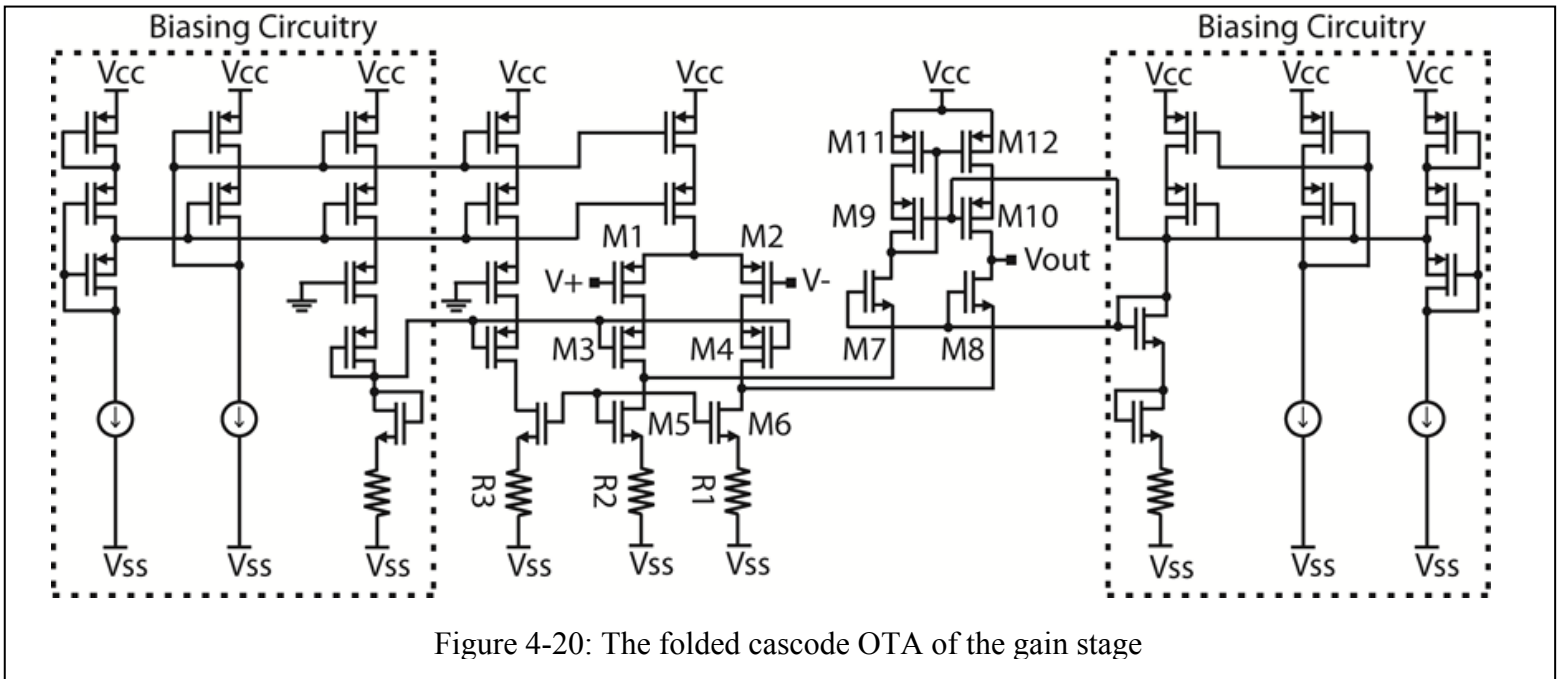


Figure 4-20: The folded cascode OTA of the gain stage

The circuit diagram of the designed folded cascode OTA is shown in figure 4-20. The OTA has 10-branches between voltage supplies including the bias circuitry and the minimum current flowing into any branch is 500nA. The presented folded cascode OTA employs local-bias-voltage, global-reference-current scheme; each OTA requires four

reference-currents for biasing purpose; the bias voltages for individual OTAs are generated locally, and the reference currents needed to bias the bias-voltage generators initiate from a precise current source at the other end of the ASIC. Some designs employ local diode-connected bias-voltage generators [4.18, 4.21]; this approach consumes less power as the current sources can be eliminated, however these OTAs are more prone to PTV compared to OTAs using local-bias-voltage, global-reference-current schemes. Even though in the current system each OTA has its own bias voltage generator, for systems with large number of channels, it is possible to combine the current sources and bias voltage generators, and distribute the global bias voltages to all the channels.

The devices which maximizing their transconductance (input differential pair), or output impedance (cascode devices), is of interest, operate in subthreshold regime by increasing their W/L ratio; whereas the devices which their matching is important, e.g. current mirrors, operate in strong inversion regime. To alleviate the limited voltage headroom while providing each branch with accurate current, all the PMOS current mirrors are low voltage cascode current mirrors [4.27] biased in strong inversion regime.

Due to the frequency band of neural amplifiers, Flicker ($1/f$) noise is an important factor in overall noise performance of the system. The most common solution to Flicker ($1/f$) noise is to use large-area PMOS devices for the neural amplifier OTA's input differential pair [4.15, 4.16, and 4.21]; it is known that PMOS transistors exhibit lower Flicker noise than their NMOS counterparts but this difference diminishes in submicron technologies [4.27]. Other transistors of the amplifier contribute to the Flicker noise and they are not necessarily optimized for small $1/f$ noise. In the presented folded cascode OTA, input differential pair is implemented with large-area PMOS devices to reduce

their Flicker noise contribution; furthermore active-low-frequency-suppression removes the low frequency contents of the output signal, therefore suppresses 1/f noise residuals.

The presented folded cascade OTA benefits from the useful techniques introduced in [4.15]. Specifically, this OTA differs from a standard folded cascode OTA as it employs source-degenerated current mirrors, cascodes the input differential pair, and uses current scaling between the input branch and the folded branch.

In a standard folded cascode OTA the currents in the folded branch and the input branch are equal. But in the presented OTA, the folded branch current is a fraction of the input branch current; this technique is known as current scaling [4.15]. Since the current noise of the CMOS transistors is proportional to g_m , by reducing the folded branch current the noise contributions of the folded branch transistors, M7-M12, becomes insignificant; therefore noise performance and power consumption are improved simultaneously.

Despite the benefits of current scaling, this technique cannot be implemented in standard folded cascode OTAs since it degrades the OTA's transconductance. Referring back to figure 4-20, in a standard folded cascode OTA the input differential pair is not cascoded (M3, M4) and the NMOS current mirrors are not source-degenerated (R1, R2); if current scaling is employed in such a circuit, by reducing the folded branch current, the impedance of the path looking into the M7 and M8 sources, increases and becomes comparable to the parallel impedance of the folding point. To resolve this issue, the presented OTA has its input differential pair cascoded (M3, M4), and employs source-degenerated current mirrors (R1, R2) to increase the impedance of the folding point such that the overall transconductance is not degraded by reducing the folded branch current.

The source-degenerated NMOS current-mirror also cancels the current noise of the NMOS devices; in fact the thermal resistance noise (R_1, R_2) replaces the NMOS drain current noise which is much larger than the thermal resistance noise.

The current scaling is explained by the circuit diagram of figure 4-21. The goal is to have the folded branch current m times smaller than current of the differential input

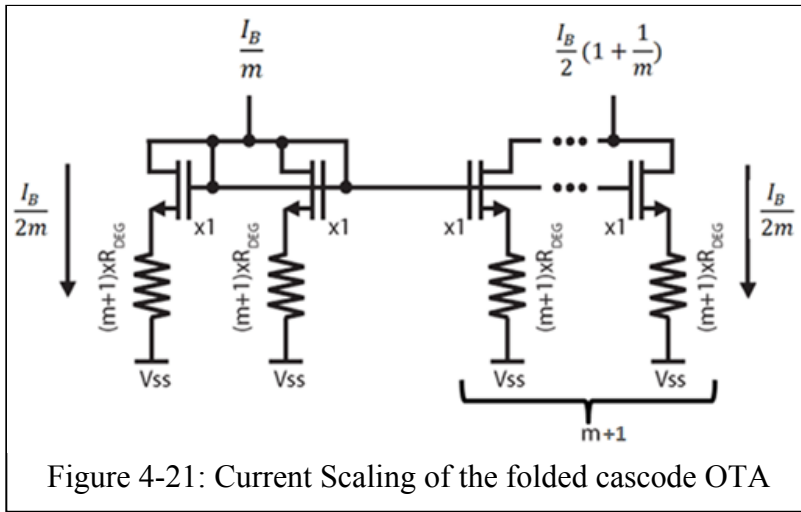


Figure 4-21: Current Scaling of the folded cascode OTA

branch. To achieve the current scaling, precise current ratio between the input differential pair branch and the biasing branch, in figure 4-21, is required. Therefore the PMOS current mirrors

are high swing cascode current mirrors [4.27] providing the input differential branch and the bias branch with current levels of $\frac{I_B}{2}$ and $\frac{I_B}{m}$ respectively. The total current into the input differential pair is I_B , such that each branch of the input differential pair has a current of $\frac{I_B}{2}$; to have a current scaling with ratio of m , each branch of the folded path should have a current level of $\frac{I_B}{2m}$. Therefore the NMOS current mirrors should have a drain current of $\frac{I_B}{2} + \frac{I_B}{2m} = \frac{I_B}{2} \left(1 + \frac{1}{m}\right)$; from this current $\frac{I_B}{2}$ flows into each branch of input differential pair and the rest, $\frac{I_B}{2m}$, flows into each branch of the folded path. All the NMOS current mirrors are designed to operate in the strong inversion regime to desensitize the OTA against PTV. The NMOS current mirrors are implemented as the

parallel combination of m unit devices; however the parallel resistors are combined to reduce the chip area and are implemented with the high resistance electrode (POLY2) layer. The presented OTA has a current scaling ratio of $m = 4$. In figure 4-20, $R_1 = R_2 = R_{DEG}$, since there are $m + 1$ resistors with the value $(m + 1)R_{DEG}$ in parallel; R_{1b} is parallel combination of two $(m + 1)R_{DEG}$ resistors, and therefore $R_{1b} = \frac{(m+1)}{2}R_{DEG}$. With a current scaling ratio of 4 and a minimum branch current of 500nA the total folded cascode OTA current is 6 μ A.

By having the branch currents fixed, sizing of the OTA elements is done with the goals of optimizing the OTA overall transconductance and noise performance. The maximum transconductance achievable by the folded cascode OTA, G_m , is the transconductance of the input differential pair, g_m .

The transconductance of the presented OTA can be formulated as:

$$G_m = g_{m1} \times \left(\frac{G_{s3}}{G_{s3} + \frac{1}{r_{01}}} \right) \times \left(\frac{G_{s7}}{G_{s7} + G_{d5}} \right) \quad (4 - 9)$$

In above formula, g_{m1} is the transconductance of the input differential pair; $G_{s,i}$ is the admittance looking into the source of M_i ; and $G_{d,i}$ is the admittance looking into the drain M_i .

$$\begin{cases} G_{s3} = \frac{g_{m3} + \frac{1}{r_{03}}}{1 + \frac{R_{L3}}{r_{03}}} \\ R_{L3} = \frac{1}{G_{d5} + G_{s7}} \end{cases} \quad (4 - 10)$$

From 4-10, and assuming the intrinsic gain of the M3 is much larger than unity ($g_{m3}r_{03} \gg 1$), G_{s3} , can be written as:

$$G_{s3} \cong \frac{g_{m3}}{1 + \frac{1}{r_{03}(G_{d5} + G_{s7})}} \quad (4 - 11)$$

G_{s7} appears in 4-11 and 4-9, and to maximize the overall transconductance, G_{s7} should be maximized. The admittance looking into the source of M7 (G_{s7}) is:

$$G_{s7} = \frac{g_{m7} + \frac{1}{r_{07}}}{1 + \frac{1}{r_{03}g_{m11}}} \cong \left(\frac{g_{m11} \times r_{07}}{1 + g_{m11} \times r_{07}} \right) \times g_{m7} \quad (4 - 12)$$

From 4-12, to maximize G_{s7} , $g_{m11} \times r_{07}$ should be much larger than unity. M11 and M7 both are in the folded branch and have the same current level, $\frac{I_B}{2m}$. However M7 is biased in subthreshold and M11 is operating in strong inversion. By substituting the parameters in the inequality, $g_{m11} \times r_{07} \gg 1$, the following size constraint on the M11 is achieved:

$$\left(\frac{W}{L}\right)_{11} \gg \frac{1}{r_{07}^2} \times \frac{m}{\mu_p \times C_{ox} \times I_B} \quad (4 - 13)$$

By proper sizing of M11 and M12 according to 4-13, the 4-12 will reduce to $G_{s7} \cong g_{m7}$.

The other admittance in both 4-9 and 4-11 is the admittance looking into the drain of M5 and M6:

$$G_{d5} = \frac{1}{r_{05}} \times \frac{1}{1 + R_{DEG} \times (g_{m5} \times (1 + \chi) + \frac{1}{r_{05}})} \quad (4 - 14)$$

In 4-14, R_{DEG} , is the resistor of the source degenerated NMOS current mirrors M5 and M6.

Now the factor $\left(\frac{G_{s7}}{G_{s7}+G_{d5}}\right)$ in 4-9 can be calculated by substituting for G_{s7} and

G_{d5} . To maximize the overall transconductance, $G_{s7} \gg G_{d5}$ which results in:

$$g_{m7} \gg \frac{1}{r_{05}} \times \frac{1}{1 + R_{DEG} \times (g_{m5} \times (1 + \chi) + \frac{1}{r_{05}})} \quad (4 - 15)$$

The inequality of 4-15 is satisfied by increasing the W/L ratio of M7, increasing the resistance of the source degenerated NMOS current mirrors (R_{DEG}), and choosing a long channel length for the degenerated NMOS current mirrors, M5 and M6.

And finally the factor $\left(\frac{G_{s3}}{G_{s3}+\frac{1}{r_{01}}}\right)$ in 4-9, should be maximized by maximizing G_{s3} ;

knowing $G_{s7} \gg G_{d5}$:

$$G_{s3} \cong \frac{g_{m3}}{1 + \frac{1}{r_{03}(G_{d5} + G_{s7})}} \cong \frac{g_{m3}}{1 + \frac{1}{r_{03}G_{s7}}} \cong \frac{g_{m3}}{1 + \frac{1}{r_{03}g_{m7}}} \cong g_{m3} \quad (4 - 16)$$

G_{s3} is maximized if $r_{03}g_{m7}$ is much larger than unity; M7 and M3 both are biased in subthreshold and therefore their transconductance is $g_m = \frac{I_D}{nU_T}$. The drain

current of M3 is $\frac{I_B}{2}$ and the drain current of M7 is $\frac{I_B}{2m}$:

$$\begin{cases} I_{D3} = \frac{I_B}{2} \\ I_{D7} = \frac{I_B}{2m} \\ g_m = \frac{I_D}{nU_T} \end{cases} \Rightarrow \frac{g_{m7}}{g_{m3}} = \frac{I_{D7}}{I_{D3}} = \frac{1}{m} \quad (4 - 17)$$

Using 4-17, the inequality $r_{03}g_{m7} \gg 1$ can be written in terms of intrinsic gain of the input differential pair cascode devices (M3, M4) and the current scaling ratio, m :

$$r_{03}g_{m3} \gg m \quad (4 - 18)$$

By satisfying the inequality of 4-18, the G_{s3} is maximized and equals g_{m3} as 4-16 predicts. Now the factor $\left(\frac{G_{s3}}{G_{s3} + \frac{1}{r_{o1}}}\right)$ in 4-9 can be written as $\left(\frac{g_{m3}r_{o1}}{g_{m3}r_{o1} + 1}\right)$. To maximize this factor: $g_{m3}r_{o1} \gg 1$; both M3 and M1 operate in subthreshold regime and have the same current level, therefore $g_{m3} = g_{m1}$; now the final constraint to maximize the overall transconductance can be expressed in terms of intrinsic gain of the input differential pair:

$$g_{m1}r_{o1} \gg 1 \quad (4 - 19)$$

By satisfying the size constraints in 4-13, 4-15, 4-18, and 4-19 the overall transconductance of the OTA is very close to that of the input differential pair $G_m = g_{m1,2}$. The simulation results of the designed OTA show that the overall transconductance is 99% of the input differential pair transconductance.

To optimize the noise performance of the OTA it should be noted that only a few devices contribute to the output noise. Referring to figure 4-17, the current noise of the bias circuitry devices are cancelled by symmetry. Therefore only the devices in the signal path should be considered; furthermore the cascode device noise contribution is attenuated by the factor $\left(\frac{1}{1 + g_m R_L}\right)$ where g_m is the device transconductance and the R_L is the impedance, the source of the cascode device sees. The following devices contribute to the OTA's output noise and should be sized to minimize their noise contribution: *i*) the input differential pair (M1, M2), *ii*) the resistors of the source degenerated NMOS current mirrors (R1, R2), and *iii*) the active current mirrors of the folded branch (M11, M12).

$$\overline{I_{out}^2} \cong 2 \times \overline{I_{out,M1}^2} + 2 \times \overline{I_{out,R1}^2} + 2 \times \overline{I_{out,M11}^2} \quad (4 - 20)$$

Equation 4-20 sums up the noise contribution of elements impacting the OTA's output current noise. By maximizing the overall transconductance, all the current noise of the input differential pair appears at the output:

$$\overline{I_{out,M1}^2} = \left(\frac{G_{s3}}{G_{s3} + \frac{1}{r_{o1}}}\right)^2 \times \left(\frac{G_{s7}}{G_{s7} + G_{d5}}\right)^2 \times \overline{I_{D,M1}^2} \cong \overline{I_{D,M1}^2} \quad (4-21)$$

The current noise of the active current mirrors of the folded branch (M11, M12), appears directly at the OTA's output with no degradation:

$$\overline{I_{out,M11}^2} = \overline{I_{D,M11}^2} \quad (4-22)$$

The source degenerated NMOS current mirror's resistors, attenuate the noise contribution of the NMOS devices by the factor $\left(\frac{1}{1+g_{m5}R_{DEG}}\right)$, and to achieve this $g_m R_{DEG} \gg 1$. However these resistors current noise appears directly at the OTA's output:

$$\overline{I_{out,R1}^2} \cong \left(\frac{g_{m5}}{g_{m5} + \frac{1}{R_{DEG}}}\right)^2 \times \left(\frac{G_{s7}}{G_{s7} + G_{d5}}\right)^2 \times \overline{I_{n,R1}^2} \cong \overline{I_{n,R1}^2} \quad (4-23)$$

The equation in 4-23 is achieved by knowing that $g_m R_{DEG} \gg 1$ and $G_{s7} \gg G_{d5}$; the latter was obtained when maximizing the overall OTA transconductance.

The thermal noise current of a MOSFET according to the Van-Der-Ziel model [4.31] is $\overline{I_D^2} = 4kT\gamma g_m$, where $\gamma = 2/3$ for devices biased in strong-inversion and $\gamma = \frac{n}{2}$ for subthreshold devices [4.15] where n is the subthreshold slope; by substituting 4-21 to 4-23 into the 4-20:

$$\overline{v_{n,thermal,in}^2} = \frac{\overline{I_{out}^2}}{g_{m1}^2} = \frac{1}{g_{m1}^2} \left[4kTng_{m1} + \frac{8kT}{R_{DEG}} + \frac{16kTg_{m11}}{3} \right] \quad (4-24)$$

Equation 4-24 describes the thermal noise of the OTA. The input referred voltage noise, 4-24, can be used to size the OTA devices with the goal of minimizing the OTA noise. From 4-24, it can be observed that the input differential pair devices transconductance should be maximized. For a fixed current, these devices should operate in subthreshold where $\frac{g_m}{I_D}$ is maximized. By increasing the input differential pair bias current the transconductance of these devices increase according to $g_m = \frac{I_D}{nU_T}$ revealing the tradeoff between power consumption and noise performance. Ideally the OTA noise is dominated by the input differential pair and the noise contribution of other devices is negligible; to have the resistor noise negligible: $\frac{8kT}{R_{DEG}} \ll 4kTng_{m1}$; by substituting for the transconductance as $g_{m1} = \frac{I_D}{nU_T} = \frac{I_B}{2nU_T}$ the minimum resistance of the source degenerating resistors is bounded as:

$$R_{DEG} \gg \frac{4U_T}{I_B} \quad (4 - 25)$$

By satisfying the source degenerating resistor according to the equation 4-25, the noise contribution by the source degenerating resistors is minimized. Also as can be seen in 4-25, by increasing the bias current the resistor value reduces which reveals the tradeoff between the power consumption and area.

To minimize the noise contribution of the folded branch active current mirrors: $\frac{16kTg_{m11}}{3} \ll 4kTng_{m1}$. Since the folded branch active current mirrors (M11,

M12) operate in strong inversion their transconductance is $g_{m11} = \sqrt{2\mu_p C_{ox} \left(\frac{W}{L}\right)_{11} I_D} = \sqrt{2\mu_p C_{ox} \left(\frac{W}{L}\right)_{11} \frac{I_B}{2m}}$. On the other hand the input differential pair transistors operate in

subthreshold region and their transconductance is $g_{m1} = \frac{I_D}{nU_T} = \frac{I_B}{2nU_T}$. Therefore the criteria for minimizing the noise contribution of the folded branch active current mirrors (M11, M12) can be formulated as:

$$\left(\frac{W}{L}\right)_{11} \ll \frac{9mI_B}{64U_T^2\mu_p C_{ox}} \quad (4-26)$$

In 4-26, m is the current scaling ratio, I_B is the input differential pair bias current, μ_p is the mobility of the holes, C_{ox} is the oxide capacitance per unit area, and U_T is the thermal voltage (kT/q). By sizing the folded branch active current mirrors (M11, M12) according to 4-26, their thermal noise contribution is minimized. Equation 4-25 and 4-26 can be used to size the devices such that the thermal noise of the OTA is dominated by the input differential pair.

In considering the flicker noise, the equation 4-20 can be used; furthermore the resistors in 4-20 have no contribute to the OTA Flicker noise. The flicker noise of a CMOS transistor in the bandwidth Δf , at the offset frequency f , can be attributed to its gate voltage as: $\overline{v_{1/f}^2} = \frac{K}{WLC_{ox}} \frac{\Delta f}{f}$ [4.27]; in this formula K is the flicker noise coefficient and is an empirically fitting parameters (hopefully) provided by the device models; W is the transistor width, L is the transistor channel length, and C_{ox} is the oxide capacitance per unit area. It is known that PMOS transistors exhibit lower Flicker noise than their NMOS counterparts ($K_P < K_N$) but this difference diminishes in submicron technologies [4.27]. Nevertheless PMOS transistors are used to implement the input differential pair of the presented OTA. Substituting for the flicker noise in equation 4-20, the flicker noise density of the output current can be expressed as:

$$\overline{I_{out,flicker}^2} = \frac{2K_P}{(WL)_1 C_{ox}} g_{m1}^2 + \frac{2K_P}{(WL)_{11} C_{ox}} g_{m11}^2 \quad (4 - 27)$$

The input referred voltage of the flicker noise can be calculated as:

$$\overline{v_{n,flicker,in}^2} = \frac{\overline{I_{out,flicker}^2}}{g_{m1}^2} = \frac{2K_P}{(WL)_1 C_{ox}} + \frac{2K_P}{(WL)_{11} C_{ox}} \left(\frac{g_{m11}}{g_{m1}}\right)^2 \quad (4 - 28)$$

Therefore to minimize the flicker noise of the input differential pair, the device area (WL) should be made large which shows the tradeoff between the area and noise performance. Furthermore to minimize the flicker noise contribution of the folded branch active current mirrors (M11, M12), the second term of the 4-28 right hand side, should be made much smaller than the first term. By substituting for the transconductances in 4-28, the input referred voltage of the flicker noise can be written as:

$$\overline{v_{n,flicker,in}^2} = \frac{2K_P}{(WL)_1 C_{ox}} + \frac{8K_P \mu_p n^2 U_T^2}{mI_B} \times \frac{1}{L_{11}^2} \quad (4 - 29)$$

Equation 4-29 can be used to size the devices such that the flicker noise is dominated by the input differential pair:

$$L_{11} \gg \sqrt{\frac{4\mu_p n^2 U_T^2}{mI_B} (WL)_1 C_{ox}} \quad (4 - 30)$$

Equation 4-25, 4-26, and 4-30 provide the designer with sizing guidelines such that the noise contribution of the folded cascode OTA is dominated by the input differential pair devices.

Table 4-2, sums up the proposed OTA devices specifications to achieve the constraints required to optimize the OTA's transconductance and noise performance according to the formulas derived earlier.

Table 4-2: The Folded Cascode OTA devices specifications

Device	W/L	I _D	Operation Region
M1, M2	300 μ m/1.2 μ m	2 μ A	Subthreshold
M3, M4	90 μ m/1.2 μ m	2 μ A	Subthreshold
M5, M6	10.5 μ m/1.2 μ m	2.5 μ A	Strong Inversion
M7, M8	120 μ m/1.2 μ m	500nA	Subthreshold
M9, M10	6 μ m/1.8 μ m	500nA	Strong Inversion
M11, M12	6 μ m/1.8 μ m	500nA	Strong Inversion

The designed folded cascode OTA is frequency-compensated by having a double-polysilicon capacitor of 8.5pF at the output node. The designed folded cascode OTA has a simulated open loop gain of 101dB and a phase margin of 75°.

4.3.2.2.2. The Continuous Time Miller Integrator

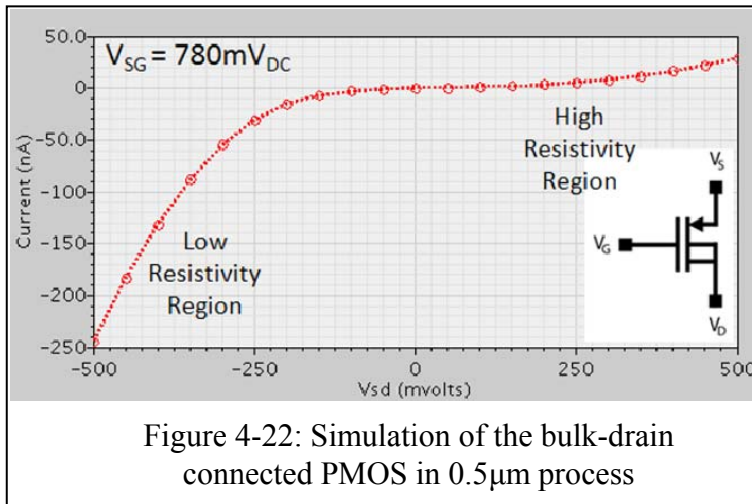
The active-low-frequency-suppression employed in the presented neural amplifier, NA_V1, has a continuous time Miller integrator as its feedback network. As derived in the equation of 4-7, the time constant of this integrator affects the overall neural amplifier frequency response; with a fixed passband gain of 40dB, to have a high pass cut-off frequency of 500Hz, the time constant of the Miller integrator should be 31.8ms. Such large time constant may not be implemented by passive RC elements. By having a moderate size, double-polysilicon, on-chip capacitor, the large time constant is achieved by using adjustable ultra-high value CMOS pseudo resistors [4.33].

The integrator resistor is a modification to the CMOS pseudo resistor introduced in [4.33]; the ultra-high-value floating tunable CMOS resistor introduced in [4.33] is based on a bulk-drain connected PMOS transistor and is explained by figure 4-22; as the

name suggests the bulk of the device (NWELL) is connected to its drain terminal and the device is biased in subthreshold. The drain current of a PMOS transistor in subthreshold is [4.34]:

$$I_D = \frac{W}{L} I_t \exp\left(\frac{V_{SG} - |V_{th}|}{nU_T}\right) \left[1 - \exp\left(\frac{-V_{SD}}{U_T}\right)\right] \quad (4 - 31)$$

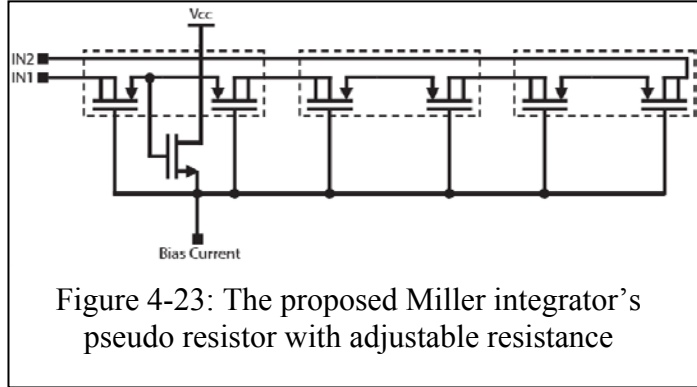
As the source-drain voltage of the device increases, the threshold voltage of the PMOS is modified and as a result the drain current increases; this phenomenon results in a finite source-drain conductance and by adjusting the source-gate bias voltage a wide range of resistance can be attained by a single device. There are two issues with this



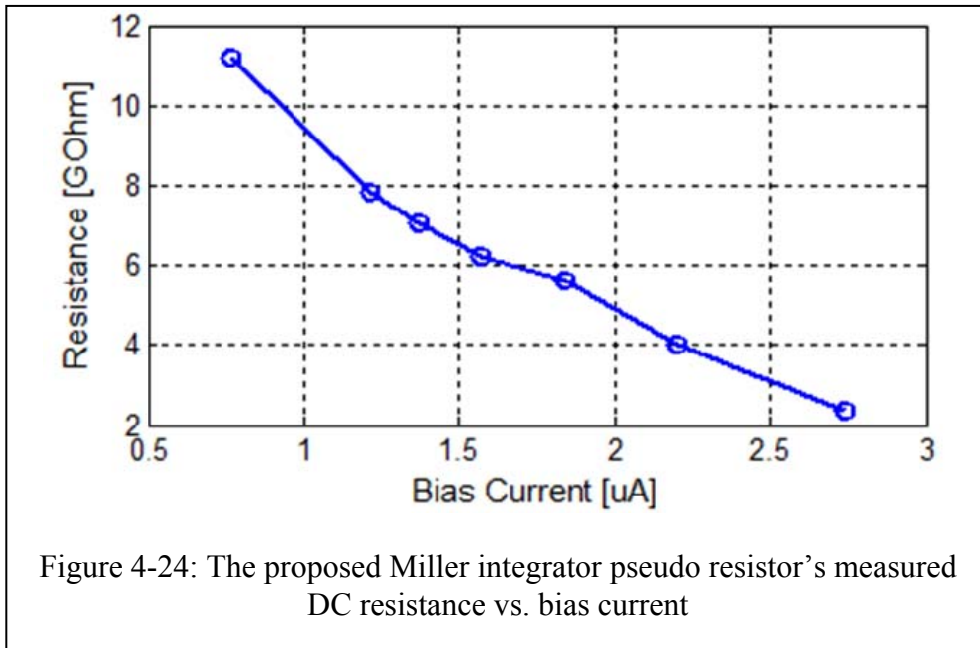
topology: *i)* for negative source-drain voltages, the device conducts considerable current and enters the low resistivity region, and *ii)* for source drain voltages larger than 0.5V the source-bulk p-

n junction starts to conduct current and therefore the resistance of the device drops. Both of these characteristics limit the range of high resistivity region and to resolve these issues two back-to-back bulk-drain connected PMOS devices can be used. The resistance of two back-to-back bulk-drain connected PMOS devices is tunable in a wide range and can have a large DC resistance in GΩ range. As the frequency increases the impedance of the device drops rapidly due to the stray capacitances of the device. Therefore these devices can only be used in low frequency applications.

The capacitor of the continuous time Miller integrator employed in NA_V1, is implemented with a 16pF double-polysilicon, linear, on-chip capacitor. According to 4-7,



to have a high pass cut off frequency of 500Hz, the unity frequency of the integrator should be 5Hz ($R_{INTEG} = \frac{1}{2\pi \times f_{UNITY} \times C_{INTEG}}$); and with a 16pF capacitance, the integrator's resistance should be about 2GΩ. Such high value resistor is implemented with the proposed pseudo resistor shown in figure 4-23. The Miller integrator's pseudo resistor is implemented as a cascaded version of the adjustable ultra-high value CMOS



pseudo resistor introduced in [4.33]. The first stage is biased by the gate-source voltage drop of the NMOS transistor; and this voltage is adjustable by the bias current. The next two stages are biased by a smaller source-gate voltage and consequently there is a

monotonic increase in their effective resistance. The bias current of the Miller integrator is generated by a dedicated global V_{th} -referenced current source. The measured DC resistance of the proposed Miller integrator's pseudo resistor versus the bias current is shown in figure 4-24. Figure 4-25 depicts the proposed pseudo resistor's measured I-V

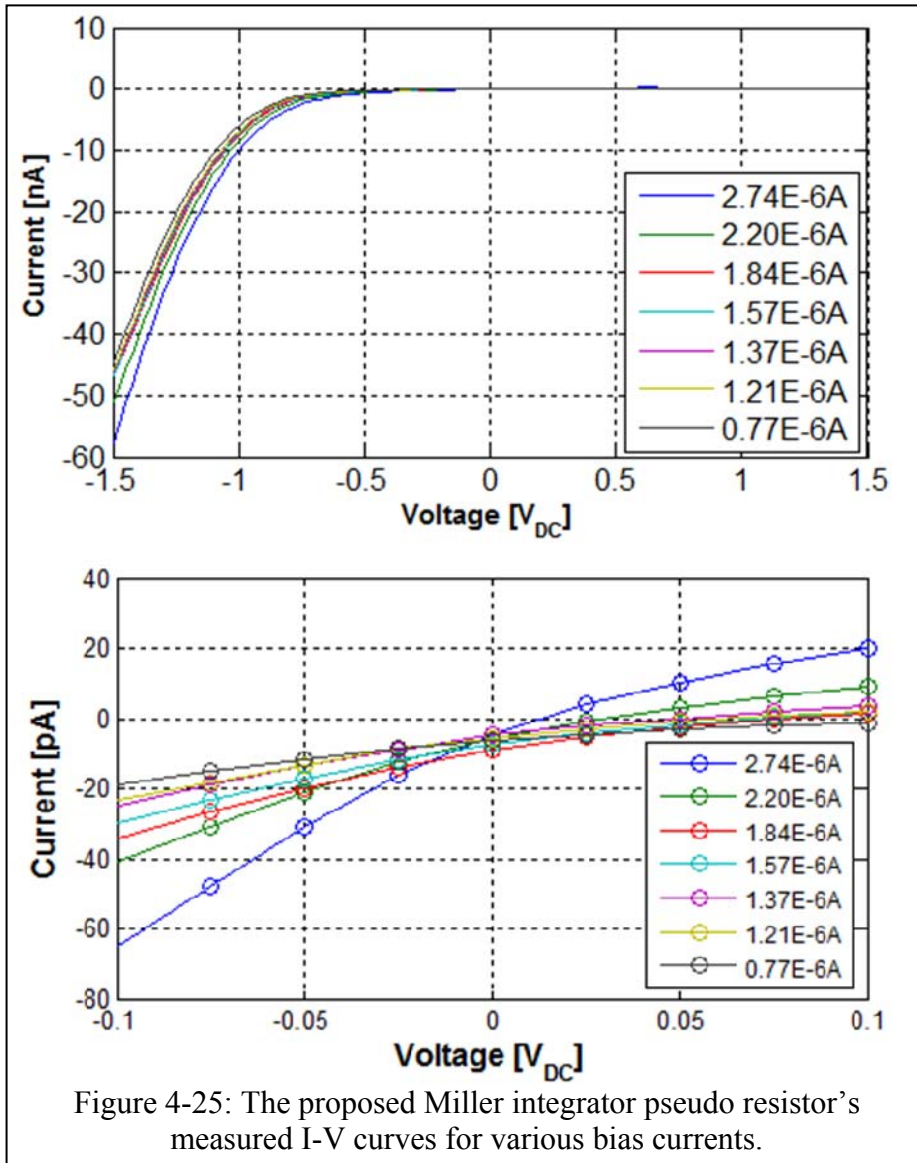


Figure 4-25: The proposed Miller integrator pseudo resistor's measured I-V curves for various bias currents.

curves for various bias currents.

The measured frequency response of the Miller integrator is shown in figure 4-26 and has a unity-gain frequency of about 3.1Hz. The gain stage of the Miller integrator is

implemented with a two-stage lead compensated OTA; the main advantage of the two-stage topology is its inherent large DC gain which is needed for the Miller integrator. The larger the DC gain the lower the flat corner frequency of the Miller integrator. The two-stage, lead-compensated OTA of the Miller integrator has a simulated phase margin of

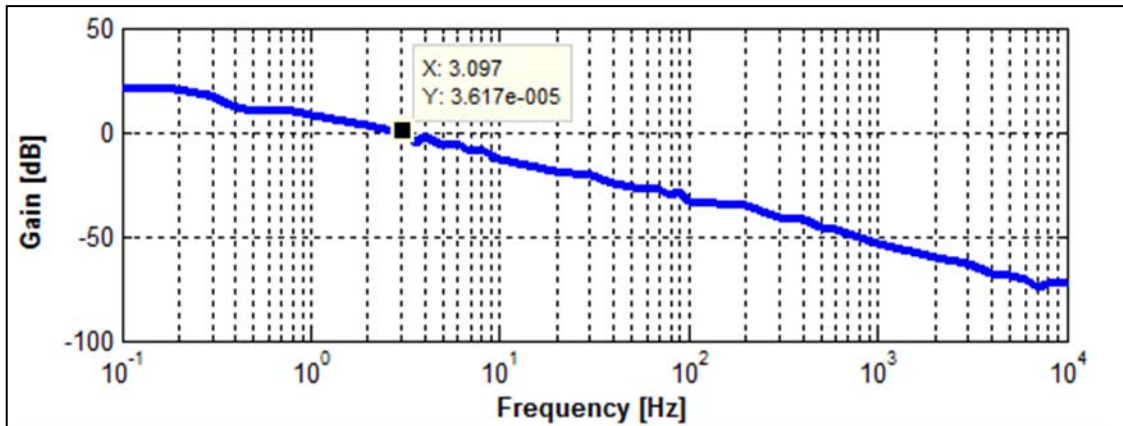
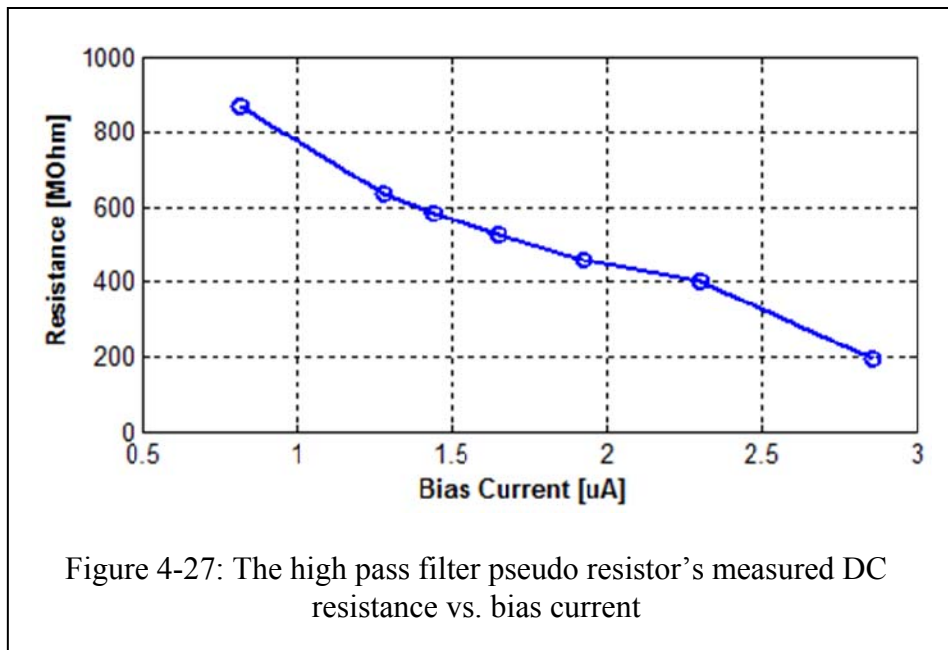


Figure 4-26: The Miller integrator's measured frequency response; the unity gain corner frequency is located at 3.1Hz

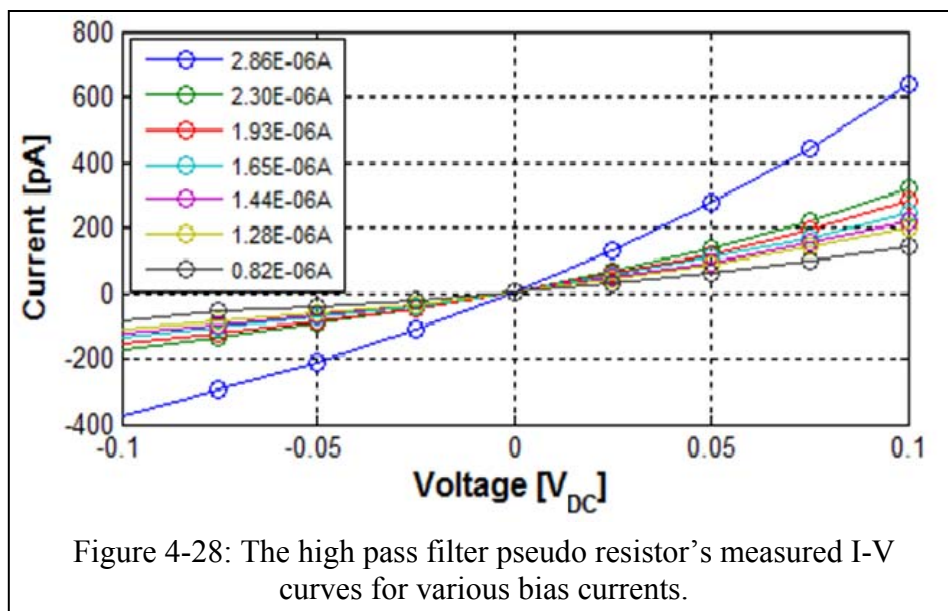
65°, a power consumption of 4.5 μ W, an open-loop gain of 84dB, and an input referred noise of 5 μ V_{rms}.

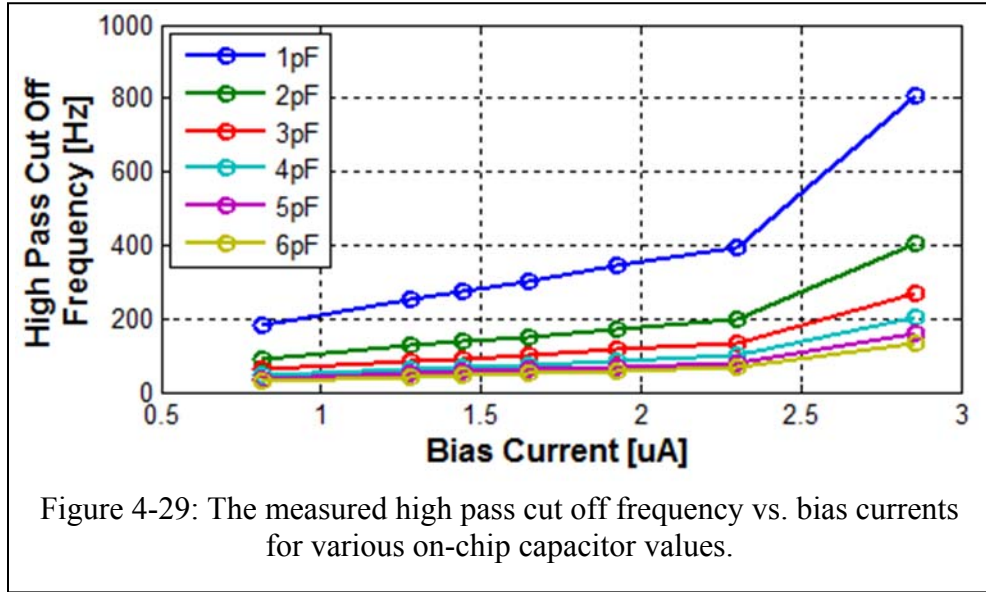
4.3.2.2.3. The High Pass Filter

As shown in NA_V1's circuit diagram (figure 4-18), the active-low-frequency-suppression core is followed by a RC high pass filter; the function of this high pass filter is to set another high pass cut off frequency at 500Hz to attenuate the low frequency noise components by 40dB/dec. The capacitor is implemented as an array of six 1pF double-polysilicon capacitor. The resistor is implemented by an adjustable ultra-high value CMOS pseudo resistor [4.33]. The high pass filter resistor is adjustable through its bias current. The bias current of the high pass filter is generated by a dedicated global



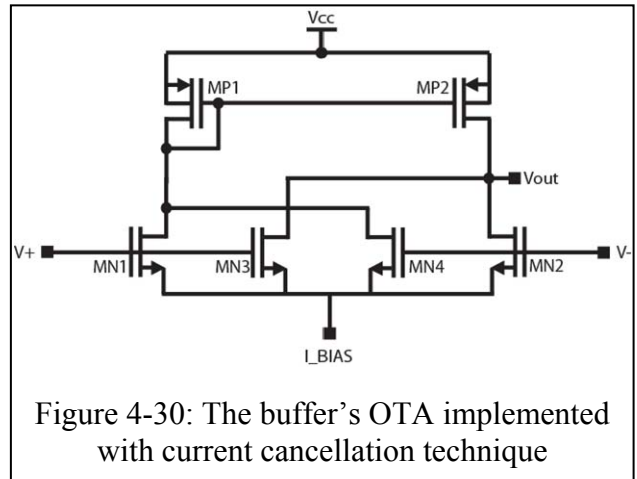
V_{th} -referenced current source. The measured DC resistance of the high pass filter pseudo resistor versus the bias current is shown in figure 4-27. Figure 4-28 depicts the high pass filter pseudo resistor's measured I-V curves for various bias currents. The measured high pass cutoff frequency of the neural amplifier versus the bias current for various values of the high pass filter capacitor is shown in figure 4-29. As can be seen the high pass cutoff frequency can be set from 30Hz to 810Hz.





4.3.2.2.4. The Buffer/Low-Pass-Filter

The final stage of the neural amplifier is the buffer; the same block also functions as the low pass filter which sets the second pole at the neural amplifier's output. By having a second low pass cut-off frequency at 10KHz, the attenuation for $f > 10KHz$ drops



with 40dB/dec which prevents aliasing in subsequent sampling stages. The buffer/LPF block consists of a single-stage OTA with input differential pair connected in unity gain configuration. The low pass cut off frequency is located at $\frac{1}{1 + \frac{sC_L}{g_{m,buf}}}$ as predicted by 4-8.

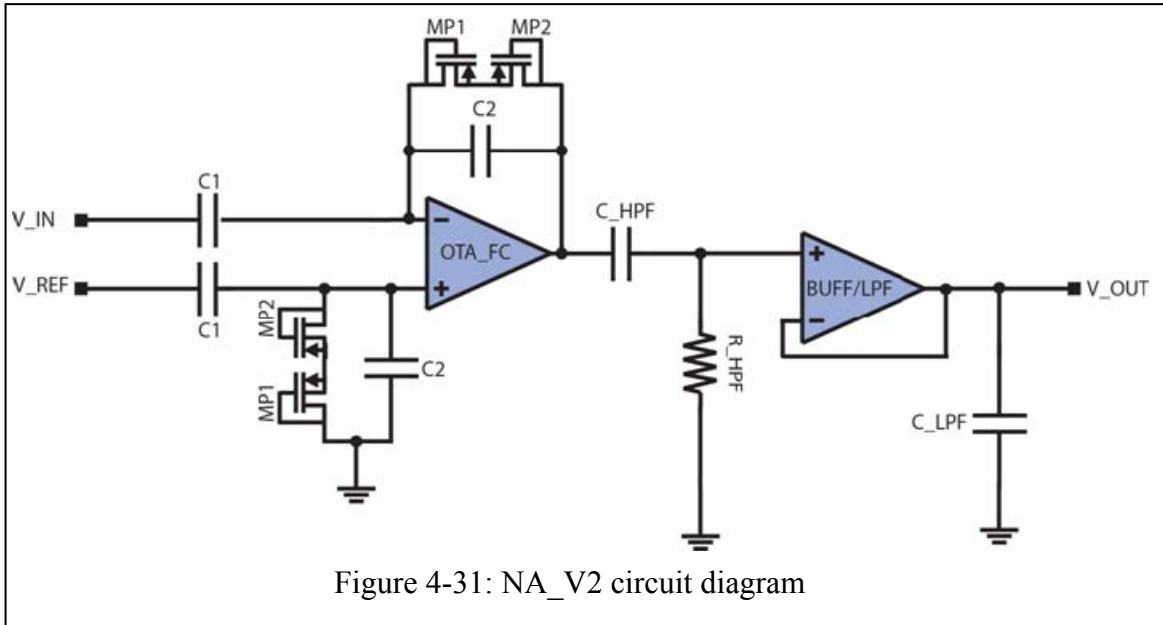
To set the f_{lp} at 10KHz, the transconductance of the buffer's OTA is reduced using current cancellation technique [4.35] as shown in figure 4-30. The low pass cut off

frequency of the buffer is also adjustable through a laser-trimmable array of four 1pF double-polysilicon capacitors.

Other than inserting a second low pass pole at the output of the amplifier, the main advantage of the last block is to isolate the active-low-frequency-suppression core from the load of the time-division-multiplexer and IO pads; furthermore the impacts of the multiplexer's switching noise is decoupled from the amplifier's sensitive core by the same buffer. The noise performance of this block does not affect the overall neural amplifier input referred noise voltage; the power consumption of the buffer/LPF is adjustable through a dedicated global V_{th} -referenced current source and is nominally set at $1.5\mu W$.

4.3.2.3. NA_V2

The circuit diagram of the NA_V2 is shown in figure 4-31; essentially NA_V2 is the same as the NA_V1 with the difference that the active-low-frequency-suppression core is eliminated. The amplification of the neural action potential is done by the folded cascade OTA in capacitive feedback configuration: OTA_{FC} , C_1 , C_2 , MP_1 and MP_2 . OTA_{FC} is a low noise, low power folded-cascode operational-transconductance-amplifier (OTA) and is the same as the folded cascade OTA of the NA_V1. The passband gain of the overall neural amplifier is set by $(-C_1/C_2)$. C_1 is directly connected to the implanted electrodes and is composed of an array of 120fF double-polysilicon capacitors; C_2 , the feedback capacitor, is a single element of the capacitor array. MP_1 and MP_2 are MOS-Bipolar pseudo resistors biasing the negative (-) terminal of the folded-cascode OTA. The V_{REF} , in figure 4-31, is either connected to the ASIC ground or to the reference channel;



either way, the series combination of MP_1 - MP_2 and the capacitor C_2 are added merely to equalize the load on the negative and positive terminals. In other words V_{REF} biases the positive (+) terminal of the folded-cascode OTA

The high pass cut off frequency created by the MOS-Bipolar elements (MP_1 and MP_2) and the feedback capacitor (C_2) is sub-mHz and will not affect the band pass characteristic of the overall neural amplifier as in the case of NA_V1. In NA_V1, the low pass cut-off frequency is created by the active-low-frequency-suppression core, but in NA_V2, the high pass filter following the amplification stage is responsible to set the high pass cut off frequency at 500Hz; therefore the low-frequency, large noise components are attenuated by 20dB/dec instead of 40dB/dec as in NA_V1. The high pass filter of NA_V2 is the same as that of NA_V1. The buffer stage is needed to drive the large capacitive load of wires and the TDM multiplexer. The buffer/LPF also isolates the sensitive amplification stage from the load of the multiplexer and IO pads; it also desensitizes the amplification stage from the TDM multiplexer's switching noise. This

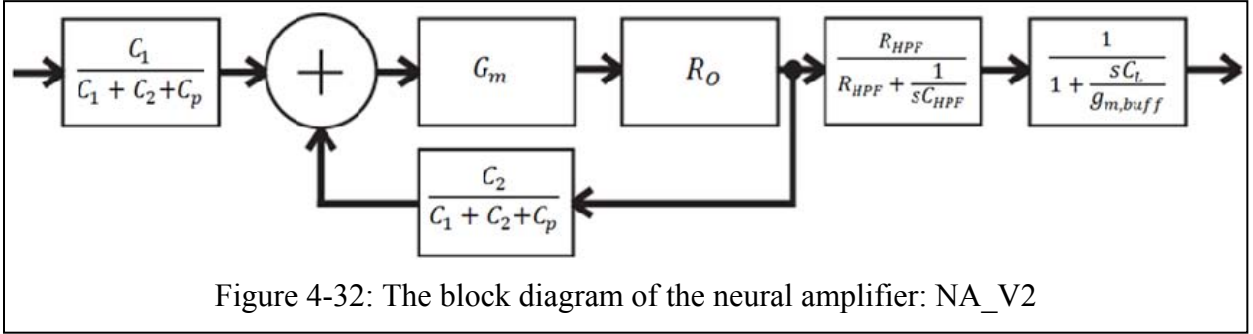


Figure 4-32: The block diagram of the neural amplifier: NA_V2

block is the same as NA_V1's buffer/LPF. The noise contribution of the last two blocks is negligible due to the large gain of the amplification stage.

The block diagram of the neural amplifier, NA_V2, is shown in figure 4-32. The noise of the overall neural amplifier is determined by the input referred noise of the folded cascode OTA and multiplied by the factor $\frac{C_1 + C_2 + C_p}{C_1}$. To lower the input referred noise of the overall neural amplifier the factor, $\frac{C_1 + C_2 + C_p}{C_1}$, should be very close to unity by choosing the C_1 and C_2 according to size of the input differential pair transistors. The last two blocks of the NA_V2, are high pass filter and low pass filter respectively; the pole of the high pass filter defines the high pass cut-off frequency of the overall amplifier; and the buffer/LPF block adds a second pole at 10KHz to further reduce aliasing in subsequent sampling stages.

From figure 4-32, the transfer function of the NA_V1 can be written as:

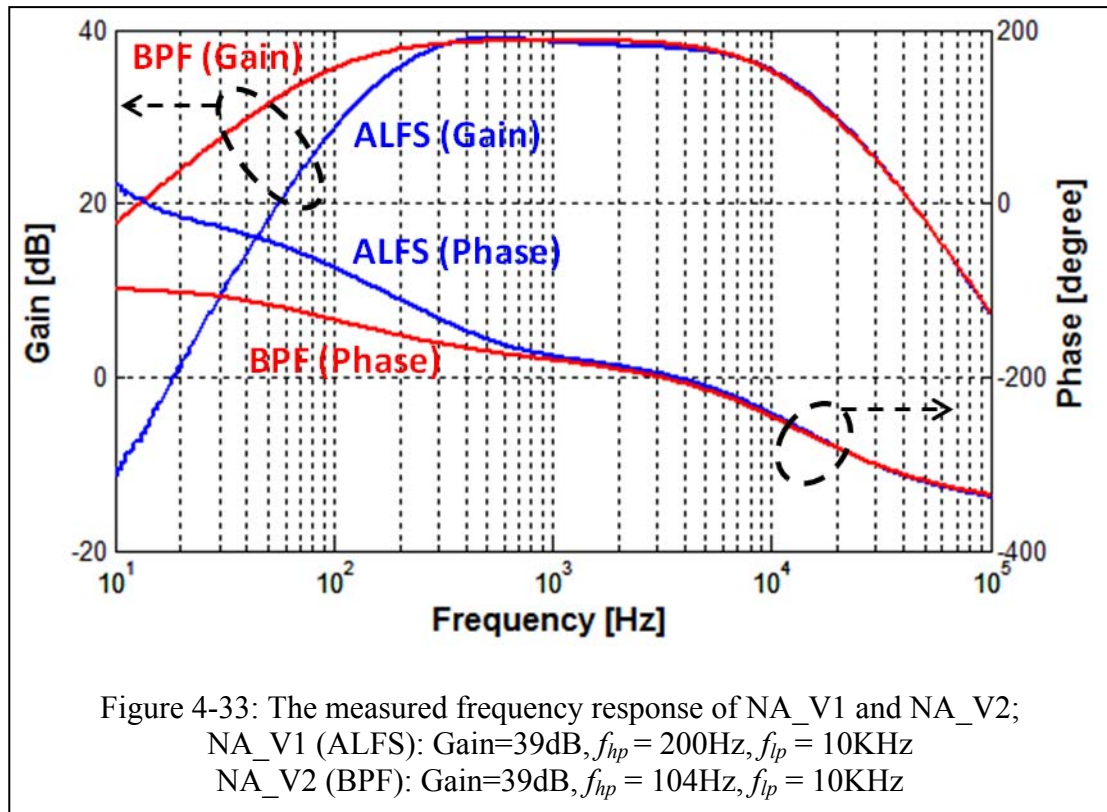
$$H(s) = \frac{-\frac{C_1}{C_2}}{1 + \frac{s}{BW}} \times \frac{R_{HPF}}{R_{HPF} + \frac{1}{sC_{HPF}}} \times \frac{1}{1 + \frac{sC_L}{g_{m,buffer}}} \quad (4 - 32)$$

In 4-32, $\frac{BW}{2\pi}$ is the low pass cut off frequency of the gain stage folded cascode OTA; R_{HPF} is the on-chip adjustable high value pseudo resistor of the high pass filter and C_{HPF} is the double-polysilicon, linear, on-chip capacitor of the high pass filter; C_L is the

adjustable load of the buffer stage; and $g_{m,buff}$ is the transconductance of the buffer/LPF.

4.3.2.4. Results and Discussions

The frequency response of NA_V1 (ALFS) and NA_V2 (BPF) are compared in figure 4-33. As can be seen NA_V1 implemented with active-low-frequency-suppression (ALFS) has a 40dB/dec slope for low frequency signals whereas the NA_V2 implemented as a bandpass filter has a 20dB/dec slope for low frequency signals.



The high pass cut off frequency of the active low frequency suppression core can be adjusted through the bias current of the Miller integrator's adjustable ultra-high value CMOS pseudo resistor. Figure 4-34 depicts the measured frequency response of the active-low-frequency-suppression core (ALFS) as the Miller integrator resistance is

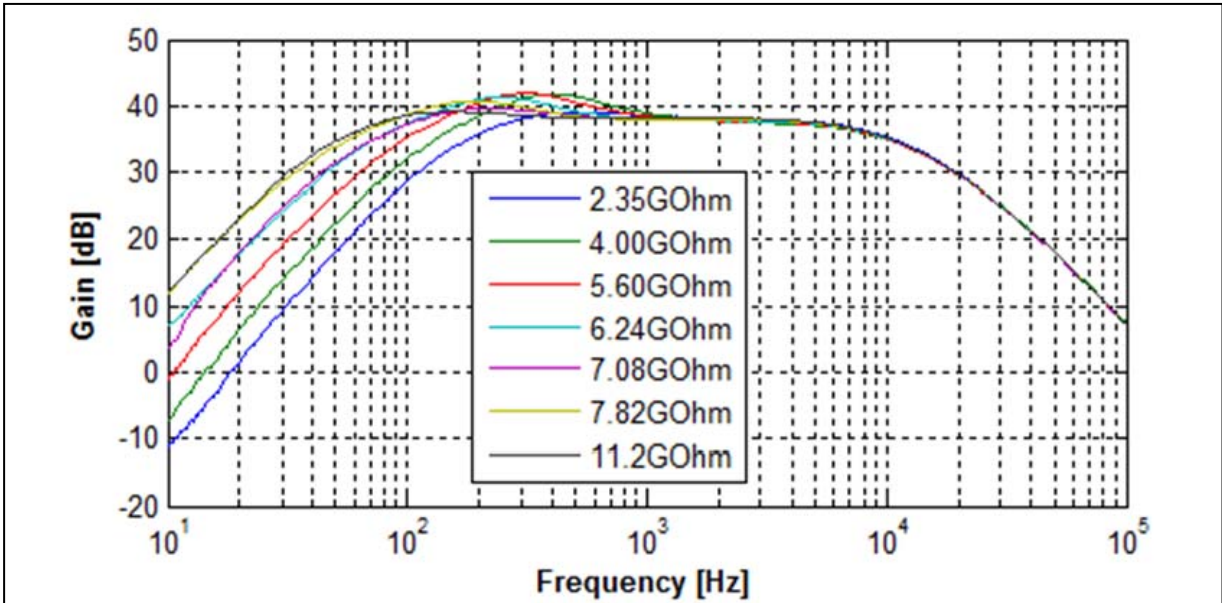


Figure 4-34: The measured frequency response of the active-low frequency-suppression (ALFS) core versus various values of the Miller integrator resistor; the high pass cut off frequency of the ALFS can be set from 60.26Hz to 208.9Hz by adjusting the resistor value.

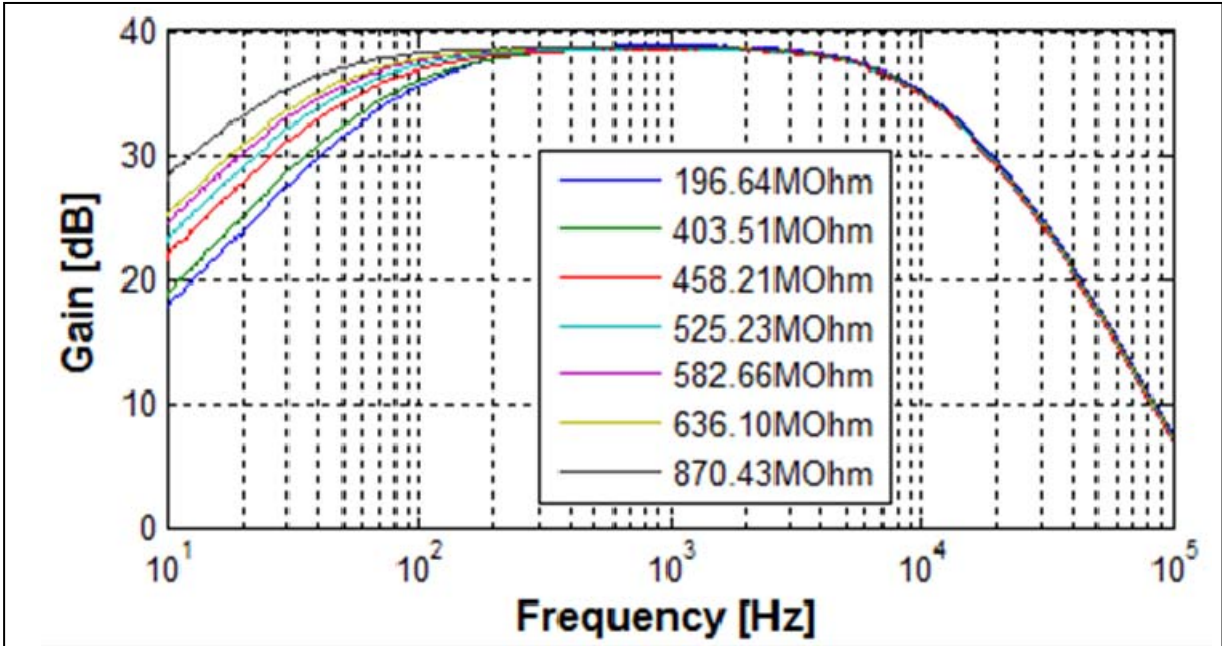


Figure 4-35: The measured frequency response of the bandpass neural amplifier versus various values of the HPF resistor; the high pass cut off frequency of the bandpass neural amplifier can be set from 34Hz to 104Hz by adjusting the resistor value.

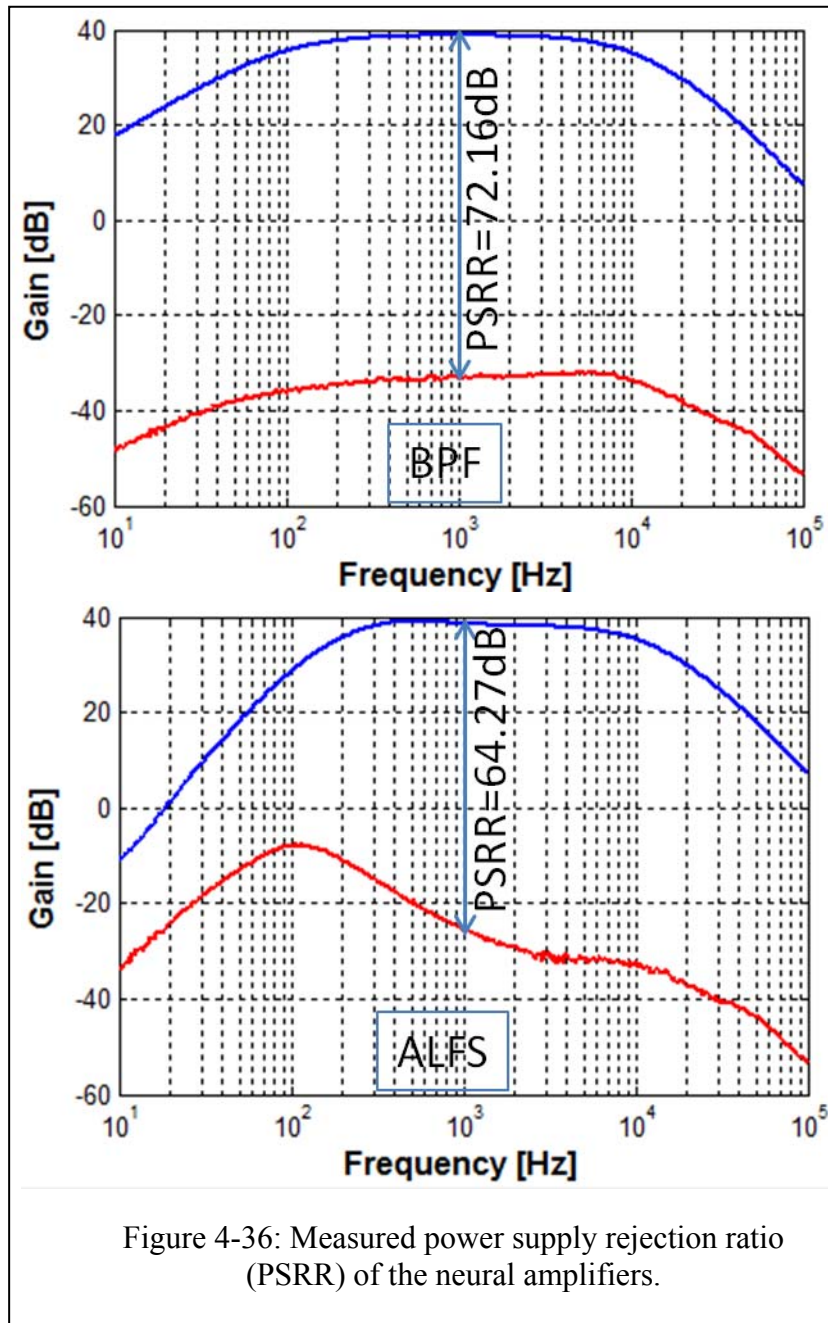
swept from 2.35GΩ to 11.2GΩ. The larger the Miller integrator’s resistance the smaller its time constant and consequently the high pass cut off frequency of the active-low-

frequency-suppression core shifts to lower frequencies. As shown in figure 4-34 the high pass cut off frequency of the ALFS can be adjusted from 60.26Hz to 208.9Hz through changing the Miller integrator resistance. Also by laser cutting the Miller integrator's on-chip capacitors, its upper high pass cut off frequency can be stretched from 208.9Hz to 840Hz in 5 discrete steps.

Figure 4-35 shows the measured frequency response of the band pass neural amplifier (NA_V2). In this graph the ultra high value resistor of the high pass filter block is swept from 196.64M Ω to 870.43M Ω and consequently the high pass cut off frequency of the neural amplifier is adjusted from 34Hz to 104Hz. In this measurement all the capacitors (5 \times 1pF) of the high pass filter are in the signal path. To change the high pass cut off frequency of the BPF neural amplifier further, the on-chip capacitor of the high pass filter can be laser trimmed; therefore the upper high pass cut off frequency can be set up to 520Hz in 5 discrete steps.

Power supply rejection ratio of the neural amplifiers (ALFS and BPF) is measured in figure 4-36. The BPF neural amplifier (NA_V2) has a measured PSRR of 72.16dB at 1KHz and the ALFS neural amplifier (NA_V1) has a measured PSRR of 64.27dB at 1KHz. In these measurements, the amplifier output frequency response with respect to the input signal applied to the power supply is measured.

The common mode rejection ratio (CMRR) of the bands pass neural amplifier (NA_V2) is measured in figure 4-37; in this measurement the BPF neural amplifier's V_{REF} signal (figure 4-31) is fed with the same signal as the input (V_{IN} in figure 4-31) and the frequency is swept from 10Hz to 100KHz. As can be seen the neural amplifier has a CMRR of 52.22dB at 1KHz. The CMRR of the active-low-frequency-suppression core

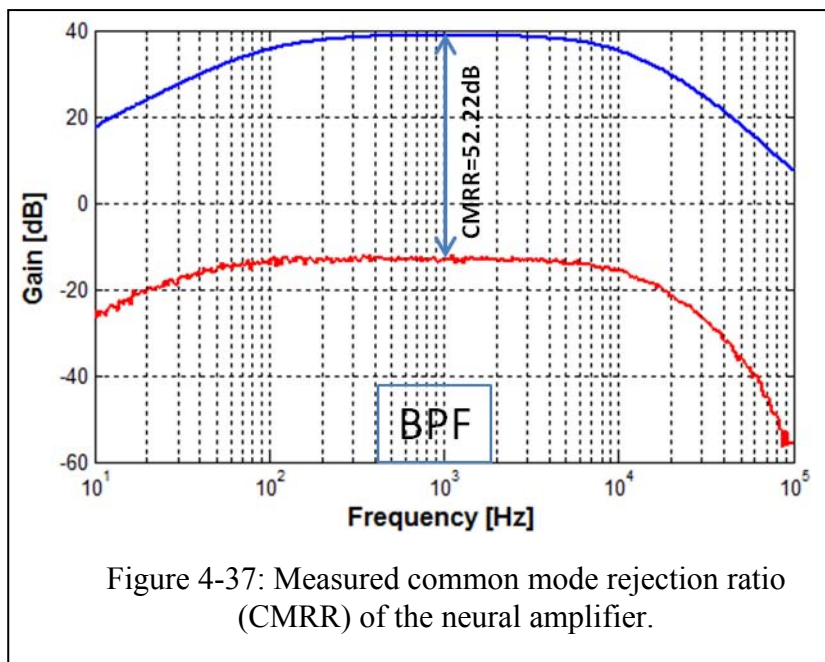


(ALFS) cannot be measured since the (-) terminal of its gain OTA is fed by the Miller integrator's output.

The total harmonic distortion (THD) of the neural amplifiers is measured in figure 4-38. For input amplitudes less than $1mV_{pp}$ the measured THD is less than 1% for both neural amplifiers (ALFS and BPF). As can be seen in figure 4-38, as the input amplitude

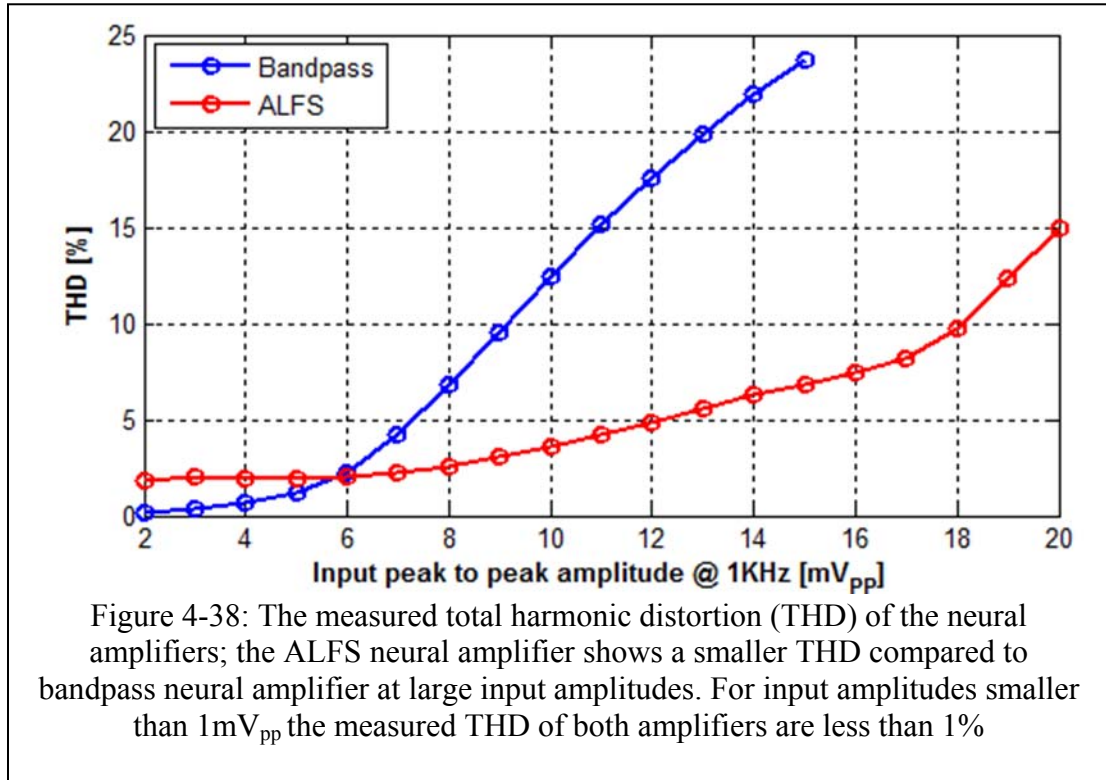
grows larger than $6mV_{pp}$ the neural amplifier implemented with active-low-frequency-suppression core (NA_V1) has a smaller THD compared to the bandpass neural amplifier (NA_V2). However this parameters is not important for neural amplifiers intended to record only the action potentials as the input neural spikes are small in amplitude ($<500\mu V_{pp}$).

An important factor in neural amplifiers is the recovery time from the muscle movement artifacts. In in-vivo experiments involving awake and mobile subjects, the muscle movement of the test subject induces large transient voltages in the signal path. These transient noise voltages can be as large as $\pm 1V$ which will destabilize the neural



amplifier. Depending on the biasing mechanism, it might take the neural amplifier up to 1s to recover from the muscle movement artifacts; during the 1s idle time all the input neural spikes are missed and therefore this condition is not acceptable in reliable neural recordings. Figure 4-39 shows the neural amplifiers responses to muscle movement artifacts; in this measurement the input is a 1KHz, $2mV_{pp}$ signal which is applied to both

neural amplifiers (ALFS and BPF); the DC offset of the input is changed abruptly by



+150mV at 166ms. As can be seen in figure 4-39, the neural amplifier implemented as a band pass filter takes about 600ms to recover from this mimicked muscle movement artifact whereas the neural amplifier implemented with active-low-frequency-suppression recovers from the artifact almost instantly. The ALFS neural amplifier has a second feedback path provided by the Miller integrator which follows the disturbance voltage at the output and instantly biases the inputs of the neural amplifier. Figure 4-40 shows the idle time of both neural amplifiers (ALFS and BPF) for various movement artifact voltage levels. For all the induced disturbance voltages the ALFS neural amplifier recovers almost instantly; the BPF neural amplifier recovers instantly from the muscle movement artifacts with negative polarity however the idle time for muscle movement artifacts with positive polarity can be as long as 960ms.

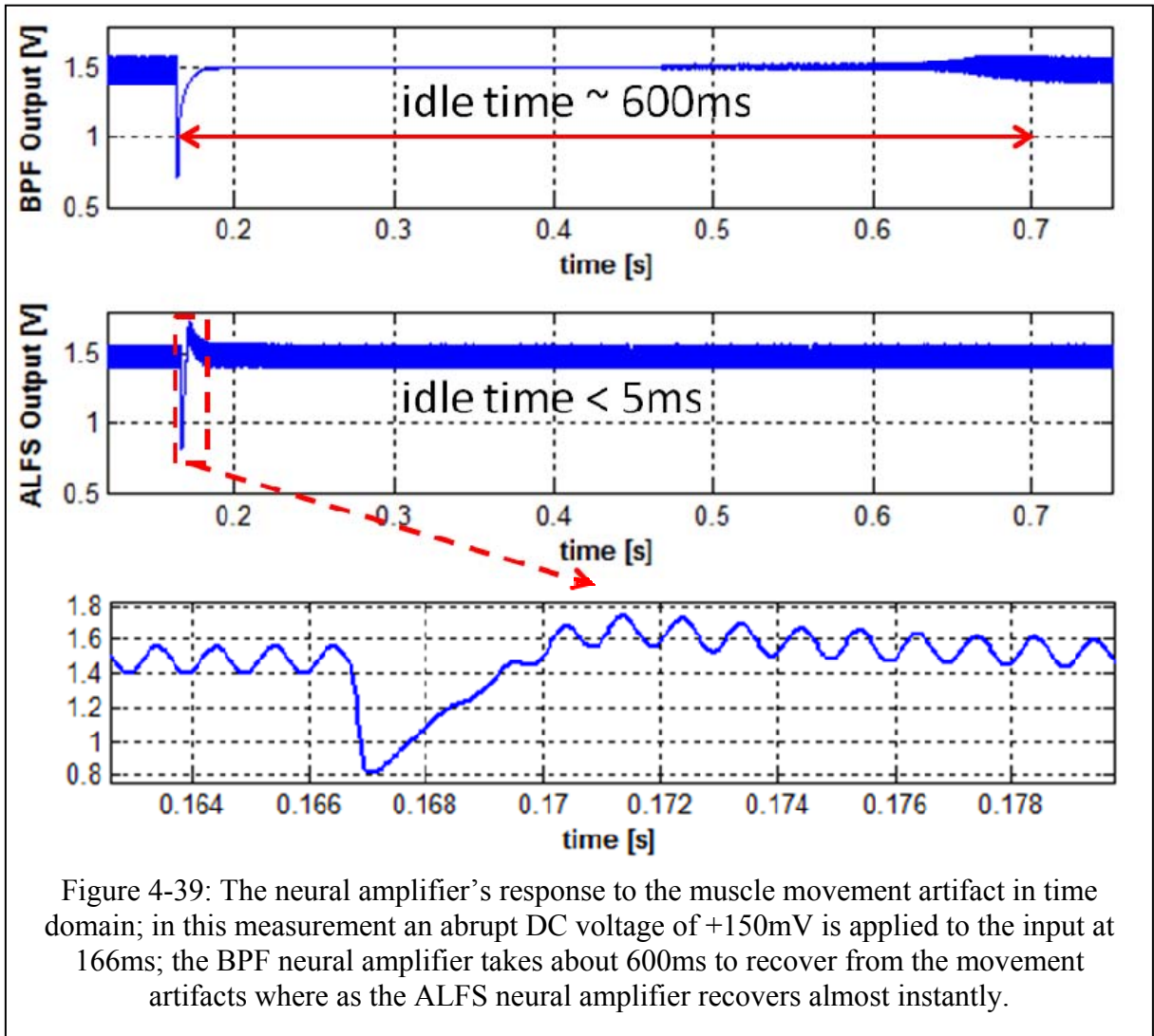
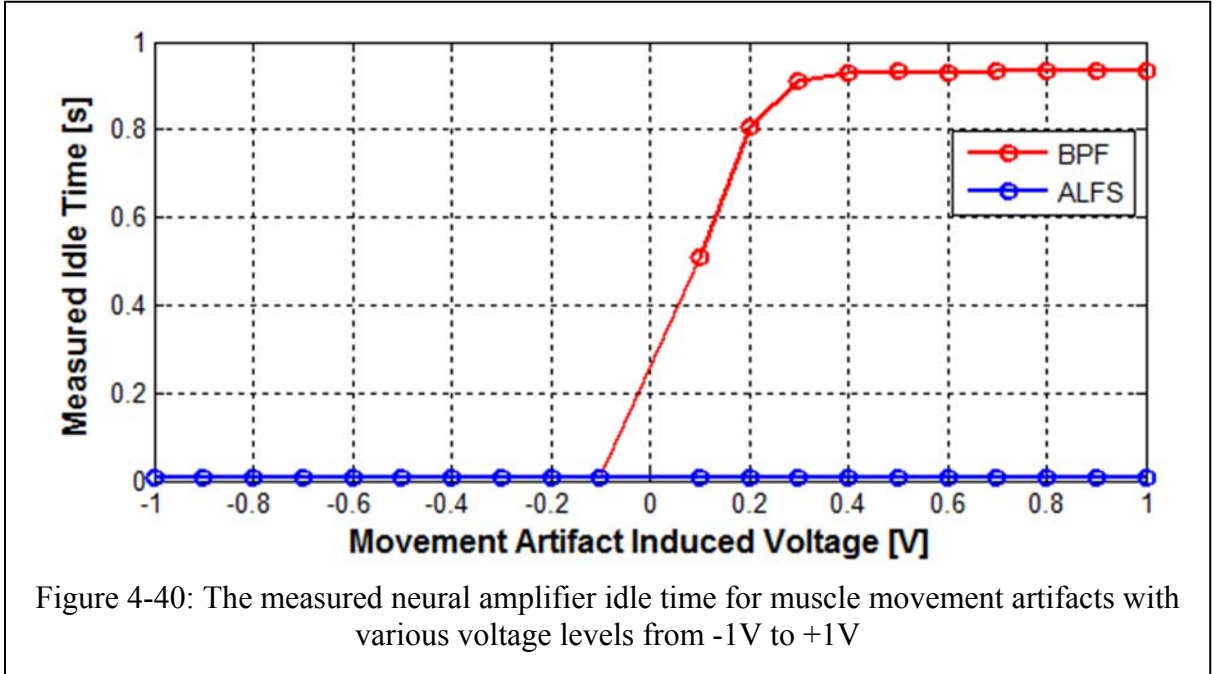


Figure 4-39: The neural amplifier's response to the muscle movement artifact in time domain; in this measurement an abrupt DC voltage of +150mV is applied to the input at 166ms; the BPF neural amplifier takes about 600ms to recover from the movement artifacts where as the ALFS neural amplifier recovers almost instantly.

To calculate the noise performance of neural amplifiers the output of the grounded channels are recorded in time domain using a USB-based data acquisition card (DAQ) for 10s with a data sampling rate of 100kSps. Therefore the noise performance is calculated in the bandwidth of 100mHz to 50KHz. Figure 4-41 compares the frequency spectrum of the band pass amplifier and active-low-frequency-suppression core. In this recording the bandpass amplifier and active-low-frequency-suppression core have an input referred voltage noise of $2.157\mu\text{V}_{\text{rms}}$ and $4.605\mu\text{V}_{\text{rms}}$ respectively. As can be seen in figure 4-41, the bandpass neural amplifier has smaller high frequency noise components



compared to active-low-frequency-suppression core. Also suppression of low frequency noise components of the ALFS can be observed in its power spectrum.

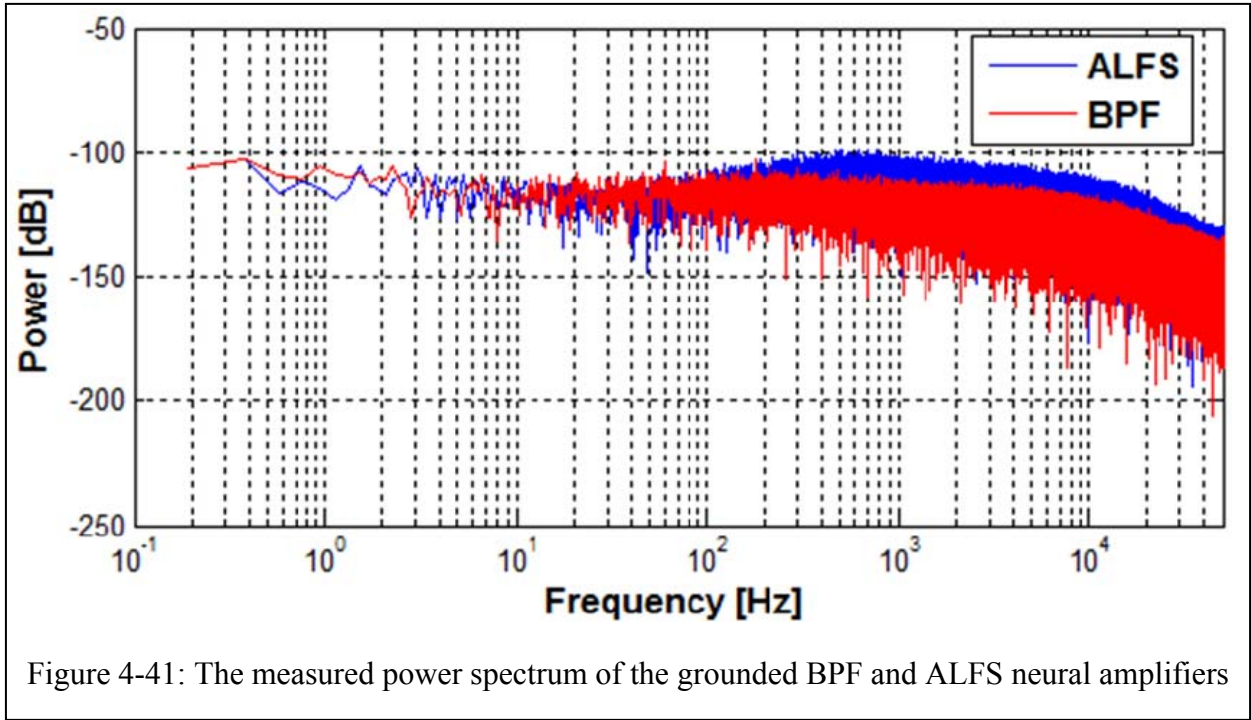
The power consumption and noise performance of the proposed neural amplifier is adjustable through a V_{th} -referenced current source. Figure 4-42 depicts the input referred voltage noise of the active-low-frequency-suppression and bandpass neural amplifiers versus signal path power consumption. As can be seen the noise performance of the bandpass neural amplifier is superior to the active-low-frequency-suppression amplifier. This is due to the Miller integrator of the ALFS amplifier which its noise is coupled to the (+) input of the neural amplifier's OTA.

A figure of merit (FoM) for comparing neural amplifiers is the Noise-Efficiency

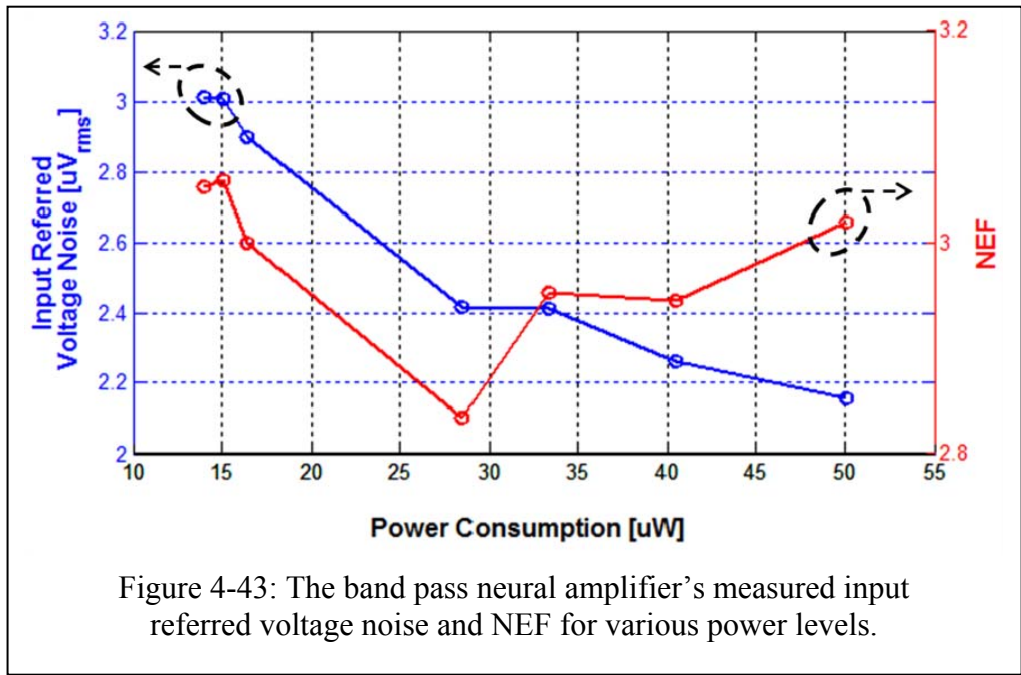
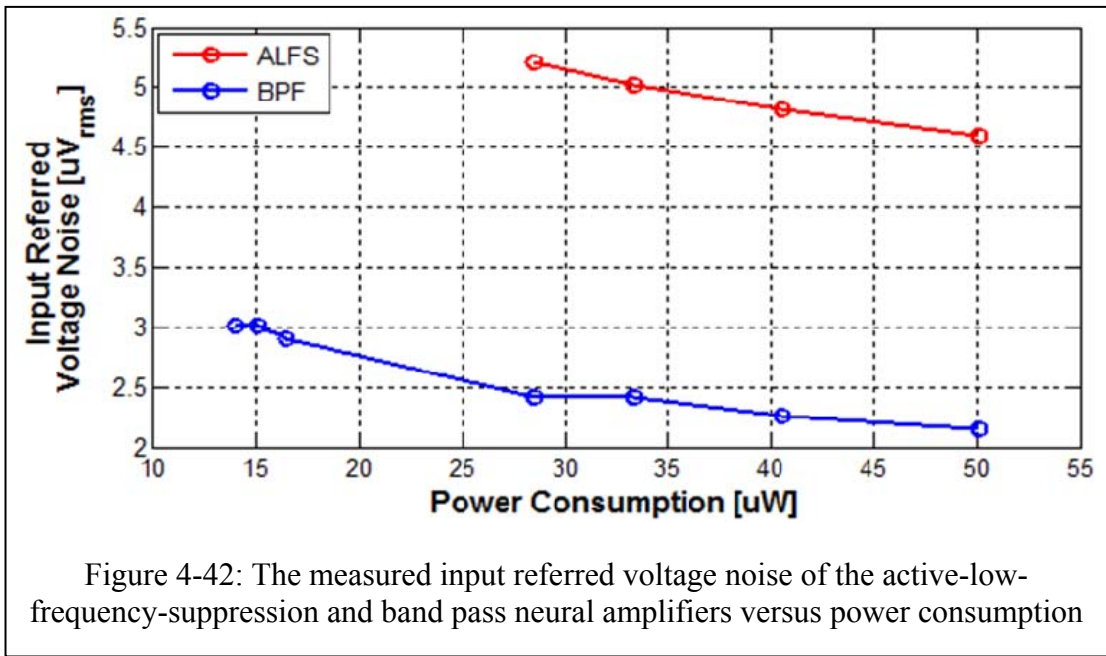
Factor (NEF) introduced in [4.32]:
$$NEF = V_{ni,rms} \sqrt{\frac{2I_{total}}{\pi \times U_T \times 4kT \times BW}}$$

In NEF equation, $V_{ni,rms}$ is the input-referred noise voltage; I_{total} is the total amplifier's signal path supply current; and BW is the amplifier bandwidth. An amplifier

composed of a noise-less single transistor has an NEF of one; all the amplifiers have their NEFs greater than one. The neural amplifier proposed in this work has a minimum NEF



of 2.834 for a signal path power consumption of $28.51\mu\text{W}$. The NEF theoretical limit for an OTA using input differential pair is 2, and the achieved NEF of 2.834 is very close to its minimum theoretical value of 2. Figure 4-43 shows the band pass neural amplifier's measured input referred voltage noise and NEF for various power levels of the signal path. Finally the NEFs of state of the art neural amplifiers are compared with the proposed neural amplifier in figure 4-44.



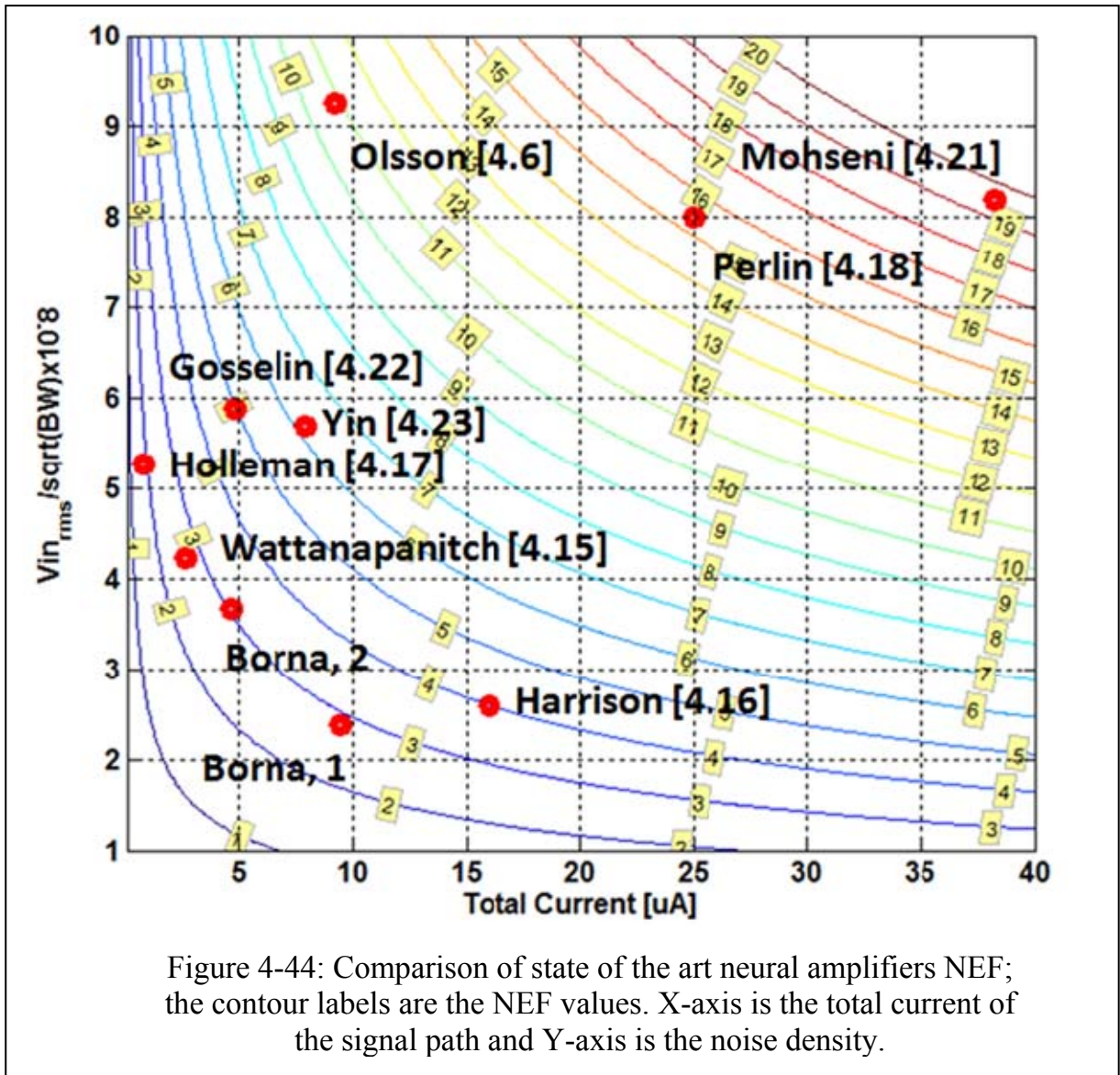


Figure 4-44: Comparison of state of the art neural amplifiers NEF; the contour labels are the NEF values. X-axis is the total current of the signal path and Y-axis is the noise density.

4.3.3. The V_{th} -Referenced Current Sources

In the proposed ASIC, the front-end analog blocks, are biased by local-bias-voltage, global-reference-current scheme; in this scheme, all the blocks have individual bias voltage generators; these local voltage generators are biased by a global current source which its current is distributed across the chip.

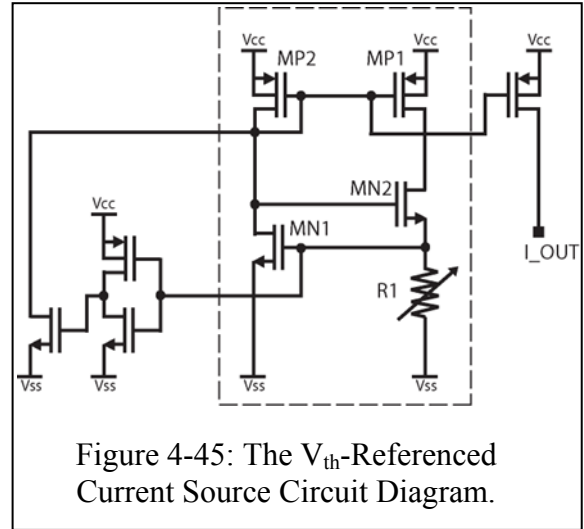
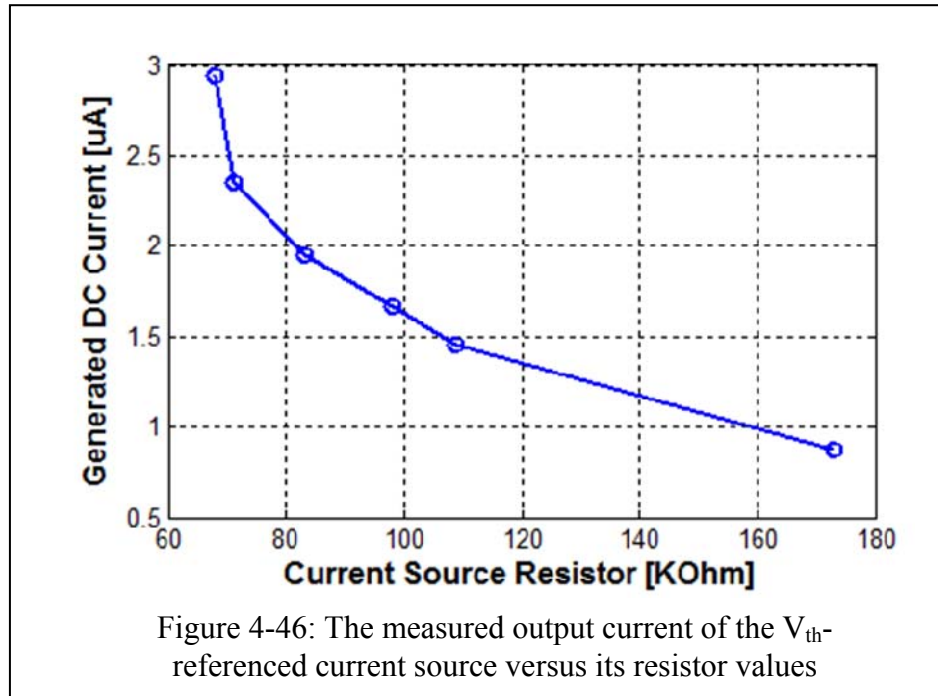


Figure 4-45: The V_{th} -Referenced Current Source Circuit Diagram.

Specifically, there are four independent current sources: *i)* CS_OTAs: the reference current for the OTA's of the amplification stage and the Miller integrator, *ii)* CS_HVR_INTEG: this current source generates the reference current for the ultra-high value resistors of the Miller integrators, *iii)* CS_HVR_HPF: the reference current for the high value resistor of the high pass filter, and *iv)* CS_BUFF: generates the reference current for the buffer/LPF stage of the neural amplifiers.

These identical current sources are adjustable using a laser trimmable resistor implemented with high resistance electrode (POLY2) layer. The circuit diagram of the current source is shown in figure 4-45. This is a threshold-referenced current source [4.34]. The current in the adjustable resistor (R_1), is determined by the voltage drop across the gate-source terminals of the MN_1 :

$$I_{R_1} = \frac{V_{GS1}}{R_1} = \frac{V_{th1} + \sqrt{\frac{2 \times I_{R_1}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}}}{R_1} \quad (4 - 33)$$



The currents in the two branches of the V_{th} -referenced current source are equalized by the two active PMOS current mirrors: MP_1 and MP_2 . To avoid process and temperature variations (PTV) all the active devices operate in saturation region; furthermore the resistor current, I_{R1} , is made close to $\frac{V_{th1}}{R_1}$, by increasing $(\frac{W}{L})_1$ while still operating the MN_1 in strong-inversion region.

The transistor MN_2 is added to increase the impedance of the reference current path; by using MN_2 , essentially the current in the R_1 is desensitized from the source-drain voltage fluctuations of the active PMOS current mirrors. The startup circuitry is composed of an inverter and a pull down NMOS device. At low current levels, the voltage drop across the resistor R_1 , is low enough to turn on the PMOS of the start-up inverter; consequently the pull down NMOS device increases the source-gate voltage of the PMOS active current mirrors and therefore increases their drain current; by increasing

the current in the resistor, R_1 , the NMOS of the startup inverter turns on and disconnects the start up circuitry from the core.

The PMOS current mirror to the right of the circuit distributes the reference current to the front-end building blocks. All the current sources are designed to have a nominal core current of $4\mu\text{A}$ and the distributed current (I_{OUT}) is scaled down to $1\mu\text{A}$. The nominal power consumption of the V_{th} -Referenced Current Source is $24\mu\text{W}$. To reduce the noise on the generated reference currents, the supply voltage is decoupled locally by a 50pF , double-polysilicon capacitor. Figure 4-46 shows the measured DC currents of the proposed V_{th} -referenced current source versus its resistor values; the resistor can be laser trimmed from $67\text{K}\Omega$ to $175\text{K}\Omega$ resulting in an adjustable DC current from $3\mu\text{A}$ to $0.87\mu\text{A}$.

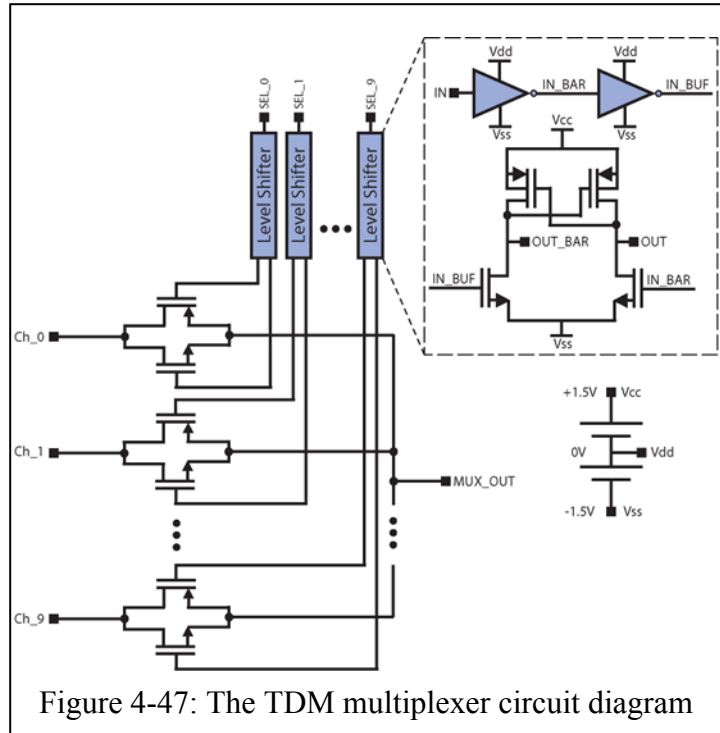
4.4. Sampling Circuitry

Sampling circuitries consist of TDM multiplexer and the unity-gain wide bandwidth buffer. The TDM multiplexer time-division-multiplexes the channels signals into one continuous stream of analog data; the wideband buffer drives the RF blocks and provides the TDM signal with the offset voltage needed to modulate the VCO's tuning input.

4.4.1. The Analog Time Dividing Multiplexer

This is a 10-to-1 analog multiplexer, shown in figure 4-47, controlled by ten select-bits; the DigiSampler operates on a 1.5V_{DC} supply voltage whereas the front-end circuitry operates on a 3V supply. The ten 1.5V select-bits are converted to 3V digital

signals by ten level shifters shown in the same figure. The TDM multiplexer has CMOS pass gates instead of NMOS pass gates; the advantage of CMOS pass gates is small effective on-resistance and fast settling time. Analog TDM multiplexers which have 2^n inputs can be implemented such that the select lines do cross neither the inputs



nor the output; in this approach every input is connected to output through n -NMOS transistors; the advantage is the reduction in clock feedthrough. The disadvantage however is two folded; by having series-connected NMOS pass transistors in the signal path (compared to the case with only one pass transistor), extra poles are added to the signal path, leading to ringing at the MUX's output. Ringing can be problematic when a large number of channels are to be multiplexed and consequently the sampling window is narrow. In the proposed ASIC, due to large number of inputs (10), the MUX ringing is of importance and consequently there is only one CMOS pass gate between the multiplexer's input and output.

An important issue in TDM multiplexer design is minimizing the inter-channel crosstalk induced by the multiplexer. There are two sources for the multiplexer induced crosstalk: *i*) the overlap of the select bits; if the two consecutively sampled channels have

their select signals overlap, there would be an inter-channel crosstalk; this problem can be resolved by writing the high level Verilog code of the DigiSampler with the accurate estimation of the capacitive loading, and robust level shifter design; in the current system the worst case overlap of the select signals is less than 0.2% of the sampling window, and *ii*) the capacitive load of the multiplexer along with the output resistance of the neural amplifiers, can result in voltage residuals from the previously sampled channel; this kind of crosstalk can be minimized by using CMOS pass gates instead of NMOS pass gates, minimizing the multiplexer capacitive load, and designing the neural amplifier's output resistance according to the capacitive load of the multiplexer.

4.4.2. The Wideband Buffer

A wide bandwidth PMOS source follower, figure 4-48, is used to buffer the time-division-multiplexed signal. The PMOS source follower is biased by a dedicated local V_{th} -referenced current source; the current source has a nominal

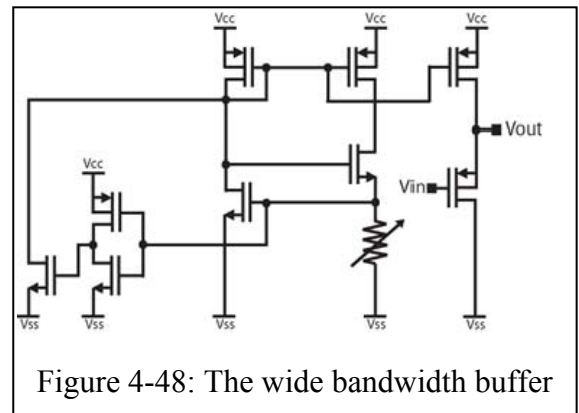


Figure 4-48: The wide bandwidth buffer

current of $4\mu\text{A}$ and the PMOS source follower has a nominal current of $12\mu\text{A}$. This block dissipates $48\mu\text{W}$ from a $\pm 1.5\text{V}$ supply voltage and has an adjustable bandwidth with a nominal 3-dB bandwidth of 8MHz. Also there is a laser trimmable array of five 1pF double-polysilicon capacitors at the output of the wideband buffer; this capacitive load reduces the multiplexing signal-path noise according to the formula $\frac{kT}{C_{buffer}}$ [4.27].

4.5. Radio Frequency Blocks

The RF blocks consist of a voltage controlled oscillator (VCO), a power amplifier (PA), and an off-chip antenna driven by the PA. The Colpitts VCO generates a wideband FM signal (WBFM) in the ISM frequency band of 433MHz which is amplified by a class-C power amplifier (PA); the transmitter's emitted power is user-adjustable through 4-bits. Having an adjustable emitted power is useful in trading transmission distance for battery life in recording setups where the transmitter is located in close proximity of the receiver ($d < 1m$). The transmitter's antenna can be either a single 1" monopole wire antenna, or a miniaturized commercial off the shelf antenna. The ISM band of 433MHz is chosen over other frequency bands, e.g. 2.4GHz, as a result of the compromise between the ASIC cost, the ASIC size, power consumption, and availability of miniaturized commercial antennas.

In [4.36], a Colpitts voltage controlled oscillator (VCO) with three off-chip components implemented in 1.5 μ m, 2P2M, CMOS process functions as the RF transmitter. It has a measured oscillator gain of 1.21MHz/V, dissipates 1.48mW from a 3V supply, transmits in the frequency band of 88-108MHz, and has a transmission range of 50cm. In [4.37] the RF transmitter is implemented by a differential LC-tank VCO in a 2P3M 0.5 μ m CMOS process, with a power consumption of 465 μ W, center frequency of 433MHz, and a transmission range of 1m; it has only one off-chip component as the inductor of the LC-tank. A wideband 900MHz receiver and transmitter with 75MHz bandwidth are demonstrated in [4.49]; the RF transmitter, implemented in 2P3M 0.5 μ m CMOS process, is a differential LC-tank VCO with only one off-chip inductor. The VCO has an oscillator gain of 23.8MHz/V, a transmission range of 1m, and a power consumption of 6.6mW from

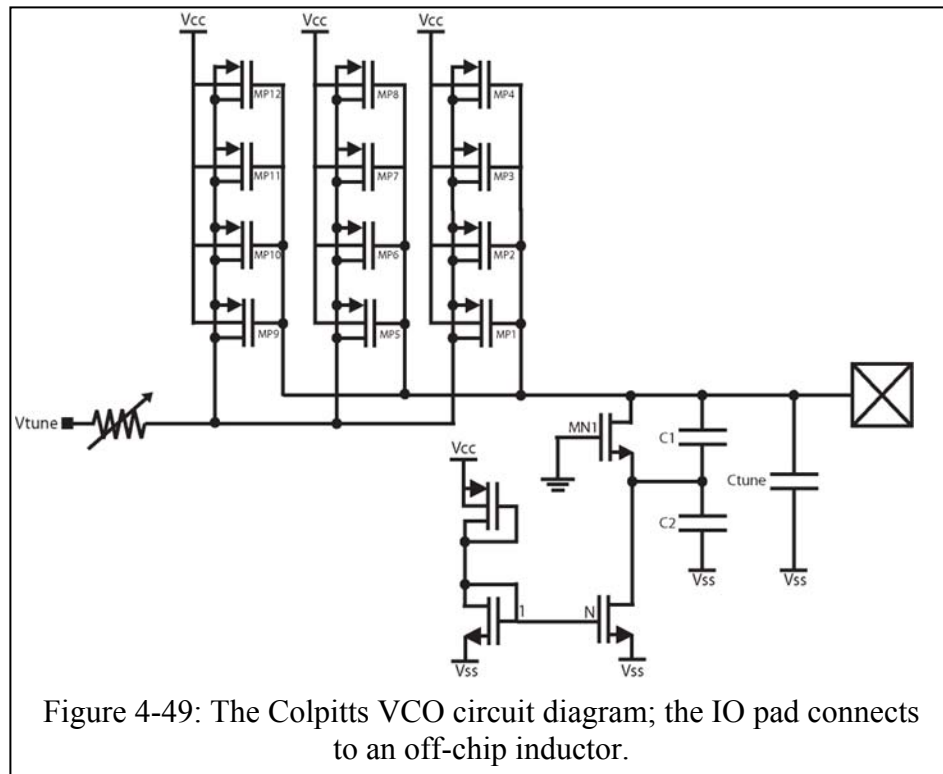
$\pm 1.5V$ power supply. An FSK VCO operating at 433MHz, implemented in 2P3M 0.5 μ m CMOS process, with only one off-chip inductor is implemented in [4.50] as the RF transmitter; this transmitter consumes 1mW from $\pm 1.3V$ power supply, with a transmission rate of 260kb/s and a range of 0.5m. And finally MAX2608 is a commercial-off-the-shelf device [4.51] with integrated IF VCO and output buffers, operating in the ISM band of 433MHz; this device requires 5 \times off-chip components, has a maximum output power of -8dBm, a maximum oscillator gain of 62.8MHz/V, with a power consumption of 8.1mW from a 3V supply.

4.5.1. Voltage Controlled Oscillator (VCO)

In the proposed work, analog frequency modulation (FM) is chosen over digital modulation schemes, e.g. FSK; this choice is justified by the fact that for the same number of channels, digital multichannel wireless biotelemetry microsystems occupy a larger bandwidth compared to their analog counterparts. The larger the bandwidth, the larger the receiver noise and consequently transmission range of digital transmitters is shorter than that of analog microsystems for the same transmitter's antenna power.

For the proposed fully analog TDM-FM wireless biotelemetry system, among the continuous wave (CW) modulation schemes frequency modulation (FM) is used for back telemetry. There are three main reasons for choosing FM over other types of CW modulation schemes: *i*) simple implementation (small active area), *ii*) low power consumption, and *iii*) superior signal-to-noise-ratio (SNR). Assuming a perfect demodulator (FM detector) the instantaneous frequency of the received FM signal ($f_c + f_{\Delta}x(t)$) can be extracted from the received RF signal. The demodulator's output

will be proportional to the FM modulator's frequency deviation f_{Δ} , and can be increased without increasing the transmitted power ($S_T = A_c^2(t)/2$). Therefore in wideband FM (WBFM), bandwidth can be traded for SNR. However, the noise advantage of WBFM



cannot be increased indefinitely. As the required bandwidth is widened to accommodate the large frequency deviation, the receiver noise increases as well, degrading the SNR of the overall system; furthermore, in a practical system there is an upper bound on the FM detector bandwidth, dictated by the external electronics. The conflicting issues of noise and bandwidth are quantified in chapter 2.

The VCO circuit diagram is shown in figure 4-49; it is a single-transistor Colpitts VCO with two laser-trimmable on-chip capacitors and one off-chip inductor. The inductor is the only off-chip component of the VCO. C_1 , figure 4-49, is implemented as an array of laser trimmable, double-polysilicon capacitors ($2 \times 100\text{fF}$, $2 \times 200\text{fF}$, and

$2 \times 400\text{fF}$); C_2 is also implemented as an array of laser trimmable, double-polysilicon capacitors ($2 \times 100\text{fF}$, $2 \times 200\text{fF}$, $2 \times 1\text{pF}$, and $2 \times 2\text{pF}$). The VCO's varactor is implemented with a laser trimmable array of $12 \times$ PMOS transistors as shown in figure 4-49. The VCO measures $390\mu\text{m} \times 890\mu\text{m}$ including the ground shields surrounding the block and the three 11.3pF power lines on-chip decoupling capacitors.

The VCO's center frequency is set at 433MHz , and has an adjustable oscillator gain with the maximum of 16MHz/V . The VCO's center frequency can also be finely tuned through a laser trimmable array of six 100fF , double-polysilicon capacitors connected to the VCO's output.

The entire transmitter operates on two 1.5V silver-oxide batteries. Since the transmitter's power consumption is dominated by the RF blocks, to prolong the battery life, the load of the VCO is on the bottom battery (GND- VSS) while the load of the PA is on the top battery (VCC- GND). The VCO's power consumption and peak to peak output voltage is set by an array of laser-trimmable current mirrors and the maximum power consumption of the VCO is achieved when all the $30 \times$ current mirrors are present (1.485mW). The VCO's phase noise is proportional to the square of its peak to peak output voltage [4.43]. By halving the supply voltage of the VCO, its phase noise increases by a factor of 4; however as derived in chapter 2, the phase noise of the VCO is not a deterministic factor in the recovered neural channel SNR. Therefore it is possible to reduce the power consumption of the VCO by a factor of two without degrading the recovered neural channel SNR. The VCO can drive the PA with a minimum of $10 \times$ current mirrors of $33\mu\text{A}$ resulting in a minimum measured power consumption of $495\mu\text{W}$.

There are several stray elements which should be included in the VCO's analysis:

- i)* the capacitive parasitics of the PCB, *ii)* the capacitive parasitics of the VCO's transconductance device, *iii)* the capacitive/resistive/ inductive parasitics of the VCO's interconnects, *iv)* the capacitive parasitics of the VCO's current source, *v)* the capacitive parasitics of the IO pads, *vi)* the resistive/

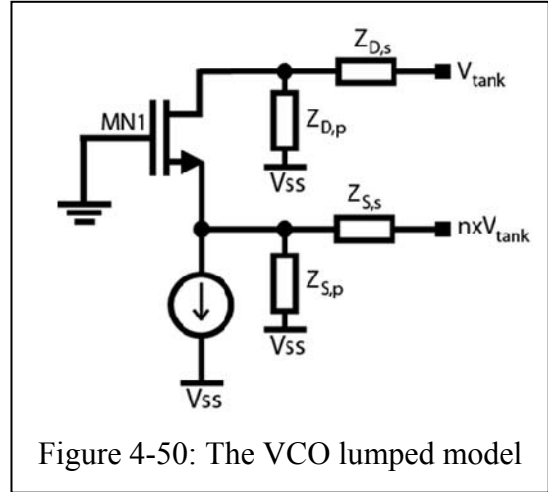


Figure 4-50: The VCO lumped model

inductive parasitics of the VCO's wirebonds, and *vii)* the resistive parasitics of the LC-tank's inductor. To include the stray elements in the analysis, the VCO model of figure 4-50 is used. The VCO is designed and optimized using a novel approach which is a combination of the Lee [4.44] and the Vittoz [4.45] methods.

In figure 4-50, various stray elements are lumped into the impedance elements $Z_{D,p}$ (Drain parallel), $Z_{S,p}$ (Source parallel), $Z_{D,s}$ (Drain series), and $Z_{S,s}$ (Source series).

$$Z_{D,p} = \frac{1}{j\omega(C_{PCB,D} + C_{IO} + C_{varactor} + C_{db} + C_{wire,D} + C_{PA} + C_{Balance})} \quad (4 - 34)$$

In 4-34, $C_{PCB,D}$ is the PCB capacitive parasitics on the drain node; C_{IO} is the capacitive parasitic of the IO pad; $C_{varactor}$ is the effective capacitance of the varactor; C_{db} is the drain-bulk junction capacitance of the VCO's transconductance device; $C_{wire,D}$ is the interconnect capacitance of the drain; C_{PA} is the capacitive load of the power amplifier (PA); and $C_{Balance}$ is the tuning capacitor array added to the VCO's drain node ($n \times 100\text{fF}$, $n \leq 6$).

$$Z_{S,p} = \frac{1}{j\omega(C_{PCB,S} + C_{IO} + C_{sb} + C_{Ibias} + C_{wire,S})} \quad (4 - 35)$$

In 4-35, C_{sb} is the source-bulk junction capacitance of the VCO's transconductance device, and C_{Ibias} is the drain-bulk junction capacitance of the VCO's current source.

$$Z_{D,S} = R_{wire,D} + j\omega L_{wire,D} + R_{wirebond} + j\omega L_{wirebond} \quad (4 - 36)$$

In 4-36, $R_{wire,D}$ is the resistance of the VCO's drain node interconnects; $L_{wire,D}$ is the inductance of the VCO's drain node interconnects; $R_{wirebond}$ is the resistance of the VCO's drain node wirebond; and $L_{wirebond}$ is the inductance of the VCO's drain node wirebond and is calculated according to the formula $L \approx 2 \times 10^{-7} l \left[\ln \left(\frac{2l}{r} \right) - 0.75 \right]$ [4.44]; in this formula l is the wirebond length and r is its diameter; as a rule of thumb the wirebond inductance is considered to be about 1nH/mm. The same way the series parasitic element of the VCO's source can be written as:

$$Z_{S,S} = R_{wire,S} + j\omega L_{wire,S} + R_{wirebond} + j\omega L_{wirebond} \quad (4 - 37)$$

By analysis of the VCO's lumped model in figure 4-50, the admittance of the circuit can be written as:

$$Y_{circuit} = \frac{I_{tank}}{V_{tank}} = - \left(\frac{n g_m \times Z_{D,p} \times Z_{S,p}}{Z_{S,s} + Z_{S,p} + g_m \times Z_{S,s} \times Z_{S,p}} - 1 \right) \quad (4 - 38)$$

In 4-38, the factor, n , stems from the capacitive voltage divider formed between C_1 , C_2 and the capacitive stray elements:

$$n = \frac{C_{1,eff}}{C_{1,eff} + C_{2,eff}} = \frac{C_1}{C_1 + C_2 + C_{PCB,S} + C_{IO} + C_{sb} + C_{Ibias} + C_{wire,S}} \quad (4 - 39)$$

In 4-39, the $C_{1,eff}$ is the same as the tank's C_1 and $C_{2,eff}$ is the parallel combination of the tank's C_2 and the capacitive stray elements between the VCO's source node and substrate (VSS).

The LC-tank of the Colpitts VCO has an admittance which near the tank's oscillation frequency can be calculated as:

$$Y_{tank} = \frac{1}{R} + j\omega C + \frac{1}{j\omega L} = \frac{1}{R} + \frac{j}{\omega_{tank}L} \left(\frac{\omega}{\omega_{tank}} - \frac{\omega_{tank}}{\omega} \right) = \frac{1}{R} + j \frac{2p}{\omega L} \quad (4 - 40)$$

In 4-40, ω_{tank} is the oscillation frequency of the tank and is equal to $\frac{1}{\sqrt{LC}}$. p is the frequency pulling and is defined as $\frac{\omega - \omega_{tank}}{\omega_{tank}}$. L is the off-chip inductor; C is the tank capacitance which in the case of a Colpitts oscillator is $\frac{C_1 C_2}{C_1 + C_2}$; R is the parallel resistor due to the inductor's finite quality factor (Q) and is defined as $R = \omega L \times Q$.

In oscillators where the tank is isolated from the circuit, the admittance of the tank described in 4-40 adequately calculates the tank characteristics near the oscillation frequency. However in an LC-tank Colpitts oscillator, the tank's parallel resistor is modified by the transformed impedance of the path looking into the VCO's source node. Therefore the Colpitts VCO tank admittance can be rewritten as:

$$Y_{tank,total} = \frac{1}{R} + \frac{n^2 g_m}{1 + g_m Z_{S,S}} + j \frac{2p}{\omega L} \quad (4 - 41)$$

In 4-41, g_m is the transconductance of the VCO's NMOS device, n is calculated in 4-39, and $Z_{S,S}$ is the parasitic impedance of the VCO's source node calculated in 4-37. As the tank total admittance in 4-41 reflects, the VCO's NMOS device transconductance, g_m , affects the tank admittance; as the g_m increases so does the tank admittance. The condition for start up can be expressed as:

$$real(Y_{tank,total} + Y_{circuit}) < 0 \quad (4 - 42)$$

The transconductance at which $Y_{tank,total} + Y_{circuit} = 0$, is called the critical transconductance ($g_{m,critical}$) which is demonstrated in the complex plane of figure 4-51

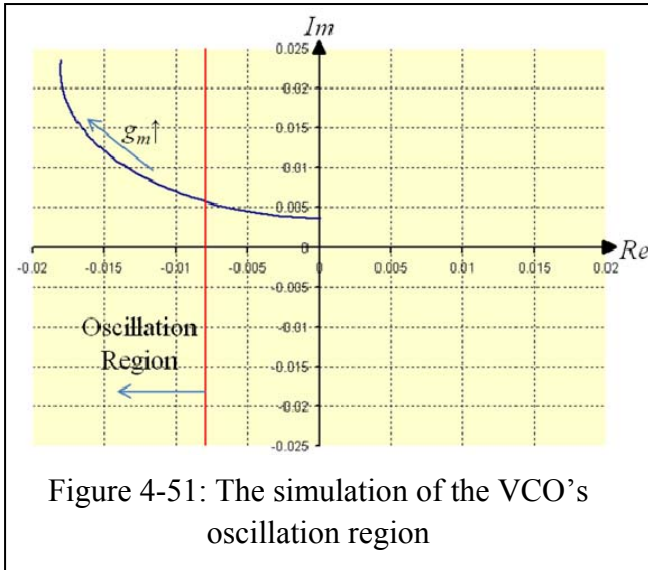


Figure 4-51: The simulation of the VCO's oscillation region

at the intersection of red and blue curves. In this figure, the blue curve is the admittance of the circuit and the red line is the worst case admittance of the tank including the transformed admittance of the VCO's source path. The admittance curve of the circuit is always located inside the upper half plane since the dominant stray elements of the circuit are capacitive. As the VCO's NMOS device transconductance, g_m , increases the absolute value of the circuit admittance real part grows larger than the worst case admittance of the tank and the VCO starts to oscillate. As can be seen the real part of the circuit admittance does not increase monotonically with the g_m , and saturates eventually.

Assuming the VCO's NMOS device transconductance is chosen in the oscillation region ($g_m > g_{m,critical}$), as the oscillation amplitude grows, due to the non-linearity of the circuit, the effective transconductance reduces. As the oscillation builds up the transconductance, g_m , in (4-38) should be replaced with the effective transconductance of the fundamental frequency: $g_{m(1)}$; this transconductance is defined as $g_{m(1)} = \frac{I_{D(1)}}{V_{(1)}}$.

This definition of the transconductance is justified by the high-Q off-chip inductor which makes the voltage across the LC-tank pure sinusoidal even though the circuit current has

higher harmonics. When the oscillation reaches the stable point the transconductance is $g_{m(1)} = g_{m,critical}$. Therefore the oscillation amplitude can be calculated as:

$$V_{(1)} = \frac{I_{D(1)}}{g_{m,critical}} = \frac{I_{D(1)}}{I_{Bias}} \times \frac{I_{Bias}}{g_{m,critical}} \quad (4 - 43)$$

In an efficient Colpitts oscillator, the VCO's NMOS device conducts current for a small fraction of the period. This characteristic of the Colpitts VCO is the underlying mechanisms of its superior phase noise performance among other VCO topologies. The factor $\frac{I_{D(1)}}{I_{Bias}}$ can be estimated as:

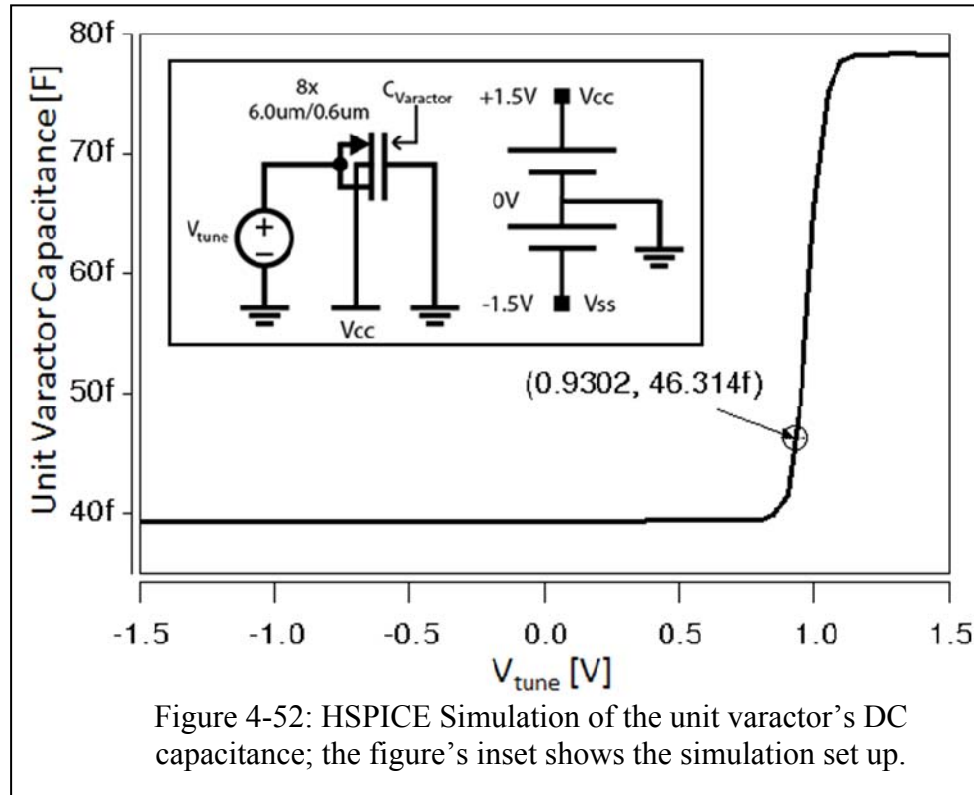
$$I_{D(1)} = \frac{2}{T} \int_0^T i_D \cos(\omega t) dt \cong 2 \times I_{Bias} \quad (4 - 44)$$

Substituting 4-44 into 4-43 the oscillation amplitude is calculated as:

$$V_{max} = \frac{2 \times I_{Bias}}{g_{m,critical}} \quad (4 - 45)$$

Therefore small critical transconductance ($g_{m,critical}$) is needed to have large oscillation amplitude. In other words, the larger the ratio, $\frac{g_m}{g_{m,critical}}$, the larger the oscillation amplitude.

The VCO's NMOS device has an aspect ratio of $300\mu\text{m}/0.6\mu\text{m}$; the minimum channel length available at the ASIC process is selected to have the highest cut off frequency ($f_T \propto \frac{1}{L^2}$ [4.34]). Furthermore this device is implemented as the parallel combination of $12 \times 15\mu\text{m}/0.6\mu\text{m}$ transistors to avoid gate resistive parasitics due to wide channel width ($300\mu\text{m}$) and finite resistance of the POLY layer ($23.5\Omega/\square$). By having a fixed aspect ratio the device transconductance is adjustable by the laser trimmable current source in 30 steps of $33\mu\text{A}$.



For high frequency applications CMOS varactors are preferred to the diode varactors due to their high quality factors [4.46]. Due to high quality factor of CMOS varactors the quality factor of the tank is determined by that of the off-chip inductor. In most VCOs intended for biomedical applications inversion-mode NMOS varactors are used [4.36, 4.37, 4.41, and 4.42]. In the presented ASIC due to the signal path architecture the VCO's varactor is implemented by a laser trimmable array of 12×PMOS transistors.

Each unit varactor is implemented as the parallel combination of eight PMOS transistors with the dimensions of 6μm/0.6μm. Figure 4-52 shows the simulation of the unit varactor DC capacitance as the tuning voltage (V_{tune}) sweeps the supply voltage range. The gate terminal is constant at the ground level, and for $V_{tune} < |V_{th,p}|$ the PMOS p -channel is not formed; therefore the total gate capacitance is dominated by the

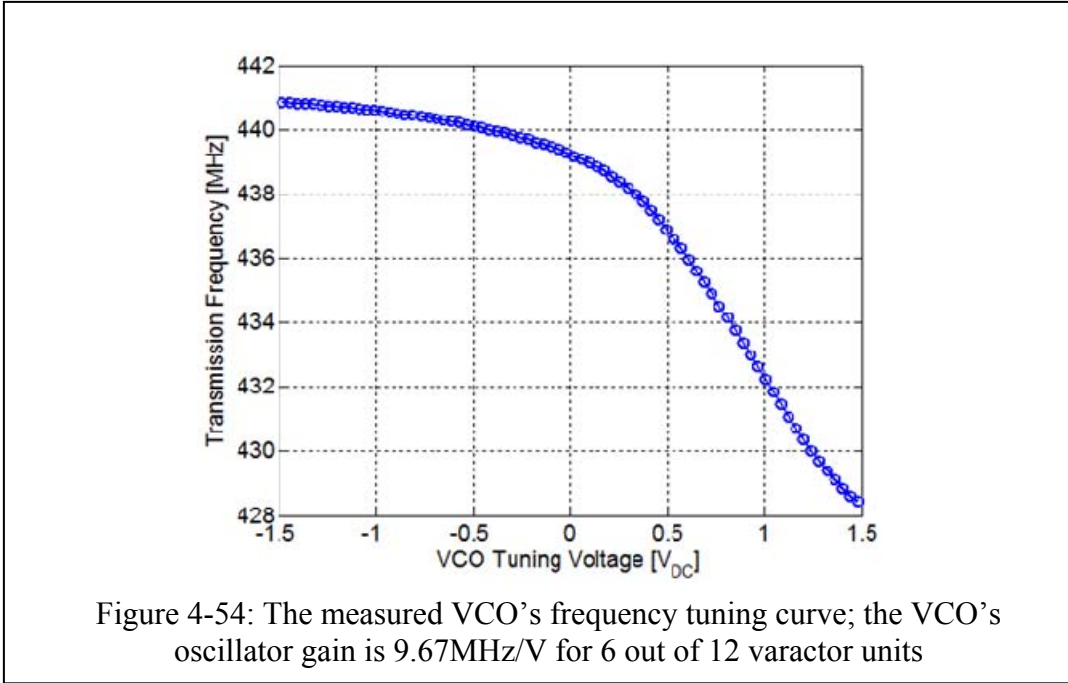
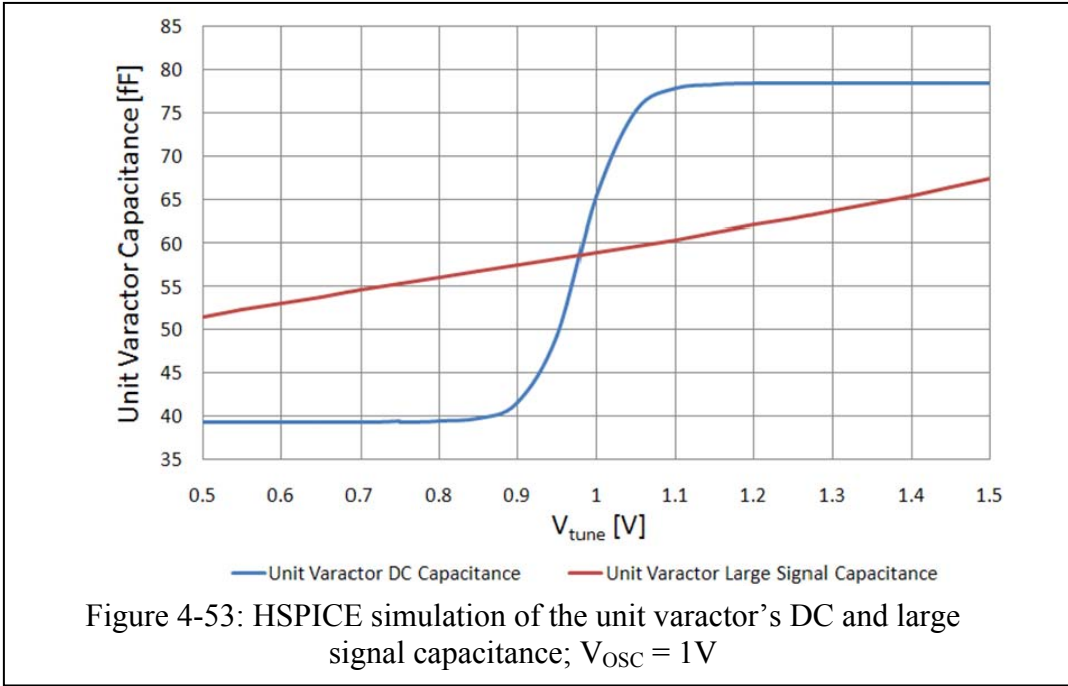
small depletion region capacitance: $C_{gate} = \frac{C_{depletion} \times (WLC_{ox})}{C_{depletion} + (WLC_{ox})} \cong C_{depletion}$. As the V_{tune} increases beyond $|V_{th,p}|$, the inversion channel is formed under the gate and the total gate capacitance starts to increase. When the channel is completely inverted, the gate capacitance becomes dominated by the gate oxide capacitance: $C_{gate} = WLC_{ox}$. This analysis is valid for the DC capacitance where the gate is at a constant voltage. However in the presented Colpitts VCO, the gate node of the varactor is connected to the VCO's drain. Therefore there is a large varying voltage on the gate and the large signal analysis is required to estimate the varactor capacitance precisely.

As shown in the ASIC architecture, figure 4-1, the V_{tune} of the VCO is connected to the wideband PMOS source follower (buffer). This buffer has a DC offset of about 930mV_{DC}. As shown in figure 4-52, an offset of 930mV_{DC} puts the varactor on the edge of the inversion region; therefore by the large varying gate voltage the average DC capacitance of the varactor is modulated by the V_{tune} . By having an oscillating voltage with amplitude of V_{OSC} on the gate node and V_{tune} on the source-drain node of the unit varactor, the voltage on varactor is calculated as: $V_{varactor}(t) = V_{OSC} \sin(\omega_0 t) - V_{tune}$ [4.36]; the varactor average capacitance per cycle is then calculated as [4.47]:

$$C_{varactor}(V_{tune}) = \frac{2}{T} \int_0^T C(V_{varactor}(t)) \cos^2(\omega_0 t) dt \quad (4 - 46)$$

Figure 4-53 shows the large signal behavior of the unit varactor capacitance and its comparison to the DC capacitance. By using 6 out of the 12 unit PMOS varactors, the proposed VCO has a measured oscillator gain of 9.67MHz/V as shown in figure 4-54.

As can be seen in figure 4-54, the frequency tuning curve of the proposed Colpitts VCO is very linear; this linear frequency tuning characteristics reduces the overall system distortion and therefore preserves the original waveform of the neural action potentials.



4.5.2. Power Amplifier (PA)

The wireless biotelemetry microsystems in which the power amplifier is not included in the transmitter's signal path [4.36, 4.37, 4.49, and 4.50], the system reliability is compromised for low power. In these systems the output of the RF modulator is directly connected to the antenna. The elimination of power amplifier has three major drawbacks: *i)* termination of the neural data back telemetry; when the nearby objects are in the antenna's near field the transmission is terminated, *ii)* instability of the back telemetry transmission center frequency and *iii)* limited transmission range. All of these drawbacks result in an unreliable system as explained in chapter 2.

Having a total transmitter power budget of less than 5mW puts stringent constraint on the total power consumption of the PA. In the intended application of the presented system, the transmission range is limited to 3m; for the short transmission distance of 3m, as quantified in chapter 2, by transmitting an RF power of $>500\mu\text{W}$ the recovered neural channel at the receiver side would theoretically have an acceptable SNR. To have a total PA power consumption of 3mW, with a transmitted an RF power of $\sim 1\text{mW}$, the PA drain efficiency should be larger than 30%, where drain efficiency is defined as the ratio of the RF output power to the PA's DC power consumption. The low power consumption of the PA and high drain efficiency are two conflicting requirements which are addressed in the proposed class-C power amplifier.

Power amplifiers are into: A, AB, B, C, D, E, and F [4.44]. In terms of linearity performance, there are two categories of power amplifiers: linear PAs (A, AB, and B) and nonlinear PAs (C, D, E, and F). In linear PAs, the output signal is a perfect replica of the input signal; non-linear PAs are also called constant-envelope since the output

Classification	A	AB	B	C	D	E	F
Maximum Efficiency(%)	50	50-78	78	100	100	100	100
Typical Efficiency(%)	35	35-60	60	70	75	80	75
Linearity	Excellent	Good	Good	Bad	Bad	Bad	Bad
V _{peak} (V)	2V _{DD}	2V _{DD}	2V _{DD}	2V _{DD}	2V _{DD}	3.6V _{DD}	2V _{DD}

Table 4-2: Comparison of power amplifier classes [4.48]

amplitude is constant and ideally independent of the input signal [4.44]; therefore non-linear PAs are suitable in modulation schemes where the input RF signal has a constant envelope and the baseband data is not encoded in the RF signal amplitude.

Theoretically efficiency and linearity are two conflicting requirements in PA design. In the proposed system efficiency is chosen over linearity by designing a non-linear Class-C PA; this design decision is justified by two system requirements: *i*) stringent transmitter power consumption constraint, and *ii*) the RF modulation scheme (FM); In the presented system, wide band frequency modulation (WBFM) is employed in which the baseband data is encoded in the zero crossing points; therefore using a non-linear Class-C PA does not pose a problem. The power amplifier classes are compared in table 4-2 [4.48].

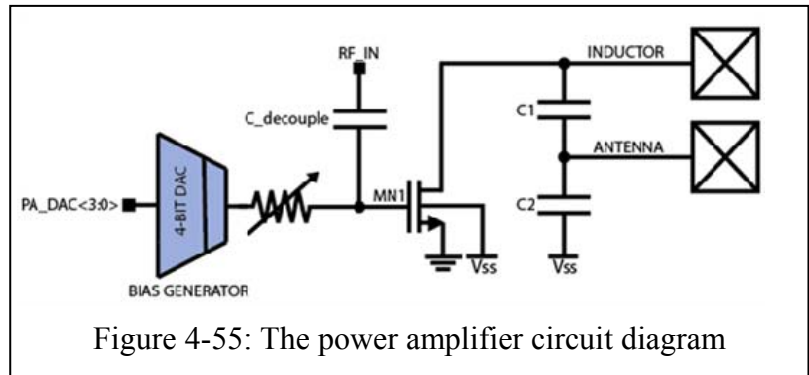
In Class-C power amplifiers the PA is biased such that the transistor conducts current for less than half a cycle which is the key in their (theoretical) superior efficiency; therefore drain current is non-zero only for a conduction angle of 2Φ ($2\Phi < \pi$). In Class-A power amplifiers the transistors conduct current for the whole cycle and therefore $2\Phi = 2\pi$; and in Class-B power amplifiers (a theoretical concept) the drain current is non-zero for exactly half the cycle: $2\Phi = \pi$. The maximum drain efficiency of the Class-C power amplifiers can be computed based on the conduction angle as [4.44]:

$$\eta_{max} = \frac{2\Phi - \sin(2\Phi)}{4(\sin(\Phi) - \Phi\cos(\Phi))} \quad (4 - 47)$$

The maximum drain efficiency of the Class-C power amplifiers approaches 100% as the conduction angle (2Φ) shrinks (4-47); however as the conduction angle reduces, so does the emitted power.

The circuit diagram of the proposed class-C RF power amplifier is shown in figure 4-55; it is a Class-C PA with two on-chip capacitors and one off-chip inductor as the LC-tank. Unlike the traditional PA designs, the presented PA has neither RF choke inductor nor RF-coupling capacitor; this design decision is justified by the fact that the transmitter PCB size is to be minimized; therefore the large off-chip RF choke inductor and RF-coupling capacitor are eliminated from the design. The PA's only RF inductor

functions as the LC-tank inductance element and also provides the power amplifier with the DC current. The LC-tank capacitor is the series



combination of C_1 and C_2 (figure 4-55); the LC-tank forms a tapped capacitor resonator which also functions as the impedance-matching-network or impedance-upconverter [4.44]. The two on-chip capacitors up-convert the antenna load to further reduce the power consumption.

The conduction angle (2Φ) and consequently the transmitted power are adjusted through PA's gate bias voltage by a 4-bit DAC. The PA DAC is set by the DigiSampler; the user-programmable PA gate's DC bias can be selected linearly between $0V_{DC}$ and

1.5V_{DC} with 4-bits of resolution. The PA DAC is very similar to the Frame-Marker DAC explained in 4.3.1.2. To minimize power consumption, the PA operates on a single silver-oxide, 1.5V battery connected between GND and VCC. There are two advantages to use the GND-VCC battery for the PA: *i)* the VSS-GND battery is used by the VCO; therefore the PA load is on the GND-VCC battery to prolong the battery lifetime, and *ii)* the body terminal of the PA's

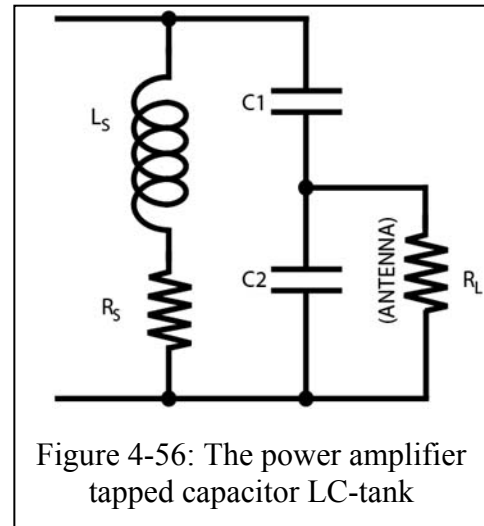


Figure 4-56: The power amplifier tapped capacitor LC-tank

NMOS is at VSS but its source is connected to the GND; a source-body voltage of 1.5V increases the NMOS threshold voltage and therefore reduces the conduction angle further. At 3mW of total power, the transmitted power to a 50Ω Antenna is about 1mW which translates into 33% drain efficiency.

One should note that in Class-C power amplifiers the conduction angle and therefore the drain efficiency are not explicit design parameters to dictate the tank characteristics; in fact these parameters are the consequence of input amplitude and the PA gate's DC bias. The design procedures for the presented Class-C power amplifier starts with the tapped-capacitor-resonator as shown in figure 4-56.

In figure 4-56, the R_L is the antenna load, e.g. 50Ω; C_1 and C_2 are the on-chip tapped capacitors; L_s is the total off-chip inductor and R_s is the parasitic resistance attributed to the finite quality factor (Q) of the inductor. In LC-tanks usually the quality factor is dominated by that of the inductor; here however due to the antenna load, all the tank elements play role in determining the overall LC-tank quality factor. The known

parameters are the center frequency ($f_0=433\text{MHz}$), the bandwidth (BW, e.g. 50MHz) and the antenna load (e.g. 50 Ω). From these parameters the desired tank quality factor is:

$$Q_{in} = \frac{\omega_0}{BW} = \frac{R_{in}}{\omega_0 L_s} \quad (4 - 48)$$

In 4-48 R_{in} is the equivalent parallel resistance looking into the tank; it is the parallel combination of two resistors: the equivalent parallel resistance of the antenna load (R_{p2}), and the equivalent parallel resistance of the inductor (R_{p1}). This resistance can be calculated as $R_{in} = R_{p1} || R_{p2}$. The tank center frequency can be calculated from the tank elements and the capacitive parasitics:

$$\omega_0 = \frac{1}{\sqrt{L_s(C_{12} + C_{x,IND})}} \quad (4 - 49)$$

In 4-49, C_{12} is the equivalent tank capacitance including the capacitive parasitics on the antenna node ($C_{x,ANT}$); and $C_{x,IND}$ is the capacitive parasitics on the PA's inductance node. C_{12} can be calculated as $C_{12} = \frac{C_1 C_{2s}}{C_1 + C_{2s}}$ where C_{2s} is the equivalent series capacitance of the tank capacitor C_2 and the capacitive parasitics on the antenna load ($C_2 + C_{x,ANT}$).

R_{p1} is calculated as $R_{p1} = Q_{L_s} \omega_0 L_s$; R_{p2} is upconverted by the tapped capacitor resonator and is calculated as

$$R_{p2} = \left(\frac{C_1 + (C_2 + C_{x,ANT})}{C_1} \right)^2 \times R_L \quad (4 - 50)$$

For any selected off-chip inductor, the R_{in} can be calculated from 4-48; by knowing the off-chip inductor quality factor at 433MHz, the equivalent parallel resistance of the inductor (R_{p1}) can be calculated. Therefore the required upconverted resistance of

the antenna load (R_{p2}) can be easily calculated as: $R_{p2} = \frac{R_{p1} \times R_{in}}{R_{p1} - R_{in}}$. By having a value for R_{p2} , the tank's capacitive ratio is calculated from 4-50 as:

$$\frac{C_1}{C_1 + (C_2 + C_{x,ANT})} = \sqrt{\frac{R_L}{R_{p2}}} \quad (4 - 51)$$

C_{12} is derived from the tank center frequency formula in 4-49; C_{12} is the series combination of C_1 and C_{2s} ; C_{2s} can be calculated from C_2 as:

$$C_{2s} = (C_2 + C_{x,ANT}) \times \frac{Q_2^2 + 1}{Q_2^2} = (C_2 + C_{x,ANT}) \times \frac{\omega_0^2 (C_2 + C_{x,ANT})^2 R_L^2 + 1}{\omega_0^2 (C_2 + C_{x,ANT})^2 R_L^2} \quad (4 - 52)$$

From 4-52, 4-51 and 4-49 the required capacitors of the tank for the selected off-chip inductor can be calculated. The power amplifier circuit elements are chosen by the described design procedure implemented in Matlab; the accuracy of the HSPICE simulation is within 0.5% of the Matlab simulation.

4.5.3. Results and Discussions

Figure 4-57 shows the measured PA total power consumption and the antenna power for various PA gate bias voltages. In this measurement the PA RF input is driven by the on-chip VCO. At $0.5V_{DC}$ of gate bias voltage, the PA has a total power consumption of 1mW and an antenna power of $158\mu W$. For a gate bias voltage of $0.65V_{DC}$ the PA total power consumption and antenna power are 2mW and $514\mu W$ respectively. And finally for a gate bias voltage of $0.8V_{DC}$ the PA total power consumption and antenna power are 3mW and 1mW respectively.

The PA power spectrum is measured in figure 4-58; the proposed PA has its center frequency at 433MHz with approximately 100MHz of bandwidth.

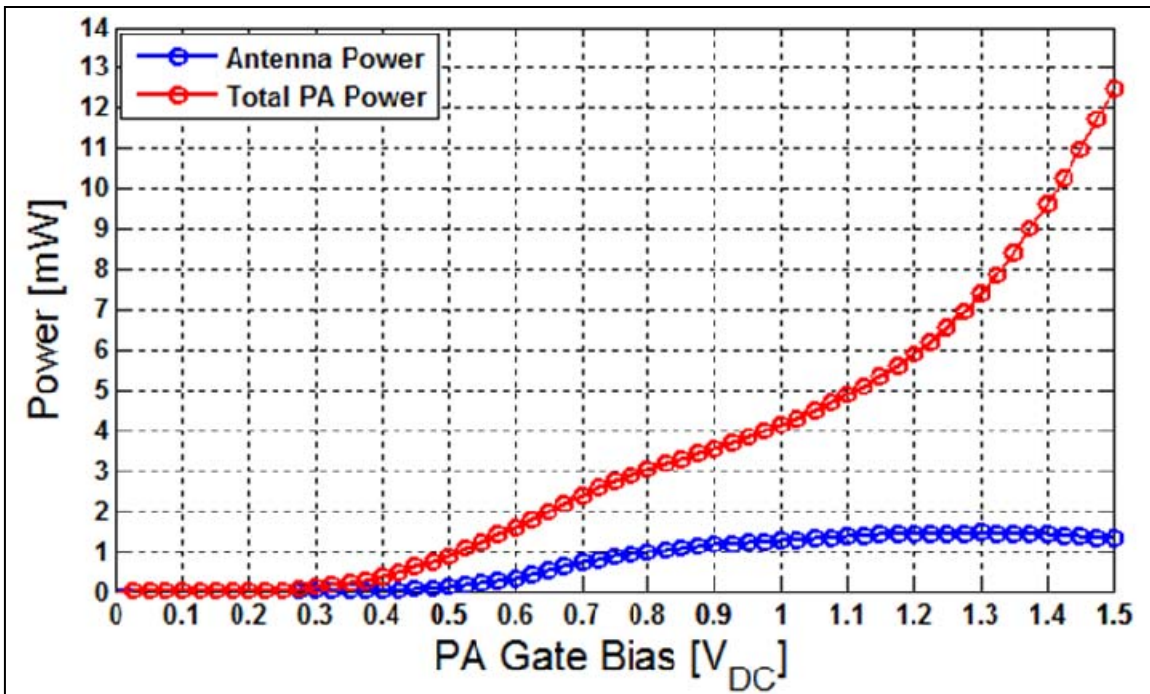


Figure 4-57: Measured total PA power consumption and emitted antenna RF power vs. gate bias

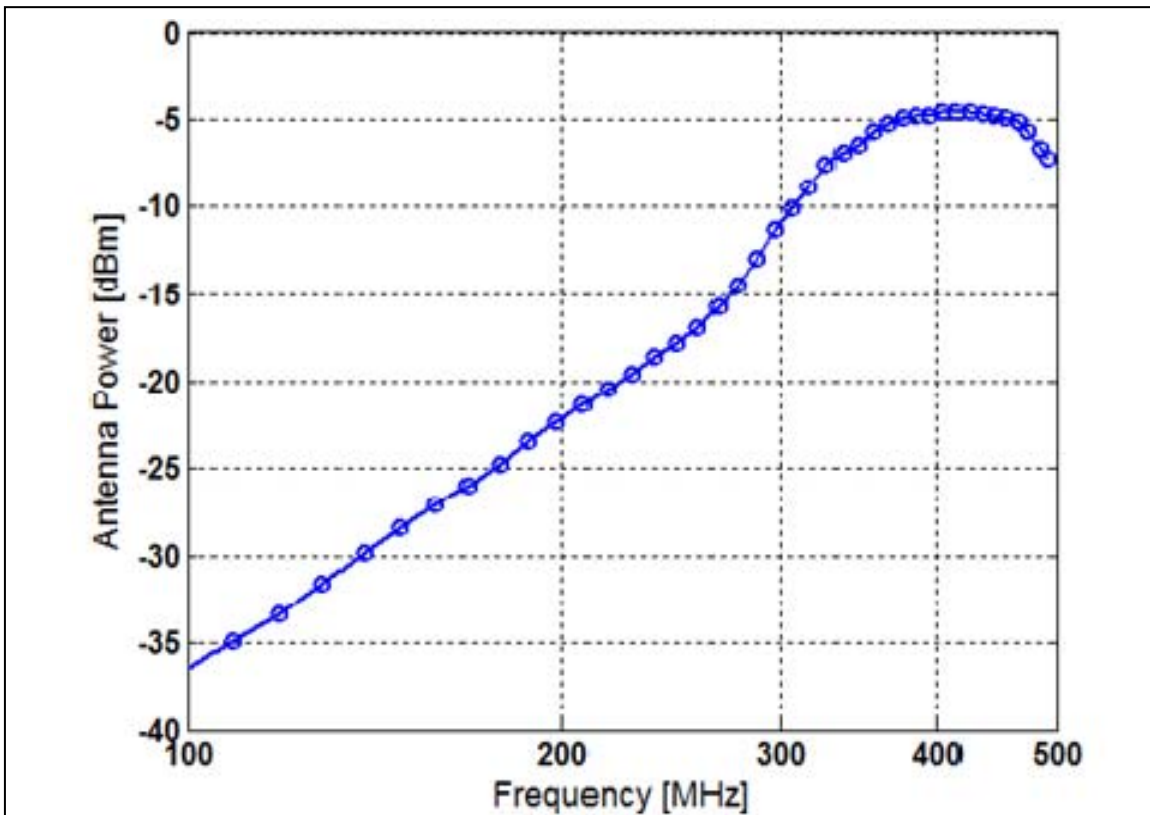


Figure 4-58: measured PA frequency response

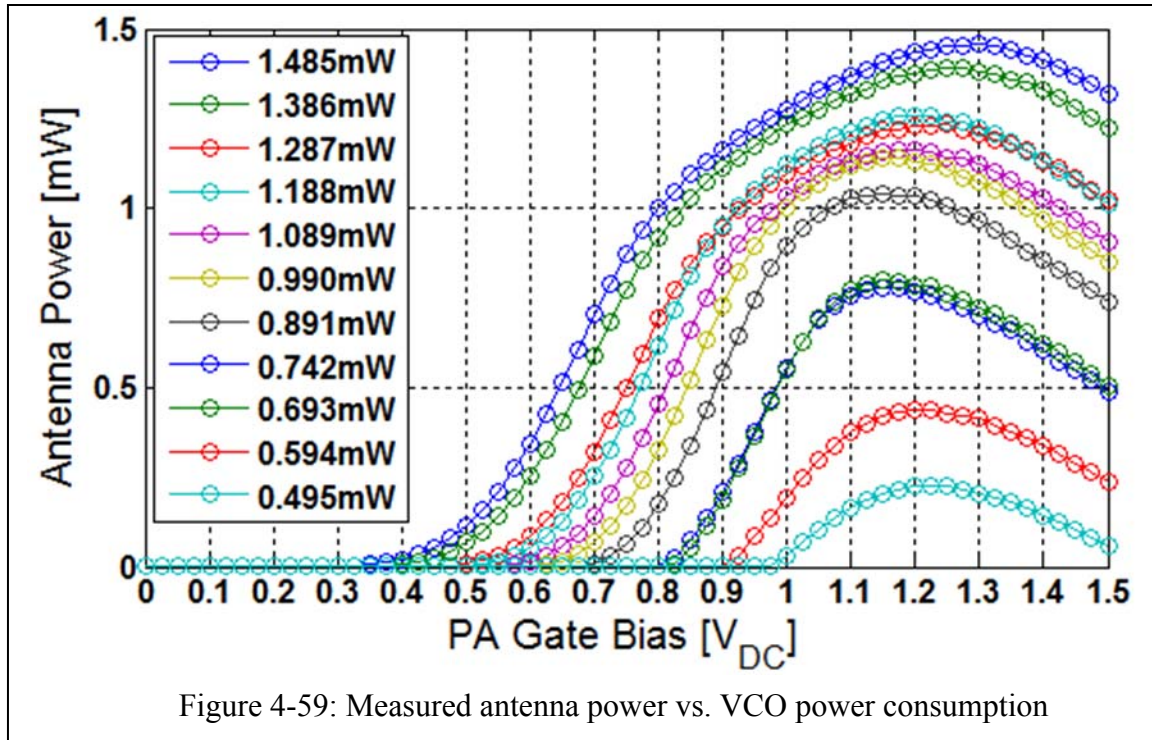


Figure 4-59: Measured antenna power vs. VCO power consumption

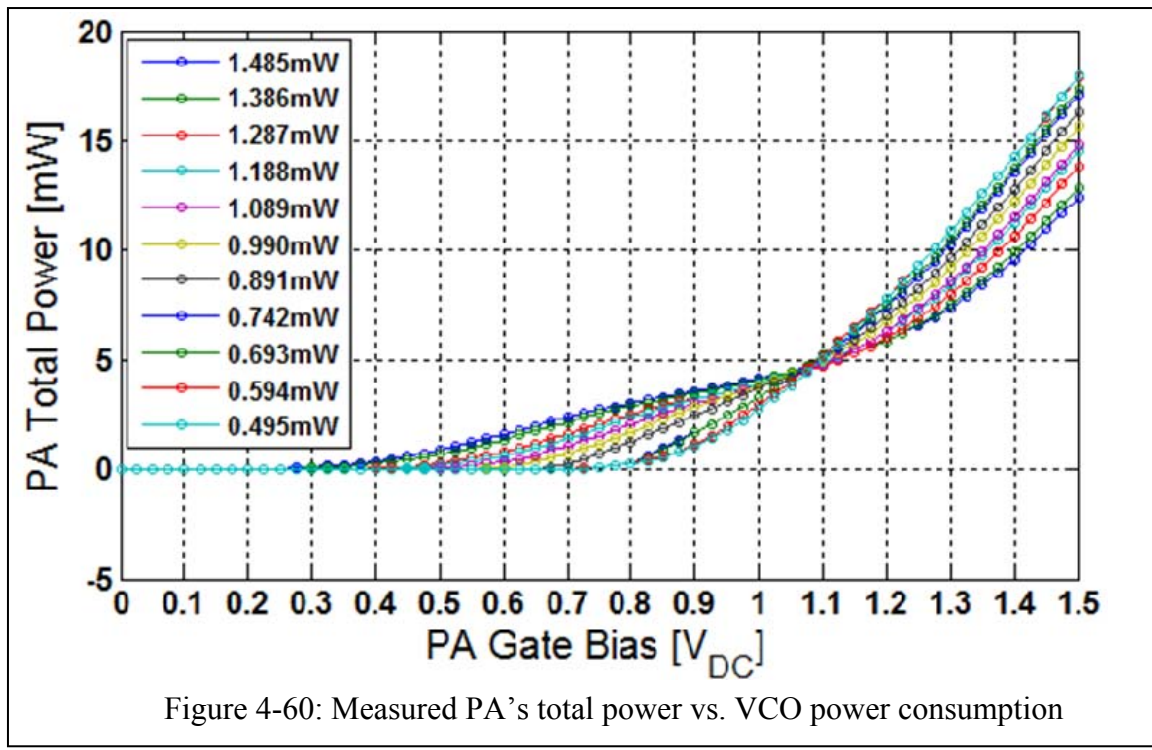
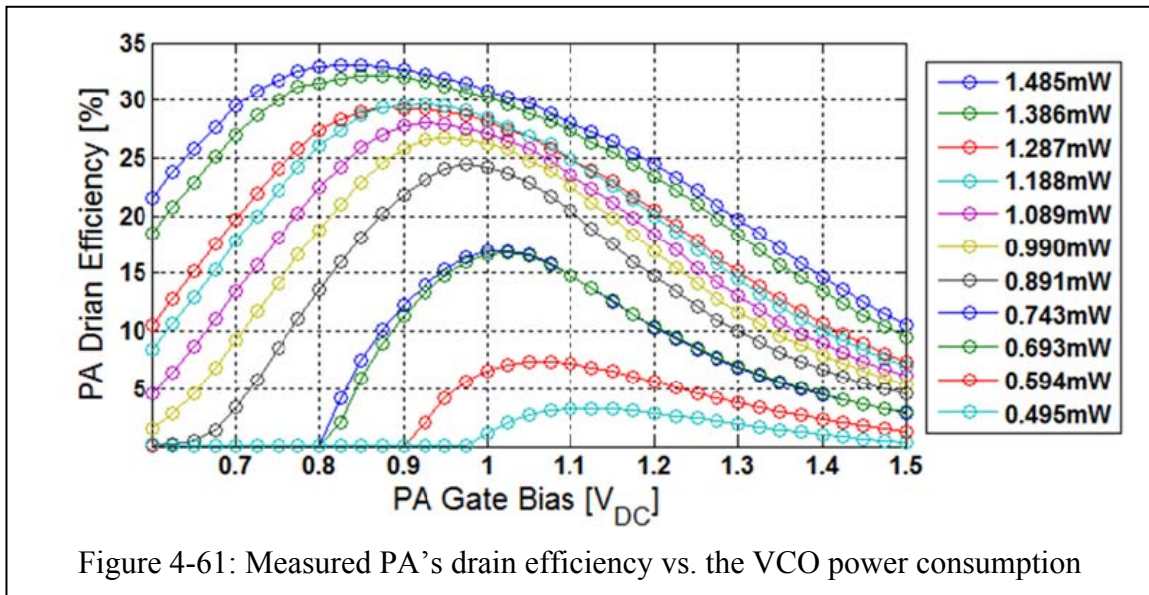


Figure 4-60: Measured PA's total power vs. VCO power consumption

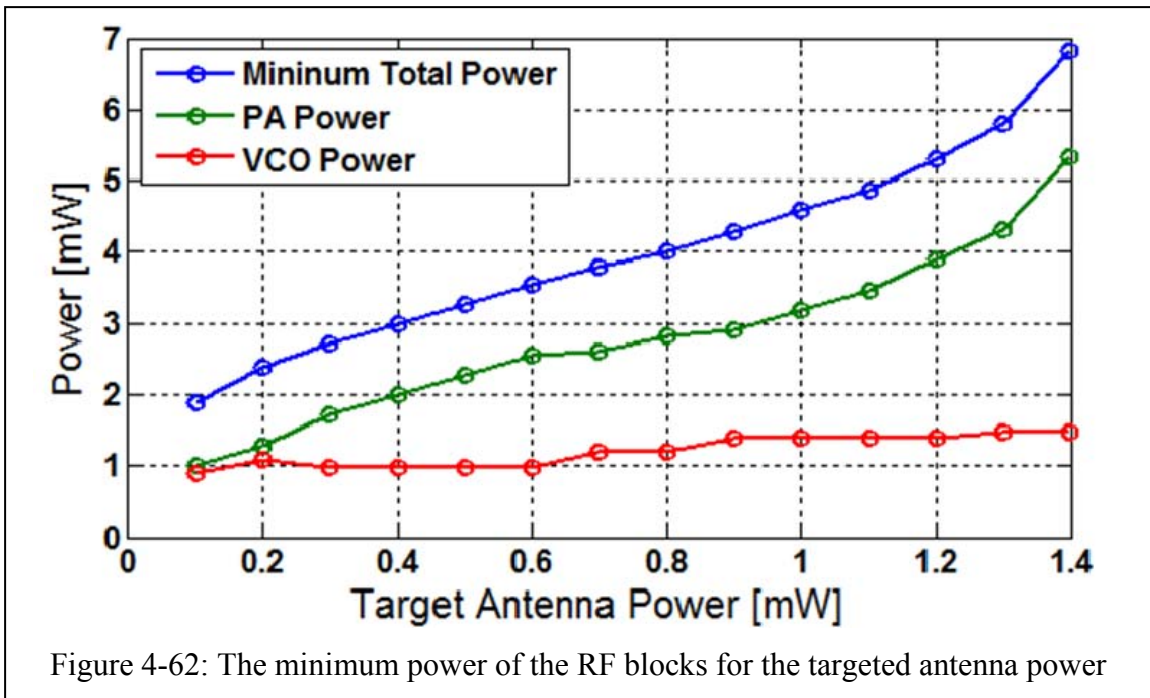
The emitted antenna RF power is function of both PA's gate DC bias voltage and the PA's input RF amplitude. The PA's input RF amplitude can be adjusted through the number of current mirrors of the VCO. Figure 4-59 shows the measured antenna power as the VCO power consumption is swept from 0.495mW to 1.485mW.

Figure 4-60 is the measured PA's total power vs. the VCO power consumption; as can be seen there is a critical gate DC bias voltage around which the behavior of the PA changes. For gate DC bias voltages smaller than $1.075V_{DC}$, the smaller the RF input amplitude, the smaller the PA total power consumption; however at gate DC bias voltages larger than $1.075V_{DC}$ this condition reverses. This voltage is the threshold voltage of the PA's NMOS device beyond which the DC power dominates the RF power.

The measured PA's drain efficiency for various VCO power consumption levels is shown in figure 4-61. The proposed PA achieves a maximum drain efficiency of 33.14%.



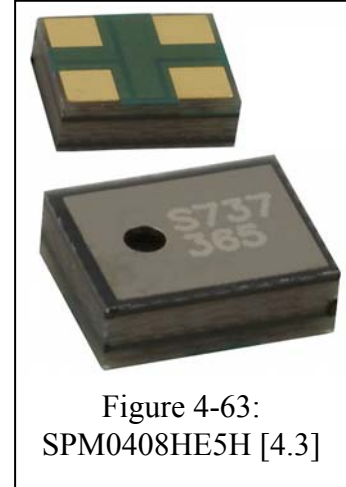
From the target transmission distance the minimum required antenna power can be calculated. A minimum antenna power can be provided by a number of combinations of PA and VCO settings. To minimize the total power consumption the data in figures 4-59 and 4-60 are analyzed to find a combination of VCO and PA settings which yields the lowest power consumption while providing the minimum antenna power. The result is shown in figure 4-62.



From the data in figure 4-62, for an antenna power of $400\mu\text{W}$, the VCO power and the PA total power should be 1mW , and 2mW respectively. Therefore a total of 3mW is required for modulation and transmitting an antenna power of $400\mu\text{W}$.

4.6. Audio Circuitry

NC_V3 features an audio channel provided by a surface mount MEMS microphone SPM0408HE5H (KNOWLES) [4.3] shown in figure 4-63. This microphone has on-chip circuitry for signal conditioning and a bandwidth of 10KHz; it consumes a current of 100 μ A (no audio signal) to 350 μ A (maximum gain and input audio signal) from a 1.5V-3.6V supply. SPM0408HE5H small dimensions, 4.72mm \times 3.76mm \times 1.25mm, and light-weight 0.06g, allow for soldering it on the back side of the transmitter's PCB. The employed MEMS microphone requires four off-chip



components (2 \times resistors and 2 \times capacitors) for filtering the microphone's output signal and gain control. The output of the off-chip RC high pass filter is connected to the TDM multiplexer's tenth-input through the dedicated IO pad and wirebond. Table 4-3 [4.3] lists

	Symbol	Condition	Limits			Unit
			Min.	Nom.	Max.	
Directivity		Omni-directional	—	—	—	
Sensitivity	S	@ 1kHz (0dB-1V/Pa)	-26	-22	-18	dB
Output Impedance	Z _{OUT}	@ 1kHz (0dB-1V/Pa)	—	—	300	Ω
Current Consumption	I _{DD5}	Across 1.5 to 3.6 volts	100	—	350	μ A
Signal to Noise Ratio	S/N	@ 1kHz (0dB-1V/Pa)	55	59	—	dB
Supply Voltage	V _s		1.5	—	3.6	V
Typical Input Referred Noise	ENL	A-weighted	—	35	—	dBA SPL
Sensitivity Loss Across Voltage		Change in sensitivity over 3.6V to 1.5V	No Change Across Voltage Range			dB
Maximum Input Sound Level			At 100dB SPL, THD < 1% At 115dB SPL, THD \leq 10%			

Table 4-3: Acoustic and Electrical Specifications of the SPM0408HE5H [4.3]

the specifications of the employed MEMS microphone.

4.7. Conclusion

In this chapter the individual circuit blocks of the wireless multichannel neural transmitter (NC_V3) were discussed. The brain of the transmitter, DigiSampler, is programmable by the user, generates the on-chip clock, and dissipates $24\mu\text{W}$ from a $1.5V_{\text{DC}}$ supply voltage. The neural amplifiers of the front-end employ a novel active-low-frequency-suppression (ALFS) architecture which suppresses the Flicker ($1/f$) noise, LFP signals, movement-artifacts, electrode-ECF DC potential, and inter-channel DC offsets. The neural amplifier once configured for band pass filter (BPF) has a measured input referred voltage noise of $2.4\mu\text{V}_{\text{rms}}$ and $3\mu\text{V}_{\text{rms}}$ for power consumptions of $14\mu\text{W}$ and $28\mu\text{W}$, respectively. In ALFS configuration, the neural amplifier has a measured input referred voltage noise of $5.2\mu\text{V}_{\text{rms}}$ and $5.86\mu\text{V}_{\text{rms}}$ at power consumptions of $31.5\mu\text{W}$ and $17\mu\text{W}$, respectively. The Colpitts voltage controlled oscillator (VCO) employed in data back telemetry at the ISM band of 433MHz , has only one off-chip inductor, and dissipates $495\mu\text{W}$ - 1.485mW with an oscillator gain of 9.67MHz/V . The designed class-C PA has only one off-chip inductor, and employs a tapped-capacitor tank which upconvert the antenna impedance to save power. The emitted power is user adjustable through 4-bits by changing the gate bias voltage of the PA. The PA has a maximum measured drain efficiency of 33% and a maximum measured antenna power of 1.457mW . This user-programmable wireless interface can be used to trade power consumption for transmission range.

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CHAPTER 5

EXTERNAL ELECTRONICS

To recover the individual neural channels from the received TDM-FM signal, three tasks are required: *i*) wideband FM demodulation, *ii*) time division demultiplexing, and *iii*) neural channel filtering. The FM demodulation, recovers the time-division-multiplexed (TDM) signal of the transmitter which carries the neural channels in one continuous stream. Time division demultiplexing separates the neural channels from the TDM stream. The last block of external electronics is the filtering; the band pass filter reduces the noise present on the neural channel and is essential to keep the recovered neural channel SNR at an acceptable level. The output of the filtering stage will be either saved in the host computer for future offline use, or will be relayed, e.g. via Ethernet, to other computers running online spike sorting algorithms.

5.1. Wideband Frequency Demodulation

As explained in chapter 2, to improve the SNR of the recovered neural channel, the transmitter VCO's oscillator gain (f_{Δ}) should be selected according to the system parameters; doing so, the RF signal emitted from the neural transmitter is a wideband frequency modulated (WBFM) signal. As of today, there is no analog commercial off the shelf FM radio capable of demodulating the TDM-FM signal of the neural transmitter which can be as wide as 6MHz around the 433MHz center frequency. To demodulate the

WBFM signal, two options are available: *i*) custom made analog WBFM radio, and *ii*) software defined radio (SDR). Four different radio architectures have been used throughout the course of this project.

5.1.1. WinRadio-1550e

WinRadio-1550e [5.1], figure 5-1, is an external, analog radio receiver which can be controlled by the host computer. This radio is capable of demodulating AM, SSB, narrowband FM, and wideband FM signals in the frequency range of 0.15-1500MHz. The demodulated data is entered in the host computer via RS-232 serial port or in continuous analog stream which has to be read into the host computer, by Data Acquisition (DAQ) card; an



Figure 5-1: WinRadio-1550e [5.1]

NI-6070E DAQ card [5.2] with a 12-bit resolution and a maximum sampling frequency of 1.25MHz is used for reading the demodulated WinRadio-1550e output. WinRadio-1550e has a PLL-based, triple-conversion, superheterodyne architecture. In the wideband-FM mode this receiver provides a maximum bandwidth of 280KHz. As explained in chapter 2, a bandwidth of 280KHz is not adequate for the wideband TDM-FM signal of the neural transmitter which can be as wide as 6MHz. In a neural transmitter with a front-end gain of <math><40\text{dB}</math>, and an oscillator gain of <math><1\text{MHz/V}</math>, if the number of channels is restricted to 3, this radio receiver can demodulate the TDM-FM signal with an acceptable crosstalk level of about 5% [5.3]. However if more than three

channels are multiplexed, the crosstalk level rises according to the formula 2-20 and can be as large as 40% [5.4].

5.1.2. NI-5660

NI-5660 [5.2] is a 2.7GHz RF vector signal analyzer targeted for automated tests.

The block diagram is shown in figure 5-2. The architecture of NI-5660, like most SDRs,

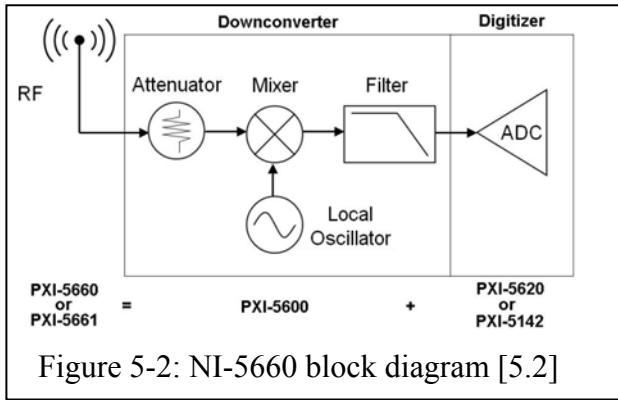


Figure 5-2: NI-5660 block diagram [5.2]

is that of a superheterodyne receiver in which the demodulation is implemented in software run by the host computer. Due to its versatile architecture any demodulation algorithms can be implemented; furthermore it has a large

realtime bandwidth of 20MHz. The wideband TDM-FM signal from the neural transmitter has a bandwidth of <6MHz which can faithfully be demodulated with this RF vector signal analyzer.

NI-5660 is comprised of a 9KHz-2.7GHz downconverter (PXI5600) followed by a 14-bit, 64MS/s digitizer (PXI5620). The downconverter module (PXI5600), figure 5-3, includes an onboard ultrahigh-stability oven-controlled crystal oscillator (OCXO) to provide the frequency accuracy and stability. It can acquire signals between 9 kHz and 2.7 GHz with a 20 MHz real-time bandwidth. The limited bandwidth of COTS FM radios results from this module which is solved in NI-5660 by its wideband downconverter. The user-selectable attenuation is applied to the input signal; the attenuated signal is then upconverted. The upconverted signal is band pass filtered through an acoustic resonator

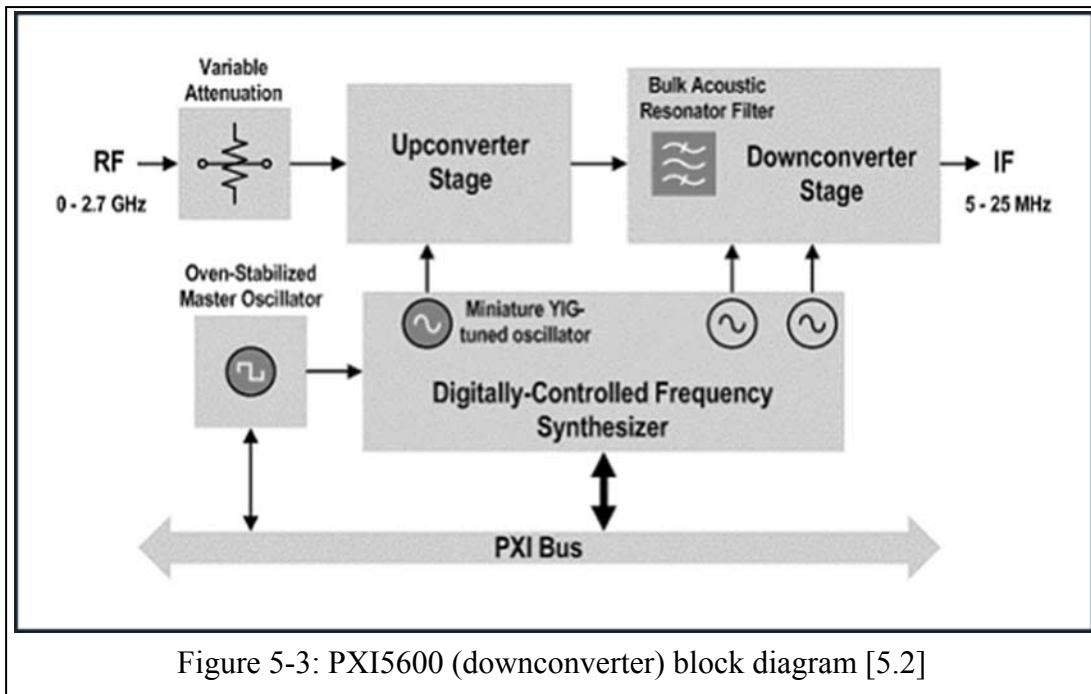


Figure 5-3: PXI5600 (downconverter) block diagram [5.2]

filter for image rejection; this acoustic resonator filter is the only filtering stage in the downconverter block. The filtered signal is fed to a multistage downconversion block which produces the output signal in the IF frequency band of 5MHz-25MHz (centered at 15MHz with a realtime bandwidth of 20MHz).

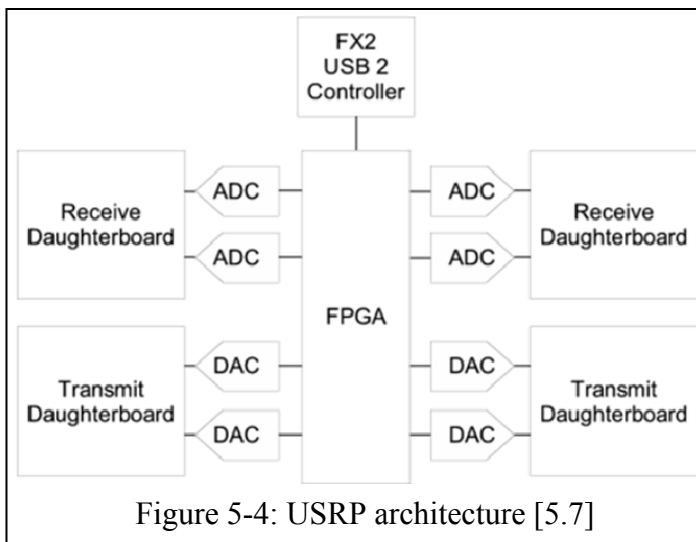
The digitizer (PXI5620) incorporates a 14-bit, 64 MS/s ADC and a digital downconversion ASIC. The digitized output of PXI5620 is available to the host computer through the PXI bus which is a 32-bit, 133MB/s data bus based on the PCI standard.

Using the NI-5660 along with Labview/Matlab software tools any demodulation algorithms can be implemented in digital domain [5.2]. The FM detector implemented with this unit has been successfully employed in demodulating the received wideband TDM-FM signal of three neural channels from NC_V1 [5.5] and fifteen neural channels from FMT_V1 [5.6].

5.1.3. Software Defined Radio

The Universal Software Radio Peripheral (USRP) is a Digital Acquisition system containing four 64MS/s 12-bit ADCs and four 128MS/s 14-bit DACs [5.7]. The high level architecture of this unit is similar to that of most SDRs, as shown in figure 5-2. This unit serves as a digital baseband and IF block of a radio communication system. In this radio all of the waveform-specific processing (modulation/demodulation) is performed on the host CPU and the high-speed general purpose operations (digital up/down conversion, decimation, etc.) are done on the USRP's FPGA (Altera Cyclone EP1C12 FPGA). The USRP connects to the host computer through a USB2 interface. The USRP architecture is shown in figure 5-4.

The main motherboard is accompanied by several transmitter and receiver plug-in daughterboards which cover the frequencies up to 5.9 GHz. These daughterboards are the RF front-end of the USRP receiver system and interface the antenna to the USRP's motherboard. The band of 433MHz is selected for the back telemetry transmission frequency as explained in section 2.4. To downconvert the signals in this band, the



TVRX daughterboard is used along with the USRP. TVRX is essentially a VHF/UHF receiver based on a TV tuner module. The TVRX daughterboard covers the RF frequency ranges from 50MHz to 860MHz, with an IF bandwidth of 6MHz. The

TVRX IF bandwidth is the bottleneck of the system limiting the FM detector's total bandwidth to 6MHz. The TVRX is built around the 4937 DI5 RF tuner module, model 3×7702; this model, shown in figure 5-5, down converts the RF input to the output center frequency of 5.75MHz (± 50 KHz) in two conversion steps. It has a tuning resolution of 62.5KHz, and an average noise figure of 8dB [5.8].

After the received RF signal is down converted to IF frequencies by the TVRX,

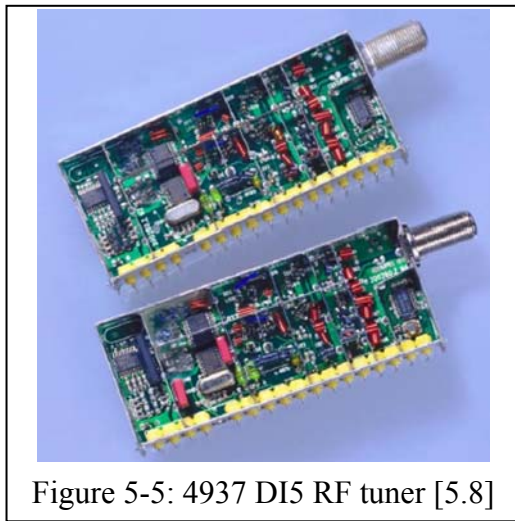


Figure 5-5: 4937 DI5 RF tuner [5.8]

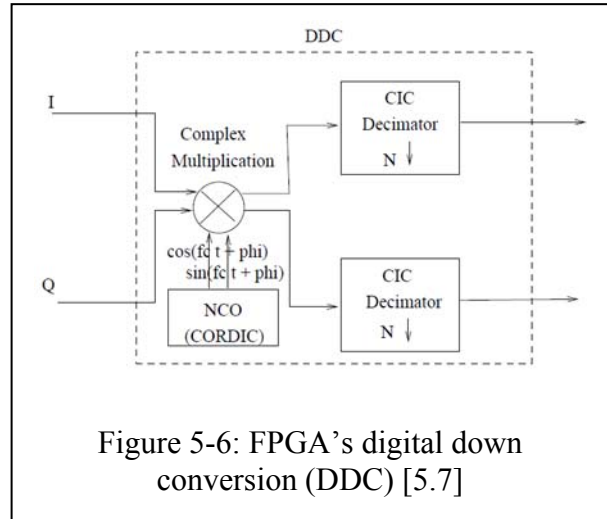
the IF signal is sampled by the dedicated ADC at a resolution of 12-bit and a sampling frequency of 64MS/s. AD9862 [5.9] provides the analog to digital conversion along with the digital Hilbert filters for complex sampling applications. In real sampling applications, there are two independent sampled IF channels available. In complex sampling, the IF signal is

sampled through AD9862, and two 12-bit streams of I-Q samples are fed to the FPGA.

The USRP's FPGA (Altera Cyclone EP1C12) performs two tasks: *i*) software controlled fine tuning through numerically controlled oscillator (NCO), and *ii*) decimation and low pass filtering. Figure 5-6 shows the block diagram of the USRP FPGA's digital down conversion.

The FPGA connects to a USB2 interface chip, the Cypress FX2, and on to the computer. The maximum data transfer rate out of the USRP is 32MB/s. The samples sent across the USB are signed 16-bit integers in I-Q format. This results in 8Mega complex samples per second. Due to complex sampling, the maximum effective total spectral

bandwidth is 8MHz; as mentioned earlier the bottleneck is not the data transfer rate, but the IF bandwidth of TVRX (6MHz). On the computer any demodulation algorithm can be implemented and applied to the received data samples from the USRP. The open source GNU Radio (for USRP board)



software is originally developed for Linux OS however recently the Simulink (Windows OS) drivers for USRP are developed. The demodulation, demultiplexing and analysis code are integrated in a user-friendly code in Matlab. More information on USRP/GNU radio can be found in [5.6].

5.2. Neural Channel Recovery

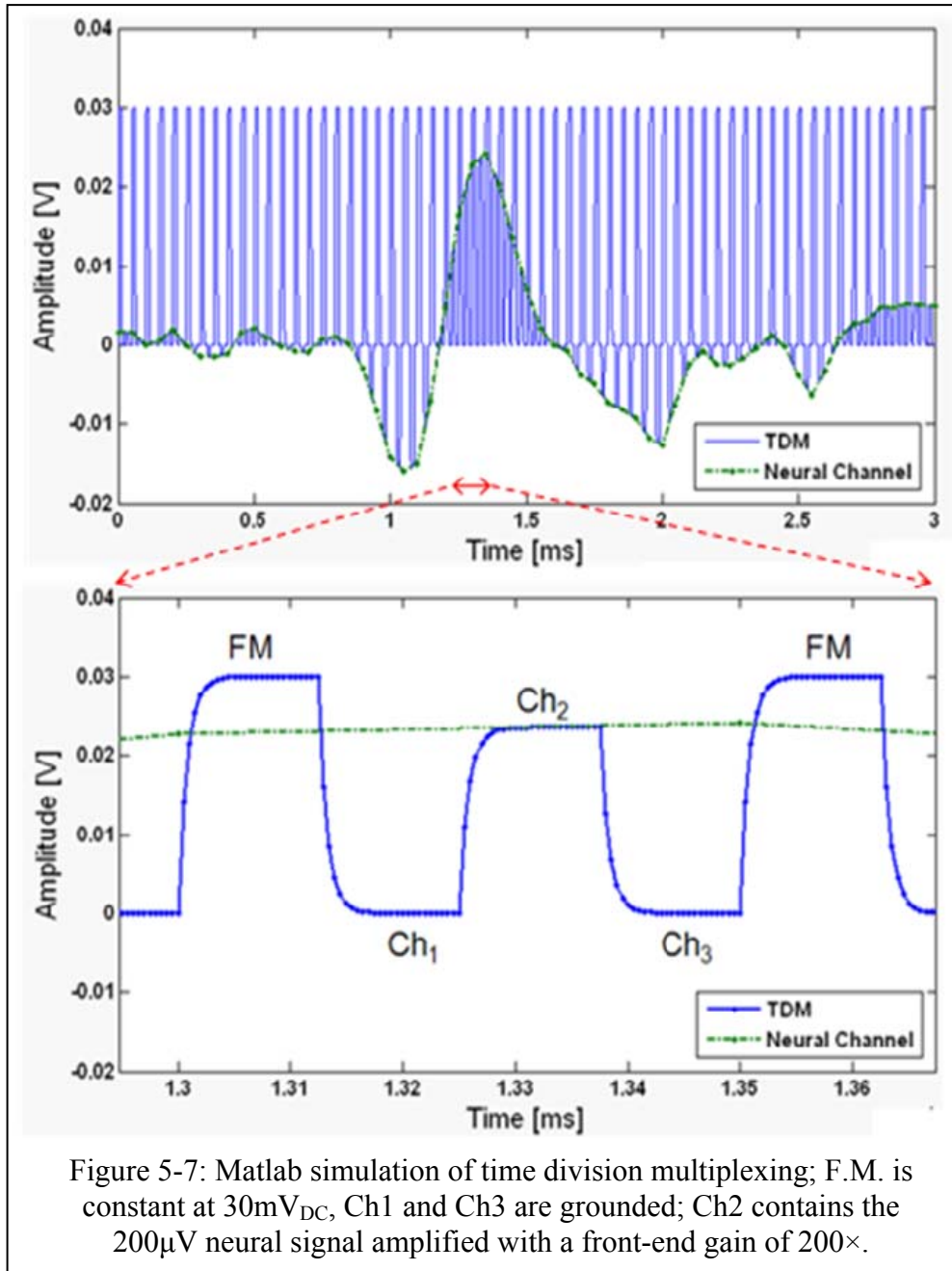
In a system employing software defined radio, other than demodulation the host computer is also responsible for neural channel recovery. The channel recovery consists of: *i*) time division demultiplexing, and *ii*) filtering.

5.2.1. Time Division Demultiplexing

After FM demodulation of the received RF signal, the individual channels must be extracted from the TDM data stream through the demultiplexing process. There are two approaches for demultiplexing. First method is implementing the algorithm by external electronics [5.10]; this approach is useful for systems employing a standalone

external receiver, e.g. a COTS analog FM receiver, in which the demodulation process happens outside the host computer. The advantage of demultiplexing through external electronic is low computing overhead which with today's computing power is negligible. The main disadvantage is the noise introduced on individual channels. The other solution is to use custom written software for demultiplexing the data stream in host computer. This solution suits the system employing SDRs since the TDM data stream is already present in the host computer's digital domain; furthermore the SDR's and TDM's software tools can be integrated in one user friendly software package. The transmitter employs a voltage-level multiplexing process, in which an extra channel, so called frame marker is added to the channels data stream; the frame marker contain a user-selectable DC voltage which stands above all other channels. In the receiver for demultiplexing process, the demodulated data stream is checked for the channel with the largest amplitude and other channels are extracted based on the occurrence frequency of the frame marker and the user-provided number of channels. Voltage level based time division multiplexing is demonstrated with Matlab Simulations in figure 5-7; in this figure a 200KHz bandwidth is assumed for the TDM signal composed of two grounded channels and one neural channel.

In voltage-level multiplexing process, the power is traded for bandwidth; in fact the voltage-level based multiplexing process can be implemented with low-power circuits on the transmitter side; also it does not require high computing power for demultiplexing on the receiver side. However the disadvantage of this process is the bandwidth required. To have a robust demultiplexing process, the frame marker voltage level has to be substantially larger than that of other channels. However, as derived in chapter 2, the



frame marker voltage level is multiplied by the large VCO's oscillator gain in the bandwidth formula (equation 2-20). The larger the frame marker level, the larger the bandwidth and consequently the larger the receiver's additive white Gaussian noise (AWGN) as derived in the formula 2-58. Therefore the frame marker level should be tuned on the fly and it would be beneficial to have the frame marker user selectable.

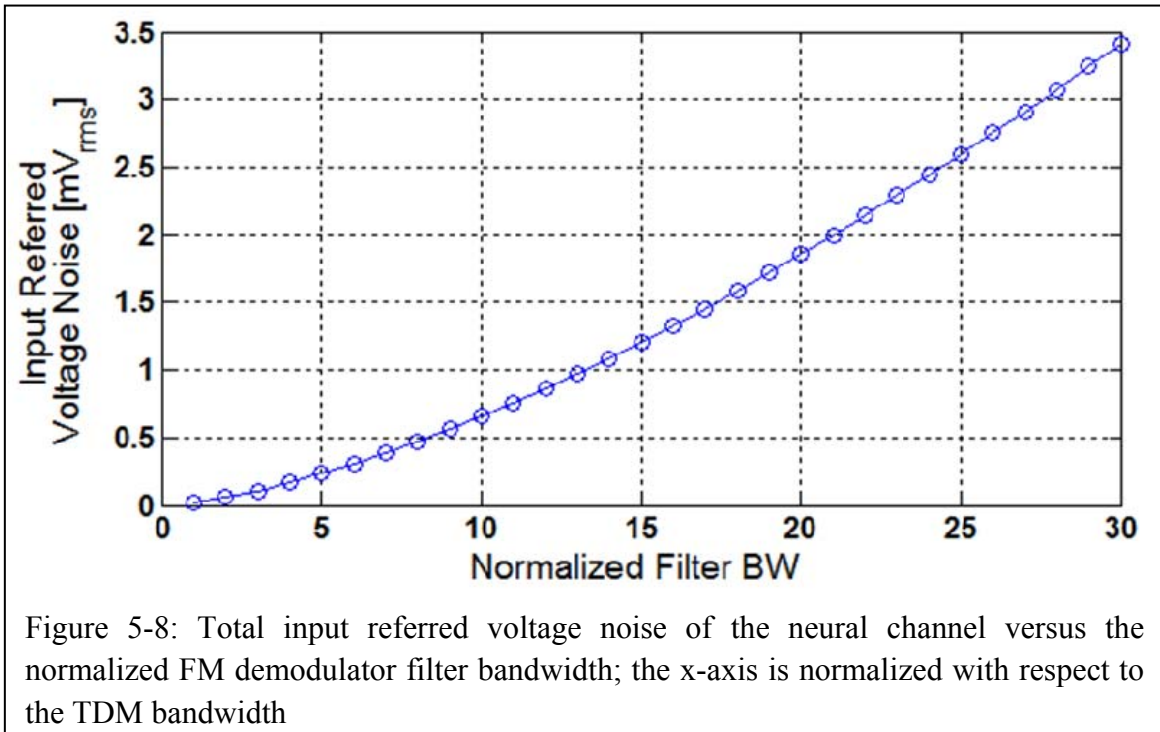
Also in chapter 2, it was shown that the power spectrum of the transmitter has a distinct part for the frame marker. If frame marker-level is too large, due to large oscillator gain of the transmitter's VCO, the receiver fails to capture the frame marker spectrum, and large amplitude noise appears instead of the constant DC voltage of the frame marker; such large noise disrupts the demultiplexing process and should be avoided by careful selection of frame marker voltage level.

The work proposed in this thesis, employs software defined radios in which the demodulator's output is in the digital domain of the host computer. The demultiplexing algorithm is implemented in a user friendly GUI program implemented in the Windows Matlab.

5.2.2. Filtering

To recover the individual neural channels with adequate SNR, the demodulated TDM signal requires two steps of filtering. The first low pass filter is applied to the FM demodulated TDM signal and the second bandpass filter is applied to the demultiplexed individual neural channels. As explained in chapter 2, the noise enters the signal path from various system nodes, and therefore it is essential to filter the TDM stream before applying the demultiplexing algorithm. In the recovered neural channel's SNR formula (equation 2-58), the last term of the denominator contains BW_{TDM}^2 ; BW_{TDM} is the bandwidth of the TDM signal as calculated in the equation 2-14. If the TDM stream is not filtered before entering the demultiplexing block, in the last term of the SNR denominator (equation 2-58), BW_{FM}^2 will replace the BW_{TDM}^2 ; BW_{FM} as calculated in the FM bandwidth formula (equation 2-20) is substantially larger than BW_{TDM} and will

lead to increased level of the receiver's additive white Gaussian noise. The total input referred voltage noise of the system versus the first stage filter bandwidth is demonstrated



in figure 5-8; in this figure the FM demodulated TDM signal is low pass filtered with varying bandwidths spanning from the transmitter's TDM bandwidth (equation 2-14) up to the FM bandwidth (equation 2-20) and normalized with respect to the transmitter's TDM bandwidth (equation 2-14). In figure 5-8, the demultiplexed neural channels are not filtered and as can be seen the input referred voltage noise increases from $23\mu\text{V}_{\text{rms}}$ to $3.5\text{mV}_{\text{rms}}$.

Filtering the TDM signal is a tedious work load for the host computer already running the demodulation, demultiplexing, and individual channel filtering. As calculated in 5.1, the output throughput of the SDR can extend to 32MB/s. At such high throughput, simple Finite Impulse Response (FIR) filters of degree less than 30 should be used to filter the TDM signal. FIR filters are known to have slow roll off characteristics,

compared to Infinite Impulse Response (IIR) of the same length. Therefore to reduce the noise outside the TDM bandwidth either a high order FIR filter (>30) should be used or the crosstalk level can be compromised by shifting the FIR filter cut off frequency to frequencies smaller than the TDM bandwidth.

After demultiplexing, band pass filtering must be applied to all the individual neural channels. In equation 2-58, all the major noise sources affect the channel SNR in the bandwidth of BW_{ch} . BW_{ch} is the bandwidth of the individual channels and for the case of neural channels, it is constant at 10KHz. Without the channel filtering, the noise sources affect the recovered neural channel's SNR in the bandwidths of BW_{TDM} (equation 2-14), or BW_{FM} (equation 2-20) which are substantially larger than 10KHz. The SNR of the recovered neural channel drops with increasing channel bandwidth with a trend, similar to the one shown in figure 5-8. With today computing power, a host computer running demodulation, TDM filtering, and demultiplexing might not be able to filter individual neural channels in realtime. Therefore the channels data can either be stored locally for offline processing, or relayed to other computers, e.g. via Ethernet, where they can be filtered in realtime.

5.3. Conclusion

In this chapter the external electronics required to recover the individual neural channels at the receiver side were discussed. Due to the large bandwidth of the transmitter's FM signal, the available commercial-off-the-shelf analog FM detectors cannot be used for FM detection purposes. Two software defined radios (NI-5660 and USRP) employed for demodulating the transmitter's TDM-FM signal during the course

of this project were introduced. Filtering the demodulated TDM signal and its impact on the recovered neural channel's SNR was discussed. Software based FM demodulation, time-division-demultiplexing, and neural channel filtering are integrated in a user friendly GUI program implemented in the Windows based Matlab environment.

5.4. References for Chapter 5

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CHAPTER 6

SYSTEM CHARACTERIZATION, RESULTS AND DISCUSSIONS

In this chapter the complete wireless multichannel neural telemetry system composed of the neural transmitter and the external electronics is characterized. The biological in-vivo experiments conducted using the proposed system are presented and finally a figure of merit is introduced to compare the state of the art wireless multichannel neural telemetry system with the proposed work.

6.1. The Neural Transmitter Assembly

The proposed multichannel wireless neural transmitter ASIC (chapter 5) is employed in two versions of the neural transmitter: single-board and double-board. These transmitter boards are essentially the same except that the single-board transmitter, figure 6-1, employs a monopole wire antenna but a 50 Ω commercial chip-antenna [6.1] is used in the double board transmitter shown in figure 6-2. The double-board microsystem is composed of 2 vertically stacked boards; the bottom board contains

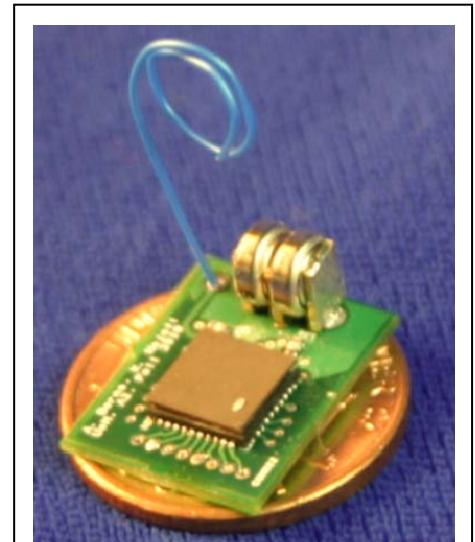


Figure 6-1: The single-board neural transmitter with monopole wire-antenna

the ASIC, two RF inductors, and batteries; and the top board houses the antenna. The two

boards of the double-board neural transmitter are connected by RF MMCX connectors [6.2]. The antenna board employs a through-hole plug (male) connector and the ASIC board uses a jack (female) surface-mount connector. The employed commercial antenna in the double-board transmitter is ANT1603-433 from RainSun which is a quarter-wavelength, miniaturized, chip-antenna with a weight of 1g and size of $16\text{mm}\times 3.1\text{mm}\times 1.65\text{mm}$. Alternatively the ANT1603-433 could be soldered on the ASIC PCB; however this approach poses two problems: 1) an increase in the area of the transmitter, due to large ground plane clearance area needed for the ANT1603-433, and 2) RF interference with the ASIC circuitry due to large transmitted antenna RF power.

Two 1.5V, silver-oxide batteries (Energizer-337 [6.3]) are used as the power source. These batteries weigh 0.13g with a diameter of 4.8mm and a capacity of 8.3mAh .

The batteries are installed on the transmitter board using custom made battery holders, made out of “quit-fit-terminals” from Keystone Electronics [6.4]. The three posts of QFT-1267, soldered on the PCB, hold the two Energizer-337 batteries in between. The PCB implemented through low

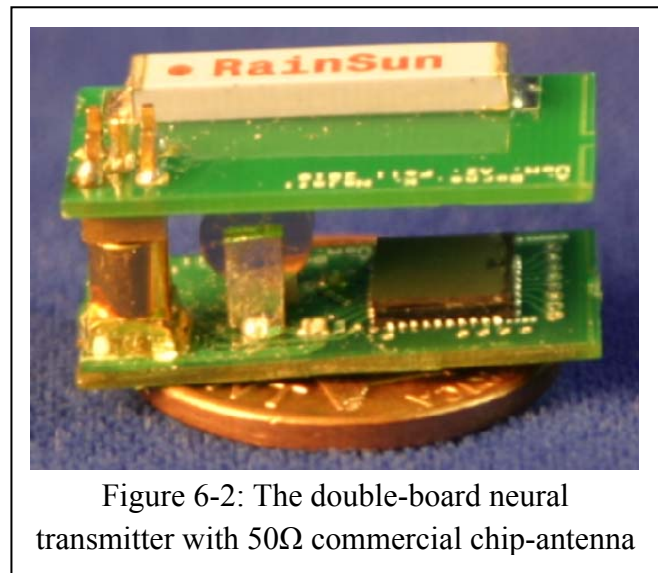


Figure 6-2: The double-board neural transmitter with 50Ω commercial chip-antenna

the mixed signal noise. The employed PQFN package weighs 0.11g including the lid and measures $6\text{mm}\times 6\text{mm}$. The two off-chip components of the RF blocks are implemented with 0402 (0.04×0.02 in) high frequency RF inductors from Taiyo-Yuden [6.6]. These small foot-print inductors have a quality factor of >22 at the ISM band of 433MHz.

The double-board neural transmitter has dimensions of $2.2\times 1.1\times 0.5\text{cm}^3$ and weighs 2.2g including the batteries. The single-board neural transmitter has dimensions of $1.57\times 1.23\times 0.5\text{cm}^3$ and weighs 1g including the batteries. Table 6-1 lists the weights of the neural transmitter components.

Component	MMCX Female	MMCX Male	RainSun Antenna	QFN Package	Antenna PCB	ASIC PCB (DB)	ASIC PCB (SB)	Battery Holders	Batteries	μPhone
Weight	0.21g	0.20g	0.26g	0.11g	0.31g	0.51g	0.39g	0.215g	2×0.13g	0.06g

Table 6-1: The neural transmitter weight table

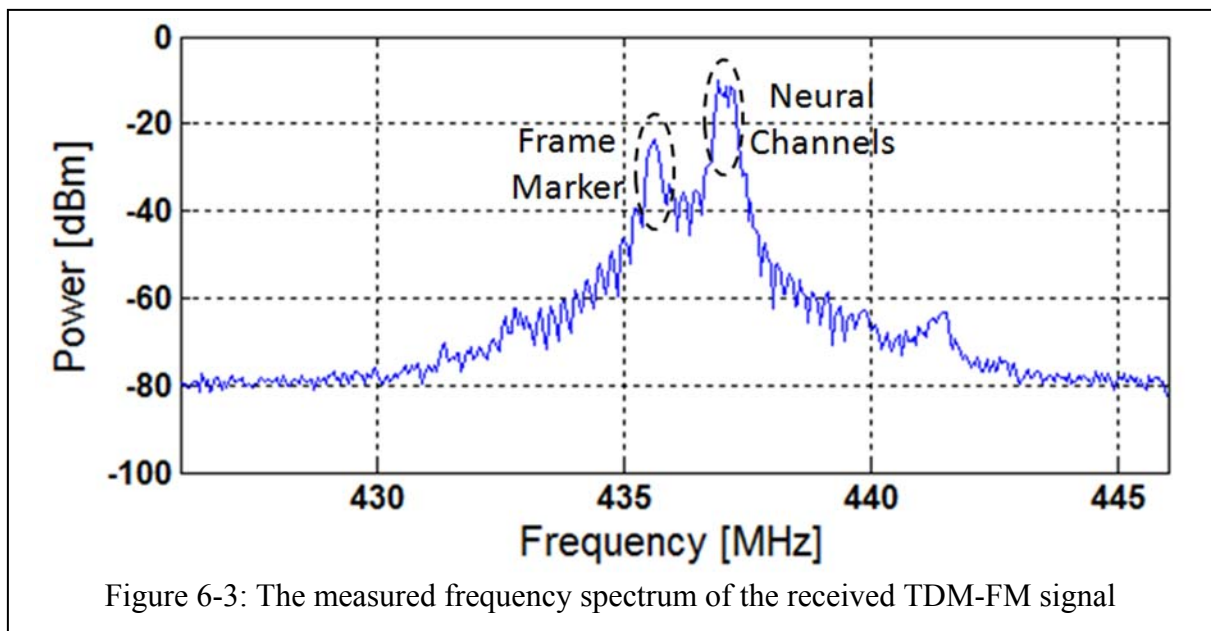
6.2. System Level Performance Characterization

The complete wireless multichannel neural system composed of the neural transmitter (chapter 4) and external electronics (chapter 5) is characterized in this section.

6.2.1. Transmission Range and Noise Performance

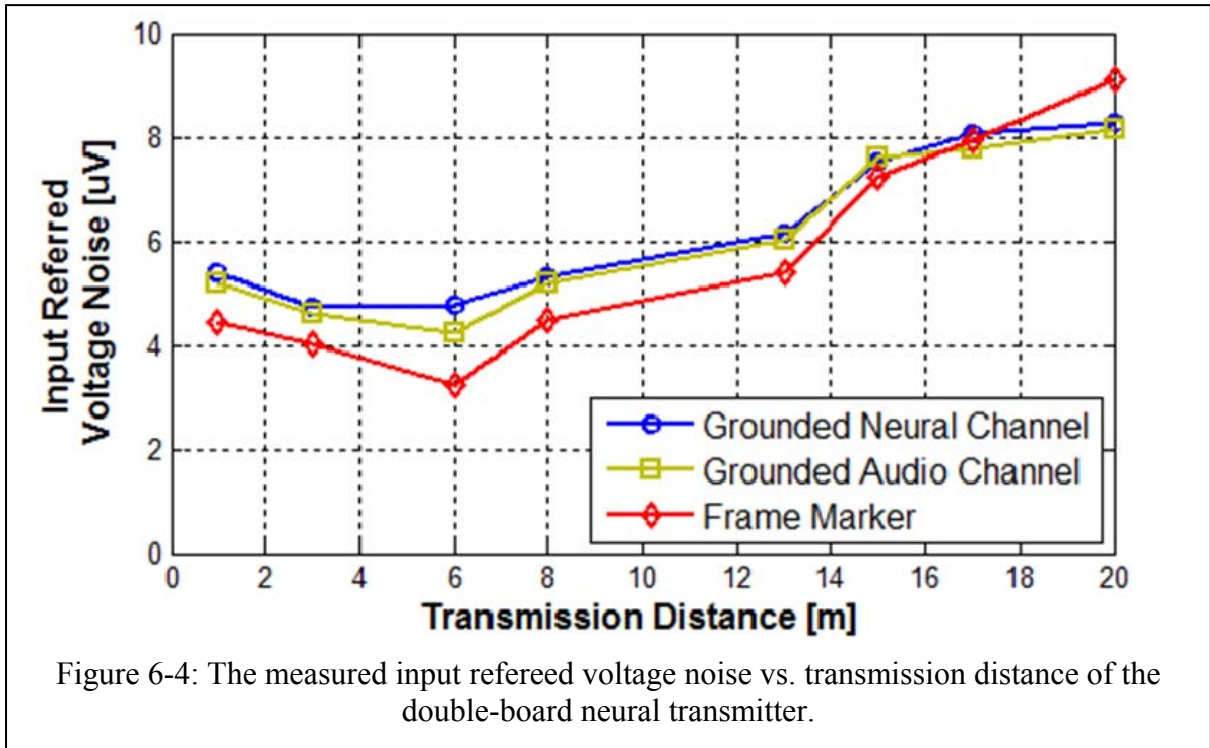
The total input referred voltage noise of the entire signal path should be less than $30\mu\text{V}_{\text{rms}}$ to distinguish the small amplitude action potentials ($50\mu\text{V}_{\text{pp}}\text{-}500\mu\text{V}_{\text{pp}}$) from the background noise. The noise performance and transmission range of the system are inter dependent parameters as the input referred voltage noise of the complete system increases with distance.

To test the transmission range of the double-board transmitter the PA was set to have $800\mu\text{W}$ of antenna power and the transmitter's 9 inputs (8-neural, 1-audio) are shorted to the ASIC's ground. Each channel is sampled with a rate of 25kSps. The PA is capable of providing the antenna with a maximum RF power of 1.5mW; however in a typical transmitter the total power should be limited to 5mW and therefore the antenna power is set at $800\mu\text{W}$ to match the total power budget. At the receiver, the Universal Software Radio Peripheral (USRP) along with custom written demodulation and demultiplexing software are used to recover the individual grounded neural channels. The



receiver employs a commercial 50Ω antenna: AX-07B from WinRadio [6.7]. AX-07B is low cost VHF/UHF antenna, with a frequency range of 100-900MHz, and a length of 16cm.

Figure 6-3 depicts the frequency spectrum of the transmitter's received signal; the received signal is the result of time-division-multiplexing and frequency-modulation of 10 channels including 9 grounded channels and one frame marker. The spectrum spreads



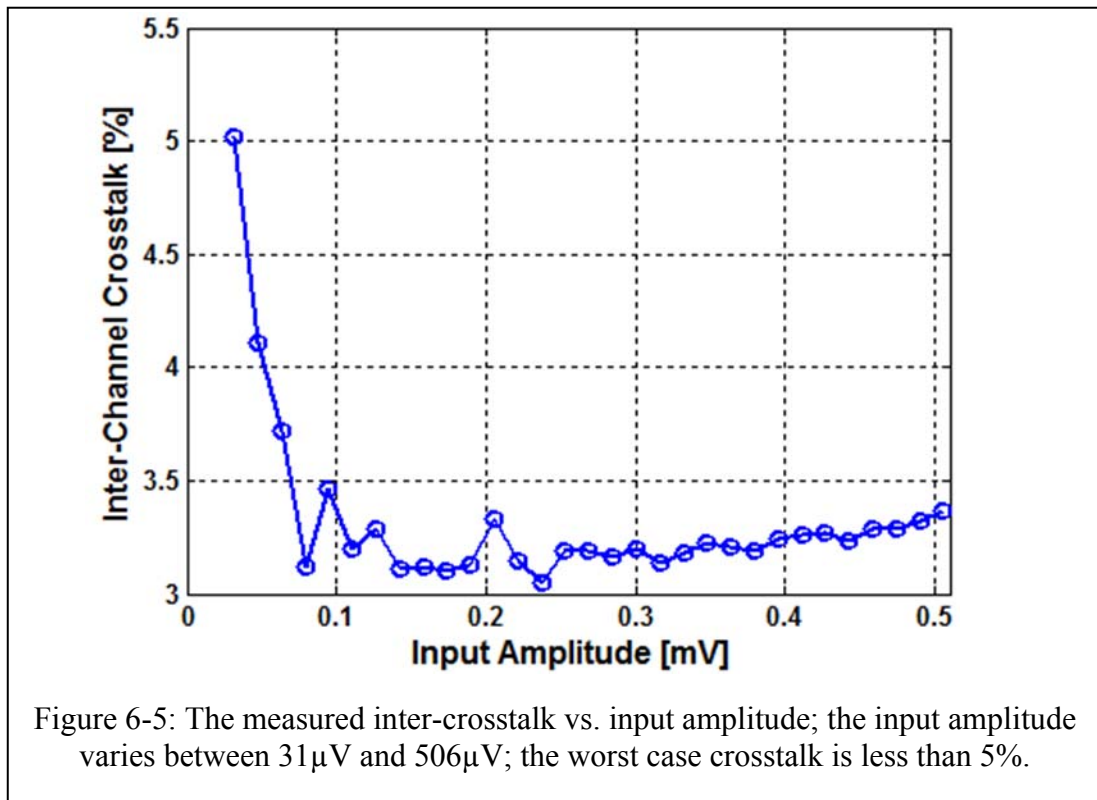
over a 2.5MHz bandwidth. The small peak of the spectrum pertains to the frame marker channel and the large peak is from all the 9 grounded channels.

To measure the transmission range and noise performance of the system, the grounded channels are recovered at the receiver and the noise of the individual channels is referred back to the system's input. Figure 6-4 shows the measured transmission range of the system. As can be seen the grounded neural channel has an input referred voltage noise of $4.74\mu\text{V}_{\text{rms}}$, $6.47\mu\text{V}_{\text{rms}}$, and $8.27\mu\text{V}_{\text{rms}}$ at transmission distances of 3m, 10m, and 20m, respectively.

The transmission range of the single-board transmitter is shorter than that of double-board transmitter due to high impedance of the monopole antenna; also the single-board transmitter's range varies by length, shape and diameter of the monopole wire antenna. On average the transmission range of the single board transmitter is limited to 2-3m for 3mW of total PA power.

6.2.2. Inter-Channel Crosstalk

Inter-channel crosstalk of wireless multichannel neural telemetry systems is one of the important performance metrics pertaining to reliability. In systems with poor inter-channel crosstalk, false action potentials are flagged on the victim channels which will lead to misleading conclusions about the brain circuit. In chapter 2 the sources of inter-channel crosstalk are discussed along with their solutions employed in the proposed system. Figure 6-5 depicts the inter-channel crosstalk of the complete system measured at a distance of 3m. In this test the input signal to the “aggressor” channel is a sinusoid at

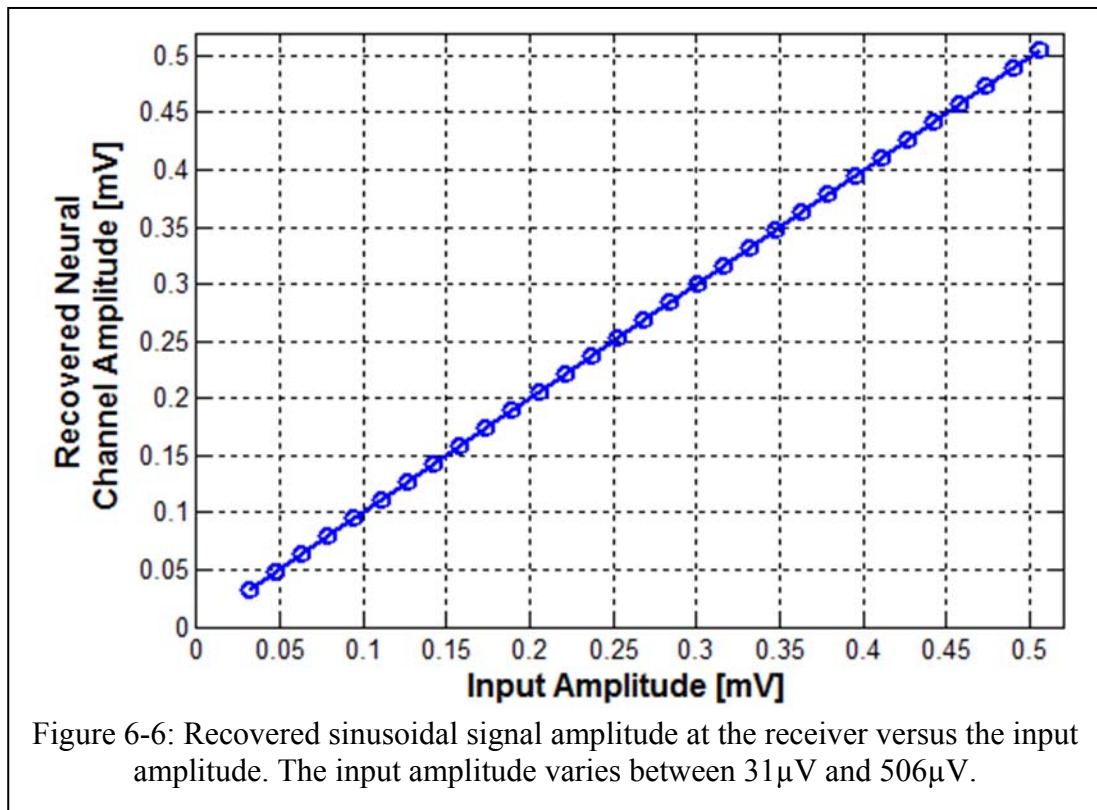


1KHz with an amplitude varied between $31\mu\text{V}$ and $506\mu\text{V}$. The inter-channel crosstalk is calculated in frequency domain. For input amplitudes less than $100\mu\text{V}$ due to small signal

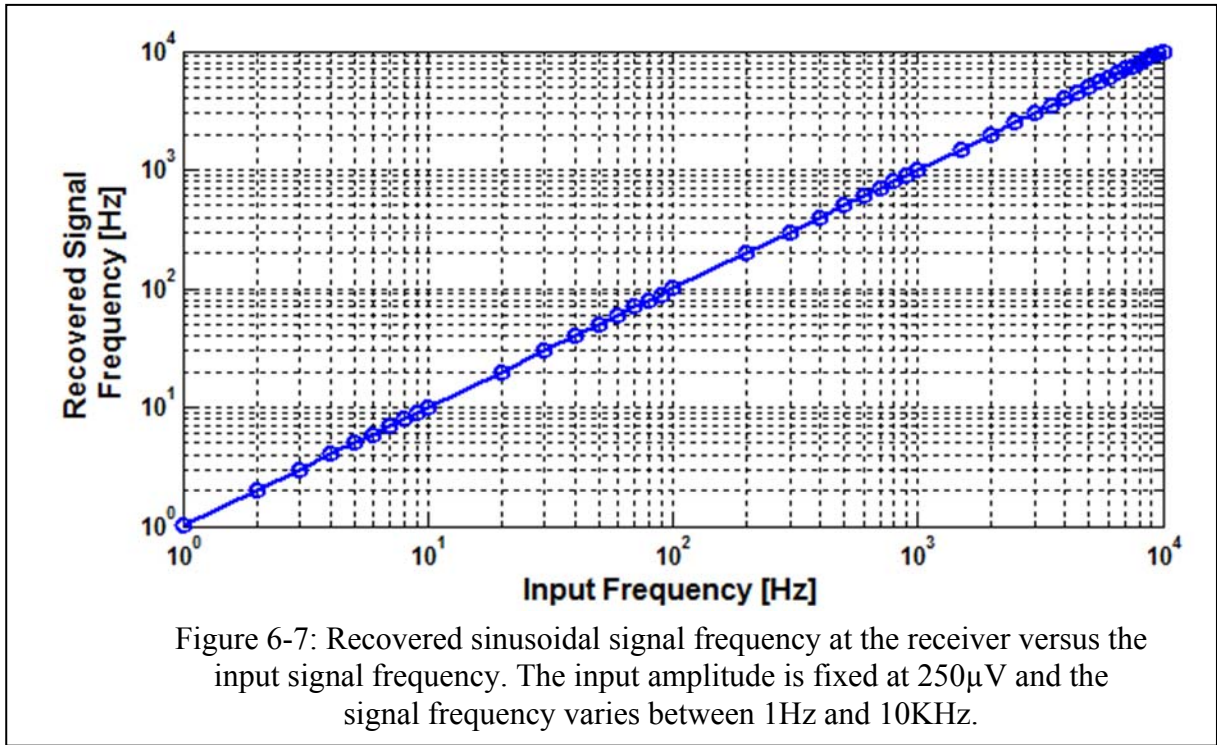
power the background noise also contributes to the calculated crosstalk. Therefore the real crosstalk of the system is less than 3.5%.

6.2.3. Action Potential Integrity

The action potential integrity refers to the similarity between the input action potential waveform and the wirelessly recovered neural signal at the receiver side. This parameter depends on the distortion introduced by the overall signal path. To have high correlation between the input action potential and the recovered one, the system should faithfully recover the input amplitude and frequency. Figure 6-6 shows the recovered



sinusoidal signal amplitude at the receiver versus the sinusoidal input amplitude. As can be seen the system transfer function is perfectly linear for all the input amplitudes varying between $31\mu\text{V}$ and $506\mu\text{V}$. Figure 6-7 shows the recovered signal frequency versus the



applied sinusoidal signal frequency. In this test the input signal varies between 1Hz and 10KHz with its amplitude fixed at $250\mu\text{V}$.

Figure 6-8-a depicts the averaged recovered action potentials for various signal amplitudes. For each data points 100 action potentials are averaged. The peak to peak amplitude of the input neural signal varies between $62\mu\text{V}_{pp}$ and $1012\mu\text{V}_{pp}$. Figure 6-8-b shows the calculated correlation of the recovered neural spikes to the input action potential for the two cases: *i*) benchtop, in which the signal generator is directly connected to the input of the neural transmitter and, *ii*) in-vitro, in which the signal generator is connected to the platinum electrode immersed in the saline solution; the neural transmitter is connected to the Michigan probes [6.8] which are used to pick up the action potential signals from the saline solution. As can be seen in figure 6-8-b for all the action potential amplitudes from $62\mu\text{V}_{pp}$ to $1012\mu\text{V}_{pp}$ the correlation between the input action potential and the wirelessly recovered action potential is larger than 95.5%.

And finally figure 6-9 is the wirelessly recorded action potential superimposed on the input signal to show the high fidelity of the signal path.

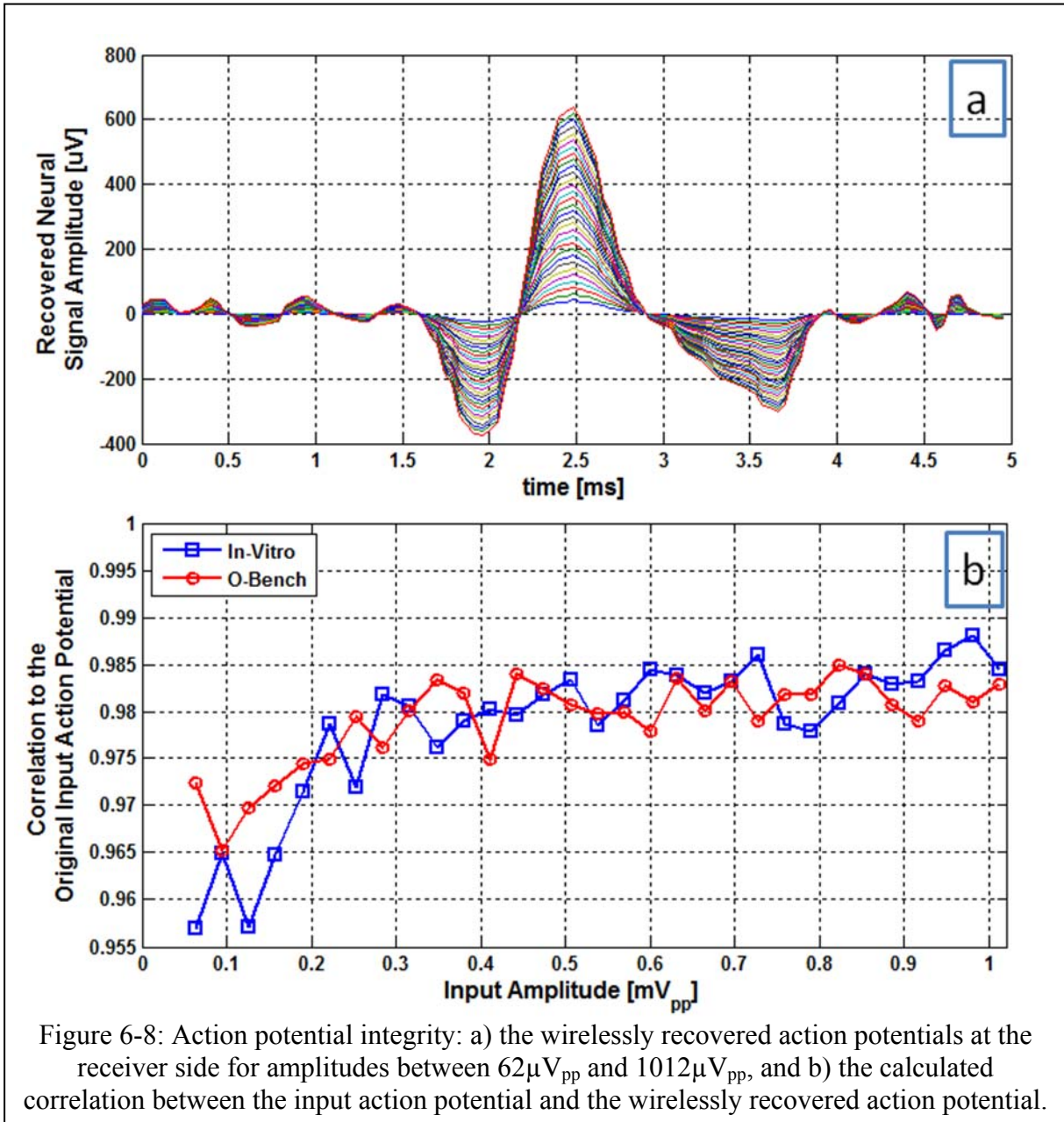
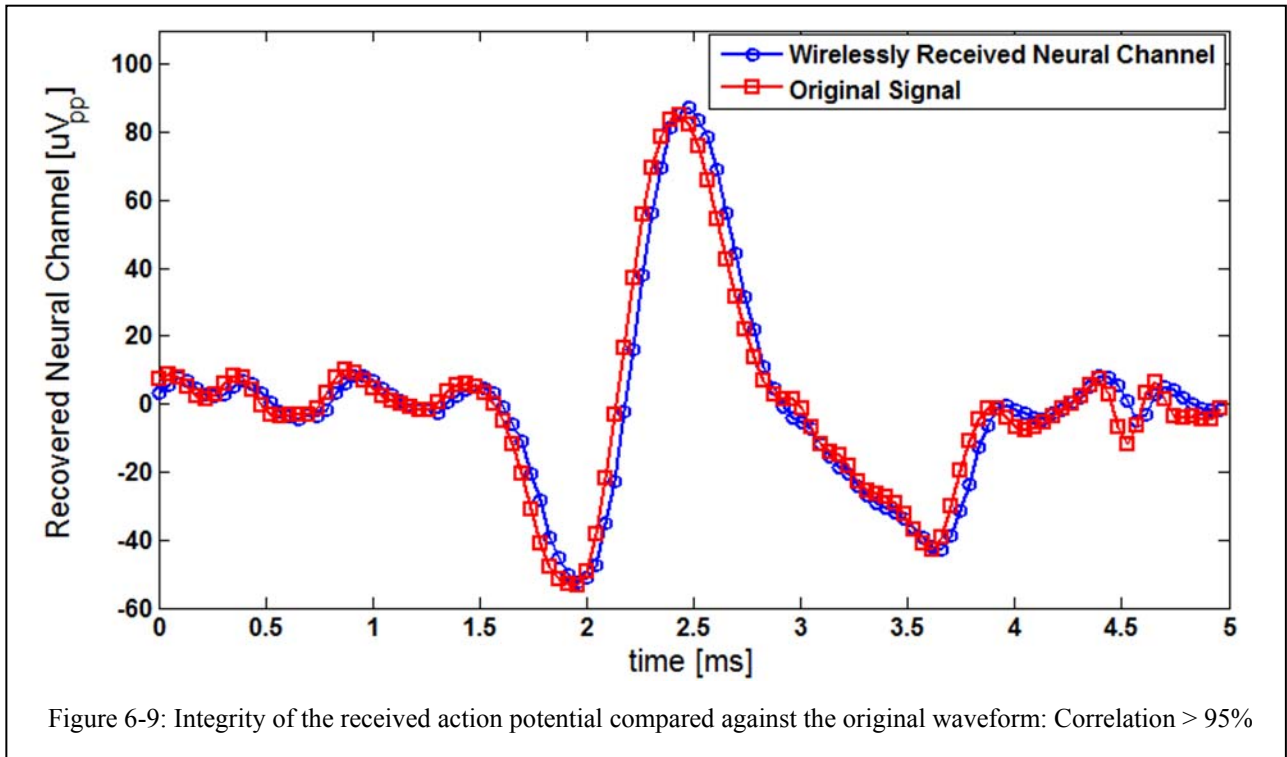
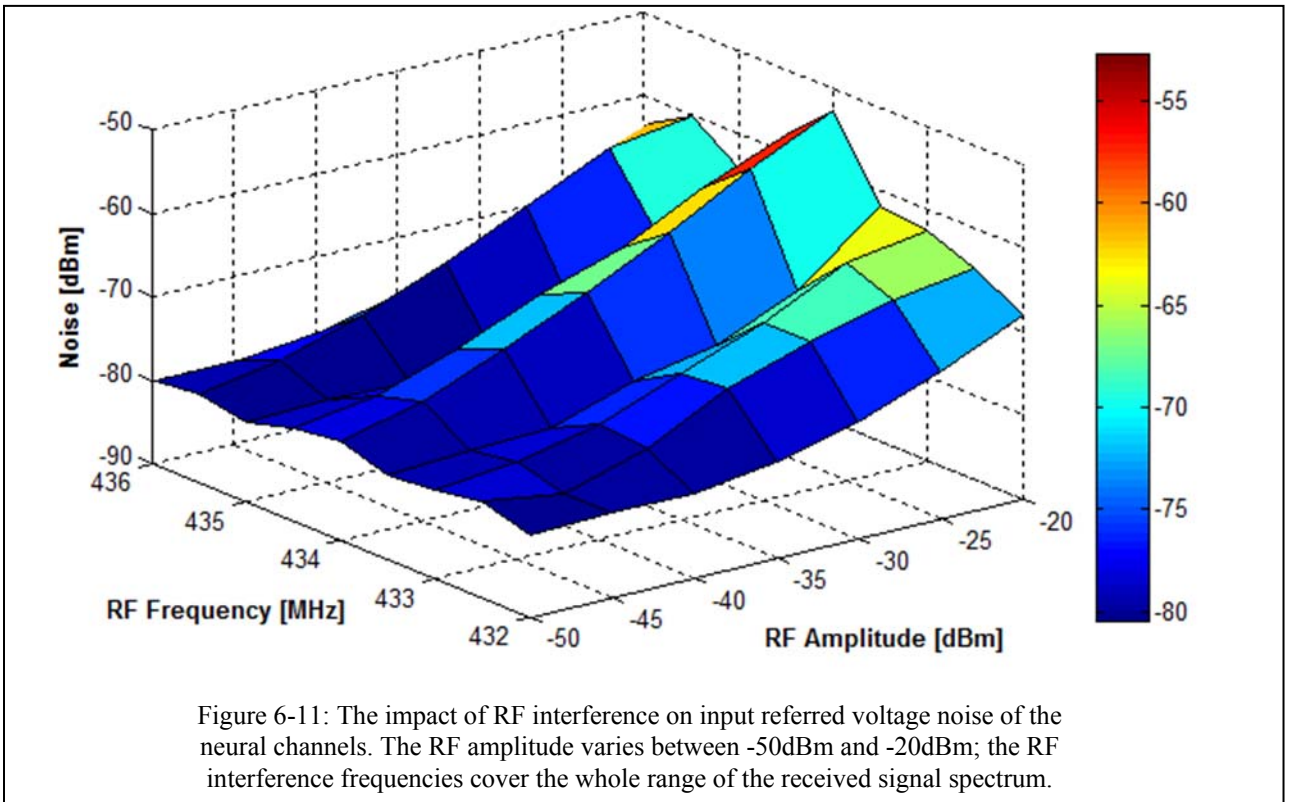
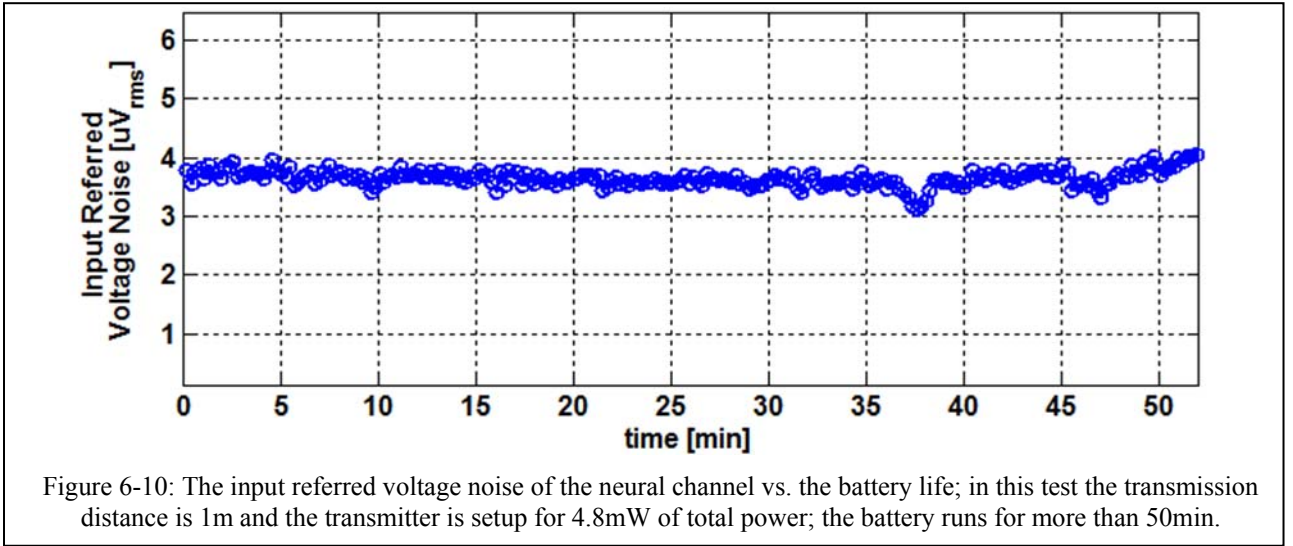


Figure 6-8: Action potential integrity: a) the wirelessly recovered action potentials at the receiver side for amplitudes between $62\mu V_{pp}$ and $1012\mu V_{pp}$, and b) the calculated correlation between the input action potential and the wirelessly recovered action potential.



6.2.4. Battery Life

To test the battery life the transmitter is setup to burn 4.8mW of total power. The receiver's antenna is positioned 1m away from the transmitter and the input referred voltage noise of the neural channels are calculated every 10s. Two Energizer-337 held by the custom made battery holders provide the power to the microsystem. Figure 6-10 depicts the input referred voltage noise of the neural channel versus time. The battery life is about an hour which afterward the frame marker is not demodulated correctly and therefore the demultiplexing process fails.



6.2.5. RF Interference

To test the system sensitivity against RF interference, the receiver antenna was positioned equidistant from the neural transmitter and a 50Ω commercial antenna

connected to an RF signal generator. A single tone RF signal with varying amplitudes (-50dBm to -20dBm) was swept across the bandwidth of the received signal spectrum. The input referred voltage noise of the grounded neural channels was calculated for each data point. The power of the neural channel noise is shown in figure 6-11. For RF interferences with power larger than -20dBm the demultiplexing process was disrupted at the receiver. The impact of the RF interference on the total noise was strongest at the middle of the received signal bandwidth.

6.2.6. Figure of Merit

To compare the wireless neural telemetry systems, an FOM is defined as the reciprocal of the power spent on broadcasting one channel over one meter distance. The state-of-the-art wireless multichannel neural transmitters are compared in table 6-2 and the proposed microsystem has the highest FOM compared to all research and commercial systems.

	Neural Channels	Weight	Dimensions (mm ³)	Battery Life time	Trans. Range	Power (mW)	Telemetry Frequency	FOM [W/m] ⁻¹
This Work	8/9	2.2g	11.3×22×5	1hr	20m	5	433MHz	3.2×10 ⁴
Harrison, [6.9]	2/4	0.79	9×13×5	2hrs	2m	2.64	920MHz	0.152×10 ⁴
Schregardus, [6.10]	1	1.1g	12×5×8	20hrs	4m	14	480MHz	0.029×10 ⁴
TBSI, W5 [6.11]	5	2.7g	15.5×11×5	3.5hrs	4m	32.45	3.05GHz	0.062×10 ⁴
TBSI, W16[6.11]	15	4g	16×17.2×8	5.5hrs	4m	32.45	3.05GHz	0.185×10 ⁴
TBSI, W32[6.11]	31	4.8g	17×19×8	5hrs	4m	32.45	3.05GHz	0.382×10 ⁴
TBSI, W64[6.11]	62	4.8g	15×20.5×12	5hrs	4m	32.45	3.05GHz	0.764×10 ⁴

Table 6-2: The comparison table; the FOM is defined as the reciprocal of the power spent on broadcasting one channel over one meter distance: $\left(\frac{Power}{N_{ch} \times R_{TX}}\right)^{-1}$

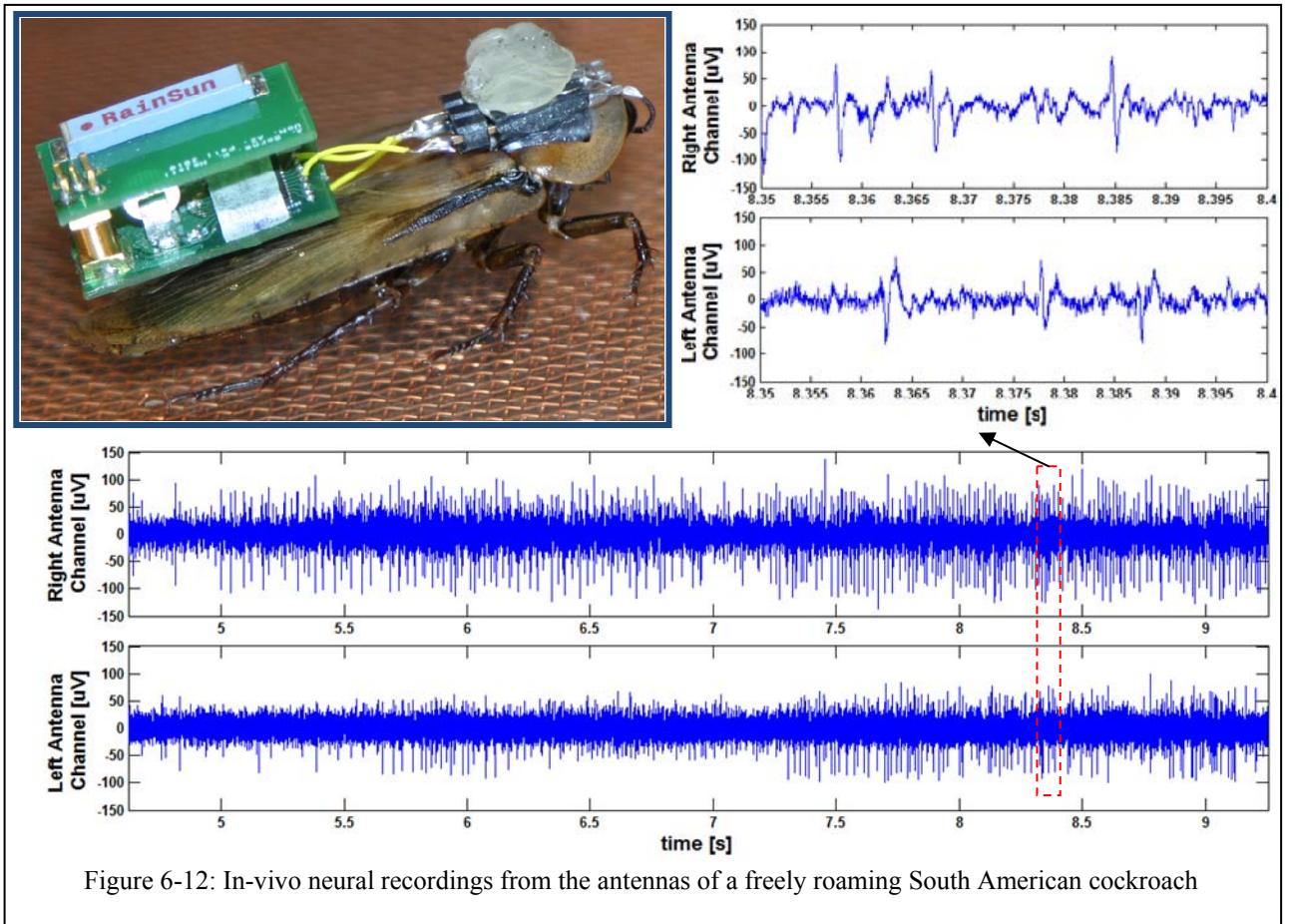
6.3. Biological Test Results

6.3.1. Mobile South American Cockroach

Two in-vivo experiments were conducted in collaboration with Backyard Brains [6.12] on the mobile South American cockroach: *i)* recording from the antennas, and *ii)* recording from the Femur sections of the rear legs.

For antenna recording, the cockroach antennas were cut in half and the recording electrodes were inserted in hollow tubes of the antennas. The electrodes were coated silver wires (gauge-38) with their tips exposed. To establish reliable connection the wires were glued to the outer body of antennas using epoxy. The other ends of silver wires were wire wrapped and soldered to a 3-pin board to board connector. The third pin of the connector was used for the reference electrode. A silver wire was inserted in the back of the cockroach between the wings and glued down with epoxy to function as the reference signal.

Two out of the eight available channels of the neural transmitter were connected to the cockroach connector through 30-gauge wires, while the rest of neural channels were grounded. Figure 6-12 depicts the recording from the cockroach's antennas. During this experiment the cockroach was awake and mobile inside a Faraday cage; the receiver antenna was also located inside the cage. The Faraday cage was merely used to limit the movement of the cockroach and was not grounded. In this experiment the left and right antennas were recorded for 12.5min and the wirelessly recovered neural channels were of high quality as shown in figure 6-12.



As can be seen in figure 6-12, the recorded neural signals are smaller than $200\mu\text{V}_{pp}$, and there is almost no visually noticeable crosstalk between the left and right antennas. Furthermore the small input referred voltage noise of the system helps in recovering action potentials with small amplitude ($<50\mu\text{V}_{pp}$).

In second neural recording experiment, the Femur sections of the cockroach legs were inserted with silver wires. The challenge was to establish a reliable connection to the left and right legs nerves as the cockroach moved. The neural interface of the legs is shown in figure 6-13-a. The reference electrode was inserted in the back between the wings as in the antenna recording experiment. Figure 6-13-b shows the cockroach with the neural transmitter recording from the left and right legs Femurs.

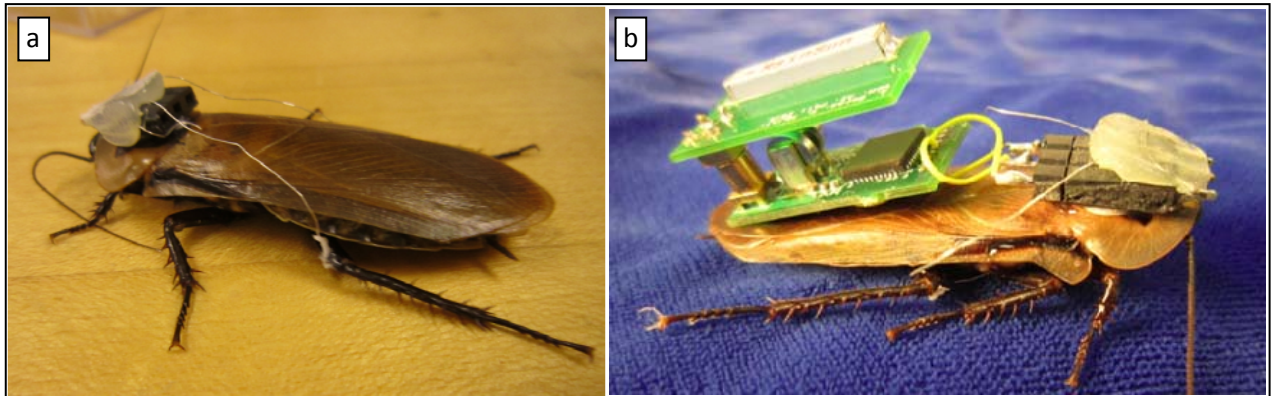


Figure 6-13: a) the neural interface to the cockroach legs Femurs, b) the cockroach and neural transmitter (courtesy of Dr. Timothy Marzullo)

In second neural recording experiment, the Femur sections of the cockroach legs were inserted with silver wires. The challenge was to establish a reliable connection to the left and right legs nerves as the cockroach moved. The neural interface of the legs is shown in figure 6-13-a. The reference electrode was inserted in the back between the wings as in the antenna recording experiment. Figure 6-13-b shows the cockroach with the neural transmitter recording from the left and right legs Femurs.

The neural recording from cockroach's legs was conducted for 20min. In this experiment neural activity of muscles are recorded and consequently the magnitude of recorded action potentials is larger than the neural signals recorded from the antennas. Two different types of neural activities were detected on the recorded neural channels: synchronized neural activity and alternative spiking activity. In the synchronized neural activity both legs have similar action potential waveforms as shown in figure 6-14. In alternative spiking activity shown in figure 6-15 the neural activities on the left and right legs alternate with a frequency of about 4Hz which can be attributed to the speed of cockroach movement.

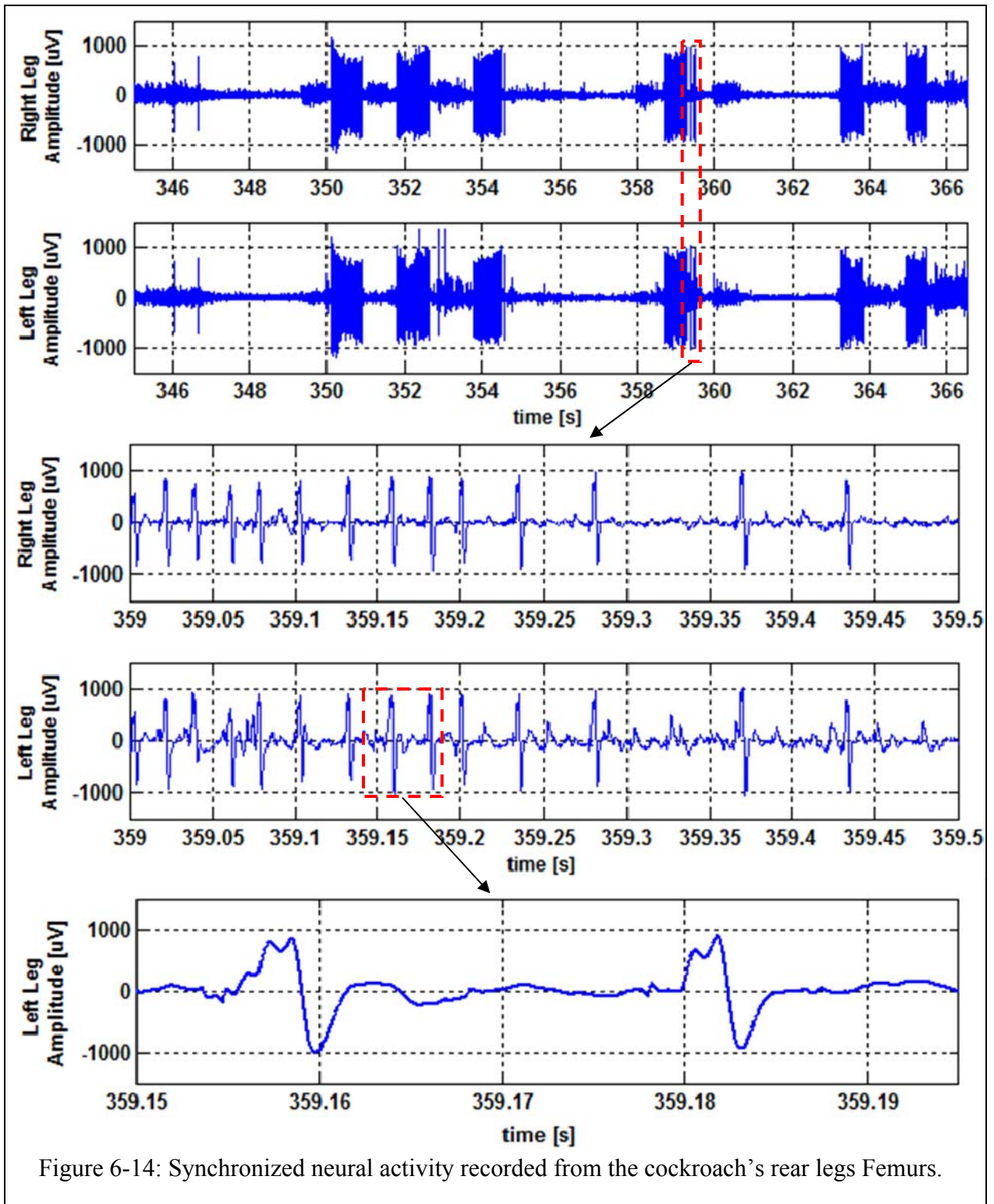


Figure 6-14: Synchronized neural activity recorded from the cockroach's rear legs Femurs.

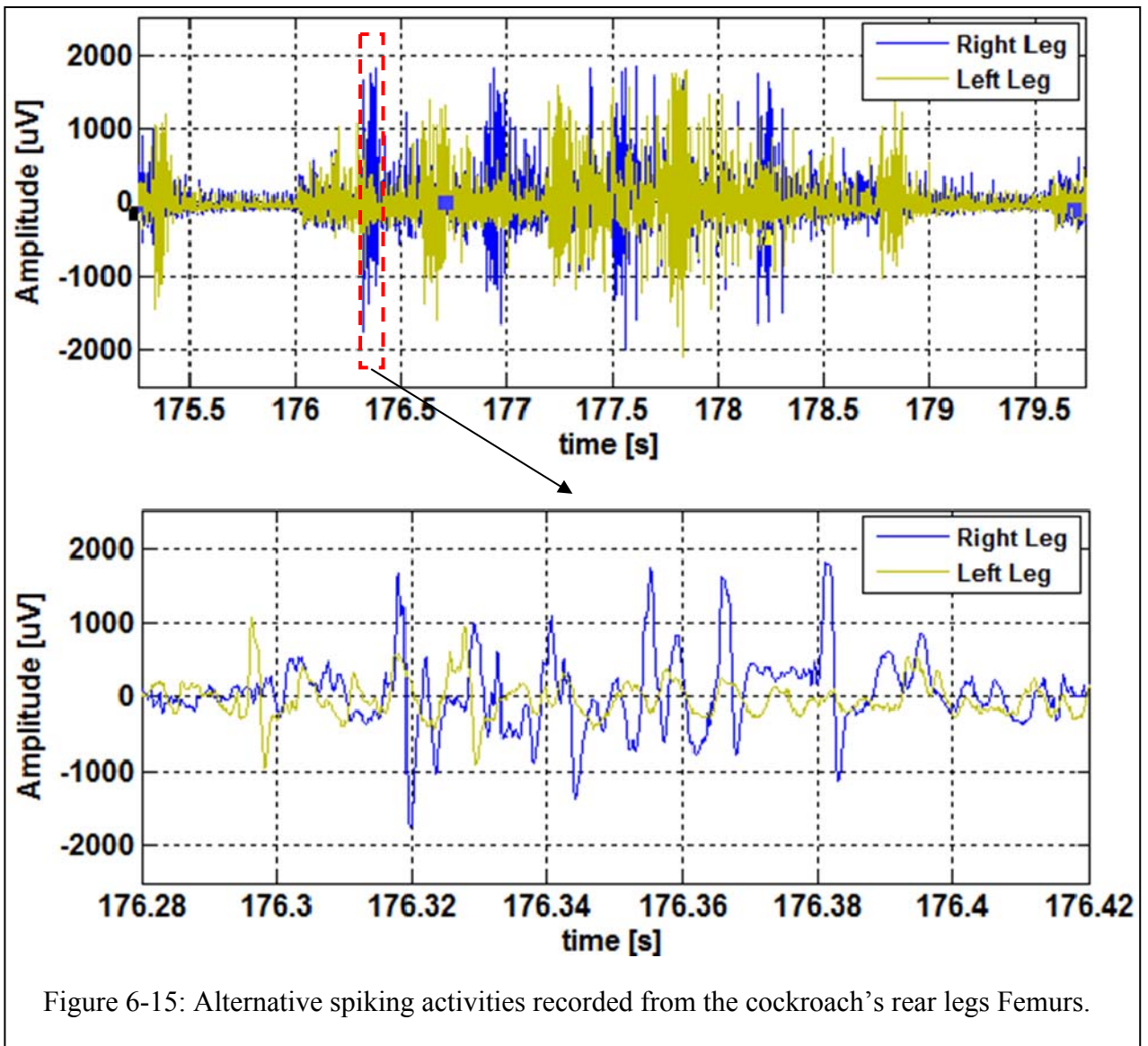


Figure 6-15: Alternative spiking activities recorded from the cockroach's rear legs Femurs.

6.3.2. Recording from the Hippocampus of an Awake, and Mobile Rat

The proposed multichannel, wireless neural recording system was employed to record from the extracellular electrodes implanted in the hippocampus of an awake and mobile rat. Figure 6-16 depicts the setup for wireless neural recording. The in-vivo recording experiment was conducted for half an hour during which the neural spikes on eight channels were wirelessly recovered. The receiver antenna was located at a distance of 1m from the test subject. The animal ground was connected to the ASIC ground and all the channels were referenced with respect to the ASIC ground. The eight recovered neural channels, demonstrated

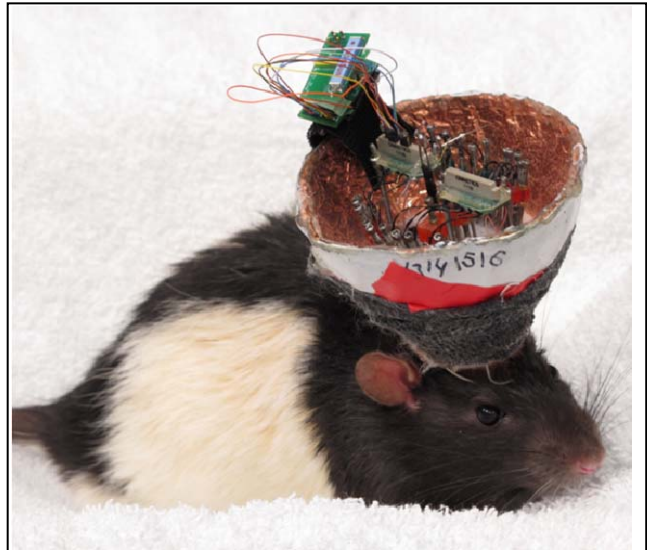


Figure 6-16: Wireless neural recording from the hippocampus of an awake and mobile rat (Courtesy of Prof. Gina Poe, Department of Molecular and Integrative Physiology, University of Michigan, Ann Arbor)

in figure 6-17 were filtered from 300Hz to 15kHz using a digital Chebyshev II bandpass filter with an order of 10.

In the second set of experiment, the proposed ALFS neural amplifier (NA_V1) was employed separately to record from the hippocampus of the same rat in anesthetized state. The neural amplifier output was sampled by a USB-based data acquisition card (DAQ) with a data sampling rate of 200kSps, and an LSB of 7.63 μ V. The recorded signal was filtered offline from 300Hz to 15kHz using a digital Chebyshev II bandpass filter with an order of 10. Fig. 6-18 shows the input referred captured waveform.

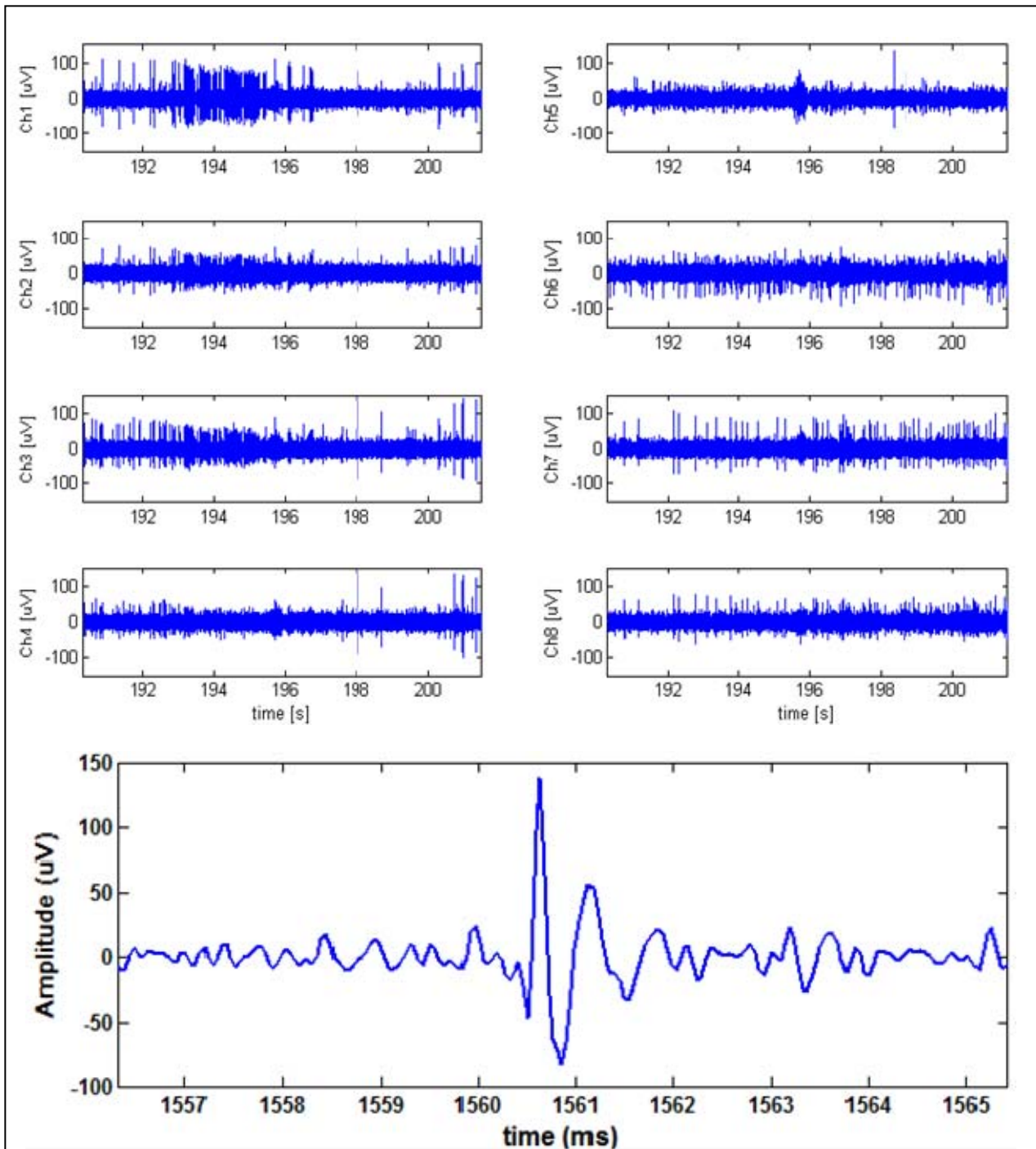


Figure 6-17: Eight neural channels recorded wirelessly from the Hippocampus of an awake and mobile rat (Courtesy of Prof. Gina Poe, Department of Molecular and Integrative Physiology, University of Michigan, Ann Arbor)

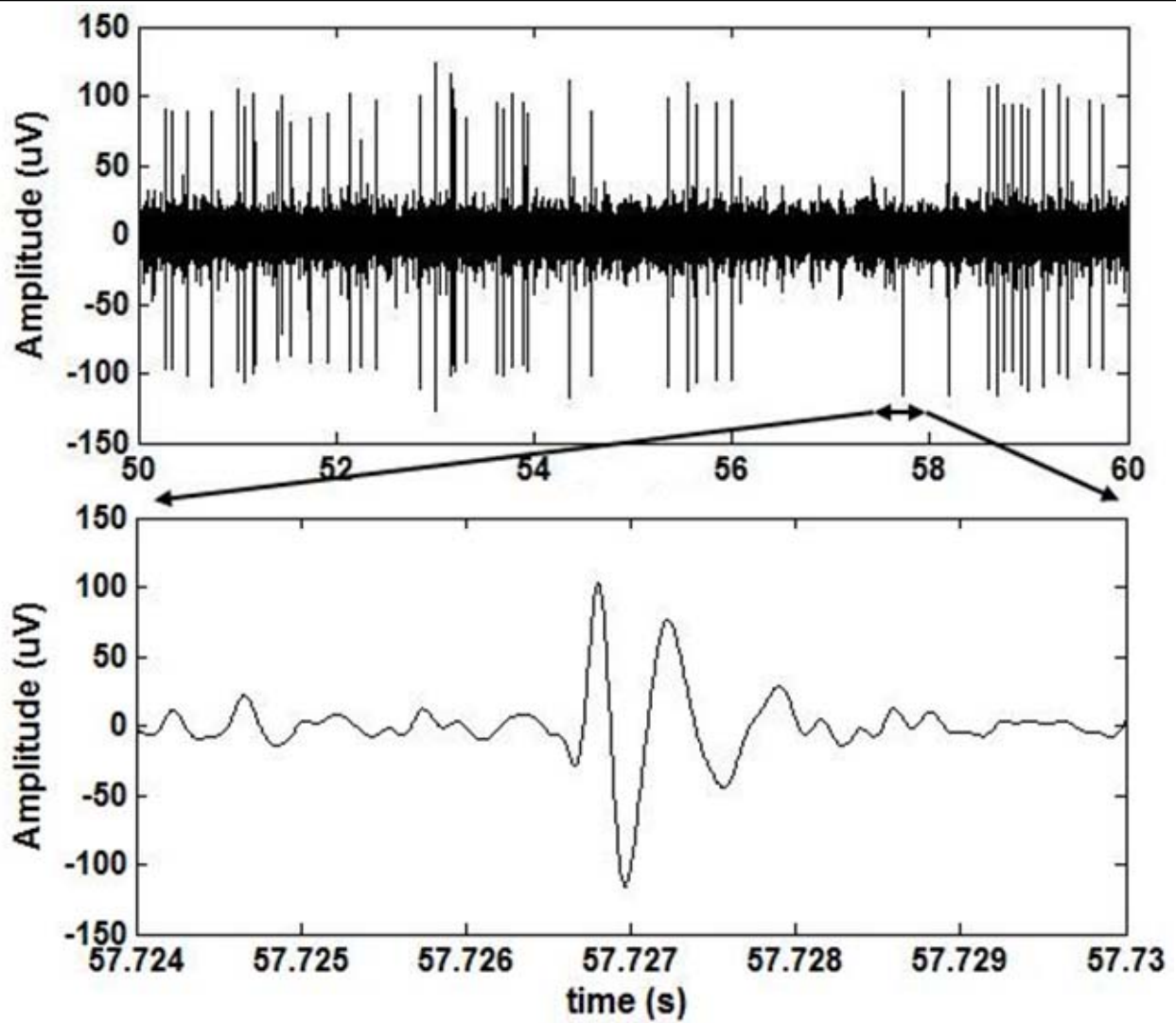


Figure 6-18: The input referred neural channel recorded from the hippocampus of an anesthetized rat using the active-low-frequency-suppression neural amplifier (Courtesy of Prof. Gina Poe, Department of Molecular and Integrative Physiology, University of Michigan, Ann Arbor)

6.4. Conclusion

The proposed wireless multichannel neural telemetry system is characterized in this chapter; it weighs 2.2g including the batteries and has the size of $2.2 \times 1.1 \times 0.5 \text{cm}^3$. The battery life is almost an hour for the transmitter setup for $800 \mu\text{W}$ of antenna power. The system has an input referred voltage noise of $4.74 \mu\text{V}_{\text{rms}}$, $6.47 \mu\text{V}_{\text{rms}}$, and $8.27 \mu\text{V}_{\text{rms}}$ at transmission distances of 3m, 10m, and 20m, respectively. The inter-channel crosstalk is less than 3.5%. At 1m distance the wirelessly received neural spike integrity is more than 96.5% for input amplitudes: $63 \mu\text{V}_{\text{pp}}$ - $506 \mu\text{V}_{\text{pp}}$. The system is immune to single-tone RF interferences up to 15dB lower than the main signal received power. A figure of merit is defined to compare the wireless neural telemetry systems and the proposed system FoM is an order of magnitude higher than the state of the art systems. The developed biotelemetry system has been successfully employed in three different in-vivo experiments: *i*) neural recordings from the antennas of a freely moving South American cockroach, *ii*) intramuscular EMG recordings from the femur sections of a freely moving South American cockroach's rear legs, and *iii*) extracellular neural recordings from the hippocampus of an awake and mobile rat.

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CHAPTER 7

CONCLUSION, CONTRIBUTIONS, AND FUTURE WORK

To understand the underlying mechanism of central nervous system, single-unit action potentials of the test subject need to be monitored continuously using minimally invasive multichannel neural recording devices. Small animal subjects such as Zebra Finch song birds have been established as the basis for neuroscience studies due to many parameters such as easy laboratory breeding, identified brain pathways of song learning and motor skills, etc. Due to small size and limited carrying capability of small test subjects the wireless neural transmitter should be limited in size ($<1\text{cm}^3$) and weight ($<1\text{g}$). These physical specifications constraint the power consumption of the microsystem and to address them in most published works the reliability and robustness of the system are compromised. This research project sought to address the conflicting requirements of low power and reliability. The two major achievements of this research are first identification of obstacles encountered in reliable wireless multichannel neural recordings and high level system modeling to address the reliability criteria at the block level. The second and most important achievement is design, development and characterization of reliable, low-power circuit blocks employed in the developed single-chip, light-weight, small-size, low power and reliable wireless multichannel neural telemetry system. The specific contributions of this thesis are:

7.1. Research Contributions

7.1.1. Theory

- By employing the preliminary developed biotelemetry systems in various in-vivo neural recordings, the system criteria for reliable neural recordings were identified; to meet these criteria, the overall system's signal path is modeled at the block level in an analytical tool: signal path co-optimization (SPCO). Using SPCO, the high level block parameters are optimized to meet the limited power-bandwidth budget.

7.1.2. Design and Development

- Developed a discrete board level 16-channel, wireless neural recording device; this transmitter was successfully employed in various in-vivo neural recordings from zebra finch, and guinea pigs [7.1].
- Designed and developed the individual integrated circuit blocks employed in high performance wireless biotelemetry systems. These circuit blocks address the conflicting requirements of low-power and reliability. The performance metrics of these blocks were fully characterized and compared with state of the art systems [7.2].
- Designed and developed a light-weight, small-size, low-power, long-range, and reliable wireless multichannel neural recording microsystem. In this microsystem the conflicting requirements of low power and reliability are addressed both at the architectural and circuit levels. To compare performance metrics representing

state of the art wireless biotelemetry systems, a figure of merit (FoM) is defined as reciprocal of the power spent on broadcasting one channel over one meter distance. The proposed microsystem has an order of magnitude higher FoM than that of all other research and commercial systems.

- Designed and developed a complete wireless neural telemetry system composed of the wireless neural recording microsystem and the external electronics along with custom written software.

7.1.3. Testing and Characterization

- Developed an automated testing platform to characterize the individual circuit blocks. The complete wireless neural telemetry system was tested and performance metrics pertaining to reliability were extensively characterized. The proposed system has been successfully used for in-vivo neural recording experiments from a freely roaming South American cockroach, and from an awake and mobile rat.

7.2. Future Work

Despite the contributions of this thesis toward advancing wireless multichannel biotelemetry systems intended for reliable neural recordings from small test subjects, there are still ample areas requiring further research and development. Some suggestions for future works are as follows:

7.2.1. Multi-Transmitters Neural Recording Systems

To understand the impacts of social interaction on brain development, it is desired to monitor multi test subjects simultaneously as they interact in a semi-natural habitat. Currently commercial devices [7.3] provide the neuroscience community with fully analog systems capable of simultaneous wireless neural recording from two test subjects. The disadvantages of these systems are: *i*) varying noise performance between test subjects as the occupied frequency spectrums have different RF interferences, *ii*) high system cost as each test subject requires a separate receiver, and *iii*) the limited number of test subjects imposed by the system architecture.

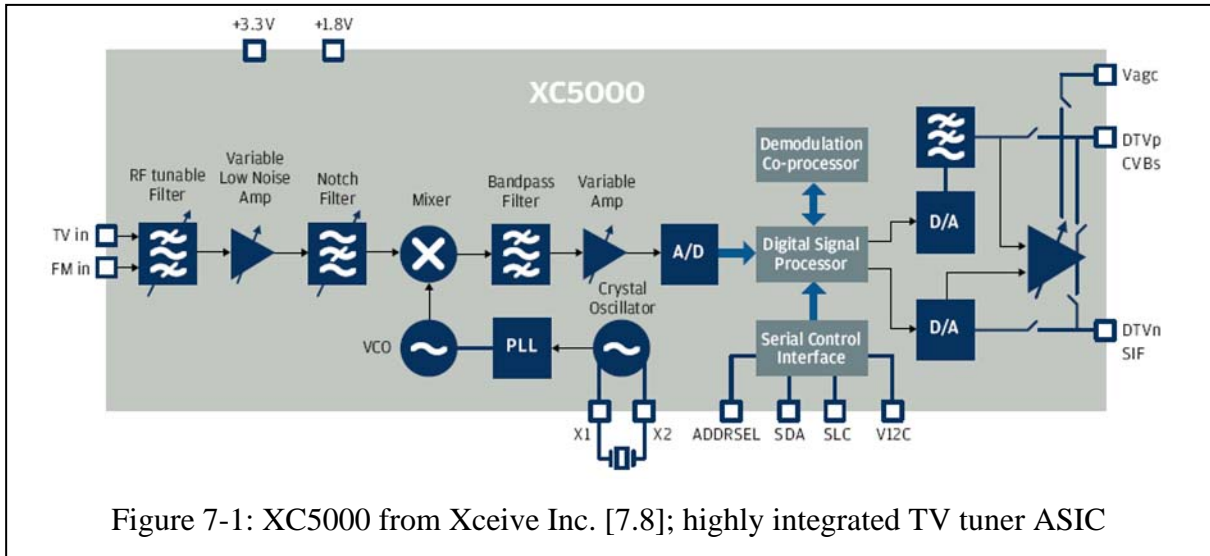
To address these issues it is possible to use digital telemetry systems. In each transmitter the time-division-multiplexed signal containing the neural channels, is digitized and encoded by code-division-multiplexing-access (CDMA) encoder. The digitized TDM data is coded at a higher frequency. The code is pseudo-randomly generated by each transmitter, and the single receiver generates the same code for each transmitter, and correlates the received signal with that code to extract the digitized time division multiplexed signal. Employing a combination of code-division-multiplexing-access (CDMA) [7.4] and ultra-wideband (UWB) [7.5] communication links, multi test subjects can use the same frequency band. In this scheme the number of transmitters is bounded by the available bandwidth of the UWB communication link and it is theoretically feasible to have up to 14 transmitter units sharing the same bandwidth.

7.2.2. Fully Integrated Neural Telemetry Microsystems

To further reduce the size and weight of the wireless neural recording microsystem, a higher level of integration is required. In the proposed microsystem it is feasible to integrate the two off-chip inductors on-chip. The proposed system dimension is bounded by the antenna size however by employing the 2.4GHz frequency band miniaturized chip-antenna can be used. As an example AN3216 [7.6] dimensions are $3.2 \times 1.6 \times 0.9 \text{mm}^3$ and has a smaller footprint than the proposed ASIC. At 2.4GHz the RF blocks inductors can be implemented on-chip with a quality factor of greater than 15 [7.7]. Furthermore by this high level of integration the ASIC chip can be wirebonded to the flexible PCB using the chip-on-board technology. At this high level of integration, other than ASIC the flexible PCB houses only the off-chip batteries and consequently the whole microsystem can be as small as $4 \times 4 \times 5 \text{mm}^3$ and have a weight of less than 0.7g.

7.2.3. Low Cost Wireless Multichannel Neural Telemetry Systems

Currently a complete wireless multichannel neural telemetry system costs about 15,000\$. To make these systems available to the neuroscience community it is desired to keep the cost of the overall system less than 500\$. In the proposed system the cost is limited by the employed receiver. However by implementing the receiver using consumer electronics it is possible to have the receiver cost less than 100\$. The XC5000 chip from Xceive Inc. [7.8] is shown in figure 7-1. XC5000 is highly integrated, ultra small ASIC designed for TV Receivers. It has a frequency range of 42-864MHz with a noise figure of 5dB. By reprogramming the on-chip DSP of XC5000 it can be used for demodulation of the received TDM-FM transmitter's signal and Demultiplexing/filtering of neural



channels. Furthermore it has been widely used in commercial off the shelf USB-based TV tuners which can be purchased for less than 100\$. Consequently by using this receiver it is possible to reduce the cost of the overall system and improve the noise performance and transmission range.

7.2.4. Single Chip, Brain Computer Interface (BCI)

In current BCI systems neural activity recorded from the test subject's central nervous system (CNS) is transmitted to an external processor that operates the extraction algorithm on the recorded signal. The extracted control signal is fed to a robot controller to move the prosthetic arm [7.9]. The external computer can be replaced with a low-power processor [7.10] implemented on the same ASIC as the data acquisition ASIC. In such system the ASIC collects the neural signals, sorts the spikes into multiple clusters, generates the control signals for the robotic arms, and transmits the control signal wirelessly to the robotic limb. The same system can be employed in prosthetic applications as well.

In conclusion, the proposed research project focused on developing wireless microsystems intended for extracellular neural recordings from central/peripheral nervous systems of awake and mobile small test subjects. The main challenge of this work is meeting the low power consumption and reliable operation criteria which was addressed at both architectural and circuit levels. The outcome of this research enables the neuroscience community study the nervous system of test subjects as they freely interact in a colony and advances our understanding of brain development.

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