Modeling of current–voltage characteristics for double-gate a-IGZO TFTs and its application to AMLCDs

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Abstract — The equations for the transfer characteristics, subthreshold swing, and saturation voltage of double-gate (DG) a-IGZO TFTs, when the top- and bottom-gate electrodes are connected together (synchronized), were developed. From these equations, it is found that synchronized DG a-IGZO TFTs can be considered as conventional TFTs with a modified gate capacitance and threshold voltage. The developed models were compared with the top or bottom gate only bias conditions. The validity of the models is discussed by using the extracted TFT parameters for DG coplanar homojunction TFTs. Lastly, the new pixel circuit and layout based on a synchronized DG a-IGZO TFT is introduced.

Keywords — *Double gate, thin-film transistor, a-IGZO, transfer characteristic, subthreshold voltage.*
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1 Introduction

There has been increased interest in adapting amorphous-indium–gallium–zinc–oxide (a-IGZO) thin-film transistors (TFTs) as a next-generation TFT technology for active-matrix flat-panel displays.[1,2] The a-IGZO TFTs have a field-effect mobility (μ) ranging from 8 to 20 cm^2/V-sec, a subthreshold swing (SS) below 200 mV/dec, a threshold voltage (V_{TH}) of about 0 V, and an off-current below 1×10^{-12} A.[3] Thus far, much of the research efforts have been focused on improving the a-IGZO material properties as well as the gate-dielectric interface.[4,5] It is important to keep in mind, however, that the electrical performance of TFTs is also influenced by the device structure.

A double-gate (DG) a-IGZO TFT structure has both a bottom-gate (BG) and a top-gate (TG) electrode that can be biased differently.[6–8] It is well known that the electrical performance of DG TFTs is improved in comparison to single bottom-gate TFTs because a larger portion of the channel area is controlled by an additional top-gate electrode. Furthermore, it is found that DG a-IGZO TFT has a higher stability under light illumination. To understand the operation principle of a DG a-IGZO TFT, a mathematical analysis based on device physics is needed. Abe *et. al.* described the mathematical analysis of a DG a-IGZO TFT for the condition when either TG or BG is biased at a constant value and concluded that the DG TFTs with a constant BG or TG bias have an electrical performance comparable (or even worse in the saturation region) to the conventional single-gate TFT.[9] To take advantage of the DG TFT, both TG and BG should be tied together (synchronized). In this paper, we present an extension of Abe's previous work. We analyzed the DG a-IGZO TFT's characteristics under synchronized bias conditions. In the latter part of this paper, the TFT parameters of the DG a-IGZO coplanar homojunction TFT are extracted and compared with the developed analytical model. In addition, a new pixel circuit based on a synchronized DG a-IGZO TFT is introduced for active-matrix liquid-crystal-display (AMLCD) application.

2 Double-gate TFT modeling

Figures 1 and 2 show a schematic cross section of a DG TFT with a channel length L and channel thickness t_S. The mathematical derivation is based on the following assumptions: (*i*) *Constant Mobility:* The mobility is constant during TFT operations; (*ii*) *Gradual Channel:* The voltages vary gradually along the channel from the source to the drain; (*iii*) *Two-Dimension:* The TFT is two-dimensional. The TFT does not have the channel width (W) dependency; (*iv*) *DC Measurements:* The bias voltage or current can be changed only after the TFT is under equilibrium states; and (*v*) *Long Channel:* There is no interaction between the source/drain electrodes. The above assumptions might not be always ade-

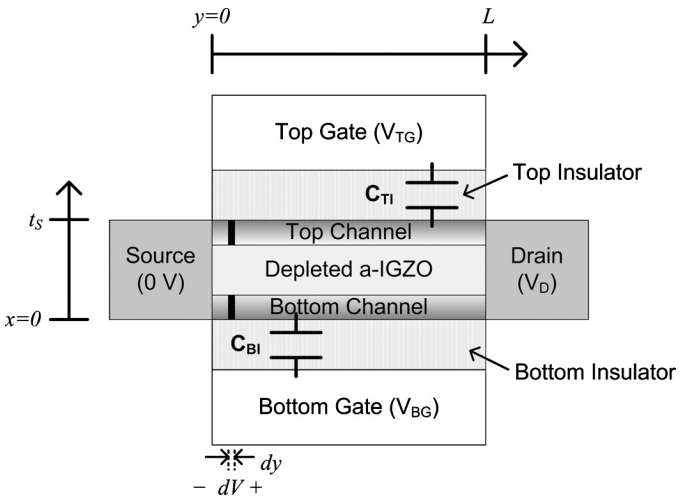

FIGURE 1 — Schematic cross section of a DG TFT (*y* direction).

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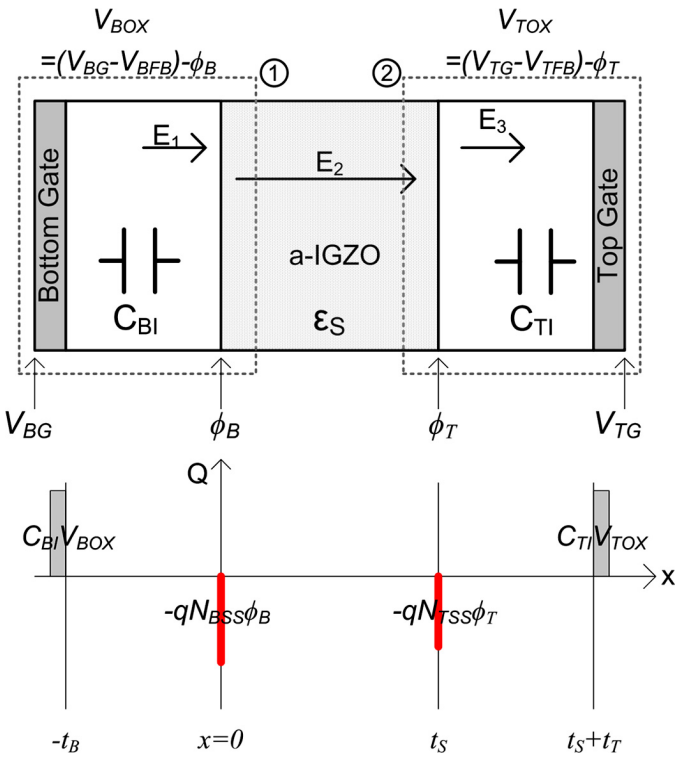

FIGURE 2 — Schematic cross section of a DG TFT and space-charge distribution (x direction).

quate for the field-effect transistors (FETs), such as a-IGZO TFTs. However, we believe that the model using these assumptions can successfully explain the electrical characteristics of conventional TFT, such as field-effect mobility (μ), threshold voltage (V_{TH}), and subthreshold swing (SS). The similar assumptions are also employed in the SPICE Level 1 model for the FETs.[10]

On Operation Region: From Fig. 1, the surface charge density, Q_S, can be written as the sum of bottom and top surface charge density (Q_{BS} and Q_{TS}, respectively)

$$Q_S = Q_{BS} + Q_{TS}. \tag{1}$$

From the parallel-plate capacitor model,

$$Q = CV. \tag{2}$$

Therefore, the Q_S can be written as

$$\begin{aligned} Q_S = {} & C_{BI}\left(V_{BG} - V_{BTH0} - V(y)\right) \\ & + C_{TI}\left(V_{TG} - V_{TTH0} - V(y)\right), \end{aligned} \tag{3}$$

where C_{BI} is the capacitances per unit area of the bottom insulator. $V(y)$ is the channel voltage at the position y, in the horizontal direction along the channel length from the source to drain. V_{BTH0} and V_{BG} correspond to the threshold voltages of the single-gate TFT only with the bottom electrode and the bias voltage applied on the bottom-gate electrode, respectively. The subscript T is associated with the top electrode.

The voltage drop dV between y to $y + dy$ is given by Ref. 11

$$dV = \frac{I_D\, dy}{W\mu|Q_S|}. \tag{4}$$

By integrating Eq. (4) for the entire channel length (from $y = 0$ to L), $\int_0^L I_D\, dy = \int_0^{V_D} W\mu|Q_S|\, dV$, the drain current ($I_D$) of the DG TFT is given by Eq. (5). Over the length of the channel, the channel voltage varies gradually from the source voltage $V(0) = 0$ to the drain voltage $V(L) = V_D$.

$$\begin{aligned} I_D = {} & \frac{W}{L}\frac{\mu}{C_{BI}+C_{TI}} \\ & \times \frac{\left\{C_{BI}\left(V_{BG}-V_{BTH0}\right)+C_{TI}\left(V_{TG}-V_{TTH0}\right)\right\}^2}{2} \\ & \times \left[1-\left\{1-\frac{\left(C_{BI}+C_{TI}\right)V_D}{C_{BI}\left(V_{BG}-V_{BTH0}\right)+C_{TI}\left(V_{TG}-V_{TTH0}\right)}\right\}^2\right]. \end{aligned} \tag{5}$$

Since $V_G = V_{BG} = V_{TG}$, in synchronized DG operation, Eq. (5) is simplified into Eq. (6).

$$\begin{aligned} I_D = {} & \frac{W}{L}\frac{\mu}{C_{BI}+C_{TI}} \\ & \times \frac{\left\{\left(C_{BI}+C_{TI}\right)V_G-\left(C_{BI}V_{BTH0}+C_{TI}V_{TTH0}\right)\right\}^2}{2} \\ & \times \left[1-\left\{1-\frac{\left(C_{BI}+C_{TI}\right)V_D}{\left(C_{BI}+C_{TI}\right)V_G-\left(C_{BI}V_{BTH0}+C_{TI}V_{TTH0}\right)}\right\}^2\right]. \end{aligned} \tag{6}$$

For more simplification, we define the double-gate capacitances per unit area (C_{DI}) and the threshold voltage of synchronized DG operation (V_{DTH})

$$C_{DI} = C_{BI} + C_{TI}, \tag{7}$$

$$V_{DTH} = \frac{C_{BI}V_{BTH0} + C_{TI}V_{TTH0}}{C_{DI}}. \tag{8}$$

Then, I_D can be expressed as

$$\begin{aligned} I_D = {} & \frac{W}{L}\mu C_{DI} \\ & \times \frac{\left\{V_G - V_{DTH}\right\}^2}{2}\left[\frac{2V_D}{V_G - V_{DTH}} - \left(\frac{V_D}{V_G - V_{DTH}}\right)^2\right]. \end{aligned} \tag{9}$$

If the TFT is under linear operation region, $V_D << V_G - V_{DTH}$, the second-order term for V_D is canceled out. Then, Eq. (9) can be approximated into

$$I_D = \frac{W}{L}\mu C_{DI}\left(V_G - V_{DTH}\right)V_D. \tag{10}$$

Moreover, when V_D is larger than V_{D_SAT} ($= V_G - V_{DTH}$), which is derived from Eq. (3) with the channel pinch-off condition [$Q_S = 0$ and $V(L) = V_D$], the current does not increase further (saturated). Hence, the saturation current is

$$I_D = \frac{W}{2L}\mu C_{DI}(V_G - V_{DTH})^2. \quad (11)$$

These equations are very similar to equations used for description of conventional TFT's electrical properties.[12]

Subthreshold Region: The current in the subthreshold region of FETs is described by Eq. (12)[13,14]

$$I_D \sim \mu \frac{W}{L}\frac{k_B T}{q} t_{eff}\left(1 - e^{-qV_D/k_B T}\right)e^{q\phi/k_B T}. \quad (12)$$

The effective channel thickness (t_{eff}) is defined as the distance from the channel/insulator interface. k_B and T are the Boltzmann's constant and the absolute temperature, respectively. And, ϕ is the potential voltage at the channel surface. From the definition of subthreshold slope (SS),

$$SS \equiv \left(\frac{\partial \log_{10} I_D}{\partial V_G}\right)^{-1}. \quad (13)$$

Therefore, it is necessary to find the relationship between a surface potential (ϕ) and gate voltage (V_G) in the subthreshold region.

In Fig. 2, applying Gauss's laws to the surface 1 (①) and 2 (②) yields the following equations:

$$\varepsilon_S \mathbf{E}_2 = C_{BI} V_{BOX} - qN_{BSS}\phi_B, \quad (14)$$

$$-\varepsilon_S \mathbf{E}_2 = C_{TI} V_{TOX} - qN_{TSS}\phi_T, \quad (15)$$

where N_{BSS} is bottom surface trap states in the unit of eV^{-1}-cm^{-2} and ϕ_B is the potential voltage at the bottom channel/insulator interface. V_{BOX} is the potential difference across the bottom-gate insulator. $V_{BOX} = (V_{BG} - V_{BFB}) - \phi_B$, where V_{BFB} is the flat-band voltage of the bottom-gate electrode. Again, the subscript T is associated with the top electrode. ε_s is the permittivity of a-IGZO semiconductor. From Eqs. (14) and (15), we can derive the equation of a charge balance $\sum Q = 0$:

$$C_{BI} V_{BOX} - qN_{BSS}\phi_B + C_{TI} V_{TOX} - qN_{TSS}\phi_T = 0. \quad (16)$$

In synchronized bias condition, $V_G = V_{TG} = V_{BG}$ and we assume that same gate material is used for the top- and bottom-gate electrodes ($V_{FB} = V_{TFB} = V_{BFB}$). Thus, Eq. (16) is rewritten as

$$\begin{aligned}(C_{BI} + qN_{BSS})\phi_B + (C_{TI} + qN_{TSS})\phi_T \\ = (C_{BI} + C_{TI})(V_G - V_{FB}).\end{aligned} \quad (17)$$

As a next step, the difference of electric potential is expressed as the integral of the electric field $\mathbf{E}(x) = -d\phi_B(x)/dx$, thus

$$\begin{aligned}\phi_B - \phi_T &= \mathbf{E}_2 t_s \\ &= -\frac{C_{TI}(V_G - V_{FB}) - (C_{TI} + qN_{TSS})\phi_T}{\varepsilon_s} t_s.\end{aligned} \quad (18)$$

By equating, Eq. (17) into Eq. (18), two relations for ϕ_B and ϕ_T are given, where $C_{BSS} \equiv q \cdot N_{BSS}$ and $C_S \equiv \varepsilon_s/t_s$;

$$\begin{aligned}&\left(1 + \frac{C_{TI}C_S}{C_{BI}(C_{TI} + C_S + C_{TSS})}\right)V_G \\ &= \left\{\frac{C_{BI} + C_{BSS}}{C_{BI}} + \frac{(C_{TI} + C_{TSS})C_S}{C_{BI}(C_{TI} + C_S + C_{TSS})}\right\}\phi_B \\ &+ \left\{1 + \frac{C_{TI}C_S}{C_{BI}(C_{TI} + C_S + C_{TSS})}\right\}V_{FB},\end{aligned} \quad (19)$$

$$\begin{aligned}&\left(1 + \frac{C_{TI}(C_{BI} + C_S + C_{BSS})}{C_{BI}C_S}\right)V_G \\ &= \left\{\frac{C_{TI} + C_{TSS}}{C_{BI}} + \frac{(C_{BI} + C_{BSS})(C_{TI} + C_S + C_{TSS})}{C_{BI}C_S}\right\}\phi_T \\ &+ \left\{1 + \frac{C_{TI}(C_{BI} + C_S + C_{BSS})}{C_{BI}C_S}\right\}V_{FB}.\end{aligned} \quad (20)$$

If the current mainly flows near the bottom interface, I_D is given by

$$I_D \sim \mu \frac{W}{L}\frac{k_B T}{q} t_{B\_eff}\left(1 - e^{-qV_D/k_B T}\right)e^{q\phi_B/k_B T}, \quad (21)$$

where t_{B_eff} is the effective channel thickness for the bottom channel. From the definition of SS [Eq. (13)] and Eq. (21),

$$\begin{aligned}SS &= \left(\frac{\partial \log_{10} I_D}{\partial V_G}\right)^{-1} = \left(\frac{1}{I_D \ln 10}\frac{\partial I_D}{\partial V_G}\right)^{-1} \\ &= \left(\frac{1}{\ln 10}\left\{\frac{\partial t_{B\_eff}}{\partial V_G}\frac{1}{t_{B\_eff}} + \frac{q}{k_B T}\frac{\partial \phi_B}{\partial V_G}\right\}\right)^{-1} \\ &\simeq \ln 10 \cdot \frac{k_B T}{q}\left(\frac{\partial \phi_B}{\partial V_G}\right)^{-1}.\end{aligned} \quad (22)$$

By substituting Eq. (19) into Eq. (22), SS is obtained.

$$\begin{aligned}SS \sim \ln 10 \cdot &\frac{k_B T}{q} \\ &\times \frac{(C_{BI} + C_{BSS})(C_{TI} + C_S + C_{TSS}) + (C_{TI} + C_{TSS})C_S}{C_{BI}(C_{TI} + C_S + C_{TSS}) + C_{TI}C_S}.\end{aligned} \quad (23)$$

Then, if C_S is larger than the other capacitances, $C_S >> C_{TI}, C_{BI}, C_{TSS}, C_{BSS}$,

$$\begin{aligned}SS &\sim \ln 10 \cdot \frac{k_B T}{q}\left(\frac{(C_{DI} + C_{BSS} + C_{TSS})}{C_{DI}}\right) \\ &= \ln 10 \cdot \frac{k_B T}{q}\left(1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}}\right).\end{aligned} \quad (24)$$

The a-IGZO TFT used in this work has C_S = 295, C_{TI} = 9.5, C_{BI} = 17.7 and $C_{TSS} = C_{BSS} \approx 9$ nF/cm^2. From these values, we can conclude that the above assumption is reasonable.

Similarly, when I_D mainly flows near the top interface, the current is given by

$$I_D \sim \mu \frac{W}{L}\frac{k_B T}{q} t_{T\_eff}\left(1-e^{-qV_D/k_B T}\right)e^{q\phi_T/k_B T} \quad (25)$$

and

$$SS \simeq \ln 10 \cdot \frac{k_B T}{q}\left(\frac{\partial \phi_T}{\partial V_G}\right)^{-1} \sim \ln 10 \cdot \frac{k_B T}{q}\left(1+\frac{C_{BSS}+C_{TSS}}{C_{DI}}\right). \quad (26)$$

Therefore, the SS of DG TFTs, when $V_G = V_{BG} = V_{TG}$, can be expressed by

$$SS \simeq S_O\left(1+\frac{C_{BSS}+C_{TSS}}{C_{DI}}\right). \quad (27)$$

The value of $S_O = \ln 10 \cdot k_B T/q$ is about 60 mV at room temperature. If SS and C_{DI} are known, the N_{BSS} and N_{TSS} values can be calculated from Eq. (27).

3 Comparison with a conventional TFT model

The equations developed in the previous sections are summarized in Table 1. The equations for a conventional single-gate TFT and the DG a-IGZO TFT with a single gate being biased (*i.e.*, either the TG or BG constant bias is applied) are also tabulated in Table 1. The equation for DG a-IGZO TFTs with BG bias ($V_G = V_{BG}$, $V_{TG} = 0$) is adapted from Abe's work, and the equations for TG bias condition ($V_G = V_{TG}$, $V_{BG} = 0$) can be derived by replacing the subscripts B and T, which stand for bottom and top gate, respectively. Table 1 shows that the DG a-IGZO TFTs with a BG or TG bias have a reduced saturation mobility μ_{SAT}, reduced saturation voltage V_{D_SAT}, and increased SS. The amount of these changes is related to the ratio between C_{BI} and C_{TI}. In contrast, the DG TFTs with synchronized bias ($V_G = V_{BG} = V_{TG}$) does not suffer from any degradation. Moreover, it is worthy to note that the synchronized DG TFTs can be considered simply as conventional TFTs with a gate capacitance of $C_{DI} = C_{BI} + C_{TI}$ and a threshold voltage of $V_{DTH} = (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})/C_{DI}$.

To confirm the validity of the developed models, we measured the TFT characteristics of the DG coplanar homojunction a-IGZO TFTs. The schematic cross section of the DG a-IGZO TFTs is illustrated in Fig. 3. The TFTs were fabricated on a Corning 1737 substrate. The Mo layer (100 nm) is sputtered as the gate electrode. An amorphous-silicon oxide (a-SiO_x) layer of 200-nm thickness is deposited by PECVD as a bottom-gate insulator. The a-IGZO semiconductor layer (30 nm) and the a-SiO_x first passivation layer (150 nm) were deposited by sputtering. During the deposition process of the second passivation layer of hydrogenated amorphous-silicon nitride (a-SiN_x:H), the exposed areas of the a-IGZO layer (not covered with sputtered a-SiO_x) were converted into low-resistance source/drain regions. Lastly, the 50-nm-thick PECVD a-SiO_x is deposited for the third passivation layer, followed by the formation of 100-nm-thick Mo source/drain electrodes. More experimental details about the TFT process can be found in Ref. 15.

The bottom-gate insulator is a 200-nm-thick layer of silicon oxide and the top-gate insulator is a stacked tri-insulator structure of a-SiO_x/a-SiN_x/a-SiO_x, with a thickness for each layer of 150/300/50 nm, respectively. The capacitance of the trilayered structure is calculated using three serially connected capacitors. The values of C_{BI}, C_{TI}, and C_S are 17.7, 9.7, and 295 nF/cm^2. The permittivity of $4\varepsilon_0$, $7\varepsilon_0$, and $10\varepsilon_0$ are used for a-SiO_x, a-SiN_x, and a-IGZO, respectively, where ε_0 is the permittivity of the air. The channel width/length

TABLE 1 — Summary of different TFT models developed in this work.

	Conventional TFT	Double Gate TFT		
	Single Gate	TG (V_G=V_{TG}, V_{BG} = 0)	BG (V_G=V_{BG}, V_{TG} = 0)	SG (V_G=V_{BG}=V_{TG})
I_D (Lin.)	$\frac{W}{L}\mu C_G(V_G - V_{TH})V_D$	$\frac{W}{L}\mu C_{TI}(V_{TG} - V_{TTH})V_D$	$\frac{W}{L}\mu C_{BI}(V_{BG} - V_{BTH})V_D$	$\frac{W}{L}\mu C_{DI}(V_G - V_{DTH})V_D$
I_D (Sat.)	$\frac{W}{2L}\mu C_G(V_G - V_{TH})^2$	$\frac{W}{2L}\frac{\mu C_{TI}}{C_{DI}}C_{TI}(V_{TG} - V_{TTH})^2$	$\frac{W}{2L}\frac{\mu C_{BI}}{C_{DI}}C_{BI}(V_{BG} - V_{BTH})^2$	$\frac{W}{2L}\mu C_{DI}(V_G - V_{DTH})^2$
SS	$S_O \cdot \left(1+\frac{C_{BSS}+C_{TSS}}{C_G}\right)$	$S_O \cdot \left(1+\frac{C_{BI}+C_{BSS}+C_{TSS}}{C_{TI}}\right)$	$S_O \cdot \left(1+\frac{C_{TI}+C_{BSS}+C_{TSS}}{C_{BI}}\right)$	$S_O \cdot \left(1+\frac{C_{BSS}+C_{TSS}}{C_{DI}}\right)$
Sat. voltage	$V_G - V_{TH}$	$C_{TI}/C_{DI}(V_{TG} - V_{TTH})$	$C_{BI}/C_{DI}(V_{BG} - V_{BTH})$	$V_G - V_{DTH}$
Mob. (Lin.)	μ	μ	μ	μ
Mob. (Sat.)	μ	$\mu(C_{TI}/C_{DI})$	$\mu(C_{BI}/C_{DI})$	μ
Gate Cap.	C_G	C_{TI}	C_{BI}	$C_{DI}(= C_{BI} + C_{TI})$
Threshold Voltage	V_{TH}	$V_{TTH} = V_{TTH0} + \frac{C_{BI}}{C_{TI}}V_{BTH0}$	$V_{BTH} = V_{BTH0} + \frac{C_{TI}}{C_{BI}}V_{TTH0}$	$V_{DTH} = \frac{C_{BI}V_{BTH0} + C_{TI}V_{TTH0}}{C_{DI}}$

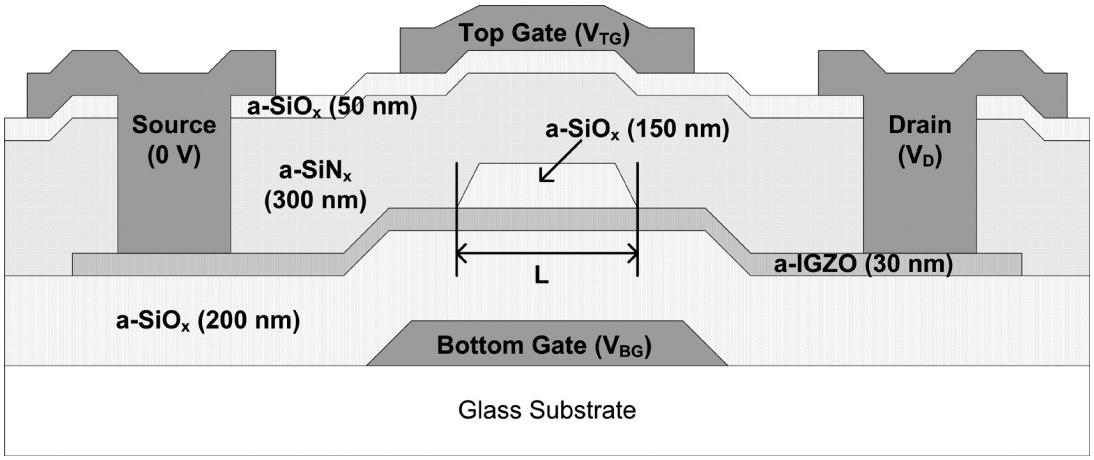

FIGURE 3 — Schematic cross section of a fabricated DG coplanar homojunction a-IGZO TFT.

(W/L) is 60 μm/10 μm. A sufficient overlap between top- and bottom-gate electrodes is used in the TFT layout to avoid misalignment of the two gates during TFT fabrication. The gate misalignment could degrade the on-current and subthreshold slope due to reduced gate controllability.[16] However, a too larger overlap to avoid the misalignment could increase the parasitic capacitance, which will worsen the TFT dynamic performance.

In the extraction of TFT parameters, SS was defined as $SS = (\partial \log I_D/\partial V_{GS})^{-1}$ around a maximum $\partial \log I_D/\partial V_{GS}$ point.[17] Since the constant mobility model is assumed in this work, V_{TH} and μ in the linear region were derived from a linear fitting to the $I_D - V_G$ curve at V_D = 0.1 V, and those in the saturation region were derived from a linear fitting to $I_D^{1/2} - V_G$ at V_D = 15 V by using the equations shown in Table 1. The transfer characteristics ($I_D - V_G$) are measured in Fig. 4 for three different bias conditions and the extracted device parameters from Fig. 4 are summarized in Table 2. As shown in Table 1, the mobility in the linear region and the μ_{SAT} with the SG bias should be identical for all three gate-bias conditions while the extracted μ_{SAT} for TG or BG being biased are proportionally decreased by the ratio of C_{TI}/C_{DI} or C_{BI}/C_{DI}. From the μ_{SAT} models and the capacitance in Table 1,

$$\mu_{SAT}(TG) = \frac{C_{TI}}{C_{DI}}\mu = 0.35\mu \text{ or } \mu_{SAT}(BG) = \frac{C_{BI}}{C_{DI}}\mu = 0.65\mu. \quad (28)$$

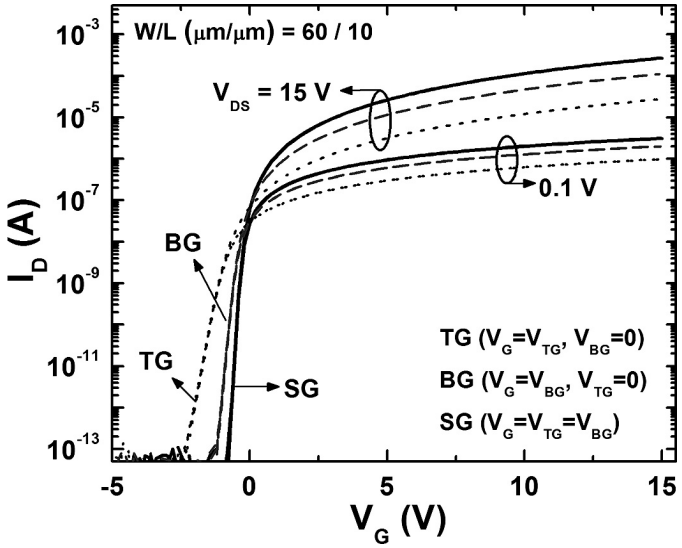

FIGURE 4 — Transfer characteristics of the DG a-IGZO TFTs for top-gate (TG), bottom-gate (BG), and synchronized-gate (SG) bias conditions.

From Table 2, we confirmed that the measured μ_{SAT} for TG or BG bias is decreased from μ in the linear region and that the amounts of the decrease are consistent with Eq. (28). In contrast, in the case of SG bias, the mobility in the saturation region is comparable to the values in the linear region. Therefore, the observed mobility degradations for

TABLE 2 — Extracted parameters for DG a-IGZO TFTs under different bias conditions.

	TG ($V_G = V_{TG}$, $V_{BG} = 0$)		BG ($V_G = V_{BG}$, $V_{BG} = 0$)		SG ($V_G = V_{BG} = V_{TG}$)	
	lin.	sat.	lin.	sat.	lin.	sat.
V_{TH} [V]	0.42	– 0.31	0.54	0.13	0.55	0.37
μ [cm^2/V-sec]	11.52	3.98	12.82	9.11	13.08	15.07
SS [V]	0.290		0.153		0.100	
C_G [nF/cm^2]	C_{TI} = 9.5		C_{BI} = 17.7		C_{DI} = 27.2	
N_{SS} [eV^{-1}cm^{-2}]	6.0×10^{10}		5.4×10^{10}		5.8×10^{10}	

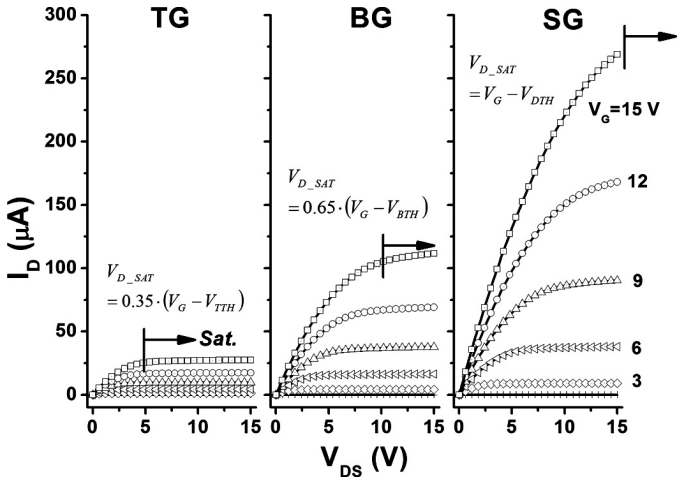

FIGURE 5 — Output characteristics of the DG a-IGZO TFTs for TG, BG, and SG bias conditions.

TG and BG bias are mainly due to the applied constant bias on one gate electrode and their difference disappears when both top- and bottom-gate electrodes are connected together.

Furthermore, from the SS value in Table 2, we can calculate the interface trap densities (N_{SS}), which are supposed not be different for all three bias conditions discussed in this paper. It is assumed that the BG and TG interface trap capacitances are the same ($C_{BSS} = C_{TSS}$) for convenience; $N_{SS} = N_{TSS} = N_{BSS}$. The calculated N_{SS} is similar for three bias conditions (*not supposed to be different*), which supports the validity of our analytic models. The previously reported μ and N_{SS} for conventional single gate coplanar homojunction a-IGZO TFTs (12.4 cm^2/V-sec and 7.3×10^{10} eV^{-1}-cm^{-2}, respectively)[15] were also comparable with our results. The device structure and fabrication details of the single-gate coplanar homojunction a-IGZO TFTs are identical to the TFTs analyzed in this paper.

Lastly, to verify V_{D_SAT} models, the $I_D - V_D$ characteristics are measured and shown in Fig. 5. If we assume that the threshold voltages for different gate bias conditions are similar, V_{D_SAT} is mainly related to C_{TI} or C_{BI}. Therefore, it is clear that the TFT saturation will take place earlier in the following sequence: the TG, BG, and SG, respectively, in agreement with Fig. 5. Hence, the proposed analytic models are in agreement with the measurement results.

4 Application to AMLCDs

Table 1 implies that DG a-IGZO TFTs with the synchronized bias condition can produce larger current and steeper subthreshold swing without increasing the channel width/length ratio (W/L) and/or the quality of the a-IGZO film. In other words, the same amount of drain current and sharp ON–OFF switching can be achieved with even smaller W/L TFTs. This observation can be advantageous in a pixel circuit designs for future AMLCDs. The future technology trends of AMLCDs are higher resolution (*i.e.*, ultra-high definition; 7680 × 4320 pixels), higher pixel density (over 300 ppi), and refresh rate (240 Hz or higher). To follow these trends, smaller and faster TFTs are required.[18] In this regard, the a-IGZO TFTs are considered as a leading approach for achieving high pixel density on large panel size because of its high mobility.[19] In addition, we believe that synchronized DG a-IGZO TFTs are more suitable than regular a-IGZO TFTs in terms of larger current in the same W/L and a steeper subthreshold swing.

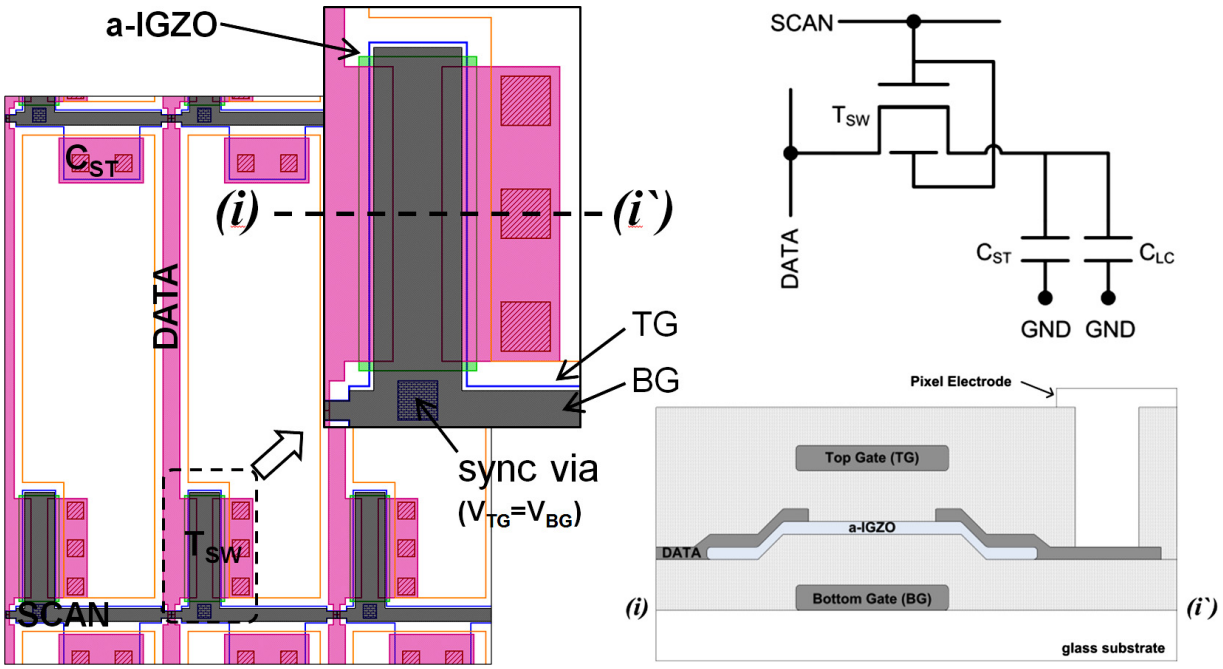

FIGURE 6 — Proposed AMLCD pixel circuit (top right), layout (left), and vertical cross section (bottom right) based on synchronized DG a-IGZO TFTs.

Figure 6 shows an example of the proposed pixel circuit with a synchronized DG TFT for AMLCD. In this pixel, the switching transistor (T_{SW}) is in the shape of an inverted staggered structure with an additional gate electrode, the top gate (TG). Moreover, TG and BG are fully overlapped and tied together (synchronized) through the sync via. By introducing an additional gate electrode, the parasitic capacitance between the two gates and the source/drain overlap could be increased. However, DG TFTs can have a smaller W for the same amount of drain current. Therefore, a decrease in device W can possibly cancel out a possible increase in device capacitance.

5 Summary

The simple analytic models of DG a-IGZO TFTs with synchronized bias conditions are developed and compared with TG or BG only bias devices. From this work, we can conclude that the DG TFTs under the bias condition of $V_G = V_{BG} = V_{TG}$ can simply be considered as conventional TFTs with a gate capacitance of $C_{DI} = C_{BI} + C_{TI}$ and a threshold voltage of $V_{DTH} = (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})/C_{DI}$. Furthermore, it is shown that the DG TFTs with TG or BG bias suffer from mobility and SS degradations. Therefore, two gate electrodes need to be tied together in order to avoid such degradations. The developed models are compared with the measurement results of the DG coplanar homojunction a-IGZO TFTs. The congruence between the models and measurements suggest that the developed models can successfully explain the electrical behaviors of the DG a-IGZO TFTs. We believe that DG TFTs are a better choice than single-gate TFTs for future AMLCDs and suggest a new pixel circuit based on synchronized DG a-IGZO TFTs.

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