High-performance top-gate a-Si:H TFTs for AMLCDs

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Abstract

High-performance top-gate hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) structures have been fabricated over a large area from plasma-enhanced chemical vapor deposition (PECVD) materials. The electrical performances of the top-gate a-Si:H TFT (μ_{FE}≈0.75cm^2/Vsec, V_T≈3.5V, S≈0.55V/dec) are comparable to the electrical performances observed for an inverted-staggered bottom-gate a-Si:H TFT. We have shown that the TFT field-effect mobility first increases with the a-Si:H thickness, and then decreases for thicker a-Si:H films. This change of the electrical performances can be associated either with the variation of a-Si:H microstructure with film thickness during the PECVD processes or a large density of TFT back interface states; it also involves the source/drain parasitic access resistances, especially for thick a-Si:H layers.

Introduction

Based on the order of thin-film deposition, there are two types of a-Si:H TFT structures: inverted-staggered bottom-gate and normal-staggered top-gate[1]. Today the top-gate TFT structure is not used by the majority of flat-panel display producers. It is generally believed that the top-gate a-Si:H TFTs have a much worse electrical performance (lower mobility and higher threshold voltage) than inverted-staggered bottom-gate a-Si:H TFTs [2].

In this paper, the experimental and simulated results of the influence of a-Si:H thickness on the TFT electrical performances clearly indicate that a high-performance top-gate a-Si:H TFT can be fabricated over a large-area from PECVD layers.

Experiment

Glass substrates covered with amorphous silicon oxide (a-SiO$_x$:H) were used to fabricated the top-gate a-Si:H TFT structures. First a 400Å-thick indium-tin-oxide (ITO) layer was patterned as source and drain electrodes, and selective ohmic source/drain contacts were formed in-situ by P-treatment process of the ITO patterned electrodes in a PECVD system [3]. Following the P-treatment process, an intrinsic a-Si:H layer and hydrogenated amorphous silicon nitride (a-SiNx:H) gate insulator were deposited by the PECVD technique at 250°C. A 4500Å thick aluminum layer was used as the gate electrode. The amorphous silicon nitride thickness was not the same for all the samples; we, therefore, used the gate electrical field rather than the gate voltage: $F = V_G / t_{a-SiN}$.

The device parameters, such as the field-effect mobility (μ_{FE}) and the threshold voltage (V_T), were extracted from a-Si:H TFT I_D-V_G characteristics by least-square fitting to the MOSFET gradual channel approximation equation: $I_D=\mu_{FE}C_i(W/L)(V_G-V_T)V_D$, where C_i is the gate-insulator capacitance per unit, W is the channel width, L is the channel length, and V_D is the applied drain voltage. The field-effect channel conductance activation energy (E_A) at different gate voltages was obtained from the slope of the Arrhenius $ln(I_D)$ versus T^{-1} plot: $I_D \approx I_{D0}\exp(-E_A/kT)$, where I_{D0} is a constant, k is the Boltzmann constant, and T is the absolute temperature.

Results and discussion

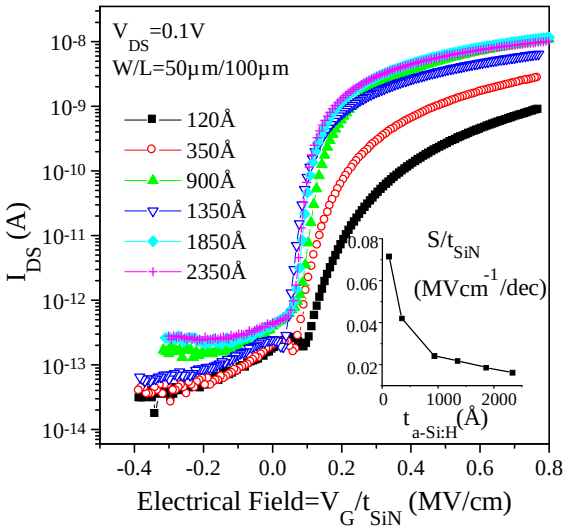

Figure 1: I_D-V_G characteristics of the top-gate a-Si:H TFTs with different a-Si:H thicknesses. The values of the subthreshold slope (normalized to the a-SiN:H thickness) are shown in the inset.

An example of the I_D-V_G transfer characteristics in the linear region (V_{DS}=0.1V) is shown in Figure 1 for

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top-gate a-Si:H TFTs with different a-Si:H layer thicknesses and a channel length of 100µm.

When the a-Si:H thickness decreases, the following trends can be observed: (i) the ON-current decreases and the I_D-V_G transfer curve moves towards higher V_G-values (reduction of the field-effect mobility and increase of the threshold voltage); (ii) the normalized subthreshold slope ($S/t_{SiN}=1//t_{SiN}$ $(\partial logI_D/\partial V_G)^{-1}$) increases; and (iii) the OFF-current decreases. Similar observations have been made for TFTs with different L-values. We have also observed a non-linearity of I_D-V_G characteristics for thinner a-Si:H layers, which can be associated with a higher value of a-Si:H band-tail state density [4].

The a-Si:H film thickness dependence of the field-effect mobility and threshold voltage is shown in Figure 2. The values corresponding to a 100µm-long TFT and the intrinsic values, extracted by the Transmission Line Method (TLM) [5], are given.

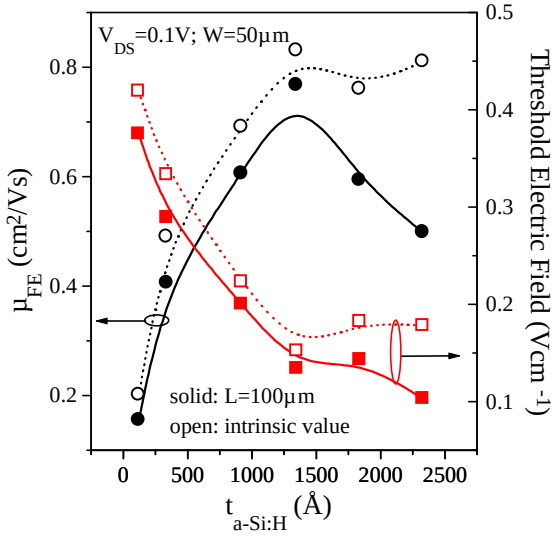

Figure 2: Field-effect mobility and threshold electric field (V_T/t_{a-SiN}) as a function of a-Si:H thickness, for top-gate 100µm-long TFT (solid). TFT intrinsic values are also shown (open).

The increase of the intrinsic mobility, together with the reduction of the subthreshold slope (insert in Figure 1) clearly indicate an improvement of a-Si:H electronic quality in terms of the density-of-states. However, for very thick films, the TFT field-effect mobility decreases with increasing a-Si:H thickness: this is due to a stronger influence of the parasitic source and drain access resistances. The rapid increase of the series resistances for thick a-Si:H films has been confirmed by the TLM results: TFT total series resistivities (source and drain contacts and access regions to the conduction channel), for a gate voltage of 15V above threshold voltage, are about 0.2 and 10Ωcm^2 for, respectively, 300 and 2330Å-thick a-Si:H TFTs. The decrease of TFT threshold voltage with increasing a-Si:H thickness could be associated with the improvement of a-Si:H electronic quality and/or with a weaker influence of TFT back interface (between the glass coating layer and the amorphous silicon) states on TFT electrical performances.

For a 1350Å thick 100µm-long a-Si:H TFT, the values of μ_{FE} and V_T are about 0.75cm^2/Vsec and 3.5V, respectively. These values are comparable to the values obtained for state-of-the-art inverted-staggered bottom-gate a-Si:H TFT having a similar a-Si:H layer thickness [5].

Figure 3 shows the variation of the field-effect channel conductance activation energy as a function of V_G for top-gate a-Si:H TFTs. To reduce the effect of the source/drain series resistance on the extraction of E_A from the Arrhenius plot, long channel length (100µm) a-Si:H TFTs were used [6]. A small series resistance effect (increase of E_A with decreasing L) on E_A-values can be observed in Figure 3 for a-Si:H TFTs with channel lengths of 10 and 100 µm. It should be noted that, for a-Si:H films thicker than 1350Å, the effect of the series resistances becomes significant even for 100µm-long TFTs.

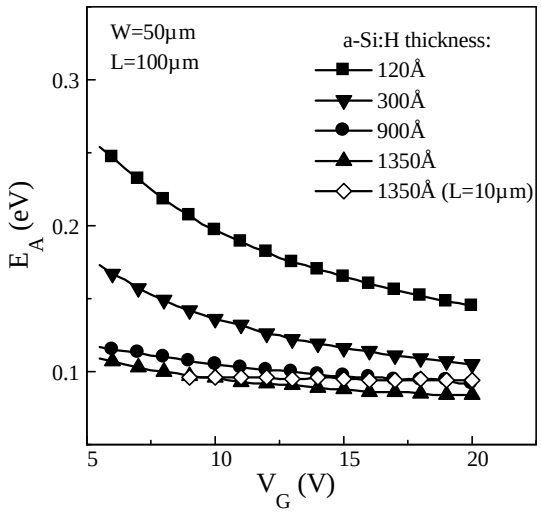

Figure 3: Channel conductance activation energy as a function of gate voltage for top-gate 100µm-long a-Si:H TFTs with different a-Si:H layer thicknesses. Values for a 1350Å-thick 10µm-long a-Si:H TFT are also shown.

We can conclude from this figure that a top-gate a-Si:H TFT with a thin a-Si:H layer (~120Å) has a high E_A-value (≈0.15eV) in the ON-state (V_G>V_T) in comparison with typical bottom-gate a-Si:H TFTs

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(E_A≈0.08eV). However, the E_A-values decrease with increasing a-Si:H layer thickness. A thicker a-Si:H top-gate TFT has an E_A-value (E_A≈0.08eV) similar to that obtained for a bottom-gate a-Si:H TFT. Assuming that E_A corresponds to the Fermi level position in the conduction channel, a higher E_A-value indicates that higher densities of conduction-band-tail- and deep-gap-states are present in thinner a-Si:H films.

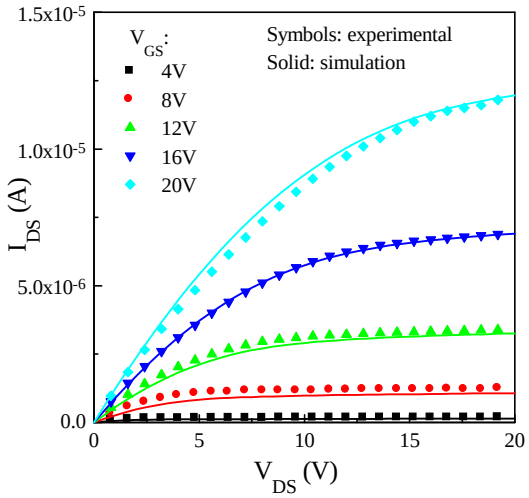

Figure 4: Example of simulated (solid curves) and experimental (symbols) I_{DS}-V_{DS} characteristics of 1350Å-thick 8µm-long a-Si:H TFTs for different gate voltages.

The experimental results discussed above are confirmed by the 2D simulation data. Figure 5 shows the evolution of the a-Si:H density-of-states parameters (band tail slope and deep-gap states) required to fit the experimental I_{DS}-V_{DS} characteristics of a-Si:H TFTs with different a-Si:H thicknesses as shown in Figure 4.

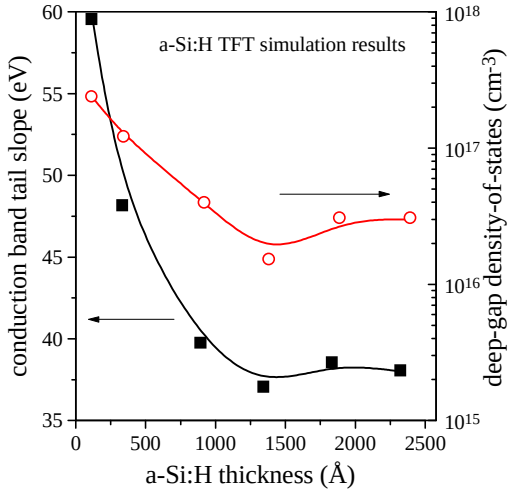

Figure 5: Values of the conduction band-tail- and deep-gap-states used to fit the experimental I_{DS}-V_{DS} (Figure 4) curves as a function of a-Si:H thickness.

It is clear from this figure that a-Si:H density-of-states decreases with increasing a-Si:H thickness. The optimum a-Si:H thickness for the best TFT electrical performances is about 1350Å, for a 100µm-long TFT. This is consistent with the data shown in Figure 2.

The thickness influence has also been observed in the high-frequency (100kHz) capacitance-voltage (*C-V*) characteristics of the metal-insulator-semiconductor (MIS) capacitors, where a higher degree of *C-V* curve stretch-out was observed for thinner a-Si:H films. These results are in agreement with the photothermal deflection spectroscopy (PDS) [7] and the electron spin resonance (ESR) [8] measurements, which have indicated that a higher deep-gap state density is expected for thinner a-Si:H films.

Reflective display

High-performance top-gate a-Si:H TFTs described in this paper can be used as a switching device in transmissive and reflective flat panel displays. A cross-section of 12.1" SVGA reflective (R)-TN mode TFT LCD is shown in Figure 6.

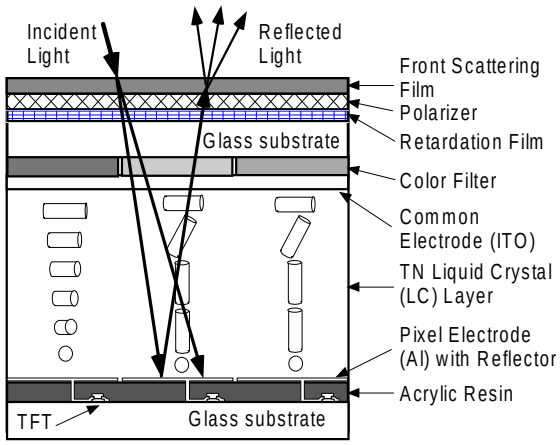

Figure 6: Cross-section of the full-color R-TN AMLCD.

The color R-TN AMLCD (normally black mode) consists of TFT active-matrix substrate, single polarizer, front scattering film, retardation film, color filter, and TN LC layer. In the configuration shown in Figure 6, the pixel electrode of the top-gate TFT is used as an internal reflector and is located just below the liquid crystal homogeneous alignment layer to avoid a parallax problem associated with the glass substrate. The pixel electrode was expanded above bus line and TFT to achieve a high aperture-ratio (88.5%). This pixel configuration is called Field Shielded Pixel (FSP) structure. The upper substrate includes the front scattering film to enhance the output (reflected) light from the display. The retardation film between polarizer and liquid crystal cell is added to display the achromatic colors.

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The variations of the reflectance and the contrast-ratio of the color R-TN AMLCD with viewing angle are shown in Figure 7; the angle of the incident light source is fixed at -30°. In this figure, the maximum reflectance is larger than 100% and the reflectance within ±15° from the detector angle at the maximum is 60% in comparison with the standard white ($BaSO_4$). Similarly, the maximum contrast-ratio is 6:1 and the contrast-ratio within ±15° from the detector angle at the maximum is 5:1. These values are comparable to those of the newspaper (reflectance and contrast-ratio are about 60% and 5:1, respectively).

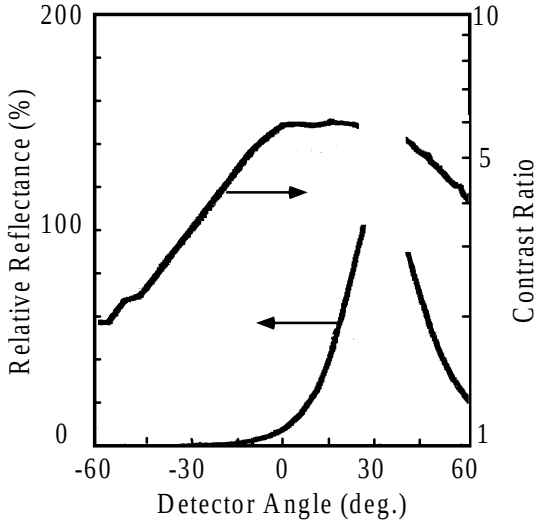

Figure 7: Viewing angle dependence of the reflectance and contrast-ratio of the color R-TN AMLCD.

The fabricated prototype color R-TN AMLCD has an excellent gray scale (64 levels), and could display 262,144 colors that are controlled by top-gate a-Si:H TFT with a low driving voltage (<5V).

The specifications of 12.1'' SVGA reflective full color display are given in Table 1.

Table 1: R-TN TFT-AMLCD specifications.

Display size	12.1" (31cm)
Number of dots	800x3x500dots
Dot pitch (WxH)	0.1025x0.3075mm^2
Contrast-ratio	6:1
Number of gray levels	64 levels
Number of colors	262,144 colors
Aperture ratio	88.5%
Number of photomask steps (TFT + Color Filter)	7 steps (4+3)

Note a high aperture-ratio and a low number of photolithography steps (for a transmissive color display, 10 photomask steps are required) that are needed to fabricate this full color reflective display.

Although usage of the color filters with a lower transmittance can result in a better chromaticity, it can cause a lower reflectance at the same time. Thus, for the present R-TN AMLCD, the RGB color filters with their transmittance of about 60 to 70% were used to satisfy both the chromaticity and the reflectance display requirements; and the chromaticity of our R-TN AMLCD is comparable to that of color pictures in a newspaper. Another factor that will affect the chromaticity is the back scattering of light from the front scattering film [9]. Further improvement of the front scattering film is needed to achieve a higher contrast-ratio and a better chromaticity of R-TN AMLCDs.

Conclusion

In this paper we have demonstrated that high-performance top-gate a-Si:H TFTs can be fabricated by the PECVD technique over a large-area. Hence, the general belief that top-gate a-Si:H TFTs have a worse electrical performance than bottom-gate a-Si:H TFTs is a myth rather than reality. We have also demonstrated that the top-gate TFT technology can be successfully applied to full color reflective TN AMLCDs.

Acknowledgments

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