Novel a-Si:H TFT pixel circuit for electrically stable top-anode light-emitting AMOLEDs

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Abstract — A novel pixel circuit for electrically stable AMOLEDs with an a-Si:H TFT backplane and top-anode organic light-emitting diode is reported. The proposed pixel circuit is composed of five a-Si:H TFTs, and it does not require any complicated drive ICs. The OLED current compensation for drive TFT threshold voltage variation has been verified using SPICE simulations.

Keywords — *AMOLED, a-Si:H, TFT, pixel circuit, reliability.*

1 Introduction

Amorphous-silicon (a-Si) technology has recently been drawing a great amount of attention as a promising candidate for backplane application in active-matrix organic light-emitting displays (AMOLEDs). The advantage of a-Si technology over its competitor, such as low-temperature polycrystalline-silicon (LTPS) technology, is that it can benefit from the existing infrastructures of the active-matrix liquid-crystal display (AMLCD) industry and that a huge part of the investment and manufacturing costs can be saved.[1] a-Si technology also delivers highly uniform active film due to its stable process capability.[2] However, the a-Si thin-film transistor (a-Si:H TFT) has some critical stability issues that could be problematic for AMOLED backplane applications. There are stability issues that arise from the degradation of TFT electrical characteristics under long-term bias stress.[3] Even a small positive gate bias applied long enough can produce negative charge trapping in a TFT gate insulator, which results in a positive shift of the TFT threshold voltage.[4] Such an increase in threshold voltage reduces the luminance of an AMOLED panel, thus reducing the overall lifetime.[5] Furthermore, such variations in TFT characteristics occur in different degrees for each pixel, causing each drive TFT in a display panel to have different threshold-voltage values. Such effect is often referred to as differential aging, which causes some undesirable visual defects, such as image sticking or the ghost effect.[6]

In order to overcome these issues, there are several pixel circuits for driving OLED current that compensates for the variation of TFT characteristics, some of which employ current-programming,[7] time-ratio gray scaling,[8] or threshold-voltage compensating[9] methods. The former two methods require the development of complicated source drive ICs which are not used in conventional AMLCDs. Therefore, in order for AMOLEDs to fully benefit from the existing AMLCD infrastructures, it is favorable to employ pixel driving schemes based on the source driving circuitry used in AMLCDs. In this paper, a pixel circuit capable of suppressing the effect of the TFT degradation to enhance the reliability of AMOLEDs without the use of any complicated drive ICs is introduced.

2 Pixel electrode circuit design

2.1 Device modeling

In order to design pixel circuits for AMOLEDs, SPICE circuit simulation and analysis must be performed. A set of highly accurate SPICE models and well-fitted device parameters are required. We extracted SPICE model parameters for a-Si:H TFT using a RPI (Rensselaer Polytechnic Institute) a-Si TFT model[10] and OLEDs using the Spectre junction diode model.[11] The curve-fitting results for a-Si:H TFTs, with channel dimensions of W/L = 60 μm/5 μm and for small-molecule RGB OLED samples, with a pixel aperture area of 10,000 μm^2, are shown in Figs. 1(a) and (1b), respectively. The maximum relative fitting error between the simulated and the experimental curves is less than 10% within circuit operation range used for driving a typical AMOLED.

2.2 AMOLED pixel circuit operation

We propose a new a-Si:H TFT pixel circuit for a top-anode light-emitting AMOLED, of which the circuit schematic and the timing diagram are shown in Figs. 2(a) and 2(b), respectively. In this study, we focused on maintaining the programmed OLED current regardless of the a-Si TFT threshold-voltage variation by compensating the gate node voltage of the drive TFT. Each pixel is composed of one power line (V_{DD}), two control lines (Gate1, Gate2), two capacitors ($C_{st1, Cst2}$), and five TFTs; two switch TFTs (SW1, SW2), a pre-charge TFT (PC), a drive TFT (DR), and a mirror TFT (MR). The pixel circuit operates in four stages;

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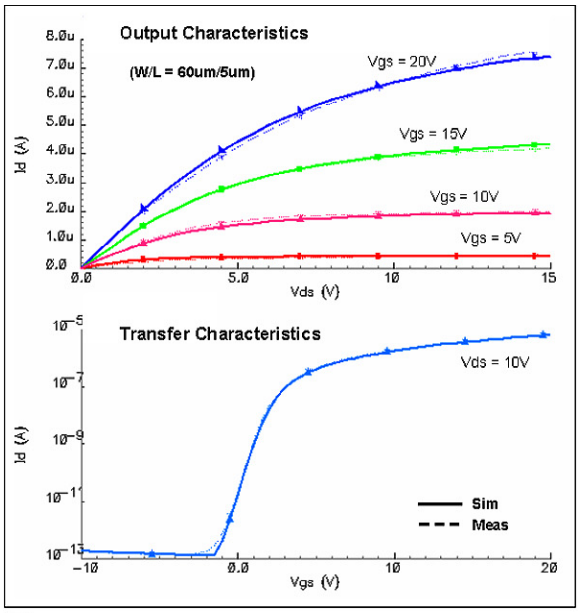
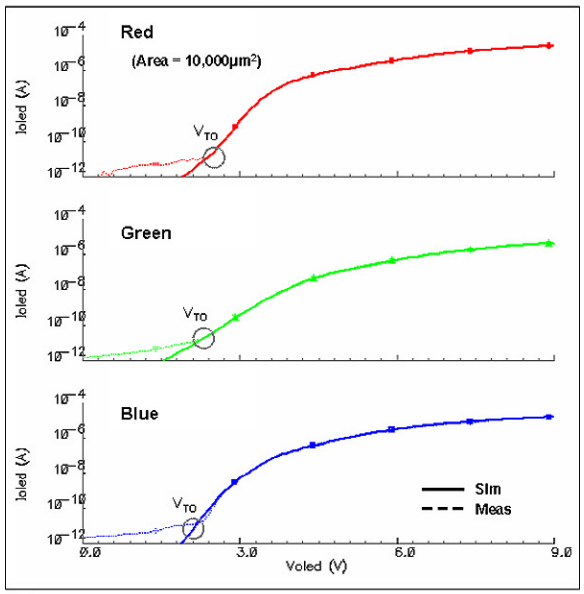


(a)



(b)

FIGURE 1 — Result of SPICE parameter extraction for device modeling of an a-Si:H TFT (a) using RPI model and (b) RGB OLEDs using the Spectre junction diode model. The maximum relative fitting error is less than 10% within device operation range.

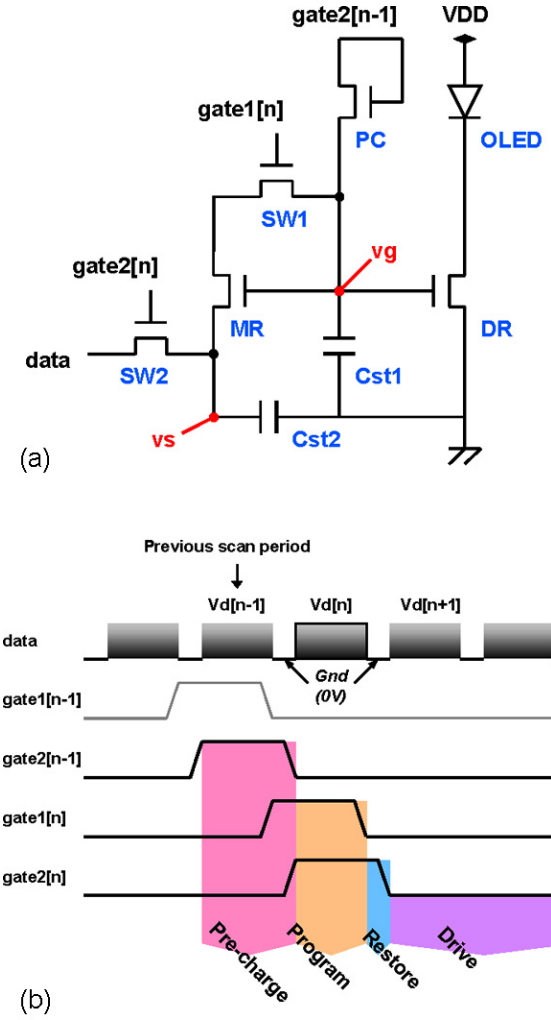


FIGURE 2 — (a) Schematic diagram of the proposed circuit and (b) timing diagram of data signal and gate control signals. The proposed pixel circuit operates in four stages; pre-charge, program, restore, and drive.

pre-charge, program, restore, and drive, as illustrated in Figs. 2 and 3. The transient analysis of SPICE simulation during these four stages is shown in Fig. 4.

During the pre-charge stage [Fig. 3(a)], previous line gate2 is high [Gate2(n – 1) = V_{GH}], which turns on the pre-charge TFT (PC). The pre-charge TFT with its drain and gate node connected act as a diode with turn-on voltage equal to the threshold voltage of pre-charge TFT (V_{to} = $V_{th_{PC}}$). Because the anode voltage of this pre-charge diode is relatively high (V_{GH} ~ 30 V), forcing the diode to be forward-biased, the gate node of the drive TFT (DR) is pre-charged to a voltage equal to the gate high voltage minus the TFT threshold voltage (v_g = V_{GH} – $V_{th_{PC}}$), as noted in Fig. 4(a).

During the program stage [Fig. 3(b)], previous line gate2 is low [Gate(n – 1) = V_{GL}], whereas gate1 and gate2 are high [Gate1(n) = Gate2(n) = V_{GH}], and the data signal voltage [$D(n)$ = V_{data}] is applied to the source node of the mirror TFT (MR). The first switch TFT (SW1) connects the gate and drain of the mirror TFT to form a diode; namely, the mirror diode, with the turn-on voltage equal to the threshold voltage of the mirror TFT (V_{to} = $V_{th_{MR}}$). Because $V_{GH} - V_{th_{PC}}$ was stored in the first storage capacitor (C_{st1}) during the pre-charge stage, and this voltage is typically much higher than V_{data}, the mirror diode is forward-biased. The gate node voltage of the drive TFT, or the source node voltage of the mirror TFT, is decreased as the storage capacitor is discharged through the mirror diode. The positive node of the storage capacitor, or the gate node of the drive TFT, will converge to the applied data voltage plus the turn-on voltage of the mirror diode (v_g = V_{data} + $V_{th_{MR}}$), as noted in Fig. 4(b). Consequently, the threshold voltage of the mirror TFT is programmed and stored in the storage

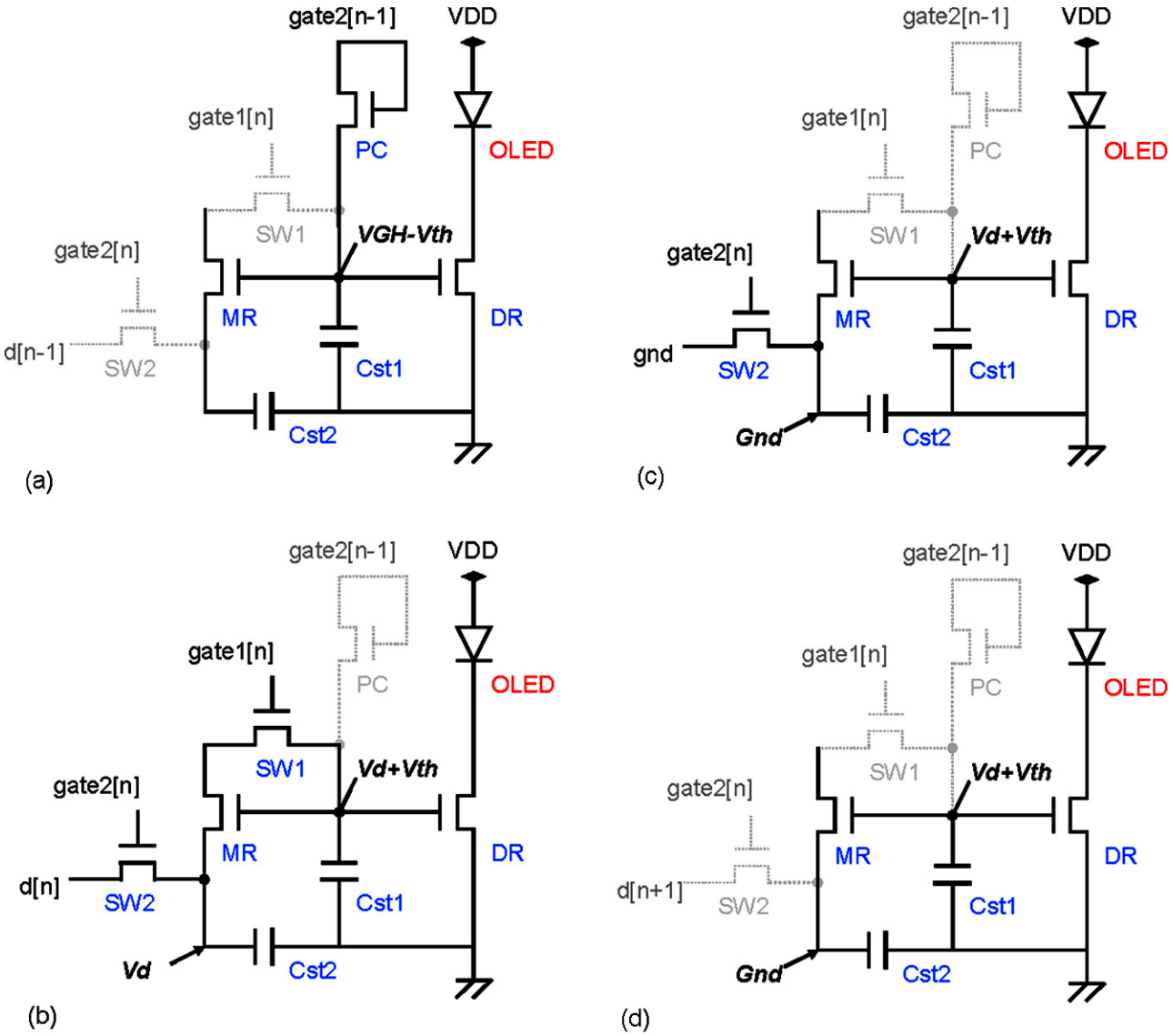


FIGURE 3 — (a) Schematic diagram of the proposed pixel circuit under operation stages of pre-charge, (b) program, (c) restore, and (d) drive. Dotted gray line indicates opened circuit path and solid black line indicates closed circuit path.

capacitor. During restore stage [Fig. 3(c)] gate1 is low, whereas gate2 is still high, and the data signal voltage is 0 V (= *Gnd*). While the gate voltage of the drive and mirror TFTs is held at $V_{data} + V_{th_{MR}}$, the source voltage of the mirror TFT is decreased from V_{data} to GND, and restored in the second storage capacitor (C_{st2}), as noted in Fig. 4(c). The purpose of restoring the source voltage of the mirror TFT to *Gnd* is to make the gate-to-source voltage (V_{gs}) of both the mirror and drive TFTs identical for most of the drive period. Our recent studies convey that the amount of threshold-voltage shift of the a-Si:H TFT depends mostly on the gate-to-source voltage applied rather than to the current applied.[12] Hence, we assume that the threshold voltages of the drive and mirror TFTs are the same.

During the drive stage [Fig. 3(d)], gate2 is low, and the drive TFT drives the programmed OLED current. Since we assumed that the threshold voltages of the mirror and drive TFTs are identical ($V_{th_{DR}} = V_{th_{MR}}$), the voltage stored in the storage capacitor will compensate the OLED current for the variation of drive TFT threshold voltage by cancelling out the threshold voltage parameter, as derived in the following equations:

$$V_{th_{DR}} = V_{th_{MR}}, \tag{1}$$

$$I_{OLED} = \frac{k}{2}\left(V_{gs} - V_{th_{DR}}\right)^2, V_{gs} = V_{data} + V_{th_{MR}}, \tag{2}$$

$$I_{OLED} = \frac{k}{2}\left(V_{data} + V_{th_{MR}} - V_{th_{DR}}\right)^2 = \frac{k}{2}V_{data}^2. \tag{3}$$

3 Results

3.1 Electrical stability of a-Si:H TFT

In order to examine the behavior of TFT degradation under long-term circuit operation, we performed bias temperature

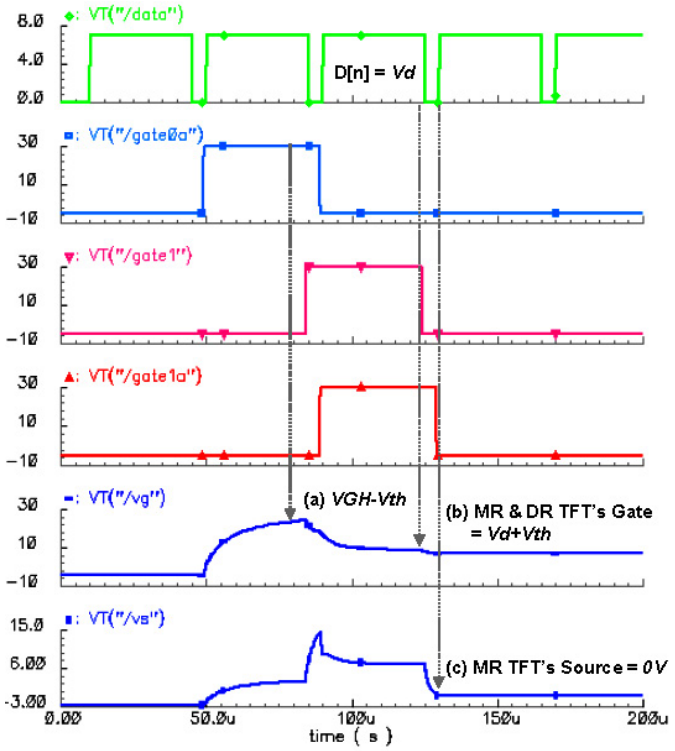


FIGURE 4 — SPICE simulation results of transient analysis. (a) The gate node voltage of the drive TFT and mirror TFT is pre-charged to $V_{GH} - V_{thPC}$ and (b) then programmed to $V_{data} + V_{thMR}$. (c) The source node voltage of the mirror TFT is restored to 0 V.

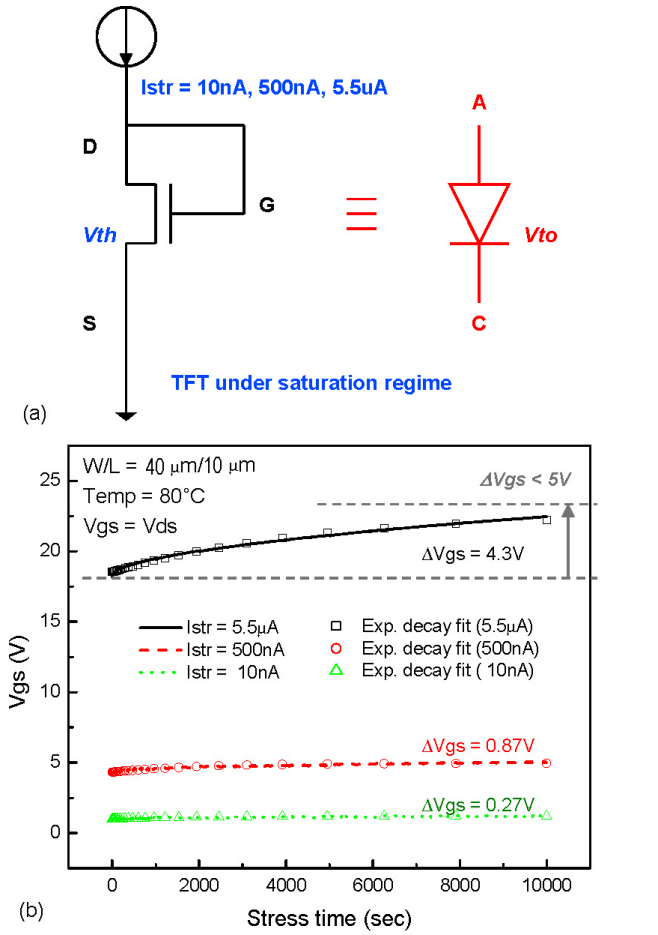


FIGURE 5 — (a) Bias temperature stress test on a-Si:H TFT under 80°C for 10,000 sec in the diode mode, where the gate and drain electrodes are connected. (b) Temporal variation plots of the voltage across the TFT in reference to an applied current of 10 nA, 500 nA, and 5.5 µA suggest that the maximum threshold variation is about 5 V.

stress tests on the a-Si:H TFT. As illustrated in Fig. 5, a constant current was applied to the a-Si:H TFT at 80°C for 10,000 sec in diode mode, where gate and drain electrodes are connected ($V_{gs} = V_{ds}$).[12] The temporal variation of the voltage across the TFT (V_{gs}) with stress time is measured in reference to the applied current, as plotted in Fig. 5(b). Under the constant current stress in the diode mode, the gate voltage of the TFT will increase according to the positive shift of the TFT threshold voltage. Hence, this stress test well characterizes the gate bias stress effect on the drive TFT of the proposed AMOLED pixel circuit because the gate voltage of the drive TFT will be adjusted in effort to maintain the OLED current constant. During the entire stress time, it is shown that the voltage increase across the TFT was not larger than 4.3 V even when the applied current exceeded 5 µA. We believe that the increase in the TFT gate-to-source voltage corresponds to the increase in the TFT threshold voltage ($\Delta V_{gs} \approx \Delta V_{th}$), and that this will eventually converge to a certain value because the voltage-time relation fits well to a first-order exponential decay curve, as shown in the Fig. 5(b). From the test results, we chose a threshold voltage shift of 5 V to be used in the SPICE simulation as the worst-case TFT degradation. Accordingly, we set our goal to design a pixel circuit capable of suppressing the OLED current variation within 15% by compensating for the TFT threshold voltage shift up to 5 V.

To find the critical factor that controls the degradation behavior of the drive TFT, we also performed a common-gate current stress test. Constant current stresses were applied to the TFTs at 80°C for 10,000 sec while fixing the gate voltage at 20 V, as shown in Fig. 6.[12] This common-gate constant current stress test emulates the bias stress effect on the proposed pixel circuit, where a pair of TFTs share the same gate node as illustrated in Fig. 6(a). The test results show that the TFT threshold voltage increases linearly with the stress time in a log-log scale and that these values are nearly identical regardless of the applied current or the corresponding drain voltage. When the applied stress currents were 10 and 500 nA, the maximum threshold-voltage difference between the two tests was about 0.5 V, which is less than 10% of the actual shift. We concluded that the critical factor controlling the threshold voltage under bias stress is the gate-to-source voltage (V_{gs}), so that the level of threshold-voltage shift is persistent with the fixed V_{gs}.

In worst case, when the drive TFT threshold voltage is 0.5 V lower or higher than that of the mirror TFT, it is shown in Fig. 7 that the OLED current exhibits rather large variation of ±13%. However, this variation can be reduced by optimizing several design parameters. When the threshold voltage difference varies from $-\Delta V_{th}$ to $+\Delta V_{th}$, the corre-

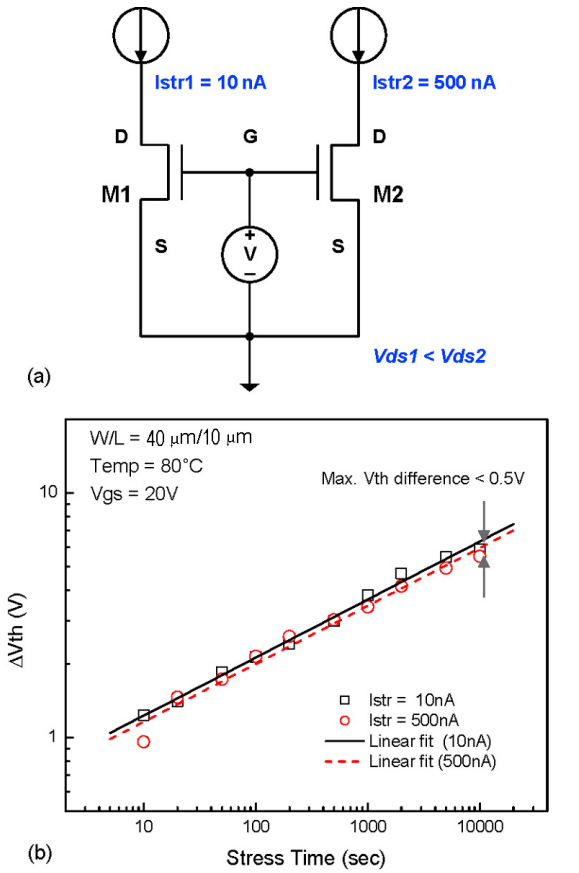


FIGURE 6 — (a) Bias temperature stress test on an a-Si:H TFT under 80°C for 10,000 sec in the common-gate mode, where the gate voltage is fixed at 20 V. (b) Temporal variation plots of the threshold voltage in reference to the applied current of 10 and 500 nA suggest that the threshold-voltage shift is mainly influenced by the gate-to-source voltage.

sponding OLED current (I_{OLED}) is equal to the drive TFT current under saturation regime. We can define the OLED current variation as the ratio of current difference to the original current, $\Delta I_{OLED}/I_{OLED}$ (%), as derived in the following equations.

$$I_{OLED} = K\left(V_{gs} - V_{th}\right)^2, \left(K = \frac{1}{2}\mu\frac{\varepsilon_{SiN_x}}{t_{SiN_x}}\frac{W}{L}\right), \tag{4}$$

$$I_{OLED1} = K\left(V_{gs} - V_{th} + \Delta V_{th}\right)^2, \tag{5}$$

$$I_{OLED2} = K\left(V_{gs} - V_{th} + \Delta V_{th}\right)^2, \tag{6}$$

$$\frac{\Delta I_{OLED}}{I_{OLED}}(\%) = \frac{I_{OLED1} - I_{OLED2}}{I_{OLED}} = \frac{2(V_{gs} - V_{th})\cdot 2\Delta V_{th}}{(V_{gs} - V_{th})^2} = \frac{4\Delta V_{th}}{(V_{gs} - V_{th})}. \tag{7}$$

It is concluded from the equation that the OLED current variation is proportional to ΔV_{th} and is inversely proportional to $(V_{gs} - V_{th})$. This implies that lower OLED currents are more sensitive to the threshold voltage variation. For a given current, the OLED current has less variation if the corresponding $(V_{gs} - V_{th})$ value is larger, or if the transconductance coefficient K is smaller. The design value of K can be easily reduced by minimizing the channel width; however, increasing the $(V_{gs} - V_{th})$ value can result in a larger threshold voltage shift. Therefore, the design value of K should be carefully chosen to satisfy both the spatial and temporal reliability requirements of the AMOLED.

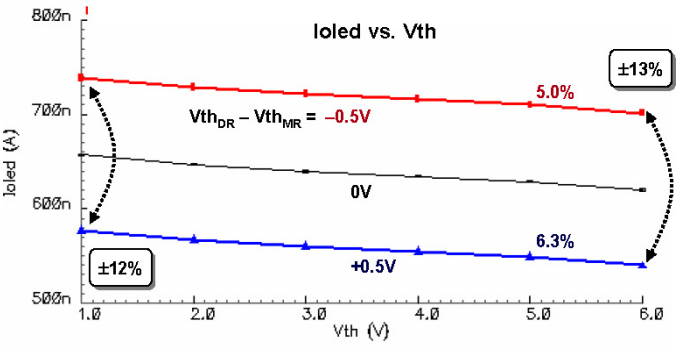


FIGURE 7 — Variation of OLED current plotted verses threshold-voltage variation of the drive and mirror TFTs. Maximum variation of the OLED current is ±13% when the threshold-voltage difference between the drive and mirror TFTs varies from –0.5 to +0.5 V.

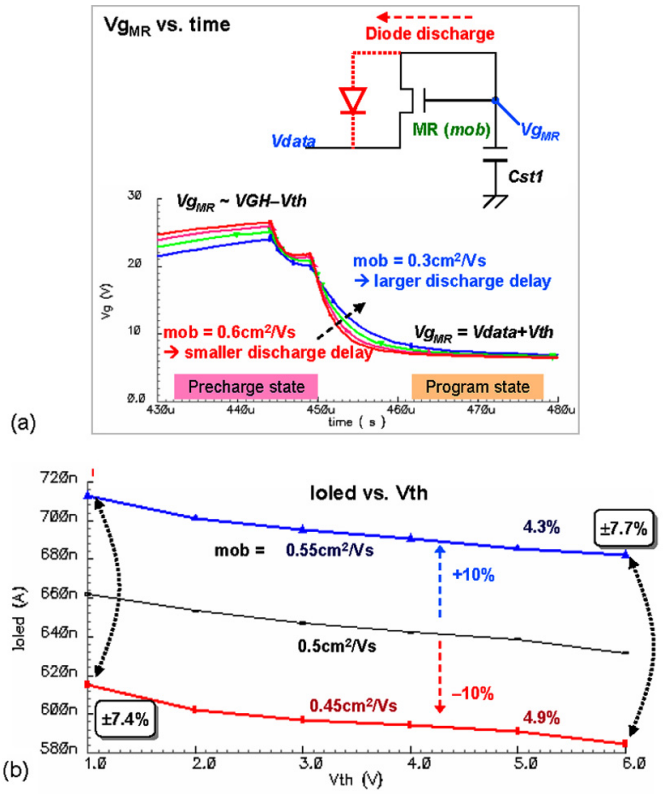


FIGURE 8 — (a) Transient analysis of the gate node voltage of the mirror TFT (V_{gMR}) during pre-charge and program stages, where the gate node voltage decreases from $V_{GH} - V_{thPC}$ to $V_{data} + V_{thMR}$ by discharging of the storage capacitor (C_{st1}) though the mirror diode (b). Maximum variation of the OLED current is ±7.7% when the mobility of both the drive and mirror TFTs varies by a deviation of ±10%.

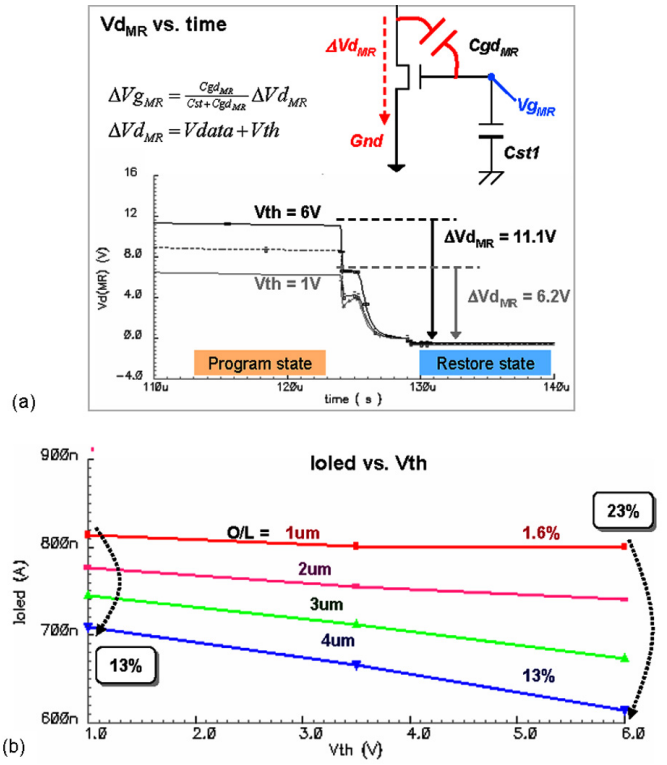


FIGURE 9 — (a) Transient analysis of the drain node voltage of mirror TFT (V_{dMR}) during program and restore stages, where parasitic gate capacitance induce gate node voltage distortion due to charge coupling. The drain node voltage of mirror TFT (V_{dMR}), which controls the gate node voltage distortion, alters from V_{data} + V_{thMR} to 0 V.

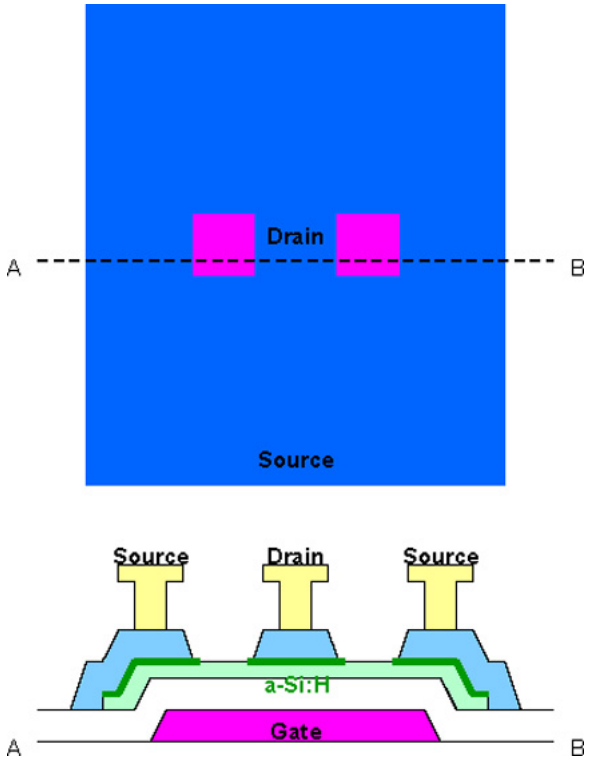


FIGURE 10 — Top- and cross-sectional view of the proposed TFT structure with the planar structure redesigned to reduce the gate-to-drain overlap capacitance. Only gate, source, and drain electrodes are illustrated in the top-view diagram.

3.2 SPICE analysis

During pixel-circuit analysis, we considered several process parameters that induce parasitic but critical effects on the pixel circuit performance. Although the a-Si:H TFT is considered to have very uniform and stable field-effect mobility, or the transconductance K, these values may vary with film thickness and etch uniformity. Figure 8(a) illustrates the transient behavior of the gate node voltage (v_g) during precharge and program stages. In transition from the precharge to program stage, the gate node voltage is decreased from $V_{GH} - V_{th_{PC}}$ to $V_{data} + V_{th_{MR}}$ by discharging the storage capacitor (C_{st}) though the mirror diode. It is shown that if the mirror TFT has higher mobility, or higher transconductance, discharge delay of the storage capacitor is lower, resulting in lower gate node voltage. As shown in Fig. 8(b), when the TFT mobility varies ±10%, the corresponding OLED current variation is reduced to ±7.7% due to the reverse compensation effect of discharge delay.

Another parameter considered is the parasitic gate capacitance of the drive and mirror TFTs. As illustrated in Fig. 9(a), the parasitic gate capacitance induce gate node voltage distortion due to charge coupling. The gate node voltage is most distorted when the gate-to-drain capacitance of the mirror TFT ($C_{gd_{MR}}$) couples with the storage capacitor (C_{st}) during transition from the program to restore stage. The drain node voltage of the mirror TFT ($V_{d_{MR}}$), which controls the gate node voltage distortion, decreases from V_{data} + $V_{th_{MR}}$ to 0 V. This voltage swing is dependent on the threshold voltage of the mirror TFT to which OLED current becomes very sensitive, particularly when the gate-to-drain overlap capacitance is noticeably large. As shown in Fig. 9(b), the OLED current decreases 13% as the TFT threshold-voltage shifts 5 V positive when gate-to-drain overlap length is 4 µm. In order to resolve this circuit instability, we redesigned the planar structure of the drive and mirror TFTs to reduce the gate-to-drain overlap area,[13] as illustrated in Fig. 10.

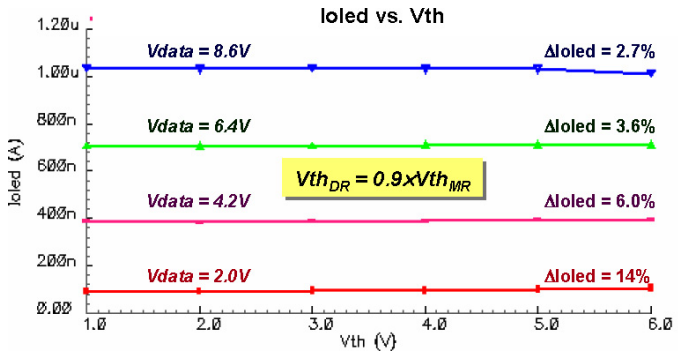


FIGURE 11 — Variation of OLED current plotted verses the threshold voltage of drive the TFT from 1 to 6 V while setting the difference of threshold voltage between drive and mirror TFT to 10%. The data voltage (V_{data}) from 2 to 8.6 V drives the OLED current from 100 nA to 1 µA, of which the maximum current variation is less than 15%.

By synthesizing all the parasitic effects and optimizing all the design parameters, the electrical stability of the proposed pixel circuit has been verified using SPICE simulations. According to the experimental data from current stress tests in the common-gate mode, the difference in threshold voltage between the drive and mirror TFT is set to 10%. The data voltage (V_{data}) from 2 to 8.6 V is applied to drive the OLED current from 100 nA to 1 μA, as the I_{OLED} variation verses the drive TFT threshold voltage plot is shown in Fig. 11. The simulated results verify that the proposed pixel circuit compensates OLED current for a TFT threshold voltage shift up to 5 V, resulting in a maximum I_{OLED} variation of less than 15%, even when the drive and mirror TFTs have 10% threshold-voltage difference.

4 Conclusion

We have reported a novel and electrically stable a-Si:H TFT pixel circuit suitable for AMOLEDs. The proposed pixel circuit is composed of a-Si:H TFTs and a top-anode OLED structure, and it does not require any complicated drive ICs. We have verified the OLED current compensation for the drive TFT threshold voltage variation using SPICE simulations. The results show that the OLED current varies less than 15% when the threshold voltage of the drive TFT shifts up to 5 V.

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