Active-matrix organic light-emitting displays employing two thin-film-transistor a-Si:H pixels on flexible stainless-steel foil

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Abstract — An active-matrix organic light-emitting diode (AMOLED) display driven by hydrogenated amorphous-silicon thin-film transistors (a-Si:H TFTs) on flexible, stainless-steel foil was demonstrated. The 2-TFT voltage-programmed pixel circuits were fabricated using a standard a-Si:H process at maximum temperature of 280°C in a bottom-gate staggered source–drain geometry. The 70-ppi monochrome display consists of (48 × 4) × 48 subpixels of 92 × 369 μm each, with an aperture ratio of 48%. The a-Si:H TFT pixel circuits drive top-emitting green electrophosphorescent OLEDs to a peak luminance of 2000 cd/m^2.

Keywords — *Stainless steel, flexible substrate, AMOLED, a-Si:H, thin-film transistor, electrophosphorescence.*

1 Introduction

Growing interest in flexible displays has extended to thin-film transistor (TFT) backplanes on stainless-steel-foil substrates. Steel foils are attractive because of their tolerance to high-temperature processing, dimensional stability, chemical resistance, impermeability to moisture and other atmospheric contaminants, and a relatively low coefficient of thermal expansion.[1] a-Si:H TFTs on steel foil have been demonstrated,[2] and single TFTs have been integrated with organic light-emitting diodes (OLEDs).[3] Polycrystalline silicon (poly-Si) TFTs, which exhibit higher electron mobilities than a-Si:H TFTs, have also been fabricated on steel foil.[4–8] Whether a-Si:H or poly-Si is the best choice for active-matrix organic light-emitting diode (AMOLED) display pixels on steel foil remains unclear. Because steel is opaque, it can only serve with top-emitting OLEDs. When integrated with top emitters, the a-Si:H pixel circuit, 2-TFTs plus a storage capacitor (C_s), may occupy most of the pixel area without reducing the display aperture ratio. In this case, the ratio is set solely by the width of the interconnects. Here, we show that the a-Si:H TFTs width-to-length (W/L) ratio can be made large enough[9,10] to deliver sufficient current to drive a top-emitting electrophosphorescent OLED.

We fabricated AMOLED backplanes with an active pixel driver matrix of 48 × 48 pixels and each pixel. Each pixel consists of four vertical strip subpixels with 92 × 369-μm footprints for future application in a red-green-blue-white (RGBW) display. Each subpixel circuit is made with a switching TFT (T1) of gate width to length ratio W/L = 50 μm/5 μm, a driver TFT (T2), with W/L = 200 μm/5 μm, and a storage capacitor $C_S \cong 2$ pF, as shown in Fig. 1(a). For expedient evaluation, the data lines of four subpixels are connected such that one data signal lights up one full pixel at a time. Figure 1(b) is the optical micrograph of one subpixel. The active OLED area is denoted by the dashed rectangle. By employing 20-μm-wide interconnect lines leaves a pixel aperture ratio of 48% was employed. A blanket electrophosphorescent[11,12] top-emitting[13,14] green OLED array with a transparent indium tin oxide (ITO) cathode completes the display. The sequence, composition, thicknesses, and energy levels of the OLED layers are shown in Fig. 1(c).

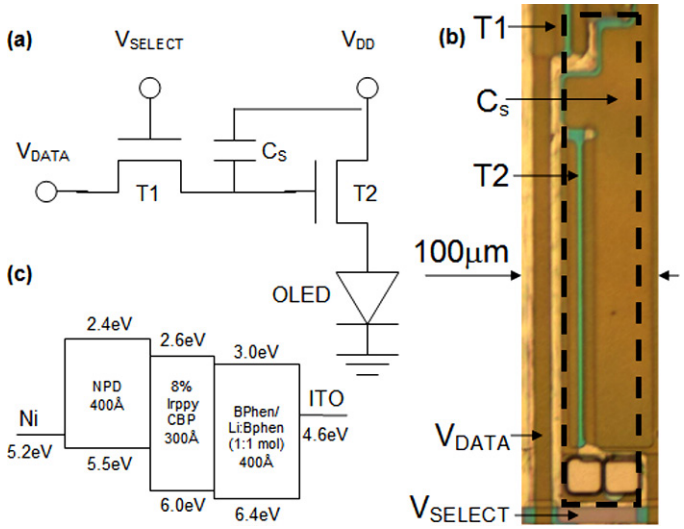

FIGURE 1 — (a) Circuit schematic of a display subpixel. (b) Optical micrograph of one pixel with the TFTs and capacitance, C_s indicated. The dashed-box outlines the location and size of the OLED. (c) Energy-level diagram of the OLED structure.

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2 Experiments

The 125-μm-thick 5 × 5 cm^2 stainless-steel-foil substrates had an "as-received" roughness of ~1.2 μm peak-to-peak. The roughness was due to unidirectional grooves formed when the steel is rolled into sheets. Along with this roughness, the substrate has point-defect-like inclusions with a height of ~1 μm. Because such roughness and defects decrease display yield by causing shorts in the OLEDs and breaks in the interconnect lines, we planarized the substrates with 2.5 μm of siloxane spin-on glass. Then, an electrically insulating layer of 200-nm-thick SiO_2 was deposited at 300°C by plasma-enhanced chemical vapor deposition (PE-CVD).[15] Next, a 90-nm-thick Cr gate metal layer was deposited by thermal evaporation and patterned using Cr-7S wet etch from Cyantek Corp.[16] The TFT stack of 340-nm-thick SiN_x, 200-nm-thick intrinsic (i) a-Si:H, and 50-nm-thick doped n^+ a-Si:H layer was deposited by PE-CVD at 500-mTorr using a 13.56-MHz RF power density of 66 mW/cm^2. The gate SiN_x was deposited at 280°C from SiH_4:NH_3 at a flow ratio of 1:9, the a-Si:H from SiH_4 at 230°C, and the n^+ a-Si:H from SiH_4:PH_3 = 70:1 at 230°C. Next, a-Si:H islands and gate vias were patterned by reactive ion etching (RIE) at 100 mTorr and power density of 140 mW/cm^2. A gas flow ratio of SF_6/CCl_2F_2 = 6:2 was used to etch the a-Si:H, and CF_4/O_2 = 7:1 for the gate vias. The source–drain and interconnect metal tri-layer of 50-nm-thick evaporated Cr, 200-nm-thick sputtered Al–1% Si, and 50-nm-thick sputtered Cr layer were then deposited. Al–1% Si has a low tendency for hillock formation,[17] and sputtering ensures good step coverage and low via and interconnect resistances. The Cr was patterned with Cr–7S wet etch, and the Al–1% Si using a mixture of H_3PO_4:H_2O:HNO_3:CH_3CO_2H = 6:2:1:1. The n^+ layer was etched with RIE at 100 mTorr and 140 mW/cm^2 by CCl_2F_2:O_2 = 7:1, which completed the TFT pixel circuits.

Prior to OLED deposition, the TFT backplanes were passivated with a 1-μm-thick layer of SiN_x deposited at 200°C by PE-CVD from SiH_4:NH_3 = 1:9 at 500 mTorr using a power density of 66 mW/cm^2. Next, vias for the T2 source-to-OLED anode connection were etched by RIE using CF_4/O_2 = 7:1. A bi-layer anode of 200-nm-thick Al–1%Si and 50-nm-thick Cr was then deposited and patterned. To planarize the TFT relief replicated in the SiN_x layer, AZ5209 photoresist was spun on at 4000 rpm, patterned to form windows to the anode and baked at 200°C for 10 min to form windows to the anode. A 5-nm-thick layer of Ni was sputter-deposited and exposed to UV-generated O_3 for 5 min to oxidize the Ni surface in preparation for OLED deposition.

The organic layers, shown in Fig. 1(c), were sequentially deposited from pre-purified[18] source materials by thermal evaporation at rates of 2–3 Å/sec without breaking vacuum (1×10^{-7} Torr). Hole transport between the oxidized Ni anode and the emissive layer was facilitated by a 400-Å-thick layer of 4,4′-bis[N-(1-naphthyl)-N-phenyl-amino]-biphenyl (NPD). The emissive layer consists of 300 Å of 4,4′-bis(N-carbazolyl)biphenyl (CBP) co-doped at 10 wt.% with the metalorganic phosphor, *fac*-tris(2-phenylpyridine) iridium [$Ir(ppy)_3$].[11,12] A 200-Å-thick layer of 4,7-diphenyl-1,10-phenanthroline (BPhen), followed by a 200-Å-thick Li-doped BPhen layer at a 1:1 molar ratio,[14] serve to transport electrons from the cathode while confining excitons within the emissive layer. The structure was completed by depositing the transparent 50-nm ITO cathode through a shadow mask, using RF magnetron sputtering at a power of 100 mW/cm^2 to obtain a rate of 0.5 Å/sec.[13] Control devices of the same structure were grown on glass substrates. They had peak forward-emitted external quantum efficiency of (3.0 ± 0.2)% at a luminance of 200 cd/m^2.

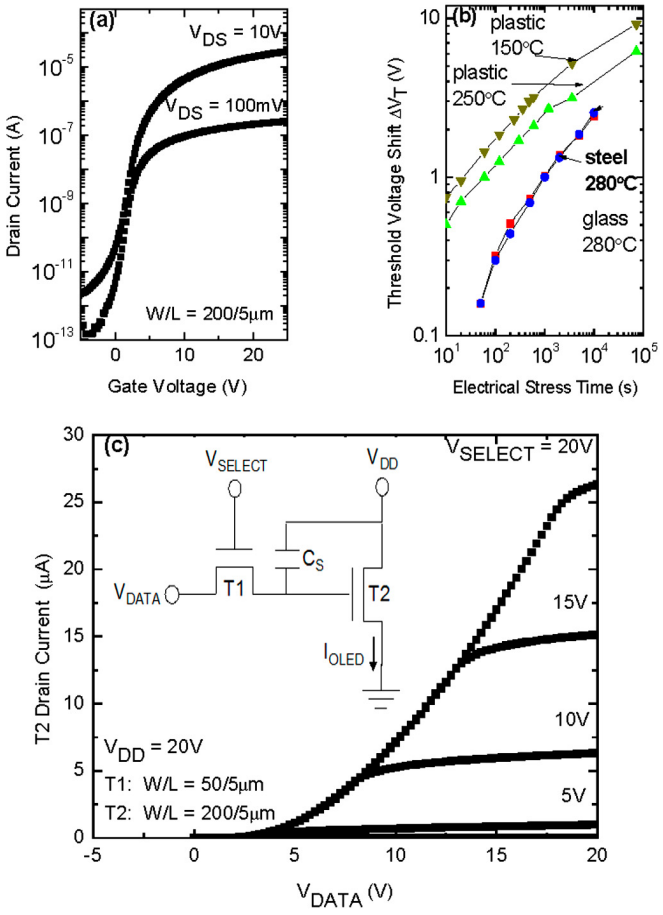

FIGURE 2 — (a) Transfer characteristics for the a-Si:H TFT for drain-to-source voltages (V_{DS}) of 100 mV and 10 V. (b) Threshold-voltage shift (δV_T) *vs.* stress time for TFTs deposited at 280°C on steel and glass, including results for 150°C and 250°C TFTs on plastic for comparison.[19] The 280°C TFTs on steel and glass have almost the same ΔV_T. (c) Source current for T2 (OLED) in a subpixel circuit versus V_{DATA} for V_{SELECT} = 0–20 V in 5-V steps.

3 Pixel circuit and display results

Electrical characteristics were measured using an HP4145 parameter analyzer. The transfer characteristics of an a-Si:H driver TFT (T2) are shown in Fig. 2(a). The TFTs have a threshold voltage $V_T \cong 3$ V, current ON/OFF ratio $I_{ON}/I_{OFF} \cong 10^7$, sub-threshold slope $S \cong 500$ mV/dec, and

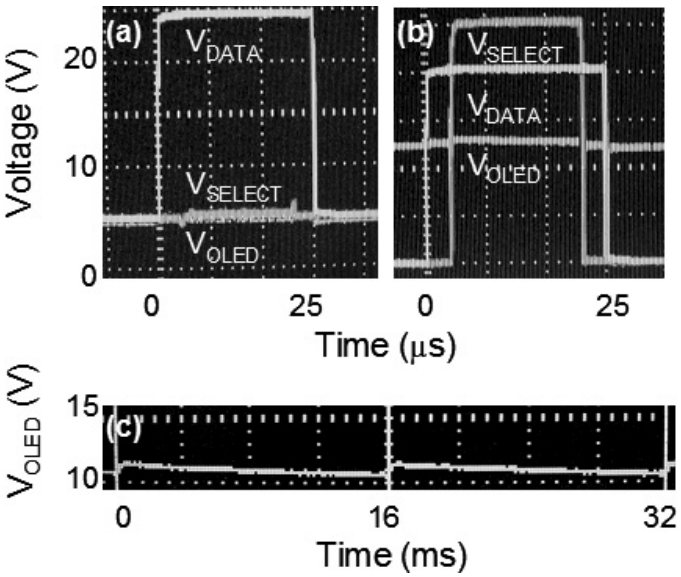

FIGURE 3 — Transient measurements of V_{OLED} using a 16-msec frame time and V_{DATA} width of 26 μsec and 20 V for (a) V_{DATA} = 25 V and V_{SELECT} = 0 V, (b) V_{DATA} = 20 V and V_{SELECT} = 25 V, and (c) two frames.

saturation electron mobility $\mu_{sat} \cong 0.5$ cm^2/V-sec. The stability of the TFTs was tested at a fixed gate-to-source/drain field of 10^6 V/cm, applied in successive stress periods of 10–10,000 sec. After each period, the transfer curve was measured and the threshold voltage was extracted. Figure 2(b) is a plot of ΔV_T *vs.* gate-bias stress time. The plot includes results for a-Si TFTs deposited at 150°C and 250°C[19] on plastic and at 280°C on glass. Deposition at high temperature clearly improves TFT stability. Steel-foil substrates have an advantage over most plastic substrates in their temperature tolerance.

The 2-TFT pixel circuits were evaluated before OLED deposition by grounding the source of T2 in the absence of an OLED load, with results shown in Fig. 2(c). The select line voltage (V_{SELECT}) was stepped in 5-V intervals from 0 to 20 V, and the data input voltage (V_{DATA}) was swept from 0 V to 20 V, at a power supply voltage V_{DD} = 20 V. At an OLED terminal, the leakage current of the pixel at $V_{DATA} = V_{DD}$ = 20 V and V_{SELECT} = 0 V lay below ~10 pA; the output current reached 26 μA at $V_{DATA} = V_{SELECT}$ = 20 V.

Transient voltage measurements were performed on a pixel circuit within the array, to ascertain sufficiently low pixel leakage during a frame time. A 1-MΩ resistor substituted for the OLED. The pixel was biased with V_{DD} = 20 V and was pulsed with V_{SELECT} between 0 and 25 V and V_{DATA} between 0 and 25 V. The pulse widths were 26 μsec for V_{DATA} and 20-μsec for V_{SELECT}, and the frame time was 16 msec. Figure 3(a) shows that V_{OLED} remains at 0 V when V_{SELECT} = 0 V. Figure 3(b) is one in a sequence of identical frames, which show that V_{OLED} = 12.5 V, corresponding to a T2 current of 12 μA at V_{SELECT} = 25 V. Figure 3(c) shows two frames (32 msec) with a drop in V_{OLED} voltage of <350 mV per frame.

Completed OLED pixels were biased using an HP4145 analyzer, and the luminance of individual OLEDs was measured using a calibrated photodiode.[20] Figure 4(a) shows the luminance versus V_{DATA} and V_{SELECT} at V_{DD} = 25 V for one such pixel. For V_{SELECT} < 4 V no luminance was observed and the maximum luminance of ~2000 cd/m^2 was reached at $V_{DATA} = V_{SELECT}$ = 25 V. A target luminance of ~100 cd/m^2, which is a standard number for a desktop display,[9,10] is reached at V_{DATA} = 7 V and V_{SELECT} = 10 V. This turn-on voltage could be further reduced by using a more efficient OLED. To evaluate the functionality of the full display while it is flexed we tied all the address lines together, and bent it to a radius of ~50 cm. The pixel emission was uniform as evident from Fig. 4(b). The entire display is shown in Fig. 4(c).

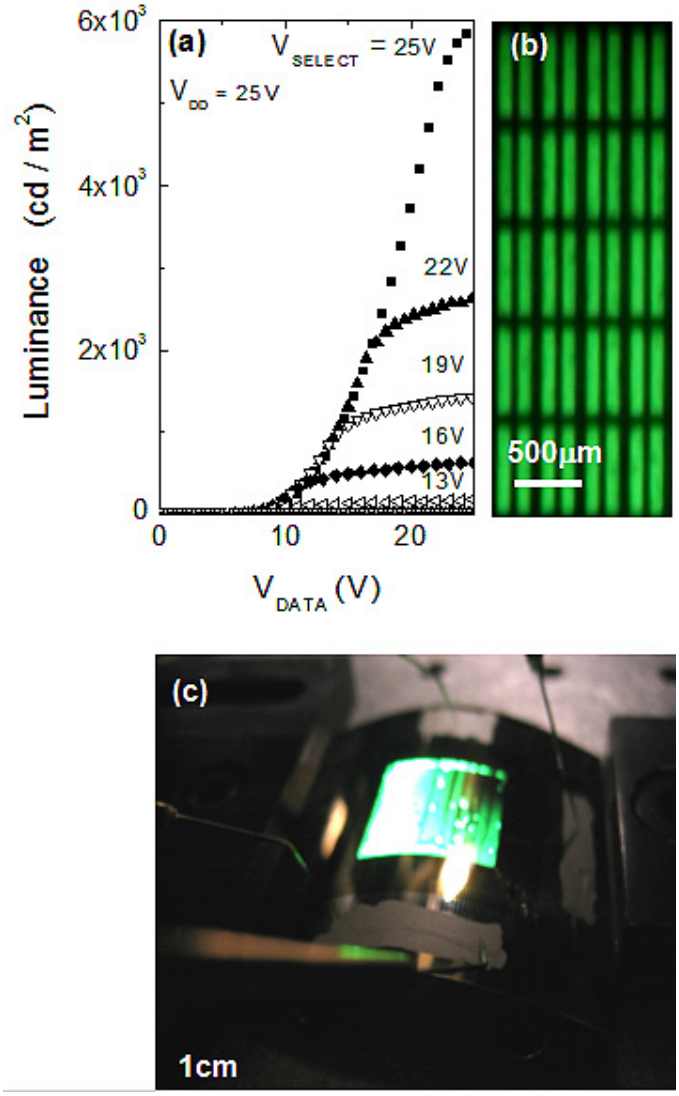

FIGURE 4 — (a) OLED luminance versus V_{DATA} for V_{SELECT} = 13–25 V in 3-V steps. (b) Optical micrograph of a subarray of 8 × 5 active subpixels. (c) Entire display flexed to a radius of 50 cm.

4 Conclusions

We demonstrated an AMOLED display using 2-TFT a-Si:H pixels circuits fabricated at 280°C on flexible stainless-steel foil. We conclude that an a-Si:H TFT backplane based on flexible steel foil can power a bright top-emitting AMOLED display based on electrophosphorescent OLEDs. The stability of the TFTs on steel was measured and found to be superior to low-temperature a-Si:H TFTs on plastic and performs comparably to our results on display glass. The next step is to implement a design using 4-TFT pixel circuits for improved long-term stability of AMOLED operation.[9,10]

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