6.5.1.3 ZnO TFTs with SiO_2 gate dielectric

As a comparison, ZnO TFTs with SiO_2 gate dielectrics were subjected to negative bias-temperature-stress studies. In this case, there are some similarities between instabilities with HfO_2 and SiO_2 gate dielectrics. Figure 6.21 shows both ΔV_T and ΔV_{TH} for TFTs with SiO_2 dielectrics. Both values are plotted because SiO_2 does not suffer threshold PBTI and thus the NBTI data is not confounded due to gate voltage range.

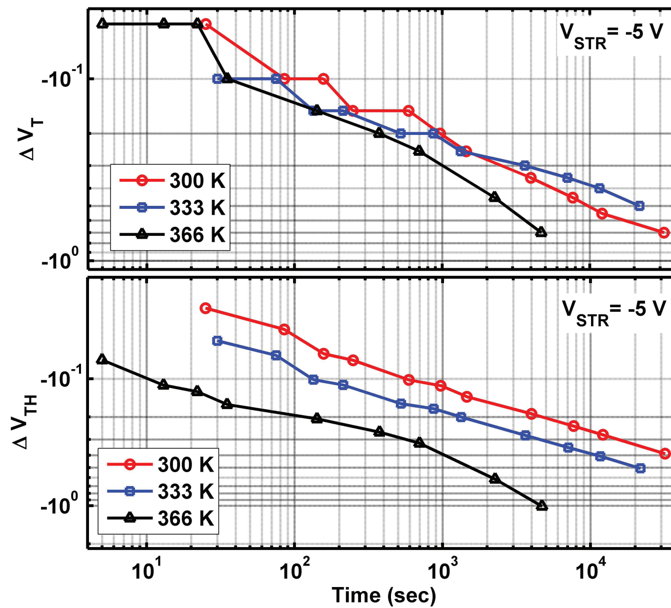

Figure 6.21: ΔV_T (top) and ΔV_{TH} (bottom) vs $\log_{10}(t_{STR})$ over range of T_{STR} values for TFTs with SiO_2 dielectrics.

SiO_2 data exhibits exponential behavior with logarithmic time in a similar fashion to HfO_2 data. ΔV_{TH} values also exhibit temperature dependence similar to the HfO_2 case. The key differences are that the SiO_2 instabilities are less in magnitude and there is no indication of NBTI saturation nor a region where the slope changes.

The similarities of NBTI between devices with HfO_2 and SiO_2 indicate there is likely a ZnO based mechanism, at least partially, at play governing NBTI of ZnO/HfO_2 TFTs.

6.5.2 NBTI Discussion

NBTI investigation of ZnO TFTs with HfO_2 gate dielectrics has yielded many clues as to the source mechanism governing the instabilities:

- ΔV_T temporal characteristics indicate charge state creation.
- ΔS temporal characteristics indicate that interface states are changing with T_{STR} and t_{STR}.
- Both ΔV_T and ΔS show a two-region type of temporal behavior where the change in region may correlate between both parameters. This may indicate a link between interface states and the threshold voltage
- NBTI studies on TFTs with SiO_2 gate dielectrics show similarities with HfO_2 dielectrics indicating, at least part of, the source mechanism resides in the ZnO.

Unlike the PBTI case, a comprehensive explanation for NBTI results has not yet been determined.

6.6 Summary

In this section the instabilities of ZnO TFTs with HfO_2 dielectrics have been presented. Positive gate bias-temperature-stress instability results show the dominant instability mechanism is charge trapping by carrier injection into the HfO_2 and a new method was presented to fully characterize V_{TH} instabilities and extract dielectric charge trap density.

Negative gate bias-temperature-stress instability results show the dominant mechanism is likely charge state creation, which could result from states created at the channel/dielectric interface or in the ZnO semiconductor. V_T data can be characterized by a fit to a model developed to describe charge state creation in a polycrystalline semiconductor.

CHAPTER VII

Illumination Stability Investigation on High-k/ZnO Devices

7.1 Introduction

Exhibiting high mobility, transparency in the visible spectrum, and compatibility with large area, flexible, and low temperature deposition methods Zinc-Oxide (ZnO) based semiconductors have become a major research focus over the past decade. Recently, the display community has shown great interest in ZnO based devices as the successor of amorphous and polycrystalline Silicon currently used in many thin-film applications. For example, next generation Active Matrix Liquid Crystal high resolution displays with 4000 x 2000 pixels, a high frame rate (>240 Hz), and sized larger than 70 inches a thin-film semiconductor with mobility above 3 cm^2/Vs are required [41]. Amorphous silicon (a-Si) cannot achieve this value. Low Temperature Poly-Silicon (LTPS) has the mobility performance, but the high thermal budget makes this a poor candidate for flexible and novel substrates. In addition, Silicon is opaque and sensitive to visible light [16]. As a result, ZnO based thin-film semiconductors have been heavily researched. The integration of high dielectric constant (high-k) insulators in ZnO TFTs has demonstrated performance advantages as discussed and reported in prior chapters. Subsequently, ZnO TFTs with high-k dielectrics are also of

importance to the electronic display community. It is important to investigate device stability to gain understanding about the material system and improve transistor performance. Active Matrix Organic Light Emitting Diodes (AMOLEDs) are currently driven by LTPS in small screen applications like hand-held devices, but electrical uniformity issues preclude LTPS from large area applications and correction circuits have to be used for even modest mobile screen sizes [41]. ZnO based thin-films can be used for this application as the switching transistor and driving transistor. In both cases threshold voltage stability is an important issue as driving transistor threshold voltage instability of only 0.1V could result in 20% change in luminance [31]. It is clear illumination stability is a critical issue as ZnO is a likely candidate for many future transparent and display applications where TFTs will be directly exposed to light in the visible spectrum. Prior work on ZnO-based semiconductor TFT bias-illumination instability has indicated that illumination typically causes or enhances negative threshold voltage shifts [74, 33, 83]. Three mechanisms have been reported as governing these instabilities: photo generated interface/dielectric hole trapping [74], photo desorption of oxygen related molecules [83], and creation of photo excited donor states [40]. In addition, reports have shown a dielectric dependence on light-induced instabilities of ZnO-based amorphous semiconductors [33, 40]. The light-induced instabilities of nanocrystalline ZnO with HfO_2 gate dielectrics have not been investigated to date and are reported in this chapter.

7.2 Sample Preparation

Samples used in this study were made from AFRL ZnO and HfO_2 as discussed in Chapter II, but also fabricated at AFRL using similar techniques as discussed in Chapter IV. The only differences were that ohmic contacts are Ti/Au (500/3500 Å) and mesa isolation was carried out with a dilute HCl etch. These devices show gate width and length corrected performance nearly identical to devices fabricated at the

University of Michigan. A picture of the multi-fingered devices used in this study can be seen in Figure 7.1.

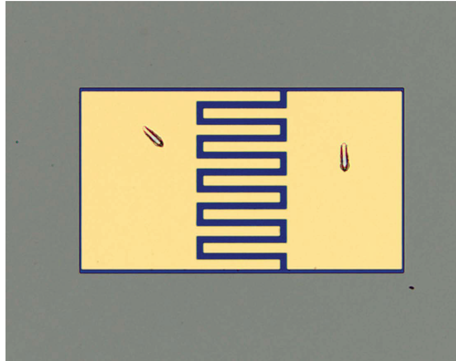

Figure 7.1: Picture of ZnO TFT fabricated at Air Force Research Laboratory. Gate Length = 5 μm, Gate Width = 50 μm X 10 fingers = 500 μm.

Half-wafer samples were sent to the University of Michigan. For illumination studies, half-wafers were cleaved into small pieces. Each piece contained, roughly, one die site. This was done so that a minimum number of devices were exposed to light in each experimental case. The method allowed data to be taken on un-tested, un-illuminated devices to eliminate history effects, which would otherwise confound the results reported in this chapter.

7.3 Testing

Electrical testing was carried out with the exact same method used in the Bias-Temperature-Stress Investigation (6.3). In each illumination case $V_{STR} = 0$ volts and $T_{STR} = 300$ K. Illumination was performed by attaching one end of a 6 foot 1/2" diameter fiber optic light guide to the probe station objective fixture so that light could be directed onto the sample chuck, where the device was measured electrically. The other end of the light guide was fixtured to a light source for maximum source light and minimum stray light transmission. A schematic diagram of the test setup can be seen in Figure 7.2.

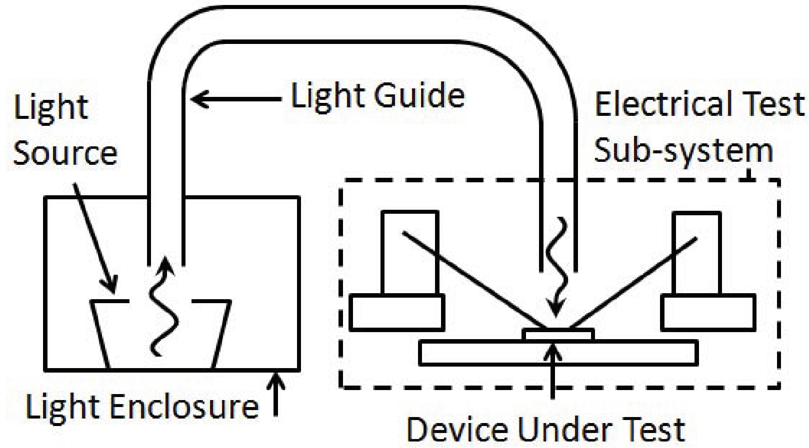

Figure 7.2: Schematic diagram of illumination instability test bench.

Red, Green, and Blue LEDs with Gaussian wavelength profiles and a UV BLAK-RAY brand light source fitted with a violet low pass filter were used. The optical power at the device was calibrated with a Melles Griot Broadband Optical Power Meter. Wavelength content information can be found in Table 7.1.

Color	Peak Wavelength (nm)	Radiation Energy (eV)	FWHM (nm)	Intensity (mW/cm^2)	Flux ($m^{-}2s^{-1}$)
Red	631	1.93	32	2.56	$8.1x10^{19}$
Green	525	2.36	65	2.43	$6.4x10^{19}$
Blue	452	2.74	61	2.75	$6.3x10^{19}$
UV	300 - 450	4.1 - 2.7	Not Gaussian	2.55	$4.7x10^{19}$ (for 375 nm)

Table 7.1: Light source specifications

7.4 Bias-Temperature-Illumination Stress Investigation

In this section an investigation of the effects of illumination on TFT stability is presented. TFTs were biased at $V_{GS} = 0$ V and $I_{DS} = 0$ V with a chuck temperature of 300 K. Two initial 'dark' I_D-V_G curves are taken. [*The first curve acts as a PBTI stabilization curve so the second dark curve can act as a true 'dark' control. This*

method allows for the illumination curves to be compared to a 'dark' curve without PBTI confounding.] Then the device was illuminated at a given wavelength and repeatedly re-measured over the course of 8x10^3 seconds.

7.4.1 Raw Data

Typical TFT transfer curves reported in all chapters are acquired by sweeping the gate voltage from negative to positive values. As discussed in Chapter III, slight hysteresis is seen in our ZnO/HfO_2 devices if they are swept from negative to positive gate voltages and then back to negative voltages as exhibited in the 'dark curve' in Figure 7.3.

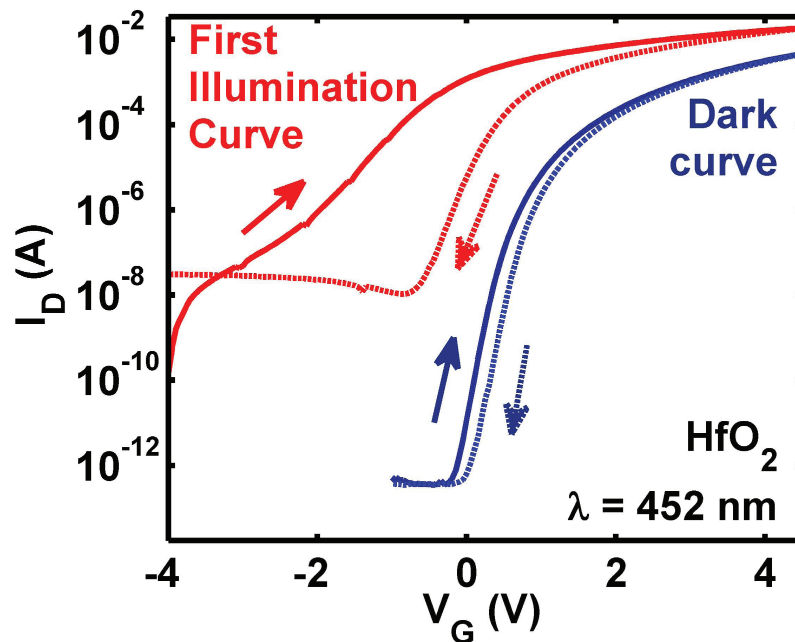

Figure 7.3: TFT Typical dark and illuminated data exhibiting different hysteresis effects.

Under illumination, however, the hysteresis effects change significantly. From the 'First Illumination Curve' in Figure 7.3 it can be seen that sweeping from negative V_G to positive V_G (termed the forward sweep) results in a curve with a multi-sloped subthreshold region and significant V_{TH} shift compared to the dark curve. Sweeping

from positive to negative V_G results in a curve with similar V_{TH} shift, but with different subthreshold characteristics and a clear I_{OFF} value. Initially, this clear change in hysteresis indicates illumination has an effect on the interface, but one issue that complicates analysis is the discovery that the forward illumination sweep is actually dependent on the starting V_G value. This issue is illustrated in Figure 7.4 where from the $\log(I_D)$ plot (left curves) it can be seen that the subthreshold characteristics change, not with light, but with the starting gate voltage value ($V_{G-Start}$). From the $I_D^{1/2}$ plot (right curves) it can be seen that the threshold voltage shifts, not with illumination, but with $V_{G-Start}$. In addition, a stable off state was not found in the range of $V_{G-Start}$ values investigated.

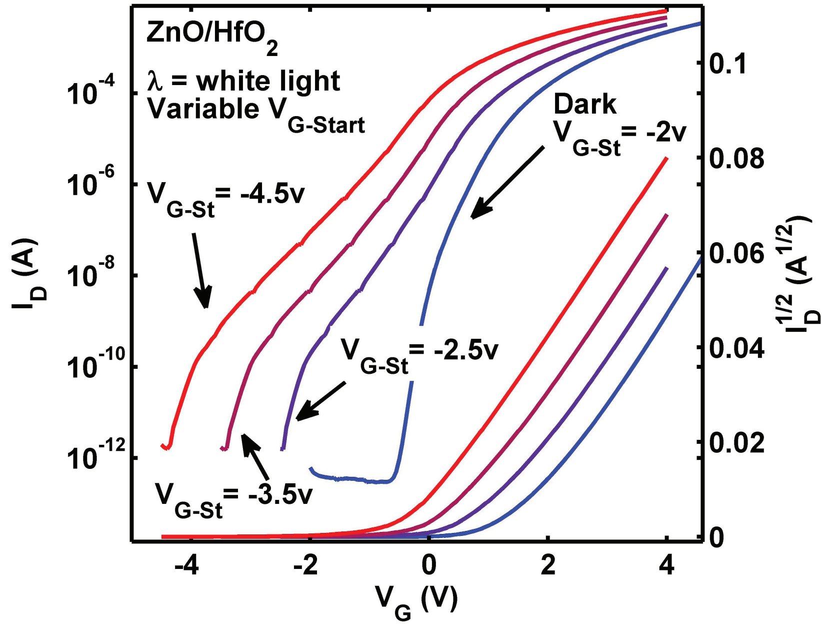

Figure 7.4: Illuminated Forward sweeps with variable gate starting voltage.

Reverse sweeps, however, demonstrate stable I_D-V_G characteristics that coherently trend with illumination photon energy and illumination time. For this reason, reverse sweep data is presented and analyzed in the following subsection. The forward sweep instabilities will be considered in the discussion later in this chapter.

7.4.2 Reverse Directional Sweep Data

A typical family of curves can be seen in Figure 7.5. For all wavelengths, each family of curves exhibited a negative ΔV_{TH}, positive ΔI_{OFF}, and positive ΔS. Figure

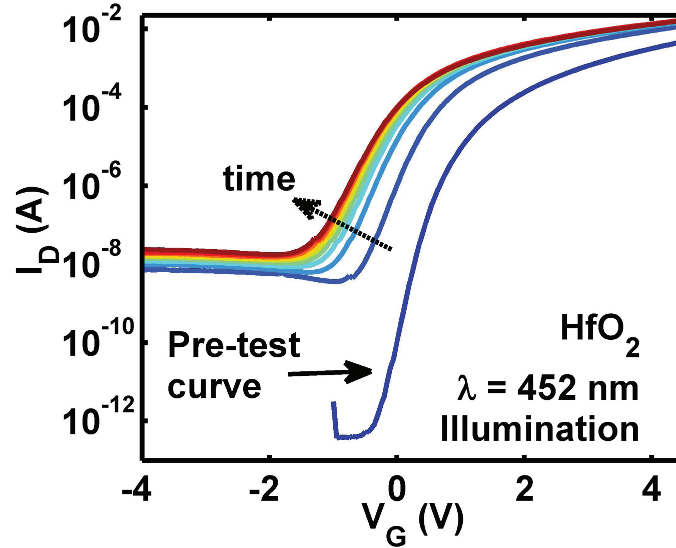

Figure 7.5: Family of TFT curves taken over the course of one illumination measurement with green illumination.

7.6(a) shows the trend in I_{OFF}, with wavelength. I_{OFF} gently increases over the first many hundreds of seconds and levels off at a value that increases with radiation energy. Figure 7.6(b) shows ΔS versus time (t_{STR}) where subthreshold slope is evaluated over a different current range for each wavelength. This was necessary due to I_{OFF} values often above typical subthreshold slope evaluation windows. Each curve shows a logarithmic-like initial increase and then a leveling off. No trend is seen with energy. Figure 7.6(c) shows the trend in V_{TH} with wavelength showing an initial exponential decay with similar logarithmic time slopes and increasing magnitudes with radiation energy. Figure 7.6(d) shows the trend in $\Delta\mu_{SAT}$. There are perhaps two regions of change in $\Delta\mu_{SAT}$ temporal characteristics; First a region of linear increase where the slope increase with light energy. 631 nm $\Delta\mu_{SAT}$ increases slowly, 525 nm $\Delta\mu_{SAT}$ increases over the first 8x10^2 seconds, and 452 and 370 nm curves show an increase in

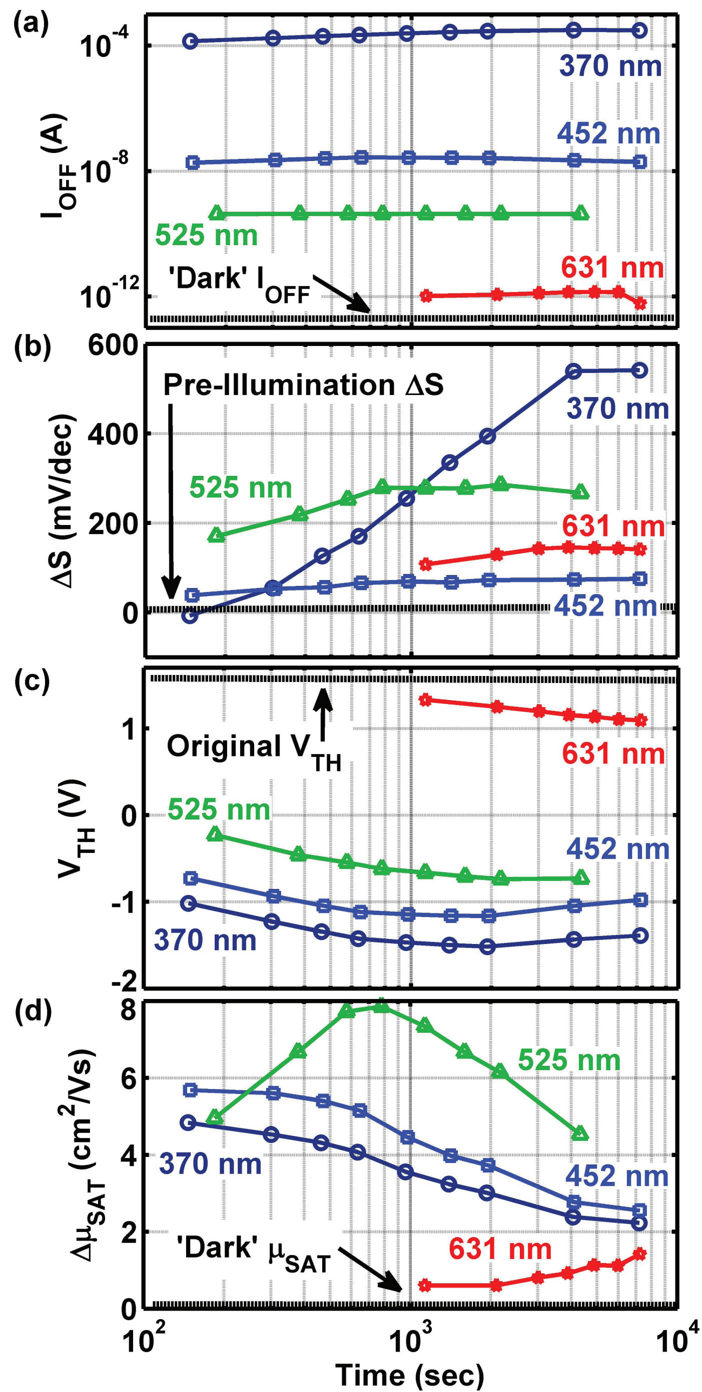

Figure 7.6: Thin film transistor parameter data for polycrystalline ZnO TFTs under various wavelength illumination.

mobility in the first illumination curve. The second temporal region is a region where after the increase in mobility, there is an exponential-like decay to an intermediate value.

After illumination each TFT was left in the dark and transfer characteristics were periodically measured to record recovery characteristics. Figure 7.7 shows two families of recovery curves including the last illumination and pre-illumination curves, for comparison.

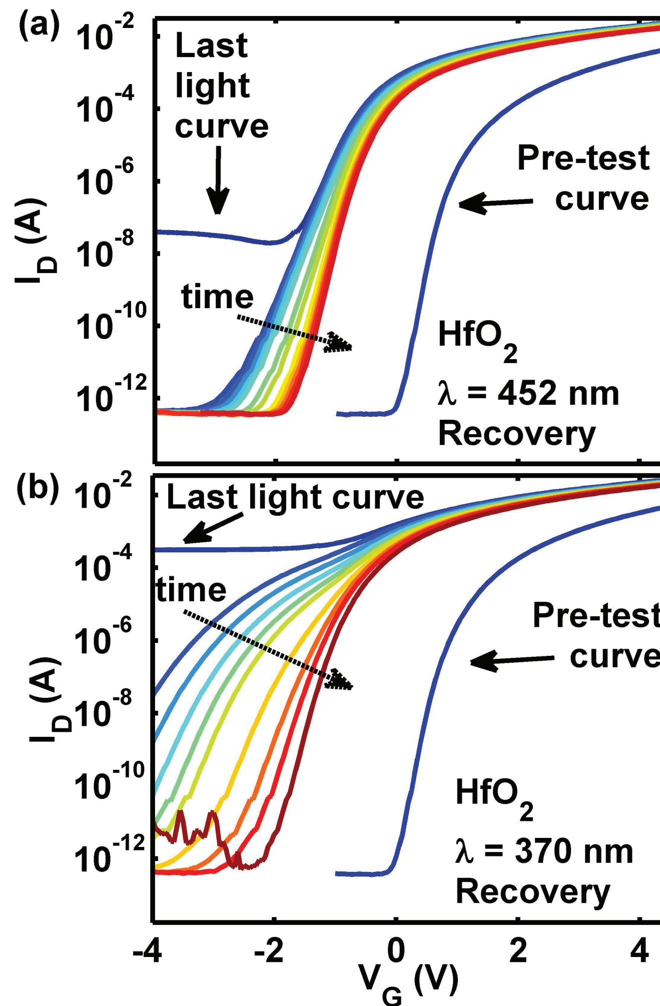

Figure 7.7: Recovery characteristics can be seen in family of TFT I_D-V_G curves for blue (a) and UV (b) illumination.

V_{TH} and S recovered partially over the measurement period with a logarithmic shape while I_{OFF} recovered fully and immediately as seen in Figure 7.7(a). Figure

7.8(b) shows subthreshold slope recovery data. Independent of energy, subthreshold slope values converge to nearly pre-illumination values. Figure 7.8(a) shows the trend in V_{TH} recovery only a fraction (less than 50% in all cases and 10% for 525 nm case) of the total is recovered in an order of magnitude more time than the illumination period. Figure 7.8(c) shows $\Delta\mu_{SAT}$ recovery data where no dominant trend is observed.

7.4.3 V_{TH} Analysis

Threshold voltage characteristics have an initial trend of linear increase of -ΔV_{TH} with logarithmic time. In the case of energies above 1.96 eV, the slope levels off at time values above 1x10^3 s. Linear increase with logarithmic time is indicative of charge trapping in a TFT system [75]. Elements in the system that could contribute to threshold voltage are increased carriers, interface charge, surface charges, and traps in the semiconductor.

From I_{OFF} data, we know that there are an increased number of carriers in the system due to photo generation. Increased carrier concentration lowers V_{TH}, but because I_{OFF} recovers very quickly and V_{TH} does not, increased carrier concentration cannot be the sole mechanism responsible for ΔV_{TH}.

Interface trapped charges need to be considered in the illuminated ZnO/HfO_2 system as increased positive charge would contribute to -ΔV_{TH}. Three reasons exist indicating that interface states are not the governing mechanism for ΔV_{TH}: First, there is no gate voltage influencing channel minority carriers towards the interface or dielectric. Second, the recovery temporal characteristics of V_{TH} are slow, but interface trapped charge is expected to recover quickly, in many seconds or minutes [17]. While charge at the interface or in the dielectric could play a role in ΔV_{TH}, we do not see strong evidence of this in our data.

Since our devices are not passivated it is necessary to consider effects due to the exposed backside semiconductor surface. Photo desorption of oxygen and water

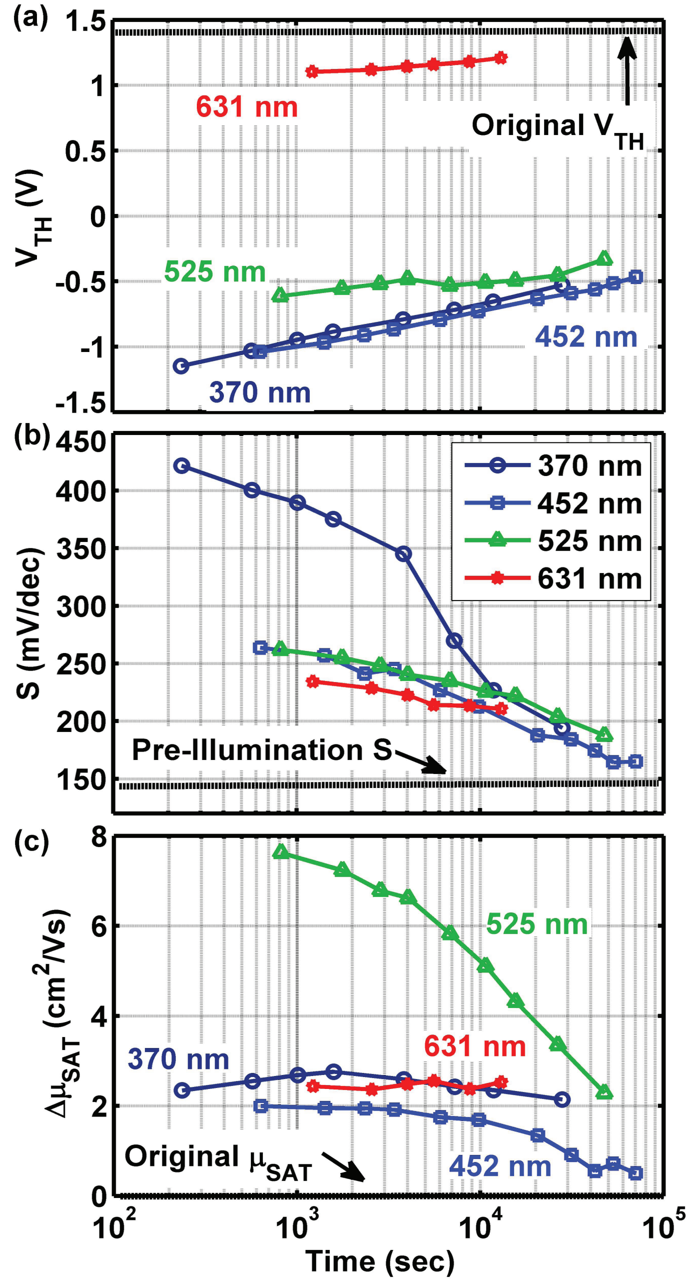

Figure 7.8: Recovery characteristics for V_{TH}, S, and $\Delta\mu_{SAT}$.

molecules from the surface of ZnO-based semiconductors has been reported to cause negative threshold voltage shifts [41]. Conversely, there have been reports of negative threshold voltage shifts which are independent of oxygen ambient or, despite unpassivated surfaces, governed by a different mechanism [40]. We do not report on the dependence of surface charges in this work, but do show strong evidence that ΔV_{TH} is, at least partially, governed by grain boundary trap states, as discussed in the next several paragraphs.

Aside from interface trap charges, dielectric trap charges, and surface states, grain boundary trapped areal charge density (N_{GB} cm^{-2}) could be present and influencing ΔV_{TH}. If grain boundary trap states play a role, one would expect ΔN_{GB} to correlate with ΔV_{TH}. N_{GB} in polycrystalline ZnO can be determined from the square root of the slope of $\ln(I_D/V_G)$ versus $1/V_G$ (Equation 7.1) as described by Levinson et al. [25, 43] and derived from Equations 7.2 and 7.3, which are discussed below.

$$N_{GB} = \sqrt{|slope|} \cdot \sqrt{\left(\frac{8\epsilon_s kTC_{OX}}{q^3 t_s}\right)} \tag{7.1}$$

Figure 7.9 shows a representative plot used to extract N_{GB} from the range of I_D-V_G near maximum V_G.

Figure 7.10 shows values for extracted grain barrier areal trap density. For each sample, pre-illumination N_{GB} = 4.21$\pm$ 0.04 x10^{12} cm^{-2}. Over the course of illumination testing N_{GB} dropped with increased photon energy and also with illumination time. The trends of N_{GB} with time and photon energy are similar to those of V_{TH}. In fact, figure 7.11 shows the strong correlation between the decrease in N_{GB} and increase in negative threshold voltage shift for all radiation energies.

The strong correlation between grain boundary trap charge and threshold voltage indicates there is a link in the mechanism reducing N_{GB} and shifting threshold voltage. This correlation can be described by the model developed for polycrystalline semiconductor conduction based on thermionic emission above grain boundary barriers.

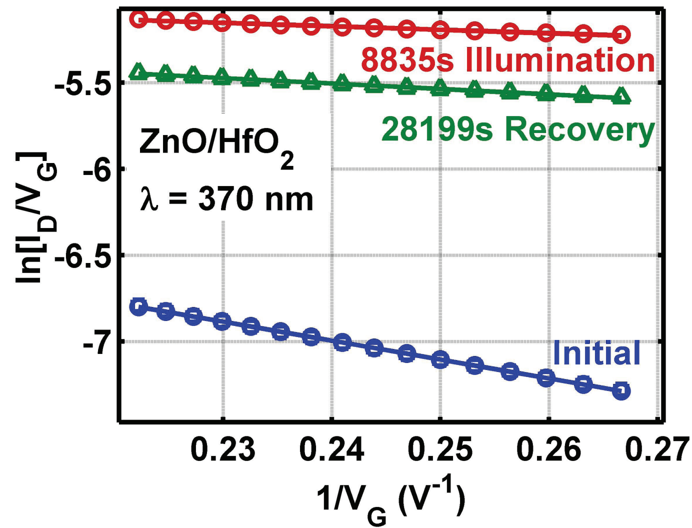

Figure 7.9: Plot of $\ln(I_D/V_G)$ versus $1/V_G$ for three time points of the UV illumination/recovery measurement. Circle, triangle, and square markers represent data and the solid lines are the fit used to extract the slope used in Equation 7.1.

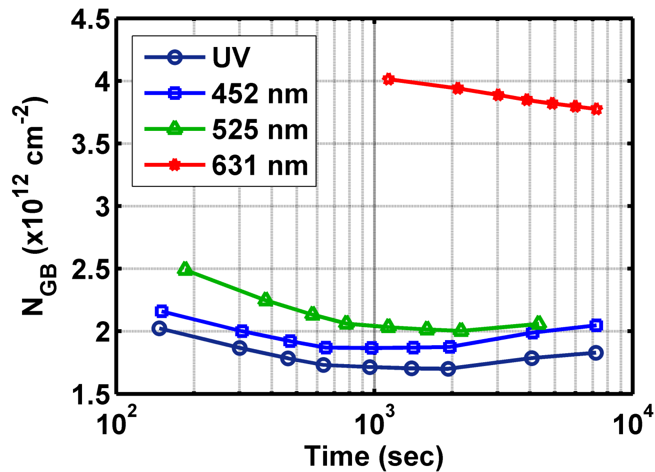

Figure 7.10: Plot of N_{GB} extracted according to Levinson [43].

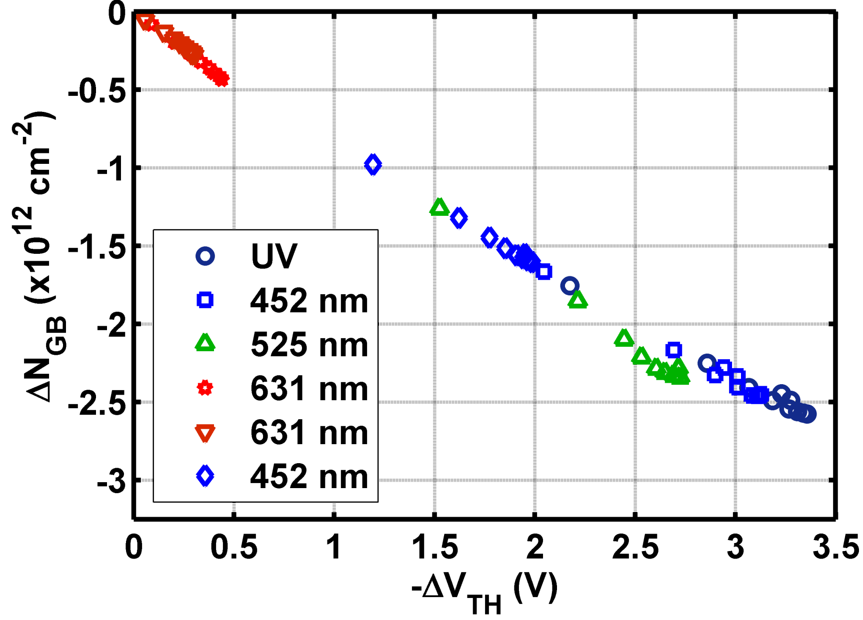

Figure 7.11: Plot of ΔN_{GB} versus -ΔV_{TH}.

The Equation developed takes the following form

$$I_D = \mathrm{w}\mu_b \frac{V_D}{l} C_{OX} V_G e^{(-E_B/kT)} \tag{7.2}$$

$$\frac{-E_B}{kT} = \frac{-q^3 N_{GB}^2 t}{8\epsilon k T C_{OX} V_G} \tag{7.3}$$

where w and l are gate width and length, μ_b is the scattering adjusted grain barrier mobility, and t is the semiconductor thickness [43]. Equation 7.2 is based on the assumption that there are partially depleted grains, which is valid for this system.

Using extracted N_{GB} values, the 'ideal' trends of I_D-V_G with varying N_{GB} can be analyzed and compared to experimental data. Figure 7.12a shows $\sqrt{I_D}$ - V_G experimental data; each curve represents a different illumination time. Figure 7.12(b) shows simulated data, using Equation 7.2, where each curve assumes a different grain boundary trap density. The N_{GB} input values were extracted from the experimental data plotted in 7.12(a). The simulation is plotted in normalized units to show the

good agreement in the shape and trend with N_{GB} between the experimental and modeled curves.

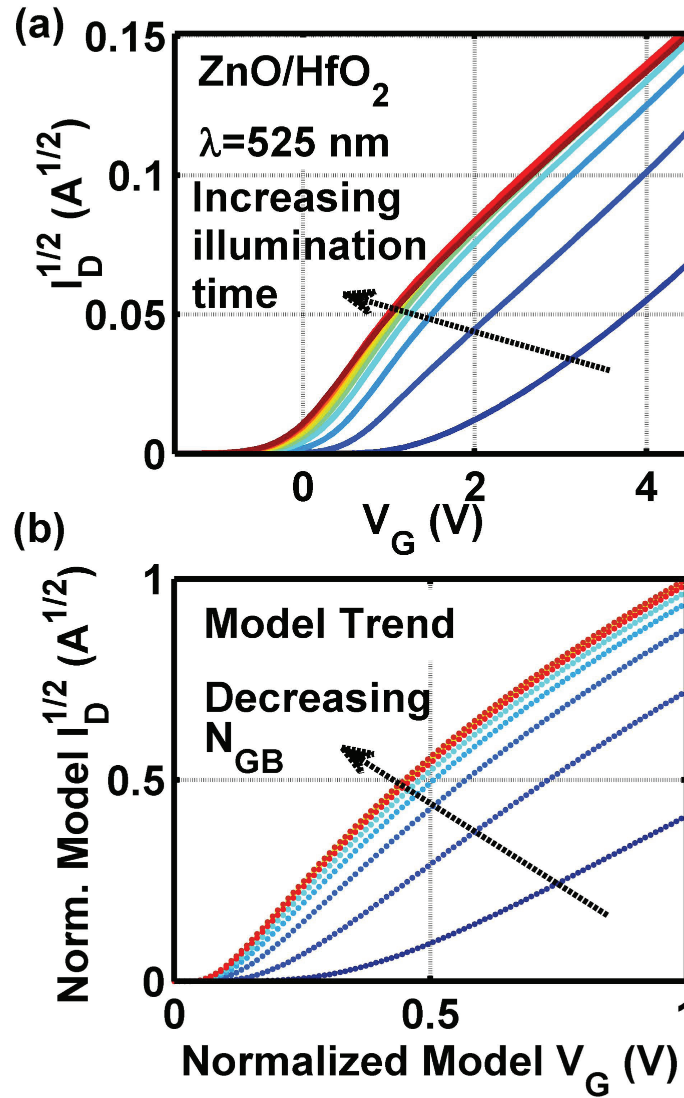

Figure 7.12: (a) Experimental data exhibiting characteristics of polycrystalline thin film transistor dominated by thermionic emission above grain boundary barrier. (b) Model data using Equation 7.2. The N_{GB} values extracted from (a) are the inputs into (b).

It can be seen that varying N_{GB} as extracted experimentally results in trends in shape and values of modeled I_D-V_G curves, which would lead to shifts in extracted threshold voltage. It is clear that a reduction in N_{GB} can cause the negative ΔV_{TH} witnessed experimentally.

With respect to the illumination dependence and effect; one assumption made in the development of Equation 7.2 is that traps are assumed to be initially neutral and become charged by trapping a carrier. Since ZnO is intrinsically n-type, we assume that the neutral traps are already filled in the as-processed case. Therefore, upon illumination a photon can give its energy to a trapped carrier exciting it out of the trap and reducing the overall charge density, thus influencing the system according to the discussion above. The band structure of a semiconductor with N_{GB-1} compared with a semiconductor with N_{GB-2} where $N_{GB-2} > N_{GB-1}$ can be seen in Figure 7.13.

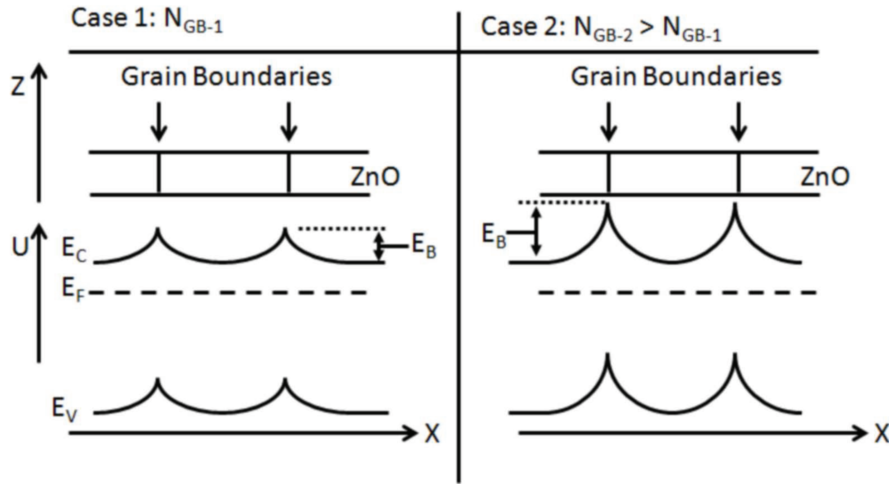

Figure 7.13: Band diagram view of polycrystalline grain boundaries limiting conduction to thermionic emission over barriers of height E_B, which is proportional to N_{GB}^2/N_D (Adopted from [43]).

7.4.4 I_{OFF} Analysis

The UV case is the only illumination source with energy above the ZnO bandgap. As a result, I_{OFF} energy dependence indicates that there are sub-bandgap states that allow light with sub-bandgap energies (< 3.37 eV) to interact with carriers. Increasing I_{OFF} with increasing radiation energy indicates states are distributed throughout the bandgap. Figure 7.14 shows a plot of I_{OFF} vs radiation energy. I_{OFF} with radiation

energy is consistent with sub-bandgap absorption decreasing exponentially below the band edge due to band tail states. It should be noted that data was taken at constant optical power density (W cm^{-2}), not constant flux density (# photons s^{-1} m^{-2}) which, as a result, is decreasing with increasing energy. The curve in Figure 7.14 would be steeper for the case of constant flux.

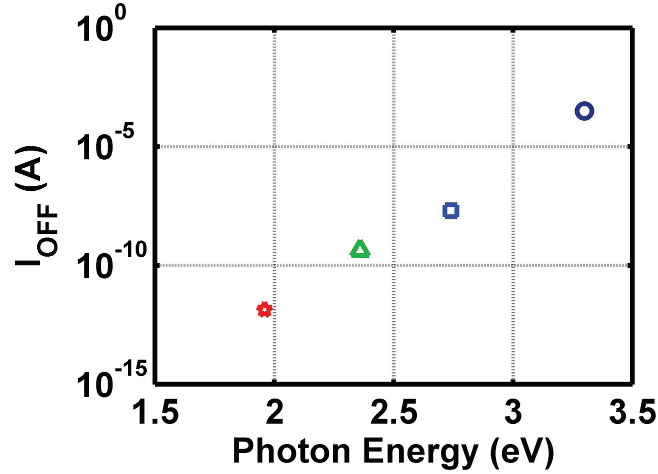

Figure 7.14: I_{OFF} vs photon energy.

While it is true that photo-current due to various sub-bandgap energies would be expected to have an exponential trend, this does not completely explain I_{OFF} characteristics. One explanation can be found by looking at trends in I_{OFF} not only over different photon energies, but also over time. In Figure 7.15 all of the curves from this study can be seen. I_{OFF}, in fact, does have two observable trends:

1. The logarithmic dependence with photon energy (as described in Figure 7.14)

2. A slight increase in I_{OFF} with illumination time (shift within each circled curve group)

This indicates two mechanisms govern I_{OFF} characteristics.

The Levison Model can, again, be used to explain these experimental characteristics. The equations can be rewritten in terms of free carrier density instead of V_G

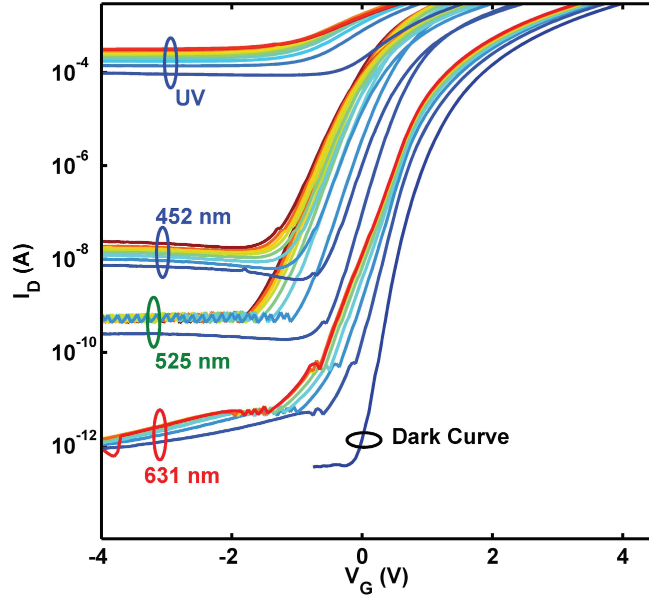

Figure 7.15: Entire reverse directional curve data set. I_{OFF} characteristics trend in two ways: (1) Increase with radiation energy (2) Increase with time.

as seen in Equations 7.4 and 7.5.

$$I_D = \mathrm{w}\mu_b \frac{V_D}{l} N_D e^{(-E_B/kT)} \tag{7.4}$$

$$\frac{-E_B}{kT} = \frac{-q^2 N_{GB}^2 t}{8\epsilon kT N_D} \tag{7.5}$$

Typically free carrier density is determined by doping and influenced by the gate voltage across the dielectric $N_D = \frac{C_{OX}V_{OX}}{q}$, but in the case of illumination N_D is a product of both photo-generated and gate influenced carriers $N_D = (N_{PH} + \frac{C_{OX}V_{OX}}{q})$. As a result Equations 7.4 and 7.5 become

$$I_D = \mathrm{w}\mu_b \frac{V_D}{l} (N_{PH} + \frac{C_{OX}V_{OX}}{q}) e^{(-E_B/kT)} \tag{7.6}$$

$$\frac{-E_B}{kT} = \frac{-q^2 N_{GB}^2 t}{8\epsilon kT (N_{PH} + \frac{C_{OX}V_{OX}}{q})} \tag{7.7}$$

Graphically, this concept can be seen in a plot of N_D vs V_G exhibited in Figure

7.16.

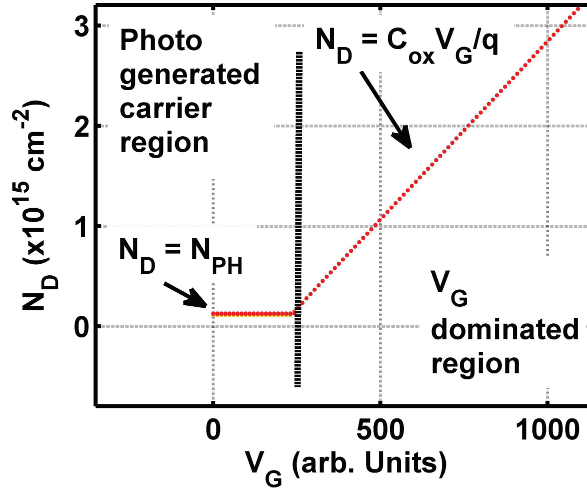

Figure 7.16: N_D vs V_G. Under illumination N_D will have photo-generated and gate voltage induced carrier concentration components.

By choosing a value for N_{PH} and inserting it into the Modified Levinson Model it becomes clear that the mechanism governing the temporal change in I_{OFF} is the grain boundary charge. Figure 7.17 shows a family of modeled curves, each with the same value of N_{PH}, but different values of N_{GB} (extracted from experimental data). It can be seen that the temporal trend of slightly increasing I_{OFF} over time can be explained by decreasing N_{GB}.

By choosing the correct value of N_{PH} that each illumination source imparts on the device, we can recreate both I_{OFF} trends witnessed experimentally as seen in Figure 7.18(a). With this, we conclude that I_{OFF} characteristics are governed by two mechanisms: photo-generated carrier enhancement and grain boundary charge reduction. The trends due to each mechanism can be explained via the modified Levison model.

A plot of selected N_{PH} vs Time can be seen in Figure 7.19(a). Except for the red wavelength case, the trend in N_{PH} with radiation energy is much more realistic relationship for photo gererated carriers than assuming the entirety of I_{OFF} was due

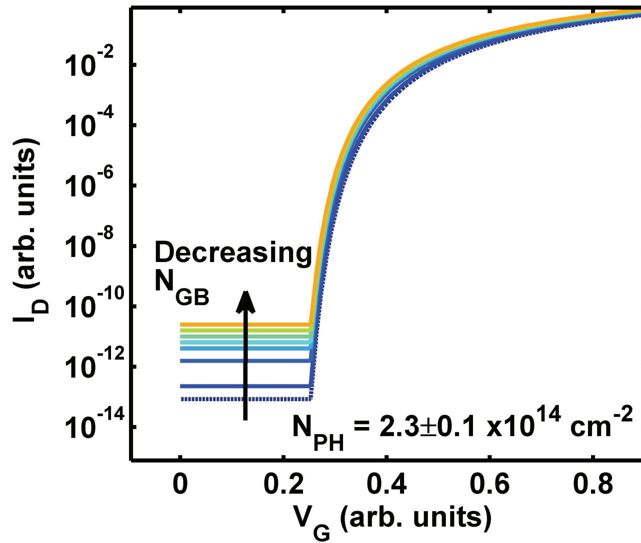

Figure 7.17: Modeled I_D-V_G. Single N_{PH} value. Variable N_{GB} (extracted from experimental data) Results show temporal I_{OFF} trend due to decreasing N_{GB}.

to radiation energy effects alone (Figure 7.14). In addition, the results can still be reasonably fit to an exponential relationship (Figure 7.19(b)).

7.4.5 μ_{SAT} Analysis

Extracted $\Delta\mu_{SAT}$ can be seen in Figure 7.20. To align temporal shape of each illumination curve, time = 0 is the first curve captured under illumination. The reference mobility, against which $\Delta\mu_{SAT}$ is calculated, remains the pre-illumination (dark) value.

As mentioned above mobility results can be described by two regions of operation. First, in the first 1x10^3 seconds $\Delta\mu_{SAT}$ rises in a linear fashion and peaks at some time, termed t_{pk}. Secondly, after t_{pk} each curve displays an exponential or 1/time like decrease to an intermediate value between the peak value and the original μ_{SAT}. This two-stage temporal characteristic indicates there are two mechanisms governing total mobility. This concept is described pictorially in Figure 7.21.

Mechanism 1 can be explained by N_{GB} reduction altering the conduction by

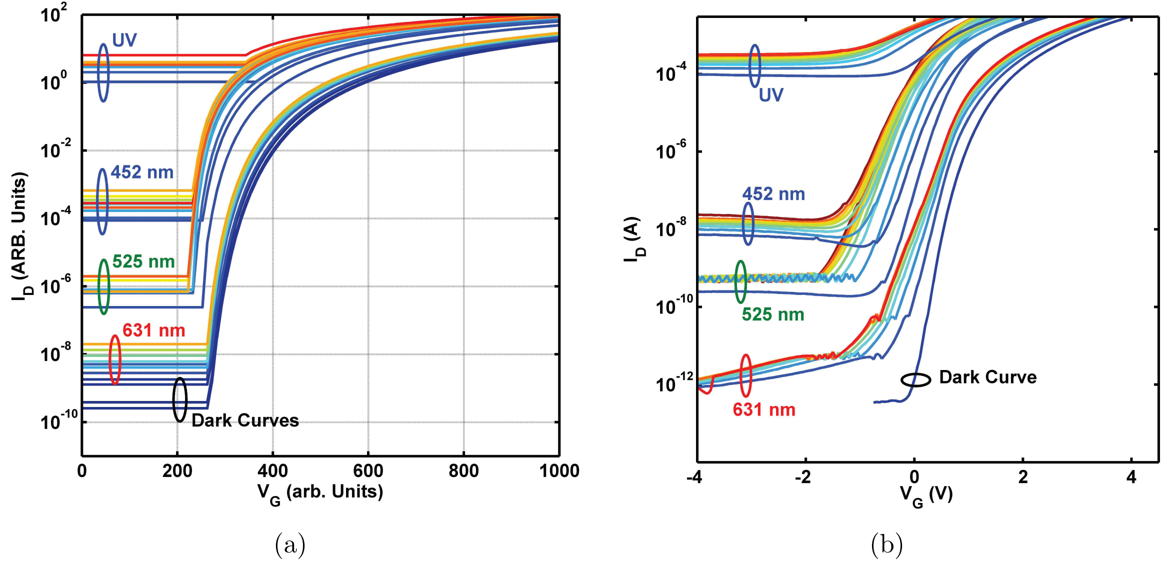

Figure 7.18: I_{OFF} characteristics can be explained by effects due to photo-generated carriers and grain boundary charge reduction. (a) Modeled I_D-V_G. Single N_{PH} value. Variable N_{GB} (extracted from experimental data) Results show temporal I_{OFF} trend due to decreasing N_{GB}. (b) Experimental data for comparison.

thermionic emission over grain barriers. This makes sense as a reduction in grain boundary charge will reduce the charge sites at which free carriers would scatter. Less N_{GB} means less scattering, which results in increased mobility. Figure 7.22 shows $\Delta\mu_{SAT}$ extracted by the method described in Chapter IV from modeled curves with experimental N_{GB}. In the cases of all illumination wavelengths, the simulated t $< t_{pk}$ $\Delta\mu_{SAT}$ temporal trends match experimental data. It is of note that the 631 nm case also fits data though its temporal trend is different. This further supports the idea that N_{GB} limited mobility is the governing mechanism for initial increase in mobility (Mechanism 1 in Figure 7.21).

Mechanism 2 must be some physical phenomena that, due to illumination over time, carrier mobility is reduced in the cases of photon energies above 1.96 eV as red illumination can be completely described by Mechanism 1. Two possible candidate mechanisms are interface state and carrier-carrier scattering.

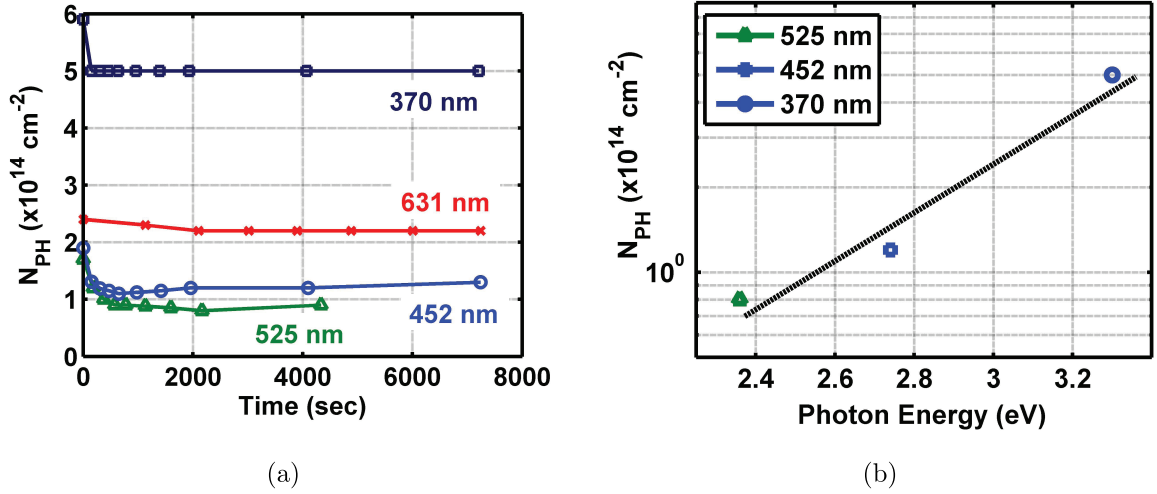

Figure 7.19: I_{OFF} characteristics can be explained by effects due to photo-generated carriers and grain boundary charge reduction. (a) Photo-generated carrier concentration used to fit experimental data. (b) N_{PH} vs photon energy. Data can be fit to exponential spanning less than one order of magnitude.

Interface State Scattering When a device is 'on', electrons are accumulated near the channel/dielectric interface. Increase interface charge (N_{it}) will increase the scattering sites for channel carriers and this can limit mobility. Since an increase in subthreshold slope indicates an increase in N_{it}, ΔS can tell us about the temporal characteristics of N_{it}. Figure 7.23 shows the temporal characteristics of ΔS and ΔN_{it}. The temporal shape of both do not match that required for Mechanism 2 thus interface states are not suspected as a limiting factor for mobilities above t_{pk}.

Carrier-Carrier Scattering When enough carriers are in the channel, mobility can be limited by carrier-carrier scattering [78]. Since illumination has been shown to increase N_D, it must be considered as a possible mobility limiting mechanism. Again, the temporal shape of N_{PH} must provide an appropriate match to Mechanism 2. Figure 7.19(a) shows that photo-generated carriers stay relatively stable over time with a slight reduction over t $<$ t_{pk}, which, if anything, would cause mobility to further increase. As a result carrier-carrier scattering is not suspected as a candidate

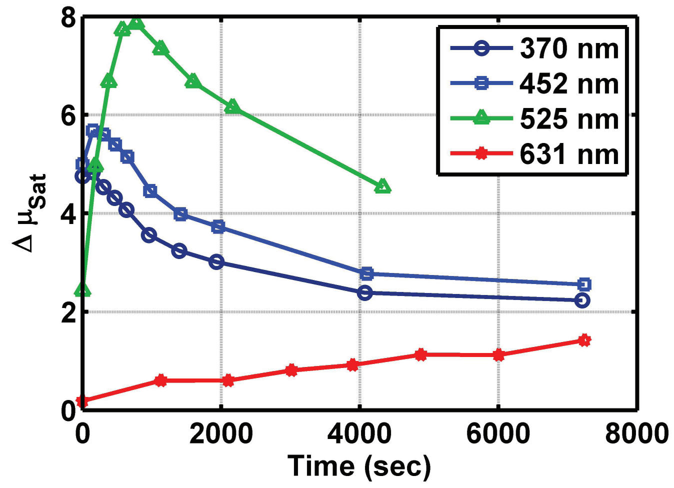

Figure 7.20: $\Delta\mu_{SAT}$ vs Time for each illumination wavelength.

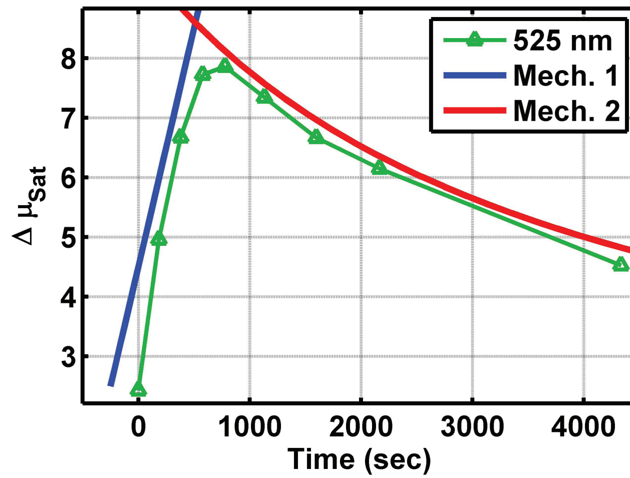

Figure 7.21: Experimental $\Delta\mu_{SAT}$ is likely governed by two different mobility limiting mechanisms.

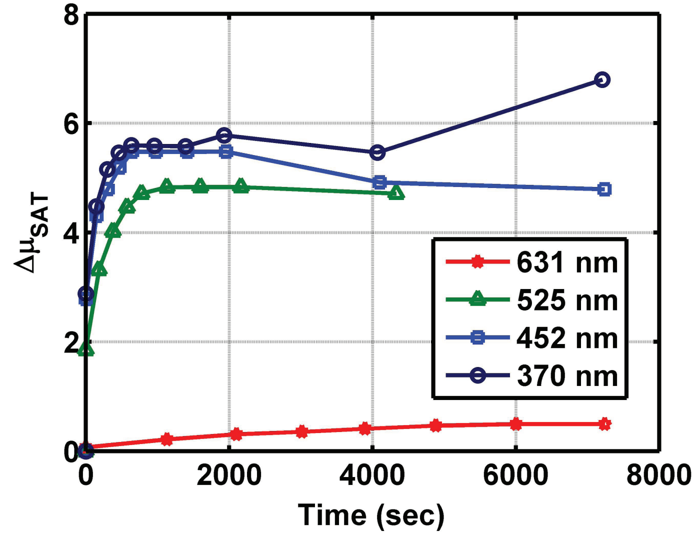

Figure 7.22: Simulated $\Delta\mu_{SAT}$ due to experimental reduction in N_{GB}. μ_{SAT} extracted via method described in Chapter IV.

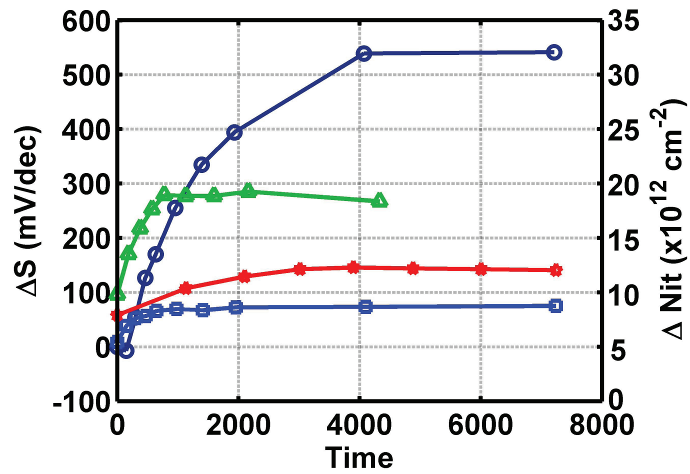

Figure 7.23: Experimental ΔS and extracted ΔN_{it}. Temporal shape indicates interface states do not play a role in mobility reduction at t ¿ t_{pk}.

for Mechanism 2.

To summarize mobility analysis, mobility characteristics indicate two mechanisms are responsible for TFT mobility under illumination. The first mechanism governing mobility at times t $< t_{pk}$ is reduction in grain boundary charge. Further investigation is required to identify the second mechanism governing mobility at times t $> t_{pk}$.

7.4.6 Bias-Temperature-Illumination Stress Discussion

In this section the instabilities of polycrystalline ZnO TFTs with high-K HfO_2 gate dielectrics have been investigated via temporal characteristics of TFT curves under illumination. Illumination of TFT devices biased at $V_G = 0$ show an increase in I_{OFF}, subthreshold slope, and -ΔV_{TH}. Mobility was observed to initially increase and then after some time, t_{pk}, decrease with time.

An extremely strong correlation between -ΔV_{TH} and -ΔN_{GB} indicates illumination enhanced carrier emission from grain boundary traps reduce total N_{GB} and thus the grain boundary potential barriers. Simulations show that reduction in N_{GB} has a direct effect on ΔV_{TH} with trends matching those of experimental data. We conclude that, while we do not have a definitive answer for complete governance, experimental data suggests that illumination causes reduction in grain boundary trapped charge density reducing the grain boundary barrier height, which has a strong influence on ΔV_{TH}. Modeled barrier height reduction with illumination (N_{GB} reduction) can be seen in Figure 7.24.

I_{OFF} characteristics indicate sub-bandgap trap states exist throughout the ZnO bandgap and can be explained by increased photo-generated carriers and reduced N_{GB}, both caused by illumination, modifying conduction due to thermionic emission over grain barriers.

Mobility characteristics can be partially explained by reduction of N_{GB}, but a second mechanism limiting mobility over times t $> t_{pk}$ has not yet been identified.

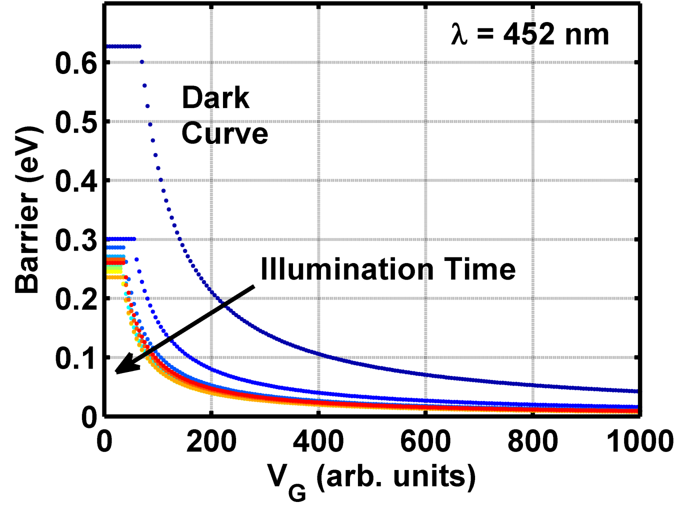

Figure 7.24: Grain boundary barrier height versus gate voltage. Each curve represents a time step in the illumination exposure experiment. Increase illumination time (reduced N_{GB}) and increased V_G lower grain boundary barrier heights in the polycrystalline ZnO.

7.5 Photo-Conductivity Investigation

Photoconductivity has been a topic of research for polycrystalline ZnO as the semiconductor has been investigated for optoelectronic applications in addition to transistors. Reports show sub-bandgap states are responsible for increased photocurrent in ZnO films [51, 54]. In this study, photoconductivity of ZnO/HfO_2 results with various wavelengths of illumination are presented.

ZnO/HfO_2 TFTs were left in the dark for 1 hour, then biased at I_{DS} = 5 V, and V_{GS} = 0 V, illuminated for 1 hour, next the illumination was removed, but bias remained for at least another hour to record recovery characteristics. Figure 7.25(a) shows photoconductivity results as raw data and Figure 7.25(b) shows normalized data for different energies.

7.5.1 Photocurrent Analysis

Photocurrent magnitude increases with illumination energy indicating sub-bandgap states throughout the ZnO bandgap. In addition, the temporal shape of the photo-

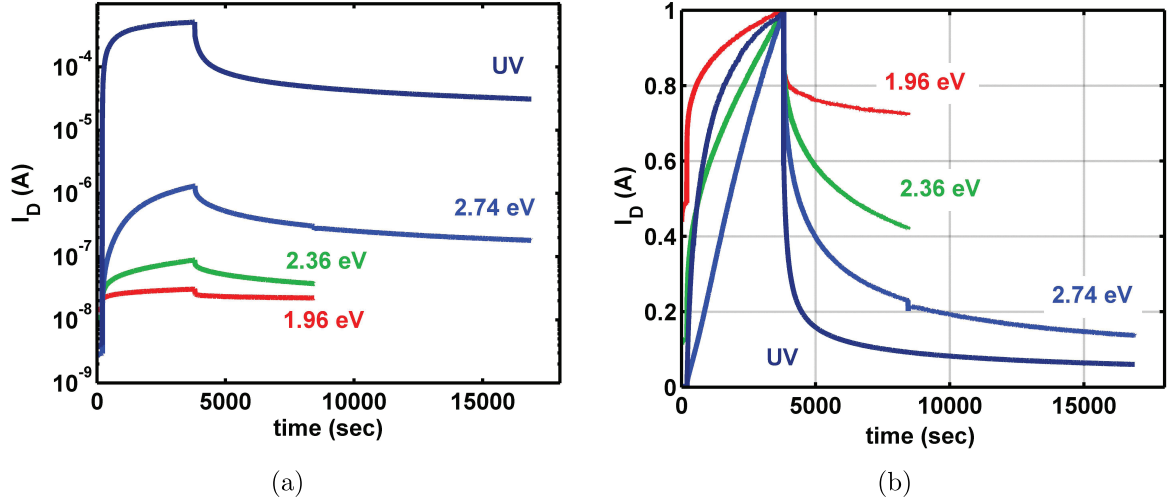

Figure 7.25: Photoconductivity curves for polycrystalline ZnO with HfO_2 gate dielectric. (a) Raw photoconductivity current versus time. (b) Normalized photoconductivity current versus time.

conductivity is indicative of the population and time constants of trap emission in the material system. An initial steep increase is indicative of traps with fast time constants emitting carriers into the conduction band, while a slow increase over time is indicative of deep traps with longer time constants contributing to the photocurrent (I_{PH}). Finally, a steady current would be indicative that all of the traps that will interact with the illumination energy have emitted carriers. Figure 7.25(b) shows the differences in temporal shape of photocurrent increase. In each case, the photocurrent has not reached saturation. Photon-energy of 1.96 eV shows the most saturation and the UV case ($E > 3.3$ eV) shows the least. Likewise, the photocurrent decay upon removal of illumination can give information about trap capture time constant.

There have also been reports on the photoconductivity effects of passivation indicating exposed ZnO surface states can contribute to photoconductivity if not passivated [51]. The experimental curves do show characteristics similar to those reported for un-passivated devices, which indicates the role of surface states should not be neglected. These characteristics include longer times to reach photocurrent saturation and very long times for post-illumination current to return to pre-illuminated state,

if it is reached at all. One element separating this study from those reported is that there is a gate dielectric and though V_G is 0 V, the TFT illumination study revealed that a threshold voltage shift will take place with $V_G = 0$. A negative threshold voltage shift would result in increased in photocurrent as I_{PH} can be thought of as a slice of the TFT I_D-V_G curves under illumination taken at $V_G = 0$ V.

To validate the relationship of photocurrent with TFT illumination curves, TFT I_D data at $V_G = 0$ V over the course of TFT illumination can be compared with I_{PH}. Figure 7.26 shows this comparison for the case of UV and 452 nm illumination. In all cases I_{PH} is much lower than the data extracted from TFT curves predicts, in some cases orders of magnitude lower.

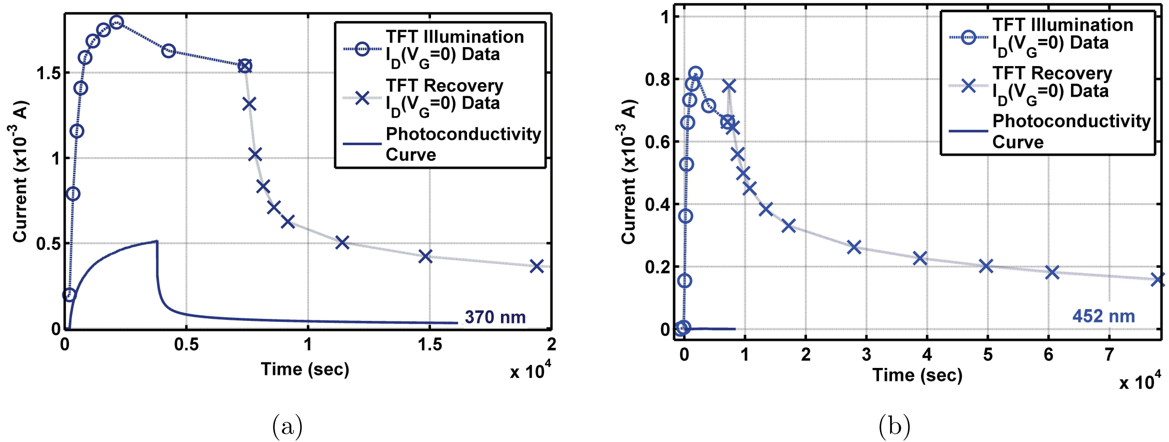

Figure 7.26: Photoconductivity I_{PH} versus time compared to TFT $I_D(V_G = 0)$ data versus time (a) UV illumination. (b) 452 nm illumination. I_{PH} is orders of magnitude lower than $I_D(V_G)$.

From the discrepancy between I_{PH} and $I_D(V_G = 0$ V) values it is clear the different bias conditions of each test have some affect on at least one mechanism that governs illumination instabilities.

Illuminated TFT I_D-V_G Bias Scheme: The bias scheme over the time of illumination is $V_D = V_S = V_G = 0$ V, but while the TFT transfer curve is being measured $V_D = 5$ V and V_G is swept from -4 to + 4.5 V. The gate to source voltage is thus -4

to 4.5 V over the course of the sweep, while the gate to drain voltage is -9 to -0.5 V. Due to equipment auto ranging in the I_{OFF} regime, curves can take anywhere from 2 to 15 minutes to finish the dual sweep measurement, most of this time is spent between -4 to -1 V_G. This means that for the first many curves, more time is spent sweeping than not, and often in the negative V_G range.

Photoconductivity Bias Scheme: The bias scheme over the time of illumination was stable at $V_D = 5$ V and $V_S = V_G = 0$. This means the gate to source voltage was 0, but the gate to drain voltage was -5 V for the entire course of the measurement.

Many reports have claimed, that for devices under illumination and subjected to negative gate stress (NBTI), photo-generated hole trapping at or near the interface is responsible for -ΔV_{TH} [74], which would also be responsible for an increase in $I_D(V_G{=}X)$. It may be possible that the bias scheme of illuminated TFT I_D-V_G introduces NBTI-like effects driving photo-generated holes into interface traps. This added effect might be responsible for the increased current values compared to photoconductivity. Further investigation into the bias effects of Photoconductivity and Illuminated TFT I_D-V_G is necessary to draw conclusions in this respect.

7.5.2 Photoconductivity Discussion

Photoconductivity measurements on ZnO semiconductor gated with HfO_2 show characteristics typical to those reported in literature for ZnO with sub-bandgap trap states. This is in agreement with conclusions made above that grain boundary traps in the ZnO are responsible for TFT instabilities. In addition, TFT illumination results agree with basic shape of photocurrent and photocurrent post-illumination decay. Discrepancies in actual photocurrent values with extracted TFT current values might be explained by the difference in bias schemes and how the electric fields in the devices cause majority and minority carrier interactions with trap states at the

channel/dielectric interface or in the dielectric.

7.6 Discussion

In this chapter the illumination instabilities of ZnO/HfO_2 have been presented. TFT I_D-V_G curves show an increase in I_{OFF}, subthreshold slope, and -ΔV_{TH}. Mobility was observed to initially increase and then after some time, t_{pk}, decrease with time. Most characteristics can be explained via a model for conduction via thermionic emission over grain barriers where illumination causes a reduction in grain boundary charge and an off-state increase in carriers due to photo-generation. Further investigation is necessary to identify the mechanism that governs mobility over long timescales.

Photoconductivity measurements were carried out and are representative of a ZnO film with trap states within the bandgap. Further investigation is required to understand the effects of the bias scheme on the correlation between photocurrent and TFT drain current, which may reveal interface or dielectric dependent illumination instabilities. This recalls the topic of TFT illuminated $V_{G-Start}$ value reported early in this chapter. The threshold voltage is observed to shift to negative voltages with increasing negative $V_{G-Start}$ sweep range (Figure 7.3), which gives weight to the idea that time spent negatively biasing a TFT could contribute to the discrepancy between I_D and I_{PH}.

Finally, passivation has been widely reported to influence illumination performance and elucidate the role of surface states and photo-desorption in ZnO-based devices. An important topic of future work is the stability of passivated devices as they compare to un-passivated devices.

CHAPTER VIII

Conclusions and Future Work

8.1 High-k dielectric selection for ZnO devices

In Chapter II the selection and deposition properties of various dielectrics were discussed as candidates for next-generation high performance ZnO/high-k devices. Perovskite Oxides Lead Zirconate Titanate ($Pb[Zr_XTi_{1-X}]O_3$ or PZT) and Barium Strontium Titanate ($Ba_{0.5}Sr_{0.5}TiO_3$ or BST)were selected due to their extremely high dielectric constants, compatibility with Pulsed Laser Deposition (PLD), and possibility for unique device characteristics due to ferroelectric and paraelectric multi-functionality.

Aluminum Oxide (Al_2O_3) and Hafnium Oxide (HfO_2) were investigated due to many advantages that have caused both materials to be used by the Silicon industry as near-term solutions to high-k integration. A key advantage is that both materials can be deposited by Atomic Layer Deposition (ALD) which allows for extremely high quality conformal amorphous films.

In Chapter III each high-k dielectric was integrated with ZnO to make a Metal - Insulator - Semiconductor Capacitor (MIS-C). The properties of the MIS-Cs were then measured with a focus on extracted dielectric constant (k_{ox}), voltage characteristics, and leakage current. Both Perovskite Oxides displayed extremely high k_{ox} values above 400 and ferroelectric and paraelectric effects. Unfortunately, very high leakage

values were observed, which were attributed to low conduction band offsets with ZnO.

Both ALD dielectrics displayed much better leakage values due to higher conduction band offsets and lower hysteresis indicating less interface charge. With superior leakage properties and $k_{ox} \approx 20$, HfO_2 emerged as the most promising candidate for insertion into next-generation ZnO high-k devices. Two characteristics were observed that could be roadblocks to ZnO/HfO_2 advancement: C-V hysteresis, which is indicative of undesirable dielectric/ZnO interface charge, and V_G translational instability, which could eliminate the use of such devices from many applications requiring relatively stable threshold voltages. Interface charge and device instabilities are a major focus of Chapters V, VI, and VII.

In Chapter IV the insertion of high-k materials into ZnO thin film transistors (TFTs) was performed and the results were presented. The goal of reducing the operating voltage and threshold voltage (V_{TH}) of ZnO TFTs was realized. Compared to Si_3N_4 gate dielectric TFTs with an Equivalent Oxide Thickness (EOT) of 68 and $V_{TH} = 22$, the high-k devices all achieved EOTs of less than 6.1 and $V_{TH} < 2.4$. TFTs with HfO_2 displayed superior I_{OFF} performance and, with the results from Chapter III were selected as the high-k of choice for next generation ZnO devices.

8.2 Interface charge of ZnO/HfO_2 thin films

Subthreshold slope (S) is an important TFT performance parameter for many applications, especially low power and high-current applications. A device with high S values will have higher threshold voltages and lower currents at a given V_G. S has been linked to interface charge. In addition, clockwise hysteresis has been observed in ZnO/HfO_2 devices, which is indicative of interface charge. Due to the importance of interface charge in advancing ZnO TFT technology, Chapter V is devoted to D_{it} study.

Complementary methods to characterize interface charge in ZnO/HfO_2 devices

have been explored. Admittance Spectroscopy was found to be the most comprehensive technique and had the best agreement with N_{it} values obtained from TFT subthreshold slope. D_{it} values were found to range from low 10^{13} to high 10^{11} cm^{-2}eV^{-1}, which is considered high for Silicon CMOS devices, but the ZnO interfaces presented in this work exhibit no fermi level pinning and are used in devices that show state-of-the-art performance.

8.3 Bias - Temperature - Stress instability of ZnO/HfO_2 TFTs

Threshold voltage stability is another important issue in developing next-generation TFT devices. V_{TH} stability requirements are application specific and poor stability can eliminate a technology from consideration for a given application or require significant excess engineering design and process cost to provide compensation. Chapter VI investigates V_{TH} stability with respect to bias and temperature stressors.

Positive gate bias-temperature-stress instability (PBTI) results show linear increase in V_{TH} with logarithmic time, which increases with gate stress voltage. Analysis of these trends reveal the dominant instability mechanism is charge trapping by carrier injection into the HfO_2. A new method was presented to fully characterize V_{TH} instabilities and extract dielectric charge trap density.

Negative gate bias-temperature-stress instability (NBTI) results show an exponential-like increase with logarithmic time, which increases with temperature. Analysis of these trends indicate that the dominant mechanism is likely charge state creation, which could result from states created at the channel/dielectric interface or in the ZnO semiconductor. V_T data can be characterized by a fit to a model developed to describe charge state creation in a polycrystalline semiconductor.

8.4 Illumination instability of ZnO/HfO_2 TFTs

A significant advantage of thin film ZnO is its transparency in the visible spectrum and high electron mobility compared to other thin film semiconductors. Thus, ZnO TFTs are well suited for transparent and display applications where both high mobility and stability under visible light are key requirements. As a result, Chapter VII investigates the illumination stability of ZnO/HfO_2 TFTs under red, green, and blue light, used in display technologies, and UV, which contains photon energies above the ZnO bandgap.

TFT I_D-V_G curves show an increase in I_{OFF}, subthreshold slope, and -ΔV_{TH}. Mobility was observed to initially increase and then after some time, t_{pk}, decrease with time. Most characteristics can be explained via a model for conduction via thermionic emission over grain barriers where illumination causes a reduction in grain boundary charge and an increase in carriers due to photo-generation.

Photoconductivity measurements were carried out and are representative of a ZnO film with trap states within the bandgap. Discrepancies in photocurrent values with extracted TFT I_D values might be explained by the difference in bias schemes and how the electric fields cause majority and minority carrier interactions with trap states in the ZnO, ZnO/dielectric interface, or in the dielectric.

8.5 Future Work

8.5.1 Interface charge

With several methods to characterize D_{it}, future work should be focused on D_{it} stability with stressors such as temperature, bias, and light which reveal a great deal about the role D_{it} plays in device operation. In addition, methods might be developed to use stressors or process techniques to reduce D_{it}. Finally, test methods can be improved and expanded to capture D_{it} over a wider range of energies. Important

issues for future work are listed below.

- Understanding the trade-offs between processes and interface charge will be important in advancing ZnO device applications. Characterizing interface state density is a good first step. The logical next step is to characterize D_{it} with respect to measurement or post-anneal temperatures. In Section 3.8, hysteresis was reduced by 50% after a 400 K device measurement. From this result, and recent reports on HfO_2, it is expected that elevated temperatures will change the D_{it} profile, likely reducing N_{it}.

- Investigate the role of Nitrogen-based forming gas anneals on ZnO/HfO_2 interfaces. It is expected that Nitrogen will passivate interface traps formed by oxygen vacancies [23],but as oxygen vacancies are also a source of n-type ZnO doping, the effects on the device performance on the whole must be characterized.

- Expanding the energies at which D_{it} can be measured would be extremely valuable. Increased experimental temperature range would expand the energy range of Thermally Stimulated Conductance and lower AC frequencies would allow a wider Admittance Spectroscopy energy range. It has also been suggested that illumination could help probe deeper energy traps than are currently accessible with the methods presented in this work.

- An important topic of future work is to understand the physical mechanisms behind D_{it}. A first step would be to perform chemical analysis on devices whose interface state density have been measured. This type of analysis has been done with Si/HfO_2 devices revealing Oxygen from HfO_2 diffusing into the interface. Cross sectional analysis like Transmission Electron Microscopy with Z-contrast analysis or surface techniques like X-Ray Photoelectron Spectroscopy (XPS) combined with a depth profling like Focused Ion Beam Sputter Depth Profling

are just two of many potential methods that can be used to look at the interface from a chemical perspective, which will provide better understanding of D_{it} in ZnO/HfO_2 structures.

8.5.2 Bias - Temperature - Stress instability

Important topics for future work on electrical and temperature stability of ZnO/HfO_2 devices are listed below:

- Identifying process techniques that can be used to limit or eliminate PBTI and NBTI. The most important future work topic is to measure and understand the effects of passivation on ZnO/HfO_2 devices. Pre- and post-process anneals and insertion of low trap density inter-layers have also been shown to be influential in stability characteristics of other material systems and should be investigated.

- Determination of the physics behind NBTI. Instability characteristics with initial exponential growth and subsequent limited ΔV_{TH} have been reported for various semiconductors and fit to a stretched exponential function. However, claims as to the mechanisms responsible are varied.

- Development of NBTI test and analysis technique that allows for mobility measurement while reducing confounding due to PBTI.

- Conducting BTS over longer times, wider bias ranges, and wider temperature ranges to increase fidelity of observed trends and to discover if trends hold over wider measurement windows.

8.5.3 Illumination instability

Important topics for future work on illumination stability of ZnO/HfO_2 devices are listed below:

- Identification of the mechanism that governs illumination induced limited mobility over times greater than t_{pk}.

- Identify the role of the bias scheme and dielectric in illumination instability. Reports have shown that devices under bias and illumination show instability characteristics that are different from what would be expected from individual studies on bias alone and illumination alone [74].

- The most important future work, as with the BTS case, is the passivation effects on ZnO/HfO_2 devices. This will help to identify effects due to surface states and interaction with the environment. Passivation has also been shown, in some cases, to significantly reduce illumination NBTI [74].

- Finally, complementary methods to determine the role of grain boundary charge will be necessary to conclusively prove the link between N_{GB} and ΔV_{TH}.

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