

# **Fully Integrated CMOS Phased-array PLL Transmitters**

by

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# ABSTRACT

With more advanced technology, complete phased array system can be integrated in CMOS. Integrated CMOS phased array systems offer lower cost, lower power consumption, higher reliability and the possibility of on-chip signal processing using ever cheaper digital circuitry. This opens up possibilities for new applications such as directional point-to-point wireless communication which provides high security and is less prone to jamming by interferers.

Integrated phased array systems are for the most part not too different from normal single channel transceivers. The key additional component is the phase shifter. A new phased array architecture that uses digital phase locked loop PLL modulator to realize phase shift is developed. To achieve phase shifting capability, PLL is a natural candidate. If we combine PLL's phase shifting and modulation capabilities then we can realize phased array system using solely PLLs. With recent breakthrough in digital PLL, a digital PLL can generate a precise and well-controlled phase shift that analog PLLs cannot. The same phase shift capabilities can be used for data modulation. With both phase shift and data modulation capabilities, we only need an array of such PLLs to realize a phased array. Compared with conventional phased arrays, PLL based phased array can achieve more precise phase shift thus

more precise radiation angle. It is also more flexible, since all channels can generate independent phase shift.

A fully-integrated 5.8GHz PLL modulator prototype implemented in 65nm CMOS that achieves digitally-controlled arbitrary phase generation is presented. The PLL is a Type II fractional-N PLL with a 1-bit TDC as its PFD. Digital phase setting, which operates by adding a proportional signal to the PFD output, is incorporated in the PLL. The prototype achieves an average measured phase resolution of  $2.25^\circ$  and phase range of more than  $720^\circ$ . The entire PLL and output buffer consumes 11mW. Four of such PLLs form a prototype phased array as a proof of concept.

# **Chapter 1**

## **Introduction**

### **1.1. Background**

Moore prophesied in his 1965 paper [1]: “The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar.” Indeed, that day has come. With more advanced technology, complete phased array system can be integrated in CMOS. Integrated CMOS phased array systems offer lower cost, lower power consumption, higher reliability and possibility of on-chip signal processing using ever cheaper digital circuitry. It opens up possibilities for new applications such as automotive radar systems. However, the application of integrated phased array system is not limited to radar as Moore envisioned. Phased arrays can also be utilized for directional point-to-point wireless communication, which provides high security and is less prone to jamming by interferers. At high frequency, phased array systems potentially offer more bandwidth, and reduce the required antenna size and spacing.

Integrated phased array systems are for the most part not too different from normal single channel transceivers. The key additional component is the phase shifter. A new phased array architecture that uses digital phase locked loop (PLL) modulator to realize phase shift is developed. To achieve phase shifting capability, PLL is a natural candidate. Furthermore, PLL transmitter has been extensively studied [2][3][4]. If we combine a PLL's phase shifting and modulation capabilities then we can realize phased array system using solely PLLs. A digital PLL can generate a precise and well-controlled phase shift that analog PLL cannot. With recent developments in digital PLL architectures [5][6], digitally dominant PLL based phased array systems are logically the next step.

This thesis focuses on PLL based phased array modulator. A digital PLL can generate precise and well-controlled phase shift. The same phase shift capabilities can be used for data modulation. With both phase shift and data modulation capabilities, we only need an array of such PLLs to realize a phased array. Compared with conventional phased arrays, PLL based phased array can achieve a more precise phase shift thus more precise radiation angle. PLL phased array is also more flexible, since all channels can generate independent phase shifts and produce independent modulation. This allows the phase array to produce a single beam or multiple beams each carrying different signals. Moreover it takes out the complicated signal routing tree required in a conventional phased array for phase delay matching.

Furthermore accurate phase control of high-speed signals is also required in serial links, clock distribution and medical imaging systems. A precise high frequency phase-setting PLL can be utilized in these applications as well.

For example, system-on-chip (SoC) design depends greatly on reusing semiconductor intellectual property (IP) [7]. However integrating existing IP cores into a single synchronous SoC faces the problem of clock distribution, because of different clock delay requirements. A clock generator with precise phase-setting ability can be used to solve the problem and alleviate the problems of clock distribution in large chips.

In an on-chip serial link, data is transmitted across the chip with a lossy on-chip transmission-line [8]. When data is received and sampled at the receiver end, it is delayed over the long transmission-line; therefore a phase shifter is needed to tune the sampling phase for proper recovery. With a precise phase-setting PLL, we can accurately adjust the sampling.

## 1.2. Introduction to Phased Array

Phased array transceivers are a type of multiple path system in which the signal in each path is time-delayed to achieve spatial selectivity [9]. The final radiation pattern is constructively interfered in the desired direction and destructively interfered in the unwanted direction to realize directionality. This is used to simulate a directional antenna. In a narrow-band system, time delay can be approximated by a phase shift. By shifting the phase of each signal path, an electronic beam can be “steered”. Besides the phase shifting element, phased array transceivers are no different from normal single element transceivers. Each signal path is connected to an independent antenna. The antenna array can be arranged in different spatial configurations. In a 1-D array shown Figure 1, the space between each antenna is  $\lambda/2$  where  $\lambda$  is the free-space wavelength of the RF frequency.

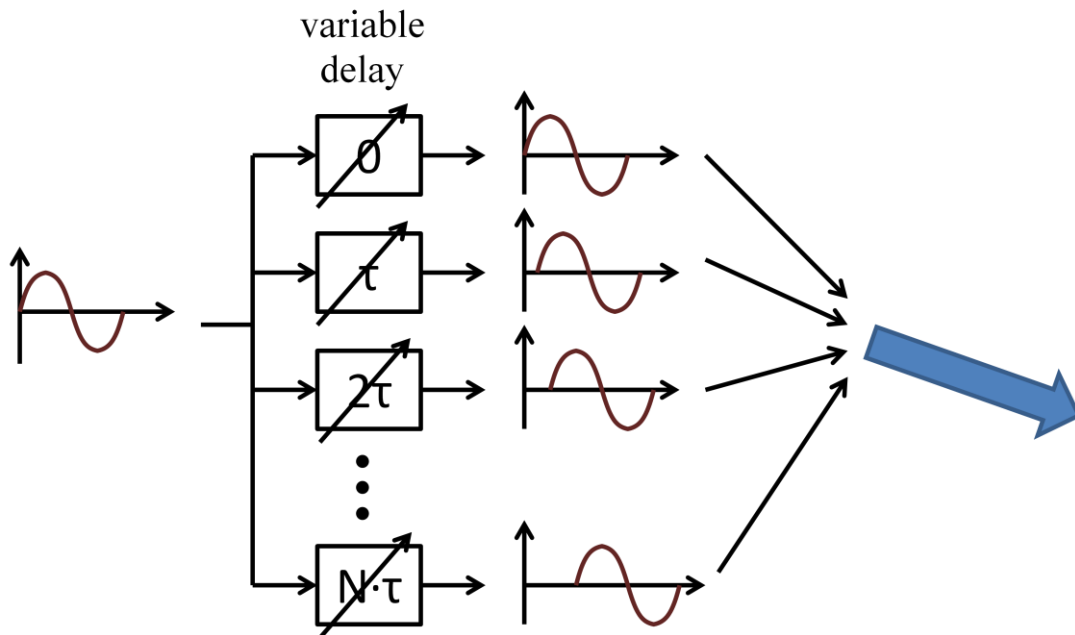


Figure 1: Phased array transmitter

Phased array receiver has the benefit of receiving less interferer as long as it does not originates from the same direction as the wanted signal. For a same given power received at the receiver, phased array transmitter requires less power than a single element transmitter. The power radiated by an N-element phased array transmitter is  $N^2$  times that of a single element in the desired direction, because of constructive interference in that direction. Furthermore, lowered power requirement in individual elements gives more design flexibilities and room for better optimization.

### 1.2.1. Phased array theory

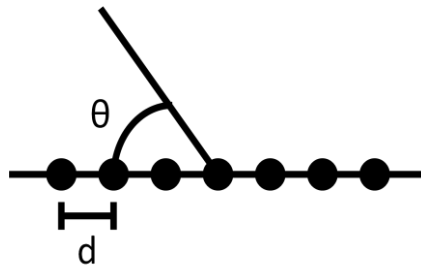


Figure 2: 1-D linear phased array

In a phased array, the phase array factor is defined as the additional power gain achieved compared to a single-element transceiver. In a 1-D linear phased array (Figure 2) with  $2N+1$  elements shown as dots, equally space by a distance  $d$ , the array factor,  $F_a$ , is described by [10]

$$Fa(\theta) = \sum_{n=-N}^{n=N} \frac{I_n}{I_0} e^{jnkd \cos \theta} \quad 1$$

where  $\theta$  is the angle from origin to a point in space,  $I_n$  is the power of individual element and  $I_0$  is the nominal power of a single-element transceiver.  $k=2\pi/\lambda$  and  $\lambda$  is the wavelength. We need to note that distance  $d$  should be less than half wavelength  $\lambda/2$ . When all elements produce the same power and same phase shift, the max power and array factor is achieved at  $90^\circ$ . However if all elements have equal amplitude but uniform progressive phase shift  $\omega\tau$

$$I_n = I_0 e^{-jn\omega\tau} \quad 2$$

the array factor becomes

$$Fa(\theta) = \sum_{n=-N}^{n=N} e^{jn(kd \cos \theta - \omega\tau)} \quad 3$$

Comparing equation 3 above to equation 1, we see that the peak power angle  $\theta_o$  can be changed from 0 in equation 1, to

$$kd \cos \theta_o - \omega\tau = 0 \quad 4$$

$$\theta_o = \cos^{-1} \left( \frac{\omega\tau \lambda}{2\pi d} \right) \quad 5$$

Thus describes the relationship between the phase shift  $\omega\tau$  in individual elements and final output radiation angle  $\theta_o$ . Since we can only control phase shift  $\omega\tau$  in the transmitter, the above equation is useful to determine the final radiation angle  $\theta_o$ . The same equation holds for a linear array of  $N$  elements. Assuming  $d = \lambda/2$ , and a 4-element array, the output power as a function of angle  $\theta$  and time delay  $\omega\tau$  in  $45^\circ$



steps is shown in Figure 3. We can also see from the figure that the peak power angle has changed by about  $14.5^\circ$  for every  $45^\circ$  of shift in input phase. The same 4-element array's radiation patterns in polar coordinates with a  $15^\circ$  steps are shown in Figure 4.

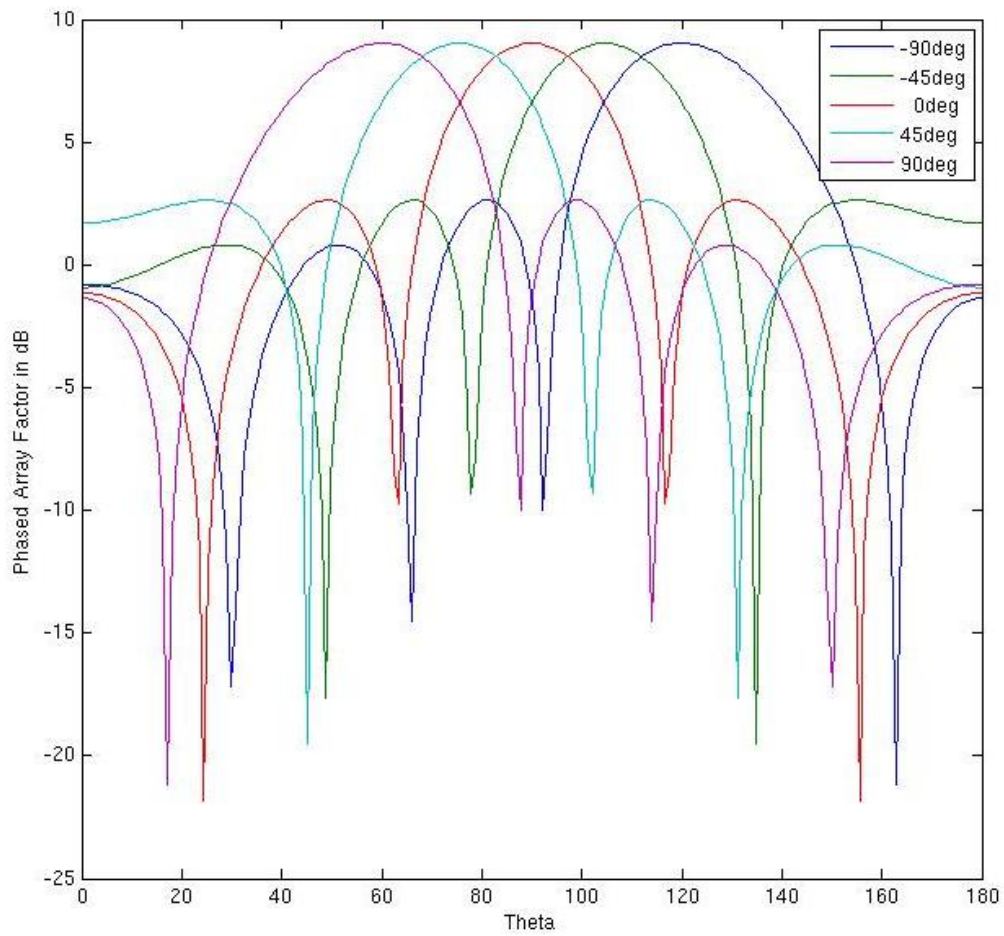


Figure 3: Array factor as a function of delay time  $\omega\tau$  in  $45^\circ$  steps

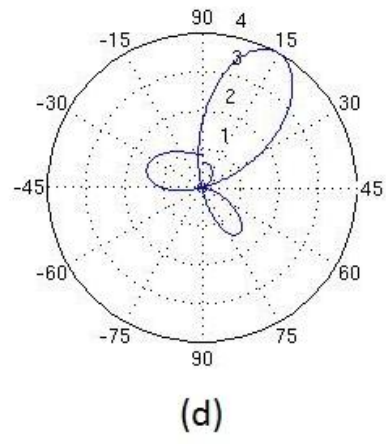
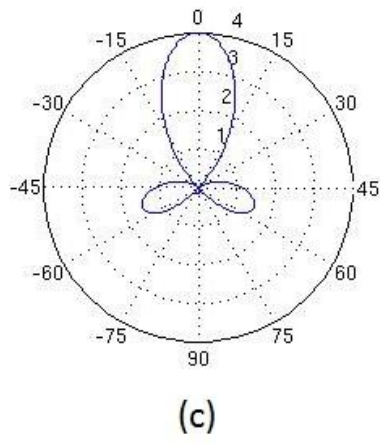
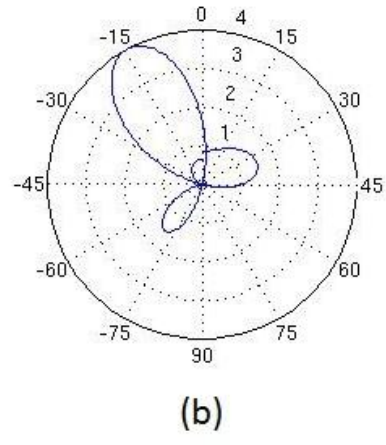
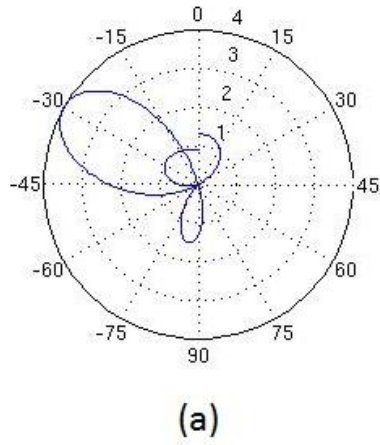


Figure 4: Array factor vs radiation angle in polar coordinates (a)  $-30^\circ$  (b)  $-15^\circ$  (c)  $0^\circ$  (d)  $15^\circ$

### 1.3. Existing Phased Array Architectures

As discussed earlier, phased array transceivers are no different from normal transceivers except for the phase shift; therefore where we introduce the phase shift gives rise to several different phase array architectures. We will only discuss the transmitter portion, but the receiver path is more or less the same except reversed.

#### 1.3.1. Phase shift at RF

The most conceptually direct way to phase shift the output is to add a phase shifter at the output of the RF signal before the PA and the antenna shown in Figure 5 [11][12] [13]. The advantage is that all channels can share all other blocks except for the phase shifter and the PA. This saves power and area. However the big disadvantage is that building a low loss and linear phase shifter at RF frequency is challenging. Being almost the last stage in the signal path, phase shifter's linearity is critical to the linearity of the whole system. Another significant disadvantage is that the phase shifter loss will lower the input signal power to the PA and thus making the PA design more difficult.

#### 1.3.2. Phase shift at DC/IF

Another common scheme that solves the difficulty at high frequency is phase shift before the up-conversion shown in Figure 6[14]. This can be done at either DC or IF frequency. Although in this scheme different channels can no longer share any blocks after the mixer, it reduces the phase shifter frequency and alleviates the challenges associated with RF frequency. One of the concerns is that the phase shifter is very early in the signal path, thus phase shifter noise performance is critical to the

whole system. Another concern is that due to the low frequency, phase shifter potentially requires much larger passive components since the values of the components (e.g. inductor and capacitors) are inversely proportional to frequency. However this entirely depends on the phase shifter architecture chosen.

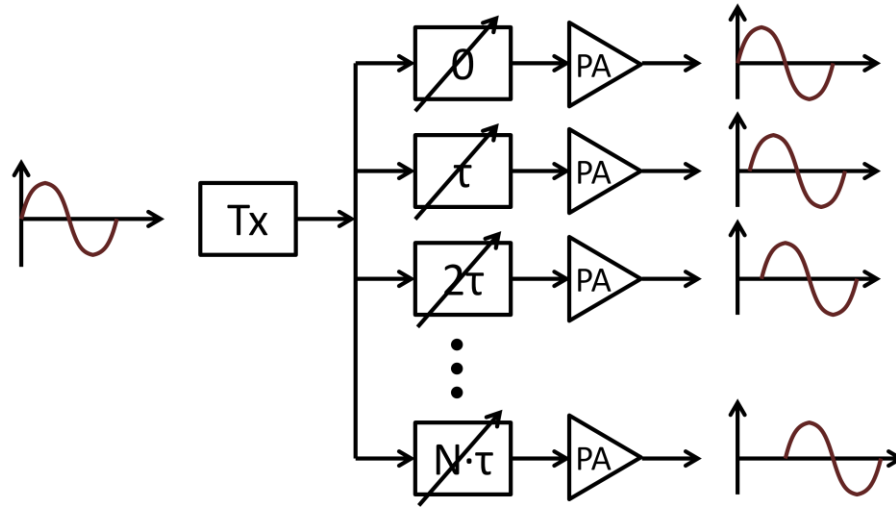


Figure 5: Transmitter with phase shift at RF

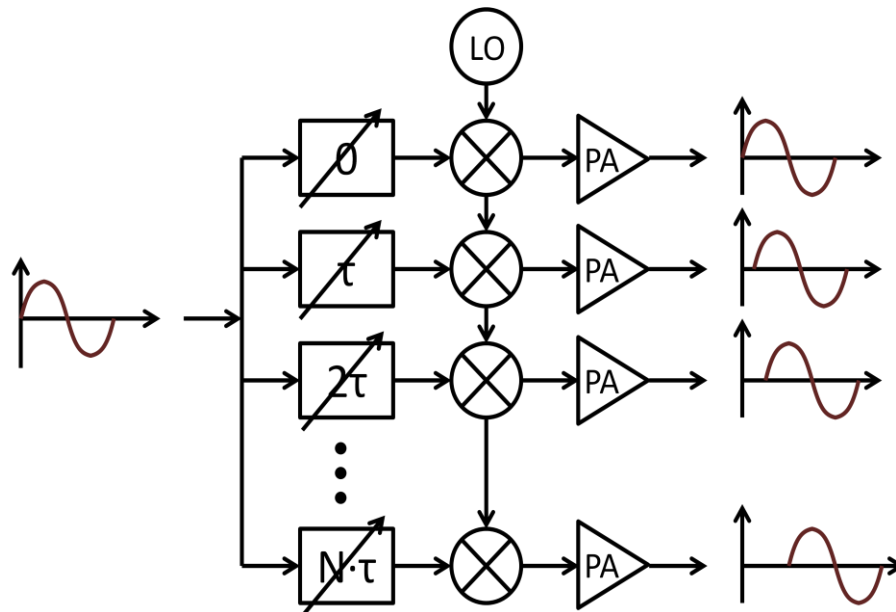


Figure 6: Transmitter with phase shift at DC

### 1.3.3. Phase shift at LO

A third architecture is to phase shift at LO as shown in Figure 7 [15][16] [17]. Since the output phase of a mixer is the sum of the IF and the LO phase, phase shift at LO has the same effect as phase shift at IF. Since the phase shifter is no longer along the signal path, its linearity is not important. The LO is much more tolerant of loss than anywhere else in the system, therefore a higher loss phase shifter can be used. The LO is also at the same approximate frequency as the RF signal, therefore passive components can be smaller than shifting at DC. However this scheme has the same disadvantages as shifting at DC those are components before the PA cannot be shared and also the need to distribute high frequency LO to each channel.

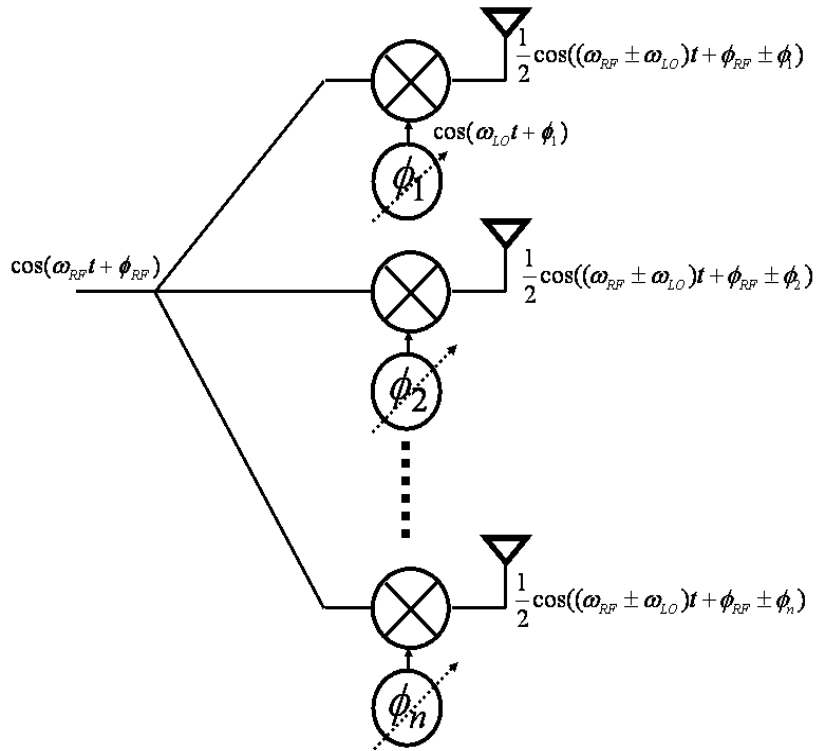


Figure 7: Transmitter with phase shift at LO

### 1.3.4. Summary of the architectures

The three phased array architectures are compared in Figure 8. They each have its own pros and cons. Depending on the requirements, one of the architectures could be more desirable than the others. Shift at RF is most suited when number of elements is high. This saves on power, area, and LO distribution. Shift at DC/IF is the best choice, when output frequency is very high and high frequency phase shifter is hard to achieve. Also at mm-wave frequency, power splitting is no longer trivial and thus power splitter's insertion loss is a concern for shift at RF. Shift at LO has the advantage not along the signal path and therefore insensitive to phase shifter performance. But it has the disadvantages of LO distribution difficulty and extra components before the PA. In the end, the key to architectural choice and performance of the phased array is the phase shifter which we'll discuss next.

	shift at RF [13]	shift at DC [14]	shift at LO [16] [17]
Phase shifter frequency	high	low	high
Phase shifter insertion loss	sensitive	average	insensitive
LO distribution	easy	hard	hard
# of mixer required	1	N	N
N=number of path			

Figure 8: Comparison of the three phased array architectures

## 1.4. Existing phase shifter

After considering where to introduce the phase shift, the next question is how to shift the phase. Many different types of phase shifters have been developed over the years. We review some of the most common techniques used.

### 1.4.1. Lumped element phase shifter

One of the most conceptually straightforward ways of introducing phase shift is by changing the length of the transmission line that the signal passes through. The signal's transmission time can be varied as a result. That however is physically impractical. To achieve the same effect varactor-loaded transmission line shown in Figure 9 can be used [18]. By electronically changing the varactor values in the low-pass  $\Pi$  network, different delays can be realized. The main advantage of this scheme is that it is passive and therefore low power. The downside is that to achieve a high phase resolution many  $\Pi$  network stages need to be used and this makes it hard to integrate on chip. High insertion loss in the network requires high gain amplifiers to offset and therefore cancels out the low power benefit. In addition, this type of phase shifter's output phase is typically not linear therefore makes its control circuitry complicated. There are many variations to this type of phase shifter, such as combined topologies of lumped low-pass filters and high-pass filters [19]. But these all suffer from the same issue of difficult to integration in CMOS since they all require multiple inductors.

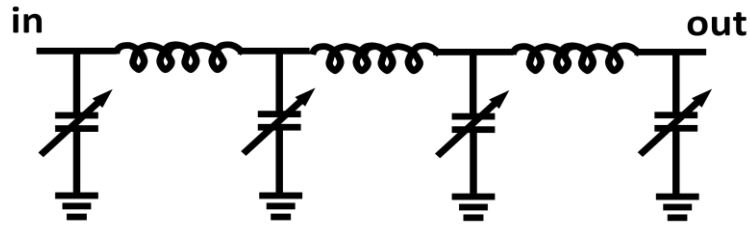


Figure 9: Varactor-loaded transmission line phase shifter

#### 1.4.2. Multiphase VCO

A phase shift scheme that can only be used with the phase shift at LO is to use a multi-phase VCO as the LO source [15]. LO signals with different phases supplied to different paths are generated using a ring of amplifiers shown in Figure 10. Although it can be easily integrated in CMOS, a multi-phase LO has very limited phase resolution and precise LO distribution is a daunting task in this scheme. Since each amplifier in the VCO usually contains an inductor for phase noise performance, its size is quite large when number of elements in the array is large.

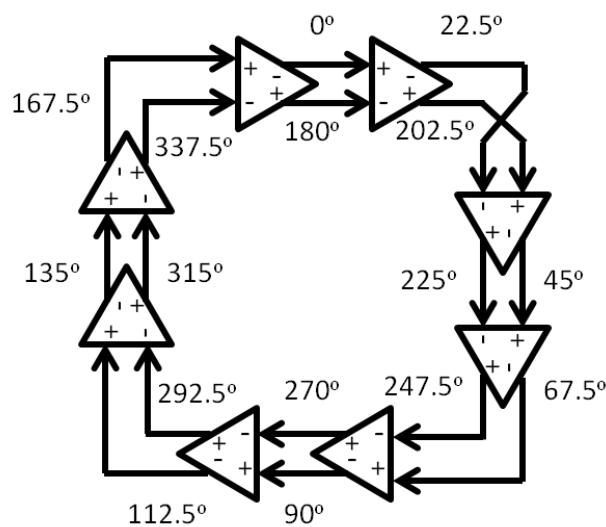


Figure 10: Schematic of a 16 phase ring VCO



### 1.4.3. Active phase interpolation

A phase shifting scheme that's becoming more popular in recent years is the phase rotator also called endless phase shifter or Cartesian phase shifter [20] [21][17]. The basic idea is by adding different weights of the orthogonal versions of the same signal an intermediate phase shifted signal can be produced as shown in Figure 11. The final output of the phase rotator is

$$out(t) = k_1 \cdot A \sin(\omega t) + k_2 \cdot A \cos(\omega t) \approx A \sin(\omega t + \theta) \quad 6$$

where  $\tan \theta = k_1/k_2$ .

As we can see from the equation above, the phase shift  $\theta$  is not linear with  $k_1$  and  $k_2$ . When  $k_1$  and  $k_2$  are set to uniform steps for the sake of implementation simplicity, phase shift has an error in some cases. The resolution of  $k_1$  and  $k_2$  determines the phase resolution of the phase shifter. Limited resolution of  $k_1$  and  $k_2$  also causes amplitude variation over different  $\theta$ . Because of this amplitude variation, this phase shifter works well with phase shift at LO, since LO signal is usually insensitive to amplitude variation. Also when used in a shift at LO architecture, it alleviates the problem of LO distribution precision issue, since each phase rotator will be local to the mixer and can be tuned individually. This type of phase shifter requires quadrature inputs however.

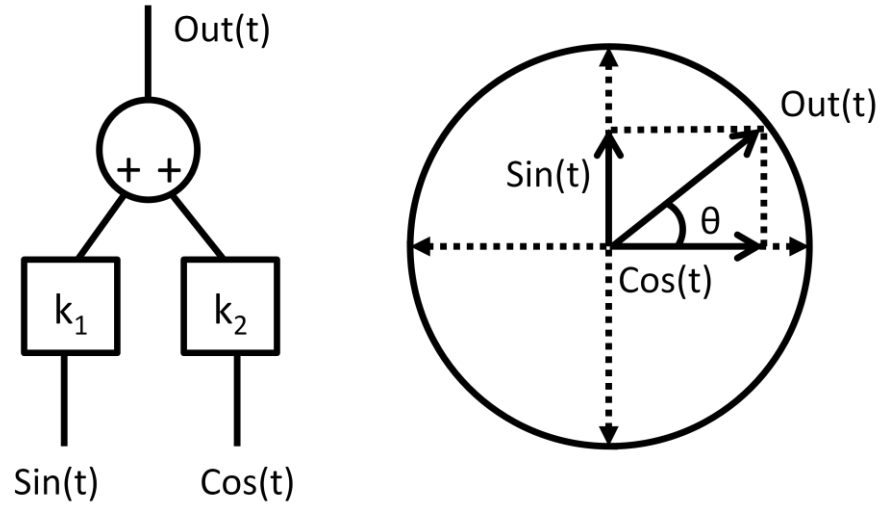


Figure 11: Phase interpolation scheme

The schematic of the original phase rotator circuit presented in [20] is shown in Figure 12. Differential quadrature I/Q signals are fed into the phase rotator through diff pairs. Differential variable gain common gate amplifiers (VGA) controlled by voltage  $V_{k1}$  and  $V_{k2}$  implements the  $k_1$  and  $k_2$  coefficients in Figure 11. The outputs of the VGAs are then summed to output the differential output,  $V_{out}$ . Some of the later implementations improve on this architecture and use pulse-width modulation (PWM) to control the amount of I and Q signals that go through to realize the coefficients [14] for more precise control.

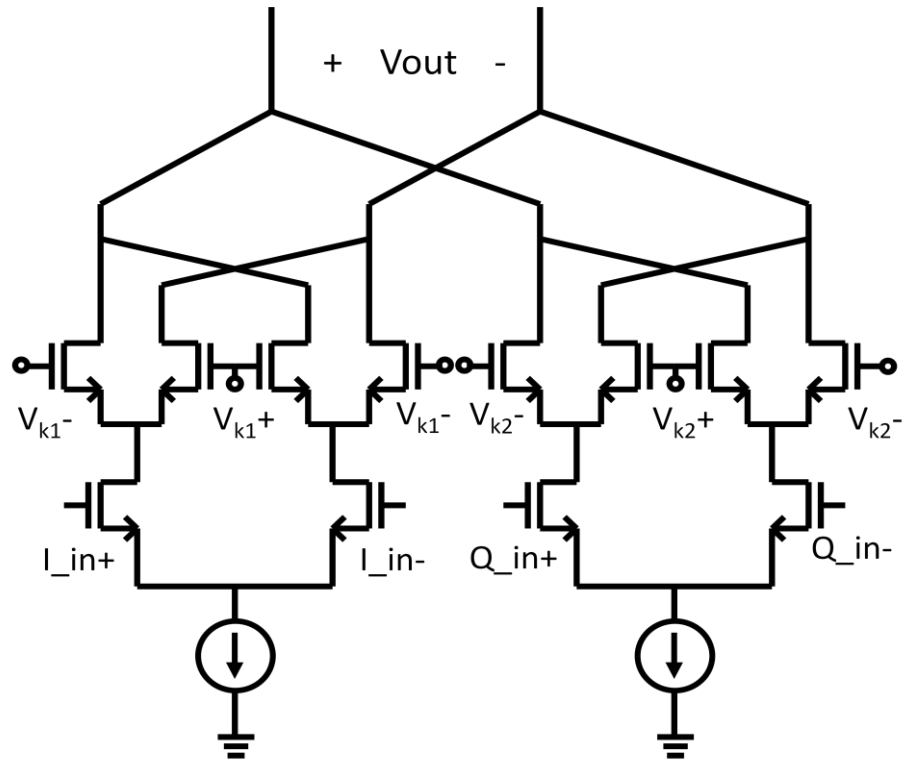


Figure 12: Phase rotator schematic

## 1.5. Conclusion

From discussion above, we can see that each of the three phase shift architectures have their own advantages and disadvantages and thus need to be used in conjunction with appropriate phase shifter. For shift at RF, the lumped elements phase shifter is the best choice, since at very high frequency passive elements used are small and their performance is very linear [13]. For shift at DC, the phase rotator is a good choice since it does not use any large passive components whose sizes are inversely proportional to frequency, therefore more CMOS compatible [14]. For shift at LO, the phase rotator is also a good choice, since LO is insensitive to insertion loss and other non-idealities caused by high frequency [9][16].

This thesis focuses mainly on phased arrays with frequency lower than mm-wave range thus we do not compare with shift at RF. For shift at DC and LO, the disadvantages of using the phase rotator are mainly the non-linearity of output phase versus control signal and the requirement for quadrature inputs. When used in phase shift at DC, noise performance becomes an issue. When used in shift at LO, distribution of high frequency LO signals is a problem. Although the LO signal's phase delay is not as important in shift at LO, distributing a signal close to RF frequency can still be difficult and power consuming. This thesis presents an architecture utilizing PLLs that solves these issues while retaining most of its benefits.

## **Chapter 2**

### **PLL Basics**

#### **2.1. Introduction to PLL**

The concept of phase locked loop (PLL) was first developed in the 1930's [22]. Since then, it has been widely used in a wide range of applications from communication to clock generation and many more. In essence a phase lock loop is a feedback control system that generates an output signal whose phase is locked to the input reference phase. Just like in an op-amp, by changing the feedback factor, output frequency is a multiple of the input frequency. The core components include a phase frequency detector (PFD), loop filter, a voltage controlled oscillator (VCO) and a frequency divider as shown in Figure 13 [23]. The VCO generates an output signal that is proportional to the input voltage. The frequency divider divides this output to a lower frequency. The PFD compares the phase between the input reference signal and the divided down output. Finally the PFD output is filtered by the loop filter and fed back to the VCO input to complete the loop. The final VCO output phase is proportional to the input phase, and its frequency is the input frequency times the divider ratio.

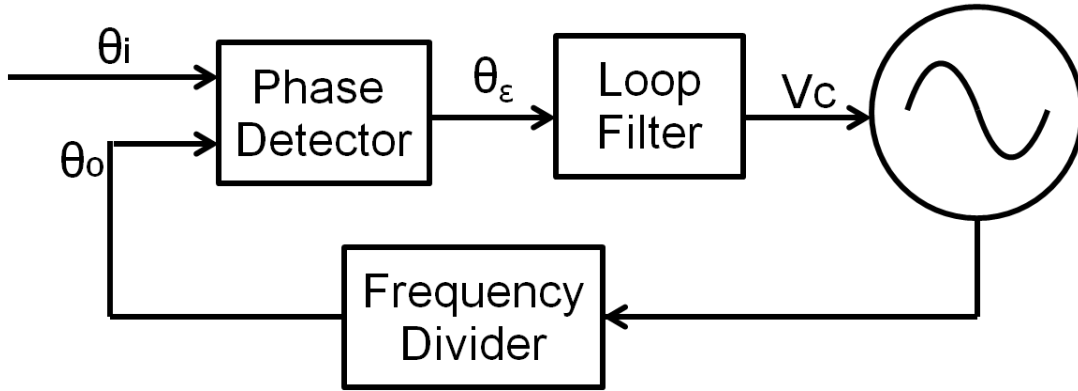


Figure 13: Simple PLL block diagram

A linear model of the PLL is shown in Figure 14. The phase detector is represented as  $K_{pd}$  with units of V/rad. Since its function is to linearly transfer phase information to a voltage, therefore it's just a linear gain element in the system. The loop filter is presented by its transfer function  $F(s)$ . A different  $F(s)$  changes the PLL behavior as we will discuss later. The VCO is represented by a gain block  $K_{vco}$  with units of Hz/V and an integrator. The VCO's input is a voltage representation of phase error information, but its output is frequency. Since phase is integral of frequency, a VCO has an innate integration. And finally the frequency divider divides phase linearly, and therefore is represented as  $1/N$ , where  $N$  is the divide ratio.

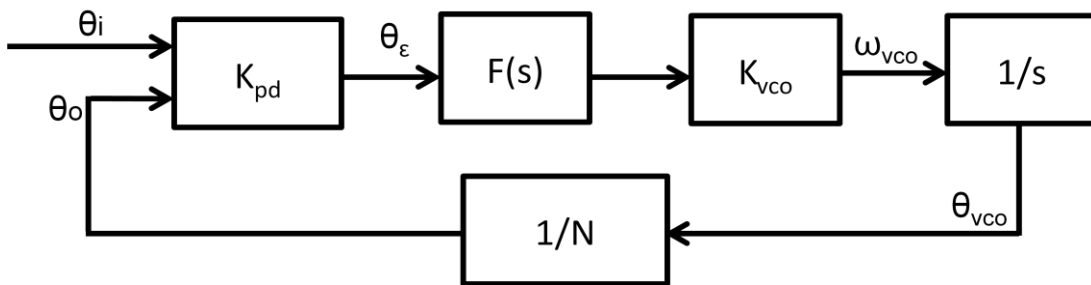


Figure 14: Linear PLL model

Using this model, we can derive the input and output phase transfer function as,

$$\frac{\theta_{vco}}{\theta_i} = \frac{K_o K_{pd} F(s)}{K_o K_{pd} F(s) / N + s} \quad 7$$

From this equation, we can see that as the frequency goes to 0, the output phase is N times the input phase. Since frequency is the derivative of phase, the output frequency is also N times the input phase.

## 2.2. Traditional charge-pump phase detector

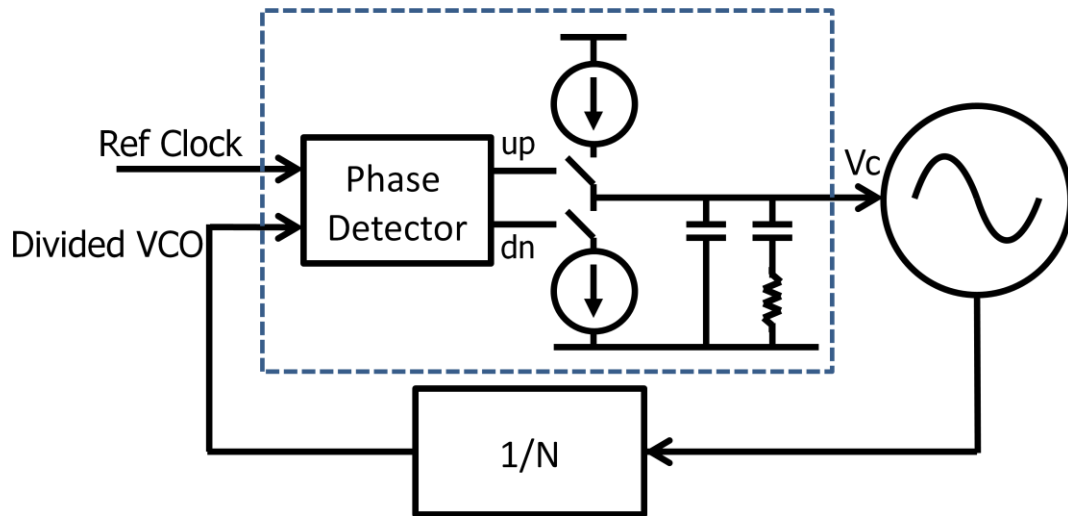


Figure 15: Charge-pump PLL schematic

One of the most common PLL architectures presented in [24][25] is a charge-pump PLL shown in Figure 15. The VCO generates a high frequency signal. The divider divides it down to a lower frequency which is then compared with a reference clock of approximately the same frequency. Typically both the divided down signal and the reference clock are both square waves. Therefore the phase detector can be a digital combinational-logic circuit that determines which clock edge is ahead. A simplified version only uses a XOR gate. Depends on which clock is ahead, the current sources in the charge pump either pump charge onto the load capacitors or takes charge out. The amount of charge put in or taken out is determined by the length of the up and down pulse which in turn represents the phase error of the VCO output signal. The final VCO control voltage is filtered by a lead-lag filter implemented by two capacitors and one resistor.



The biggest drawback of this architecture is the phase detector/charge pump/filter circuitry shown in dotted box in Figure 15 is analog intensive and prone to mismatch and process variation. The exact current output of the two current sources has to be very accurate, since phase detector gain  $K_{pd}$  in this case is  $I_{cp}/2\pi$ , where  $I_{cp}$  is the charge pump current. Although the phase detector is a digital circuit, the phase information represented by the length of the up and down pulse is still an analog signal and needs to be very accurate. Charge can also feed through to the integration capacitor when the up and down switches switch [26].

### 2.3. Type I PLL vs. Type II PLL

A Type I PLL has one integrator in its open loop transfer function. Normally this integrator is the VCO, which converts input frequency into phase. Since phase is the integral of frequency, the VCO acts as an integrator as discussed earlier. On the other hand, a Type II PLL has two integrators. Beside the VCO, it also has an integrator in the loop filter. A Type II PLL forces the steady state phase detector error to zero because the phase error is integrated by the additional integral. Due to this high pass effect, a Type II PLL also suppresses close to carrier up-converted flicker noise. However Type II loops are harder to design and require a stabilizing zero.

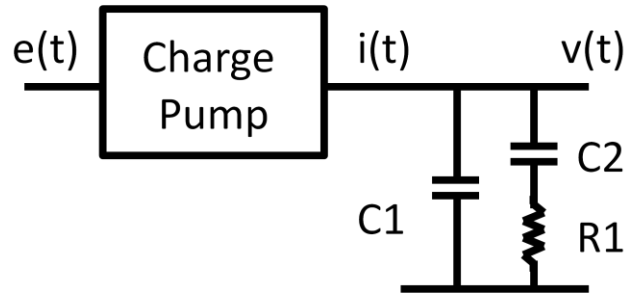


Figure 16: Simplified charge pump loop filter

The conventional Type II PLL architecture is shown in Figure 15. Looking at its loop filter in Figure 16, the charge pump and  $C_2$  forms an integrator in the loop. This extra integrator makes this architecture Type II. The resistor  $R_1$  in series with  $C_2$  introduces a stabilizing zero. Moreover a smaller capacitor  $C_1$  is added in parallel to smooth out the ripple caused by the addition of  $R_1$ . The final loop filter transfer function is given in [25] as,

$$F(s) = \frac{s + \frac{1}{R_1 C_2}}{s C_2 \left( s + \frac{1}{R_1 \left( \frac{C_1 C_2}{C_1 + C_2} \right)} \right)} \quad 8$$

As we can see, it has one pole at the origin,  $\frac{1}{s C_2}$  which is the integrator, one zero at

$\frac{1}{R_1 C_2}$ , and one pole at  $\frac{1}{R_1 \left( \frac{C_1 C_2}{C_1 + C_2} \right)}$ . The loop's stability is maintained if the zero

frequency is much lower than the pole frequency. A rule of thumb is  $f_z/f_p = 1/8$ .

## 2.4. Fractional-N divider

In all the discussions above the frequency divide ratio is always an integer  $N$ , because integer division is easy to achieve in CMOS since it is simply a digital counter. But fine output frequency step is important for selecting the right band for telecommunication purposes and for other applications. We could use a small reference value. However that is impractical, because PLL is a sampled system. We can think of phase error as being sampled at the PFD by the reference signal. To avoid aliasing, a reference frequency higher than the loop bandwidth is needed. Therefore we cannot use an arbitrary low reference frequency and thus fractional divide ratio is necessary.

One of the first attempts to implement a fractional divider is switching between different integer divide ratios. This way a fractional divide ratio can be achieved. For example, by switching between divide ratios of 1, 2, 1, 2..., the resulting average divide ratio is 1.5. However this type of highly repetitive pattern causes fractional spurs in the PLL's output.

A better way to switch divide ratio is to use a  $\Sigma\Delta$  modulator. In this case the PLL is referred to as a  $\Sigma\Delta$  fractional-N PLL. A  $\Sigma\Delta$  modulator converts a high precision value into a stream of quantized lower precision values and keeps the output's average equal to the input. A simple first order  $\Sigma\Delta$  modulator and its typical output when fed a constant decimal value are shown in Figure 17. We can see from the output that a constant input of 12.368746 is converted to a stream of 12s and 13s. The average of the stream is still 12.368746 and no obvious periodicity can be seen from

the stream. How to incorporate such divider in a PLL is shown in Figure 18. The  $\Sigma\Delta$  modulator converts the fractional divide ratio into a stream of integers and feeds it to the divider. Using this type of divider, fractional divide ratio with low fractional spur can be achieved.

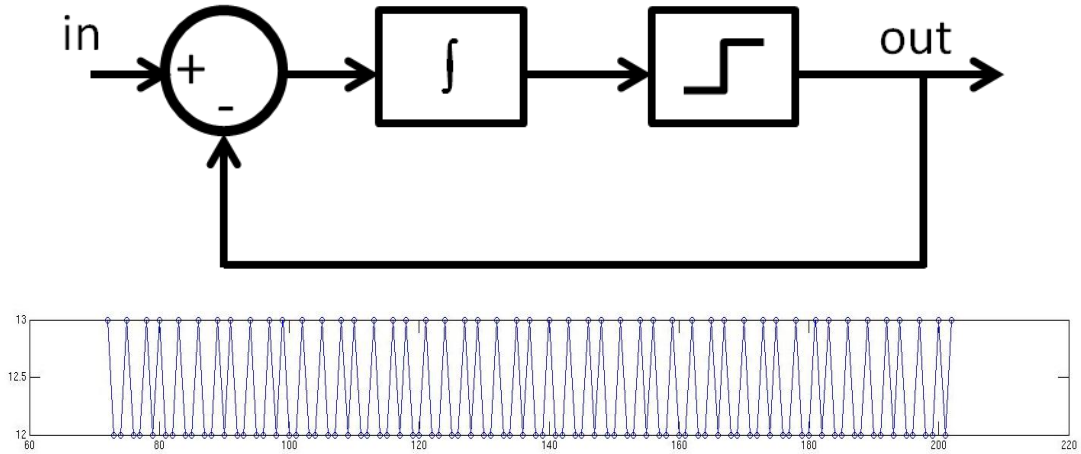


Figure 17: First order  $\Sigma\Delta$  modulator and typical output with a constant input

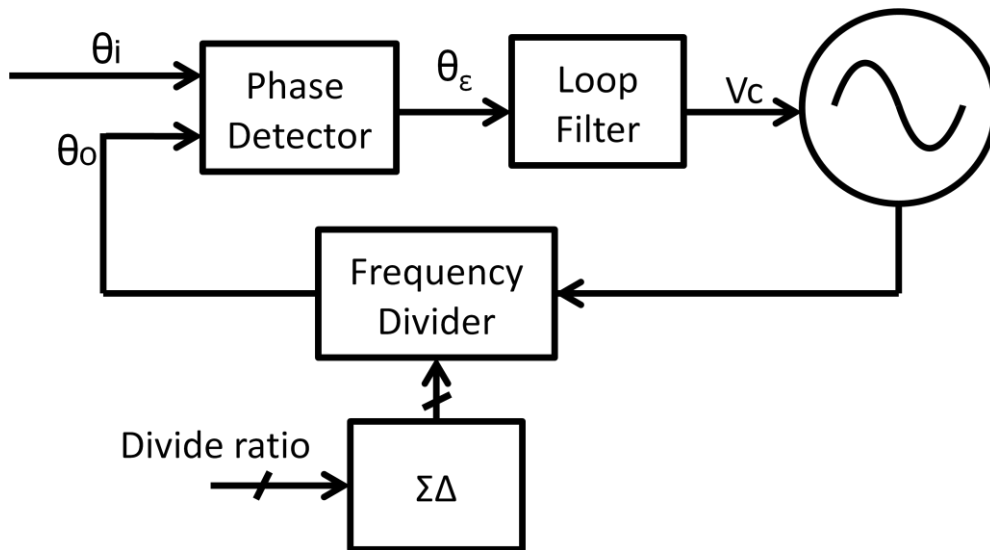


Figure 18:  $\Sigma\Delta$  fractional-N PLL

## 2.5. PLL phase noise analysis

Typically a  $\Sigma\Delta$  PLL has three main sources of phase noise, VCO noise, PFD noise and  $\Sigma\Delta$  noise. VCO noise and PFD noise are common to all PLLs. Their origin can be thermal noise,  $1/f$  noise, or digital switching noise.  $\Sigma\Delta$  noise is quantization noise associated with the  $\Sigma\Delta$  modulator used in the divider. A typical Type II  $\Sigma\Delta$  PLL phase noise plot is shown in Figure 19. The PLL bandwidth is 100 kHz in this example. PFD noise spectrum is generally flat. The loop simply acts as a low pass filter and attenuates the PFD noise outside the bandwidth. A  $\Sigma\Delta$  modulator has noise shaping effect that pushes noise to higher frequency. Therefore  $\Sigma\Delta$  noise spectrum has high pass behavior. However  $\Sigma\Delta$  noise is also low pass filtered by the loop, the combined effect is a band pass response. A free-running VCO's phase noise linearly decreases 20dB/decade, if we ignore  $1/f$  noise. VCO noise however is not low pass filtered, but high pass filtered. This is because VCO noise adds directly to the output. Intuitively, the feedback loop will try to keep the output aligned. Inside the bandwidth, the gain is high enough to minimize the error, but outside the feedback loop won't be fast enough to suppress the error. Therefore as can be seen in Figure 19, the VCO noise contribution is attenuated inside the PLL bandwidth, but not outside. Overall, a higher bandwidth suppresses more VCO noise, but at the same time it lets through more PFD noise and  $\Sigma\Delta$  noise. Thus there is a PLL bandwidth where total phase noise is minimized.

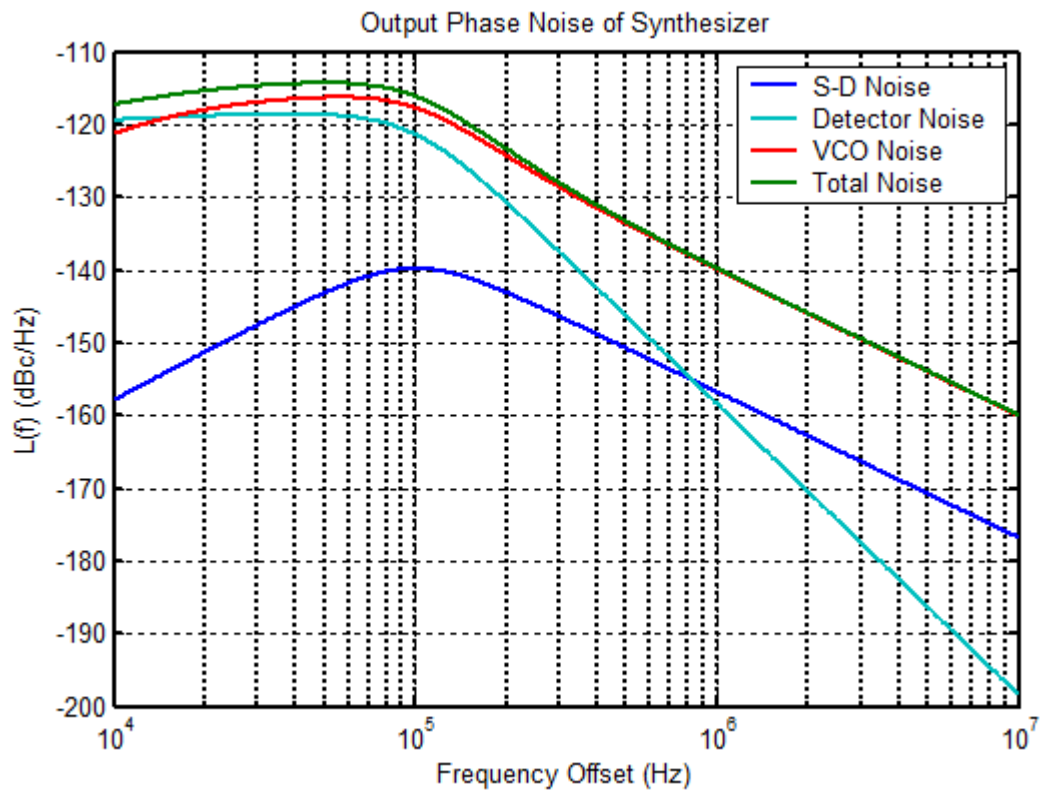


Figure 19: Typical type II  $\Sigma\Delta$  PLL phase noise plot with PLL bandwidth of 100 KHz generated with cppsim

## **Chapter 3**

### **Phase-Setting PLL**

#### **3.1. Background**

Accurate phase control of high-speed signals is required in serial links, radar, beam-steering and medical imaging systems. CMOS integrated phased-array transceivers offer enormous possibilities for secure, low cost wireless communication systems [9][15][3]. One of the main challenges in realizing these applications in CMOS is the implementation of a precise, flexible, and physically small phase shifter. Multi-phase VCOs have limited resolution, RF phase shifters are expensive and hard to design, and baseband phase shifters require bulky components. On the other hand, phase interpolation requires quadrature inputs, has limited linearity and is prone to phase error due to amplitude variation.

We present a digital PLL architecture that can make precise high-resolution steps in phase of its output signal. Here phase control is implemented in the digital domain; no additional analog circuits are required other than the PLL itself. This phase generation mechanism consumes little power, and it does not affect the phase noise of the PLL.



### 3.2. Overview of phase control mechanism

This work presents a new fractional-N PLL architecture to implement precise, high-resolution programmable setting of phase. Conceptually, the most straightforward way of achieving a phase change at the output of a PLL is to add a time delay  $\Phi$  to the input reference path as shown in Figure 20a [27]. Instead, we achieve the same result by adding a signal  $K_{pd}\cdot\Phi$  that is proportional to the PFD gain,  $K_{pd}$ , at the PFD output, show in Figure 20b. In the first case, the output phase  $\theta_o$  is

$$\theta_o = \frac{K_o K_{pd} F(s)}{s} (\theta_i + \Phi - \theta_o) \quad 9$$

where  $F(s)$  is the loop filter transfer function,  $K_o$  is the VCO gain and  $\theta_i$  is the input reference phase. In the second case,  $\theta_o$  is

$$\theta_o = \frac{K_o F(s)}{s} (K_{pd}(\theta_i - \theta_o) + K_{pd}\Phi) \quad 10$$

And in both cases,  $\theta_o$  can be represented as

$$\theta_o = \frac{K_o K_{pd} F(s)}{K_o K_{pd} F(s) + s} (\theta_i + \Phi) \quad 11$$

Comparing equation 11 to a standard PLL's transfer function

$$\theta_o = \frac{K_o K_{pd} F(s)}{K_o K_{pd} F(s) + s} (\theta_i) \quad 12$$

We see that the resulting phase change at the output of the PLL is  $\Phi$  times the PLL closed loop response in equation 12. Using this phase setting technique in combination with a digital PLL architecture, very precise phase can be set. Moreover no additional analog circuitry is required.

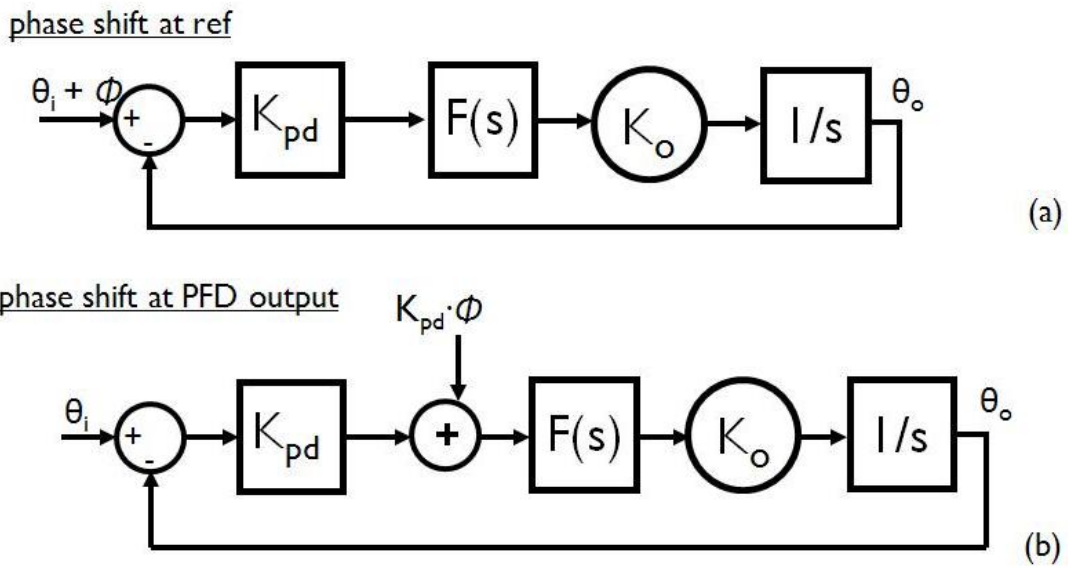


Figure 20: Two conceptual approaches to phase shift

In an analog PLL, the  $K_{pd} \cdot \Phi$  signal addition might be done by adding a current proportional to  $K_{pd}$ , usually proportional to the charge pump current, and the desired phase shift. This approach is impractical, because it requires a very well-controlled and programmable current source. Instead, we introduce a digital PLL implementation of this concept that avoids the limitations of the analog approach. In this work, a digital 1-bit TDC PFD with a phase alignment loop introduced in [6] is used. The advantage of this approach is that a digital phase-shift equivalent of  $K_{pd} \cdot \Phi$ , matched to the PFD gain, can be added at the output of the PFD. Since the PFD gain is digitally well-controlled, very accurate phase shifting can be achieved. The output phase vs. digital control is very linear and thus the digital control circuitry can be very simple. The output phase change is only dependent on digital parameters. This allows almost infinite theoretical phase resolution. In practice, phase resolution is limited by the length of the phase shifting code word however.

### 3.3. PLL architecture

The phase-setting PLL, shown in Figure 21, leverages the oversampling 1-bit TDC digital architecture presented in [6]. The architecture mainly consists of a 1-bit TDC PFD, a loop filter, a 6-bit resistor-string  $\Sigma\Delta$  DAC, a 2<sup>nd</sup> order  $\Sigma\Delta$  fractional-N divider and a VCO. A 1-bit TDC PFD compares a 430MHz reference clock with the divided down feedback signal. After passing through the digital loop filter, the digital output is converted to analog by a 6-bit resistor-string  $\Sigma\Delta$  DAC and fed to the VCO. An 8-15 programmable divider, controlled by a 3-bit 2<sup>nd</sup> order  $\Sigma\Delta$  modulator, divides down the VCO output. Finally, a simple power-amplifier, implemented as a two-stage self-biased amplifier, buffers the VCO output. Everything in the loop, with the exception of VCO gain is digital, and therefore the loop characteristics can be digitally controlled.

In the proposed PLL scheme, phase is adjusted adding a 16-bit word to the output of the digital PFD, before the second integrator. As discussed earlier, a PLL's output phase can be shifted by adding a proportional signal at the output of the PFD. Since most of the loop characteristics are digitally controllable, the 16-bit digital value can be set to achieve a precise phase. The phase shift precision is limited only by the 16-bit code word resolution. The instantaneous phase accuracy is limited only by the PLL's phase noise. We introduce a Type II PLL characteristic helps to substantially reduce any phase error compared to the reference clock.

Phase modulation can also be introduced through the same port as the phase shift. Digital modulation data is added to the phase shift data and applied to the output

of the PFD. Consequently the PLL can employ both phase modulation and phase setting. Next we will go through each block in detail.

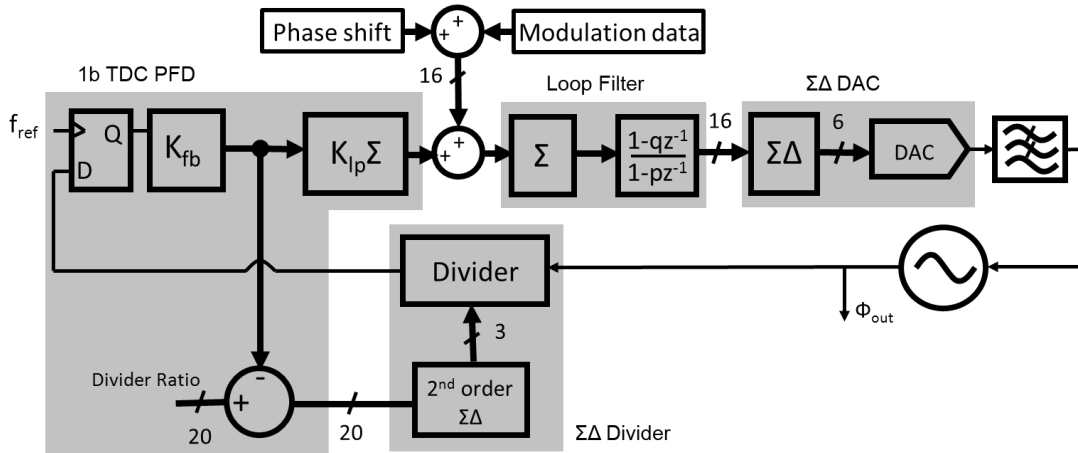


Figure 21: PLL modulator architecture

### 3.3.1. 1-bit TDC PFD

One of the key components used in a phase shifting PLL is the 1-bit TDC PFD with a phase alignment loop [6]. The 1-bit TDC simply consists of a flip-flop. The reference clock samples the divided down VCO output on its rising edge and determines whether the VCO output is ahead or behind. Compared to multi-bit TDC PFD, a single bit gives much less phase information. To overcome this issue, oversampling is employed. Using an ADC analogy, multi-bit TDC is akin to flash ADC, whereas the 1-bit TDC is analogous to oversampled ADC. In this case the reference clock is much faster than the loop bandwidth to achieve this oversampling. For this oversampling TDC to work, dithering is also required, otherwise the output might be stuck at 1 or 0. Fortunately dithering comes almost for free in this architecture in the form of noise. The  $\Sigma\Delta$  controlled divider of the PLL introduces

significant  $\Sigma\Delta$  noise to the divided down VCO output and dithers the signal. The final output of the TDC is filtered to remove the  $\Sigma\Delta$  noise. This PFD can also be seen as a type of bang-bang PFD.

Additionally a feedback loop shown in Figure 22 is added to minimize the phase difference between the reference clock and the divided down clock. If the phase difference is too large, the 1-bit TDC will rail to 1 or 0. The output of the TDC phase detector is scaled by a factor,  $K_{fb}$  and fed back to the divider ratio input. The feedback signal is subtracted from the divide ratio. If the phase detector indicates that the divided down clock is ahead, in which case the feedback signal is positive, then a lower the divide ratio slows it down, if it is behind, in which case the signal is negative, then an increase in the divide ratio speeds it up. This feedback loop keeps the phase difference small and keeps that output of the phase detector from railing.

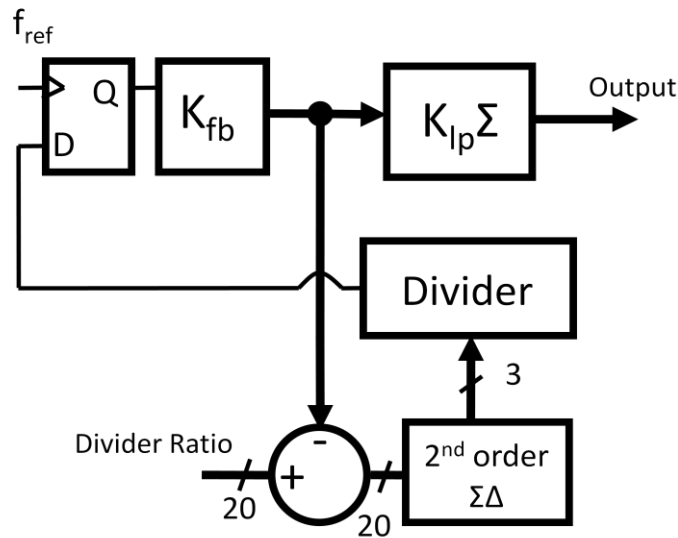


Figure 22: 1-bit TDC PFD block diagram

### 3.3.2. PLL Type

We would like to use a Type II PLL for phase setting operation. As discussed in section 2.3, a Type II PLL removes the dc phase error associated with a Type I PLL. The key to achieve a Type II PLL is to have two integrators in the loop. At first glance, it appears that the 1-bit TDC PFD contains an integrator and therefore no additional integrator is necessary in the loop filter. However upon closer examination, we see that the feedback loop in the PFD introduces a differentiation in the loop and cancels the integration. In Figure 22, the output of the  $K_{fb}$  block represents phase information, but it is subtracted from the divider ratio, which controls frequency. Phase is the integral of frequency. Integration in the feedback loop causes a differentiation in the whole loop. This can be seen from Figure 23. The transfer function of this system is

$$A \left( in - \frac{out}{s} \right) = out \quad 13$$

Simplifying we get

$$\frac{out}{in} = A \frac{s}{s+A} \quad 14$$

This transfer function consists of two components, the differentiation part  $s$  in the numerator and a pole at  $-A$  in the denominator. If  $A$  is sufficiently large so that the pole is higher in frequency than most other poles in the system, the pole can be ignored leaving only the differentiation component. Therefore without another integrator in the loop, a PLL using this PFD is Type I, as in [6]. However there is no

fundamental reason why the 1-bit TDC PFD cannot be used to realize Type II architecture.

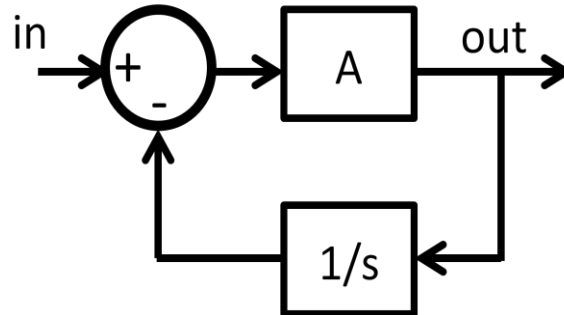


Figure 23: Linearized model of the PFD feedback loop

### 3.3.3. Loop filter

To achieve Type II behavior an additional integrator is required as well as a stabilizing zero. Therefore to stabilize the PLL, a digital pole zero pair is added to the loop filter, shown in Figure 21, after the second integration. What we want to achieve is a digital version of the RC filter shown in Figure 16, since that filter contains an integration at the same stabilize the overall closed loop behavior. Type II PLL removes static offset, which is prone to variation, improves the phase shift reliability and also suppresses close-to-carrier up-converted flicker noise.

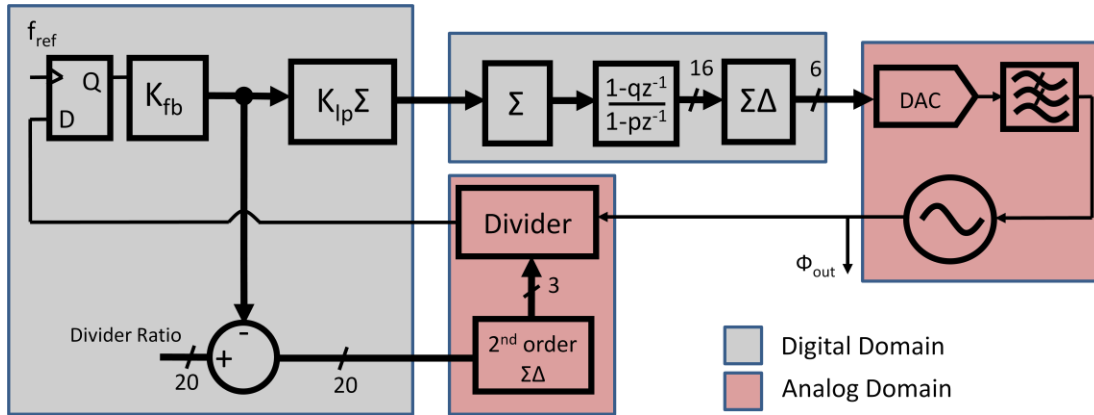


Figure 24: Digital and analog signal domains

We need a loop filter whose transfer function is identical to equation 8 to give us an integration and a stabilizing pole/zero pair. Looking at Figure 24, we can see that our loop filter is in the digital signal domain. However equation 8 is in continuous time domain. To convert between Laplace domain and Z domain, we can use the bilinear transform [28]

$$S = \frac{2}{T} \frac{z-1}{z+1} \quad 15$$

where T is the clock period. Using this transform on equation 8, we get

$$H(z) = \frac{\frac{2z-1}{Tz+1} + \frac{1}{R_1 C_2}}{\frac{2z-1}{Tz+1} C_2 \left( \frac{2z-1}{Tz+1} + \frac{1}{R(C_1 \parallel C_2)} \right)} \quad 16$$

Let zero,  $\omega_z = \frac{1}{R_1 C_2}$ , pole,  $\omega_p = \frac{1}{R_1 \left( \frac{C_1 C_2}{C_1 + C_2} \right)}$ , and ignore all constant factors from now on,

we get



$$H(z) = \frac{\frac{2z-1}{Tz+1} + \omega_z}{\frac{2z-1}{Tz+1} \left( \frac{2z-1}{Tz+1} + \omega_p \right)} \quad 17$$

We can separate the integral part and the pole zero pair, and then simplify.

$$H(z) = \frac{z+1}{z-1} \cdot \frac{\frac{2}{T}(z-1) + \omega_z(z+1)}{\frac{2}{T}(z-1) + \omega_p(z+1)} \quad 18$$

Converting everything to the form  $z^{-1}$  we get

$$H(z) = \frac{1+z^{-1}}{1-z^{-1}} \cdot \frac{1-z^{-1} \left( \frac{\frac{2}{T} - \omega_z}{\frac{2}{T} + \omega_z} \right)}{1-z^{-1} \left( \frac{\frac{2}{T} - \omega_p}{\frac{2}{T} + \omega_p} \right)} \quad 19$$

What we have is an integrator  $\frac{1+z^{-1}}{1-z^{-1}}$ , a zero  $q_1$  at  $\left( \frac{\frac{2}{T} - \omega_z}{\frac{2}{T} + \omega_z} \right)$ , and a pole  $p_1$  at  $\left( \frac{\frac{2}{T} - \omega_p}{\frac{2}{T} + \omega_p} \right)$ .  $\omega_z$

and  $\omega_p$  are pole zero frequencies in a traditional Type II PLL. Using this transfer function, pole/zero values and open loop gain can be chosen appropriately for the required bandwidth. By plotting its gain and phase Bode plots, using the basic phase margin criterion, loop stability can be inferred. In practice, these values can be calculated using cplusplus. Cplusplus utilizes a close loop approach algorithm, which determines the close loop response of the transfer function based on desired criteria such as loop bandwidth. From the close loop transfer function, the open loop transfer function is calculated and the loop filter transfer function is then derived [29]. After obtaining the transfer function, we need to implement it in digital circuitry. We

separate the integrator and the pole zero pair into two blocks. Since the transfer function is basically output divided by input,

$$H(z) = \frac{Out}{In} \quad 20$$

We can substitute in the transfer function and get

$$\frac{Out}{In} = \frac{1+z^{-1}}{1-z^{-1}} \quad 21$$

$$Out (1 - z^{-1}) = In (1 + z^{-1}) \quad 22$$

$$Out = In + In z^{-1} + Out z^{-1} \quad 23$$

$z^{-1}$  is delay by one time step in the  $z$  domain. Therefore the output is the un-weighted sum of the current input, the previous input, and the previous output. However if we simply implement this in digital, we will have an issue. Because the PFD block before the integrator  $K_p \Sigma$  in Figure 24 outputs an unsigned value, if we simply accumulate the inputs, the output will monotonically increase and overflow. Therefore we offset the unsigned value to the midpoint to create both positive and negative value. Furthermore the previous input term,  $In z^{-1}$  only introduces a FIR filter to the overall function and doesn't affect integration. After close loop simulation in both cppsim and Spectre we found that this term can be ignored. Therefore the final output is

$$Out = In + Out z^{-1} - K_{mid} \quad 24$$

We can use the same method to obtain the equation for the pole zero pair.

$$\frac{Out}{In} = \frac{1 - q_1 z^{-1}}{1 - p_1 z^{-1}} \quad 25$$

$$Out = In - q_1 In z^{-1} + p_1 Out z^{-1} \quad 26$$

Since a scaled version of the previous input is subtracted, the output is not monotonically increasing and therefore does not overflow. Cascading the integrator and the pole zero pair forms the digital equivalent of the loop filter shown in Figure 16.

This stability of the PLL is then verified with Spectre simulations. To verify that the phase is stable, we look at the integral of the VCO's control voltage. The VCO control voltage is proportional to the frequency of the VCO and therefore its integral is proportional to the phase. By looking at the integral of VCO control voltage, which is proportional to the output phase, we can make sure that the loop is settled with no significant ringing.

#### 3.3.4. VCO

A schematic of the VCO and the output buffer schematic is shown in Figure 25. LC VCOs are usually used in transmitters because of their low phase noise requirements. Coarse tuning is necessary for the VCO to oscillate in the right frequency range. A simple self-biased inverter-based buffer is used to buffer the output. All stages are ac coupled to avoid dc biasing issues.

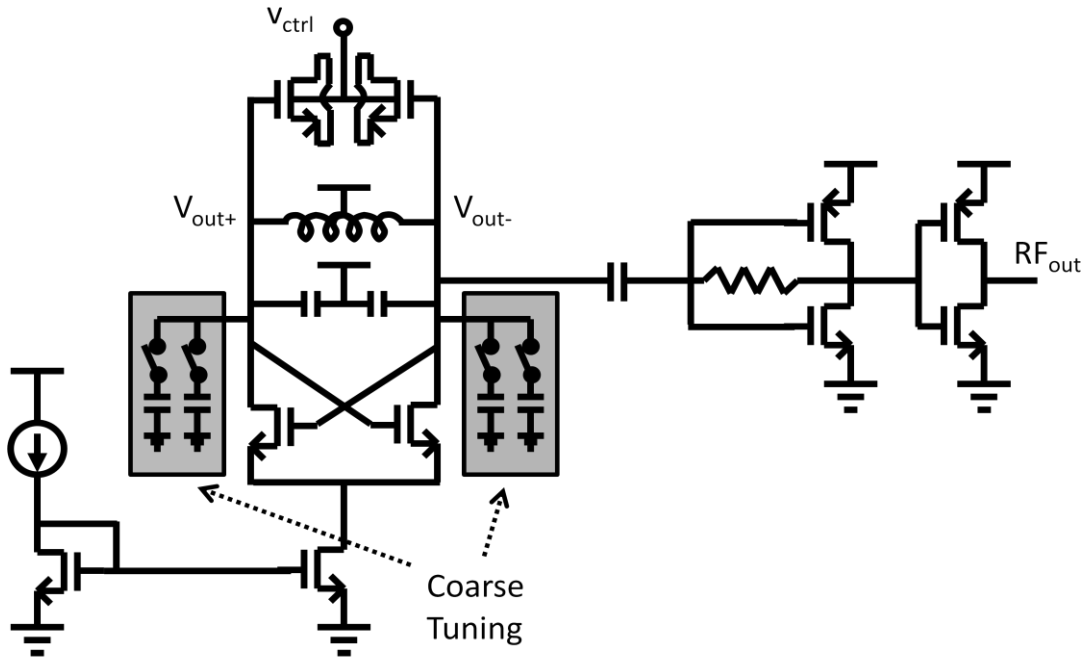


Figure 25: VCO and output buffer schematics

### 3.4. Data modulation

To achieve a phased array transmitter, the system not only has to set output phase, it also needs to be able to modulate data. In a PLL, there are several places where output phase or frequency can be modulated. We discuss two of the architectures that we examined.

#### 3.4.1. Divide ratio modulation

The most common data modulation method is frequency modulation by changing the divider value as shown in Figure 26.

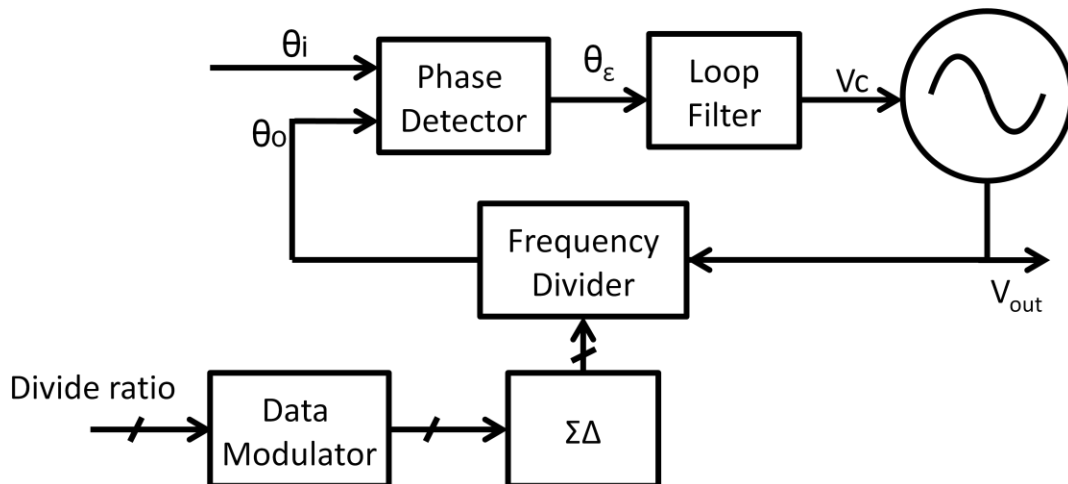


Figure 26: Divide ratio modulator

Since output frequency  $V_{out}$  is described by the following equation,

$$f_{out} = N \cdot f_{ref} \quad 27$$

where  $N$  is the divide ratio and  $f_{ref}$  is the input reference frequency, by changing  $N$  we can change the output frequency and perform FM or FSK.

This modulation scheme has some issue when working in conjunction with our phase-setting mechanism. Since during data transition when divide ratio is changing, the loop is out of lock. During the rellocking process, the final output phase could potentially shift. This presents an issue for this architecture as it interferes with phase setting. To overcome this issue, our first attempt was to split the roles of phase shifting and data modulation into two different stages of cascaded PLLs as shown in Figure 27. The first stage is a low frequency PLL responsible for phase-setting; the second stage is a high frequency PLL responsible for data modulation. The first stage of PLLs produces four phase-shifted reference signals. This reference is then feed into the second stage, which modulates the signal. The two stage cascaded architecture is able to combine the two functions in a single system.

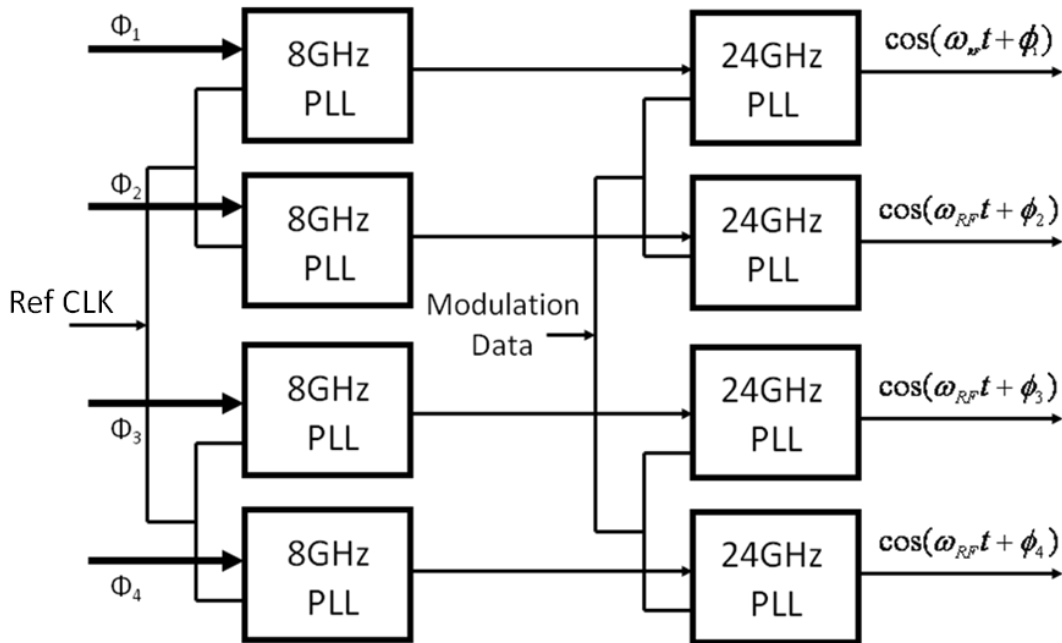


Figure 27: two-stage cascading PLL architecture

However this architecture has a few major drawbacks. The biggest issue is its large size and power consumption. By using two PLLs, we almost double the size and power compared to a single PLL system. The design complexity is also immensely increased. The second problem is increased phase noise. The phase noise of the first stage is amplified by the second stage as explained in [30]. Due to these major issues, this method is not a viable solution.

### 3.4.2. Direct phase modulation

Another place to add modulation data to a PLL is to add it after the PFD [4]. This is the same terminal where we add phase setting value. In another words, by varying the phase setting value in Figure 20, we can easily achieve PM or PSK. Since we already have the phase shifting capability, phase modulation comes almost for free. This phase modulation can be superimposed onto our phase shift schemes and enables both phase modulation and phase shifting. As highlighted in Figure 28, the phase shift value and the modulation data are added before being applied to the PLL. In this architecture both phase modulation and phase setting can be achieved at once, with little overhead.

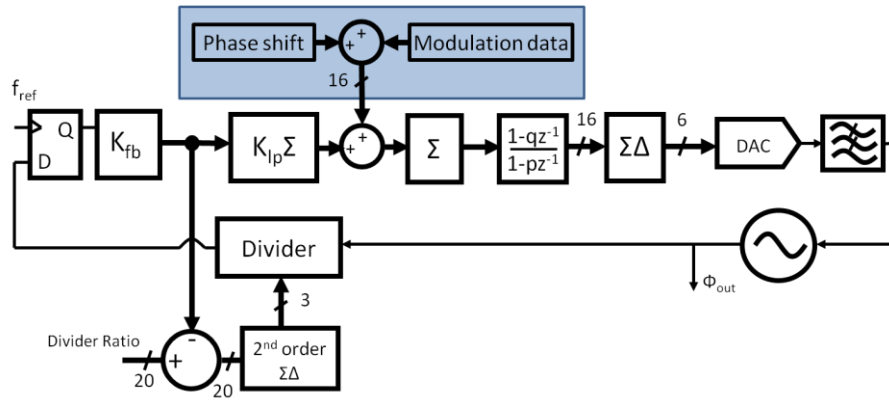


Figure 28: Phase modulation and phase setting superimposed together

### **3.5. Phased array and conclusion**

As we can see from the above discussion, PLL is the natural system to use for phase shifting applications. With both phase setting and data modulation capabilities, we only need to employ copies of this PLL to achieve a phased array. The final phased array transmitter architecture is shown in Figure 29. The phased-array system consists of 4 phase-setting PLLs described previously. The four PLLs each receive the same reference signal. Since each PLL can independently set phase, the phased-array function is achieved by shifting each PLL's phase by a set incremental amount. Furthermore, due to this independence, any phase mismatch in the four channels can be calibrated. The phase shifting input can also be used to perform PSK modulation as described before.



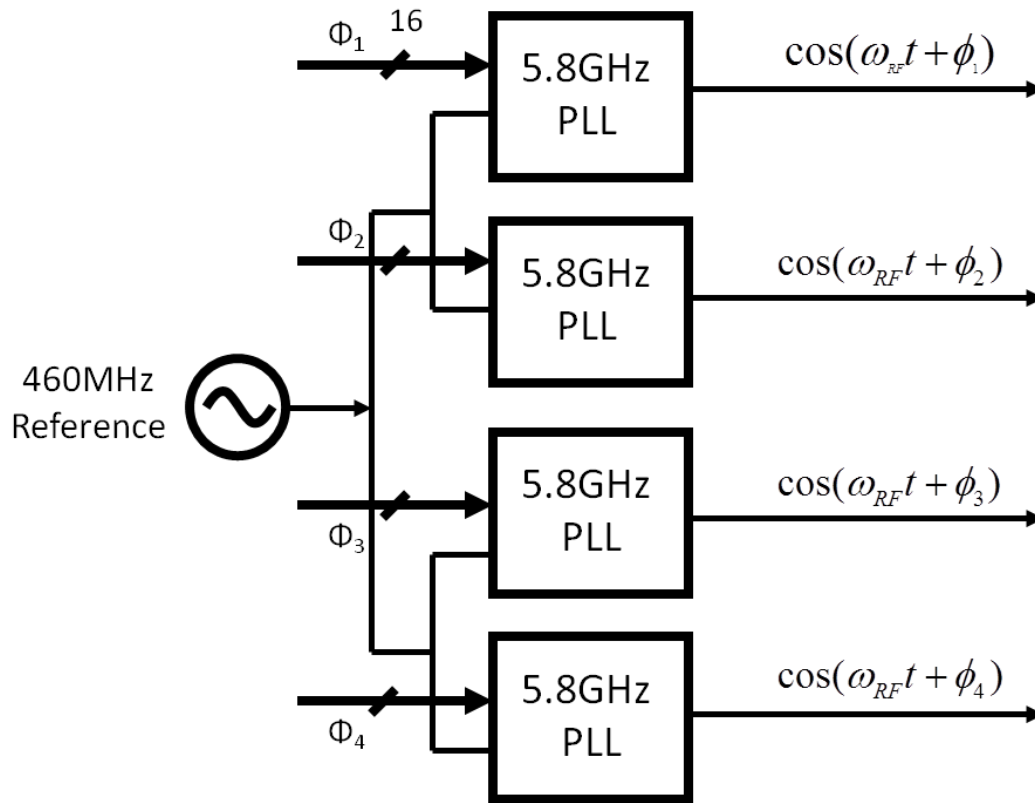


Figure 29: Phased array system diagram

Overall the phased array system includes four 5.8GHz phase-setting PLLs each capable of PSK modulation. Each channel has an output buffer that buffer the output to a measurable signal level.

## **Chapter 4**

### **Prototypes and Measurements**

#### **4.1. Overview**

A total of three prototypes were implemented all in 65nm CMOS technology. The first prototype is a 24GHz PLL phased array utilizing an architecture shown in Figure 27. Due to the major drawbacks discussed earlier, a second prototype with an updated architecture is fabricated. The second prototype is a 5.8GHz PLL phased array with a PLL architecture shown in Figure 21. The third prototype is also a 5.8GHz PLL phased array with the same architecture as the second prototype aimed at improving upon the second prototype's performance.

## 4.2. First Prototype

The first prototype is a 24GHz PLL phased array utilizing a cascading PLL architecture. It is implemented in 65nm CMOS and a die photo is shown in Figure 30. It occupies  $2\text{mm} \times 2\text{mm} = 4\text{mm}^2$ . The prototype consumes 55mW per channel and a total of 210mW. The two stage cascaded 24GHz PLL successfully locked to the reference signal. However beside the architectural drawbacks discussed earlier, its output signal is smaller than expected, which makes testing more difficult. This was due to a VCO design mistake where not enough current was supplied to the VCO. Nevertheless FSK modulation with a bandwidth up to 2MHz was achieved in this prototype shown in Figure 31.

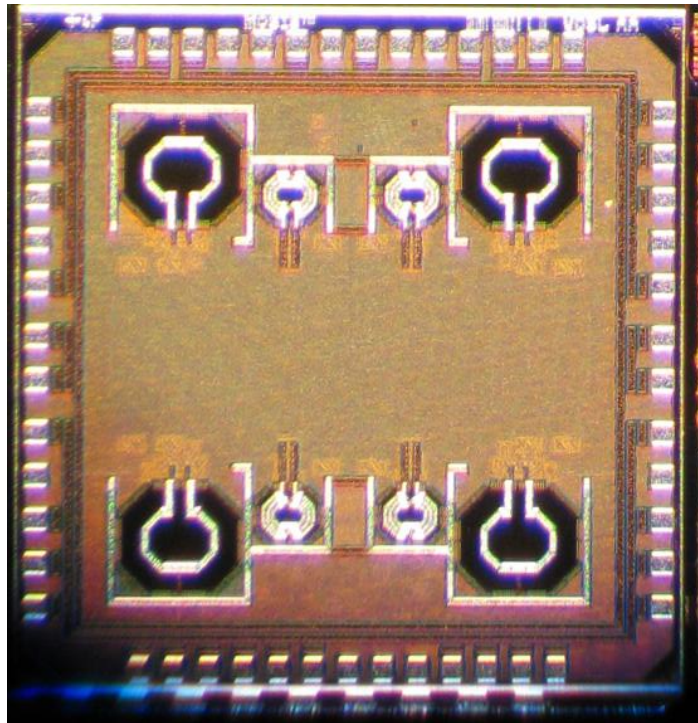


Figure 30: Die micrograph of the first prototype

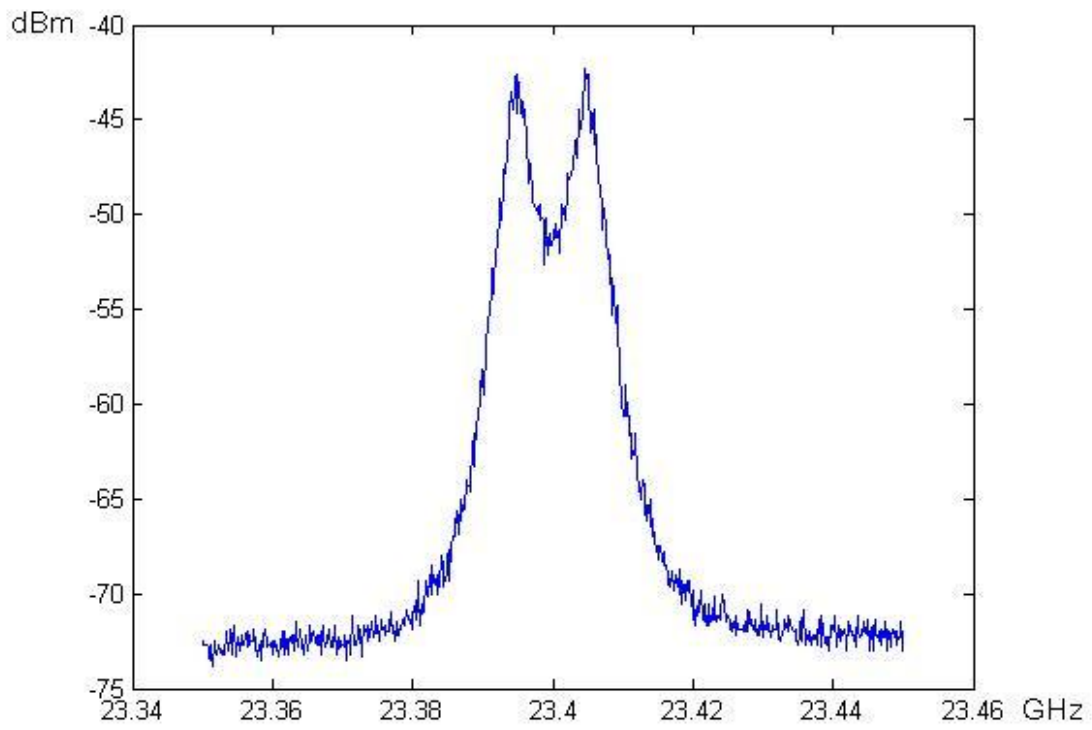


Figure 31: 2MHz BFSK modulated spectrum

### 4.3. Second Prototype

The second prototype is a 5.8GHz PLL phased array with a PLL architecture shown in Figure 21. It is implemented in 65nm CMOS and occupies  $0.133\text{mm}^2$  per channel. Die micrograph of a single channel is shown in Figure 32. The entire device consumes 13mW, including the estimated 3mW power consumption of the output buffer. The analog circuitry consumes 6.1mA from a 1.1V supply, and digital circuitry consumes 6.2mA from a 1V supply.

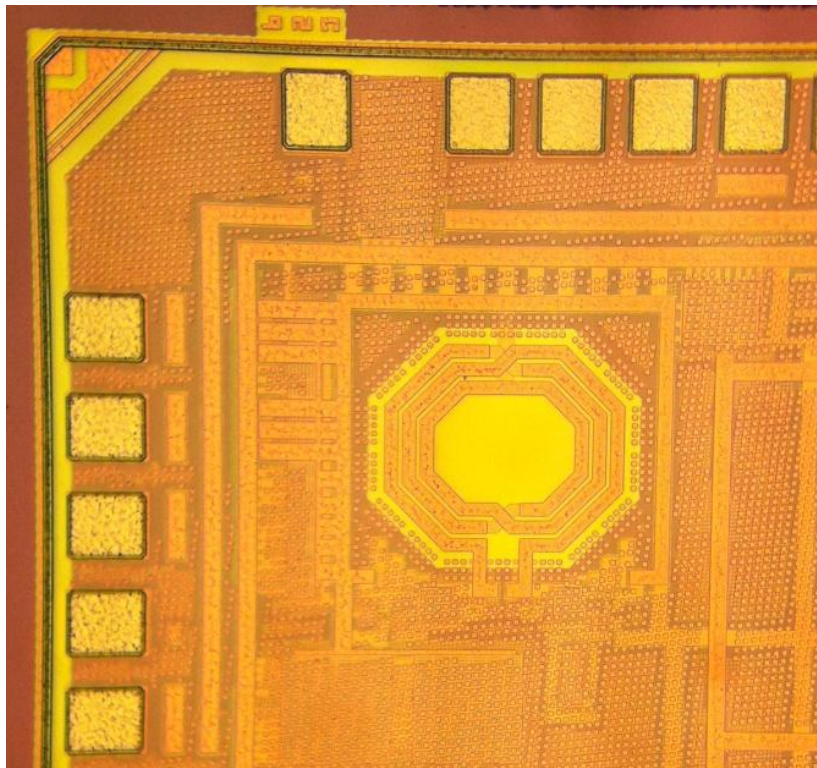


Figure 32: Second Prototype Die micrograph

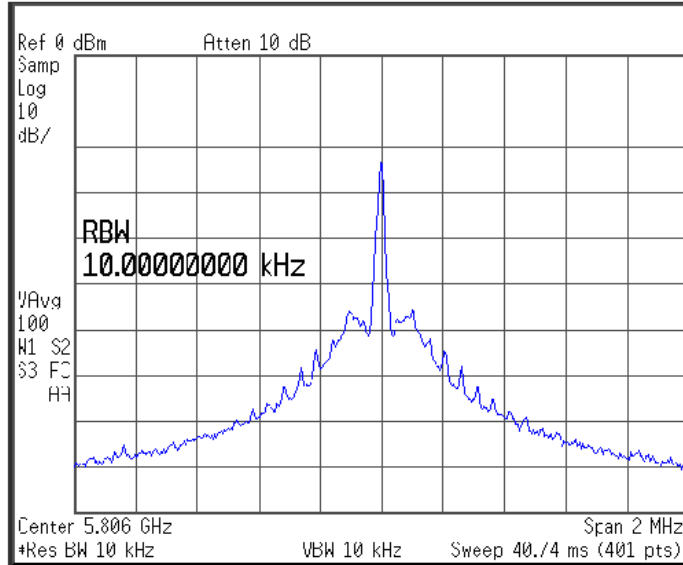


Figure 33: Locked PLL spectrum

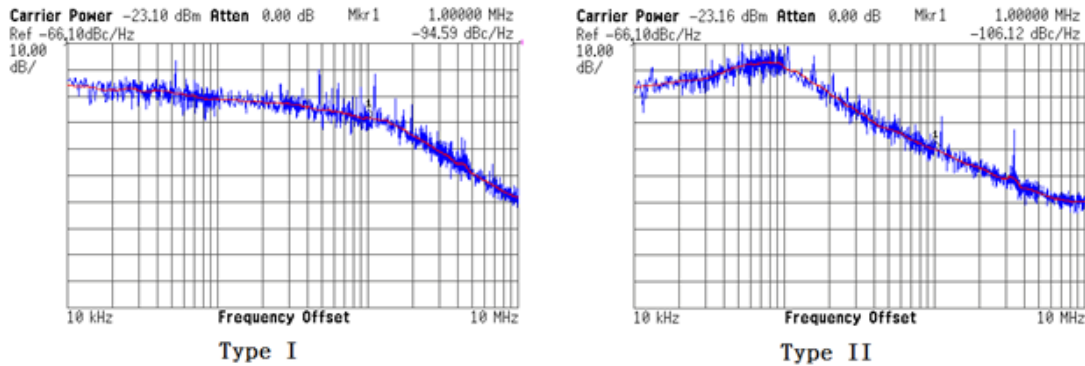


Figure 34: Comparison of measured type I & II mode phase noise with the same loop parameters.

The PLL achieves a measured phase noise of -106.12dBm at 1MHz offset and -125.94dBm at a 10MHz offset. Type II operation can be enabled or disabled in the prototype with all parameters staying the same, except that the second integrator is turned off in Type I mode. Measured phase noise profiles for Type I and Type II modes are compared in Figure 34. As expected, the Type II mode suppresses in-band

noise much better than Type I. The effects of phase shifting are measured by overlaying the output before and after shift on an oscilloscope in histogram mode.

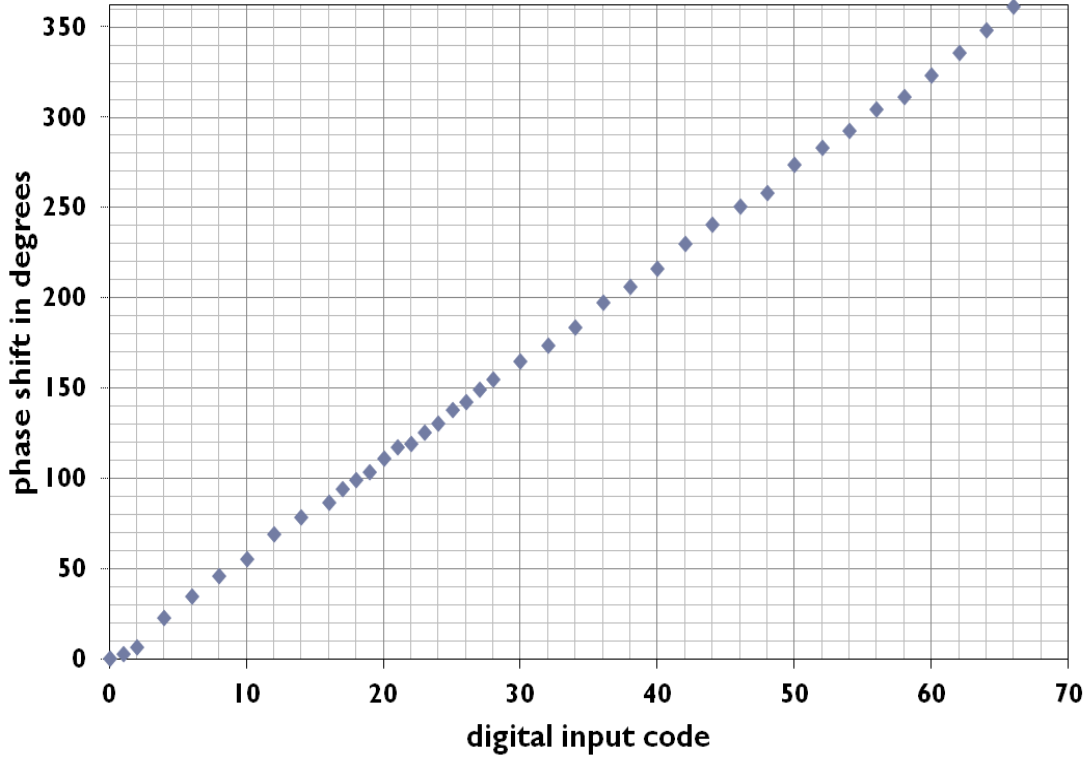


Figure 35: Measured phase shift vs. input code at 5.8GHz

Figure 35 shows a plot of the measured input digital code versus phase shift from 0-360°. A minimal detectable phase shift of 1.5° and a phase range of more than 540° are achieved. The maximum phase shift is limited by the size of the internal digital buffers. A phase shift of 180° settles within 37µs. The modulator is also capable of PSK modulation and Figure 36 shows the measured constellation plot of QPSK modulation with a rate of 34 kHz. Data is generated externally and feed to the prototype.

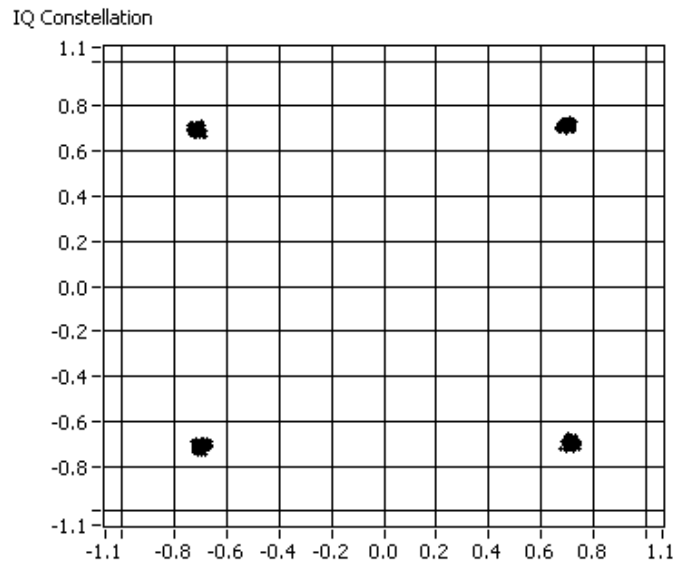


Figure 36: Measured 34kHz QPSK constellation plot



#### 4.4. Third Prototype

The third prototype is also a 5.8GHz PLL phased array with the same architecture as the second prototype. It is also implemented in 65nm CMOS and occupies  $0.133\text{mm}^2$  per channel. A die micrograph is shown in Figure 37. The entire device consumes 11mW, including the estimated 3mW power consumption of the output buffer. The analog circuitry consumes 8mA from a 1V supply, and digital circuitry consumes 3mA from a 1V supply.

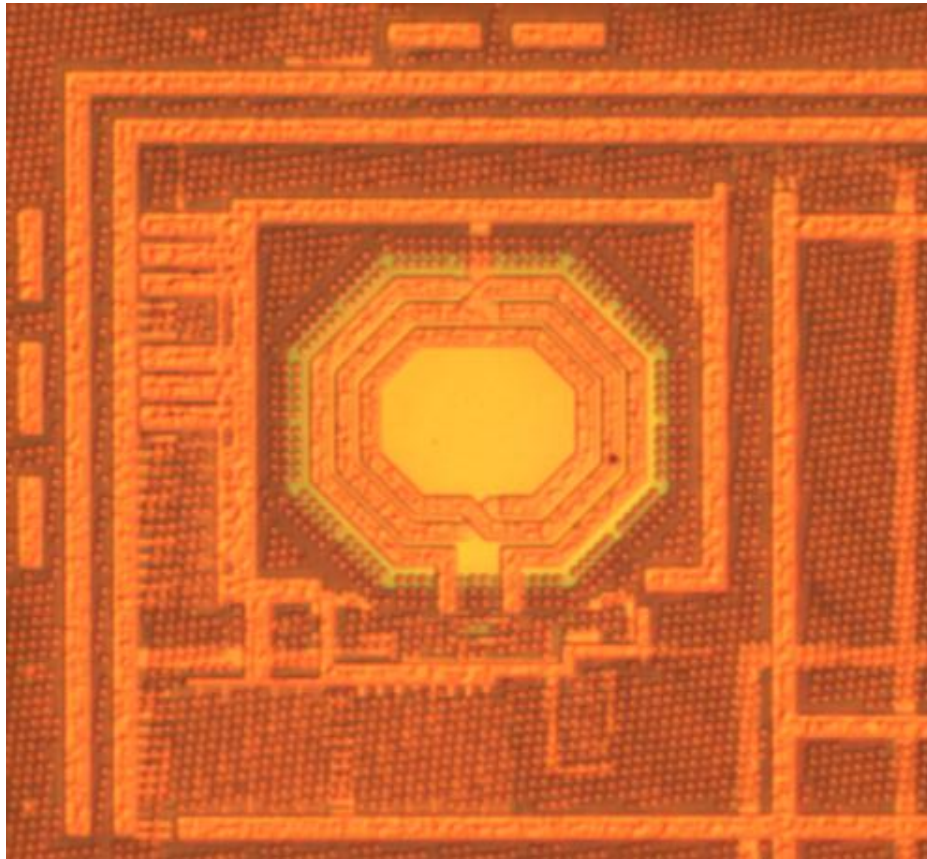


Figure 37: Third Prototype Die Micrograph

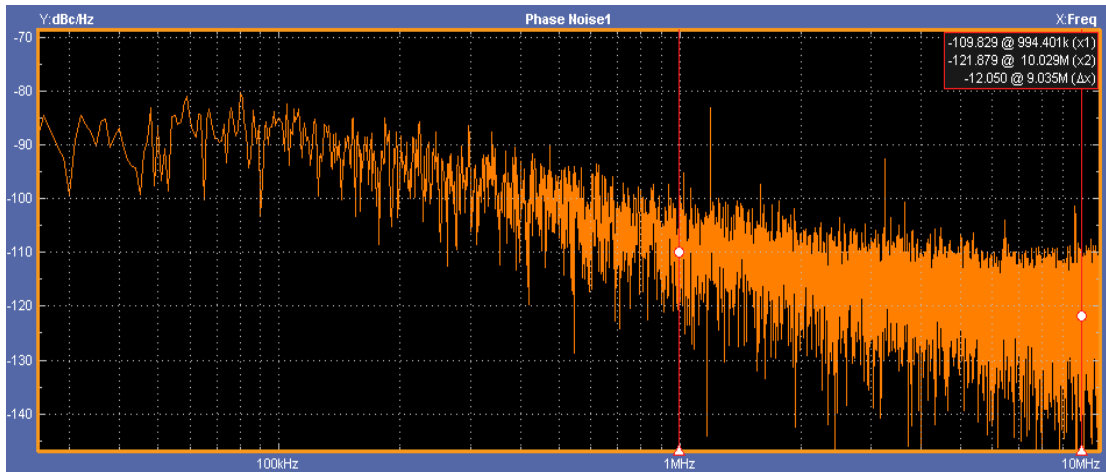


Figure 38: Phase noise plot of the type II PLL

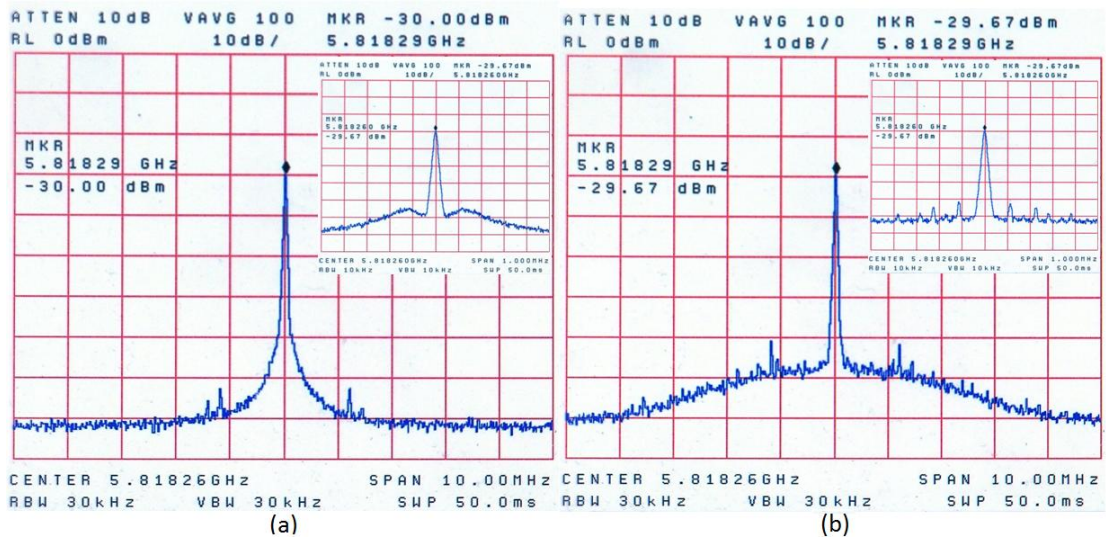


Figure 39: (a) Type II PLL spectrum and zoomed in 1MHz spectrum (b) Type I PLL spectrum and zoomed in 1MHz spectrum with the same loop parameters as the type II in (a)

The PLL achieves a measured phase noise of -110dBm at 1MHz offset and -122dBm at a 10MHz offset. The rms jitter is 1.03ps. The phase noise plot of the Type II PLL is shown in Figure 38. Type II behavior of the loop suppresses in-band noise before 100kHz. As with the first prototype, Type II operation can be enabled or disabled in the prototype with all parameters staying the same, except that the second

integrator is turned off in Type I mode. Measured spectrum profiles for Type I and Type II modes are compared in Figure 39. As expected, the Type II mode suppresses in-band noise much better than Type I.

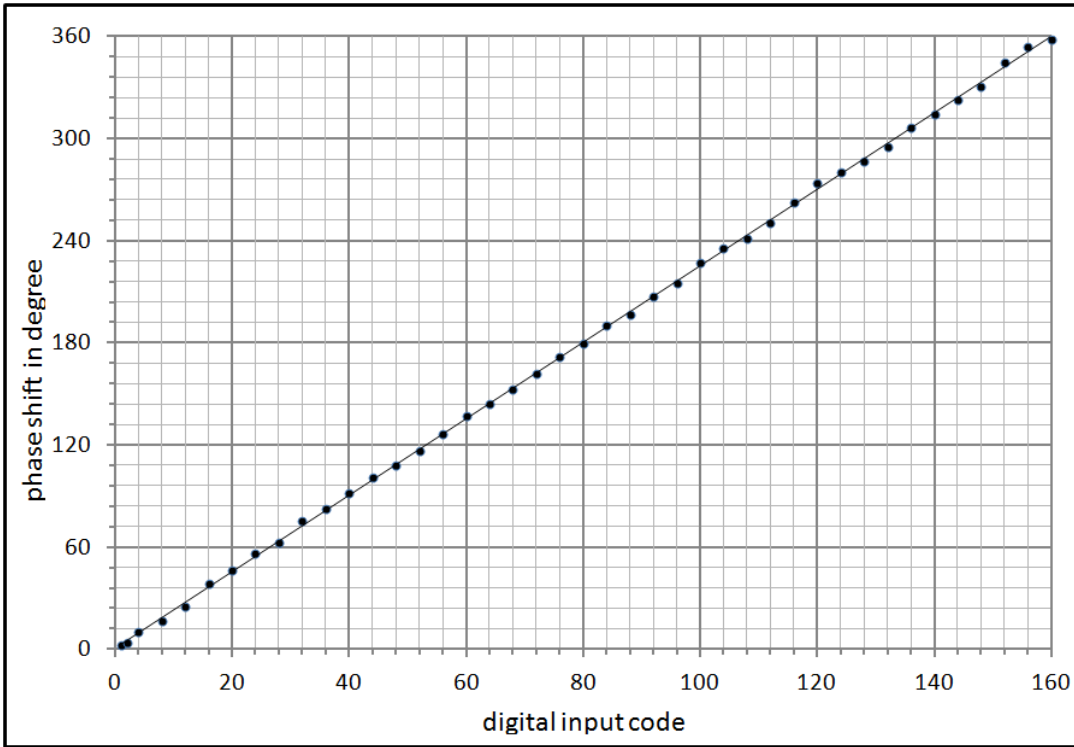


Figure 40: Phase shift vs. digital input

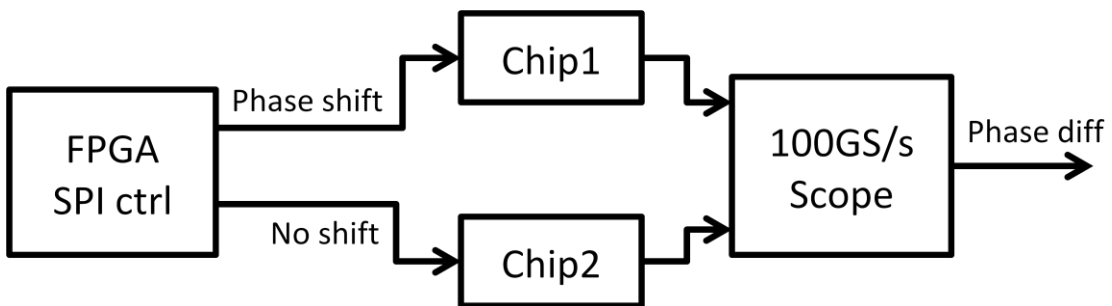


Figure 41: Phase shift test setup

Figure 40 shows a plot of the measured input digital code versus phase shift from 0-360°. Phase shift is measured by measuring the average phase difference

between two phase-setting PLLs, with one generating a fixed phase to serve as a measurement reference shown in Figure 41. An average phase shift of  $2.25^\circ$  or 7.3bits of phase resolution and a phase range of more than  $720^\circ$  are achieved. The maximum phase shift is limited by the size of the internal digital buffers, and the minimal phase shift is limited by phase noise. A phase shift of  $90^\circ$  settles to within  $3^\circ$  accuracy within  $10\mu\text{s}$ . The modulator is capable of most PSK modulations. The constellation plot of a 30.05 kHz 8-nary PSK is shown in Figure 42. The eight symbols are well apart with no overshoot or ringing. Modulation data is generated externally and feed to the prototype. The measured performance and a comparison with recent works are summarized in Figure 43.

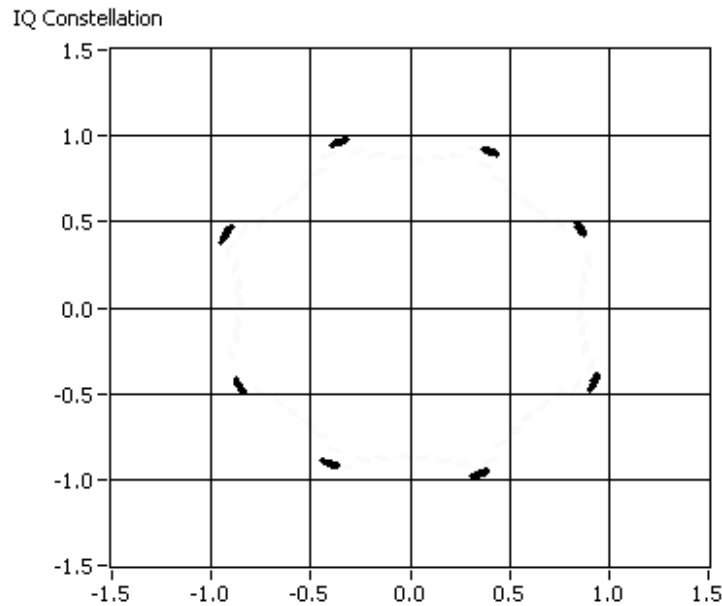


Figure 42: Measured Constellation plot of 30 kHz 8-nary PSK

Four such prototypes are put together on a single printed circuit board (PCB) to realize a phased array. The test setup with two channel connected are shown in Figure 43.

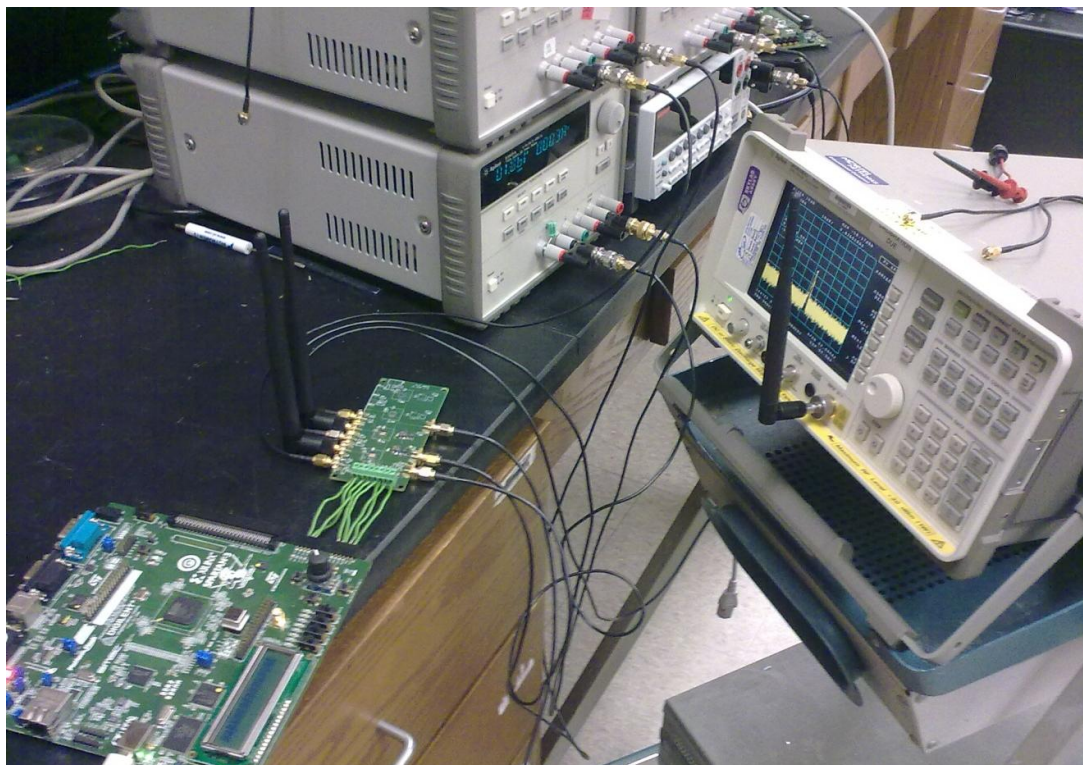
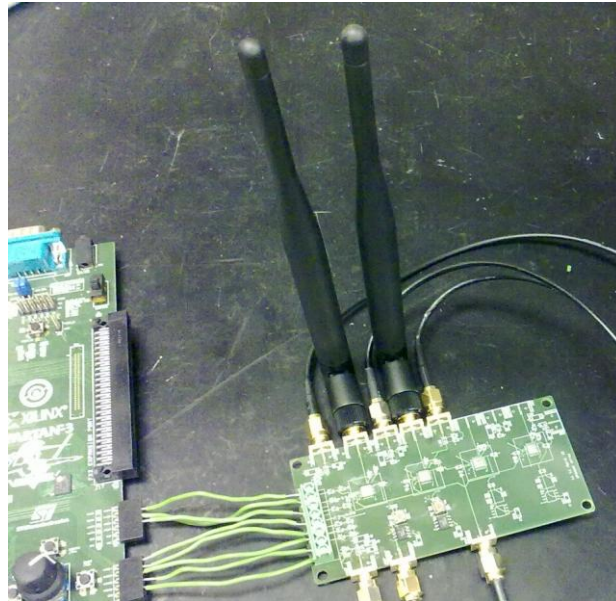


Figure 43 Phased array PCB with 2 channels connected

	This Work	[16]	[31]	[32]	[33]	[9]	[3]	[17]	[14]	[13]
process	65nm CMOS	0.25 $\mu$ m CMOS	0.18 $\mu$ m CMOS	MEMS	MEMS	0.18 $\mu$ m CMOS	0.13 $\mu$ m CMOS	0.12 $\mu$ m SiGe BiCMOS CS	65nm CMOS	0.12 $\mu$ m SiGe BiCMOS CS
freq.	5.8GHz	5.2GHz	4GHz	1-2GHz	100MHz-40GHz	24GHz	24GHz	77GHz	60GHz	60GHz
phase shift resolution	2.25 $^{\circ}$	10 $^{\circ}$	N/A	5.625 $^{\circ}$	22.5 $^{\circ}$	22.5 $^{\circ}$	N/A	Varies	5.625 $^{\circ}$	11.25 $^{\circ}$
power consumption per channel	11mW	61mW	66mW	passive	passive	492mW*	245mW*	300mW*	34mW*	237mW*
modulation	PSK	64-QAM	OOK	N/A	N/A	QPSK	PM	QPSK	QPSK	OFDM
*include PA power										

Figure 44: Results summary and comparison with other work

## **Chapter 5**

### **Conclusion**

#### **5.1. Key contributions**

The primary contribution of this work is the development and demonstration of a novel CMOS phased array architecture using phase-setting PLLs. Various conventional CMOS phased array architectures are either CMOS incompatible due to component size or have output phase resolution or linearity limitations. This work overcomes these shortcomings.

Compared to existing phased array architectures discussed in section 1.3 and 1.4, this architecture has many advantages. This architecture does not require low loss phase shifters at RF frequencies, which are difficult to build. The output before the PA is an un-attenuated full-scale signal. Also it does not require any large phase shifters that are hard to integrate onto CMOS.

Compared to the popular phase rotator architecture discussed in section 1.4.3, this architecture retains most of its benefits while improves on some of its shortcomings. First of all, the most important advantage of this architecture is that it can achieve a very linear and high resolution phase shift. The output phase vs. input

digital code linearity is outstanding. The phase resolution is only limited by the PLL's phase noise. The prototype achieves the highest phase resolution reported. Although in a phased array system with few elements, this resolution would not be fully utilized. In a large array with high number of elements, high phase resolution could translate to very fine radiation angle. Secondly this architecture does not require complicated high frequency LO distribution network. Although you still need to distribute the reference clock signal to all PLLs, it's at a much lower frequency than the output RF frequency. Nothing special need to done to ensure its proper distribution. And finally this architecture does not require quadrature I/Q signals.

In addition, this work improves on previous digital PLL design to achieve Type II behavior with a 1-bit TDC PLL architecture. This improvement allows this popular architecture to suppress in-band noise and reduces overall jitter. In doing so, we demonstrate that one of this digital PLL architecture's shortcomings can be overcome.



## 5.2. Future works

One difficulty encountered in this work is the problem of on chip inductor coupling. Since inductor coupling is stronger as their resonance frequency get closer, inductors used in PLLs experience the worst case scenario. To overcome this issue, one of the solutions is to use VCOs with different frequencies in each channel shown in Figure 45. Each VCO in the original design is replaced with a real VCO and a frequency multiplier. The combined output of the two blocks is still at the original RF frequency. But each VCO has a different oscillating frequency and thus does not couple to the other VCOs. A low noise frequency multiplier is a challenge in this architecture.

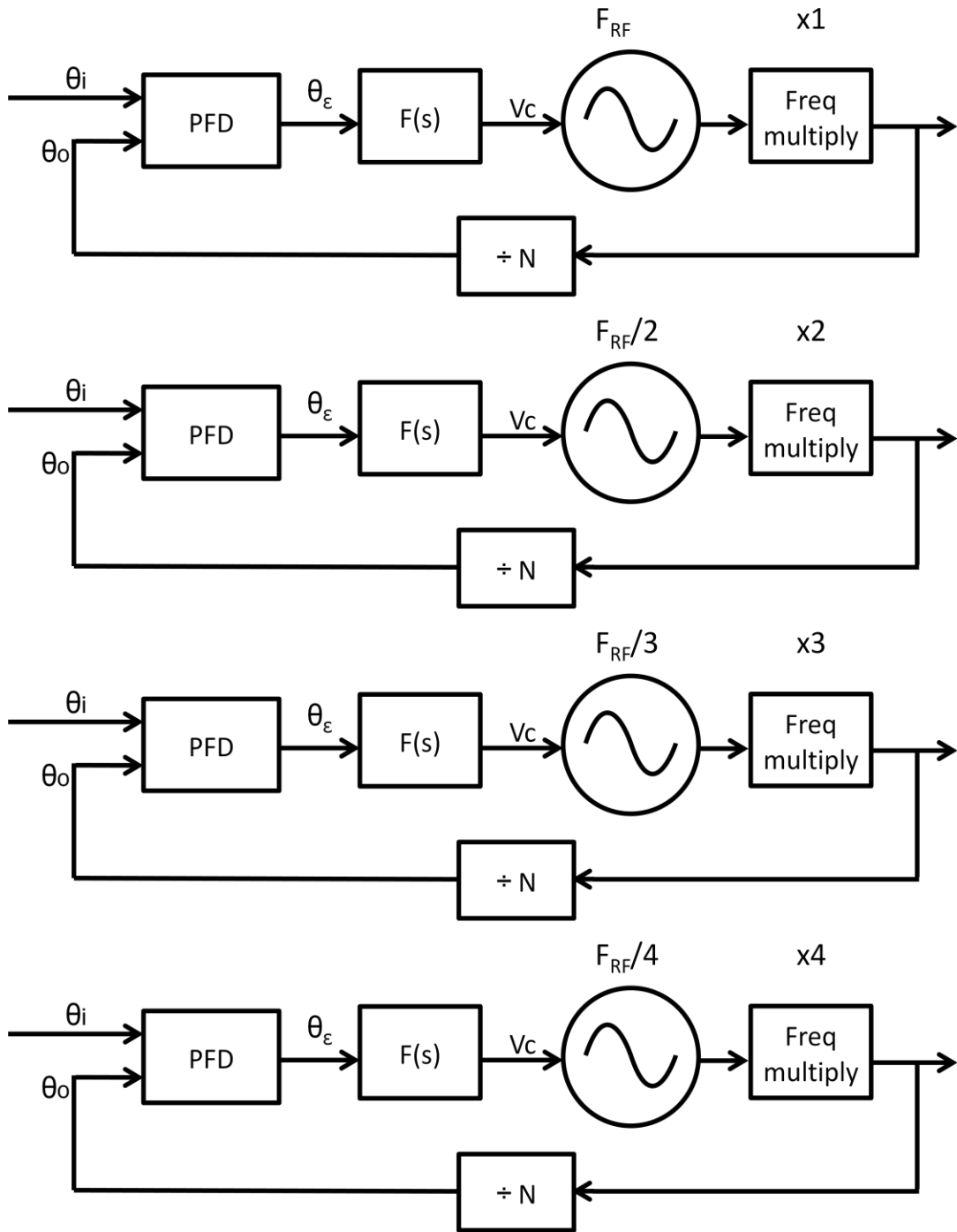


Figure 45: New PLL phased array architecture

Another more fundamental solution to overcome on-chip inductor coupling is to switch from LC VCOs to ring oscillators. With new development in the area of noise cancelling oscillators [34], the traditional phase noise limitation that restricts transmitters from using anything besides LC VCOs will be gone. This will not only solve the problem of inductor coupling, it can significantly reduce the area of a PLL. Such development can lead to very compact individual channel PLLs and thus large number of element arrays. With large number of elements, this PLL phased array architecture's high phase resolution can be fully utilized.

## **Appendix A**

### **A flexible wireless receiver with configurable DT filter embedded in a SAR ADC**

The following section discusses the other work [35] completed in collaboration with David Lin.

#### **A.1 Introduction**

The modern day desire for ubiquitous connectivity using multiple standards and bands necessitates the development of flexible, software-configurable receivers. One of the challenges of creating such receivers is the design of low power, configurable filters for rejecting aliasing interferers and adjacent channels. Analog filters become difficult to design at the reduced supply voltages of deep submicron processes. Digital filters require significant over-sampling with a high resolution ADC, at the expense of power consumption, in order to prevent aliasing of the interferer and to capture a weak wanted signal in the presence of a strong interferer.

This work presents a better alternative of embedding a software-configurable, discrete time (DT) filter within a SAR ADC. The DT filter attenuates interference by performing passive charge-sharing, so power consumption and speed improve with process scaling. Compared to receivers with a separate DT filter stage [36][37], the embedded filter reduces capacitor area and saves energy by eliminating charge

resampling between the filter and the ADC [38]. Configurability allows the receiver to adapt to its environment and to different communication standards. For example, the receiver can save power by operating in a “no filter” mode when no interferer or adjacent channel activity is present. As the power and the frequency of the interferer change, the receiver can respond by enabling the DT filter and optimally adjusting sampling rate and filter parameters. This 500MHz to 3.6GHz configurable receiver is verified with the 915MHz and 2450MHz bands of the IEEE 802.15.4 standard and the IEEE 802.11 standard.

## A.2 Receiver Architecture

The receiver consists of direct conversion I and Q channels with all the necessary components to receive an RF signal and output digital baseband signals, as shown in Figure 46. A wide-band LNA with matched inputs captures an RF signal and outputs a current signal to a switching mixer. The mixer switches are driven by a 2x LO divider. The down-converted signal is amplified by a chain of baseband amplifiers before filtering and digitization by a 7-bit SAR ADC with embedded, software-configurable DT filtering ("SARfilter ADC").

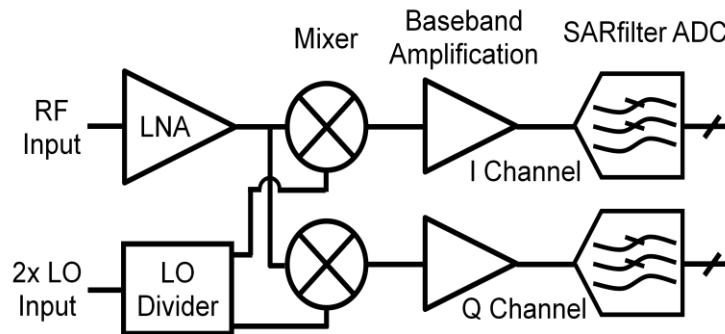


Figure 46: Block diagram of the SARfilter ADC receiver

Details of the LNA, mixer, and first stage of the baseband amplifier chain are shown in Figure 47. The differential LNA [39] achieves low-power and wideband operation by connecting two common-gate and two shunt feedback stages in parallel. The parallel combination reduces the total input resistance and power consumption by a factor of 4 compared to an individual common-gate or shunt feedback LNA, at the cost of coupling capacitor area. The output of the LNA is buffered and coupled to passive NMOS mixer switches that drive a transimpedance amplifier. No inductors are used, in order to support a wide range of carrier frequencies, to minimize circuit area, and to maintain compatibility with digital CMOS processes.

Self-mixing of the LO signal and process mismatch can induce a DC offset at baseband. While the use of a 2x LO mitigates the offset error, even a small error can still saturate the baseband amplifiers due to their significant gain. Therefore, binary-weighted current DACs source current from the feedback resistors of the transimpedance amplifier in order to cancel DC offset.

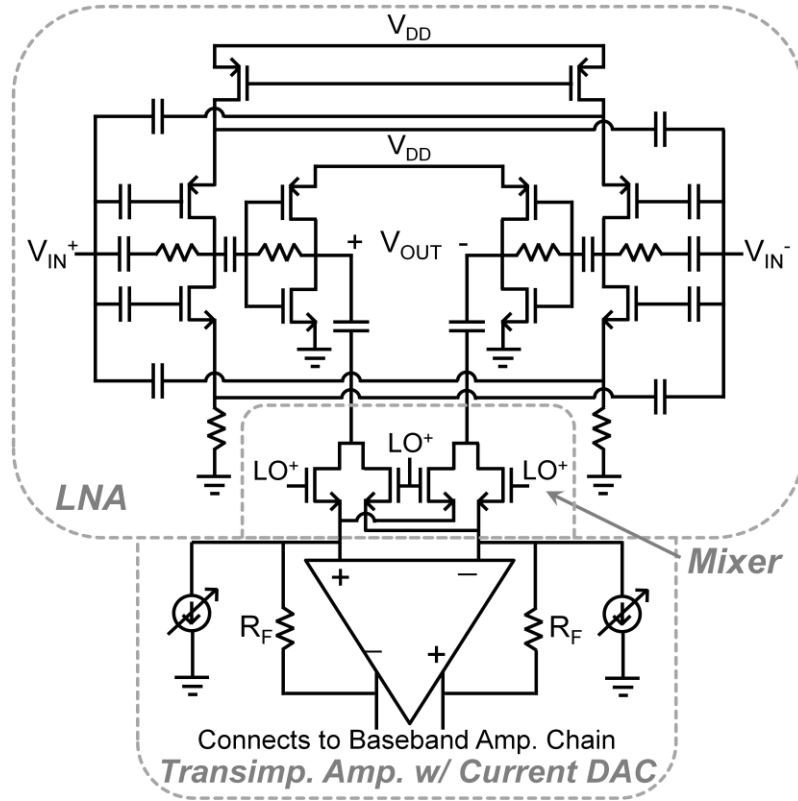


Figure 47: Simplified diagram of the LNA, mixer, and transimpedance amplifier with binary-weighted current DACs for DC offset correction

### A.3 SAR ADC with Embedded DT filter

The charge sharing DT FIR filter is embedded in the sampling process of a SAR ADC. The SAR ADC capacitors are arranged into groups that are proportional to the relative coefficient sizes of an FIR filter. For example, the implementation of a 4-tap filter with coefficients  $[.25 \ .25 \ .25 \ .25]$  requires 4 groups of capacitors, as shown in Figure 48, assuming this particular arrangement, the input voltage is sampled onto capacitor group 1, 2, 3 and 4 at time  $0$ ,  $\tau$ ,  $2\tau$  and  $3\tau$ , respectively. The timing diagram for the filtering and SAR conversion process described above is shown in Figure 49. After acquiring these four samples, all of the capacitor groups are charge shared, as shown in lower diagram of Figure 48. This averages the previously sampled

voltage levels and implements the FIR transfer function,  $H(z)=(z^{-1}+z^{-2}+z^{-3}+z^{-4})/4$ . The successive approximation operation that follows is identical to that of a SAR ADC without filtering, but produces filtered output code since it operates on a filtered input. Once the conversion process completes, the process described above repeats.

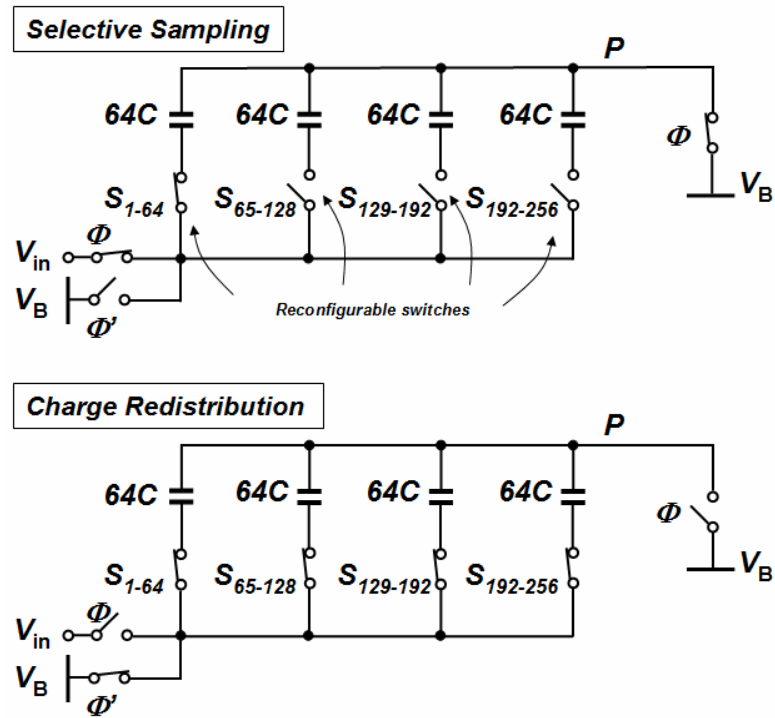


Figure 48: Principle of filtering with charge sharing sampling

The timing diagram in Figure 49 shows that multiple samples are collected during the sampling phase and no samples are collected during the conversion phase. Nonetheless, this non-uniform sampling results in the desired FIR filtering response. Exactly enough samples are collected during each sampling phase to generate a single filtered output sample, each of which is generated at the ADC conversion rate. Note that the IEEE 802.15.4 compatible filter implemented in this chip is much more complex than the example 4-tap filter, but the idea is the same.



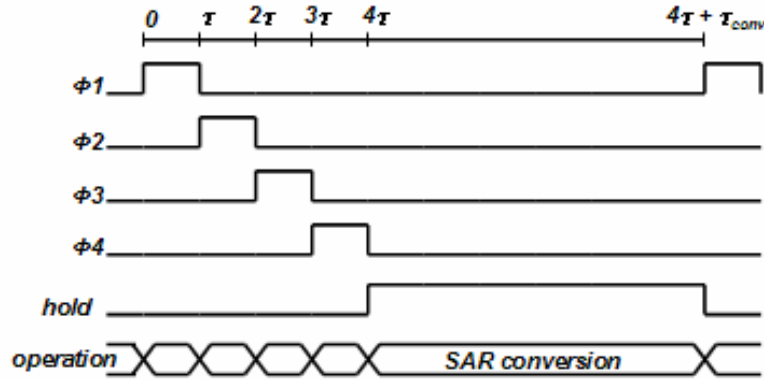


Figure 49: Timing diagram of embedded FIR filter and SAR ADC operation

#### A.4 Results

The design is implemented in a 1P9M 65nm process with MIM capacitors. The die photo is shown in Figure 50. The receiver supports RF frequencies ranging from 500MHz to 3.6GHz. Assuming minimal input loss from a matched RF source, which is reasonable given the measured S11 of less than -10.5dB, the gain from the RF input to the ADC input is approximately 60dB. The ADC conversion rate can be as high as 21.25MS/s with the 16-tap filter enabled, which corresponds to  $f_{s,filter}$  of 340MS/s. Power consumption is 3.98mW, 5.51mW, and 9.47mW for 802.15.4 915MHz and 2450MHz bands and 802.11, respectively.

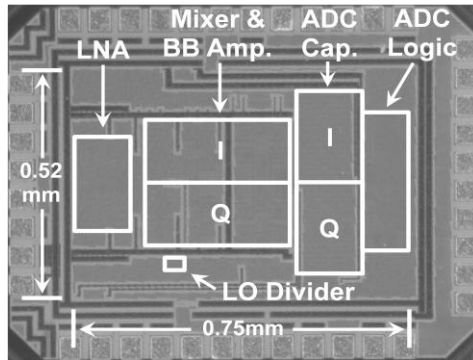


Figure 50: Die photo of the SAR filter prototype

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