Applications of Semiconductor Nanowires for Nanoelectronics and Nanoelectromechanical Systems

by

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Dedication

To my parents

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Table of Contents

Dedication ii

Acknowledgements.. iii

List of Figures ix

Chapter 1 Overview.. 1

Chapter 2 Growth of Si, Ge, and Ge/Si core/shell nanowires: toward CMOS integration..12

2.1: Introduction...12

2.2: Overview of the nanowire growth process 14

2.3: Growth and electrical properties of Al-catalyzed Si nanowires 16

2.3.1: Growth of small-diameter nanowires with high yield 18

2.3.2: Recovery of semiconductor behavior at small diameter 22

2.3.3: Possible mechanisms of carrier concentration reduction 26

2.4: Vertical integration of Ge nanowires on Si for high-performance nanoelectronics...29

2.4.1: Material system: Ge/Si core/shell nanowires 31

2.4.2: Vertical epitaxial growth of Ge nanowires on Si (111)..........35

2.4.3: Ge buffer layer for nanowire location control and high growth yield 39

2.4.4: Post-growth Au catalyst removal 42

2.5: Summary 43

Chapter 3 Toward Ge nanowire-based vertical tunnel field-effect transistors for hybrid nanowire-CMOS systems....44

3.1: Introduction....44

3.1.1: Subthreshold non-scaling in CMOS 44

3.1.2: The tunnel field-effect transistor....46

3.1.3: TFET using a vertical Ge NW grown on Si 48

3.1.4: Chapter overview....52

3.2: Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions..53

3.2.1: Vertical diode fabrication 54

3.2.2: High performance at room temperature....56

3.2.3: Temperature dependence indicates low-defect density....57

3.3: Prospects for ultrasharp vertical nanowire-based Si-Ge heterojunctions for tunnel field-effect transistor applications....62

3.3.1: Vertical growth of Ge nanowires on Si nanopillars for optimal vertical FET gate alignment 63

3.3.2: Sub-eutectic growth of vertical epitaxial Ge nanowires on Si for ultrasharp heterojunctions 65
3.4: Prospects for vertical junctionless field-effect transistors based on Ge/Si core/shell nanowires 67
3.4.1: Introduction to junctionless FET 68
3.4.2: Device proposal and preliminary electrical measurements 70
3.4.3: Fabrication developments 73
3.5: Summary 75
Chapter 4 Radio frequency nanowire resonators and *in situ* frequency tuning 76
4.1: Introduction 76
4.2: Device fabrication 80
4.3: Electrical actuation/detection setup 83
4.4: High Q achieved at room temperature and size scaling 84
4.5: Nonlinear operation 85
4.6: *In situ* frequency tuning 87
4.6.1: Discussion of tuning mechanisms 89
4.7: Selective actuation of different vibrational modes 91
4.8: Summary 92
Chapter 5 Conclusion 94
5.1: Nanowire growth techniques for hybrid nanowire-CMOS systems 94

5.2: Toward a Ge nanowire-based vertical tunnel FET 96

5.3: Nanowire-based NEMS 97

5.4: Final remark...98

References 100

List of Figures

FIG. 1 Example of semiconductor nanowires 2

FIG. 2 Trend in transistor geometry toward a gate-all-around structure 3

FIG. 3 Trend in power density in CMOS technology 4

FIG. 4 Technology scaling trends of power supply voltage V_{dd} 5

FIG. 5 Qualitative transfer characteristics of a conventional MOSFET 6

FIG. 6 Reported III-V, Si, and Ge room-temperature mobilities of electrons (red squares) and holes (blue circles) as a function of lattice constant 7

FIG. 7 Qualitative transfer characteristics comparing MOSFET (solid line) and TFET (dashed line) 8

FIG. 8 Example of a doubly clamped nanomechanical beam resonator 10

FIG. 9 Example binary alloy phase diagram illustrating the VLS process for nanowire growth 15

FIG. 10 19

(a) Schematic of the Al–Si binary phase diagram

(b) SEM image of Al-catalyzed Si nanowires

(c) Diameter distribution of Al-catalyzed Si NWs grown at 520 °C

(d) Same as (c) but with 75 Torr SiH_4 partial pressure

FIG. 11 23

(a) Transfer curve (I_{DS}-V_{GS}) at $V_{DS} = -0.1$ V for a device with diameter = 23 nm.

(b) Family of I_{DS}-V_{DS} curves for the same device in (a)

(c) Family of I_{DS}-V_{DS} curves for another device with diameter = 40 nm

(d) Family of I_{DS}-V_{DS} curves for another device with diameter = 80 nm

FIG. 12 25

(a) Measured carrier concentration (squares) vs nanowire diameter shown in semilog plot

(b) Measured field-effect mobility vs nanowire diameter

FIG. 13 and diagram and schematic showing the surface depletion region (dark annular region) due to trapped holes at the surface of a p-type nanowire 27

FIG. 14 Schematic comparing strain relaxation in a thin-film geometry vs. a nanowire geometry 30

(a) Strain relaxation in thin film showing a dislocation defect beyond the critical thickness

(b) Coherent radial strain relaxation in a nanowire

FIG. 15 Ge/S core/shell nanowire 32

(a) Schematic and band diagram showing the presence of a degenerate hole gas.

(b) HRTEM image of a nanowire showing a 10 nm Ge core and 2 nm Si shell.

FIG. 16 34

(a) Output curves for a laterally configured back-gated FET with a Ge/Si core/shell nanowire. with 20 nm core diameter and 1 μm channel length

(b) Transfer curves for a laterally configured back-gated FET with a Ge/Si core/shell nanowire with 20 nm core diameter and 1 μm channel length

(c) Output curves for a similar device with Ge 10 nm core diameter

(d) Transfer curves for a similar device with Ge 10 nm core diameter

FIG. 17 36

(a) SEM image of a vertical Ge nanowire (20 nm in diameter) epitaxially grown on a Si substrate

(b) Low magnification image of the epitaxial Ge NW growth.

FIG. 18 37

(a) SEM image showing kinking during nanowire nucleation

(b) SEM image showing tapered nanowires

FIG. 19 SEM image showing high yield vertical growth 41

FIG. 20 Au catalyst removed from vertical Ge nanowire....................................43

FIG. 21 45

(a-b) Band diagrams showing the operation of a conventional n-type FET in the (a) ON state and (b) OFF state.

(c-d) Corresponding band diagrams showing the operation of a n-type TFET

FIG. 22 49

(a) Schematic of a vertical TFET having an n+ Si source and a Ge nanowire channel

(b) The corresponding band diagram

FIG. 23 First order calculations of the proposed TFET saturation current (ON current) as a function of gate voltage 51

(a) Comparison with a Si-based TFET shows improvement in ON current when replacing the channel with smaller band gap material Ge

(b) With varying nanowire diameter

FIG. 24 56

(a) Schematic of the cross section of the completed vertical Esaki diode structure

(b) Equilibrium band diagram of the Si-Ge heterojunction

(c) Current-voltage characteristic of the selected device showing a PVR of 2.75 at room temperature

(d) Expanded semi-logarithmic plot of the voltage sweep shown in (c)

FIG. 25 Temperature dependence (down to 86K) of the current-voltage characteristics of the device shown in Fig. 24....................................58

(a) Forward bias

(b) Reverse bias

FIG. 26 Measured peak current I_p vs temperature 62

FIG. 27 64

(a) TFET gate is misaligned with the Ge/Si NW/substrate junction

(b) By first etching a Si nanopillar, the geometry allows optimal gate alignment for control of the tunnel junction

(c) SEM image of vertical Ge nanowires (diameter 30 nm) grown epitaxially on Si nanopillars

FIG. 28 66

(a) SEM image (taken at 45° viewing angle) of vertical Ge nanowires (20 nm in diameter) nucleated on Si (111) at 320 °C

(b) High resolution TEM image showing a sharp Ge/Si heterojunction at the interface of a Ge nanowire grown on a Si nanopillar at 320 °C

FIG. 29 Schematics comparing the operation of the conventional MOSFET and the junctionless FET..69

(a) Conventional MOSFET OFF state

(b)) Conventional MOSFET ON state

(c) Junctionless FET OFF state

(d)) Junctionless FET ON state

FIG. 30 71

(a) Device schematic of preliminary design of vertical junctionless FET

(b) Output curves of fabricated device showing high ON-current density

FIG. 31 Fabrication techniques for vertical FET structures 74

(a) Cylindrical Al gates around vertical nanowires (20 nm diameter) encapsulated in 25 nm Al_2O_3

(b) Controlled wet etching of Al_2O_3 using spin-on glass as an etch mask to expose a Si/Ge core/shell vertical nanowire for gate dielectric deposition

FIG. 32 Maximum reported Q factors in mechanical resonators varying in size from the macroscale to nanoscale 79

FIG. 33 HRTEM image of a SnO_2 nanowire showing a smooth surface................80

FIG. 34 Schematics of two configurations of doubly clamped nanowire resonator ..81

(a) Substrate is used as global back gate

(b) With local side gate

FIG. 35 82

(a) SEM image of a representative doubly clamped nanowire resonator

(b) Schematic of the double-source method

(c) Electrical readout from a typical device along with a Lorentzian fit

(d) Plot of f_0 vs geometry factor d/L^2 for nine devices

FIG. 36 Nonlinear response of a back-gated device.......................................86

(a) Family of response curves as the ac gate drive V_g^{ac} is increased from 60 to 350 mV_{pp}

(b) For V_g^{ac} = 350 mV_{pp} (top curve in (a)), a hysteretic response is observed depending on the direction of the frequency sweep

FIG. 37 *In situ* frequency tuning 88

(a) Resonant frequency f_0 of the in-plane motion vs varying dc bias on the back gate V_{back}, with V_{side} = 5 V

(b) f_0 of the in-plane motion vs V_{side} with V_{back} = 0 V

FIG. 38 Selective actuation of in-plane and out-of-plane modes 92

(a) Electrical readout of the device at bias configurations of V_{side} = 5 V and V_{back} = 0 V

(b) Electrical readout of the device at bias configurations of V_{side} = 0 V and V_{back} = 5 V

Chapter 1

Overview

Until the past few years, the tremendous success of complementary metal oxide semiconductor (CMOS) technology since its invention in the 1960s was the result of shrinking the size of transistors through the use of top-down lithographic techniques. Owing to the excellent natural interface between silicon and silicon dioxide, no major changes to the device design were needed, in spite of the existence of high mobility materials such as germanium and III-V compounds. However, this top-down paradigm of transistor size scaling is now being seriously challenged due to a number of practical and fundamental problems as the device size approaches the few-nanometer scale [1-3]. As the device size shrinks, the device characteristics become increasingly sensitive to dimensional variations. For example, simulations of a double-gate metal-oxide-semiconductor field-effect transistor (MOSFET) [3] predict that for a device with channel length 5 nm and channel thickness 2 nm, either a 0.2 nm variation in the length or a 0.1 nm variation in the thickness would result in a 50 mV shift in the threshold voltage. It is very difficult to control the device dimensions with such precision, and the increasing costs associated with lithography equipment and operating facilities needed for traditional manufacturing may create an economic barrier to continued scaling. Hence the bottom-up growth of functional

nanoscale materials, in which at least one critical device dimension (e.g. channel thickness) is defined via a chemical synthesis process with near-atomic-scale precision, may be an attractive alternative to traditional top-down techniques. Such materials, including molecules[4-8], graphene[9-13], carbon nanotubes[14-17], and semiconductor nanowires (NW) [18-20], have attracted much interest with the expectation that they may be able to complement or replace CMOS in the future.

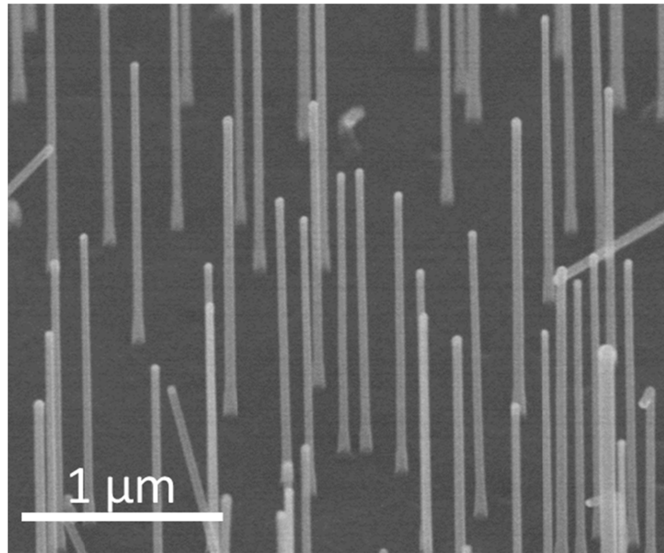

FIG. 1. Example of semiconductor nanowires. Shown here are vertical Ge nanowires epitaxially grown on Si.

In particular, semiconductor nanowires hold much technological promise. These are single-crystals with diameters of a few nanometers and lengths up to tens of micrometers, typically grown through a vapor-liquid-solid or a vapor-solid-solid process mediated by nanoparticles[18] (Fig. 1). They can be prepared with reproducible electronic properties in high yield. Recent developments in nanowire growth have led to the demonstration of a wide range of nanowire structures with

precise control of composition, morphology and electrical properties, including group IV[21, 22], III-V[23] and II-VI[24] core/shell[25], superlattice[26] and branched[27] nanowires. In addition, their crystalline structure and smooth surfaces help reduce scattering and typically result in better characteristics compared with nanofabricated samples of similar size. They are especially interesting in light of another trend in the semiconductor industry: in addition to size scaling, recently there has been a gradual transition from a planar device structure to a tri-gate structure, for increased gate coupling to the transistor channel (Fig. 2). For example, in 2012 Intel introduced a tri-gate structure into its high-volume production at the 22 nm node. Following this development, the next evolutionary step would be the introduction of a gate-all-around (GAA) structure, in which the channel is completely surrounded by the gate. The nanowire geometry is especially suited for the GAA structure.

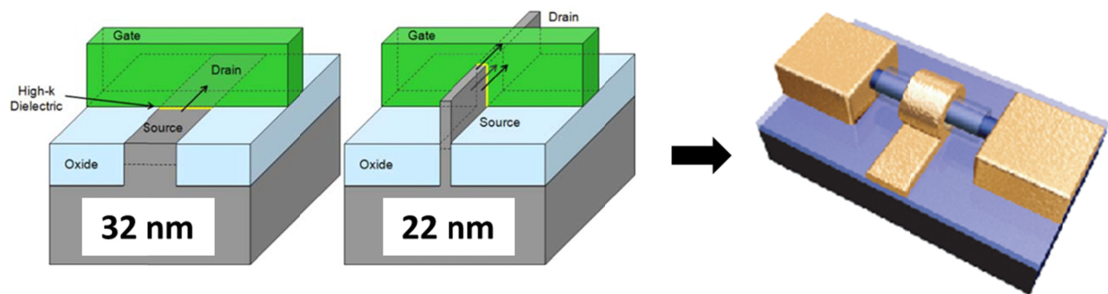

FIG. 2. Trend in transistor geometry toward a gate-all-around structure. Shown here are Intel's 32 nm planar geometry (2010) and Intel's 22 nm tri-gate geometry (2012).

This thesis explores the technological potential of semiconductor nanowires. To date, most efforts have focused on Si nanowires, since CMOS is based on silicon. One requirement for the integration of Si nanowires with CMOS is that the nanowire growth process should be CMOS-compatible. To this end, in Ch. 2.3 we explore Si nanowire growth using CMOS-compatible Al as catalyst (in particular we demonstrate small diameter nanowires that retain their semiconducting behavior).

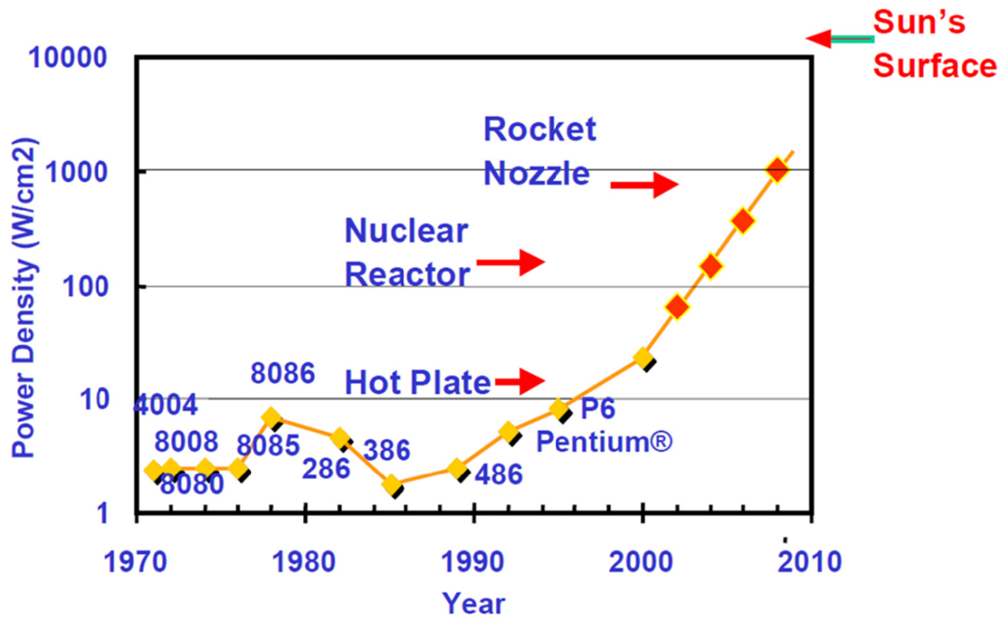

FIG. 3. Trend in power density in CMOS technology. Adapted from Ref.[28].

One fundamental challenge that CMOS technology faces today is power dissipation. As shown in Fig. 3, the power density has increased at a near-exponential rate toward the air-cooling limit of ~100 W/cm^2 [28]. Today's chips hover near this limit; for example, both of Intel's 32 nm and 22 nm microprocessors have a power density of ~40-50 W/cm^2. Power density cannot increase much further without incurring substantial packaging and cooling costs that are impractical for most

applications. From a device perspective, the situation may be elucidated by examining the trend in the power supply voltage V_{dd}, shown in Fig. 4. As this figure shows, the supply voltage V_{dd} has bottomed out at ~ 1 V starting from the 65 nm node. Dynamic power dissipation is roughly proportional to V_{dd}^2, while static power dissipation is proportional to V_{dd}, so it would be desirable to reduce V_{dd}. However, in a conventional MOSFET the ON current $I_{ON} \propto \mu\left(V_{dd} - V_T\right)^2$, where μ is the channel mobility and V_T is the threshold voltage, would also decrease, which would increase

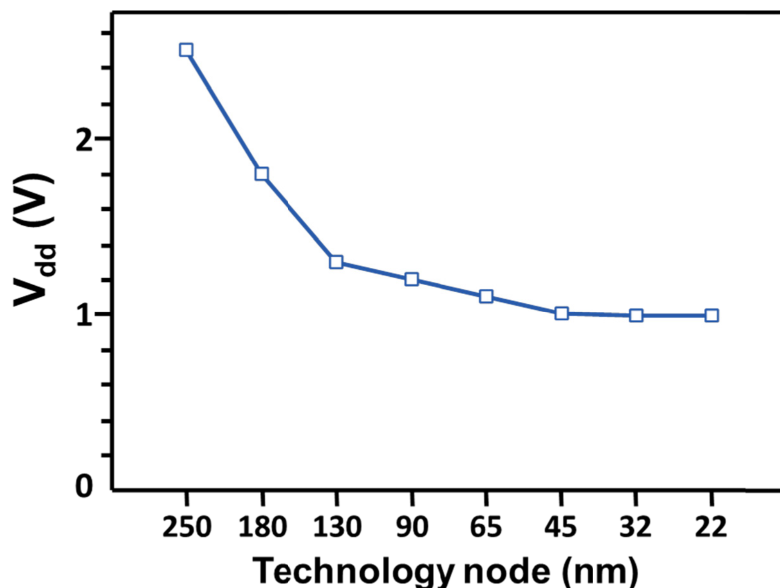

FIG. 4. Technology scaling trends of power supply voltage V_{dd}. Adapted from Ref. [29].

the gate delay and compromise switching speed. One could maintain high I_{ON} by reducing V_T, but this would result in an exponential increase in the OFF current I_{OFF}, which would increase static power dissipation. The exponential dependence of I_{OFF} on V_T is given by $I_{OFF} \propto \exp\left(-qV_T/kT\right) = 10^{-V_T/SS}$, where q is the electronic charge, k is

the Boltzmann constant, and T is the temperature. SS is a figure of merit (defined by the equation) called the subthreshold swing, and it measures the gate voltage swing needed to reduce the current by a factor of 10. Fig. 5 shows the relationship of I_{ON}, I_{OFF}, V_T, V_{dd}, and SS in a conventional MOSFET.

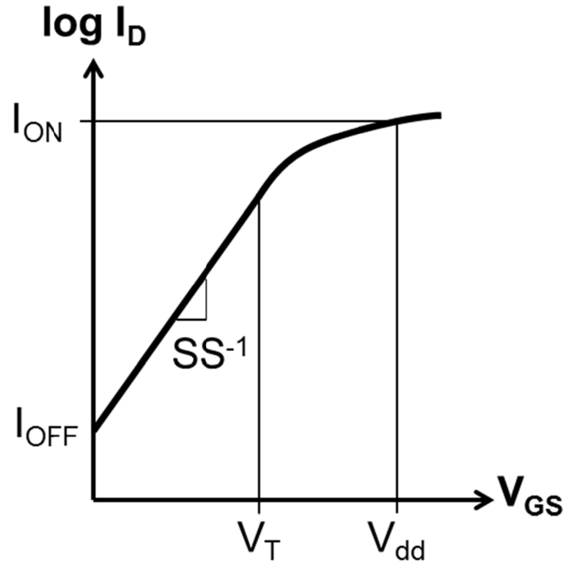

FIG. 5. Qualitative transfer characteristics of a conventional MOSFET.

This thesis touches on two ways to address the power dissipation problem. One possible solution is to maintain high I_{ON} by increasing μ, that is, by forming the transistor channel out of a high mobility material in which charge carriers travel at a much higher velocity than in silicon. This would allow a reduction in V_{dd} without a loss of performance. Rather than developing a completely new non-Si-based technology, however, it would be much more cost-effective to integrate the new materials on Si and complement traditional CMOS technology in an evolutionary manner. The ideal channel material should have equally high electron and hole

mobilities, since CMOS requires n-channel and p-channel FETs with reasonably matched performance. But Fig. 6 shows that at present no such material exists. While III-V compound semiconductors have very high electron mobilities, at any lattice constant there is a large gap between electron and hole mobilities [30].

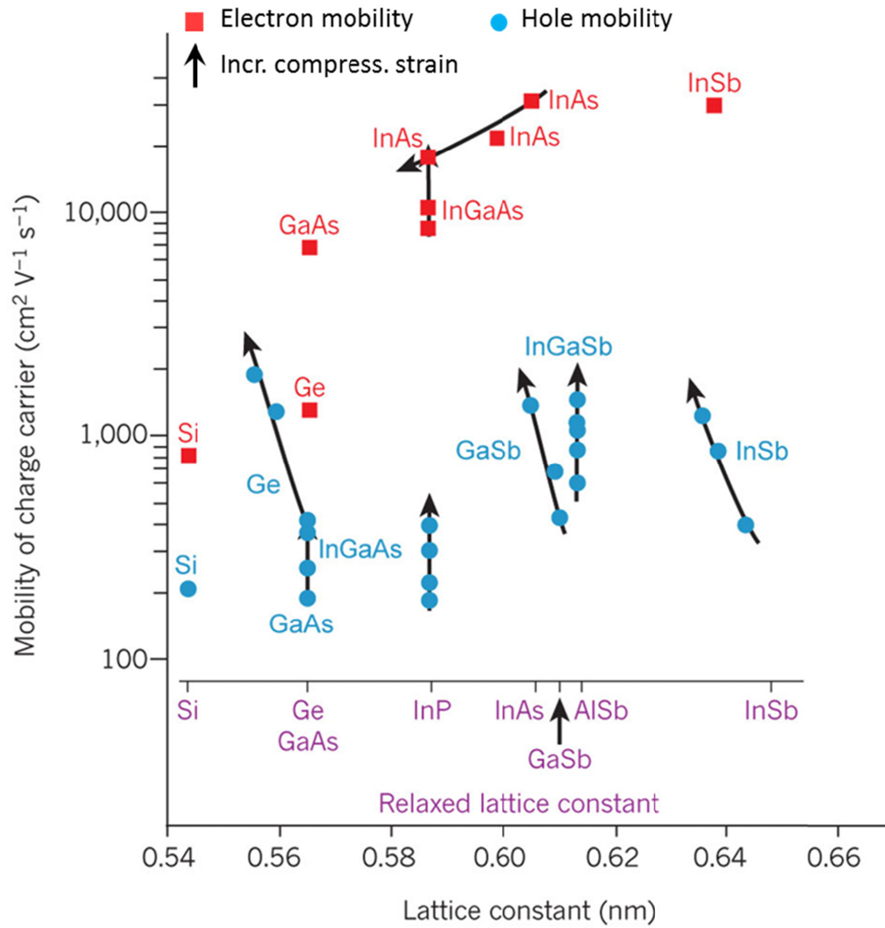

FIG. 6. Reported III-V, Si, and Ge room-temperature mobilities of electrons (red squares) and holes (blue circles) as a function of lattice constant, measured from inversion layers and quantum wells. Black arrows point toward increasing biaxial compressive strain. Relaxed lattice constants are shown on the scale. It is seen that Ge has a high hole mobility and a smaller Si-lattice mismatch than that of III-V materials. Adapted from Ref. [30].

Compressive biaxial strain (increasing along the black arrows in Fig. 6) plays a large role in bridging this gap, but it seems that, at the moment, the leading contender for the p-channel FET is Ge, which has a high hole mobility (even when compared with III-V materials), and whose technology is more mature than III-V technology. It also happens that Ge has a smaller lattice mismatch with Si than almost any III-V material, making the integration on a Si substrate a little easier. Still, the 4.2% lattice mismatch between Ge and Si poses a significant challenge for integration. To this end, the nanowire geometry may be able to relax strain coherently and allow the formation of low-defect Si-Ge interfaces. Hence in Ch. 2.4 we develop the vertical epitaxial growth of Ge nanowires on Si. Also, in Ch. 3 we investigate the prospects for vertical transistors using a vertical Ge nanowire as the channel (we focus on the tunnel FET and touch on the junctionless FET along the way).

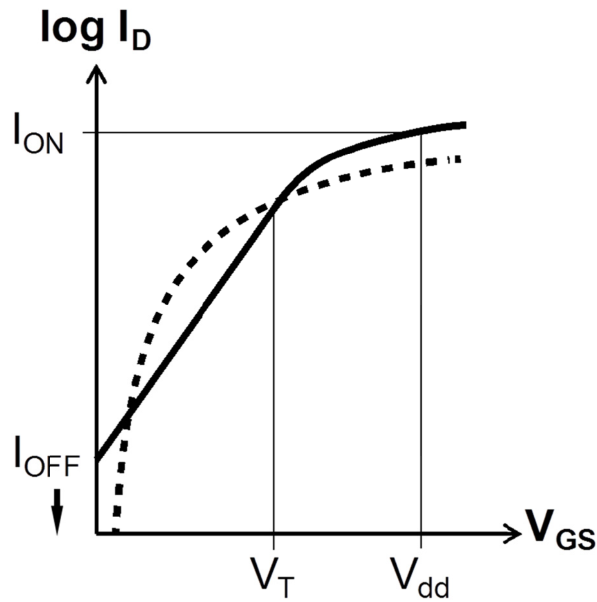

FIG. 7. Qualitative transfer characteristics comparing MOSFET (solid line) and TFET (dashed line). The TFET is capable of much lower OFF current.

Another route toward reducing power dissipation is to reduce I_{OFF}. In a conventional MOSFET, *SS* has an inherent thermodynamic lower bound of 60 mV/decade at room temperature. To this end, an alternative device concept, the tunnel field-effect transistor (TFET), has been proposed to circumvent this limit (Fig. 6). While the current conduction mechanism in a conventional MOSFET is thermionic emission over a potential barrier, a TFET uses quantum-mechanical band-to-band tunneling to bring charge carriers into the device channel. Thus in a TFET very low OFF currents are possible. This would allow a reduction of V_T (and hence a reduction in V_{dd}). However, Si-based TFETs suffer from low ON currents owing to its large band gap. Ge has a smaller band gap and thus may offer higher ON currents. To this end, in Ch. 3 we explore the use of vertical Ge nanowires grown on Si for the construction of a p-channel TFET. In addition, the nanowire geometry offers several attractive features when used as the channel of a TFET, including excellent gate coupling, scalability, and the coherent relaxation of strain for creating defect-free tunnel heterojunctions on Si.

While much effort in nanowire research is aimed at creating high performance electronic devices, the technological promise of semiconductor nanowires extends beyond their electronic properties: exploiting their mechanical degrees freedom will be a key to unlocking their full potential. Nanoelectromechanical systems (NEMS) is an emerging field in which nanoscale structures are mechanically manipulated with electrical actuation. In particular, nanoscale resonators have the potential for important applications in ultrasensitive mass and force sensing, and quantum measurement [31-38] (Fig. 8). Here nanowire-based mechanical resonators

potentially can obtain ultrahigh quality factors by suppressing acoustic energy losses intrinsic to a bulk crystal, minimize surface losses owing to their atomically smooth surfaces, and minimize losses due to bulk impurities and crystal defects owing to their small size and excellent material quality. To this end, in Ch. 4, we investigate a doubly clamped nanowire mechanical resonator.

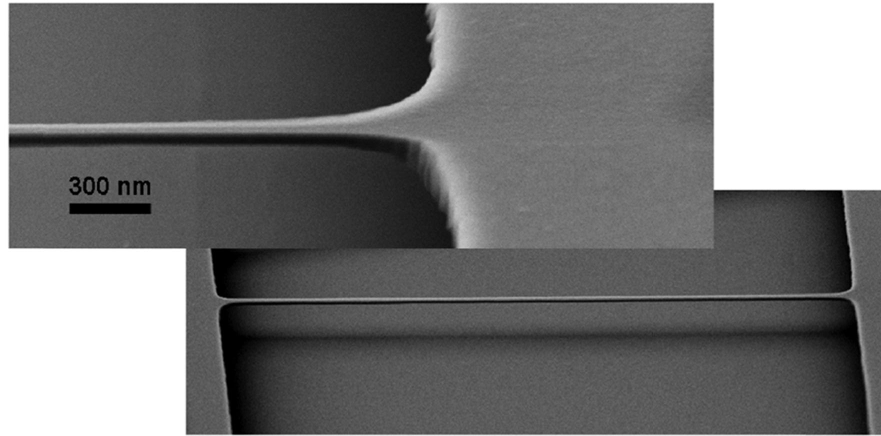

FIG. 8. Example of a doubly clamped nanomechanical beam resonator, made from silicon nitride. Adapted from Ref.[39].

To summarize the contents of this thesis, Chapter 2 focuses on nanowire CMOS-compatible growth techniques with an eye toward hybrid nanowire-CMOS systems. Chapter 3 examines the prospects for a Ge nanowire-based vertical tunnel field-effect transistor. We demonstrate high performance Esaki diodes constructed from Ge/Si core/shell nanowires and discuss the junctionless field-effect transistor concept. Chapter 4 demonstrates doubly clamped, Very-High Frequency (VHF) nanowire resonators with a dual-gate configuration that allows integrated electrical actuation/detection, *in situ* frequency tuning and selective actuation of different

vibrational modes. Finally in Chapter 5, we make some concluding remarks and discuss the future work to be done.

Chapter 2

Growth of Si, Ge, and Ge/Si core/shell nanowires: toward CMOS integration

2.1: Introduction

Over the last five decades, reducing the size of complementary metal–oxide–semiconductor (CMOS) field-effect transistors (FETs) has enabled extraordinary improvements in the switching speed, density, functionality and cost of microprocessors. But now, due to this aggressive device scaling, CMOS technology faces serious challenges[1-3]. As discussed in Ch. 1, semiconductor nanowires can help address some of these challenges. They can enable control of channel thicknesses with near-atomic-scale precision, and the nanowire geometry is ideally suited for the gate-all-around structure toward which the semiconductor industry is moving. Since nanowires are grown from the bottom-up, they represent a radical break from traditional top-down manufacturing methods. The traditional technology, which is implemented in semiconductor fabrication plants and developed over decades and billions of dollars, is quite mature and it would not make economic sense to replace it with entirely new technology. Instead, semiconductor nanowires can be used for

special high performance devices to complement traditional devices on the same chip.

Realizing such a hybrid nanowire-CMOS system would require careful consideration of whether the nanowire growth process could disturb the properties of the CMOS devices. When considering the CMOS-compatibility of the growth process, it is useful to look at two components: thermal budget and materials. The thermal budget used for fabricating nanowire-based devices depends on whether metal diffusion is a concern. For example, if the nanowire growth occurs during the back-end-of-line (BEOL) portion of the fabrication process, which begins with the first metal interconnect layer, then the thermal budget would be highly constrained. To prevent metal diffusion, a general rule of thumb is that the process temperature should not exceed ~450 °C [40], although the time t spent at the process temperature also influences diffusion (with a diffusion length evolving roughly as $\sqrt{Dt}$, where D is the diffusion coefficient whose temperature dependence follows a thermally activated Arrhenius equation). On the other hand, if the nanowires are grown during the front-end-of-line (FEOL) portion of fabrication, and prior to gate metal deposition, much higher growth temperatures could be tolerated.

Material compatibility means that any new materials introduced into the process should not contaminate the existing CMOS devices. Throughout most of the history of CMOS, there had been only a handful of CMOS-compatible materials: Si and its oxides and nitrides, dopants, and Al-based metals. Recently, there has been a trend in the industry to introduce more materials: SiGe, Cu-based metals, high-k dielectrics (e.g. HfO_2, ZrO_2), and low-k dielectrics (e.g. carbon-doped oxide). The

list is expanding (e.g. high mobility III-V materials are being considered). In any effort to introduce a new material, it is important to consider whether the material could be a contamination risk, and if so, whether the process can be designed to mitigate the risk.

In this chapter, we explore nanowire growth strategies that aim toward CMOS integration and strive to remain CMOS-compatible. To this end, after some additional background in Ch. 2.2, in Ch. 2.3 we discuss our progress in Si nanowire growth, by replacing the Au catalyst with Al, which is CMOS-compatible. In Ch. 2.4, we discuss progress toward the vertical integration of Ge, a technologically important material, on a Si substrate (which is envisioned to contain CMOS devices in the future), while maintaining a low thermal budget.

2.2: Overview of the nanowire growth process

Semiconductor nanowires are generally synthesized by employing metal nanoclusters as catalysts via a vapor-liquid-solid (VLS) or a vapor-solid-solid (VSS) process, the former being more widely used than the latter. We now illustrate the VLS process using as an example the growth of a Ge nanowire with a Au nanoparticle as the catalyst (the main process used in Ch. 2.4 and Ch. 3; the Al-Si system discussed in the Ch. 2.3 behaves similarly - see Fig. 10(a)). Fig. 9 depicts the binary alloy phase diagram for the Au-Ge system. The process begins with a metal nanoparticle (Au) in the presence of a vapor phase containing the semiconductor

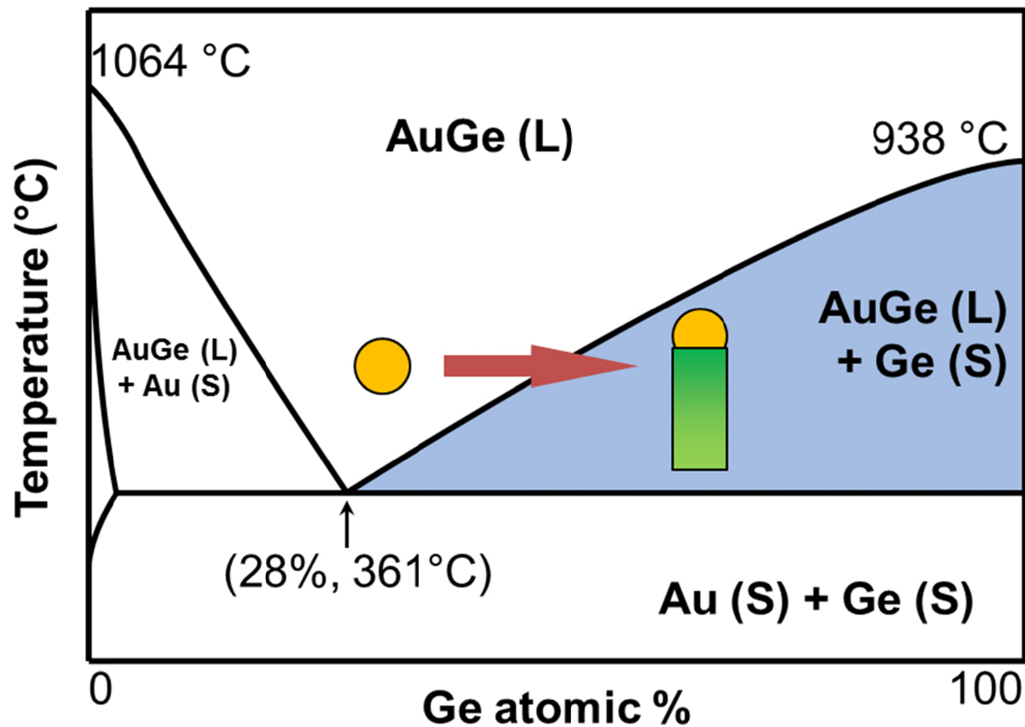

FIG. 9. Example binary alloy phase diagram illustrating the VLS process for nanowire growth. Here the Au-Ge system for the growth of Ge nanowires using Au as the catalyst. The eutectic point is located at 28 % Ge content and 361 °C.

material (GeH_4). As the temperature is increased, the metal nanoparticle helps catalyze the decomposition of the vapor phase material, releasing the semiconductor material (Ge). The metal nanoparticle acts as a sink for this material, and an alloy of the metal and semiconductor material is formed (AuGe). The alloy melts (the liquid L region in Fig. 9), which speeds up further incorporation of semiconductor material into the alloy droplet (due to increased diffusion coefficient). The minimum temperature at which melting is possible is called the eutectic temperature (361 °C for AuGe); hence the temperature should be increased to a user-defined nucleation

temperature above this value. Eventually the alloy becomes supersaturated with the semiconductor material (shaded region in Fig. 6), at which point a crystalline semiconductor phase (c-Ge) precipitates out of the alloy. This latter phase constitutes the growing nanowire; nanowire nucleation has occurred. The continued precipitation of the solid semiconductor at the solid-liquid interface leads to nanowire elongation, with the alloy droplet riding on top. In the VSS process, this sequence of events is similar except that the metal nanocluster remains in the solid state. In this case, the diffusion of semiconductor material through the nanocluster is much slower[41].

The nanowires used in Chapter 4 (nanoelectromechanical devices) are crystalline metal oxide (SnO_2) nanowires. These are grown using a vapor-phase, metal-catalyzed process, very similar to VLS. First, vapor phase Sn is generated from heating a Sn source metal. Then the vapor condenses at a Au nanocluster, and from the nanocluster a SnO_2 nanowire is nucleated. However, the exact mechanism of metal oxide nanowire growth is still under debate in the literature. Since Chapter 4 focuses on the nanoelectromechanical device properties rather than potential CMOS integration, for further details we refer the reader to Chapter 2 of Ref. [42].

2.3: Growth and electrical properties of Al-catalyzed Si nanowires

One requirement for the integration of nanowires with CMOS is that the nanowire growth process should be CMOS-compatible. In this section we address one of the CMOS integration issues, namely, the material contamination risk posed by the catalyst material used in the nanowire growth process. Currently the most

widely used catalyst material is Au. For example, the SnO_2 and Ge nanowires we use in Ch. 2.4, Ch. 3, and Ch. 4 are grown using Au as the catalyst. Furthermore, Au is often the catalyst for the growth of Si nanowires[43, 44], which have been widely studied due to the fact that CMOS technology is based on silicon. However, Au forms deep trap levels inside the Si band gap, and poses a potential contamination problem for processing. This is particularly an issue for hybrid nanowire-CMOS systems. Even though several studies have found that the influence of Au residing in the nanowire bulk is negligible [45-47], alternative catalyst materials may still be preferred. To date, Fe and Cu were reported as catalysts for Si nanowire growth with limited success [48, 49]. Ni as a catalyst[50] was also studied. However, due to the high eutectic temperature (964 °C) of Ni–Si alloy, a high synthesis temperature was required. Recently Al-catalyzed Si nanowire growth has attracted significant interest[51, 52]. However, the growth of Si nanowires using Al catalysts has been shown to be difficult due to the fact that Al readily reacts with ambient O_2 and H_2O, thereby forming a surface oxide layer that prevents the continued influx of Si reactants into the catalyst[51]. In addition, Al is a shallow acceptor in Si and is therefore expected to yield p-type Si nanowires[53]. Previous studies have thus far resulted in large-diameter Si nanowires that behave as degenerately Al-doped semiconductors with minimal gate response, making them unsuitable in electronics applications[52].

In this study we demonstrate Al-catalyzed, small diameter Si nanowires grown via the VLS process, and discuss their electrical properties. Specifically, by using high H_2 and SiH_4 partial pressures we were able to minimize the Al oxidation effect and

successfully grew large quantities of small diameter Si nanowires with high growth rate, minimal tapering, and high aspect ratio. In addition, we observed that the effective doping level is diameter-dependent, and small diameter ($d < \sim 25$ nm) Al-catalyzed nanowires behaved as p-type semiconductors with good gate response, while larger diameter Al-catalyzed nanowires behaved as degenerately doped semiconductors due to excessive Al-doping.

2.3.1: Growth of small-diameter nanowires with high yield

Fig. 10(a) shows the Al–Si binary phase diagram employed in the VLS nanowire growth process[54]. The substrates used for nanowire growth consisted of (111) N-type Si wafers with a resistivity of 0.001–0.002 Ω-cm. The substrates were first cleaned in 1:1 H_2SO_4:H_2O_2 to remove organic surface contamination for 20 min, and then dipped in 1 M HF for another 20 min to remove the native oxide and create a hydrogen-terminated Si surface. The subsequent de-ionized water rinse was minimized to retain as much of the hydrogen-termination as possible. The substrates were immediately transferred into the evaporator chamber to deposit 6 nm Al seed layer followed by the growth of Si nanowires in a low-pressure chemical vapor deposition (CVD) system. Once the Al-coated Si substrates were loaded into the CVD system, they were annealed at 590 °C for 5 min under 100 Torr H_2. The annealing, performed at a temperature above the Al/Si eutectic temperature of 577 °C, was intended to facilitate the Al film agglomeration on the surface and the formation of liquid eutectic droplets with the Si substrate. In particular, the hydrogen-rich environment during annealing was found to be effective to remove

existing aluminum oxide on the Al surface[52, 55]. For example, we observed identical results when comparing growth from fresh Al-coated Si substrates with those that have been stored in air for up to 48 h prior to growth, showing the effectiveness of hydrogen annealing to mitigate the effect of aluminum oxide. After

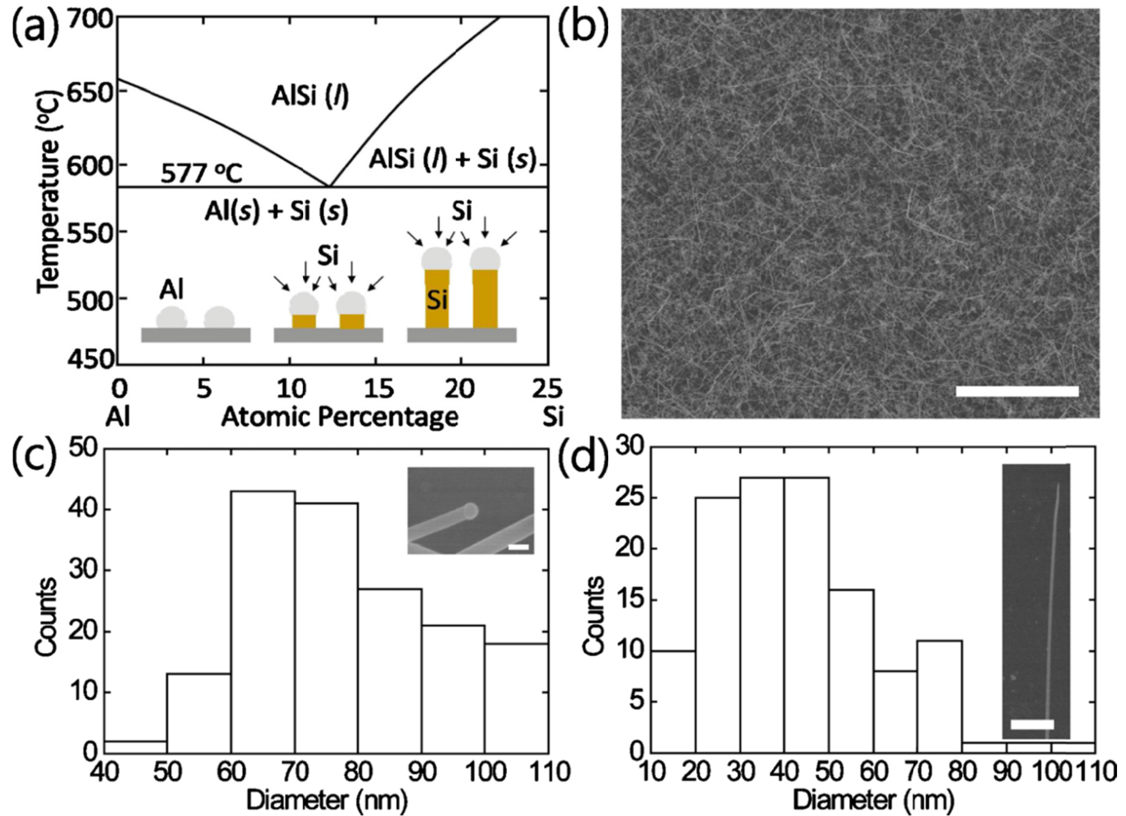

FIG. 10. (a) Schematic of the Al–Si binary phase diagram. Inset: schematic of VLS growth of Si nanowires. (b) SEM image of Al-catalyzed Si nanowires. Scale bar: 25 μm. (c) Diameter distribution of Al-catalyzed Si NWs grown at 520 °C, 100 Torr reactor pressure, and 50 Torr SiH_4 partial pressure. Inset: SEM image showing Al catalyst at the tip of nanowires. Scale bar: 100 nm. (d) Same as (c) but with 75 Torr SiH_4 partial pressure. Inset: SEM image of a single Si nanowire. Scale bar: 500 nm.

annealing, Si nanowires were grown at 520 °C for 30 s in the same system. The SiH_4 partial pressure during growth ranged from 50 to 75 Torr, and the total reactor pressure was kept at 100 Torr balanced by H_2. The H-rich environment during growth in turn helps prevent aluminum oxide poisoning and results in long, Al-catalyzed Si nanowires.

Fig. 10(b) shows a scanning electron microscopy (SEM) image of typical Si nanowires grown on the Al-coated Si substrate at 520 °C. Higher magnification SEM image of the tip region of the nanowires shown in Fig. 10(c) inset verified the presence of metal nanoparticle at the tip of the nanowires. High density Si nanowires with large aspect ratio were obtained with minimal tapering. Compared with earlier studies, the reduced tapering is believed to be due in part to the high nanowire growth rate (> 5 μm/min), which reduced the time available for vapor-solid deposition to occur[52]. Furthermore, the high growth rate suggests that the Al catalyst remains in the liquid state during the growth, even though the growth temperature is below the bulk eutectic temperature. Similar effects have been observed in the growth of Au-catalyzed Ge nanowires and can be explained by supercooling of the eutectic[56], and lowering of the eutectic temperature in the nanoparticle form[57]. Depending on the SiH_4 partial pressure, the as-grown Si nanowires have diameters in the range of 20–100 nm and exhibit a unimodal diameter distribution with peak range at 60–70 nm and 30–50 nm for SiH_4 partial pressures of 50 and 75 Torr during growth, respectively [Figs. 2.3.1(c) and (d)]. In general, we observed that higher SiH_4 partial pressure resulted in smaller diameter nanowires, consistent with previous studies on Au-catalyzed nanowires[43, 58].

Notably, we were able to obtain long Al-catalyzed nanowires with diameters down to 20 nm, much smaller than previously reported[51, 52]. The effect of the SiH_4 partial pressure is to adjust the thermodynamic conditions for nanowire growth. Growth proceeds by thermodynamically driving the transition from the vapor phase (SiH_4) to the nanowire phase, which is a combination of bulk solid phase and the formation of surfaces. The transition occurs because there is a net decrease in the effective chemical potential. However, when the nanowire is made thinner, the effective chemical potential of the nanowire phase can increase due to the increased surface area-to-volume ratio which is more dominated by surface free energy. This increased chemical potential makes the nanowire phase less favorable since during the phase transition the reduction of chemical potential is less pronounced. To restore the difference in chemical potentials between the two phases, the chemical potential of the vapor phase should also increase, which is accomplished by increasing the partial pressure.

Si nanowire growth with a 10 nm Al seed layer was also tested, resulting in an increase in average nanowire diameter up to 100–120 nm. This result matched well with the recent studies by Wacaser et al.[51] showing that the average diameter increased with the Al seed layer. The finding was attributed to the AlSi alloy droplet formation during the hydrogen annealing, where thicker films agglomerated into larger droplets.

2.3.2: Recovery of semiconductor behavior at small diameter

After growth, the nanowires were transferred to an isopropyl alcohol solution through sonication and drop-casted to a SiO_2/Si substrate (p-type, 0.001–0.005 Ω-cm with a 50 nm thermal SiO_2 layer), and a number of device structures were fabricated and tested. Briefly, photolithography was used to define pairs of source/drain (S/D) electrodes to contact each nanowire, followed by 3 s buffered oxide etch (10:1) dip to remove the native oxide on the nanowire surface immediately before the samples was loaded into the evaporator chamber to deposit 100 nm thick Ni electrodes. Contact annealing at 320 °C for 2 min in forming gas (N_2/H_2, 90/10%) completes the final device structure, with the p+ Si substrate serving as the back gate [Fig. 11(a), upper right inset]. All devices reported here contain only a single nanowire bridging the S/D contacts, with the electrical measurements carried out in air at room temperature. Fig. 11(a), lower left inset, shows a SEM image of such a device. Gate dependent current-voltage measurements indicate that the as-grown wires are p-type, and suggest that Al is incorporated into the Si nanowires [Fig. 11(a)]. Figs. 11(b), (c) and (d) show the family of I_{DS}-V_{DS} curves for representative devices with nanowire diameter d = 23, 40, and 80 nm, respectively. Significantly, the Si nanowire device with d = 23 nm shows typical p-type semiconductor characteristics and can be turned off within a V_{GS} bias window of 10 V. However, the Si nanowire device with d = 40 nm shows reduced gate response, and cannot be turned off. Finally, Si nanowire device with d = 80 nm

completely loses its gate control, suggesting that the larger diameter nanowire is degenerately doped.

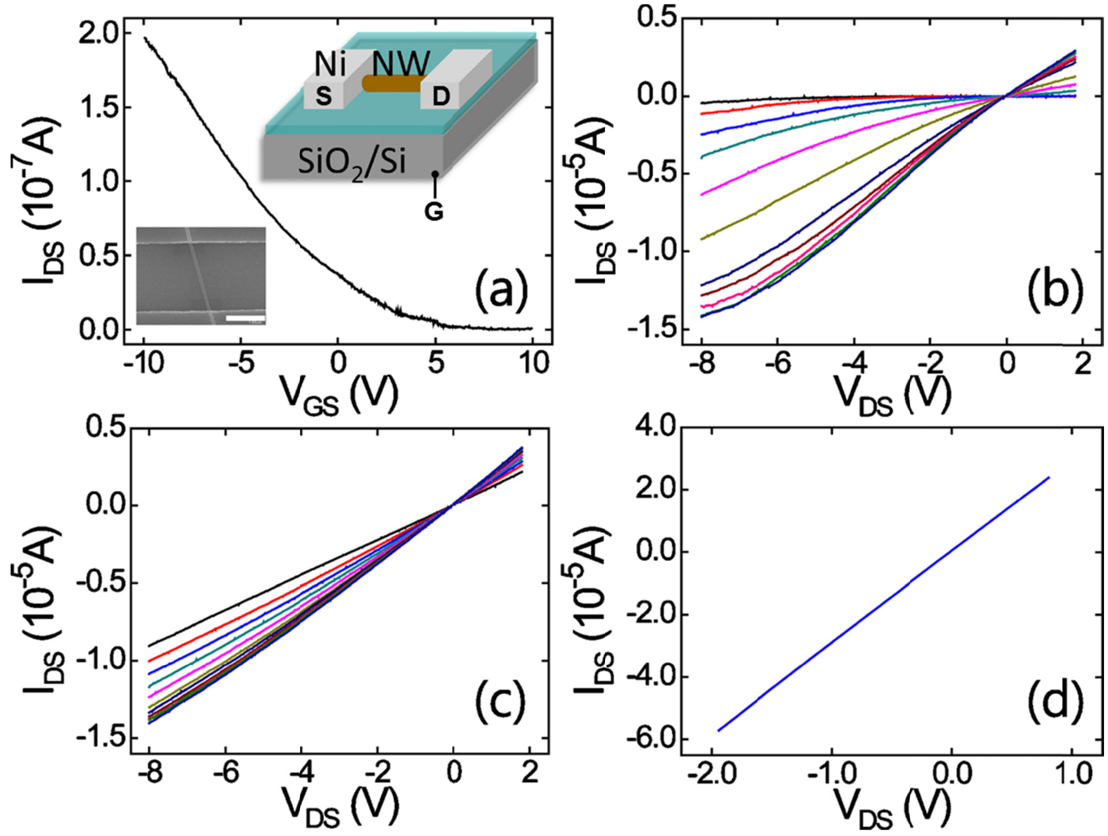

FIG. 11. (a) Transfer curve (I_{DS}-V_{GS}) at $V_{\mathrm{DS}} = -0.1$ V for a device with diameter = 23 nm. Upper right inset: schematic of the device. Lower left inset: SEM image of a similar device. Scale bar: 1 μm. (b) Family of I_{DS}-V_{DS} curves for the same device in (a). V_{GS} = 10 to −10 in −2 V steps. (c) Family of I_{DS}-V_{DS} curves for another device with diameter = 40 nm. V_{GS} = 10 to −10 in −2 V steps. (d) Family of I_{DS}-V_{DS} curves for another device with diameter = 80 nm. V_{GS} = 10 to −10 in −10 V steps.

The carrier concentration can be calculated by extracting the threshold voltage V_T from the transfer curve measured in the linear ($V_{DS} = -0.1$ V) region. The carrier concentration N (at $V_{GS} = 0$ V) was then calculated from $N = C_g\left(0 - V_T\right)$, where C_g is the capacitance of the back gate and can be estimated from the cylinder-on-plane model, $C_g = 2\pi\varepsilon_r\varepsilon_0 L \big/ \cosh^{-1}\left[\left(2h+d\right)/d\right]$, where ε_0 is the vacuum dielectric constant, $h = 50$ nm is the thickness of the SiO_2 layer, and d is the lateral size of the nanowire. ε_r is the relative dielectric constant and was chosen to be 2.5, which is the average of air (1) and SiO2 (3.9)[59]. Over 70 devices have been measured. However, for devices having nanowire diameters > 70 nm the carrier concentration cannot be reliably extracted due to the lack of gate response. Fig. 12(a) plots the carrier concentration versus the nanowires diameter obtained from 43 devices with nanowire diameter < 70 nm. Overall the carrier concentration remains high due to Al doping and a large spread of data was observed for large diameter devices due to the weak gate dependence and the associated uncertainties in extrapolating the carrier concentration data. However, linear fit [red line, Fig. 12(a)] to the data shows an overall gradual reduction of the effective doping level as the nanowire diameter is reduced. Furthermore, a substantial reduction of the carrier concentration was observed for nanowires with diameter < 25 nm, consistent with results from Figs. 11(a) and (b) and suggesting that nanowires with small diameters show semiconductor characteristics. The field-effect mobility μ_{fe} of the devices versus diameter was plotted in Fig. 12(b) for comparison. Here the mobility μ_{fe} was estimated using the equation, $g_m = \mu_{fe} C_g V_{ds} \big/ L^2$ in the linear operation regime. Here,

$g_m = dI_{DS}/dV_{GS}$ is the linear-region transconductance, and L is the nanowire device channel length. Overall, the mobility remains roughly constant independent of the nanowire diameter.

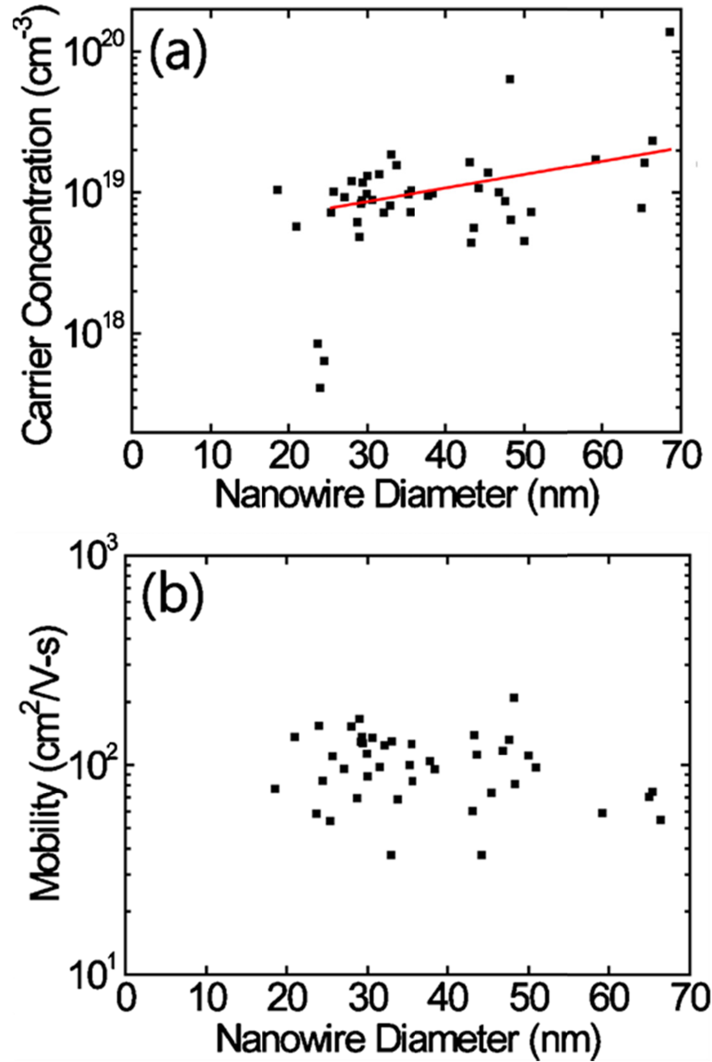

FIG. 12. (a) Measured carrier concentration (squares) vs nanowire diameter shown in semilog plot. The red line is a linear fit for data obtained from nanowires with diameter $d > 25$ nm. (b) Measured field-effect mobility vs nanowire diameter.

2.3.3: Possible mechanisms of carrier concentration reduction

Several factors may have contributed to the observed reduction of carrier concentration at small nanowire diameters. One possibility is due to quantum confinement and the amphoteric defect model (ADM) that governs doping limits in both bulk and nanoscale semiconductors [60]. Quantum confinement shifts the valence band edge downward from its bulk value in the case of p-type doping (or the conduction band edge upward in the case of n-type doping). Meanwhile, ADM sets a limit to the attainable Fermi level. Consequently, the maximum achievable carrier concentration is suppressed with diameter reduction. However, this effect is expected to occur only for diameters < 10 nm [60, 61]. The most plausible explanations for the observed reduction in carrier concentration are surface depletion, nanoscale dielectric confinement, and/or surface segregation of dopants. These are described next.

2.3.3.1: Surface depletion of charge carriers

One possible explanation is based on surface depletion[62]. For a p-type nanowire, trapped holes at surface states lead to a positive surface charge, which creates a depletion region at the surface (dark annular region in Fig. 13). This depletion region reduces the effective conducting cross-sectional area (light circular region), and hence reduces the effective carrier concentration. As the nanowire diameter decreases, the depletion region occupies a greater portion of the cross-sectional area. In the limiting, very small diameter case, the nanowire can become fully depleted and current can no longer flow.

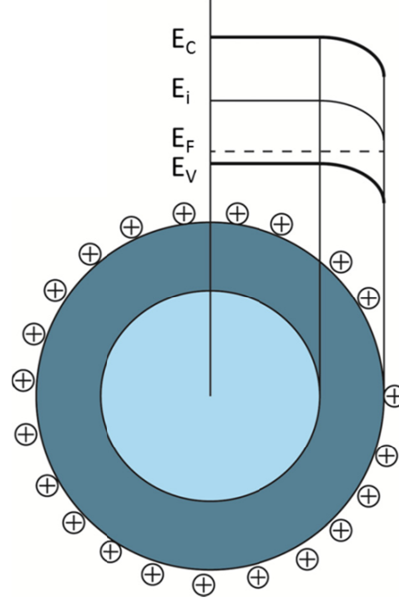

FIG. 13. Band diagram and schematic showing the surface depletion region (dark annular region) due to trapped holes at the surface of a p-type nanowire.

2.3.3.2: Reduced dielectric screening of the impurity potential

The second possible explanation is the dielectric confinement model[63, 64]. A donor or acceptor impurity has a Coulomb potential that give rise to bound states in the energy gap. In a bulk semiconductor, the Coulomb potential is strongly screened (dielectric constant $\varepsilon_r \sim$ 10-20) which leads to a large Bohr radius (~1-5 nm) and a correspondingly small ionization energy (few hundredths of an electron volt); impurities in a bulk material are ionized at room temperature. In this case, the ionization energy E_d can be estimated [65] using the Bohr model of the atom as $E_d = 13.6\left(m^*_{cond}/m_0\right)/\varepsilon_r^2$ [eV], where m_0 is the electron rest mass and m^*_{cond} is the effective conductivity mass. In a semiconductor nanowire, however, the close proximity of the impurity atoms to the lower dielectric constant of the environment

(which is air in our measurements, $\varepsilon_r \sim 1$) reduces the dielectric screening effect and increases the ionization energy. Therefore the activated doping level and free carrier concentration is reduced in small diameter nanowires.

2.3.3.3: Surface segregation of dopants

A third possible explanation is the surface segregation of dopant atoms [66, 67]. As the surface area-to-volume ratio of a nanowire increases, a greater portion of its atoms reside at the surface; these may undergo surface reconstruction since the inter-atomic forces are altered due to terminating the bulk crystal. From *ab initio* simulations it turns out that dopant atoms play a role in the reconstruction such that it is energetically favorable for them to reside at the surface. It has been shown that when the nanowire diameter is small ($d < 23$ nm in Ref. [66]) all dopants can be accommodated at the reconstructed surface with an intrinsic core. Once this occurs, the surface depletion (Ch. 2.3.3.1) and dielectric confinement (Ch,. 2.3.3.2) mechanisms can take effect, reducing the effective carrier concentration. As the surface-to-volume ratio decreases in larger diameter nanowires, the dopants cannot be fully accommodated at the surface and there is a transition back to bulk-doped material.

2.3.3.4: Summarizing remark

It is not clear at this moment which of the above three factors is dominating in our devices, but it is reasonable to suspect that all three factors should have an influence on the observed device behaviors such as the gradual reduction of effective doping level for large diameter nanowires and a sharp roll-off for small diameter ($d <$ 25 nm) nanowires. Further experimental studies (such as the one carried out in Ref.

[66]) and theoretical studies will be needed to confirm any dominating mechanism responsible to the experimental findings. In any case, the ability to grow small-diameter, semiconducting Al-catalyzed Si nanowires could be a significant step forward for incorporating nanowires into future electronic devices/circuits.

2.4: Vertical integration of Ge nanowires on Si for high-performance nanoelectronics

In this section we explore the integration of Ge on a Si substrate, with the epitaxial growth of vertical Ge nanowires as our core strategy. Germanium offers both electron- and hole-mobility enhancements over Si, but is especially attractive for its high hole mobility (4X larger). Its smaller band gap (0.66 eV) enables larger tunneling currents for applications such as the tunnel FET, as well as photodetection at near-infrared wavelengths. However, the heterogeneous integration of Ge-based devices on a Si substrate has been challenging due to lattice mismatch (~ 4%) during thin film growth. To this end, the vertical nanowire geometry allows for radial strain relaxation and the growth of heterojunctions with low defect density and sharp interfaces [68-71] (Fig. 14). Thus the hybrid integration of bottom-up nanowire-based devices with traditional Si substrates offers possibilities to circumvent problems associated with conventional thin-film-based heterogeneous integration approaches.

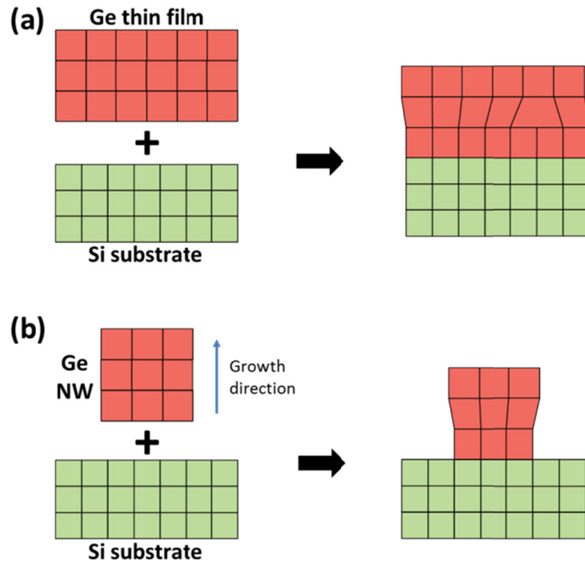

FIG. 14. Schematic comparing strain relaxation in a thin-film geometry vs. a nanowire geometry. (a) Strain relaxation in thin film showing a dislocation defect beyond the critical thickness. (b) Coherent radial strain relaxation in a nanowire. While a coherently strained film deforms vertically, a nanowire can distribute strain both vertically and laterally, and thereby accomdate a larger lattice mismatch.

Such devices, based on epitaxially grown, vertical nanowire structures, also offer the potential to be integrated vertically on top of CMOS devices, thus further increasing device density with 3-dimensional architectures. The epitaxial growth of vertical Ge nanowires on a Si substrate holds much potential as a platform for future electronic, photonic, and NEMS technologies. For FET structures (e.g. junctionless FET, tunnel FET, floating-gate memory), the vertical nanowire geometry offers optimal gate coupling due to the small channel thickness (= nanowire diameter) and the ability to fabricate a gate-all-around (GAA) structure. In addition, since the channel length of a

vertical FET is determined by the thicknesses of deposited films, which are more easily controlled than lithographically defined lengths, very short channel lengths are readily achieved[72].

2.4.1: Material system: Ge/Si core/shell nanowires

The nanoscale element that serves as the device channel in our CMOS integration and device proposals of Chapter 3 is a Ge nanowire with an optional Si shell. Ge nanowires and Ge/Si heterostructures have been shown to be able to offer high carrier mobility and device performance. For example, in a Ge/Si core/shell nanowire heterostructure developed by Lu et al. consisting of a ~2 nm Si shell epitaxially grown over a ~10 nm diameter Ge nanowire, a 1D hole gas was found to be formed and confined inside the Ge core with near ballistic transport even at room temperature[22, 73] (Fig. 15(a)). In these quasi-one-dimensional devices, it is possible that mobility can degrade due to surface roughness scattering. However, this is not expected to occur until diameter < 8 nm [74, 75]. In addition, it is known that silicon can passivate a Ge surface for reduced interface state density and higher hole mobility [76]. Furthermore, in a nanowire geometry, this passivation effect can be enhanced since the nanoscale and comparable sizes of the core and shell lead to a coherently strained Si-Ge interface to accommodate the relative large lattice mismatch between Ge and Si [77]. By integrating the nanowire channel with high-k gate dielectrics (e.g. HfO_2) and metal gate electrodes, it has already been shown that these nanowire FETs can outperform state-of-the-art Si MOSFET devices[73]. Very short channel nanowire FETs whose performance approaches the ideal ballistic

transistor limit have also been demonstrated using the Ge/Si core/shell nanowire system[78].

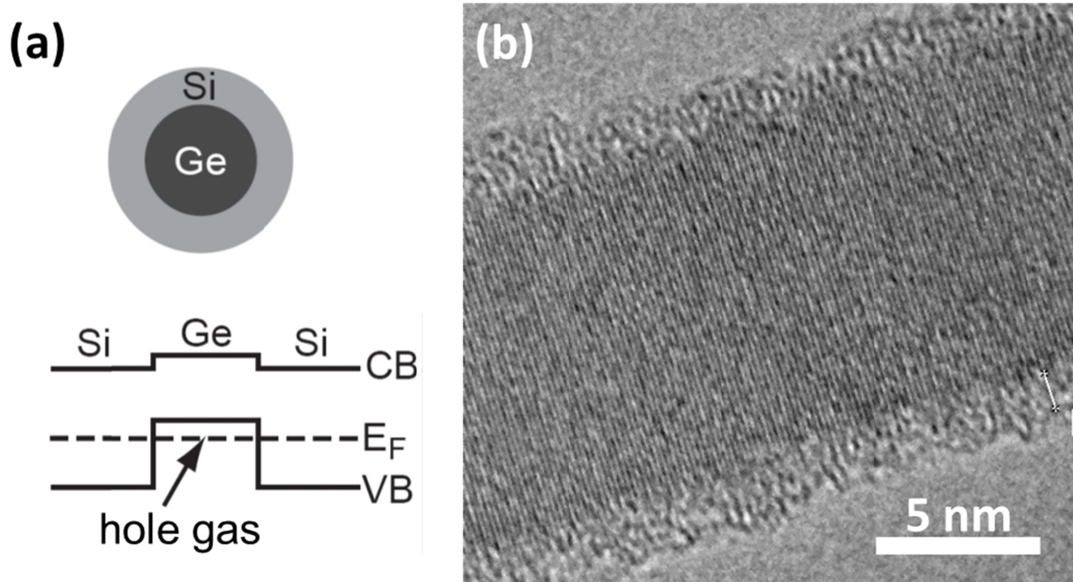

FIG. 15. Ge/Si core/shell nanowire. (a) Schematic and band diagram showing the presence of a degenerate hole gas. (b) HRTEM image of a nanowire showing a 10 nm Ge core and 2 nm Si shell.

In our group at the University of Michigan, we have developed the capability to grow Ge/Si core/shell nanowires in bulk (later in Section 2.4.2 we demonstrate controlled epitaxial growth on a Si substrate). Beginning with Au catalyst nanoparticles deposited on a SiO_2-coated Si growth substrate, Ge nanowires 10 or 20 nm in diameter (via 10- or 20-nm Au nanoparticles) were nucleated in a hot-wall tube furnace at 315 °C and 300 Torr total pressure, with gases flows of 30 sccm 10% GeH_4 in H_2, and 200 sccm H_2. Then a ~2 nm-thick Si shell was deposited around the nanowires *in situ* at 465 °C with 20 sccm SiH_4 and 5 Torr total pressure. A high-

resolution transmission electron microscopy (HRTEM) of a representative nanowire is shown in Fig. 15(b).

To verify the quality of our nanowires, we have configured them in lateral back-gated devices for electrical characterization. The nanowires were transferred from the growth substrate to a device substrate consisting of degenerately doped Si (which serves as the back gate) with a 50 nm-thick layer of thermal SiO_2 (which serves as the gate dielectric). To make source and drain metal contacts to individually selected nanowires, a standard lift-off technique was employed using PMMA (950 K), electron-beam lithography, and Ni evaporation (where just prior to evaporation the sample was dipped in buffered HF for ~2 s to remove the native oxide coating the nanowires). To make metal contact to the Ge core, a drive-in anneal (320 °C for 10 s) was performed in forming gas (5% H_2 in N_2) using rapid thermal annealing. Each device contains one nanowire (inset of Fig. 16(d)).

Figs. 16 (a) and (b) show the output and transfer characteristics, respectively, of a representative device with 20 nm Ge core diameter and 1 μm channel length. The output characteristics show long channel behavior with high ON-current density. From the transfer characteristics and using the cylinder-on-plane model for the gate capacitance (with an effective dielectric constant of 2.5, which is the average of air (1) and SiO_2 (3.9)[59]) the hole mobility was extracted to be 550 cm^2/Vs, which is comparable to the best values reported for this nanowire material system[73]. Figs. 16 (c) and (d) show analogous data and similarly good performance for a representative device with 10 nm Ge core diameter, with an extracted hole mobility of 440 cm^2/Vs.

In addition, we estimate a degenerate hole density $N \sim 10^{19}$ cm^{-3} from $N = C_g\left(0 - V_T\right)$ where C_g is the gate capacitance and V_T is the threshold voltage (estimated from the transfer curves). In Ch. 3.2 we take advantage of this modulation doping effect to demonstrate high performance vertical Esaki diodes. More generally, a high hole density is important for p-type device contacts, as well as for the development of the junctionless FET which is explored in Ch. 3.4.

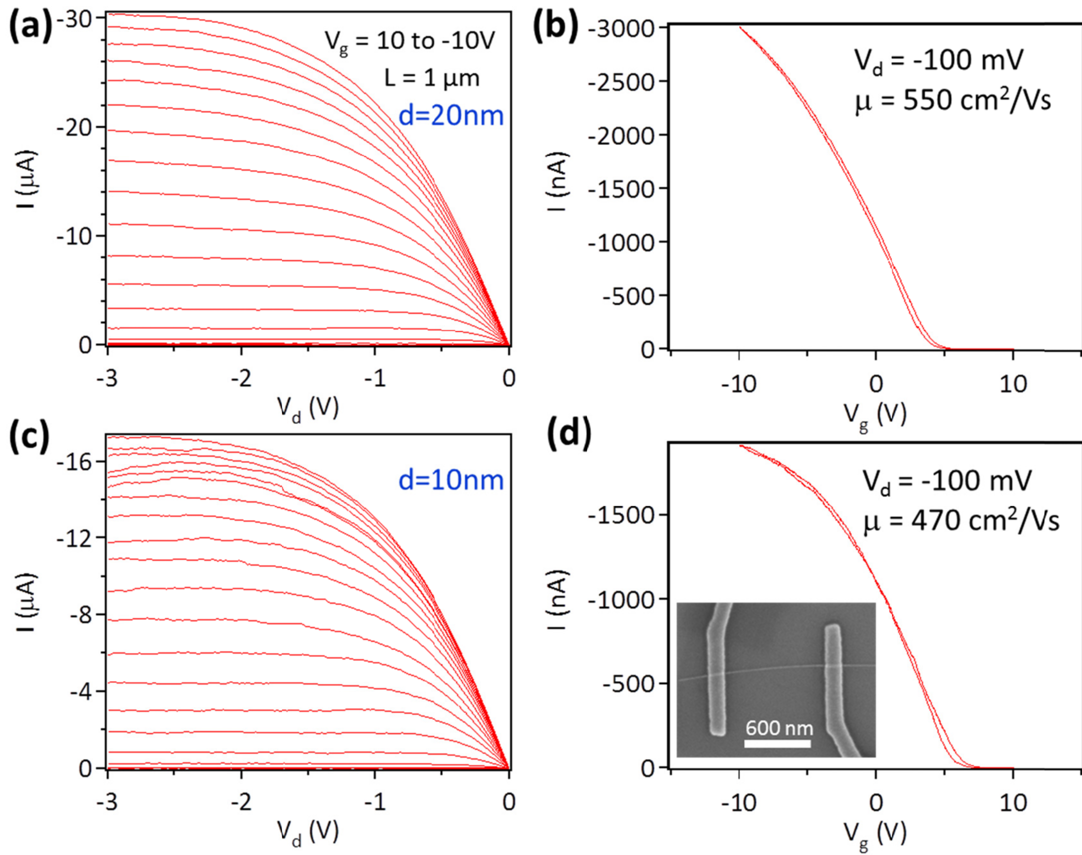

FIG. 16. (a) Output and (b) transfer curves for a laterally configured back-gated FET with a Ge/Si core/shell nanowire with 20 nm core diameter and 1 μm channel length. (c) Output and (d) transfer curves for a similar device with Ge 10 nm core diameter. Inset: SEM image of a representative device.

Thus we have demonstrated good control of the nanowire growth and produced high quality Ge/Si core/shell nanowires. We next discuss the vertical integration of this material system on Si.

2.4.2: Vertical epitaxial growth of Ge nanowires on Si (111)

As mentioned earlier, the vertical epitaxial growth of Ge nanowires has several advantages as a technique for integrating Ge on a Si substrate. The vertical nanowire geometry allows for radial strain relaxation for defect-free interfaces, narrow channel thickness and gate-all-around structure for better gate control, and 3-dimensional device integration for higher device density. Since Ge nanowires normally grow along the <111> direction, vertical epitaxial growth can be achieved on (111) Si substrates. Several studies have verified the feasibility of vertical growth of Ge nanowires on (111) Si using the vapor-liquid-solid (VLS) mechanism[79-81]. Our work closely follows Ref. [81] with the use of Au nanoparticles (20 nm in diameter, colloid purchased from Ted Pella, Inc.) as catalyst. Under a reduced-pressure (30 Torr) atmosphere composed of 0.9% GeH_4 in H_2, a two-step temperature profile was used, in which a high-temperature nanowire nucleation step (1 min. at 380 °C) was followed by a low-temperature nanowire elongation step (300 °C) to minimize conformal Ge deposition (which would lead to nanowire tapering). Fig. 17(a) shows a representative vertical Ge NW with diameter 20 nm and length 1-2 μm. As shown in Fig. 17(b), we can grow small-diameter (20 nm) vertical Ge NWs on Si with good vertical yield (> 80%). Next we discuss the growth technique in greater detail.

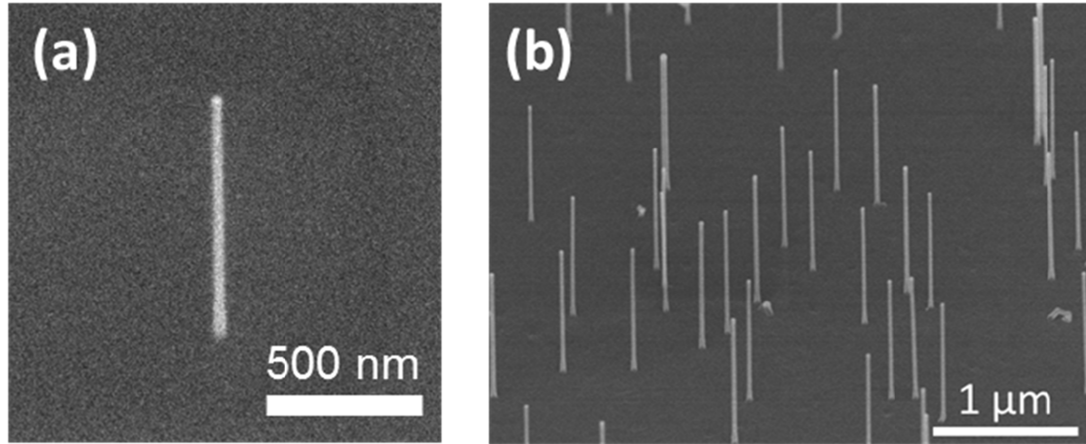

FIG. 17. (a) SEM image of a vertical Ge nanowire (20 nm in diameter) epitaxially grown on a Si substrate, taken at a 45° angle. (b) Low magnification image of the epitaxial Ge NW growth.

2.4.2.1: HF-addition for enabling epitaxial growth

To enable an epitaxial relationship between the nanowires and the Si substrate, the substrate should have no native oxide. This was achieved by soaking the substrate in 1 M hydrogen fluoride (HF) to create a hydrogen-terminated surface. We also added HF to the as-received Au colloid to a concentration of 0.1 M, to further promote hydrogen-termination [81]. This HF-addition also promotes the adhesion of the Au nanoparticles to the substrate. The H-terminated Si substrate is negatively charged at neutral pH and would tend to repel the as-received Au nanoparticles, which are also negatively-charged due to citrate-stabilization. The addition of HF to the Au colloid lowers the pH of the colloid to about 2, which tends to neutralize the citrate ions and hence reduce the repulsive forces at the substrate. However, the reduced citrate-stabilization tends to cause the colloid to agglomerate,

so that care should be taken to use the colloid immediately after HF-addition (we found no noticeable agglomeration if the colloid is used within 10 min). Finally, for the best results, the time the sample spends in air should be minimized (< 5 min.) after the Au nanoparticles have been deposited.

2.4.2.2: Pressure stabilization

Once the sample has been loaded into the furnace, it was found that the pressure should be stabilized prior to ramping of the temperature; otherwise the nanowires would kink during the nucleation step. Fig. 18(a) shows this effect. Most of the kinked non-vertical nanowires bear the same angle with the substrate, suggesting that an epitaxial relationship with the substrate still exists[81]. Other groups have used this kinking effect to create novel device structures [82, 83], but here we wish to prevent kinking and promote vertical growth.

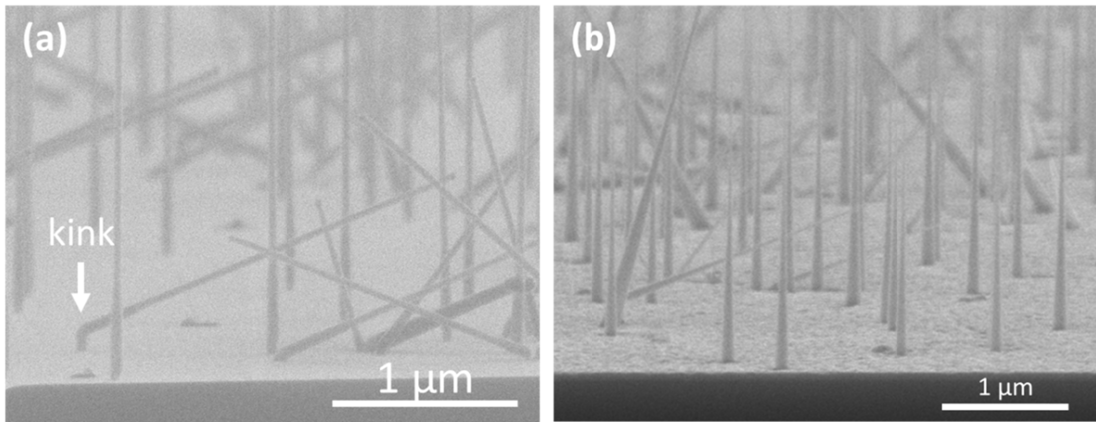

FIG. 18. (a) SEM image showing kinking during nanowire nucleation, taken at a 75° angle. (b) SEM image showing tapered nanowires.

2.4.2.3: Temperature ramp rate

Once the pressure is stable, it is also important to ramp the temperature at a sufficiently high rate to prevent ill-formed nucleation at low temperature (i.e. at less than the desired nucleation temperature). It was found that a local substrate heater capable of a ramp rate ~5 °C/s was sufficient for producing > 80% yield of well-formed vertical epitaxial nanowires.

2.4.2.4: Nanowire diameter

The nanowire diameter is governed by the diameter of the Au catalyst. We have chosen 20 nm Au nanoparticles to catalyze the growth of 20 nm-diameter nanowires. This size approaches the lower bound for growth in the <111> direction. For diameters < 15 nm, nanowires begin to exhibit different growth directions, such as <110> and <112> [77, 84], making it more difficult to achieve vertical growth on a (111) substrate. At the same time, for diameters < 10 nm, quantum confinement in the radial direction will increase the effective Ge band gap. This latter effect is undesirable for the tunnel field-effect-transistor since it negates the gains of using a small band gap material for higher tunneling drive current (See Ch. 3).

2.4.2.5: Nucleation and elongation

As is typical in VLS growth[18], the nanowire length is governed by the time spent at the elongation step (growth rate is about 50-100 nm/min). The duration of the nucleation step governs the nucleation yield (the fraction of Au catalyst nanoparticles that nucleate well-formed nanowires); a longer nucleation time corresponds to a higher yield. However, the trade-off is increased nanowire tapering due to thermal decomposition of GeH_4 at the high nucleation temperature. Shown in

Fig. 18(b) is a growth with a high nucleation yield but also a high degree of tapering. At the preferred short nucleation time of 1 min., the nanowires have little tapering, but there is also a low nucleation yield. The reasons for the low nucleation yield are currently unclear. Ref. [85] suggests that the growth conditions (temperature and pressure) could be further optimized. During our investigations, we have also seen SEM evidence of Au catalyst droplets migrating along the Si surface [44]. At ~400 °C, the apparent velocity of droplet migration is ~0.3 nm/min. Such a migration could indicate the presence of an external (non-equilibrium) disturbance during nucleation. Finally, we have observed that the substrate surface properties can have a large influence on the nucleation yield. In particular, we found that a Ge buffer layer can enable high nucleation yields; this we discuss next.

2.4.3: Ge buffer layer for nanowire location control and high growth yield

For fundamental studies, it is sufficient to select one nanowire and build a device from it. However, nanowire location control is required for any effort toward array fabrication, 3D integration with lateral CMOS devices, and more complex nanoscale circuits. Ideally, the Au catalyst nanoparticles are first patterned (placement of single particles), and from each nanoparticle a vertical nanowire is grown. Several attempts have been developed to selectively deposit nanoparticles at pre-defined locations[80, 86-92]. For example, using nanoimprint lithography[90], nanosphere lithography[91, 92], or block copolymer-templated deposition[89, 93], one can form nanoparticle patterns in a periodic array and achieve controlled

nanowire or nanotube growth. Other approaches include surface patterning of charges[80, 87, 94]. For example, by patterning a substrate with positive and negative charges using self-assembled monolayers, Huang et al. were able to deposit single 20 nm Au nanoparticles at 400 predefined sites with 91% accuracy[94].

However, for vertical Ge nanowires, there are a few challenges that must be addressed before patterned growth can be realized. First, the above patterning methods often result in oxidation of the Si substrate which would destroy its epitaxial relationship with the growing nanowire. Removal of this oxide and restoration of epitaxial growth may be achieved with the use of Cl-based chemistry during growth, although a high temperature of > 800 °C is normally required which may not be desirable during device integration. Second, both the nucleation yield (the fraction of Au catalyst nanoparticles that nucleate well-formed epitaxial nanowires) and the vertical yield (the fraction of well-formed nanowires that are vertical) should be sufficiently high. As discussed in Ch. 2.4.2.5, high nucleation yield is difficult to achieve without significant tapering of the nanowires.

A Ge buffer layer deposited on the Si substrate prior to Au catalyst deposition can address both of the above issues[95]. The native oxide of this layer would not hinder epitaxial growth because GeO_x is much more volatile than SiO_2 and hence is easily removed during nanowire growth in H_2 ambient. This makes available the

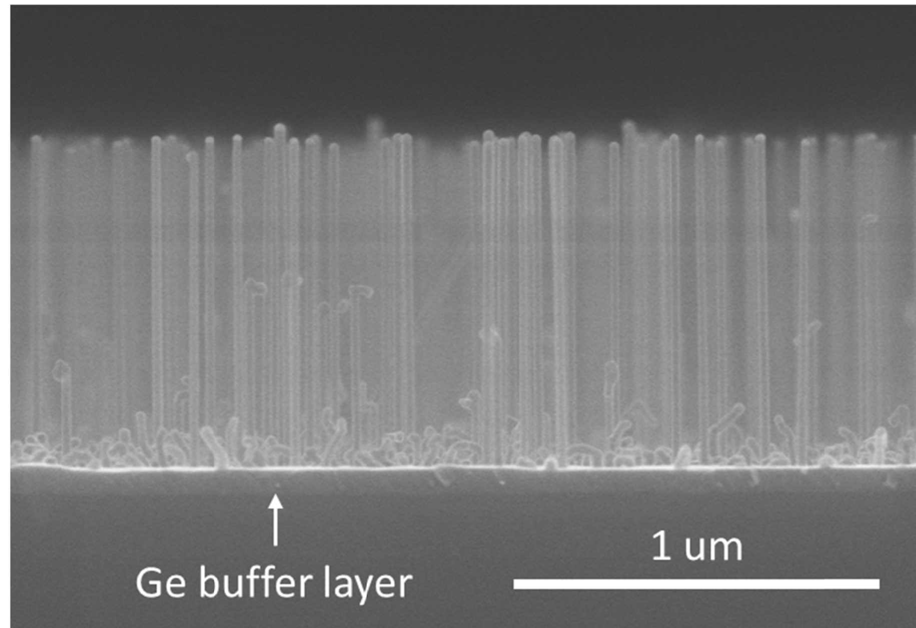

FIG. 19. SEM image showing high yield vertical growth, obtained from a Ge buffer layer that was oxidized in air for ~12 hours.

various patterning techniques mentioned above for patterning vertical Ge nanowires. Also, since the Ge buffer layer is lattice-matched with the nanowire, high nucleation and vertical yields are possible with little nanowire tapering. We have recently demonstrated the feasibility of this approach. We first deposited a ~50 nm-thick Ge buffer layer on a (111) Si substrate at 550 °C. Next, the sample was coated with the polyelectrolyte poly-L-lysine (which is positively charged), followed by the deposition of 20 nm Au nanoparticles (negatively charged in colloid). Finally, we grew nanowires using a nucleation step of 1 min at 380 °C. The result is that both nucleation and vertical yields are > 90 %, high enough for patterned NW growth. Fig. 19 shows that a high vertical yield can still be obtained on a Ge buffer layer that has been oxidized in air for ~12 hours. The use of polyelectrolyte suggests that a

charge patterning technique (as in Ref. [94]) may be employed for the location control of the catalyst nanoparticles.

While the Ge buffer layer is likely full of crystal defects and hence not suitable as a device layer, it can still serve as a contact for devices. To this end, in the future the layer should be heavily doped. Also, lower deposition temperatures should be tested, since 550 °C could be too high for CMOS compatibility for BEOL integration (see Ch. 2.1). We note that it is possible that doping can also help reduce the crystallization temperature. We have demonstrated that boron-doped Ge layers of resistivity ~1-5 mΩ-cm can be deposited at 425 °C.

2.4.4: Post-growth Au catalyst removal

The Ge nanowire growths discussed above use Au nanoparticles as the catalyst. Au is a contaminant in CMOS technology because it can create deep trap levels in the band gap, which are detrimental to device performance (for example, for tunnel devices, they increase trap-assisted tunneling in the OFF state and degrade the subthreshold swing). There are a few points to note regarding the influence of Au on device performance. First, studies strongly suggest that the electrical properties, including minority carrier transport, of Au-catalyzed Ge and Si nanowires are dominated by surface states rather than bulk impurities [45, 46]; in particular, they find that the influence of Au residing in the bulk is negligible. Second, in Au-catalyzed vapor-liquid-solid growth of Si and Ge nanowires, most of the Au remains exposed at the surface and nanowire sidewalls [44, 96]. Hence the removal of the Au exposed at surfaces would largely eliminate its influence on electrical behavior.

Woodruff et al demonstrated a wet chemical etch for this purpose [81]. We have experimentally verified their result as shown in Fig. 20.

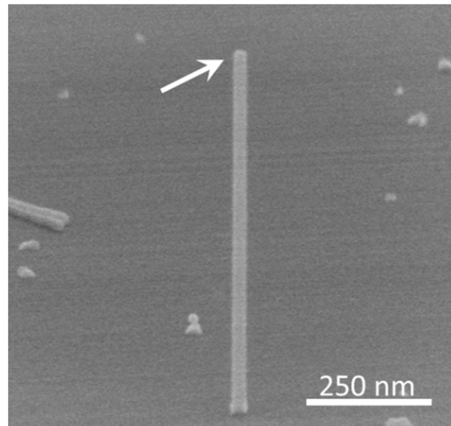

FIG. 20. Au catalyst removed from vertical Ge nanowire using a wet chemical etch (described in Ref. [81]).

2.5: Summary

In summary, we have developed several growth techniques. We have grown large quantities of Al-catalyzed small diameter Si nanowires with high growth rates and large aspect ratios using the VLS method. The Al doping levels in small diameter Si nanowires can be reduced so the nanowires still exhibit semiconductor characteristics. We have grown Ge/Si core/shell nanowires that exhibit hole mobilities > 450 cm^2/Vs. We have achieved good control of the growth of vertical epitaxial Ge nanowires on Si with 20 nm diameter; furthermore, we have achieved nucleation and vertical yields > 90% using a Ge buffer layer. Finally we have demonstrated post-growth Au catalyst removal. These developments address several of the important problems facing hybrid nanowire-CMOS systems.

Chapter 3

Toward Ge nanowire-based vertical tunnel field-effect transistors for hybrid nanowire-CMOS systems

3.1: Introduction

3.1.1: Subthreshold non-scaling in CMOS

As discussed in Ch. 1, one of the fundamental challenges that aggressively scaled devices face is increased power dissipation due to subthreshold non-scaling. Along with transistor scaling, the supply voltage V_{DD} and the threshold V_T need to be scaled accordingly to minimize power dissipation and reduce high-field effects. However, in a conventional MOSFET, a reduction in V_T results in an exponential increase in the OFF current I_{OFF}, which would increase static power dissipation. To first order, the exponential dependence of I_{OFF} on V_T in an conventional MOSFET with ideal gate coupling is given by $I_{OFF} \propto \exp\left(-qV_T/kT\right)$, where q is the electronic charge, k is the Boltzmann constant, and T is the temperature. This equation illustrates a theoretical limit to the rate at which a conventional transistor can be turned off. The origin of this limit lies in the thermal injection of carriers over a barrier into the channel (Figs. 21(a) and (b)). Due to the Boltzmann distribution, some carriers always have enough energy to overcome the barrier, and furthermore

the application of a gate voltage to raise the barrier can only reduce the current at a finite limited rate. Here it is convenient to define in the subthreshold region a figure of merit called the subthreshold swing *SS* as $SS = \partial V_G / \partial \log I_D$, which measures the gate voltage swing needed to reduce the current by a factor of 10. Equating $I_{OFF} \propto \exp(-qV_T/kT) = 10^{-V_T/SS}$ shows that *SS* has a theoretical lower limit of $kT/q \cdot \ln(10) \approx 60\,\mathrm{mV/decade}$ at room temperature. For practical devices *SS* is typically 60-70 mV/decade and normally degrades with extreme scaling. Fig. 5 (in

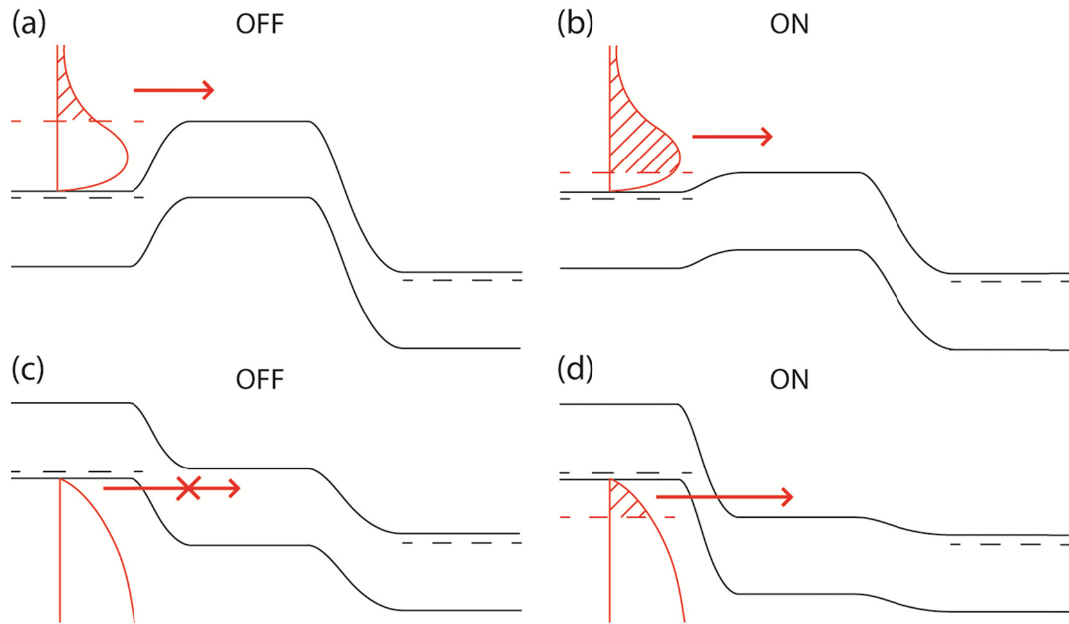

FIG. 21. (a-b) Band diagrams showing the operation of a conventional n-type FET in the (a) ON state and (b) OFF state. The turn-off process is limited by the Boltzmann distribution of carriers at the source. (c-d) Corresponding band diagrams showing the operation of a n-type TFET. The current here is determined by tunneling of electrons from the valence band in the source to the conduction band in the channel.

Ch. 1) shows the relationship of I_{ON}, I_{OFF}, V_T, V_{dd}, and SS in a conventional MOSFET. To maintain acceptably low I_{OFF}, the non-scaling of SS leads to the non-scaling of V_T. To maintain acceptably high I_{ON}, the non-scaling of V_T in turn puts a restriction on V_{DD} scaling, and causes severe power dissipation (both static and dynamic) and reliability issues for aggressively scaled devices (see Ch. 1).

3.1.2: The tunnel field-effect transistor

To continue performance scaling and address the power dissipation issue, the tunnel field-effect transistor (TFET) has been proposed. This device can potentially offer very steep SS, extremely low I_{OFF} and high speed. A TFET is essentially a gated reverse-biased p-i-n diode. The operations of an n-type TFET are schematically shown in Figs. 21(c) and (d). When an overlap of the conduction band and valence band is achieved between the source and channel, electrons in the valence band in the source can tunnel into the conduction band in the channel and be collected by the drain (Fig. 21(d)). Since in a TFET the carriers are not thermally injected over a barrier, but rather tunnel through it instead, an average SS steeper than 60 mV/decade is achievable since it is not limited by the Boltzmann distribution on the source side, if the gate can effectively change the tunnel barrier thickness. To obtain a high I_{ON} and a steep average SS in a TFET, having efficient gate control to create a high electric field for a thin tunnel barrier is of paramount importance. Fig. 7 in Ch. 1 illustrates the subthreshold behavior of a TFET. It is seen that in a TFET SS varies with gate bias and hence is less physically meaningful than in a conventional

MOSFET. For purposes of comparison an average SS can be considered, but then care must be taken to also specify the current range over which this average is taken.

A number of studies have been performed to explore prototype TFET devices. So far, impressive OFF-currents and subthreshold slopes have been obtained[97-102]. In a TFET, the OFF-current leakage is caused by the reverse bias current through the p-i-n diode and can be suppressed to as low as 0.12 pA/μm[97]. Experimentally, several groups have achieved $SS < 60$ mV/dec in various device structures[97-100, 102]. However, devices to date suffer from poor ON-state performance due to a low band-to-band tunneling probability, which is exponentially dependent on the band gap and the thickness of the tunnel barrier. The highest I_{on} demonstrated to date in a Si-based device is 12.1 μA/um at 1 V[98], which is still about two orders of magnitudes lower than that offered by state-of-the-art CMOS devices. Employing a narrow band gap material at the source/channel junction can give improved ON-state performance[103]. Additionally, heterostructures with staggered or even broken band alignment can further reduce the effective tunneling barrier and improve the ON-state performance. TFETs based on heterostructures including Si/InAs[104] and InAs/GaSb[105] have been demonstrated. However, the performance of the reported devices including SS and I_{ON} are still not sufficient due mostly to material/interface issues. In addition, questions still remain about how to integrate these new materials with Si. To this end, germanium-based materials may offer a better approach. Germanium offers high hole mobility, a small band gap, and can form a staggered heterostructure with a Si source to facilitate high tunneling currents. However, the heterogeneous integration of Ge-based devices on a Si

substrate has remained challenging due to the relatively large (~ 4%) lattice mismatch during thin film growth. A Ge-based TFET on a Si substrate has been demonstrated[97], but this device suffers from, in addition to having a low I_{ON} and an average *SS* ~ 76 mV/dec, a relatively large fixed charge density at the gate, probably due to high defect concentration in the Ge thin film on Si.

3.1.3: TFET using a vertical Ge NW grown on Si

One promising route for fabricating a TFET with steep *SS* and and high I_{on} is to use the Si-Ge tunnel junction formed at the interface between a vertical Ge nanowire grown on a n+ Si substrate. This heterostructure is suitable for a p-channel TFET with a Si source and Ge channel (band diagram shown in Fig. 22(b)). Compared with approaches based on planar structures, the nanowire geometry allows for coherent relaxation of radial strain to accommodate for the lattice mismatch between Ge and Si, as well as the creation of sharp interfaces with low defect density. In addition, the large valance band offset (~ 600 meV) between Si and Ge and the staggered band structure means the effective band gap for tunneling can be greatly reduced at the Si/Ge source/channel junction to achieve high ON-current. The Ge nanowire or a Ge/Si core/shell nanowire with a thin shell serves as the channel, offering high carrier mobility and long mean free path for effective collection of carriers at the drain side. To complete the device structure, a p+ drain can be made on the same nanowire with a thicker shell (our studies have found that the effective p-doping in Ge/Si core/shell nanowire structures can be significantly

modulated by controlling the shell thickness). The completed device structure and the corresponding band diagram are shown in Figs. 22(a) and (b), respectively.

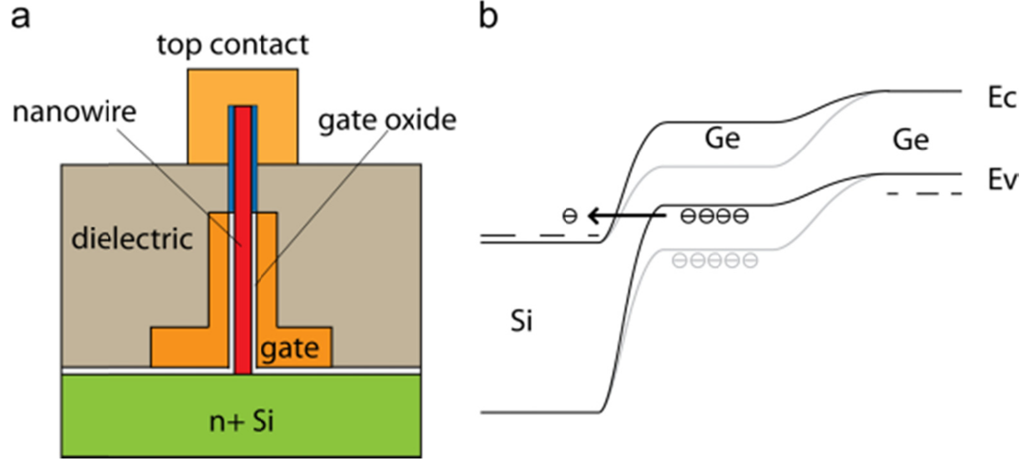

FIG. 22. (a) Schematic of a vertical TFET having an n+ Si source and a Ge nanowire channel. (b) The corresponding band diagram.

To gain further insight into the device design, we have performed first order calculations of the TFET saturation current as a function of the gate voltage, as shown in Fig. 23. The calculation is described as follows. The TFET current is dominated by the tunneling current through the Si/Ge source/channel barrier. Current saturation is reached when the drain valence band is moved beyond the channel valence band at sufficient drain-source voltage. Under this condition, the saturation current density can be estimated using an effective mass tunneling model, as

$$\begin{aligned} j &= \int \frac{dk_x 2\pi k_\perp dk_\perp}{8\pi^3} \frac{\hbar k_x}{m} qT\left(f_1 - f_2\right) \\ &= \frac{qm}{4\pi^2\hbar^3} \int_{E_C^s}^{E_V^{ch}} \left(f_1 - f_2\right) dE \int_0^{E-E_C^s} TdE_\perp \end{aligned} \tag{1}$$

where E_C^s is the conduction band edge in the source, E_V^{ch} is the valence band edge in the channel, f_1 and f_2 are the Fermi-Dirac distributions of the channel and source respectively, k_x and $k_\perp$ are the components of the electron wave vectors parallel and transverse to the direction of current flow respectively, m is the effective tunneling mass, and T is the tunneling probability. We use an expression for T derived using a Wentzel–Kramers–Brillouin (WKB) approximation for a parabolic tunnel barrier, neglecting quantum confinement effects and taking transverse kinetic energy $E_\perp$ into account [65],

$$T = \exp\left(-\frac{\pi\sqrt{m}E_g^{3/2}}{2\sqrt{2}q\hbar F}\right)\exp\left(-\frac{2E_\perp}{\overline{E_\perp}}\right) \qquad \overline{E_\perp} = \frac{4\sqrt{2}q\hbar F}{3\pi\sqrt{mE_g}} \tag{2}$$

where E_g is the effective bandgap (approximately that of Ge) and F is the average field at the junction. F is estimated using the natural length model of a MOSFET [106],

$$F = \frac{q^{-1}E_g - (V_{gs} + V_{th})}{\lambda} \tag{3}$$

$$\lambda = \sqrt{\frac{2\varepsilon_{Ge}d_{nw}^2 \ln\left(1 + \frac{2t_{ox}}{d_{nw}}\right) + \varepsilon_{ox}d_{nw}^2}{16\varepsilon_{ox}}} \tag{4}$$

where V_{th} is the threshold voltage, V_{gs} is the gate voltage, d_{nw} is the nanowire diameter, t_{ox} is the gate dielectric thickness and nanowire diameter, and λ is the natural length of a MOSFET with cylindrical gate geometry [107]. As the current depends exponentially on the field, the simple estimate of F made here using the

natural length is likely to be the largest source of error in this calculation. Replacing f_1 and f_2 with step functions and multiplying Eq. (1) by the cylindrical cross-sectional area, we get an expression for the saturation current of the TFET:

$$I_{sat} = \frac{d_{nw}{}^2 qm}{16\pi\hbar^3} \exp\left(-\frac{\pi\sqrt{m}E_g{}^{3/2}}{2\sqrt{2}\hbar qF}\right)\frac{\overline{E_\perp}}{2}$$

$$\times\left\{-q\left(V_{gs}+V_{th}\right)+\frac{1}{2}\overline{E_\perp}\left[\exp\left(2q\frac{V_{gs}+V_{th}}{\overline{E_\perp}}\right)-1\right]\right\}. \quad (5)$$

Using achievable values for the parameters within experimental control, Fig. 23 plots Eq. (5) under various conditions. Fig. 23(a) compares the proposed Ge/Si-based device with an all-Si device, and confirms that using a smaller band gap material (Ge) leads to > 1 order of magnitude improvement in ON current.

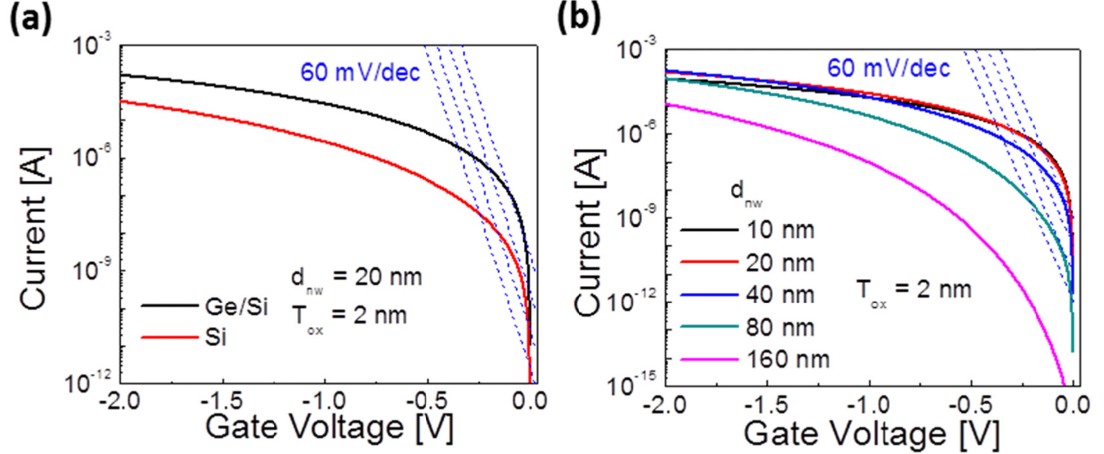

FIG. 23. First order calculations of the proposed TFET saturation current (ON current) as a function of gate voltage. (a) Comparison with a Si-based TFET shows improvement in ON current when replacing the channel with smaller band gap material Ge. (b) With varying nanowire diameter.

Fig. 23(b) shows the improvement in saturation current as the nanowire diameter decreases. It is seen that, due to increased gate coupling, which in turn causes efficient modulation of the tunnel barrier width, the total current improves down to d_{nw} = 20 nm, even though the channel cross-sectional area is decreasing. At d_{nw} = 10 nm, the benefit is not as pronounced, and a drop in total current is seen, although the current density still improves slightly. This suggests that 20 nm is a good diameter to work with. This value is also important in other respects as well. Below 20 nm, nanowire growth becomes increasingly difficult and the growth direction begins to exhibit non-<111> directions. Additionally, below 10 nm, quantum confinement effects will increase the effective band gap, reducing the drive current.

3.1.4: Chapter overview

In this chapter we address some of the engineering challenges in realizing a high performance TFET. First and foremost, achieving a vertical epitaxial Si/Ge heterostructure that can form an excellent tunnel junction at the source/channel interface is the key to realizing a high performance device. This heterojunction should have low defect density and a sharp transition region. To this end, in Ch. 3.2 we demonstrate high performance Esaki tunnel diodes using the heterojunction formed by a vertical Ge nanowire grown on a Si substrate. Our results suggest that a sharp Si/Ge heterojunction with low defect density is readily achievable. To obtain proper gate alignment and further refine the junction properties, in Ch. 3.3 we propose a raised source structure combined with low nanowire nucleation temperature. Device performance will also critically depend on the details of the

fabrication process. In Ch. 3.4, we propose to realize another important FET structure, the vertical junctionless FET; the fabrication techniques we develop through optimizing this device will greatly aid in realizing the competitive performance metrics sought for the TFET.

3.2: Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions

In this section, we demonstrate the fabrication and the electrical characterization of heterojunction Esaki tunnel diodes based on small-diameter (~20 nm) Ge/Si core/shell nanowires grown vertically on a Si substrate. Esaki diodes[108] have been proposed in applications in neuromorphic circuits[109, 110], solar cells[111], and microwave amplifiers[112]. Besides these practical applications of Esaki diodes, this device structure is also useful for studying and evaluating the tunnel junction itself for the TFET. The Esaki tunnel diode essentially constitutes the critical source/channel portion of a TFET (e.g. Fig. 22(a), except that the lightly doped Ge nanowire channel is replaced with a heavily doped Ge nanowire, and without a gate electrode). We find that a representative device exhibits a peak-to-valley current ratio (PVR) of 2.75 at room temperature, a high peak current density of 2.4 kA/cm^2, and a high tunneling current density of 237 kA/cm^2. Furthermore, the temperature dependence of the current-voltage characteristics indicates a low density of defect states at the heterojunction. Thus this study forms a solid foundation for further TFET research.

3.2.1: Vertical diode fabrication

The vertical diode fabrication also provides insight into how the vertical TFET can be fabricated. The tunnel diode device began with a degenerately doped n-Si (111) wafer (resistivity of about 0.002 Ω-cm, which corresponds to an n-type doping level of ~4×10^{19} cm^{-3})[113]. 20 nm Au catalyst nanoparticles were dispersed onto the Si substrate and vertical Ge nanowires were grown epitaxially using the methods discussed in Ch. 2.3.2. Nanowire nucleation took place at 380 °C for 1 min, followed by elongation at 300 °C for 45 min at a total pressure of 30 Torr (0.9% GeH_4 in H_2). To selectively grow the Si shell to create heavy p-doping in the nanowire, as well as limit leakage current between the top and bottom contacts outside the nanowire contact window, the as-grown nanowires were transferred to an Atomic Layer Deposition (ALD) chamber where a 25 nm-thick conformal layer of Al_2O_3 was deposited at 150 °C. Next, the Al_2O_3 film was selectively removed from the nanowires by masking the substrate with 30 nm-thick layer of spin-on-glass (semiconductor grade 700B from Filmtronics, Inc.), followed by wet etching in a 36 °C bath of 85% H_3PO_4 for ∼15 min After a de-ionized (DI) water rinse and critical point drying, the sample was loaded into a tube furnace where a ∼2 nm-thick Si shell was grown around the Ge nanowires at 465 °C for 3.5 min and 5 Torr with a flow of 20 sccm SiH_4. The bottom portion of the core/shell nanowire was then encapsulated in a 250 nm-thick layer of spin-on-glass and cured at 300 °C for 45 min. To make electrical contact to the exposed upper portion, the sample was dipped briefly in buffered hydrogen-fluoride, rinsed in DI water, and immediately transferred to an

evaporator where 100 nm Ni was deposited at an angle of 30°- 45° to ensure sufficient contact area between metal and nanowire. A drive-in anneal was performed using rapid thermal annealing at 320 °C for 30 s in 5% H_2/N_2 to form contact to the Ge core. Care was taken to ensure that the selected device under study contained only one nanowire. A schematic of the cross section of the completed device structure is shown in Fig. 24(a).

Some features of the above fabrication process are noteworthy in regard to a future attempt at realizing a vertical tunnel FET. First, the process shows that the Si shell deposition need not be deposited *in situ* after nanowire growth. In spite of the fact that the bare Ge nanowire was exposed to air, Al_2O_3, H_3PO_4, and H_2O prior to the Si shell deposition, we achieved high performance devices (see following section). This is attributed to the fact that GeO_x is volatile and is readily removed in a hydrogen-rich ambient (which is present during shell deposition). The implication is that the Si shell deposition can be used as a general technique for selective passivation and/or doping of the Ge nanowire. Second, the technique of wet etching the high quality ALD-deposited Al_2O_3 using H_3PO_4 as etchant and spin-on glass as etch mask is selective against both Si and Ge, and therefore is a general technique for creating high quality spacer layers in a future vertical FET device. This contrasts with the efforts of research groups who use polymer spacer layers that may breakdown easily and introduce leakage currents.

3.2.2: High performance at room temperature

The band diagram of the junction between the Si substrate and the Ge nanowire core is that of an Esaki tunnel diode as shown in Fig. 24(b), where both sides have degenerate carrier densities (as discussed in Ch. 2.4.1, the Si shell induces a hole gas). The devices were measured using a Keithley 4200 semiconductor

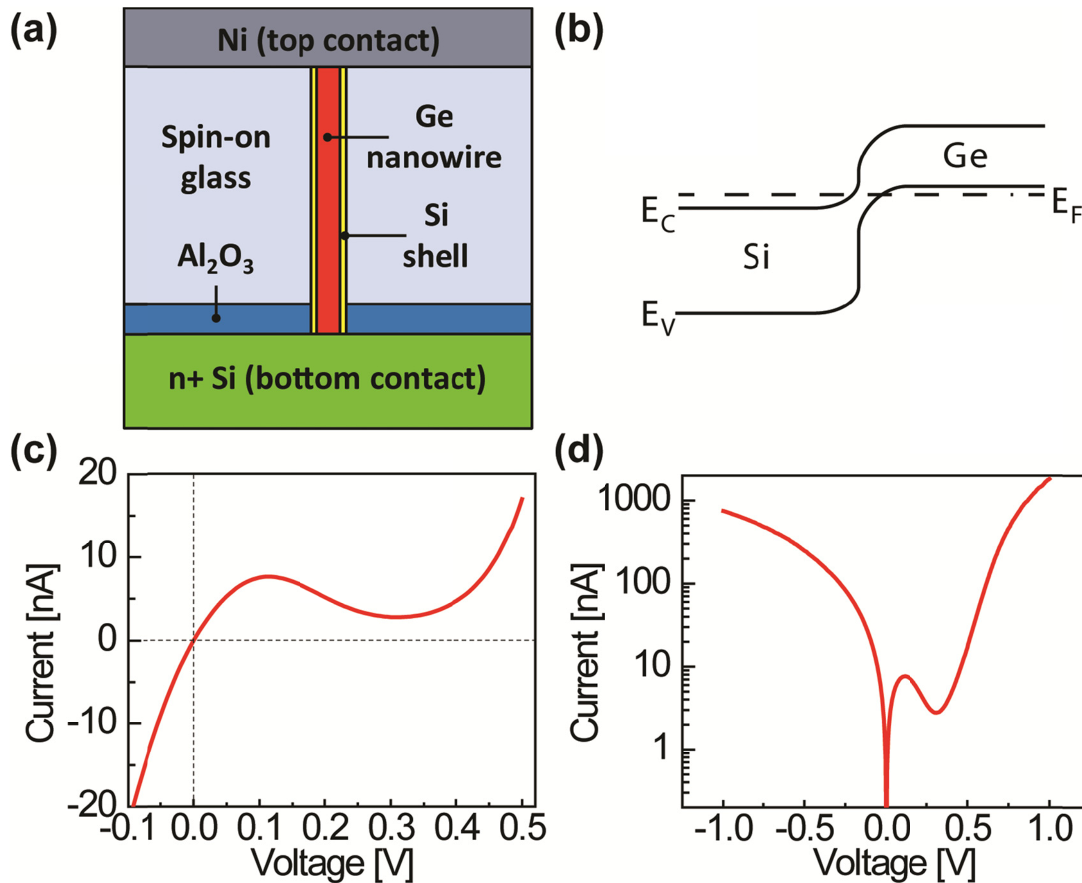

FIG. 24. (a) Schematic of the cross section of the completed vertical Esaki diode structure. (b) Equilibrium band diagram of the Si-Ge heterojunction. (c) Current-voltage characteristic of the selected device showing a PVR of 2.75 at room temperature. (d) Expanded semi-logarithmic plot of the voltage sweep shown in (c).

analyzer with the bias applied to the Ni top contact while keeping the Si substrate grounded. Several devices were measured and showed similar characteristics. Data from the most representative device are shown here. Fig. 24(c) shows a current voltage (I-V) plot taken at room temperature (294 K) showing pronounced negative differential resistance (NDR) with a PVR of 2.75, the signature behavior of an Esaki diode and confirming the band diagram of Fig. 24(b). The peak current density is estimated to be 2.4 kA/cm^2, which is among the highest values previously reported for nanowire- or Si-based Esaki diodes[111, 114]. Fig. 24(d) shows a semi-logarithmic plot taken from the same voltage sweep showing a larger voltage range at both forward and reverse bias. The reverse tunneling current density of 237 kA/cm^2 at 1 V reverse bias is also among the highest previously reported for nanowire-based devices[111, 115] and confirms the potential of the Ge/Si nanowire-based tunneling devices.

3.2.3: Temperature dependence indicates low-defect density

Detailed temperature-dependence measurements were performed to elucidate the physical mechanisms of the observed current-voltage characteristics. Fig. 25 shows several representative I-V curves at both forward and reverse bias taken at various temperatures. We first focus on the NDR region located in the forward-bias window from 0 to 0.4 V (Fig. 25(a)). The PVR increases as the temperature is decreased, with the highest PVR of 4.29 obtained at 86 K (the lowest temperature studied here). More importantly, the current in this region can be well-fitted to a model based on band-to-band tunneling[65]

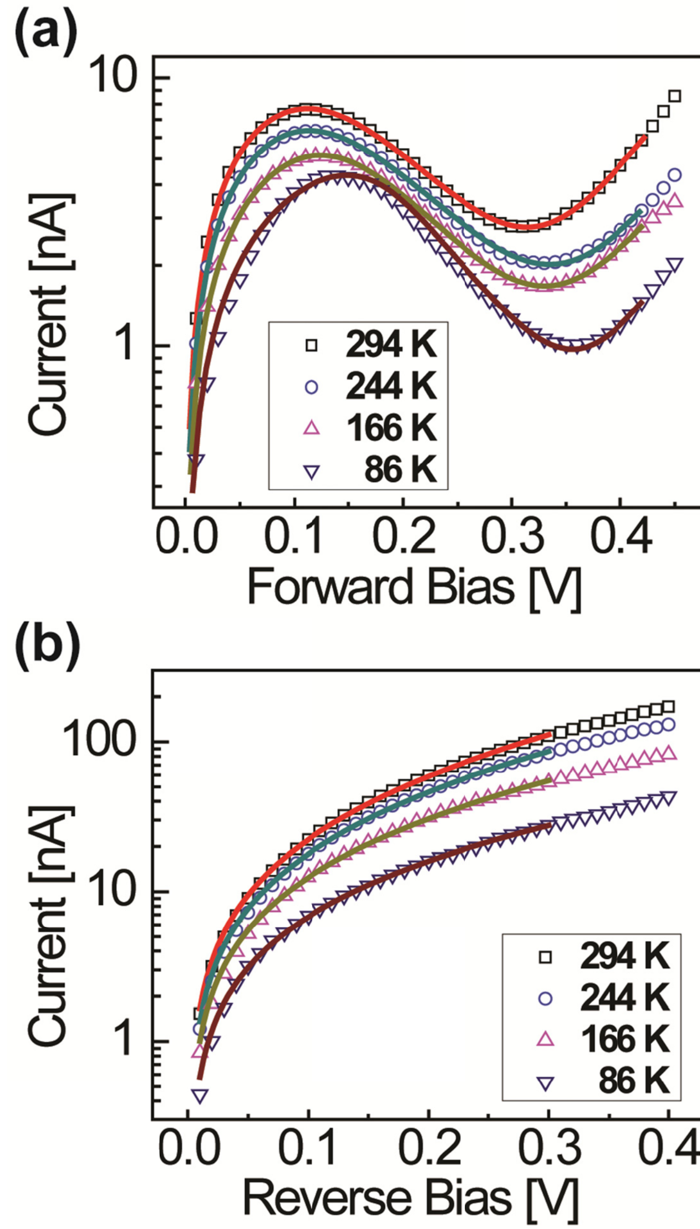

FIG. 25. Temperature dependence (down to 86K) of the current-voltage characteristics of the device shown in Fig. 24, with measured data (open symbols) and curve fits (solid curves) at 4 different temperatures. (a) Forward bias. (b) Reverse bias.

$$I = I_p \frac{V_{in}}{V_p} \exp\left(1 - \frac{V_{in}}{V_p}\right) + I_{th0}\left[\exp\left(\frac{V_{in}}{nkT}\right) - 1\right], \tag{6}$$

where V_{in} is the voltage across the heterojunction, I_p and V_p are, respectively, the peak current and peak voltage of the NDR, I_{th0} is the saturation current for thermionic emission, and n is the diode ideality factor. Essentially, the first term in Eq. (6) empirically models the direct band-to-band tunneling current which dominates at low bias, while the second term models the thermionic emission current which dominates at high bias. Using I_p, V_p, I_{th0}, and n as fitting parameters, we obtained very good fits to our data as seen in Fig. 25(a). To obtain the best fits, a temperature-dependent parasitic series resistance R_s was also included[114] so that $V_{in} = V - IR_s$, where V is the external applied voltage. The temperature-dependence of R_s is likely due to the presence of a small Schottky barrier at the interface between the Ni top contact and the Ge nanowire, and its inclusion into the model does not change the main results. From the fitting, the intrinsic peak voltage $V_p \approx 0.082$ V was found to be roughly independent of temperature. The term for the so-called excess current, which accounts for tunneling via defect states in the band gap[65], was not included here. We found that the excess current term was not needed to accurately reproduce the behavior of our device, suggesting that the device contains a low density of defect states and a high quality Si-Ge heterojunction between the n-type Si substrate and the p-type Ge nanowire.

Similar fittings were performed for reverse bias (Fig. 25(b)). Here, the current is modeled by the expression for tunneling across a triangular barrier[65]

$$I_R = \frac{CFV_R}{E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F} \right), \tag{7}$$

$$F = \sqrt{\frac{qN\left(V_{bi} + V_R\right)}{\varepsilon_s}}, \tag{8}$$

where V_R is the absolute value of the applied reverse bias, m^* is the effective tunneling mass, E_g is the effective band gap, $\varepsilon_s = 14\varepsilon_0$ is the permittivity of the semiconductor (taken to be the average between that of Si and Ge[65]), F is the maximum field at the junction interface, N is the doping concentration, V_{bi} is the diode built-in potential, and C is a device-dependent prefactor. From the literature, the effective tunneling mass m^* is estimated to be $0.037m_0$ for the Si-Ge heterojunction[116]. The effective band gap is given by $E_g = E_g\left(\text{Ge}\right) - \Delta E_C$, where E_g(Ge) is the band gap of Ge and ΔE_C is the conduction band offset between Si and Ge, which is estimated to be 0.05 eV from the difference in electron affinities[65]. E_g(Ge) has a temperature dependence established empirically as[65]

$$E_g\left(\text{Ge}\right) = 0.74 - 4.77\times10^{-4} \frac{T^2}{T + 235} \ \text{eV}. \tag{9}$$

The series-resistance effect was not considered in this case since the Schottky barrier at the Ni/Ge contact would be forward-biased at these bias conditions and its contribution should be small. As a result, only two fitting parameters, N and V_{bi}, were used to fit all the curves at different biases and temperatures in Fig. 25(b). Excellent fits were obtained with $N = 3\times10^{19}$ cm^{-3} and V_{bi} ranging from 0.67 V to 1.17 V. The value of N is consistent with an assumption made in Eq. (8) that the

doping level is similar on both sides of the junction. V_{bi} is given by $qV_{bi} = E_g + E_p + E_n$, where E_p (E_n) is the distance between the Fermi level and the valence (conduction) band edge. The fact that we obtained $qV_{bi} > E_g$ is again consistent with the band diagram and the tunneling picture shown in Fig. 24(b). These analyses unambiguously verify that the band-to-band quantum mechanical tunneling model captures the dominant conduction mechanism in reverse bias, and again support the claim that the nanowire and the substrate form an effective tunnel junction for Esaki diode and TFET applications.

The temperature dependence of the peak current I_p is shown in Fig. 26. Theoretically, I_p can also be estimated from the tunneling model and has the following form[65, 117]:

$$I_p = I_{p0} \exp\left(-\frac{4\sqrt{2m^*} E_g^{3/2}}{3q\hbar F} \right), \tag{10}$$

Here the only temperature dependence term originates from the band gap E_g. Using Eq. (10) and keeping the same parameters used in the fitting results of Fig. 22, we obtained a good fit of I_p vs. temperature as shown in Fig. 26. This agreement suggests that the temperature dependence of I_p manifests itself only through the temperature dependence of the band gap (Fig. 26, inset), i.e., a reduction in E_g leads to a higher tunneling probability. This observation again justifies the use of Ge nanowires to form high-performance Esaki diodes and possibly TFETs.

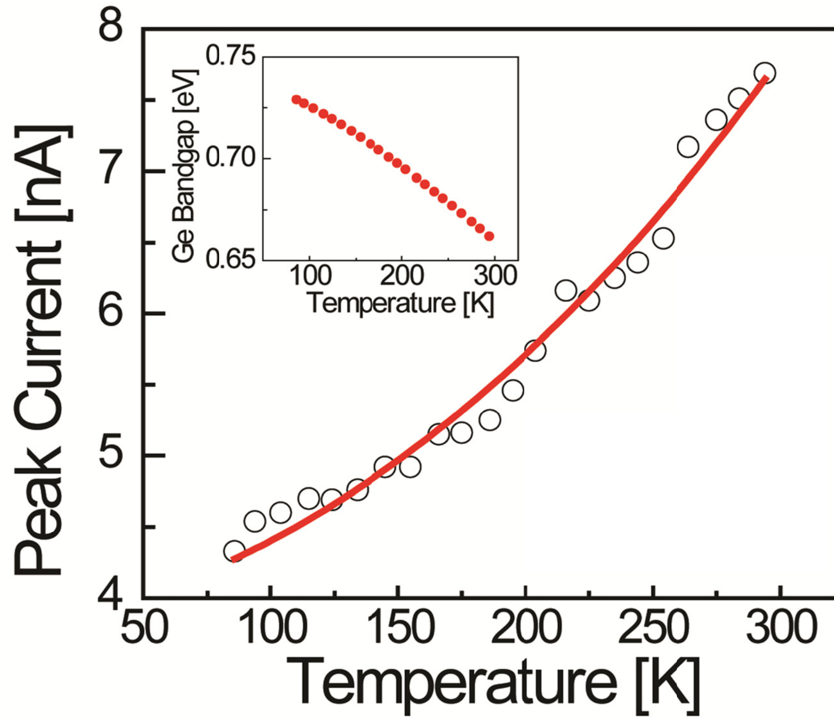

FIG. 26. Measured peak current I_p vs temperature. I_p was extracted from the measured data (open circles) and is fitted using Eq. (10) (solid line). Inset: temperature dependence of the band gap of Ge used in the fitting.

3.3: Prospects for ultrasharp vertical nanowire-based Si-Ge heterojunctions for tunnel field-effect transistor applications

The results of Ch. 3.2 suggest that the interface between a vertical Ge NW and the Si substrate on which it is grown may be an effective tunnel junction for TFET applications. The advantage of our approach is that the degenerate doping of the Si substrate (TFET source) is achieved prior to and decoupled from the nanowire growth (TFET channel formation), while in planar devices it is achieved through implantation and subsequent annealing which creates graded doping profiles. Here

we show some work-in-progress that continues our development toward a high performance TFET. In Ch. 3.3.1 we address the issue of gate alignment, and in Ch. 3.3.2 we demonstrate sub-eutectic vertical epitaxial growth for improving the junction sharpness. We also demonstrate that both of the proposed techniques may be combined.

3.3.1: Vertical growth of Ge nanowires on Si nanopillars for optimal vertical FET gate alignment

An apparent disadvantage of the nanowire-substrate geometry is that it does not allow for optimal alignment of a gate to the source-channel interface, which is critical for tuning the tunnel barrier thickness there. As shown in Fig. 27 (a), the dielectric spacer layer between the gate and the source misaligns the gate from the nanowire-substrate tunnel junction. A more ideal geometry is shown in Fig. 27(b), in which the Ge nanowire has been grown on a Si nanopillar. As shown in the figure, this raised source structure allows proper gate alignment for optimal coupling with the tunnel junction. We have demonstrated the feasibility of this hybrid top-down/bottom-up technique (Fig. 27(c)). The process begins with the use of a Au nanoparticle as an etch mask for creating a Si nanopillar using reactive ion etching[118]. Then the same Au nanoparticle catalyzes the growth of a vertical Ge nanowire in a self-aligned fashion. In addition to allowing precise gate alignment, this geometry may offer reduced defect density at the interface due to the so-called compliant substrate effect[68-71, 119], in which not only can the nanowire geometry

coherently accomodate strain along three dimensions, but the substrate can do so as well, such that the strain is partitioned between the two.

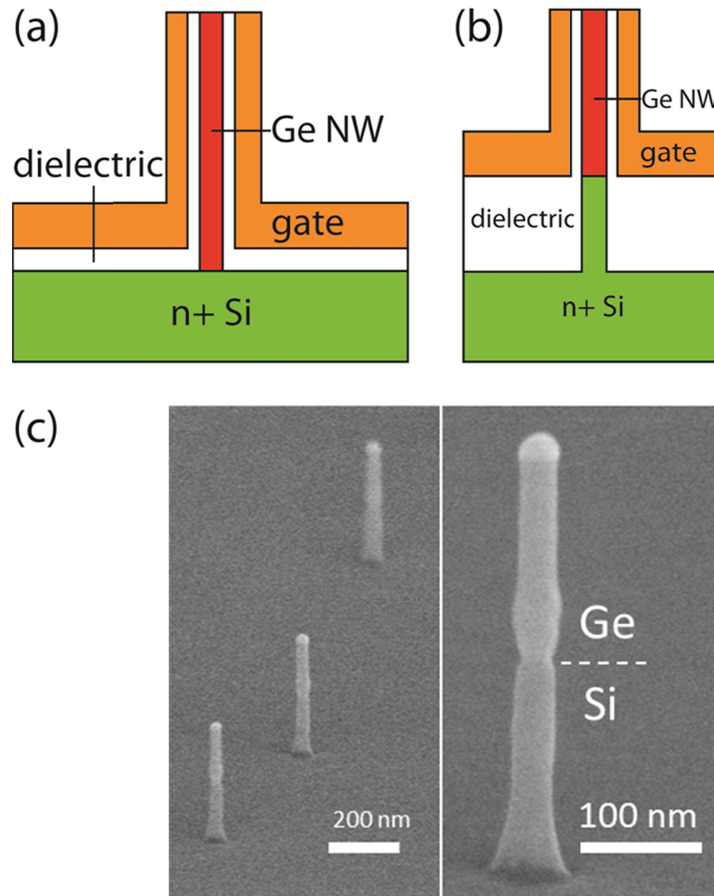

FIG. 27. (a) TFET gate is misaligned with the Ge/Si NW/substrate junction (b) By first etching a Si nanopillar, the geometry allows optimal gate alignment for control of the tunnel junction. (c) SEM image of vertical Ge nanowires (diameter 30 nm) grown epitaxially on Si nanopillars.

3.3.2: Sub-eutectic growth of vertical epitaxial Ge nanowires on Si for ultrasharp heterojunctions

To achieve a steep subthreshold slope in the TFET, ideally its tunnel junction should be atomically sharp and defect-free. The Esaki diode measurements of Ch. 3.2 suggest that our Ge/Si heterojunctions have a low defect density and a transition region of a few nanometers or less (otherwise negative differential resistance would not have been observed). While the results are promising, there is still a concern regarding the junction sharpness. Since the bulk eutectic temperatures of Au-Si and Au-Ge are similar (360 °C for Ge, 363 °C for Si), Si-Ge intermixing may still occur during nanowire nucleation at 380 °C. There have been several studies regarding the feasibility of achieving sharp axial Si-Ge heterojunctions in bottom-up grown nanowires[120-123]. Generally, junctions formed via the vapor-liquid-solid growth mechanism become graded due to the so-called reservoir effect that occurs in liquid catalysts. Wen et al. have achieved ultrasharp junctions using the vapor-solid-solid mechanism (where the catalyst remains in the solid state)[121]; however, the Au_2Al alloy catalyst they used most likely would result in high levels of unintentional Al p-doping of the Ge nanowire ([121]; also see Ch. 1.2). Here we propose to investigate the Si-Ge heterojunction formed by a vertical Ge nanowire grown on a Si substrate, using Au catalysts and nucleation temperatures < 360 °C. Our work suggests that vertical growth and ultrasharp junctions are achievable for nucleation temperatures $<$ 320 °C. Shown in Fig. 28(a) is an SEM image of vertical Ge nanowires nucleated at 320 °C on a Si substrate. The vertical yield is comparable to that obtainable at higher temperature nucleation ($>$ 50%). Fig. 28(b) shows a high resolution TEM

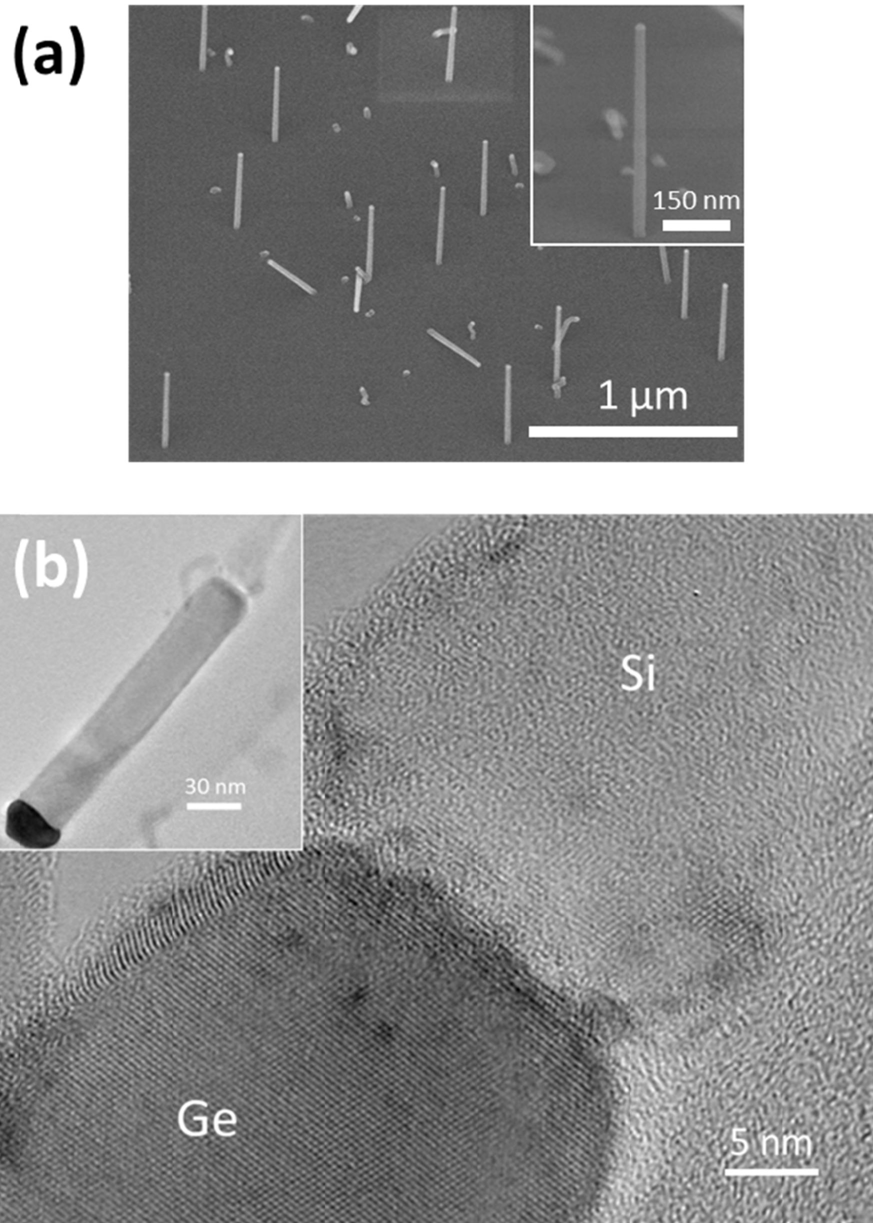

FIG. 28. (a) SEM image (taken at 45° viewing angle) of vertical Ge nanowires (20 nm in diameter) nucleated on Si (111) at 320 °C. Inset: High magnification image taken at 75° viewing angle. (b) High resolution TEM image showing a sharp Ge/Si heterojunction at the interface of a Ge nanowire grown on a Si nanopillar at 320 °C. Inset: low-magnification image of the same nanowire showing faceted Au catalyst nanoparticle.

image of a Ge nanowire nucleated on a Si nanopillar at 320 °C. The transition region appears to be very sharp (< 2 nm). Interestingly, the Au catalyst at the tip of the nanowire (inset of Fig. 28(b)) is faceted, suggesting that the growth condition is close to that of the vapor-solid-solid mechanism[56, 121]. More detailed studies are needed to confirm these conclusions.

3.4: Prospects for vertical junctionless field-effect transistors based on Ge/Si core/shell nanowires

Growing a nanowire channel on a substrate which is then used as a device contact creates a convenient platform for exploring other device concepts. For example, by changing the substrate doping from n+ to p+, a vertical tunnel FET is transformed immediately into a conventional MOSFET with gate-all-around geometry. If in addition, the nanowire is also doped p+, another important FET structure, the vertical junctionless FET, is formed. While the basic physics of the tunnel FET and the junctionless FET are very different from each other, optimizing the performance of one will greatly aid the optimization of the performance of the other. Since they share the same basic vertical Ge nanowire channel grown on a Si substrate, they share fabrication challenges such as optimizing the gate stack, forming a low-resistance top contact, and depositing spacer layers. Indeed, with our nanowire platform it can be argued that fabricating a high performance junctionless FET is a prerequisite for a high performance tunnel FET, since the former is a simpler structure that does not need a tunnel junction. To this end, here we show some

work-in-progress toward realizing a high performance junctionless FET. As this device has gained much interest recently, first we begin with some background.

3.4.1: Introduction to junctionless FET

As CMOS devices continue to scale down, it becomes increasingly difficult to fabricate devices with short channel lengths (sub-100 nm). Extremely sharp doping profiles (e.g. transition from 10^{19} cm^{-3} n-type to 10^{18} cm^{-3} p-type in a couple nanometers) are required, and this imposes severe constraints on the processing thermal budget. In nanowire-based FETs, short channels are achievable with a controlled silicidation process to form nanoscale source-drain silicide contacts[78]. However, these devices suffer from high OFF current due to the use of Schottky contacts which cause ambipolar conduction (i.e. the lack of a band gap in the silicide allows carriers of the opposite type to tunnel into the channel at large gate voltages). Furthermore, the use of any junctions to separate contacts from the channel makes gate alignment increasingly difficult as the channel length decreases.

To address the above issues, a nanowire structure, termed a "junctionless FET," has emerged as a promising candidate[124]. The junctionless FET is very similar in construction to the conventional MOSFET except that its source, channel and drain are heavily doped uniformly throughout, i.e., there are no junctions separating them. Fig. 29 compares the operation between the two devices. The channel region is only defined by the gate so issues with alignment or dopant profiles do not come into play. Unlike the conventional MOSFET in which the channel is a sheet of inversion charge at the oxide-semiconductor interface (Fig. 29(a-b)), the

junctionless FET has a bulk semiconductor channel through which majority carriers travel and whose cross-sectional area is controlled by the gate (Fig. 29(c-d)), similar to the JFET and MESFET in this respect. The device turns on at the flat-band

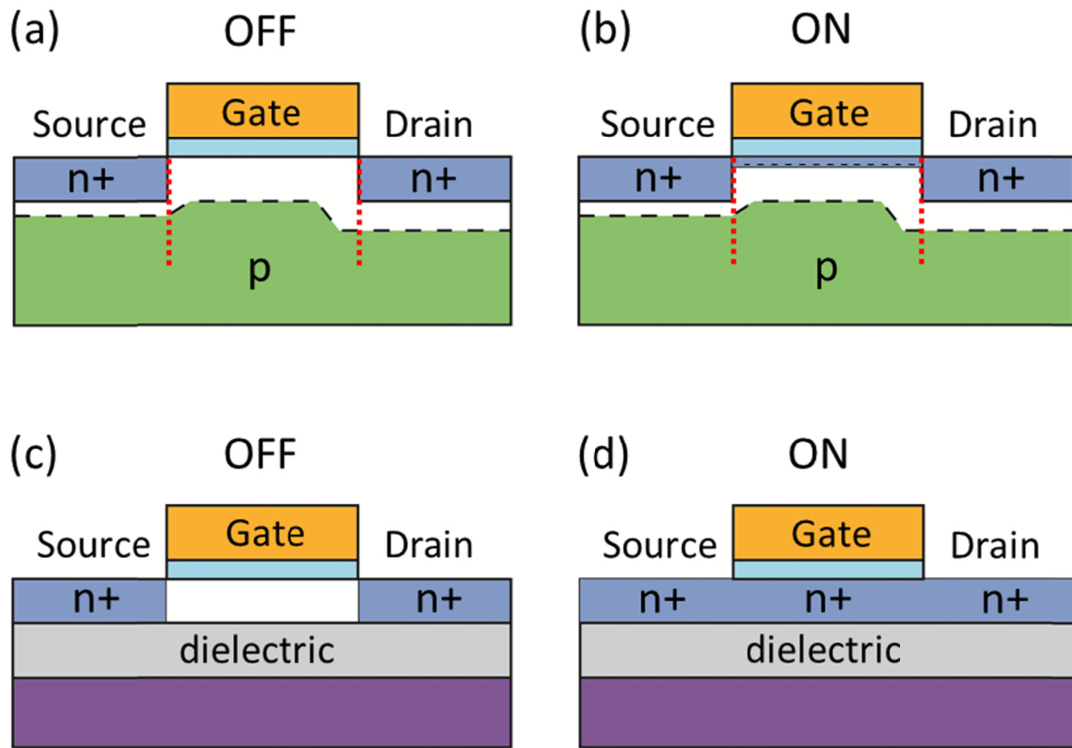

FIG. 29. Schematics comparing the operation of the conventional MOSFET and the junctionless FET. (a) Conventional MOSTFET OFF state. (b) Conventional MOSFET ON state. (c) Junctionless FET OFF state. (d) Junctionless FET ON state. For the conventional MOSFET, the vertical red dotted lines show the positions of the pn junctions that the gate must align to. The junctionless FET has no such requirement for alignment.

condition, which minimizes carrier scattering at interfaces (enhancement mode operation is achieved through tuning of the gate metal work function). Hence, a

junctionless transistor requires nanoscale dimensions and nanowire geometry to allow full depletion of carriers in the OFF state, and a high density of majority carriers to allow sufficient drive current in the ON state. As it becomes more and more challenging to define junctions in aggressively scaled MOSFETs, this concept offers an attractive alternative with its much-easier fabrication flow and competitive performance metrics. Nanowire-based FETs are especially suited to implement this concept due to their small channel thicknesses and gate-all-around geometry for excellent gate coupling. At the same time, vertical nanowire-based FETs are attracting interest due to their scaling potential. To date, more progress has been made in developing n-channel vertical FETs[125, 126] than in developing p-channel vertical FETs[127]. Only a few vertical p-channel nanowire-based FETs have been demonstrated, and their performance is nowhere near that of their lateral counterparts [73], and hence currently there is an opportunity to significantly advance the state-of-the-art.

3.4.2: Device proposal and preliminary electrical measurements

We can develop a vertical junctionless p-channel FET using a vertically grown Ge/Si core/shell nanowire. In our device, schematically shown in Fig. 30(a), the underlap regions between gate and contacts serve as source and drain. To get a reasonable ON current, the nanowire needs to be doped to a level of 10^{19} cm^{-3} or more. With conventional dopants, however, the hole mobility will typically degrade to about 50 cm^2/Vs or less. But in our device, the Si shell can provide (via modulation doping effects) a high density hole gas in the Ge core without intentional

doping of the core, and thus greatly reduce impurity scattering. Moreover, the Si shell provides excellent passivation of the Ge nanowire surface, which further promotes carrier mobility. As was shown in Ch. 2.4.1, our nanowires exhibit high hole mobilities, and previous research on this nanowire material system demonstrated that it can be > 700 cm^2/Vs, which is over 10 times higher than the hole mobility obtained in heavily doped Ge films[73]. Finally, the vertical geometry allows a gate-all-around structure for optimal gate coupling, as well as excellent control of very short channel lengths through tailoring of film thicknesses[72].

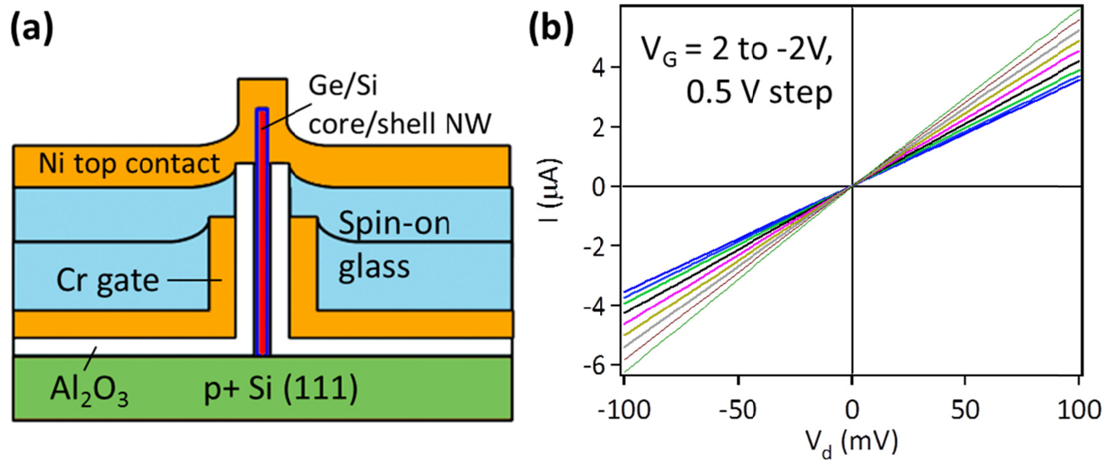

FIG. 30. (a) Device schematic of preliminary design of vertical junctionless FET (b) Output curves of fabricated device showing high ON-current density.

We have fabricated devices with basic transistor functionality. The most notable difference between lateral and vertical processing is that in the former, dimensions are determined by lithography, while in the latter they are governed by film thicknesses, which are readily controlled at the nanoscale. To establish basic

working devices, our tentative process flow is as follows (once optimized, the fabrication process also will give valuable insight into the processing of the TFET and other vertical device structures). We begin with a p-type degenerately doped Si (111) wafer which serves as external connection to the drain contact. Vertical Ge nanowires (20 nm in diameter, 1-2 μm in length) are grown and a ~2 nm-thick Si shell is deposited in situ, using the methods described in Ch. 2.4.1 and 2.4.2. Next, atomic layer deposition (ALD) is used to deposit a 25 nm-thick conformal layer of Al_2O_3, which acts as both gate dielectric and as spacer between gate and bottom contact. Next, ~30 nm Cr is sputtered to form the gate-all-around structure. The gate length is defined with a ~200 nm-thick layer of spin-on glass (SOG, 700 B from Filmtronics) cured at 300 °C, followed by wet etching of Cr in CR-14. The SOG acts as etch mask for the Cr etch; hence the thickness of the SOG determines the gate length. To form the spacer between gate and top contact, another layer of SOG (which again serves as etch mask) is spin-coated, and the Al_2O_3 exposed at the nanowire tips is wet-etched in a temperature-controlled bath of 85% H_3PO_4. Finally, the top metal contact is formed with Ni (evaporated at an angle of ~30°- 45° to ensure sufficient contact area along the nanowire sidewall), followed by a drive-in anneal using rapid thermal annealing (320 °C for 30 s) to make metal contact to the Ge core.

With the above process, we have established basic transistor functionality. Shown in Fig. 30(b) are output curves showing transistor gating and high ON current density. This device shows short channel behavior, probably caused by uncertainties in the Cr etch and the thick oxide. With further improvements (see next section), it

should be possible to improve the device performance to levels comparable to state-of-the-art lateral devices based on the same nanowire material system[73].

3.4.3: Fabrication developments

Here we show some fabrication techniques we have developed at the time of this writing that will improve upon the process described in the previous section, and make progress toward realizing a high performance nanowire-based vertical junctionless FET. The techniques are general enough that they can be directly applied to the fabrication of the vertical tunnel FET as well.

First, we have changed the gate metal from Cr to Al. Besides being CMOS-compatible, Al has a work function low enough to yield enhancement-mode devices based on Ge/Si core/shell nanowires [73]. Second, we can define the gate length using PMMA instead of spin-on glass. The latter is difficult to remove selectively, while the former is easily removed using acetone. Selective removal of this gate-definition layer allows one to inspect the gate and measure its length directly in the scanning electron microscope. Shown in Fig. 31(a) are ~300 nm Al gates defined in this manner.

We have also refined our control of the wet etching of Al_2O_3, such that we can separately define the gate-bottom contact spacer and the gate dielectric (in the previous process, the same Al_2O_3 layer was used as both spacer and gate dielectric). Fig. 31(b) demonstrates that a reproducible timed etch of the Al_2O_3 at 36 °C can remove the conformal Al_2O_3 layer around the nanowire, while leaving it undisturbed (via a spin-on-glass etch mask) elsewhere so it can serve as a high quality spacer layer.

Following this step, the gate dielectric of choice (e.g. HfO_2) may be deposited. The inset of Fig. 31(b) shows a partial etching (which is also reproducible), demonstrating the level of control this technique can achieve. For reproducible wet etching, it is essential that the temperature and concentration of the etchant bath is well controlled, and attention must be paid to the method of sample agitation.

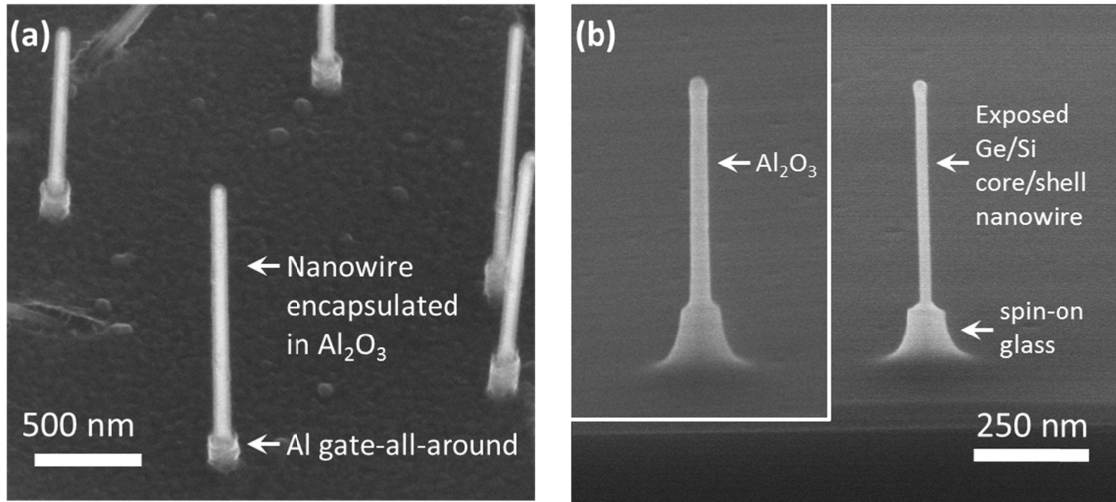

FIG. 31. Fabrication techniques for vertical FET structures. (a) Cylindrical Al gates around vertical nanowires (20 nm diameter) encapsulated in 25 nm Al_2O_3. Image taken at 45° tilt angle. (b) Controlled wet etching of Al_2O_3 using spin-on glass as an etch mask to expose a Si/Ge core/shell vertical nanowire for gate dielectric deposition, while keeping the Al_2O_3 on the substrate and the base of the nanowire to be used as spacer. The structure at the base of the nanowire is due to the up-slope formed during spin-coating of the spin-on glass. Alternatively, the inset shows a partial etch leaving 8 nm Al_2O_3 as gate dielectric and 25 nm Al_2O_3 as spacer. Image taken at 75° tilt angle.

3.5: Summary

In summary, high performance Esaki diodes made from Ge/Si core/shell nanowires have been demonstrated. Temperature-dependent current-voltage measurements indicate a high quality Si-Ge heterojunction. Further studies may include probing the junction quality at lower temperatures (e.g. 4.2 K with liquid He) where trap assisted tunneling can be observed to quantitatively study the trap density at the junction [128].

In addition, we have grown vertical epitaxial Ge nanowires on Si nanopillars at a sub-eutectic temperature of 320 °C. This result is useful for creating ultrasharp heterojunctions and enabling proper TFET gate alignment at the junction. Finally, we have developed some fabrication techniques for vertical FET structures. In particular we have demonstrated Al cylindrical gates and the use of high quality Al_2O_3 as spacer material while allowing independent selection of gate dielectric material/thickness.

Chapter 4

Radio frequency nanowire resonators and *in situ* frequency tuning

The previous two chapters focused on topics which emphasized the electronic properties of nanowires, with particular attention to CMOS-compatibility. However, the technological potential of nanowires reaches into novel degrees of freedom, in particular the mechanical degrees of freedom. With its small mass, a nanowire can be set into mechanical motion at energies that are easily accessible via on-chip electrical forces. Such nanoelectromechanical systems (NEMS) have potential applications including ultrasensitive mass and force sensing [31-35], ultra-low-power frequency domain signal processing [129], and quantum measurement [36-38]. NEMS devices can be roughly classified as quasistatic, in which each mechanical state is static (e.g. the two states of a single-pole, single-throw switch), or resonant, in which the mechanical motion and transducing signals are time varying (e.g. mechanical resonators). Here we focus on the latter.

4.1: Introduction

For many NEMS applications, the pursuit of ultrahigh quality factor Q is of paramount importance. This dimensionless parameter quantifies how well a

resonating structure can store its energy in the preferred oscillating mode. Q can be defined as $2\pi \times$ (energy stored) / (energy lost per cycle of oscillation). A resonator in communication with its environment will ultimately achieve thermal equilibrium, and hence no resonator is perfect, such that during each cycle some energy is dissipated into the environment. Minimizing the dissipation ($\sim 1/Q$) within a resonant mechanical element is essential for maximizing its sensitivity to externally applied forces (signals), maximizing its tolerance to fluctuations that degrade spectral purity (i.e. broaden its natural linewidth), and minimizing power consumption. There are a number of fundamental dissipation mechanisms, including interactions between the normal mode of interest (a normal mode is a dynamic state of the system in which all degrees of freedom have the same harmonic time dependence, e.g. motion of the oscillator) and other mechanical normal modes (e.g. phonons) and interactions between electrons and phonons. There are also non-intrinsic dissipation mechanisms, including the motion of ions or defects in the crystal due to the imposed strain, and interactions with surface contaminants. Finally, there are device-dependent external dissipation mechanisms such as clamping loss.

It was expected that nanoscale mechanical resonators potentially can obtain ultrahigh Q by suppressing acoustic energy losses intrinsic to a bulk crystal [130]. As a resonator's dimensions decrease, the wavevectors of the allowed normal mechanical modes (through which energy exchange and heat conduction are possible) become more spread apart in k-space, such that many of these phonon modes can be frozen out at low enough temperatures. The sample becomes smaller than the mean free path of phonons. Eventually, when only a handful of modes remain (it is not

possible to freeze out all modes), we reach the quantum limit of thermal conduction, where each mode conducts heat with the thermal conductance quantum, and phonons travel ballistically through the resonator (inside which temperature is no longer well defined). Ballistic phonon transport has been demonstrated experimentally. In nanoscale rods with very smooth surfaces, phonon mean free paths have been measured in excess of 3-10 μm [131, 132]. Thus, a resonator with such minimal thermal conductance can be expected to minimize the energy exchange between its oscillating mode and other mechanical modes and achieve high Q.

However, experiments with nanoscale resonators have indicated a degradation of Q as the surface-to-volume ratio increases, and there is strong evidence that surfaces play a dominant role in the dissipation(see Ref. [133] and references therein). Fig. 32 shows that experimentally measured Qs tend to scale downward with linear dimension (i.e. volume-to-surface ratio), illustrating the importance of surface-related dissipation mechanisms. In this respect it may be difficult for top-down etching techniques to produce an ultrahigh Q NEMS resonator out of a bulk substrate or thin film, since these techniques can result in rough and/or contaminated surfaces. To this end, bottom-up chemically synthesized nanowires and nanotubes have emerged as attractive candidates for the construction of NEMS devices because of their small size, excellent material properties, and atomically smooth (potentially low-loss) surfaces[134]. Very-high frequency (VHF) and ultrahigh frequency resonators have recently been demonstrated based on these nanomaterials [34, 134-139].

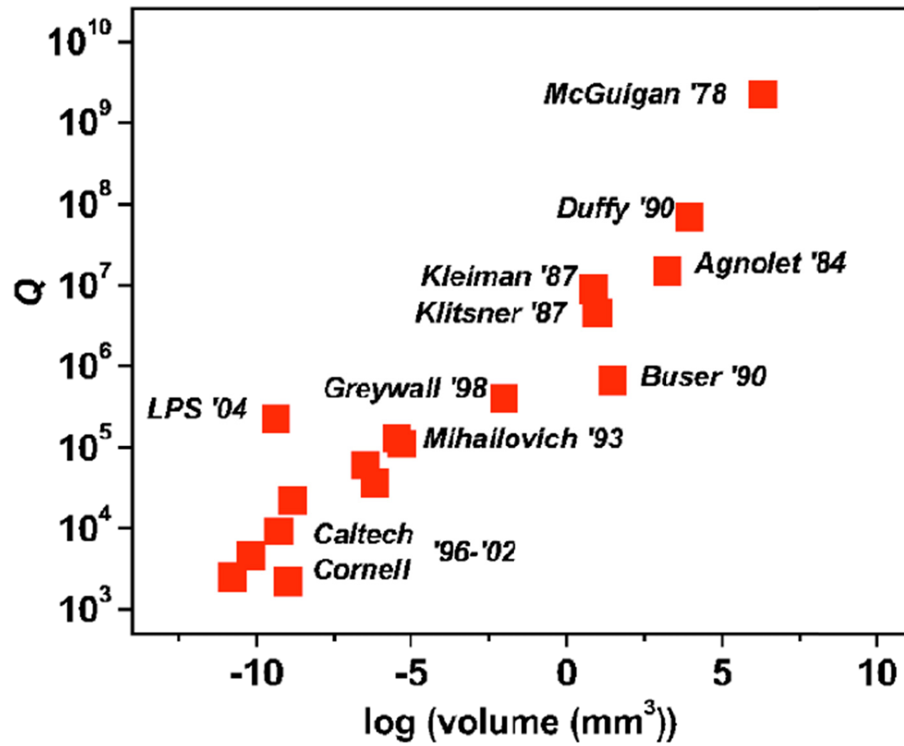

FIG. 32. Maximum reported Q factors in mechanical resonators varying in size from the macroscale to nanoscale. The data follow a trend showing a decrease in Q factor that occurs roughly with linear dimension, i.e., with increasing volume-to-surface ratio. Adapted from Ref. [133].

Here, we report a study on doubly clamped, VHF nanowire resonators with a dual-gate configuration that allows us to achieve integrated electrical actuation/detection, *in situ* frequency tuning and selective actuation of different vibrational modes. A representative device exhibits Q ~ 2200, which is among the highest achieved for doubly clamped nanotube or nanowire resonators at the time of this writing.

4.2: Device fabrication

The nanoscale mechanical element in our device is a suspended SnO_2 nanowire supported by two patterned Au pads at the bottom and clamped by a pair of Au electrodes at the top [Fig. 35(a)]. The Sb-doped SnO_2 nanowires were grown using a vapor transport process using high-purity (99.99%) Sn and Sb powders (200:1 weight ratio) as source materials and Au nanoparticles as catalysts [140, 141]. Fig. 33 shows a high-resolution transmission electron microscopy (HRTEM) image of a representative nanowire showing a smooth surface suitable for addressing surface-related dissipation mechanisms.

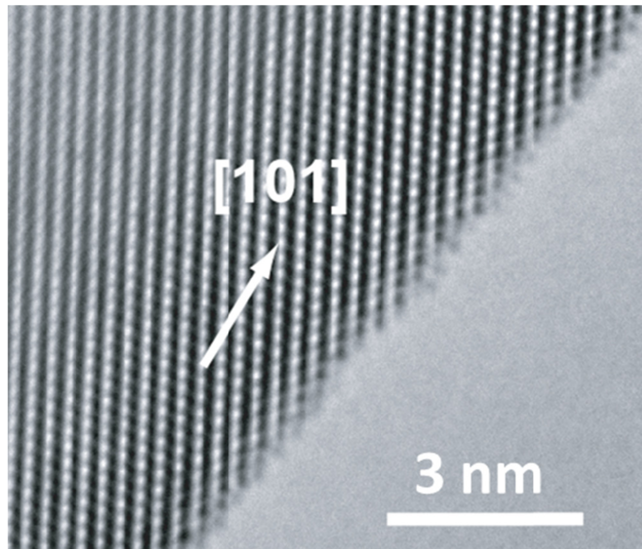

FIG. 33. HRTEM image of a SnO_2 nanowire showing a smooth surface.

The resonator devices were fabricated on a degenerately doped n-type silicon substrate capped with a 50-nm-thick layer of thermal silicon dioxide. First, 30-nm-thick Au pads with spacing ranging from 1.5 to 3 μm were defined using electron-

beam (e-beam) lithography followed by evaporation of Ti /Au (10/20 nm). Next, the nanowires were deposited over these pads by directly dry transferring the nanowires from the growth substrate [142]. This dry-transfer technique oriented the nanowires along the transfer direction and produced suspended nanowires with a reasonable yield and little slack or residual tension as verified below. After the suspended nanowires were located on a scanning electron microscope (SEM), a second e-beam lithography and lift-off process was carried out to form a pair of Ti/Au (10/400 nm) top electrodes that clamp the nanowire to the supporting pads. The two Ti/Au top electrodes further provide electrical contact to each device, with the degenerately doped Si substrate serving as a back gate (Fig. 34(a)). An optional third electrode situated adjacent to the suspended nanowire beam can also be fabricated and can serve as a local side gate (Fig. 34(b) and insets of Fig. 37).

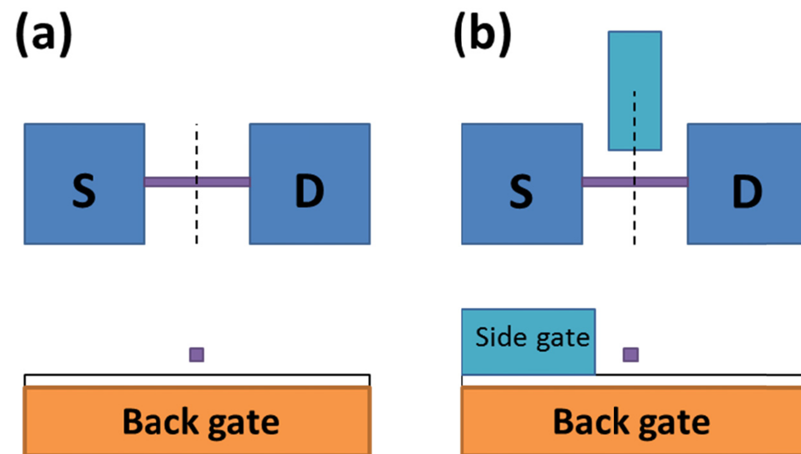

FIG. 34. Schematics of two configurations of doubly clamped nanowire resonator. (a) Substrate is used as global back gate. (b) With local side gate. Dashed lines are the slices at which the cross-sectional views are taken.

Critical point drying was employed during the lift-off processes to minimize slack formation [136]. Figure 35(a) shows a typical suspended nanowire resonator device clamped by the electrodes.

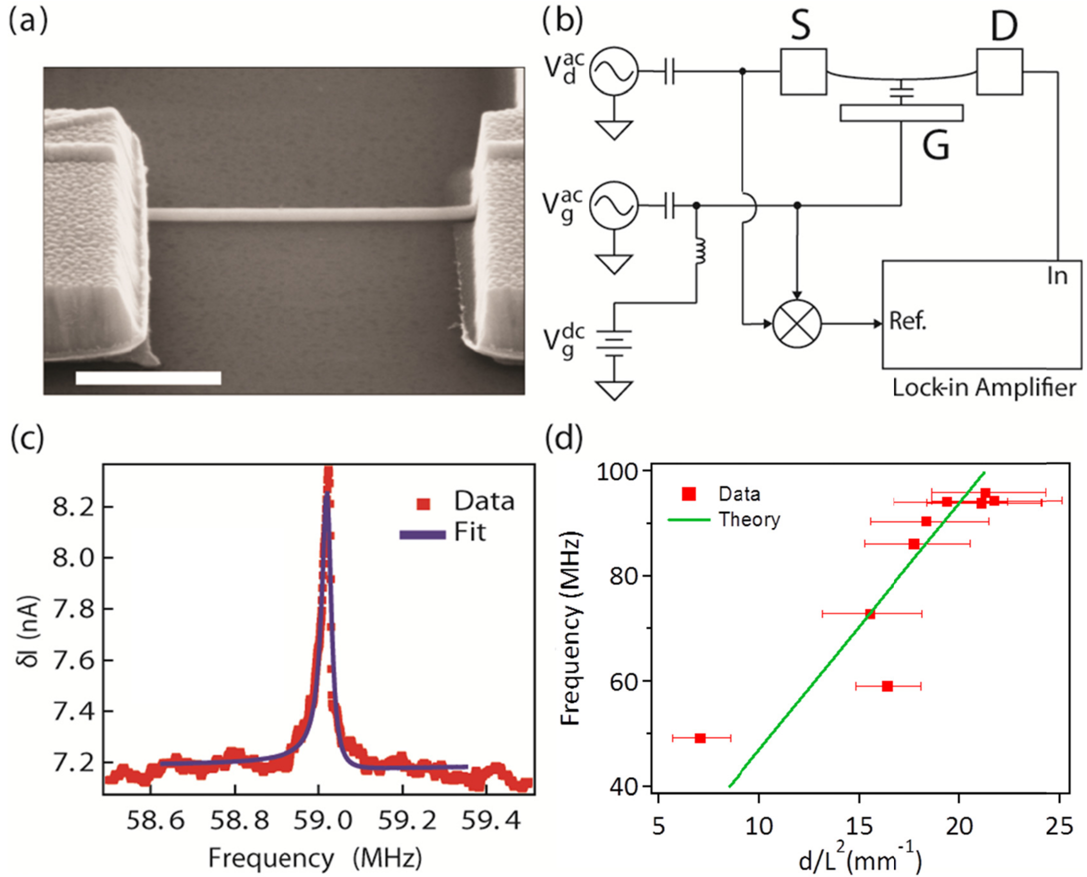

FIG. 35. (a) SEM image of a representative doubly clamped nanowire resonator. Scale bar: 1 μm. (b) Schematic of the double-source method. (c) Electrical readout from a typical device along with a Lorentzian fit. (d) Plot of f_0 vs geometry factor d/L^2 for nine devices. Also shown is the theoretical prediction from Eq. (1.1). The error bars represent measurement uncertainties in d ($\pm$5 nm) and L ($\pm$50 nm).

4.3: Electrical actuation/detection setup

The nanowire resonators were actuated capacitively from the gates and detected electrically using a scheme in which the nanowire itself, also configured as a transistor, serves as a mixer [136, 137]. In capacitive actuation, an electrostatic force is induced on the NW by applying an ac drive voltage at frequency ω either to the gate or one of the S/D electrodes. The resulting motion modulates the capacitance C between the nanowire and the gate. The changing capacitance is converted into an ac current signal at the drain, and is added to the ac current that is already present from normal transistor action. Since at high frequencies the ac current is not directly measurable because it escapes through the parasitic capacitances of the contact pads, a mixing signal with a frequency offset $\omega + \Delta\omega$ is applied at the drain contact so that the transistor will mix the signal of interest down to a low frequency that can be measured with a lock-in amplifier.

In the double source setup (Fig. 35(b)), the drive signal $v_g^{ac} = v_g \cos(\omega t)$ is applied to the gate and the mixing signal $v_d^{ac} = v_d \cos((\omega + \Delta\omega)t)$ is applied to the drain, and the resulting signal amplitude at mechanical resonance as measured by the lock-in amplifier is given by

$$\delta i\big|_{\omega=\omega_0} = \tfrac{1}{2}\mu\left(\tfrac{dC}{dz}\right)^2 \left(V_g^{dc}\right)^2 v_g v_d k^{-1} Q \ , \qquad (11)$$

where μ is mobility of the nanowire transistor, C and z are respectively the capacitance and distance between nanowire and gate, V_g^{dc} is the dc bias on the gate, and k and Q are respectively the spring constant and quality factor of the resonator. In

the single source setup, both the drive and mixing signals are provided at the drain via amplitude modulation: $v_d^{ac} = \left(1+\cos\left(\Delta\omega t\right)\right) v_d \cos\left(\omega t\right)$ and $v_g^{ac} = 0$. In this case, the resonance signal at the lock-in is given by

$$\delta i\big|_{\omega=\omega_0} = \tfrac{1}{2}\mu\left(\tfrac{dC}{dz}\right)^2 \left(V_g^{dc}\right)^2 \left(v_d\right)^2 k^{-1} Q\,, \qquad (12)$$

i.e. both methods give similar output amplitudes. All measurements were performed inside a vacuum probe station at room temperature at a pressure of ~ 10^{-5} Torr.

4.4: High Q achieved at room temperature and size scaling

The output signal for a typical nanowire resonator using this electrical actuation/detection method is shown in Fig. 35(c), along with a Lorentzian fit that yields a quality factor of Q = 2200 and resonant frequency f_0 = 59.0 MHz. The quality factor value measured at room temperature was among the best that have been reported on doubly clamped nanotube or nanowire resonators at the time of this writing [34, 135-139]. The force sensitivity of the nanowire resonator was estimated to be 1.4×10^{-13} N/Hz$^{0.5}$.

For the fundamental flexural mode of a suspended beam, the resonant frequency f_0 can be estimated as

$$f_0 = 1.03\frac{d}{L^2}\sqrt{\frac{E}{\rho}} \qquad (13)$$

where E is the Young's modulus, ρ is the mass density, d is the thickness of the beam in the direction of motion, and L is the length of the suspended region. In Fig. 35(d) we plot the dependence of f_0 as a function of the geometry factor d/L^2 for nine

devices (markers), along with the theoretical prediction (solid line) using $\rho = 7103$ kg/m^{-3} for bulk SnO_2, $E = 154$ GPa for SnO_2 nanobelts[143] and d and L values measured from direct SEM imaging. The good agreement with the data verified the feasibility to electrically actuate and detect the fundamental flexural mode of nanowire resonators using this approach. In addition, it indicates that our nanowire resonators behave as rigid beams with little residual tension or slack[144] and whose frequencies can be well predicted from parameters controlled during the fabrication process.

4.5: Nonlinear operation

In addition, the nanowire resonators can be readily driven into the nonlinear operation regime. This is due to the fact that the onset of nonlinearity occurs for small applied force (hence low input power) in large aspect ratio (e.g., one-dimensional) structures [138, 139, 144]. Fig. 36(a) shows the response of a typical nanowire resonator at different DC gate biases. At large drive amplitudes (high DC bias) the increase in tension results in a strong non-linear effect and lead to a bi-stable region manifested as hysteresis in the response-frequency curve (Fig. 36(b)), a state commonly known as a Duffing oscillator [145]. The critical amplitude a_c at which the resonator response becomes nonlinear can be calculated by fitting the resonance amplitude vs. frequency at different drive voltages and yielded $a_c = 13$ nm for the device in Fig. 4.5, corresponding to a driving force of 3.7×10^{-10} N. The small driving force puts a limit on the dynamic range (DR) of the nanowire resonator, but it has also been argued that non-linear operations may lead to novel applications such

as parametric amplification, sensing, and noise squeezing [146-148]. At very large aspect ratios, DR for a nanowire resonator may even become negative and the resonator is naturally a non-linear device [149]. The excellent control in the nanowire resonator system and the ability to produce nanowires down to atomic scale [84, 150] thus make it possible to systematically study the evolution of DR as a function of device geometry. By carefully designing the device parameters, either a large DR or a small a_c may be realized in the nanowire resonator system.

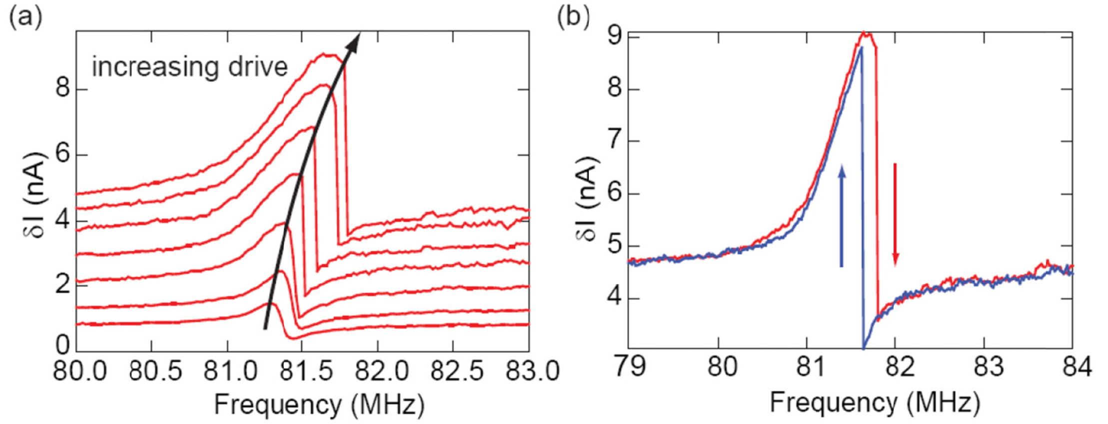

FIG. 36. Nonlinear response of a back-gated device. (a) Family of response curves as the ac gate drive V_g^{ac} is increased from 60 to 350 mV_{pp}, showing the evolution of the nonlinear response. (b) For V_g^{ac} = 350 mV_{pp} (top curve in (a)), a hysteretic response is observed depending on the direction of the frequency sweep. The double source method was used with V_g^{dc} = 6 V and V_s^{ac} = 30 mV_{pp}.

4.6: *In situ* frequency tuning

Besides providing a means to electrically actuate and detect the nanowire mechanical motion, the on-chip gates offer the capability to tune the resonant frequency f_0 of the nanowire resonators *in situ*. This feature can be used in applications such as NEMS-based tunable bandpass filters [129]. Gate induced frequency tuning can be attributed to either a capacitive softening effect (which reduces f_0) or elastic hardening effect (which increases f_0)[136, 144]. In this study we employed a dual-gate setup that enables us to study the two effects independently and show that the resonant frequency f_0 can be tuned up or down simultaneously by applying appropriate dc biases to the gates. The insets of Figs. 37(a) and 37(b) show a SEM image and a schematic of a device with the dual-gate setup consisting of a global back gate and a local side gate near the nanowire, respectively. The double source method was used in this study in which the ac drive signal V_g^{ac} was applied to the side gate and induced flexural motion inside the electrode plane (the "in-plane" motion). The main panels of Figs. 37(a) and 37(b) show the position of the resonant frequency f_0 (for this in-plane motion) as a function of the dc voltages applied to the bottom gate V_{back} and side gate V_{side}, respectively. It can be seen that the resonant frequency increases as the magnitude of V_{back} increases [Fig. 37(a)] while the opposite is true for the side gate bias V_{side} [Fig. 37(b)], thus allowing independent tuning of the frequency for the same vibrational mode.

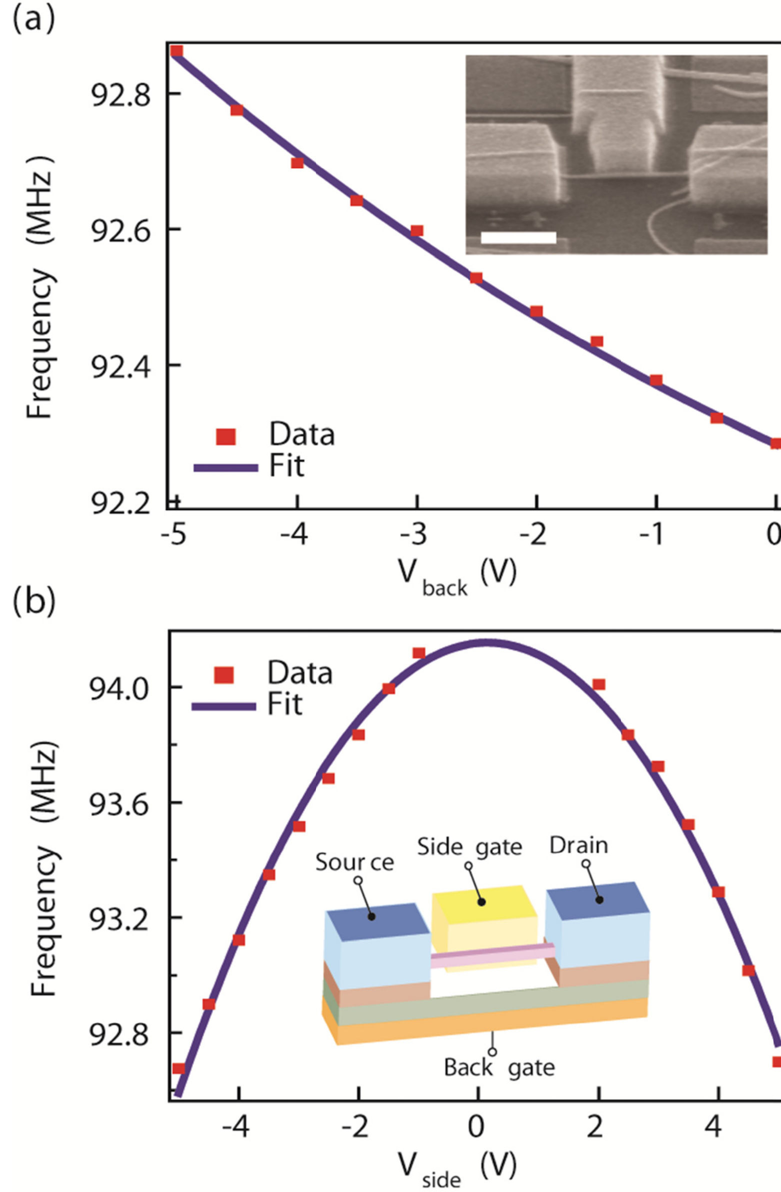

FIG. 37. *In situ* frequency tuning. (a) Resonant frequency f_0 of the in-plane motion vs varying dc bias on the back gate V_{back}, with V_{side} = 5 V. Inset: SEM image of the device. Scale bar: 1 μm. (b) f_0 of the in-plane motion vs V_{side} with V_{back} = 0 V. Inset: Schematic of the dual-gate configuration. The double source method was used to actuate the device with V_s^{ac} = 50 mV$_{pp}$, V_g^{ac} = 200 mV$_{pp}$ applied to the side gate and $\Delta\omega$ = 5 kHz.

4.6.1: Discussion of tuning mechanisms

The observed frequency tuning behavior can be attributed to two different mechanisms: the elastic hardening and capacitive softening of the spring constant[144]. When a dc voltage V_{back} is applied to the back gate, it pulls the beam toward the gate thus induces tension inside the nanowire resonator. This elastic hardening increases the resonant frequency and can be estimated from Eq. (14) when tension is not too large (in the so-called bending regime),

$$f_0^2 = f_0^{'2} + \frac{\pi^2 E Z_{dc}^2}{4\rho L^4}, \tag{14}$$

where Z_{dc} is the static displacement of the center of the beam and can be estimated from $Z_{dc} = F/k_{eff} = \left[\tfrac{1}{2}\left(dC/dz\right) L V_{back}^2\right] / \left(32Ed^4/L^3\right)$, where F is the static force of deflection and $C = 2\pi\varepsilon / \cosh^{-1}\left(2z/d\right)$ is the capacitance per unit length of a cylindrical wire with diameter d at a distance z from the gate. The resulting expression shows that in the bending regime, the resonant frequency depends on the gate voltage following $\sqrt{A + BV_{back}^4}$. Using measured parameters z, d, and L, the factor B can be calculated to be $\approx 1.7\times109$ $\mathrm{Hz}^2\,\mathrm{V}^{-4}$. This value agrees reasonably well with the fitting (solid curve) in Fig. 37(a), which yielded $B = 5\times10^8$ $\mathrm{Hz}^2\,\mathrm{V}^{-4}$, considering the uncertainties involved in the system. The corresponding dc deflection of the nanowire beam Z_{dc} was estimated to be ≈ 1 nm at maximum dc bias of 5 V.

On the other hand, if a dc voltage V_{side} is applied to the side gate, the electrostatic force is in the direction of the nanowire oscillation and the bias not only

creates tension but also induces a capacitive softening effect, which we show below can be dominating. Since the electrostatic force is proportional to dC/dz and is strongest but opposite to the elastic restoring force when the nanowire moves closest to the gate, and weakest but adding to the elastic force when the nanowire is furthest to the gate, the net result of the electrostatic force is a reduction ("softening") of the effective spring constant k_{eff} and results in a decrease in the resonant frequency. The k-softening effect can be calculated from

$$f_0^2 = f_0^{'2} - \frac{\frac{1}{2}\frac{d^2C}{dz^2}V_{side}^2}{\rho A}\frac{2}{(2\pi)^2}, \quad (15)$$

and affects f_0 in the form of $\sqrt{A'-B'V_{side}^2}$. Using only measured device parameters, the factor B' was calculated to be $\approx 6\times10^{12}\ \mathrm{Hz^2\,V^{-2}}$, agreeing again reasonably well with that extracted from the fitting in Fig. 37(b) which yielded $B' = 1\times10^{13}\ \mathrm{Hz^2\,V^{-2}}$.

In the back gate case, the electrostatic force is perpendicular to the motion of the beam and induces tension effects only. However in the side gate case, the electrostatic force is in the direction of the beam motion and will in principle induce both the *k*-softening and tension effects. To compare the two effects, we calculated the expected shifts in f_0^2 for the side gate over a 10 V span using measured device parameters. It was found that for the side gate the softening effect is about 20 times larger than the hardening effect, thus explaining the observed decrease in resonant frequency. However, due to its stronger dependence on V_{side} the tension effect will eventually dominate at larger biases (e.g., for $V_{\mathrm{side}} > 45\ \mathrm{V}$).

4.7: Selective actuation of different vibrational modes

The dual-gate setup not only leads to greater freedom in frequency tuning but also provides the capability to selectively actuate the nanowire resonator in different modes of vibration. Figure 38(a) shows a frequency scan of the same device using the single source method, with $V_{side} = 5$ V and $V_{back} = 0$ V. Since the driving force is proportional to the dc component of the electric field[136, 137], this configuration mainly excites the in-plane motion of the nanowire resonator. Indeed, while two resonance peaks at f_1 = 81.4 MHz and f_2 = 92.6 MHz were observed, from Lorentzian fits the amplitude of the f_2 peak was about twice that of the f_1 peak. We therefore attributed the f_2 peak to the in-plane mode and the f_1 peak to the out-of-plane mode. When the gate voltages were exchanged so that the side gate was grounded and the back gate was biased at 5 V [Fig. 38(b)], the size of the f_1 peak (out-of-plane motion) became much larger than the f_2 peak (in-plane motion). Thus, by changing the dc bias configurations one can selectively excite one mode over the other. This capability, combined with the frequency tuning capability, can potentially utilize the coupling effects of different vibrational modes to enable parametric amplification and dynamic range enhancement [151, 152] (e.g. for sensing applications). In addition, the difference in frequency between the two peaks observed here implied that the nanowire does not have a perfectly square cross section. From Eq. (13) the thickness of the nanowire was estimated to be 6 nm smaller than its width.

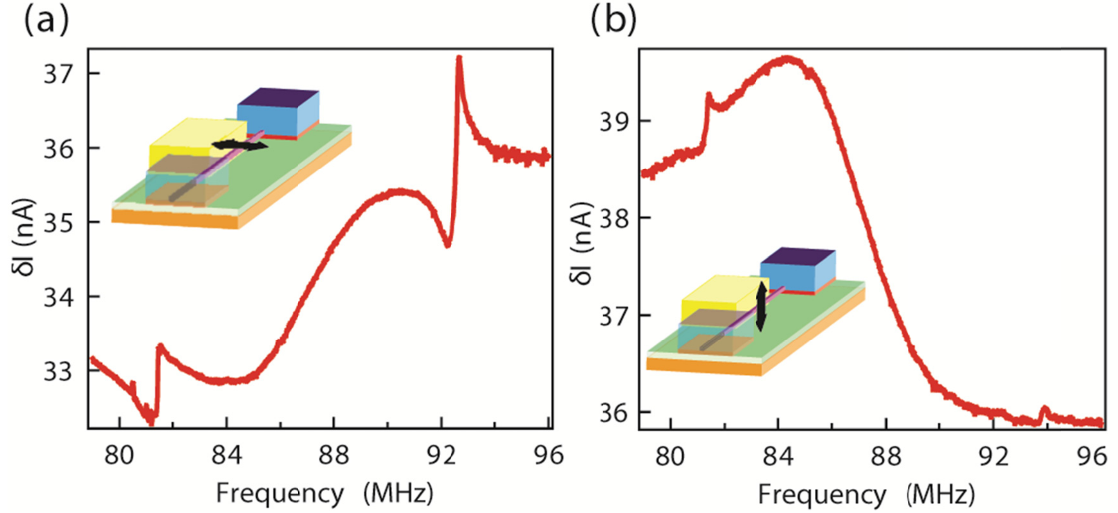

FIG. 38. Selective actuation of in-plane and out-of-plane modes. (a) Electrical readout of the device at bias configurations of $V_{side} = 5$ V and $V_{back} = 0$ V. (b) Electrical readout of the device at bias configurations of $V_{side} = 0$ V and $V_{back} = 5$ V. The peaks at 81.4 and 92.6 MHz correspond to the out-of-plane and in-plane vibrational modes, respectively. The single source method was used with V_s^{ac} = 500 mV_{pp} and 100% amplitude modulation at 5 kHz. The insets show the schematics of the vibrational modes.

4.8: Summary

In summary, we report the electrical actuation and detection of semiconductor nanowire-based very-high frequency mechanical resonators. A representative device exhibits Q ~ 2200, which is among the highest achieved in nanowire-based NEMS resonators. The devices can be driven into nonlinear operation. By adjusting the gate configuration in a dual-gate setup, the resonant frequency of our nanowire resonators can be tuned *in situ* either up or down. In

addition, different vibrational modes can be selectively actuated. These results will provide valuable insight into the understanding and future applications of nanowire-based NEMS.

Chapter 5

Conclusion

In this work, we have achieved some experimental advances toward realizing the full technological potential of semiconductor nanowires. Here we will summarize our main results, make general comments, and discuss the work that remains to be done in the future.

5.1: Nanowire growth techniques for hybrid nanowire-CMOS systems

Semiconductor nanowires have excellent properties that could be beneficial for high performance CMOS devices, tight critical thickness control, ultra-smooth surfaces, and cylindrical geometry suitable for gate-all-around structures. Integrating them with CMOS is a challenging primarily due to their bottom-up growth technique which radically departs from traditional top-down processing. We have developed nanowire growth techniques that should be beneficial toward hybrid nanowire-CMOS systems.

We have demonstrated the growth of small-diameter Si nanowires using Al (instead of Au) as catalyst. Previous studies have shown only nanowires with a high level of unintentional Al doping, while here we have shown that semiconducting

behavior can be recovered at small diameters. However, the unintentional p-doping even in small diameter nanowires is significant, and hence further investigation is warranted. This may include TEM analysis, post-growth annealing steps, and/or selective surface etching to remove surface dopants. Another issue is diameter control. Researchers generally use Al thin films since Al nanoparticles spontaneously combust in the presence of oxygen. But achieving uniform droplet diameters may be difficult using a thin film as a starting point. In the future, Al nanoparticles could be used, provided that an experimental apparatus (such as a glove box) is designed to prevent oxygen exposure during the deposition of nanoparticles on a substrate, as well as during the loading of the substrate into the nanowire growth furnace. Alternatively, an Al film could be patterned into discs, although the final droplet size would be too small (< 30 nm) for standard photolithography to pattern directly.

We have also demonstrated the vertical epitaxial growth of Ge nanowires on Si with high yield with a diameter of 20 nm, which is smaller than what previous studies have achieved; 20 nm is a technologically important size for reasons both practical and theoretical. We have also demonstrated some refinements to the basic growth process, including post-growth Au catalyst removal. We have shown that a buffer layer can enhance vertical and nucleation yields, enabling the location control of vertical Ge nanowires. In the future, work should continue along this trajectory. Methods to pattern the vertical nanowires on the buffer layer (e.g. via charge patterning of Au nanoparticles) should be investigated. Also, at the time of this writing we believe it should also be possible simultaneously to lower the deposition temperature of the buffer layer to a more CMOS-compatible level (< 450 °C)

without sacrificing growth yield, and to heavily dope the layer so it can serve as a device contact.

5.2: Toward a Ge nanowire-based vertical tunnel FET

We have demonstrated high performance Esaki diodes using the heterojunction at the interface between a vertical Ge nanowire and a Si substrate. The temperature dependence of these devices indicates a heterojunction that contains low defects. We have shown that vertical Ge nanowire growth can be achieved on Si nanopillars, freeing up the potential for optimal gate alignment in a tunnel FET device. We have shown that vertical growth can be achieved at sub-eutectic temperatures, and this is anticipated to counter the reservoir effect inherent in VLS growth, enabling the sharpest heterojunctions for higher gate coupling. In the future, careful TEM analysis of the Ge nanowires grown on Si nanopillars at 320 °C should be done. The sharpness of the dopant profile and the Ge-Si interface should be evaluated. Also, tunnel diodes using the nanowire-nanopillar structure should be fabricated and tested. Once ultrasharp heterojunctions are realized, a prototype tunnel FET should be fabricated and tested.

Finally, we have made progress toward fabricating vertical FET devices, and fabrication of the vertical junctionless FET should continue in the future. It is anticipated that surface states in the gate stack may need to be addressed, so that passivation strategies should be investigated. Once the vertical junctionless FET has been realized with sufficiently high performance, we can use the same fabrication techniques to realize the tunnel FET.

5.3: Nanowire-based NEMS

We have demonstrated doubly clamped nanowire resonators with quality factor ~2200, on-chip electrical actuation/detection, *in situ* frequency tuning, nonlinear operation, and selective actuation of different vibrational modes. These results can potentially be used to enable applications of nanowire-based NEMS. High Q is of paramount importance in many applications including ultrasensitive mass and force sensing [31-35], ultra-low-power frequency domain signal processing [129], and quantum measurement [36-38]. Frequency tuning is useful for applications such as tunable bandpass filters [129]. The nonlinear response is useful for parametric amplification, sensing, noise squeezing, and mechanical logic [146-148, 153, 154]. The selective actuation of modes can be used to study mode coupling effects, which potentially can be used for parametric amplification and dynamic range enhancement [151, 152] (e.g. for sensing applications), as well as highly condensed mechanical logic [155].

In the future, the quality factor of our devices needs to be improved significantly. The nature of the main loss mechanism is currently unclear. Clamping loss is one possibility, in which case, to this end, resonators can be fabricated using nanowires that are alloyed to their end supports, via epitaxial growth. Another possibility is surface-related loss, in which case a treatment such as high temperature annealing may help remove surface defects. Also, it has been shown [156] that the application of tensile stress to a doubly clamped beam increases the quality factor, although the mechanism by which this occurs is unclear (it is presumed that tension

increases the acoustic impedance mismatch between the oscillating beam and the clamping support structures). NEMS is a much less mature technology than nanoelectronics. To exploit the excellent intrinsic properties of nanomaterials such as nanowires, the technology for manipulating and anchoring them, and measuring their mechanical properties, needs to mature significantly to minimize external loss mechanisms (such as back-action and clamping losses).

5.4: Final remark

We note that underlying our work with Si and Ge nanowires is the constant need to remove native oxide. The epitaxial growth of Si nanowires was not discovered until the source gas was switched from SiH_4 to $SiCl_4$, where chlorine was more effective at removing SiO_2 than hydrogen. Similarly, the addition of HF to the colloid of Au nanoparticles proved to be critical for promoting high-yield epitaxial growth of Ge nanowires on Si. Also, the VLS growth of Al-catalyzed Si nanowires was not discovered until high partial pressures of hydrogen were used to remove native aluminum oxide (initial studies used oxygen-free vacuum environments). Finally, we speculate that our work with Ge nanowires (buffer layer, *ex situ* Si shell deposition, vertical FET fabrication, etc.) largely took advantage of the fact that Ge oxide is very easy to remove (it evaporates at temperatures > 400 °C, and is easily removed using hydrogen annealing); otherwise the laboratory resources available at the time of writing might not have have allowed us to make our achievements. In light of these observations, ideally one would like to prevent samples from being

exposed to oxygen during processing. Perhaps future fabrication tools that accommodate nanowire-based devices could be designed with this in mind.

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