Bismuth Telluride and Antimony Telluride Based Co-evaporated Thermoelectric Thin Films: Technology, Characterization, and Optimization

by

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To my parents.

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Abstract

Bismuth Telluride Antimony Telluride Based Co-evaporated Thermoelectric Thin Films: Technology, Characterization, and Optimization

by

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Co-Chairs: Khalil Najafi and Rebecca L. Peterson

Thermoelectric (TE) materials have been widely investigated and used in a variety of systems such as solid-state coolers, infrared detectors, and power generators. Integration of TE thin films in micro-scale systems offers advantages such as integration, size, and weight for many new applications. In order to provide design flexibility for thermoelectric microsystems, high-quality TE thin films with good adhesion and uniformity are needed on a variety of substrates. Motivated by the applications of TE materials in microsystems, the goal of this dissertation is to explore the technology and characterization of co-evaporated high quality (Bi,Sb)Te-based thin films on various substrates.

Thermal evaporation is an attractive thin film deposition technique because of its relative simplicity, reproducibility, ease of process control, and high throughput. Characterization techniques are applied to a variety of TE films in order to enhance physical understanding of the effects of deposition conditions, substrate material/crystallinity, and substrate preparation on film properties. This dissertation shows that the grain size, composition, and TE properties of thin films depend strongly on the co-evaporation process conditions including substrate material, deposition substrate temperature, and elemental flux ratio. Our results show that maximum power factors are achieved on Poly-Si and Kapton® substrates at T_{sub}= 270 °C for *n*-type Bi_2Te_3 films, and on oxide and poly-Si substrates at T_{sub}= 250°C for *p*-type Sb_2Te_3 films. The optimum (Bi,Sb)Te-based binary films have tellurium atomic percentage of about 60%.

This work moves beyond co-evaporation of binary alloys towards advanced thermoelectric films of ternary alloys. It demonstrates co-evaporation as a low-cost process for the deposition of telluride-based ternary films for the first time.

One of the main challenges in devices using TE thin films compared to bulk material is the increasing importance of contact resistance. Contact resistance can cause major degradation in TE microsystems performance. In this dissertation, test structures are introduced with novel material-shape combinations for minimization of electrical contact resistivity between (Bi,Sb)Te-based thin films and various contact metals. Characterization of resistivity based on the contact material, physical structure, and surface treatment facilitates control and reduction of electrical contact resistance.

Chapter 1

Introduction

With the advent of micro-scale devices and the increasing popularity of ubiquitous micro-electromechanical platforms, one of the most critical challenges moving forward, is to find environmentally-friendly energy sources to replace conventional means of supplying power. For power generation and cooling applications, the thermoelectric effect has the advantages of reliability, silent operation due to the absence of moving mechanical parts, as well as being environmentally friendly. The thermoelectric phenomenon is described as the conversion of thermal energy into electrical energy or vice-versa. This conversion is based on three important transport effects: the Seebeck effect, the Peltier effect and the Thomson effect. Chapter 2 discusses these effects in more details. Thermoelectric (TE) materials have become a popular research area over the past several years due to their unique characteristics and applications. The energy efficiency of thermoelectric devices such as solid-state coolers and power generators, as described in Chapter 2, is primarily determined by the performance of their TE materials.

Despite the advantages of thermoelectric technology, the efficiency of thermoelectric devices is still not high enough for many applications. Telluride-based alloys are well-known room temperature TE materials with a high thermoelectric figure of merit (ZT) in comparison to other materials. During the past decade, novel material systems such as

Skutterudites [50,56], superlattices [46,91] and nano-structured films [47,83] have been developed to achieve higher values of *ZT* by decreasing lattice thermal conductivity. These materials usually require complex and expensive processing technology or have been optimized for use at high temperatures. Therefore, for many applications, the best thermoelectric materials near room temperature are still (Bi,Sb)Te-based alloys.

Traditional thermoelectric systems employ these alloys in bulk form, which is not appropriate for highly integrated systems due to its mechanical limitations during fabrication of micro-scale devices [42]. Therefore, there is a need to develop high-quality TE thin films, with figures of merit comparable to bulk materials and compatible with micro-fabrication processing. On the other hand, the development of thermoelectric thin films for microsystem applications presents many challenges and complications.

The first challenge is that current state-of-the-art microsystems usually use very complex and expensive deposition techniques to achieve high-quality TE films. In addition, optimizing TE thin film properties for a specific substrate limits microsystem design flexibility. However, switching a substrate based on a new application and device structure causes new issues for (Bi,Sb)Te-based thin films. There will be variation in TE thin film adhesion, stress, and optimal co-evaporation conditions. Thus, developing high-quality TE thin films with good uniformity and adhesion on a variety of substrates is crucial to sustain future success in fabrication and applications of novel thermoelectric microsystems.

In addition, using thin films instead of bulk materials increases the importance of contact resistance when the TE material is integrated with metal contacts in microsystems. As the thickness of a TE film decreases, its resistance becomes comparable to the contact

resistance, limiting the conversion efficiency and degrading the overall device performance.

In this dissertation, to address these challenges, the optimization of thermal co-evaporation as a fairly simple, reliable, non-expensive and high-throughput deposition method for (Bi,Sb)Te-based thin films is investigated. The effects of using various substrate materials and crystal structures on TE thin films, in addition to deposition conditions for optimal thermoelectric performance of each thin film are also studied. Furthermore, this dissertation moves beyond co-evaporation of binary alloys towards more advanced thermoelectric ternary alloy films. In bulk, alloying Bi_2Te_3 with Sb_2Te_3 can improve the figure of merit in thermoelectric materials above the reported values for binary compounds due to thermal conductivity reduction via mass defect scattering. Furthermore, bulk ternary alloys have been shown to be less sensitive to crystal orientation and the stoichiometric ratios of individual compounds in the alloy. This thesis is the first work demonstrating that thermal co-evaporation is a low-cost and suitable process for the deposition of telluride-based ternary films with good thermoelectric qualities.

Finally, this work shows that it is possible to minimize metal/TE contact resistivity by employing various metal-shape pairings and substrate treatment before TE deposition and annealing.

The following section discusses various thermoelectric applications in microsystems and an overview of thermoelectric micro-scale devices. It provides a comparison of various thermoelectric devices that have been developed to date, and discusses the contributions this work makes to the state of the art.

1.1. Thermoelectric Microsystems Applications

1.1.1. Thermoelectric Micro Coolers

The operation of thermoelectric coolers is based on the Peltier effect, which is discussed in Chapter 2. Despite not having the same cooling performance as conventional refrigerators, these devices are appealing in applications where small size and quiet operation are important. They can also be useful when standard AC power is not available but DC power is. Although thermoelectric cooling is not very efficient for macro-scale applications, it has become appealing at the micro-scale, due to its maintenance-free, solid-state operation, and small size. Micro thermoelectric coolers can

Reference	Cooling ΔT (K)	Ambient temperature T_H (°C)	Power Consumption (mW)	Structure	Material
Huang [53]	5.6	-	844	1-stage vertical	*n*-type poly-Si *p*-type poly-Si
Fan [27]	12	200	-	1-stage vertical	*p*-type Si/SiGe superlattice
Böttner [8]	48	85	-	1-stage vertical	$(BiSb)_2Te_3$ $Bi_2(SeTe)_3$
Bulman[10]	55	-	362	1-stage vertical	*p*-type Bi_2Te_3/Sb_2Te_3 *n*-type $Bi_2Te_3/Bi_2(SeTe)_3$
Bulman [11]	102	-	28.11×10^3	3-stage vertical	*p*-type Bi_2Te_3/Sb_2Te_3 *n*-type $Bi_2Te_3/Bi_2(SeTe)_3$
Goncalves[39]	5	-	0.33	1-stage lateral	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3
Da Silva[20]	1.3	62	41	1-stage vertical	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3
Gross [41,42]	22.3	-	24.8	6-stage lateral	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3

Table 1.1 Comparison of state-of-the-art thermoelectric micro-coolers:

have a major impact on critical medical and consumer applications including substantial performance improvement of existing systems such as infrared detectors. Additionally, the quality factor of MEMS resonators and the thermal noise in circuits such as low-noise amplifiers and sensor buffers improve significantly at reduced temperature. Performance of state of the art thermoelectric micro coolers is compared in Table 1.1.

1.1.2. Thermoelectric Micro Generators

The growth of micro-scale implantable biomedical systems, wireless sensor networks, and portable consumer products has increased the demand for on-site, small volume, and replacement-free energy sources as an alternative to conventional electrochemical batteries. On-site energy scavenging techniques from various environmental sources including ambient heat, solar energy, and vibrations have been introduced as efficient and promising approaches. Among various energy scavenging techniques, micro thermoelectric generators, which convert waste heat to electrical energy, are becoming

Reference	Output Power (μW)	ΔT (K)	Power density (μW/cm^2)	Structure	material
Kishi (Seiko) [58]	22.5	3	3.6	vertical	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3
Snyder [86]	1	-	40	vertical	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3
Glatz [38]	0.0035	20	0.01346	vertical	Cu/Ni
Böttner [7]	0.0035	9	0.3125	vertical	*n*-type Bi_2Te_3 *p*-type $(BiSb)_2Te_3$
Weber [94]	4	11	18.5185	vertical	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3
Qu [73]	-	30	-	vertical	*n*-type Bi_2Te_3 *p*-type Sb_2Te_3
Ghafouri [32]	1.2	11	15	Lateral	*n*-type $Bi_2(SeTe)_3$ *p*-type $(BiSb)_2Te_3$

Table 1.2 Comparison of state-of-the-art micro-thermoelectric generators: structure, material and performance

more and more popular. Their operation is based on the Seebeck effect, which converts a temperature difference directly into an electric potential difference. Despite the high cost and low efficiency of micro thermal harvesters, their reliability due to the absence of moving parts and their silent operation makes them the platform of choice in many energy scavenger systems. Several approaches to build micro thermoelectric generators using a variety of TE materials have been developed in the past. Table 1.2 summarizes these generators and their performance.

1.2. Dissertation Contributions and Outline

The motivation for this dissertation lies in the emergence of many new TE applications in microsystems and the complications experienced while integrating TE thin films in different microsystem platforms. In order to address the challenges associated with developing thermoelectric thin films for microsystems, this dissertation makes the following contributions:

1. Optimization of binary alloys (Bi_2Te_3 and Sb_2Te_3) thin film characteristics prepared by co-evaporation and investigation of the effects of substrate materials on their properties.
2. Development of a set of characterization techniques and experiments to understand and optimize deposition condition effects on film properties.
3. Introducing co-evaporation as an effective technique for development of telluride-based ternary films.
4. Minimizing metal/TE film contact resistivity by investigation of various metal-shape pairings and substrate treatment before TE deposition and annealing.

The following chapters of this dissertation will present development, characterization and

optimization of (Bi,Sb)Te-based thin films in microsystems. In Chapter 2, principles of thermoelectric phenomenon for power generation and cooling are discussed. An overview of various thermoelectric materials used at both macro and micro scales, the unique structure of tetradymite-type (Bi,Sb)Te-based compounds, and the motivation to move towards the development of thin film TE materials are described. In addition, an overview of the state-of-the-art TE thin film deposition techniques is reviewed.

Chapter 3 presents detailed description of co-evaporation system used to deposit (Bi,Sb)Te-based materials. The principles and technology of thin film physical vapor deposition are also discussed. Furthermore, experimental techniques for growth and characterization of co-evaporated (Bi,Sb)Te-based thin film compounds are presented. The effect of various deposition parameters such as substrate material, substrate temperature during deposition and elemental evaporation flux ratio on TE film properties are investigated. A customized procedure for measurement of thin film transport properties is described in detail. Various techniques for characterizing crystal structures, composition and mechanical properties of thin films are described.

Chapter 4 presents a comprehensive analysis of the binary (Bi_2Te_3 and Sb_2Te_3) thin film optimization process and compares their performance with previously reported values in literature. The effects of substrate material and crystal structure on the properties of TE thin films are discussed. In addition, optimization of thermoelectric properties of Bi_2Te_3 and Sb_2Te_3 on each substrate and possible issues with deposition of thin films on different substrates are described.

Chapter 5 introduces co-evaporation as an effective method for deposition of ternary $(BiSb)_2Te_3$ compounds. Ternary alloys have exhibited higher figures of merit compared

to binary compounds, however, co-evaporation has not been used for deposition of these thin films before. Initial data on $(Bi,Sb)_2Te_3$ alloys show the feasibility of thermal co-evaporation as a low-cost, high-throughput, and CMOS-compatible deposition method for developing (Bi,Sb)Te-based ternary thin films.

In Chapter 6, minimizing the contact resistivity between metals and TE thin films in microsystems is investigated by development of test structures for different contact shape and contact metals. The effect of substrate treatment before thin film deposition and post-deposition annealing is also discussed.

Chapter 7 presents directions for future work and improvements to the technology for (Bi,Sb)Te-based thin films, and provides a conclusion and summary of this dissertation.

Finaly, The design and fabrication of a micro-scale thermoelectric energy harvester using bulk (Bi,Sb)Te-based material is presented in Appendix A. This device is meant to use for harvesting energy from temperature difference between a beetle's body and the enviroment.

Chapter 2

Introduction to Thermoelectric Materials and Thermoelectric Thin Film Deposition

This chapter introduces basic principles of thermoelectric phenomenon and various thermoelectric materials used at both macro and micro scales. It describes the unique structure of tetradymite-type (Bi,Sb)Te-based compound semiconductors and the motivation to move towards the development of thin film Sb_2Te_3 and Bi_2Te_3 materials.

In order to clearly understand the reasons for studying (Bi,Sb)Te-based TE thin films, this chapter presents an overview of thermoelectric properties and their effect on TE material quality and performance. Furthermore, it summarizes properties of several important state-of-the-art thermoelectric materials. Finally, it gives an overview of various thermoelectric deposition techniques.

2.1. Principles of Thermoelectrics

2.1.1. Seebeck, Peltier and Thomson Effects

Seebeck Effect: In 1821 Thomas Johann Seebeck, the German physicist, first discovered the Seebeck effect. Seebeck first detected that a compass needle deflected when placed in the vicinity of a closed loop formed of two dissimilar metals with a temperature

difference between the junctions. This observation provides direct evidence that a current flows through the closed circuit driven by the temperature difference. A temperature difference causes charge carriers (electrons or holes) in the material to diffuse from the hot side to the cold side. Mobile charge carriers migrate to the cold side and leave behind their oppositely charged and immobile nuclei at the hot side thus giving rise to a thermoelectric voltage. The buildup of charge carriers on the cold side eventually ceases when an equal amount of charge carriers drift back to the hot side as a result of the

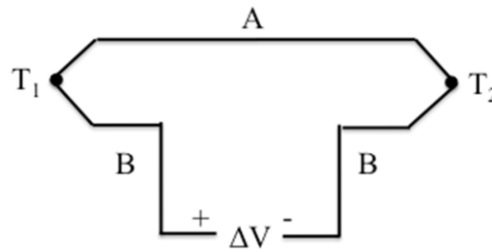


Figure 2.1. Seebeck effect: A temperature difference create a potential difference for the junction between materials A and B

electric field created by the charge separation. At this point, the material reaches steady state. Only an increase in the temperature difference can resume a buildup of more charge carriers on the cold side and thus lead to an increase in the thermoelectric voltage. The voltage, called the thermoelectric *emf*, is generated by a temperature difference between two different materials (A and B) such as metals or semiconductors as shown in Equation (2.1)[59]:

$$\Delta V = (\alpha_A - \alpha_B)\Delta T, \tag{2.1}$$

where, α_A and α_B are the Seebeck coefficients of materials A and B, respectively. This drives a continuous current flowing through the conductors if their junctions are kept at different temperatures. In case of an open circuit as shown in Figure 2.1, the charge

gradient due to the diffusion current will result in the buildup of an electric field, until drift current in the opposite direction is equal to the diffusion current. The Seebeck coefficient of a material defines the strength of the electric field generated by a given temperature gradient in the material.

Peltier Effect: Transport of heat through a sample due to electrical current is called the Peltier effect. This effect was first observed in 1834 by Jean Peltier. The Peltier effect is the underlying foundation for thermoelectric refrigeration and can be regarded as the reverse of the Seebeck effect. When an electric current passes through two dissimilar materials such as metals or semiconductors that are connected at two junctions, heat will be absorbed at one junction and liberated at the other junction. As a result, one junction cools off while the other heats up, depending on the direction of the current. The Peltier coefficients represent how much heat current is carried per unit charge through a given material. The Peltier heat (*Q*) absorbed by the cold junction per unit time is given by [59]:

$$\frac{dQ}{dt} = (\Pi_A - \Pi_B)I \tag{2.2}$$

In this equation, Π_A and Π_B are the Peltier coefficients of materials A and B.

Thomson Effect: The Thomson effect was predicted and subsequently experimentally observed by William Thomson (Lord Kelvin) in 1851. It refers to the emission or absorption of heat by a current carrying conductor exposed to a temperature gradient. If a current density J passes through a homogeneous conductor, heat production per unit volume q is [59]:

$$q = \rho J^2 - \mu J \frac{dT}{dx} \tag{2.3}$$

In this equation, ρ is the electrical resistivity of the material, dT/dx is the temperature gradient along the conductor, and μ is the Thomson coefficient. The first term in Eq. (2.3), ρJ^2, represents the Joule heat per unit volume, which is not reversible. The second term, $\mu J \frac{dT}{dx}$, is the Thomson heat, whose sign alternates when current flux, J, changes direction. The Thomson coefficient, μ, is related to the Seebeck coefficient by the following equation:

$$\boldsymbol{\mu = T \frac{d\alpha_s}{dT}} \tag{2.4}$$

2.1.2. Thermoelectric Figure of Merit

The key parameters that determine the quality of a thermoelectric material for cooling or power generation are the Seebeck coefficient, thermal conductivity, and electrical resistivity. The Peltier coefficient is simply the Seebeck coefficient scaled by temperature. Similarly, the Thomson coefficient can be derived from the Seebeck coefficient if its value is known over of a range of temperatures. In the early 1900s, E. Altenkirch introduced the concept of thermoelectric figure of merit. It revealed that good thermoelectric materials should have low electrical resistivity to minimize Joule heating, low thermal conductivity to maintain a large temperature gradient, and high Seebeck coefficients for maximum conversion of heat to electrical power or electrical power to cooling performance. The relationship between these properties can be quantitatively expressed by the thermoelectric figure of merit, Z, defined as [59]:

$$\boldsymbol{Z = \frac{\alpha_S^2}{\rho . \kappa}} \tag{2.5}$$

Since Z has a unit of K^{-1}, the dimensionless figure of merit ZT is often used as the measure of a material's thermoelectric performance. The optimization of ZT is not simply possible by optimizing the relevant individual material properties, i.e. Seebeck coefficient, electrical and thermal conductivities. These material properties are inter-related, so optimizing one can have a negative effect on the others. In particular, carrier thermal conductivity and electrical resistivity are related through carrier concentration as well as carrier mobility and at a given temperature have a constant ratio based on the Wiedemann–Franz law [59].

$$\frac{\kappa}{\sigma} = LT, \qquad L = \frac{\pi^2}{3}\left(\frac{\kappa_B}{e}\right)^2 = 2.45 \times 10^{-8}\frac{W\Omega}{K^2} \qquad \textbf{(2.6)}$$

where, κ_B is the Boltzmann constant and e is the electron charge Theoretical and experimental studies of solid-state materials have indicated that some semiconductors have relatively high power factor (α^2/ρ) and low thermal conductivity, which makes them a perfect fit for use in high ZT materials. However, semiconductors are not immune to the relations between various thermoelectric material properties. Both the Seebeck coefficient and resistivity are related to the separation between the conduction band in *n*-type (valence band in *p*-type) and the Fermi level of the material. As a result, attempts to raise the Seebeck coefficient by manipulating the Fermi level usually result in increases in resistivity as well. On the other hand, doping the material to increase electrical conductivity decreases Seebeck because the Fermi level is moved close to the corresponding band edge or even into the band itself. Therefore, it is critical to find a doping level where the power factor is optimized. In order to reduce thermal conductivity, the common approach is to introduce additional short-range disorder into

the crystalline structure. On the other hand, the distortion inevitably blocks charge transport, which may reduce electrical conductivity.

2.1.3. Seebeck Coefficient

The Seebeck coefficient of a material is a measure of the induced thermoelectric voltage produced by a temperature difference across its ends. The Seebeck coefficient is given by [59]:

$$\boldsymbol{\alpha_S = \frac{8\pi^2\kappa_B^2}{3eh^2} m^* T (\frac{\pi}{3n})^{2/3}} \quad , \tag{2.7}$$

where, κ_B is the Boltzmann constant, e is the electron charge, h is the Planks constant, m^* is the effective mass, T is the temperature, and n is the carrier concentration. Based on this equation the Seebeck coefficient is negative if carriers are electrons, positive if they are holes, and its maximum is achieved for large effective mass and low carrier concentration. In semiconductors, which are known to have high Seebeck coefficients, this relation can be defined based on the band model:

$$\boldsymbol{\alpha_S = -\frac{\kappa_B}{e}\left[(\frac{5}{2} + s) + \ln\frac{2(2\pi m^*\kappa_B T)^{3/2}}{h^3 n}\right]} \quad . \tag{2.8}$$

Here, S is the scattering parameter, assuming that the carrier relaxation time can be expressed in terms of carrier energy in a simple way ($\tau = \tau_0 E^S$, where τ is the carrier relaxation time, E is the carrier energy and τ_0 is a constant).

It can be seen that the Seebeck coefficient is inversely related to the carrier concentration in a semiconductor. Equation 2.8 is for n-type semiconductors with electron carriers, but the same relation stands for p-type TE semiconductors as well.

2.1.4. Electrical Resistivity

The other factor that influences TE material figure-of-merit is electrical resistivity (ρ). The material resistivity, with units of Ω-m, is given by:

$$\boldsymbol{\rho = {}^{1}/_{\sigma} = \frac{1}{en\mu}} \qquad \textbf{(2.9)}$$

Electrical resistivity of a material is also inversely proportional to its carrier concentration. The TE material figure-of-merit is proportional to the power factor (${}^{\alpha_S^2}/_{\rho}$).

As shown in Figure 2.2, power factor is related to carrier concentration and is maximized at $n \sim 10^{20}$ cm^{-3} in semiconductors.

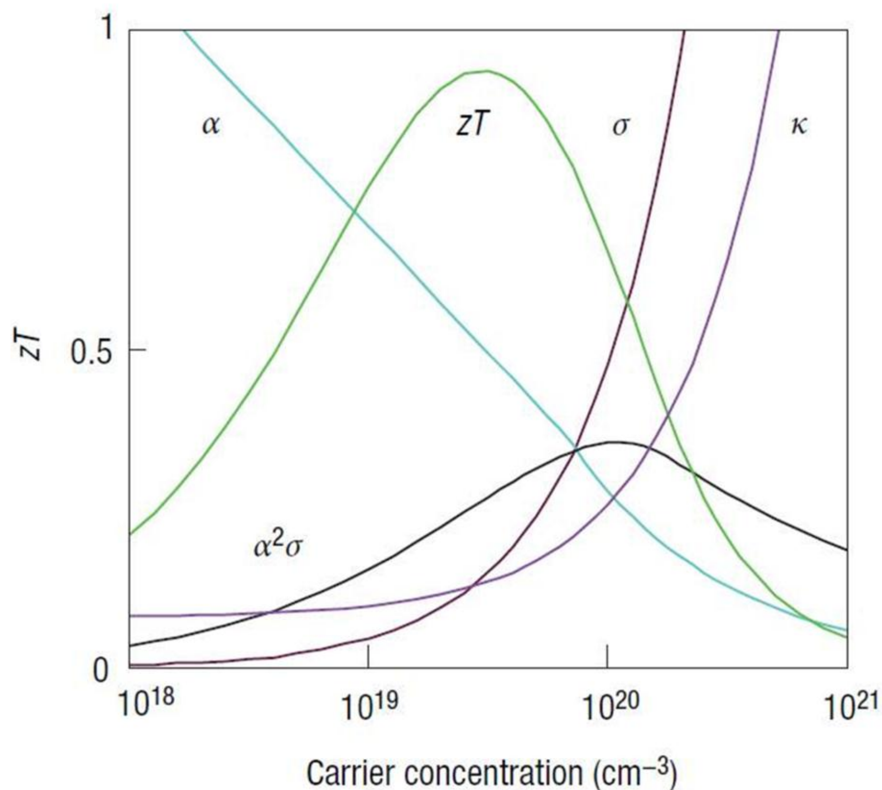


Figure 2.2 Effect of carrier concentration on thermoelectric properties of a material [85].

2.1.5. Thermal Conductivity

Thermal conductivity is the ability of a material to transfer heat under the effect of a temperature gradient across different points. The thermal conductivity of thermoelectric materials consists of the conductance via electrons ($\kappa_{electron}$) and phonons (κ_{phonon}).

Thermal conductivity through phonons is defined as follows:

$$\boldsymbol{\kappa_{phonon} = Cvl/3}\ , \tag{2.10}$$

where C is the phonon heat capacity per unit volume, v is the average phonon velocity, and l is the phonon mean free path between Umklapp scattering events. The mean free path is inversely proportional to the number of excited phonons (which is directly proportional to T). Therefore, phonon thermal conductivity increases as temperature decreases. This trend changes at very low temperatures where C becomes proportional to T^3, reducing κ_{phonon} toward to zero as the temperature approaches 0 K.

Thermal conductivity through electrons is governed by a similar equation with electron heat capacity, electron velocity and electron mean free path, and leads to the following equation:

$$\boldsymbol{\kappa_{electron} = \frac{\pi^2 n k_B^2 T \tau}{m} = \frac{\pi^2 n k_B^2 T \mu}{e}} \tag{2.11}$$

2.2. Thermoelectric Applications

The relationship between the figure of merit and efficiency (in the case of thermoelectric power generation) or performance coefficient (in the case of thermoelectric cooling) was derived by Ioffe theoretically [76], after neglecting thermal and electrical contact resistances. Therefore, improving figure of merit as the major definitive factor in thermoelectric materials' efficiency is the main goal of efforts to find materials for future

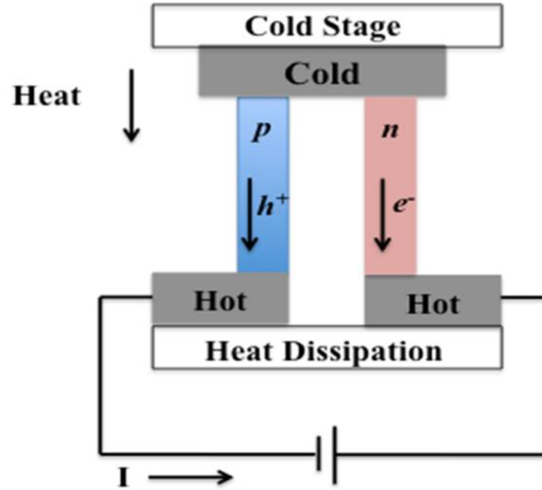


Figure 2.3 Illustration of thermoelectric cooling.

generation thermoelectric applications.

2.2.1. Thermoelectric Cooling

If an electric current is applied to a thermocouple as shown in Figure 2.3, heat is pumped from the cold junction to the hot junction. The cold junction will rapidly drop below ambient temperature, provided that heat is removed from the hot side.

The coefficient of performance (COP), φ, for a thermoelectric cooler is defined as the ratio of the cooling capacity Q_c to the total power consumption P [70].

$$\varphi = \frac{Q_C}{P} \tag{2.12}$$

The maximum COP is given by the following equation:

$$\varphi_{max} = \frac{T_C(\gamma - 1) - \Delta T}{\Delta T(\gamma + 1)} \; ; \; \gamma = (1 + ZT)^{1/2} \tag{2.13}$$

In this equation, T is the average temperature of the hot and cold junctions. The performance of a thermoelectric cooler depends on the figures of merit of the

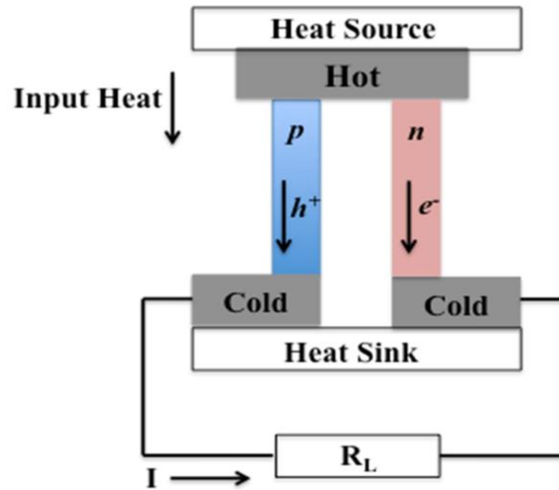


Figure 2.4 Illustration of thermoelectric power generation.

thermocouple materials.

At the macro-scale, consumer products including refrigerators and wine coolers[1] are capable of maintaining temperatures as low as 0 °C. Despite having lower cooling performance than conventional refrigerators[42], thermoelectric cooling devices are appealing in applications where small size and quiet operation are important. They can also be useful when DC power is available as opposed to the standard AC power. Thermoelectric modules are also available with a wide range of performance parameters for a variety of applications including Peltier coolers for cooling electronics. Although thermoelectric cooling is not very efficient for macro-scale applications, it has become appealing at the micro-scale, due to its maintenance-free, solid-state operation, and small size.

2.2.2. Thermoelectric Power Generation

Thermoelectric generators convert heat into electrical power based on the Seebeck effect. The basic operation is illustrated in Figure 2.4. The thermocouples in a thermoelectric

[1] http://www.sunpentown.com/winecoolers.html

device are connected thermally in parallel and electrically in series. Heat is pumped into one side of the couple, flows through the thermocouples and rejected from the opposite side. The generator open-circuit voltage is proportional to the number of thermocouples, the Seebeck coefficients of *n*-type and *p*-type legs (α_n and α_p), and the temperature gradient between the hot and cold junctions (ΔT).

$$V = N(\alpha_p - \alpha_n)\Delta T. \tag{2.14}$$

When the generator is connected to an electrical load of resistance R_L, the Seebeck voltage produces an electrical current. The output power of the generator is given by:

$$P = \frac{V^2}{R_L} = \frac{N^2(\alpha_p - \alpha_n)^2\Delta T^2}{R_L} \tag{2.15}$$

The efficiency of thermoelectric power generation, η, is defined as the ratio of the generated power, P, to the power drawn from a heat source Q_H [70].

$$\eta = \frac{P}{Q_H} \tag{2.16}$$

If the load R_L is chosen to maximize the output power, efficiency, η_{max}, is given by:

$$\eta_{max} = \frac{(\gamma-1)\Delta T}{(\gamma+1)T_H - \Delta T} \; ; \; \gamma = (1 + ZT)^{1/2} \tag{2.17}$$

Equation 2.17 shows that power generation efficiency depends on the thermocouple materials' figure of merit, the temperatures of the hot and cold sides, and the generator load resistance.

2.3. Thermoelectric Materials

2.3.1. Bulk Thermoelectric Materials

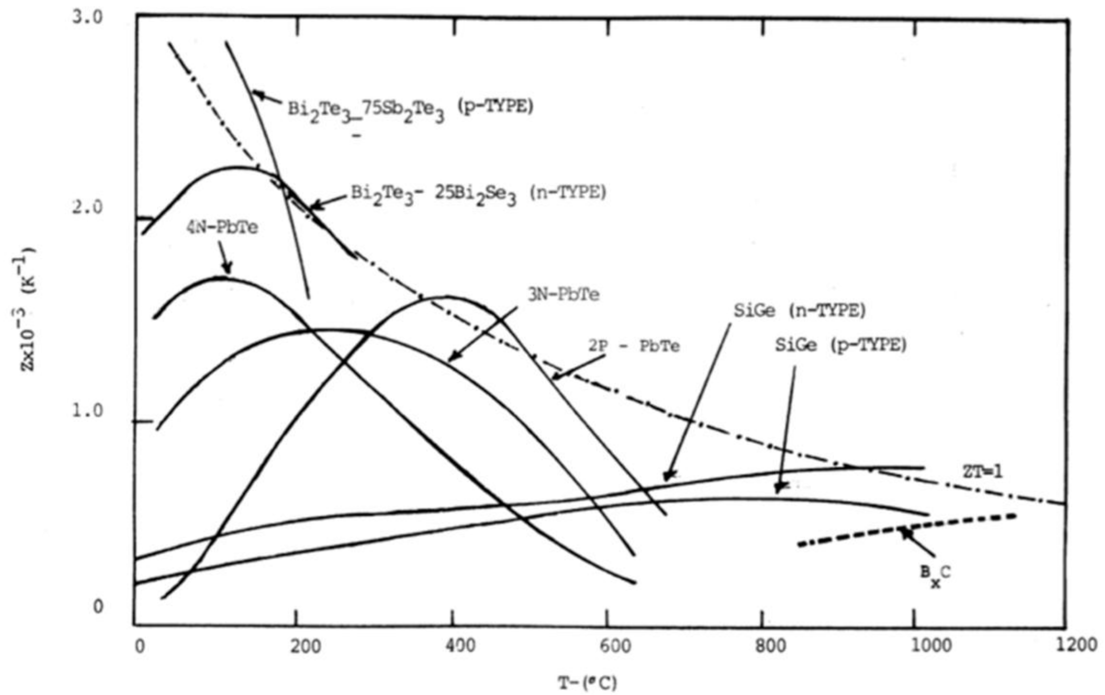


Figure 2.5 A comparison of common TE materials figures of merit at 0-1200 °C. Below 200 °C tertiary compounds of (Bi,Sb)2Te3 and Bi2(Te,Se)3 have the highest figures of merit. Reproduced from [26].

Bulk thermoelectric materials have demonstrated good performance in macro-scale applications. There are two basic processes for incorporating bulk materials into devices. One option is to fabricate all elements individually, then align and bond them on the device structure. The second possible process involves bonding large pieces of TE material in place and etching (or dicing) away the excess material.

The following sections summarize the thermoelectric properties of several commonly used bulk semiconductor thermoelectric materials including silicon, lead chalcogenides, Skutterudites, BiSb, Bi_2Te_3, Sb_2Te_3 and (Bi,Sb)Te-based ternary alloys. Figure 2.5 shows the figure of merit for a number of common materials over a wide range of operating temperatures.

2.3.1.1. Silicon

Silicon has demonstrated high Seebeck coefficients that are logarithmically related to resistivity for both *n*-type and *p*-type materials. The magnitude of the Seebeck coefficient varies from about 450 μV/K at resistivity value of 35 μΩ-m to as high as 1600 μV/K for resistivity values approaching 1 Ω-m. However, even at the optimum point of 35 μΩ-m resistivity, silicon's high thermal conductivity of 140 W/m-K means that *ZT* is about 0.012 at T=300 K [48]. The wide variety of available well-characterized processing technologies means that TE technologies based on silicon could potentially be easier to integrate with CMOS circuits and MEMS devices compared to other materials.

2.3.1.2. Lead Chalcogenides

Chalcogenides are predominantly semiconductors, most of which are stable and have relatively high melting points. At temperatures above 550 K, lead telluride alloys are commonly used in thermoelectric applications. PbTe has a maximum *ZT* of around 0.8 at approximately 800K. Reformed lead telluride compounds have been reported to exhibit a *ZT* of greater than 1 for portions of the temperature range between 550 K and 750 K, and can be used at temperatures as high as 600-900 K [26]. Because of its tolerance for high temperatures, lead telluride is often considered for use in applications such as power generation from waste heat of exhaust or engine on vehicles.

2.3.1.3. Skutterudites

Skutterudites represent a family of compounds with an MX_3 structure, where M is Co, Rh, or Ir, and X is P, As, or Sb. These compounds can reach *ZT* values beyond 1 in the temperature range of 700-900 K [84]. The name of "Skutterudite" originates from the name of a small Norwegian town called Skutterud where $CoAs_3$ was extensively mined. Skutterudites have shown promise as semiconducting materials with superior

thermoelectric properties at temperatures up to at least 650 °C.

2.3.1.4. Bismuth-Antimony Alloys

Both bismuth and antimony are semi-metals due to the energy overlaps between the conduction and valence bands. The overlap is small enough for the elements to display non-metallic features such as change of carrier concentration after addition of impurities. The thermoelectric figure of merit of Bi-Sb alloys can be substantially improved by applying magnetic fields. N-type $Bi_{85}Sb_{15}$ has been shown to have a figure of merit of ZT= 0.54 at 80 K, which can be increased to ZT=0.88 through the application of a large, properly aligned magnetic field [96]. However, BiSb alloys figures of merit diminish rapidly as the temperature increases toward room temperature.

2.3.1.5. Bismuth Telluride

In 1954 Goldsmid demonstrated the excellent thermoelectric properties of bismuth telluride, attributed mainly to the large mean molecular mass, low melting temperature and partial degeneracy of the conduction and valence bands of this V-VI chalcogenide [76]. Since then, bismuth telluride has been widely studied as a thermoelectric material, particularly in the temperature range around 300 K. The non-cubic structure of bismuth telluride contributes to anisotropy in thermoelectric properties, to physical characteristics (easy cleavage along the basal plane), as well as to the diffusion coefficients of impurities or dopants. It has a tetradymite structure with space group $R3m$ and the lattice is stacked in a repeated sequence of five atom layers: Te^1-Bi-Te^2-Bi-Te^1 along the c-axis (Figure 2.6). The superscripts 1 and 2 denote differently bonded tellurium atoms. Te and Bi layers are held together by strong ionic-covalent bonds (Te^1-Bi and Bi-Te^2). The Te^1 bonds between cells are of the van der Walls type and are extremely weak.

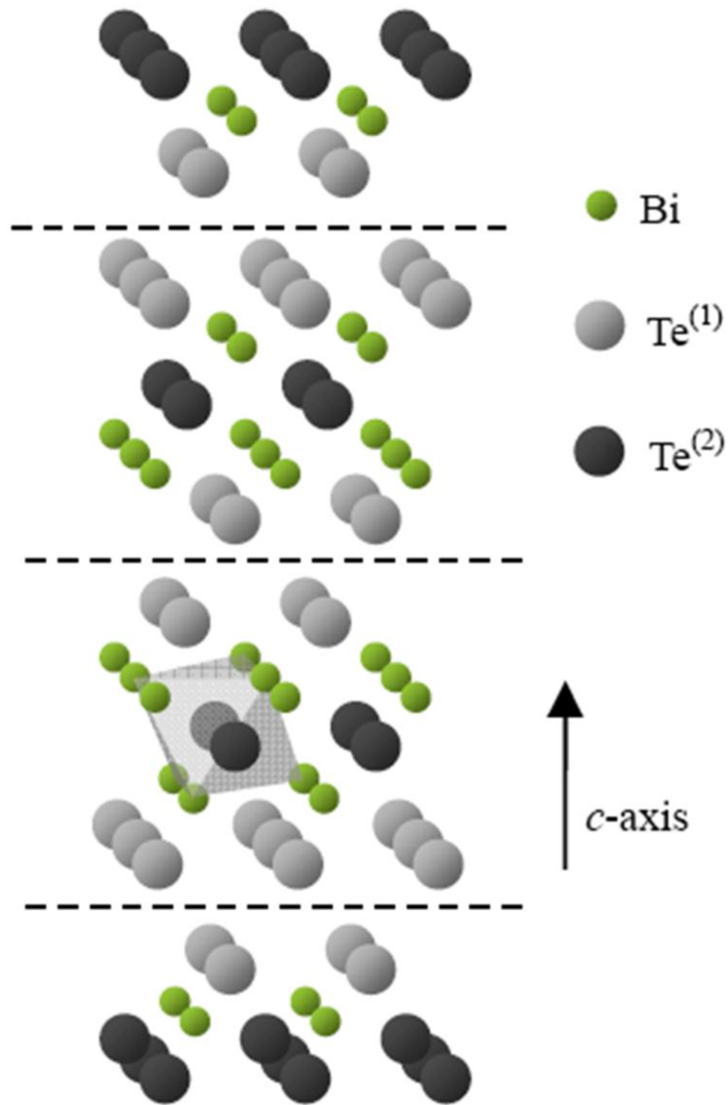


Figure 2.6 Atomic layers in the Bi_2Te_3 crystal structure. Dashed lines indicate van der Walls gaps. The octahedral coordination is highlighted for a Te $^{(2)}$ atom. Reproduced from [76]**.**

Stoichiometric Bi_2Te_3 is p-type with α_s=227 μV/K, ρ=19.5 μΩ-m, and κ=1.73 W/m-K leading to a *ZT* value of 0.45. Bismuth telluride compound can be doped as either *n*- or *p*-type material by creating either a tellurium-rich composition or a bismuth-rich composition respectively [76].

2.3.1.6. Antimony Telluride

Antimony Telluride, Sb_2Te_3, is a *p*-type semiconductor with a structure similar to Bi_2Te_3. The composition of Sb_2Te_3 can be manipulated to maximize the figure of merit. The optimal properties perpendicular to the *c*-axis are α_s=83 μV/K, ρ=1.89 μΩ-m, and κ=1.62 W/m-K, producing *ZT*=0.20 at 67 At.% tellurium. The thermoelectric properties of Sb_2Te_3 improves significantly parallel to the *c*-axis and *ZT*=0.48 has been observed at 72% tellurium [76].

2.3.1.7. (Bi,Sb)Te-based Ternary Alloys

In order to make the thermoelectric bulk materials *p*-type or *n*-type, it is common to introduce doping and/or make modifications for the synthesis of solid solutions of *p*-type $(Bi_2Te_3)_x(Sb_2Te_3)_y$ or *n*-type $(Bi_2Te_3)_x(Bi_2Se_3)_y$ alloys.

Alloying Bi_2Te_3 with Sb_2Te_3 or Bi_2Se_3 is expected to enhance the *ZT* above the values reported for binary compounds due to reduced thermal conductivity. Many commercial macro/meso-scale TE devices have used bulk $(Bi,Sb)_2Te_3$ for *p*-type and $Bi_2(Te,Se)_3$ for *n*-type; Bi_2Te_3 and Sb_2Te_3 can be combined in solid solutions due to their similar crystal structure. Single crystal $(Bi_{0.45}Sb_{1.55})Te_3$ has been measured to have α_s=206 μV/K, ρ=8.89 μΩ-m, and κ=1.5 W/m-K producing *ZT*=0.96, which is about a factor of 5 better than the measured *ZT* of Sb_2Te_3 perpendicular to the *c*-axis [77].

Achieving high quality *n*-type Bi_2Te_3 relies on obtaining the correct composition within a very narrow tolerance. Alloying Bi_2Te_3 with Bi_2Se_3 reduces the dependence of TE properties on crystal structure and atomic ratio of the constituent elements. $Bi_{40}Te_{58.5}Se_{1.5}$ compound achieves the maximum performance with α_s=-230 μV/K, ρ=11 μΩ-m, and κ=1.7 W/m-K producing *ZT*=0.87 [77].

2.3.2. Thin Film Thermoelectric Materials

There has been a wide variety of power generation and cooling devices made at the macro scale, utilizing bulk thermoelectric materials. However it is difficult to integrate bulk materials at the micro-scale processes as discussed in section 2.1. TE thin films, which can be deposited directly onto the surface of the substrate, are more suitable for micro-scale systems. Many of the same bulk TE materials can be used in thin-film form for micro-scale applications. However, because the films are not formed under equilibrium conditions, and are usually amorphous or polycrystalline, their properties can vary significantly from their single crystal bulk counterparts. (Bi,Sb)Te-based alloys are the best-performing materials near room temperature in bulk form. Therefore, their thin films have received significant attention as the TE material of choice for microsystems. Due to compatibility with integrated circuits technology, polycrystalline SiGe alloys and polycrystalline Si are also commonly used in thermopile applications. Their use in TE micro coolers and generators have also been investigated; however, their thermoelectric performance is very low compared to that of BiTe compounds[27,53].

2.3.3. Novel Thermoelectric Materials

Although ternary alloys have exhibited increased TE figures of merit over binary films, in order to obtain $ZT > 1$, superlattices and nanostructured materials have been explored recently. In either case, quantum confinement in one, two or three dimensions reduces phonon conduction. Therefore, thermal conductivity in that direction is lowered while maintaining electrical conduction, which leads to increasing ZT [23,49].

Significant experimental progress has been made in recent years to demonstrate increased ZT using nanostructured materials such as thin-film superlattices [83,91] and thick films

of quantum-dot superlattices [46]. Superlattices use alternating layers of different materials with thickness of 1-40 nm in order to create an artificial lattice constant that can influence the dispersion of both electrons and phonons. The lattice mismatch, electronic potential differences at the interfaces, resulting phonon and electron interface scattering, and band structure modifications can be exploited to reduce phonon heat conduction while maintaining or enhancing the electron transport [12]. The most successful results of superlattice research have used MOCVD to produce *p*-type Bi_2Te_3/Sb_2Te_3 material with a ZT of 2.4, and *n*-type $Bi_2Te_3/Bi_2Te_{2.7}Se_{0.3}$ material with a *ZT* of 1.4. [10,11,91].

2.4. Thermoelectric Thin Film Deposition Techniques

One of the main challenges of integrating thin film TE materials with microsystems is patterning of TE films. Most TE thin film deposition methods are performed at high substrate temperatures (~ 250°C), so patterning by liftoff is not a possibility since photoresist would burn when heated up to such temperatures. Patterning the TE film by etching is also very hard due to the weak adhesion between the TE material and substrate, as well as lack of anisotropic wet etch processes. Moreover, BiTe compounds are incompatible with typical cleanroom processing. Therefore, dry reactive ion etching of TE films as done in [7] is feasible only by using a specifically designated tool. A shadow-mask technique has been used successfully to pattern thin films with lateral dimensions as small as 23 μm at the University of Michigan[42,51].

The second challenge for TE film integration in microsystems is the low melting points of many TE constituent elements. This means that the TE deposition step must be a back-end process to avoid earlier high-temperature processing steps. Therefore it is critical to choose a TE material deposition technique and conditions which not only are suitable for

integration with the larger process flow used to make the device, but also allow for simple patterning techniques at the micro-scale.

2.4.1. Sputtering

Sputtering is used extensively in the semiconductor industry to deposit thin films of various materials. Sputtering sources usually utilize strong electric and magnetic fields to trap electrons close to the surface of the magnetron, which is known as the target. An inert gas, typically Argon, is used for sputtering. This deposition technique uses direct current or RF power sources to either co-sputter from individual element targets [7,55], or direct sputter from one target containing a mixture of constituent elements [9,52]. Films are deposited onto heated substrates and then further annealed at temperatures around 300 °C. Böttner deposited films with the highest recorded power factors of 3 mW/K^2m for *n*-type and 4 mW/K^2m for *p*-type materials [8]. While the *n*-type material performance is somewhat lower than its bulk equivalent, the *p*-type material approaches the performance of bulk $(Bi,Sb)_2Te_3$.

2.4.2. Molecular Beam Epitaxy (MBE)

Molecular beam epitaxy is one of several methods to deposit single crystals. The most important aspect of MBE is the slow deposition rate (typically less than 1000 nm per hour), which allows the films to grow in an epitaxial manner. Slow deposition rates require proportionally better vacuum to achieve the same impurity levels as other deposition techniques. MBE systems are optimized to maintain very high purity, with high-vacuum chambers that are capable of reaching pressures as low as $\sim10^{-10}$ Torr, and to produce single-crystal thin-film epitaxial layers. Sources of pure constituent elements

are evaporated or sublimated from individual effusion cells that are separated from the substrate by shutters or valves, and the substrate is heated. Bi_2Te_3 has been deposited with a Seebeck coefficient of 180 μV/K [16] and $(BiSb)_2Te_3$ has been reported with a Seebeck coefficient of 184 μV/K and a power factor of 1.6 mW/K^2m)[17].

2.4.3. Metal Organic Chemical Vapor Deposition (MOCVD)

Metal-organic chemical vapor deposition is a CVD method of materials epitaxial growth from the surface reaction of organic compounds or metalorganics and metal hydrides containing the required chemical elements. Formation of the epitaxial layer occurs by final pyrolysis of the constituent chemicals at the substrate surface. In contrast to MBE, the growth of crystals is by chemical reaction and not physical deposition. This takes place at moderate pressures instead of vacuum. MOCVD has been investigated using precursors of trimethylbismuth, triethylantimony, diethyltellurium, and diethylselenium as a means of growing thermoelectric materials. The growth temperature is between 350°C and 480°C. Bi_2Te_3 and Sb_2Te_3 films have power factors of 7.2 mW/K^2m and 4 mW/K^2m, respectively [35,36]. *P*-type $(Bi,Sb)_2Te_3$ films have shown higher Seebeck coefficients and resistivity resulting in a power factor of 3.3 mW/K^2m [68].

High quality *n*-type and *p*-type materials have been produced using this technique. The most successful results of Bi_2Te_3/Sb_2Te_3 superlattice research have used MOCVD to produce *p*-type material with a *ZT* of 2.4, and *n*-type material with a *ZT* of 1.4 [91]. Superlattices use alternating layers of different materials with thickness of 1-40 nm in order to create an artificial lattice constant and lower thermal conductivity. The high figure-of-merit of superlattice materials make them the material of choice for many applications, however the toxicity of the metal organic precursors requires additional

safety and security procedures, which make MOCVD deposition quite expensive. Moreover, these superior TE properties are only achieved in the direction perpendicular to the layers of the superlattice, which is not suitable for many planar structures.

2.4.4. Electrochemical Deposition (ECD)

Thermoelectric films have also been produced by ECD. The constituent elements are dissolved in a nitric acid solution, which may also contain a chelating agent to prevent precipitation of insoluble oxides. Several researchers have investigated electrochemical deposition of (Bi,Sb)Te-based alloys. Yoo deposited Bi_2Te_3 with power factor of 0.17 mW/K^2m [97]. Kim *et al.* [57] have reported power factors of 0.71 mW/K^2m and 0.57 mW/K^2m for Bi_2Te_3 and Sb_2Te_3, respectively. The work in [63] utilized ECD to deposit *p*-type Sb_2Te_3 and $(Bi,Sb)_2Te_3$ with power factors of 0.57 mW/K^2m and 0.12 mW/K^2m, respectively. $(Bi,Sb)_2Te_3$ films have also been deposited with Seebeck coefficients between 40 μV/K and 100 μV/K [86]. Electrochemical deposition of thin films is a convenient alternative to vacuum-based methods because of simplicity, low cost, and ambient temperature and pressure operation [5]. However, the lower material quality and poor performance limit its applications and usefulness.

2.4.5. Flash Evaporation

Flash evaporation is one of the prominent techniques for the deposition of thin films alloys whose constituents have different vapor pressures. The main advantage of flash evaporation is that it does not require maintenance of the critical vapor pressures of the components via the temperatures of the boats. Dispensing the powder onto the boat is a crucial part of this deposition method. Most techniques for powder dispensing use

Deposition method	Source material	T_{sub} range	Indep. control of T_{sub}	Indep. control of dep. rates	*In situ* patterning	CMOS compatible	Other
Sputtering	**fixed composition target(s)**	**unlimited**	**Yes**	**No**	**shadow masking**	**Possible**	**High-quality films, require annealing**
Co-sputtering				**Yes**			
ECD	**solution**	**ambient**	**difficult**	**No**	**lift off**	**Unlikely**	**--**
Flash evaporation	**alloy solids (e.g. powder)**	**typically ambient**	**Yes**	**No**	**shadow masking**	**Possible**	**Require post-annealing**
MBE	**constituent elements**	**unlimited**	**Yes**	**Yes**	**shadow masking**	**Possible**	**--**
MOCVD	**metal-organic precursors**	**typically 350 – 480 °C**	**Yes**	**Yes**	**none**	**Unlikely**	**High-quality films, expensive, complicated**
Thermal co-evaporation	**constituent elements (e.g. pellets)**	**unlimited**	**Yes**	**Yes**	**shadow masking**	**Possible**	**Simple reconfigured**

Table 2.1 Comparison of thermoelectric thin film deposition techniques.

complex mechanical devices, which require expensive cleaning processes or are contaminative in nature if different materials are used for evaporation because of direct contact of the powder with the powder dispenser.

This simple deposition technique requires neither complicated evaporation equipment nor special precursors. Because of the rapid deposition of TE alloy on the substrate, the grains have a short time to grow. Thus post-deposition annealing is required to increase the grain size. $Bi_{0.5}Sb_{1.5}Te_3$ films were deposited by flash evaporation of SiO_2/Si wafers with *ZT* of 0.87 in [92]. The best performance of *p*-type $Bi_{0.4}Te_{3.0}Sb_{1.6}$ thin films annealed at 300°C resulted in a power factor of 3.49 mW/ K^2m [89]. *P*-type $Bi_{0.4}Te_{3.0}Sb_{1.6}$ and *n*-type $Bi_{2.0}Te_{2.7}Se_{0.3}$ had Seebeck coefficients of 170 μV/K and -90 μV/K, respectively [61]. The maximum power factor of $Bi_2Te_{2.7}Se_{0.3}$ thin film is enhanced to 1.2mW/ K^2 m when annealed at only 100°C [24].

2.4.6. Thermal Evaporation

Thermal evaporation is similar to MBE deposition. Elements are evaporated from individual sources and deposited on the surface of the substrate to form the compound. MBE is an advanced form of thermal evaporation, in which the source is heated by an electron beam with energy up to 15 keV. However, the thermal evaporation systems are simpler than MBE systems because thermal energy is utilized to produce the vapor of the evaporant materials. Thermal evaporation is an attractive deposition technique because of the relatively high film quality, simple vacuum deposition technology, ease of process control and configurability, and compatibility with post-CMOS processing [20] [99].

Due to the large vapor pressure difference of the constituent elements, direct evaporation of a bulk compound material results in a compositional gradient along the film thickness [20]. Alternately, thermal co-evaporation of pure Bi, Sb and Te can be achieved by independent control of the power supply used to heat each source, resulting in independent control of the constituent deposition rates and consequently good stoichiometry control of the deposited thin films [40]. The optimization of TE films is performed by changing the flux ratio (FR) and the substrate temperature during deposition. Several works have investigated co-evaporation of binary compounds with the highest power factors achieved of 4.9 mW/K^{2}m for Bi_2Te_3 and 2.8 mW/K^{2}m for Sb_2Te_3 thin-films [13].

A summary of all of these techniques is provided in Table 2.1, highlighting the advantages and disadvantages of each approach.

Chapter 3 Thermoelectric Thin Film Evaporation and Characterization Techniques

As discussed in the previous chapter, one of the simplest processes for thin film deposition is the evaporation of the material and its condensation on the desired substrate. In this chapter, thermal evaporation for depositing (Bi,Sb)Te-based thermoelectric thin films and the vacuum system used for this process are described. Various measurement and characterization techniques for studying deposited TE thin films are explained in detail.

3.1. Thermal Evaporation of Thin Films

Thermal evaporation is a physical vapor deposition (PVD) technique using thermally-heated material sources [66]. In this process, materials are thermally vaporized and reach the desired substrate with little or no collision with the gas molecules inside the evaporation chamber. The vacuum deposition usually happens at the gas pressure range of 10^{-6}-10^{-9} torr, reducing the environment gaseous contamination to a very low level. The high vacuum also provides a long mean free path for collision between the source and the substrate. Transfer of thermal energy into the materials leads to the formation of the vapor phase and the transform into the gas phase. An atom or a cluster of atoms has to

Material	Melting point (K)	T (K) @ vapor pressure 750 (Torr)	T (K) @ vapor pressure 75 (Torr)	T (K) @ vapor pressure 7.5 (Torr)
Bi	544.7	1835	1538	1325
Sb	903.8	1858	1491	1219
Te	722.7	1266	1042	888

Table 3.1 Melting points and temperatures for a given vapor pressure of Bi, Sb and Te elements

overcome the intermolecular forces in the condensed phase to be able to leave the solid surface. The composition of the vaporized material is proportional to the relative vapor pressures of the solid or liquid material in the source. The vapor pressure of different materials at the same temperature can be quite different. A high vapor pressure of 10^{-2} torr usually is needed to begin the evaporation rate from solid or liquid phase of the material.

The melting points for Bi, Sb and Te elements are shown in Table 3.1. It also summarizes the temperatures for a given vapor pressure of these elements. In a (Bi,Sb)Te-based system, antimony (Sb) has the vapor pressure of 10^{-2} torr at temperatures below its melting point and is thus transformed to vapor by sublimation. The advantage of Sb sublimation is that the material will not melt and overflow the crucible while heating the source. The drawback is the poor thermal contact between solid Sb and the heated crucible. Moreover, Sb vaporizes in the form of atom clusters, which makes controlling the evaporation rate very difficult. Also, vaporizing the alloy produces a gradient in the deposited thin film due to vapor pressure differences of Bi, Sb and Te elements. These alloys can be deposited on the substrate using multiple sources with individual deposition rate controllers [65].

Vaporized atoms can be re-evaporated from the substrate instead of condensing. Re-

evaporation is a function of substrate temperature, and we observe its occurrence for tellurium at high deposition temperatures (Chapter 4). If thermally vaporized atoms condense on the surface of the desired substrate, they release energy by cooling down, by bond formation and by chemical reactions. At high deposition rates, this released energy can increase the substrate temperature significantly. Therefore, the evaporation rates must be controlled carefully. The deposited film uniformity across the wafer is achieved by adjusting the substrate distance from the sources and rotating it during evaporation.

Properties of a thermally evaporated film of a specific material depend on several factors[88]:

- Substrate surface conditions including surface morphology, surface chemistry, mechanical properties and outgassing.
- Deposition process details such as substrate temperature, evaporation rate, flux incident angle and gaseous contamination.
- Growth of film on the substrate details such as condensation of the arriving particles, interfacial flaws, surface mobility of the depositing particles and gas entrapment.

Thin films deposited using thermally evaporation method usually have high residual stress, pinholes and are less than fully (bulk material) dense.

3.2. Co-evaporation System for TE Materials

Reference	Material	α_S (μV/K)	ρ (μΩ-m)	α_S^2/ρ (mW/K^{2}m)	*ZT*	T_{sub} (°C)
Zou 2001[98]	*p*- Bi_2Te_3	81	3.2	2.05	0.36	314
	n- Bi_2Te_3	-228	13	3.99	0.70	260
Zou 2002 [99]	*p*- Sb_2Te_3	171	10.4	2.8	0.49	230
Da Silva 2005 [18]	*n*- Bi_2Te_3	-228	28.3	1.84	0.32	260
	p- Sb_2Te_3	149	12.5	1.78	0.31	270
Goncalves 2008 [39]	*n*- Bi_2Te_3	-248	12.6	4.9	0.86	270
	p- Sb_2Te_3	188	12.6	2.8	0.49	220
Huang 2008 [51]	*n*- Bi_2Te_3	-208	18.8	2.3	0.41	260
	p- Sb_2Te_3	160	12.9	2.0	0.35	230

Table 3.2 Comparison of co-evaporated binary thin films. The Bi_2Te_3 and Sb_2Te_3 figure-of-merit is calculated assuming κ=1.7 W/m.K.

Co-evaporation has been shown to produce (Bi,Sb)Te-based TE material with figure-of-merit comparable to other deposition techniques and is also arguably the simplest among all the vacuum deposition technologies discussed above. It requires neither unusual chemical precursors/reaction effluents that need to be processed (MOCVD) nor comprehensive knowledge of electrochemistry to optimize the process (ECD). Moreover, the line-of-sight deposition allows the use of shadow masks to define the area of deposition. Table 3.2 summarizes and compares properties of co-evaporated binary thin films investigated by previous works.

As discussed in the previous section, due to different vapor pressures and melting points of the constituent elements, direct evaporation from the compound source can result in an incorrect atomic ratio of elements in the thin film, despite the correct composition of the source. In the co-evaporation process, the deposition rate of each source can be controlled independently by adjusting the power supplied to heat up each source. As a result, the flux rates of the different materials at the wafer surface can be controlled to determine the composition of the film. Adjusting the temperature of the substrate during co-evaporation affects the crystal growth condition of the film and results in different crystal orientation,

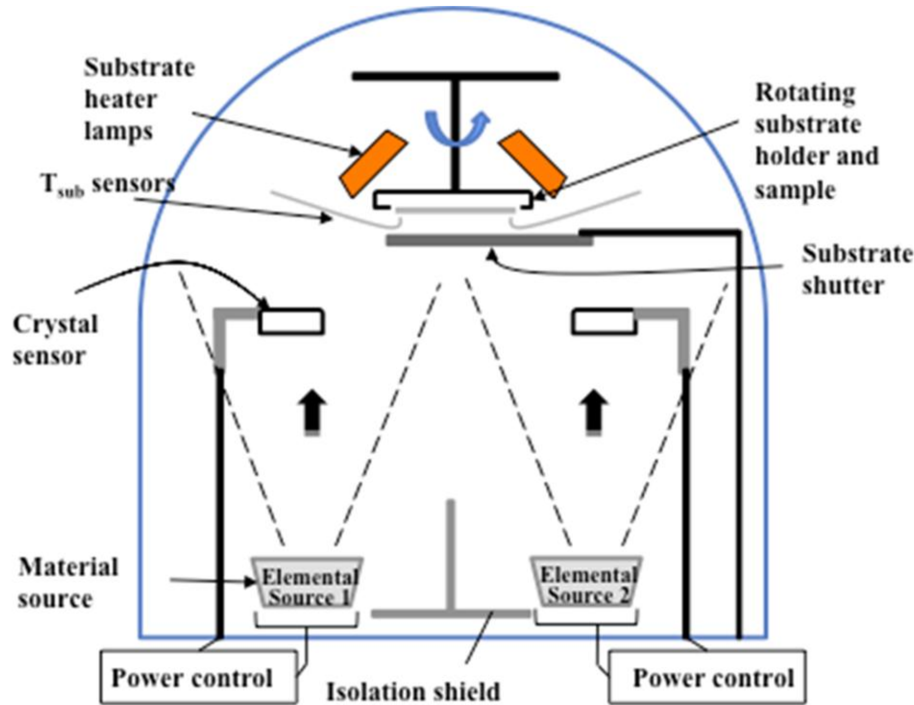


Figure 3.1 Schematic of a vacuum co-evaporation system.

size and structure. A basic schematic of the co-evaporation system is shown in Figure 3.1.

The thermal evaporator system used for this work is supplied by the Kurt J. Lesker company and is shown in Figure 3.2. The Lab 18 system includes six individual sources with relatively high capacities. Therefore, there is no need to refill the sources between deposition runs. Moreover, having more than two sources in the system facilitates the deposition of ternary compounds. Each material source (99.999% pure Bi, Sb shots and Te powder from Alfa Aesar supplier in Ward Hill, MA) is held in an alumina crucible that is heated by a resistive element.

All of the crucibles and the substrate wafer are individually shuttered. The crucibles are separated using stainless steel isolation shields to reduce cross-contamination. The substrate holder supports either 4 or 6 inch wafers and has a rotation mechanism. The

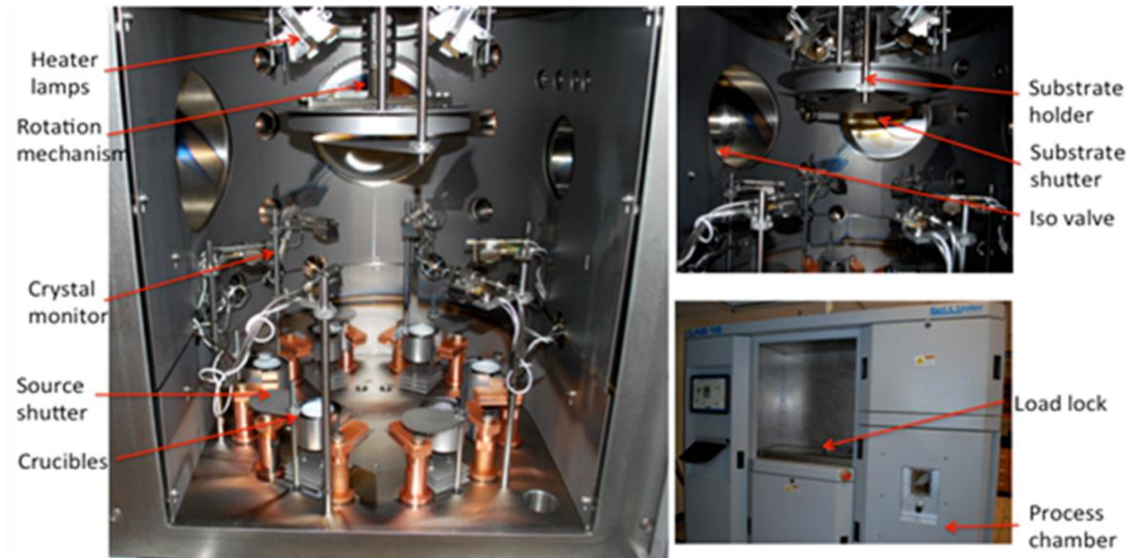


Figure 3.2 Co-evaporation system for (Bi,Sb)Te-based thin films. Basic parts inside the deposition chamber and the exterior of the tool are shown.

system has a crystal thickness monitor for each source, and the crystals are shuttered to allow for discrete sampling of the deposition rate. Covering the crystal sensors with shutters for a portion of time during the deposition increases their lifetime and makes longer depositions, and as a result thicker TE films, possible. The Te source crystal sensor deteriorates faster compared to the crystals of Bi and Sb sources and has to be replaced more frequently. Due to the corrosive effect of the Te element on the crystal sensors, its evaporation rate error is about ± 0.5 Å/s, while Bi and Sb evaporation rate errors are ± 0.1 Å/s.

This system includes a load lock and isolation valve, allowing for rapid sample loading. It is not necessary to vent the process chamber between each run to load the substrate and as a result, low base pressure in the process chamber is preserved. The process chamber pressure can reach values as low of 10^{-8} Torr using a cryo pump. All samples are cleaned with acetone/IPA/DI water and blow dried with nitrogen gun before loading in the tool. After the wafer is loaded in the process chamber face down, the halogen lamps used to

heat up the substrate are turned on, and the wafer temperature is allowed to stabilize. The substrate temperature is measured with two sets of K-type thermocouples placed about 1 cm below the edges of the wafer holder.

Subsequently, designated material crucibles are heated until the evaporation rates reach appropriate levels. The power to each source is automatically set using a computer-controlled PID loop to match the measured deposition rate to the desired rate. While the evaporation rates are being stabilized, the substrate shutter is closed to prevent uncontrolled material deposition. After opening the substrate shutter, deposition with the desired FR continues until the final film thickness is reached. When the deposition is complete, the sample is allowed to cool down slowly to < 40 °C before being transferred to the load lock chamber. Excessive oxidation and stress would occur in the deposited film if it were removed from the process chamber immediately.

The system is also equipped with integrated RF plasma functionality for *in situ* wafer cleaning and etching. Inert gas plasma can be used to clean surfaces in the deposition chamber. A plate is used as the cathode or anode electrode of a DC discharge to create the plasma.

This system had to be calibrated for (Bi,Sb)Te-based thin film co-evaporation for the first time. The calibration of the evaporator system started with characterizing the deposition of Bi_2Te_3 and Sb_2Te_3 compounds on silicon wafers coated with a thin film of silicon dioxide (SiO_2/Si). Deposition conditions similar to those examined in [51] were set as the starting point for optimization of binary films. The tooling factor for each of the elemental sources (Bi, Sb and Te) in this system has been calibrated both by deposition of single element film and measurement of its thickness. Tooling factor accuracies were also

checked by composition analysis of co-evaporated compound thin films. Calibration of thermocouples has been done by attaching temperature dots to a test wafer and monitoring dot color changes while increasing the nominal temperature of the lamp heaters.

3.3. Thermoelectric Thin Film Characterization

In this chapter, characterization techniques for co-evaporated bismuth telluride and antimony telluride thin films are presented. The experimental techniques to analyze TE film properties including electrical resistivity, Seebeck coefficient, carrier concentration, chemical composition, grain size, and crystal structures are described. Test set-ups for quick and efficient characterization of several TE properties are introduced.

3.3.1. Crystal Structure, Orientation and Composition

The crystal structure of the co-evaporated materials (grain size and orientation) is examined using a high-resolution scanning electron microscope (SEM) both on the surface and cross-section of the films. The underlying substrates of TE films are scribed and cleaved to prepare samples for the cross-section of SEM analysis. Care must be taken during the cleaving process to avoid damaging film grains at the surface. A Philips XL30 field emission gun scanning electron microscope (FEG SEM) was used to provide SEM images. The images were taken at a working distance of 10 mm from the sample with 10 kV.

Buildup of electrons (charge) on semi-conductive samples creates an electric field, which could deflect the electron beam in undesirable ways and ruin SEM images. Therefore, a 4 nm layer of gold was deposited on top of TE film samples to reduce the undesirable

charging effect in the SEM and get good images.

The X-ray detector attached to the SEM equipment is used to verify film composition for the TE samples through energy dispersive X-ray spectroscopy (EDX). The relative concentration of the elements is measured with an accuracy of ±2% in 5 different locations on each sample using EDX analysis.

Orientation of film crystals is determined using X-ray diffraction (XRD) analysis. Similar to SEM analysis, in order to perform XRD measurements, the underlying substrates of TE films are cleaved and small pieces (5 mm × 5 mm) of the specimen are cut and attached to the sample holder. The measured XRD pattern is compared to available diffraction patterns of the same crystal structure. Theta-2Theta scans are taken of select TE films for the XRD analysis. A power of 40 KV and 100 mA is used for the gun, which produced K–alpha radiation from copper. The scans sweep from 2 – 80° with a scan time of 30 seconds per degree. The results are compared to XRD powder profiles obtained from the International Center for Diffraction Data (ICDD) for indexing. The PDF cards used are 01-085-0439 for Bismuth Telluride, 04-003-0996 for Antimony Telluride, 04-002-0492 for Bismuth Antimony Telluride, and 99-000-3405 for Silicon.[2]

A powder sample of a material theoretically contains all the crystallographic planes *(hkl)* of that material in equal amounts. However, with X-ray diffraction, certain crystal planes produce stronger returns than others (higher peaks), even if the two orientations have the same intensity. This effect can be seen in the powder XRD returns for bismuth telluride and antimony telluride. Figure 3.3 shows the XRD pattern of a Bi_2Te_3 thin film as an example. The red lines indicate the powder diffraction profile for bismuth telluride, while the blue lines relate to the crystal orientation of a Bi_2Te_3 film on a glass substrate.

[2] http://www.icdd.com/

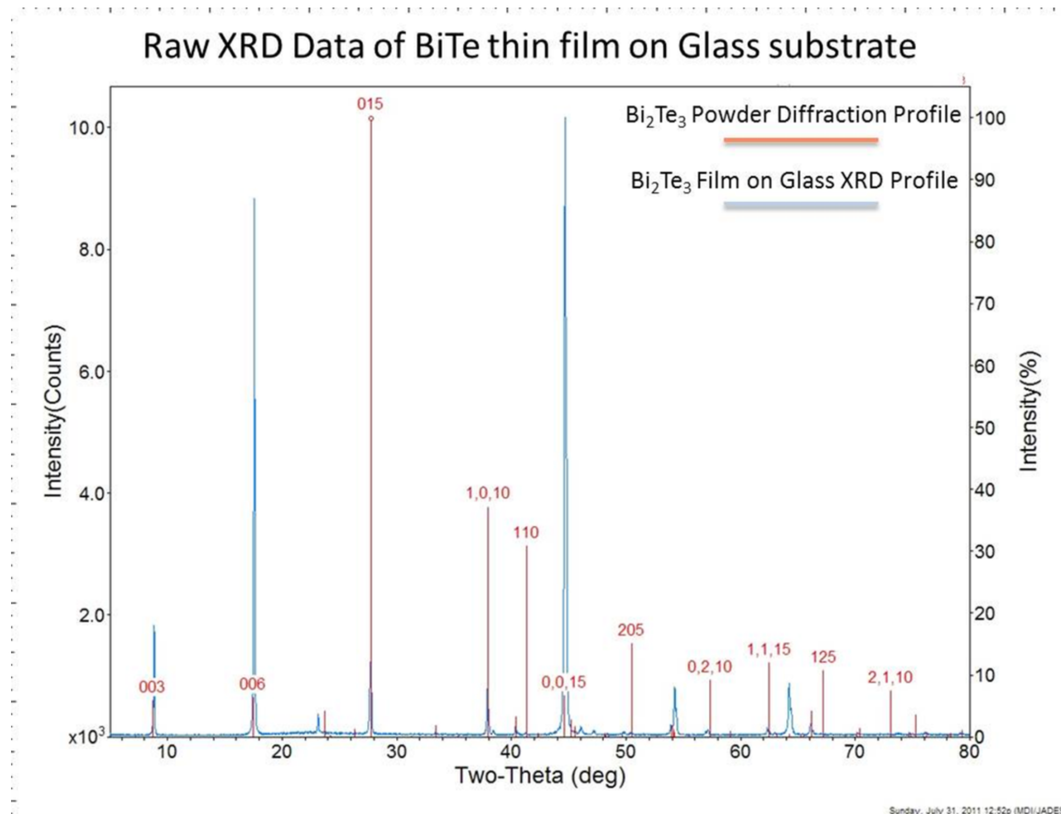


Figure 3.3 X-ray diffraction pattern of Bi_2Te_3 on glass and diffraction profile of Bi_2Te_3 powder.

To estimate the crystallographic composition of the XRD data, normalized XRD plots have been generated [90]. The peak area for each reflection plane in the sample is divided by the corresponding peak area in the powder diffraction pattern to obtain the normalized data. For instance, assuming the XRD pattern of a specific film shows intensities of 200 counts in (0,0,3) and 900 counts in (0,0,6) orientations, and the reference powder of that material shows 200 counts in (0,0,3) and 200 counts in (0,0,6) reflection planes, normalized XRD data will demonstrate intensities of 1 and 4.5 at (0,0,3) and (0,0,6) orientations, respectively (Figure 3.4).

Relative amount of *c*-orientation growth in TE film samples is characterized by dividing the sum of total areas of *c*-oriented peaks by the sum of total peak area.

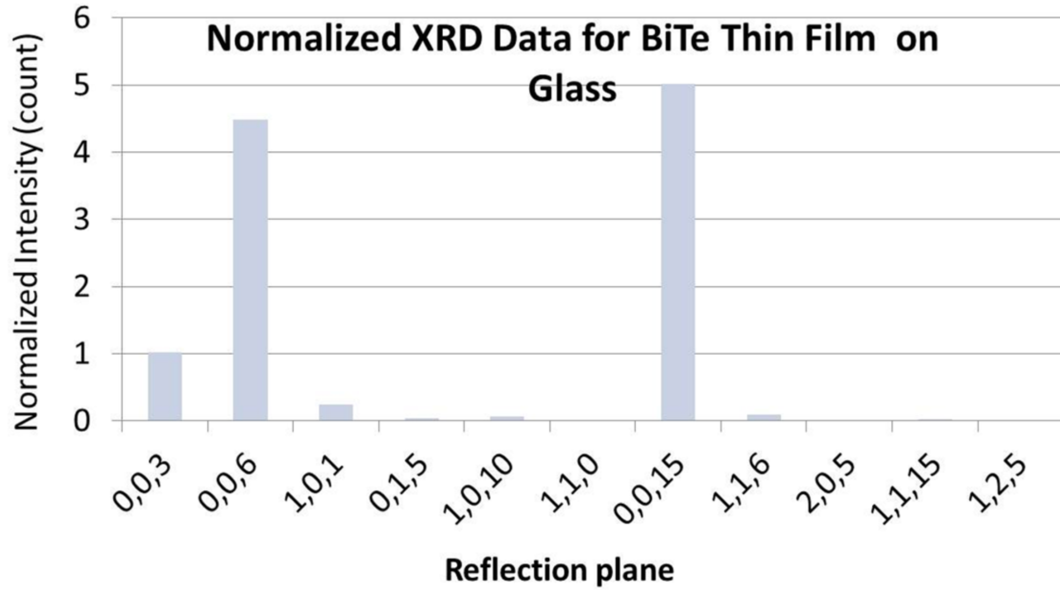


Figure 3.4 Normalized diffraction pattern of the Bi_2Te_3 films on glass.

3.3.2. Thin Film Thickness and Surface Roughness

Several physical characteristics of TE thin films such as carrier concentration and resistivity are related to thickness. Therefore, thin film thickness and its precise measurement are very important. Crystal thickness monitors embedded inside the evaporation chamber provide the elemental deposition rates and monitor the thickness of the film deposited on them. However, this thickness is different from the thickness of the compound film deposited on the substrate due to different locations, sticking coefficient and temperatures. TE film thickness can be measured more precisely using DEKTAK surface profilometer. The film thickness is obtained by taking the average of measured values at three different locations on the sample with an accuracy of ± 5%. It is possible to get a close estimate of the co-evaporated film thickness by careful calibration of the relation between elemental deposition rates and substrate temperature with DEKTAK measured thickness.

Characterization and measurement of TE film surface roughness have been carried out using Atomic Force Microscope (AFM). A Nanoman AFM, operating in tapping mode over a 5×5 μm area is used to measure the surface roughness (R_q) of the films. Surface roughness influences various TE film properties, including thermal and electrical contact resistances. AFM technique is also useful in characterization of TE films polishing process.

3.3.3. Thermoelectric Properties

In this section, principles of thermoelectric material transport properties measurement and some applied practical techniques are described. Performance of a TE material can be expressed in terms of the dimensionless figure of merit *ZT*. To determine *ZT*, it is necessary to make independent measurements of the Seebeck coefficient, electrical resistivity, and thermal conductivity. Measurements of the Seebeck coefficient and electrical resistivity are performed for all film samples. TE films are characterized and compared by their power factors, which is defined as α_S^2/ρ. Experimental results in [72] show that for films that are thicker than 1 μm, thin film thermal conductivity is equal to its value for the bulk material. For films thinner than 1 μm, thermal conductivity drops due to the film/substrate contact resistances. Since the majority of co-evaporated TE film samples are thicker than 1 μm, thermal conductivity values are assumed to be the same as their bulk counterparts. The thermal conductivity is assumed to be 1.7 W/m-K for both Bi_2Te_3 and Sb_2Te_3 materials.

3.3.3.1. Seebeck Coefficient

The Seebeck coefficient and its sign are related to charge carrier concentration in the TE material. P-type TE materials have positive and *n*-type TE materials have negative

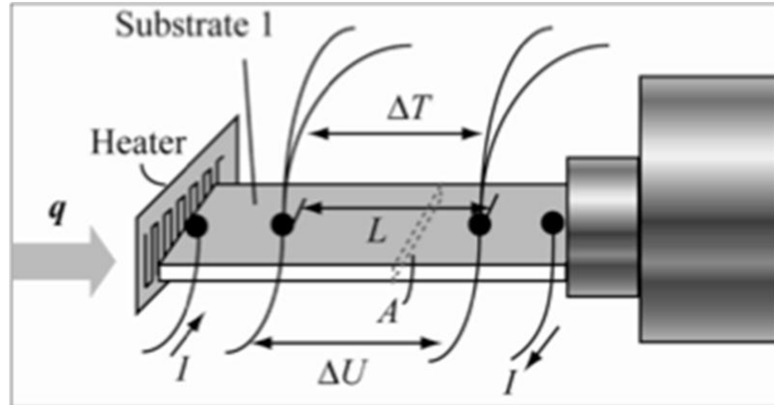


Figure 3.5 Setup for Seebeck coefficient and electrical resistivity measurements using the four-probe steady-state technique.

Seebeck coefficients. Seebeck coefficients of deposited thin films are measured at room temperature. Measurement data is collected from two different samples of the same wafer to verify uniformity of film properties. In this work, two different methods are used to measure the Seebeck coefficient. In the first procedure, electrical conductivity and Seebeck coefficient are measured simultaneously by the four-probe steady-state technique using a cryostat under vacuum (Figure 3.5). The samples (~ 20 mm long and 4 mm wide) are mounted on the cryostat and protected from radiation loss by radiation shields. One end of the sample (cold side) is attached to a heat sink by indium solder and clamping. Input heat is provided using a micro-heater with a 350 Ω resistance, attached to the back of the opposite end of the sample using varnish. Temperatures of the two contact points, separated by a distance L along the sample, are measured using AuFe-Chromel thermocouples. The heater develops a temperature difference, ΔT, between the two points. Copper (Cu) wires are attached to the contact points of the sample to measure both Seebeck voltage and electrical conductivity because of the low resistivity and small Seebeck coefficient of copper. The cross-section area of sample, A, is used to calculate thin film electrical resistivity. The Seebeck voltage between two contact points, ΔU, is

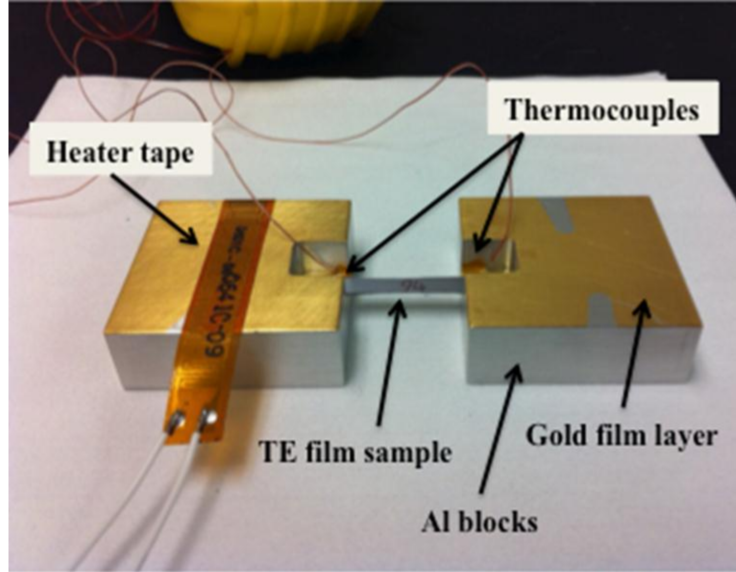


Figure 3.6 Custom test setup for quick and efficient characterization of Seebeck coefficient.

measured using the Cu wires. The Seebeck coefficient of metals including Cu (α_{Cu}) can be found in [6]. The Seebeck coefficient of the film is given by:

$$\boldsymbol{\alpha_S = \frac{\Delta U}{\Delta T} + \alpha_{Cu}} \qquad \textbf{(3.1)}$$

To minimize measurement error, the TE film sample should have a much lower thermal conductivity compared to the metallic probe, so that the temperature difference mainly occurs across the TE film.

In the second procedure, which is a faster measurement technique, two aluminum blocks (5cm×5cm×1.5cm) with cut-out cube-shaped notches (15mm×15mm×5mm) are machined and covered with a thin layer of deposited gold film (Figure 3.6). These blocks are placed about 20 mm apart on a thermally and electrically insulating platform. One of the blocks is kept at room temperature, while the temperature of the other block is varied using an attached heater tape. These temperature values are measured by thermocouples attached to the cube-shaped notches with silver epoxy. The samples (25-30 mm long and

Select Bi_2Te_3 samples	Cryostat measurement α_s (μV/K)	Test Setup measurement α_s (μV/K)	Measurement error (%)
1	-226	-208	7.9
2	-187	-160	14.4
3	-158	-137	13.2
4	-79	-67	15.2

Table 3.3 Comparison of measured Seebeck coefficient values by steady-state cryostat and custom test set-up procedures.

4 mm wide) are placed upside down, hanging off between the blocks while their edges rest on the notches.

In this setup, the TE film on the edges of the sample is in contact with the gold layer covering the blocks. Each side of the sample has the same temperature as the aluminum block at their contact position. Thermocouples are placed very close to the sample edges on the notches to make sure that the temperature difference reading is approximately equal to the two contact points. Seebeck voltage can be measured by probing the gold layer on the blocks close to the contact points. The whole setup is covered during the measurement to reduce radiation loss.

Seebeck coefficients of several samples measured using both procedures are compared to check the reliability of the second measurement technique. It is shown that the Seebeck coefficient values of the test setup measurement have about 8-15% error compared to the cryostat measurement procedure (Table 3.3). However, since the test setup provides an easier measurement platform, it is advantageous for our studies, which involve comparison of many TE, film samples' Seebeck coefficients.

3.3.3.2. Electrical Resistivity

Electrical resistance of the TE film is also measured in the cryostat using the four-point-

probe method at room temperature and under vacuum. As shown in Figure 3.5, electrical current passes through the ohmic contacts at the two ends of the samples. The voltage contact points are positioned away from the current feed contacts to ensure uniform current flow through the voltage probes. The four-point-probe configuration eliminates measurement error caused by the wires and contact resistance. Electrical resistivity is given by the following equation:

$$\boldsymbol{\rho = \frac{RA}{L};\ \ R = \frac{\Delta U}{I}} \qquad \textbf{(3.2)}$$

In this equation, R is the measured electrical resistance, L is the film length between the copper wires used for ΔU measurement, and A is the TE film cross-section area.

There are some additional concerns during measurements due to the thermoelectric nature of these materials. Excessive Joule heating can impose parasitic thermal gradients across the sample. Because of the large Seebeck coefficient of thermoelectric materials, the induced Seebeck voltage is added on top of the resistive voltage. In order to subtract and minimize the error, current flow is reversed quickly and the average of the two readings is reported.

Another source of parasitic temperature difference is generated by the Peltier effect at current contacts. The Peltier effect occurs at the junction between two dissimilar materials, which in this case are the sample and the current leads in the setup, when current is applied. Because the Peltier effect changes linearly with current, current reversal inverses the sign of both the resistive voltage and the Peltier effect, which results in an increase in the actual resistive voltage. Since it takes a while for the thermal gradient to build up due to the Peltier heat, we can deal with this Peltier contribution by

switching the current polarity before a thermal gradient is established.

Therefore, to eliminate error due to the TE material Seebeck voltage and Peltier effect at the current contacts, electrical resistivity is calculated from multiple measurements at different currents in both directions.

Electrical resistivity of TE thin films is also measured quickly at wafer level using Miller FPP-5000 4-Point Probe tool located in the Lurie Nanofabrication Facility (LNF) at the University of Michigan. This tool measures the sheet resistance of the TE film, which should be multiplied by the film thickness to calculate electrical resistivity. The film thickness is obtained using the procedure explained in section 3.3.2.

3.3.3.3. Hall Effect and Carrier Concentration

The Seebeck coefficient is generally inversely proportional to the charge carrier concentration, while electrical conductivity is directly related to the carrier concentration. Therefore, it is important to determine carrier concentration in order to fully characterize a thermoelectric material. For semiconductors of single carrier type, this property can be determined experimentally by Hall effect measurements.

The Hall effect is a conducting phenomenon involving moving charge particles in conductors due to the Lorentz force. If an electric current flows through a conductor in a magnetic field, the magnetic field exerts a Lorentz force on the moving charge carriers, pushing them to one side of the conductor. A buildup of charge on the sides of the conductors balances this magnetic influence, producing a measurable transverse voltage between the two opposite sides of the conductor. The presence of this transverse voltage is called the Hall effect.

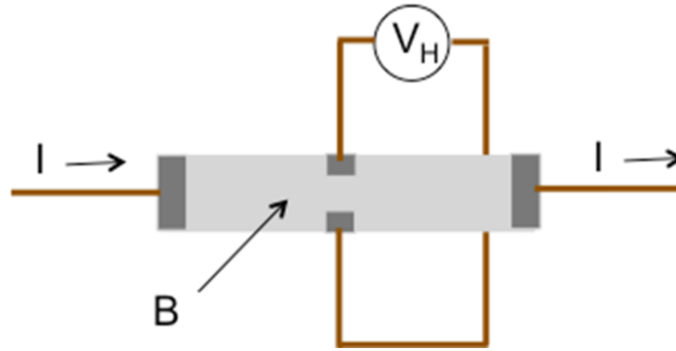


Figure 3.7 Schematic of the Hall effect measurement.

The illustration of Hall coefficient measurement is shown in Figure 3.7. A magnetic field *B* and current *I* are applied, and V_H is measured. The Hall coefficient R_H is defined by the following equation:

$$\boldsymbol{R_H = E/jB.} \qquad \textbf{(3.3)}$$

Charge carriers in a magnetic field *B* are subject to the Lorentz force $F_{Lorentz}$, given by

$$\boldsymbol{F_{Lorentz} = q(v \times B),} \qquad \textbf{(3.4)}$$

where *q* is the charge of a carrier, and *v* is the velocity of carriers. At steady state, electric force (*qE*) counterbalances the Lorentz force $F_{Lorentz}$, enabling continuous current flow. The required electric field *E* is

$$\boldsymbol{E = v \times B.} \qquad \textbf{(3.5)}$$

The velocity of the carriers is related to the current density according to the following equation:

$$\boldsymbol{J = n_c q v,} \qquad \textbf{(3.6)}$$

where n_c is the charge carrier concentration and the electric field can be defined as:

$$\boldsymbol{E = jB/qn_c.} \qquad \textbf{(3.7)}$$

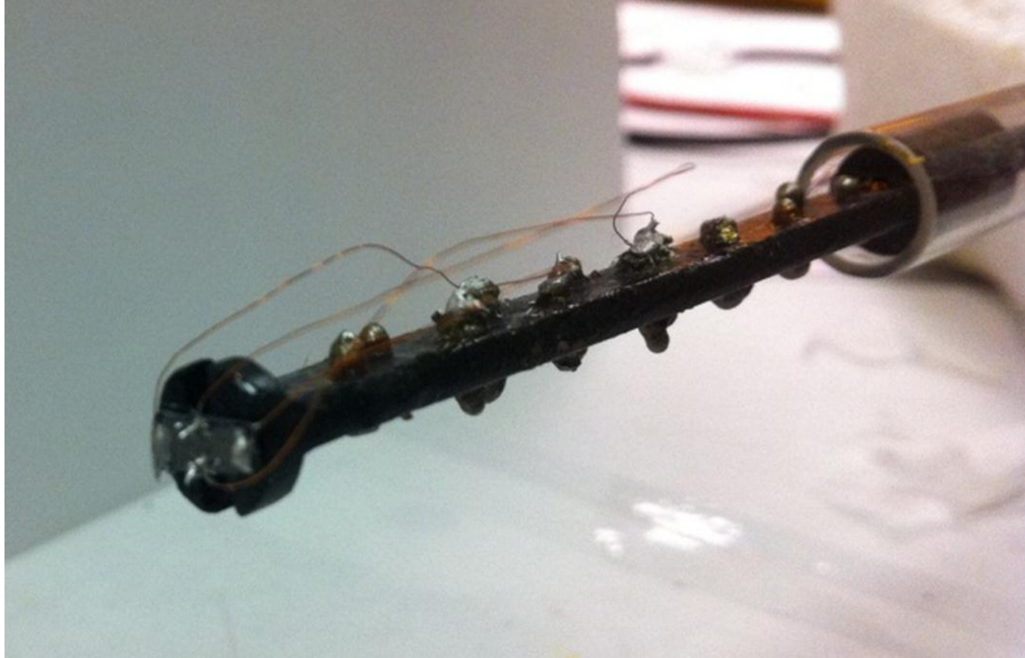


Figure 3.8 TE sample preparation and mounting for Hall coefficient measurement.

Comparing this equation with the Hall coefficient definition, the relationship between carrier concentration and the measured Hall resistance is derived to be

$$R_H = 1/qn_c. \quad \textbf{(3.8)}$$

Carrier mobility, μ, can also be derived from the combined measurements of electrical resistivity ρ and Hall coefficient R_H:

$$\mu = R_H/\rho. \quad \textbf{(3.9)}$$

Figure 3.8 shows the TE sample preparation and mounting for Hall coefficient measurement. Rectangular samples with a size of 6mm×2mm are cut from the wafer with deposited TE film. Four electrical contacts are made to the edges of the sample by indium soldering. Hall effect measurements are performed with a 4-point probe ac technique in a cryostat equipped with a superconducting magnet capable of fields up to 5 Tesla for the temperature range of 10-300 K.

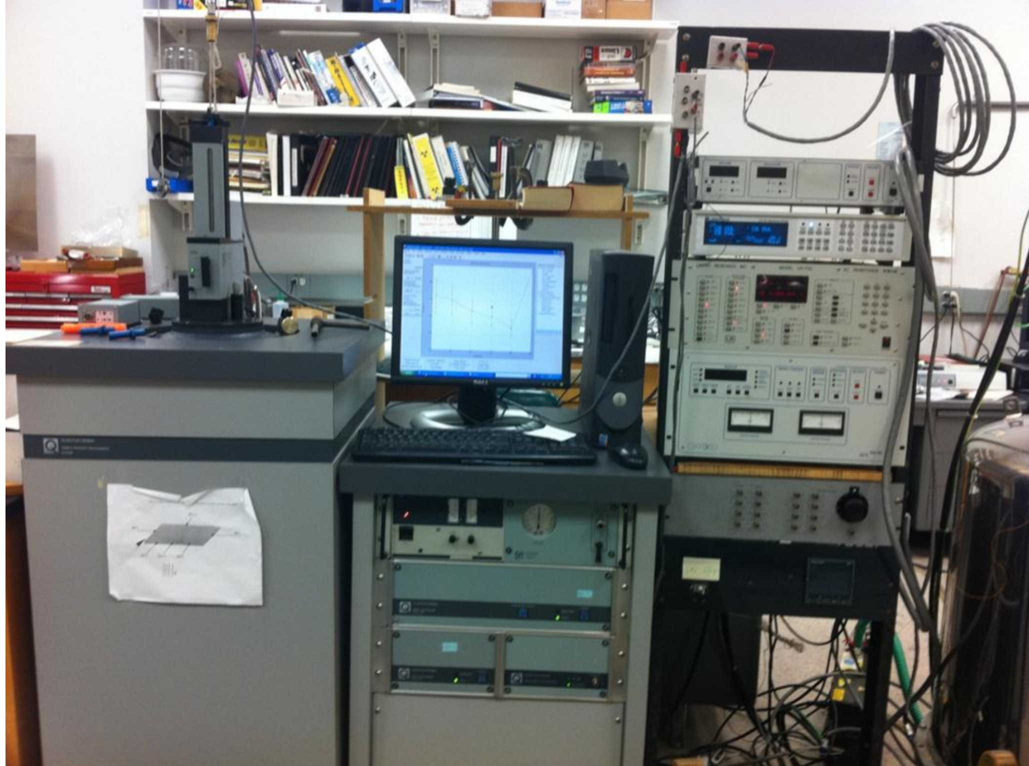


Figure 3.9 Magnetic Property Measurement System (MPMS) setup.

The Magnetic Property Measurement System (MPMS) for Hall coefficient characterization is shown in Figure 3.9. R_H data are taken in both magnetic field directions to eliminate effects due to any probe misalignment. Hall coefficient measurements above 200 K are quite noisy, which limits the accuracy of data collection for (Bi,Sb)Te-based TE thin films. It is suspected that the indium and/or silver epoxy electrical contacts to the TE film sample become loose during sample mounting and cause the observed noise. Better Ohmic contacts by careful soldering or contact metal deposition on the TE film can reduce measurement error.

The TE film sample resistivity measurement over the temperature range of 10-300 K can usually be done together with Hall measurements. However, the restriction on the sample size in the MPMS causes technical difficulties for indium Ohmic contact formation and

wire bonding to implement the resistivity measurement. In the future, the resistivity measurements must be performed in a cryogenic vacuum probe-station to calculate the carrier mobility and complete the characterization of TE thin films.

3.4. Summary

Thermal co-evaporation is an attractive deposition technique for TE thin films because of the relatively high film quality, simple vacuum deposition technology, ease of process control and configurability, and compatibility with post-CMOS processing. Detailed procedure of thin film deposition by thermal evaporation and the tool for this purpose were explained. This deposition method is able to produce TE material with figures-of-merit comparable to other expensive and complicated deposition techniques. Thus, thermal co-evaporation is regarded as one of most promising methods for preparing (Bi,Sb)Te-based thin films with high quality for microsystem applications.

Specific characterization methods for TE thin films have been described in this chapter. The measurement techniques for Seebeck coefficient and electrical resistivity are explained in detail and used to analyze TE performance of different samples. Test set-ups for quick and efficient characterization and comparison of several TE properties are introduced. SEM and EDS analysis show the morphology and composition of the films, while X-ray diffraction is used to verify the orientation and quality of thin film crystals. The characterization techniques reported here are used to analyze the performance of TE thin films on various substrates in Chapter 4.

Chapter 4

Effect of Substrate on the Characteristics of Co-evaporated (Bi,Sb)Te-based Thin Films

Many thermoelectric devices especially in micro-scale systems use lateral instead of vertical structures, meaning that the TE elements are laid down on a substrate between hot and cold junctions. Since TE film thickness deposited by co-evaporation is limited, lateral TE elements have higher aspect ratio compared to the vertical ones resulting in higher efficiency and lower power consumption in the thermoelectric module.

However, the drawback of lateral TE design is that another material should be used under the TE elements as the structural support between the two junctions. Ideally, TE elements must be the only materials spanning between isothermal islands, but due to their poor mechanical properties, suspending TE material without a supporting layer is not possible. On the other hand, increased parasitic thermal conductance through this supporting layer reduces the difference and degrades device efficiency. Therefore, the choice of supporting material in lateral designs is crucial to minimize parasitic thermal conduction and optimizing device efficiency.

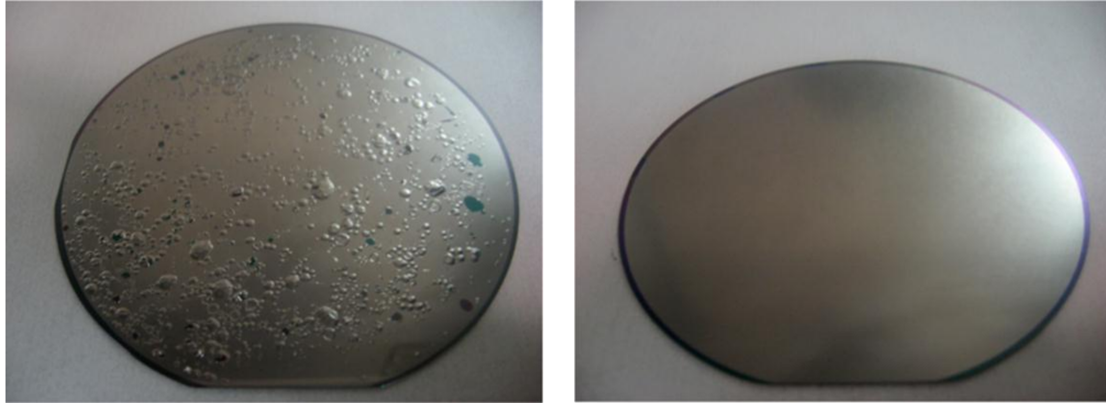
Furthermore, although the substrate does not have an adverse effect on the thermal conduction between hot and cold junctions in vertical thin film structures, it has been

shown that they could still affect other characteristics of the TE device such as flexibility, CMOS-compatibility, and heat sink and heat source performance (Table 1.1 and Table 1.2). As a result, the choice of substrate is an important and critical step in the design of vertical TE modules as well.

4.1. Micro Thermoelectric Thin Film Device Substrates

High-quality thermoelectric thin films with good adhesion and uniformity are needed on a variety of substrates in order to provide design flexibility in microsystems. In a previous work at the University of Michigan, silicon dioxide was chosen as the underlying layer in the planar micro thermoelectric cooler for several reasons. First, it has a low thermal conductivity of approximately 1.1 W/m-K [74], which is close to the thermal conductivity of (Bi,Sb)Te-based TE materials. In addition, silicon dioxide is a standard material in micro-fabrication processes with well-characterized deposition techniques. Finally silicon dioxide has a very high thermal tolerance and is appropriate for the high temperature co-evaporation process of TE materials. Other materials such as silicon, silicon nitride and polymers were not selected for this device for various reasons. Silicon and silicon nitride have been used extensively in MEMS devices, but both have thermal conductivities that are much greater than silicon dioxide's. Polymers such as Parylene and polyimide have thermal conductivities as low as 0.12 W/m-K [74], but they cannot withstand high temperatures during deposition of the TE materials.

Silicon dioxide substrates for deposition of Bi_2Te_3 and Sb_2Te_3 materials were prepared by PECVD process. However, deposited TE films, especially Sb_2Te_3, showed extremely poor adhesion on PECVD oxide even at low deposition temperatures. Although these films did not peel off the oxide substrate, many cracks and bubbles appeared on the



(a) **(b)**

Figure 4.1 (a) Sb_2Te_3 thin films on PECVD SiO_2/Si. (b) Sb_2Te_3 thin films on LPCVD SiO_2/Si.

surface of these films (Figure 4.1(a)). *In situ* RF plasma cleaning was applied to these substrates before TE film deposition, which did not improve the film adhesion significantly.

To solve this problem, an LPCVD process was used to deposit silicon dioxide on Si wafers ((Figure 4.1(b)). The TE films co-evaporated on LPCVD oxide substrates exhibit much better adhesion and TE properties compared to those on PECVD oxide substrates. The LPCVD process produces oxide layers with excellent uniformity of thickness and material characteristics. The process requires high deposition temperature (~ 600°C) and the relatively slow deposition rate. The PECVD process can operate at lower temperatures (~ 300° C) due to the extra energy supplied to the gas molecules by the plasma in the reactor. However, the quality of the oxide films tends to be inferior to processes running at higher temperatures. PECVD oxide films are less dense and might contain pinholes and contamination.

In addition to adhesion problems, deposition of Sb_2Te_3 thin films on silicon dioxide substrate exhibits mechanical stress issues. During fabrication of the micro-cooler device

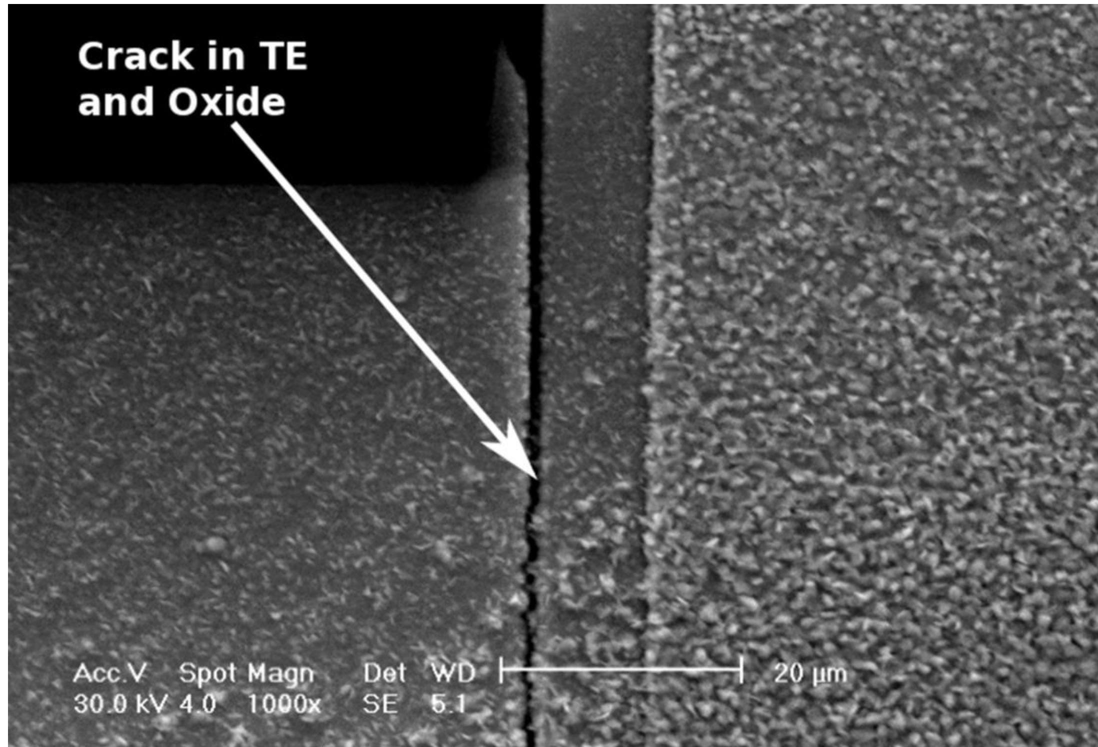


Figure 4.2 Cracks on the Sb_2Te_3 thin film and the underlying oxide layer.

previously accomplished at the University of Michigan [42], widespread cracks appeared in the Sb_2Te_3 thin film and the underlying oxide layer (Figure 4.2). These cracks happened in all Sb_2Te_3devices after releasing from the Si substrate and removing the protective photoresist layers on top of the films, whereas Bi_2Te_3 films did not have any cracks or mechanical stress problems.

Intrinsic stress of both Bi_2Te_3 and Sb_2Te_3 films were measured using the Flexus 2320-S equipment located at the Lurie Nanofabrication Facility at the University of Michigan. This equipment can measure changes in the radius of curvature of a substrate. First the curvature of the Si wafer coated with LPCVD oxide was measured. After deposition of the TE thin film, the curvature of the wafer was measured again. The difference between these two measurements indicates the intrinsic stress of TE films. Bi_2Te_3 thin films

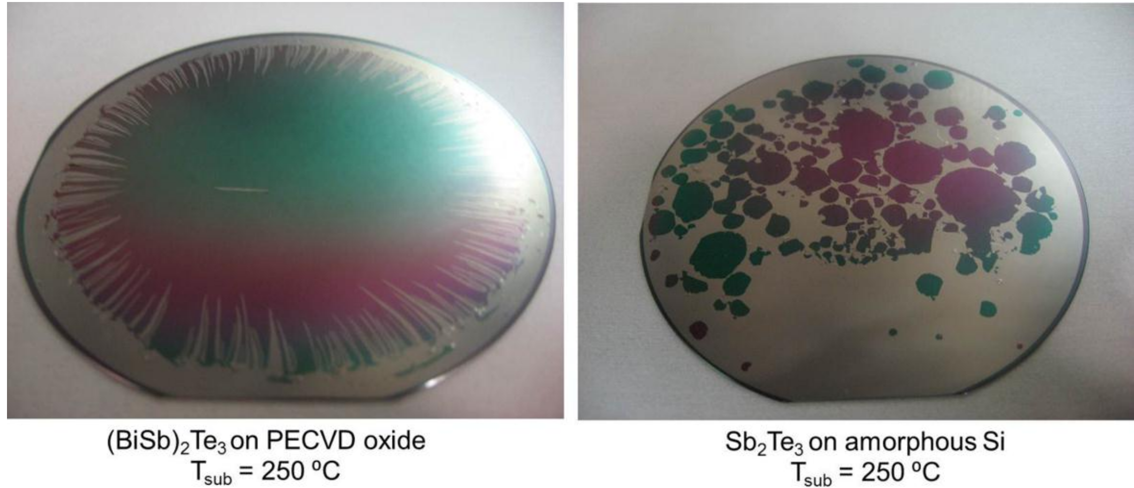


Figure 4.3 Delamination of TE thin films on two different substrates due to stress/adhesion.

deposited under optimal co-evaporation condition had a tensile stress of 65 MPa, while the optimum Sb_2Te_3 thin films had a tensile stress of 128 MPa - about twice as much as the Bi_2Te_3 films, leading to the mentioned cracks.

In addition to the material type, deposition temperature influences the intrinsic stress of the TE films such that co-evaporation at lower substrate temperatures reduces the TE film stress level. Although optimum Sb_2Te_3 films had been co-evaporated at T_{sub}= 250 °C, stress measurement of films deposited at lower temperatures showed tensile stresses of 90 MPa and 65 MPa at T_{sub}= 220 and 200 °C, respectively. Therefore, it might often be necessary to compromise on the performance of TE thin film to minimize the stress and avoid the device failure.

These experiments on (Bi,Sb)Te-based materials' co-evaporation showed that optimal deposition conditions for TE film on a specific substrate may not necessarily provide the best TE material on a different substrate. In addition, such optimal deposition conditions may produce a TE film with poor adhesion or high intrinsic mechanical stress. Therefore,

switching a substrate based on a new application and device leads to many challenges in (Bi,Sb)Te-based thin films. There will be variations in their adhesion and stress due to CTE mismatch, in addition to different optimal co-evaporation conditions for each substrate. For instance, delamination of two TE thin films on different substrates due to stress/adhesion is shown in Figure 4.3.

As mentioned before, due to mechanical limitations of the TE material, it is not possible to suspend it without using a supporting layer. Using advanced etching tools, the substrate thickness can be reduced such that its parasitic thermal resistance and thus its adverse effect on the device efficiency become negligible. Therefore, (Bi,Sb)Te-based films with optimal performance on oxide substrate might lead to devices with TE elements that have minimal support and are almost suspended.

Increasing the application of flexible TE microsystems necessitates incorporation of TE materials onto new, flexible substrates. Deposition of a high-quality TE film onto a soft and bendable substrate enables a new class of flexible micro thermoelectric coolers and generators. Silicon, oxide and glass are all standard materials in micro-fabrication process and suitable for high temperature during TE materials co-evaporation, but they are all rigid and not suitable for flexible device fabrication.

A flexible substrate with high temperature tolerance is required for fabrication of flexible thermoelectric devices. Polyimide (Kapton®) material can be used as the substrate in these TE applications, since it is flexible and remains stable over a wide range of temperatures, from -273 to +400°C. Furthermore, the low thermal conductivity of Kapton® (~ 0.38 W/m·K) together with its good dielectric qualities and its availability in thin sheets have made it a favorite material in cryogenic applications. Polyimide

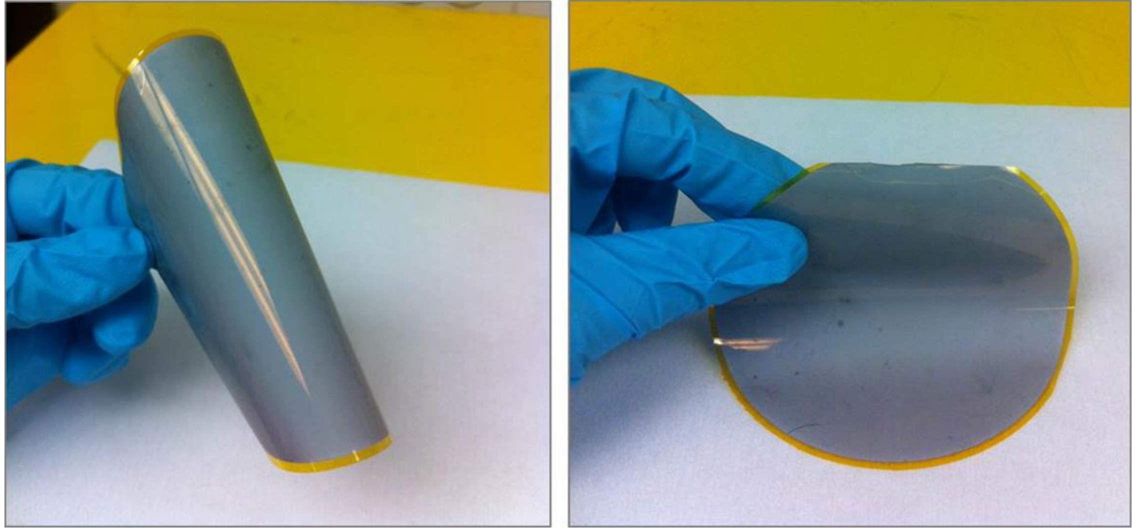


Figure 4.4 Bi_2Te_3 thin film on flexible Kapton® substrate.

(Kapton®) also has a very low outgassing rate, which is desirable in high-vacuum systems, such as the thermal evaporator deposition chamber used for TE materials.

On the other hand, TE thin films themselves have brittle structures in addition to other issues such as sticking to the polymer substrate and high stress. Therefore, co-evaporation of these brittle (Bi,Sb)Te-based thin films on flexible polyimide is carefully characterized to satisfy the flexibility requirements of the final TE device. Figure 4.4 shows Bi_2Te_3 thin film on Kapton® substrate with optimal co-evaporation conditions. Co-evaporation of TE film on polyimide is carried out by cutting 4-inch circle out of the 25 μm thick Kapton® sheet and attaching it to a Si carrier wafer using clamps. As can be seen, there are no cracks and/or delamination effect in Bi_2Te_3 thin film even when the polymer substrate is bent.

Finally, Bi_2Te_3 and Sb_2Te_3 thin films have shown high TE quality on glass substrates [21]. However, good TE film adhesion and optimal properties are not uniform across the glass substrate. TE film inconsistency is because of the low thermal conductivity of the

thick glass wafer which leads to a considerable temperature difference across its two ends [51].

This chapter reports on the effects of substrate materials and crystallinity on the properties of *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 thin films prepared by thermal co-evaporation.

4.2. Substrate Preparation for Bi_2Te_3 and Sb_2Te_3 Films Deposition

Structure and properties of films can be dependent on the state of the surface on which they are deposited. A single crystal, an amorphous material, or a polycrystalline material substrate of the same composition may produce different types of film crystal structure and characteristics. Also, the geometry of the interface between two solids, the terminating layer of the substrate, and lattice mismatch influence the film growth conditions as well [88].

As mentioned before, studied substrates include silicon dioxide (SiO_2/Si), glass, poly-silicon, amorphous silicon, and polyimide (Kapton®) film. Silicon dioxide (SiO_2) films with thickness of ~ 1 μm are deposited on 500 μm silicon wafers using both PECVD and LPCVD techniques. Due to poor TE thin film quality on PECVD oxide, as illustrated in Figure 4.1(a), only TE samples on LPCVD oxide are characterized in this chapter. Both amorphous Si and poly-silicon are also prepared by LPCVD. First, about 1 μm LPCVD Oxide is deposited on Si wafer. Next, amorphous or poly-crystalline Si layer are deposited by LPCVD at different temperatures. Half-micron amorphous Si and 0.75 μm poly-Si layers are deposited at furnace temperatures of 560 and 685 °C, respectively.

Both glass wafers and polyimide (Kapton®) sheets have low thermal conductivity. Direct placement of these wafers in the deposition chamber, without attachment to a high thermal conductivity material, results in non-uniform temperature distribution during co-evaporation and TE film inhomogeneity. In order to address this problem, a Si wafer is bonded to the 500-µm glass wafer using anodic bonding. The high thermal conductance of the Si wafer distributes the temperature across the glass substrate evenly during the co-evaporation process.

In the process of optimizing (Bi,Sb)Te-based TE films' figure of merit on each substrate, deposition conditions such as the substrate temperature and evaporation rate of individual elements are studied. Furthermore, the effect of substrate on TE film properties including electrical resistivity, Seebeck coefficient, chemical composition, grain size, and crystal structures are analyzed. Experiments and results in this chapter show that the morphology, grain size, stoichiometry, and thermoelectric properties of thin films depend strongly on substrate material and deposition conditions.

4.3. Deposition Conditions of Binary TE Films

The work in [51] characterized properties of binary TE materials on silicon dioxide substrate for various deposition conditions, such as substrate temperature and flux ratio, and determined the best deposition conditions for each material. The best Bi_2Te_3 films were produced at a substrate temperature of 260 °C with a $FR_{(Bi:Te)}$ of 1:2.4, and produced a film with a power factor of 2.3 mW/K^2 m. Similarly, based on these experiments the best Sb_2Te_3 films were produced at a substrate temperature of 230 °C with a $FR_{(Sb:Te)}$ of 1:3, and produced a film with a power factor of 1.9 mW/K^2 m.

In this work, we started by reproducing optimal Bi_2Te_3 and Sb_2Te_3 thin films using the new thermal evaporation system explained in Section 3.2. In the process of optimizing binary TE films, higher evaporation rates for individual elements were investigated to accelerate the deposition process, reduce deposition time and increase the lifetime of crystal monitors for co-evaporation of thicker TE films. Examined evaporation rates were between 2 and 3 times higher than optimal values. For instance, a Bi evaporation rate of 4 Å/s and Te evaporation rate of 6 Å/s were used instead of 2 Å/s and 3 Å/s, respectively. The composition analysis of these films compared to those deposited at lower rates, shows that the atomic percentage of elements is slightly off from stoichiometry values. TE properties, i.e. Seebeck coefficient and electrical resistivity, also degrade from the optimal values. Therefore, unless very thick films are required for a specific process, it is preferable to keep the elemental evaporation rates at their lower optimal values.

The relationship between the deposited film thickness and its TE properties has been studied before [51]. In the thickness range between 0.75 and 4 μm, there are no distinguishable correlations between the TE properties and film thickness. Therefore, TE films with a thickness of around 1 μm have been co-evaporated and characterized in this work as a representative of all thickness values in that range.

4.3.1. Reproducibility of the Thermal Co-evaporation Process

One of the crucial requirements in TE thin film experiments is reproducibility of material characteristics for a standard recipe between different deposition runs. Therefore, in this work, binary TE materials are co-evaporated with the same conditions at different times to investigate reproducibility of the results on a routine basis. Reproducing results for TE thin films require careful control of substrate preparation and deposition conditions. The

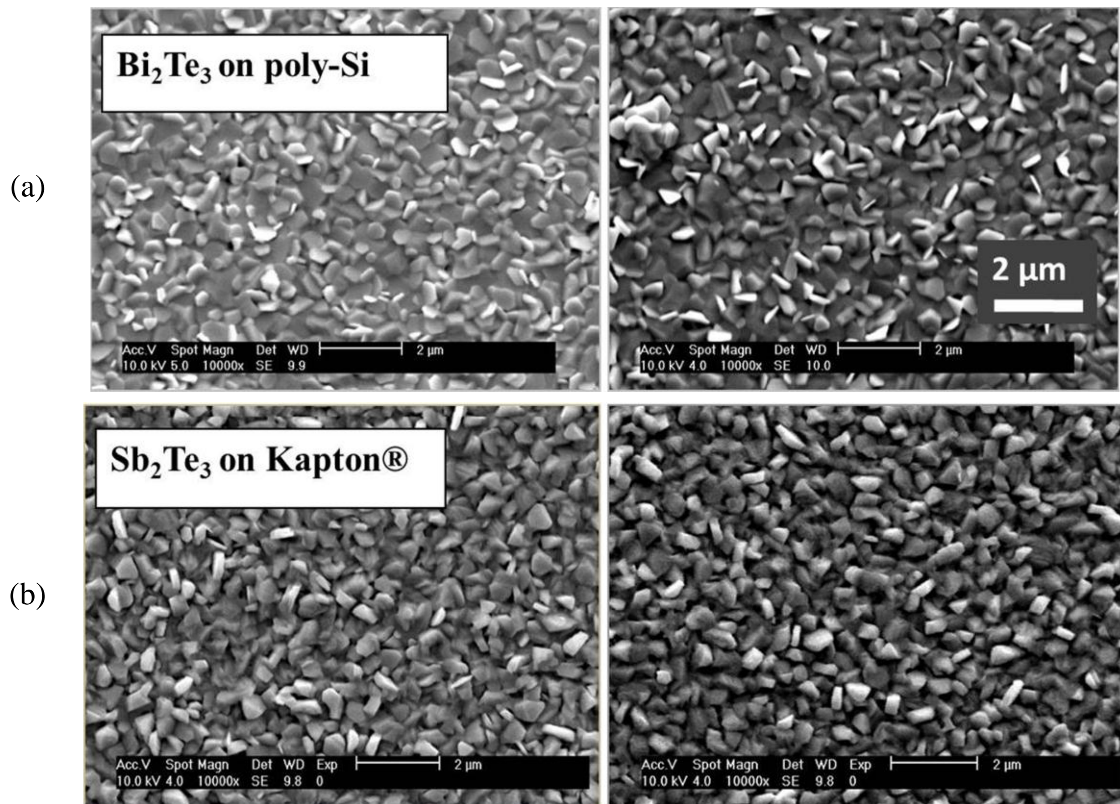


Figure 4.5 Surface SEM micrographs of TE films (a) Bi_2Te_3 and (b) Sb_2Te_3 co-evaporation at identical deposition conditions.

basic challenge originates from the high sensitivity of TE film preparation and characteristics to the environmental and substrate condition. The reproducible measurements are obtained by co-evaporation of Bi_2Te_3 and Sb_2Te_3 thin films using standard recipe at the following deposition conditions:

- Bi_2Te_3 thin film at T_{sub} = 270 °C and $FR_{(Bi:Te)}$=1:3 on poly-Si substrate.
- Sb_2Te_3 thin film at T_{sub} = 250 °C and $FR_{(Sb:Te)}$=1.5:3 on Kapton® substrate.

The procedure for preparation and loading of poly-Si substrates in the co-evaporation tool is kept as identical as possible. Similar careful preparation is carried out in preparation of Kapton® substrates for Sb_2Te_3 deposition. The similar TE films are deposited several days apart.

Material	Substrate	T_{sub} (°C)	$FR_{(Bi/Sb:Te)}$	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^2m)	At% (Bi/Sb:Te)
Bi_2Te_3	Poly-Si	270	1:3	10.5	-180	3.08	39.2 : 60.8
				11.7	-188	3.02	38.6 : 61.4
Sb_2Te_3	Kapton®	250	1.5:3	40.8	186	0.85	35.9 : 64.1
				35.3	178	0.89	34.3 : 65.7

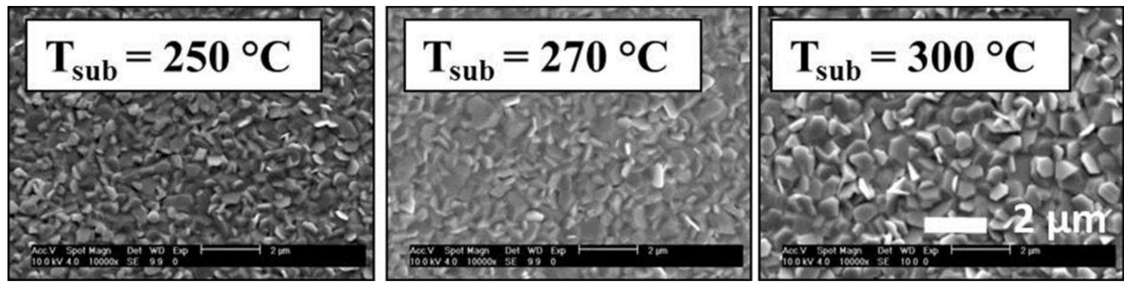
Table 4.1 TE properties and composition of Bi_2Te_3 and Sb_2Te_3 thin films at identical deposition conditions.

The surface SEM micrographs of Bi_2Te_3 and Sb_2Te_3 thin films in Figure 4.5 and the corresponding characteristics in Table 4.1 show very close crystal structure, composition and TE properties for the samples produced at identical deposition condition. The similarity of TE thin films prepared by carefully controlling the deposition conditions for a given recipe confirms the reproducibility of thermal co-evaporation process.

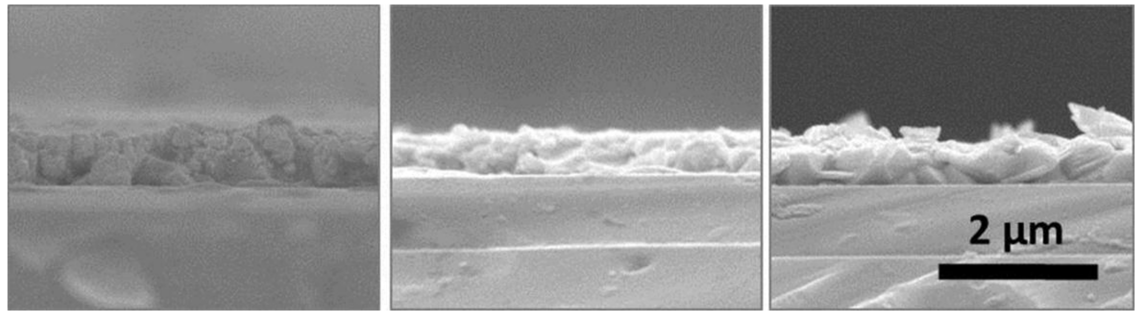
4.4. Optimal Deposition Parameters for Bi_2Te_3 Films

Bismuth telluride films with a thickness of ~ 1 μm ± 20% are deposited on different substrates, at various substrate temperatures. Elemental FR has been slightly varied to find the film with stoichiometric composition.

4.4.1. Effect of Substrate Temperature and Film Composition



(a)



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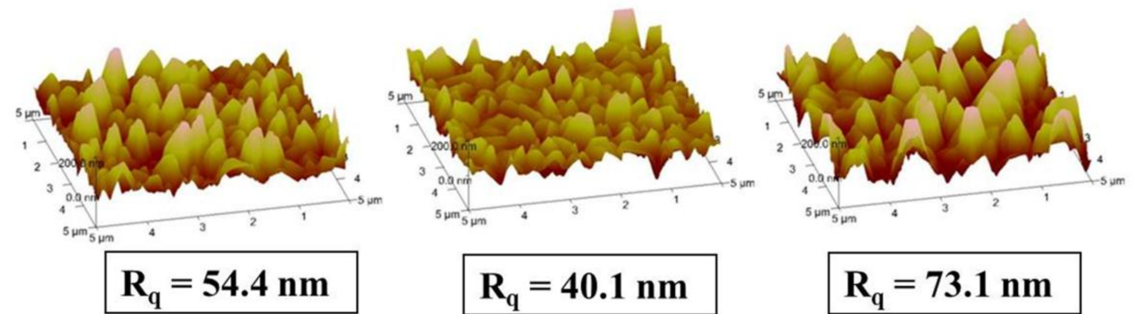


(c)

Figure 4.6 (a) Surface SEM micrographs of Bi_2Te_3 films deposited on SiO_2/Si substrate at various temperatures and $FR_{(Bi:Te)}$ of 1:3. (b) Cross-sectional images of these films. (c) AFM images of Bi_2Te_3 film surface roughness.

Substrate temperature is one of the most important parameters governing thin film properties. It controls the composition, structure, and morphology of the film by affecting the mobility of the atoms lying on the surface as well as the rate of any chemical reaction occurring on the substrate [88]. For each substrate material, the effects of substrate temperature and film composition are studied to optimize film properties. Deposition temperature for Bi_2Te_3 thin films varies between 220, 250, 270 and 300 °C. Elemental fraction ratio, $FR_{(Bi:Te)}$, is set to 1:4, 1:3 and 2:3 to find the optimal composition [33].

T_{sub} (°C)	FR(Bi:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Bi:Te)
250	1:3	14.7	-161.7	1.778	38.2 : 61.8
270	1:3	19.1	-210	2.309	39.1 : 60.9
300	1:3	72.2	-191.7	0.508	38.7 : 61.3

Table 4.2 Measured optimum TE properties of co-evaporated Bi_2Te_3 films deposited on oxide substrates at T_{sub} = 250, 270 and 300 °C.

Initial studies have shown that the Seebeck coefficients of Bi_2Te_3 films are negative indicating that they are *n*-type material. The surface SEM micrographs of select Bi_2Te_3 films deposited on SiO_2/Si substrates with similar FRs at T_{sub}= 250, 270 and 300 °C are shown in Figure 4.6(a). These images show that for low values of T_{sub}, grains are small and their boundaries are blurry. The cross-sectional images in Figure 4.6(b) further illustrate the effect of substrate temperature during co-evaporation on the film grain size and crystal orientation.

The Seebeck coefficient of Bi_2Te_3 samples is negative indicating that the films are *n*-type. This coefficient increases to its maximum value with T_{sub} at 270 °C. Electrical resistivity does not change considerably for T_{sub} < 270°C, but increases significantly for T_{sub} = 300°C. The reason is that at higher temperatures, Te can re-evaporate from the substrate leaving point defects such as an antisite defect in the crystal structure, resulting in the sharp increase of resistivity. AFM images of Bi_2Te_3 samples surface roughness are shown in Figure 4.6(c). AFM analysis also shows TE film variation based on deposition temperature. As the substrate temperature increases up to 270°C, surface roughness decreases slightly, however when T_{sub} goes above 270°C, the average film roughness increases.

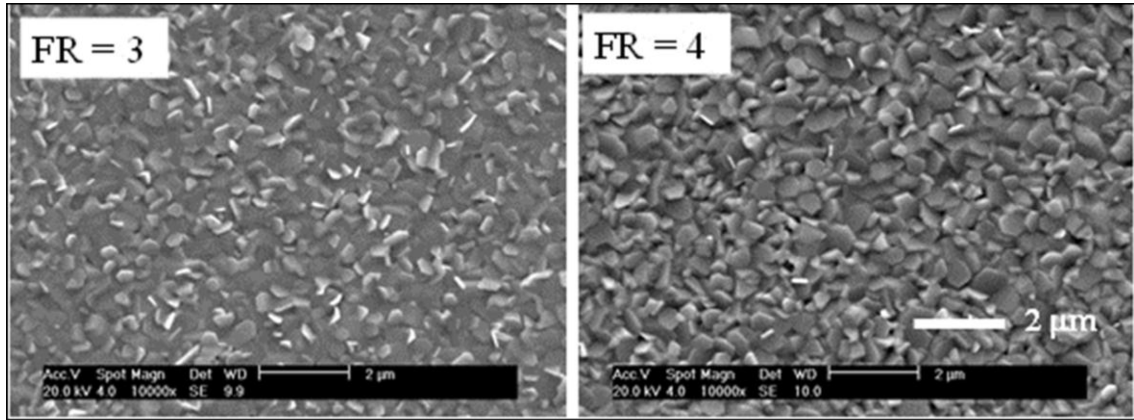


Figure 4.7 Top surface SEM micrographs of Bi_2Te_3 films deposited at T_{sub}= 270 °C.

TE properties of these Bi_2Te_3 samples along with their composition are summarized in Table 4.2. The maximum power factor for Bi_2Te_3 thin film on SiO_2/Si substrate is 2.3 mW/K^2 m deposited at T_{sub} = 270°C with $FR_{(Bi:Te)}$ = 1:3. The optimum Bi_2Te_3 thin film also has Te atomic percentage very close to the stoichiometry value (39.1:60.9) compared to the samples deposited at other substrate temperatures. The tellurium atomic percentage in non-optimal samples is still lower than 62%. Due to re-evaporation of Te from substrate especially at higher T_{sub}, which leads to point defects such as antisites and vacancies and thus increases in resistivity, it is not possible to develop Bi_2Te_3 films with Te atomic percentages of much higher than 60%.

The elemental fraction ratio (FR) for co-evaporation of Bi_2Te_3 thin film on silicon dioxide substrates has been varied between 2 to 4 to find the optimum composition. For FR < 3, the composition of Bi_2Te_3 does not vary significantly due to re-evaporation of Te. For FR = 4, the excess tellurium accumulates on the substrate, resulting in poor thermoelectric properties.

In addition to the Bi_2Te_3 compound, atomic Te also condenses on the substrate, which can be verified by x-ray diffraction analysis. The top surface SEM micrographs of Bi_2Te_3

T_{sub}	FR(Bi:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Bi:Te)
270	1:3	19.1	-210	2.309	39.1 : 60.9
270	1:4	19.2	-122	0.775	37.5 : 62.5

Table 4.3 Measured TE properties of co-evaporated Bi_2Te_3 films deposited on oxide substrates at T_{sub} = 270 °C.

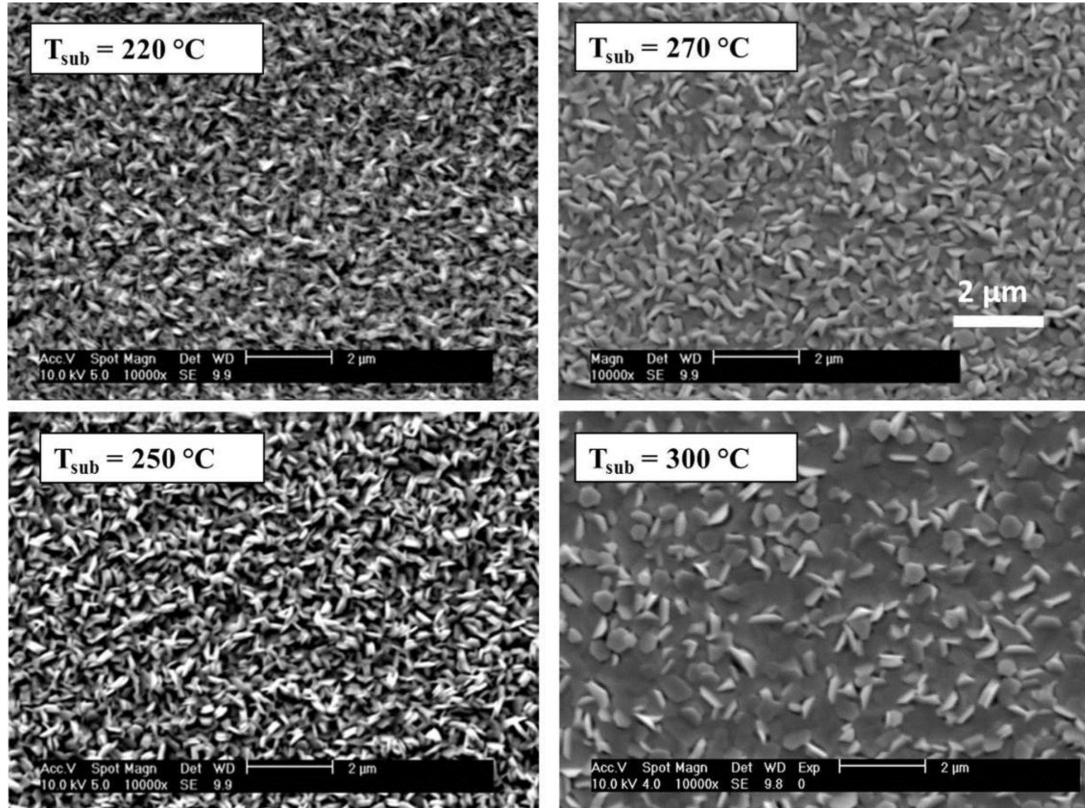


Figure 4.8 Surface SEM micrographs of co-evaporated Bi_2Te_3 films on Kapton® substrate for various temperatures.

films deposited at T_{sub}= 270 °C with FR=3 and 4 are shown in Figure 4.7.

Furthermore, properties and composition of these Bi_2Te_3 samples are summarized in Table 4.3. The grain size slightly increases with FR, but the Seebeck coefficient decreases in this case despite larger grain size. This is because the high FR resulted in high atomic concentration of Te in the Bi_2Te_3 thin film, which caused reduction of both the Seebeck coefficient and resistivity.

T_{sub} (^{0}C)	FR(Bi:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Bi:Te)
220	2:3	18.3	-176	1.693	38.8 : 61.2
250	2:3	13.3	-180	2.436	39.9 : 60.1
270	2:3	20	-250	3.125	38.5 : 61.5
300	2:3	31.2	-208	1.387	38.6 : 61.4

Table 4.4 Properties of evaporated Bi_2Te_3 films on Kapton® substrate.

Surface SEM micrographs of co-evaporated Bi_2Te_3 films on Kapton® substrate and their properties are summarized in Figure 4.8 and Table 4.4, respectively.

The substrate temperature affects the grain structure of Bi_2Te_3 films, and as can be seen in Figure 4.8, for low T_{sub}, grain size is small, the grain boundaries are blurry and film has an amorphous structure. As T_{sub} increases from 220 °C, the grain size increases and charge carriers boundary scattering tends to reduce. As a result, the charge carrier mobility increases and lowers electrical resistivity. Growth of grain size also decreases carrier concentration and increases the Seebeck coefficient of TE samples. As shown in Table 4.4, electrical resistivity increases for Bi_2Te_3 deposited at T_{sub} = 270 °C. This is because with increasing grain size, the effect of reduction in carrier concentration dominates the effect of increase in carrier mobility, leading to an overall increase in resistivity.

The absolute value of the Seebeck coefficient increases with substrate temperature for all different substrates. Optimum film composition on Kapton® is obtained at elemental fraction ration of $FR_{(Bi:Te)}$ = 2:3. The cross-sectional view of samples deposited at T_{sub} = 220 and 270 °C (Figure 4.9) demonstrate that as the deposition temperature increases, the

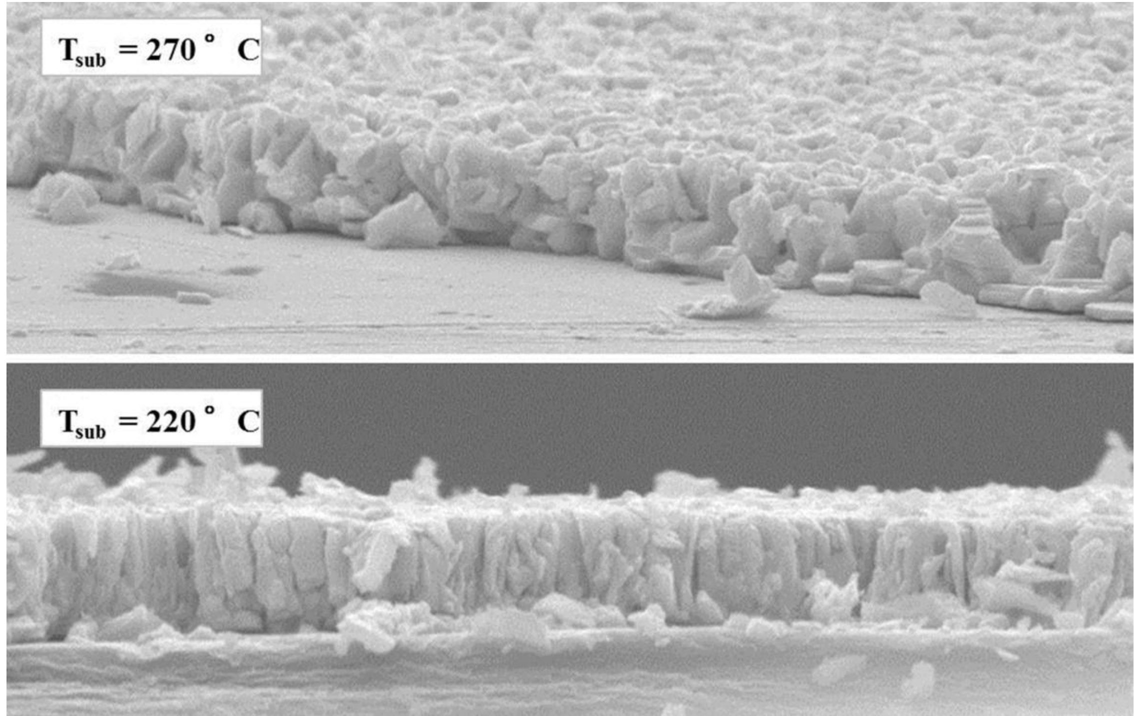


Figure 4.9 Cross-sectional view of samples deposited at T_{sub} = 220 and 270 °C on Kapton® at elemental fraction ration of $FR_{(Bi:Te)}$ = 2:3.

amorphous structure of the film with fuzzy grain boundaries transform into a poly-crystalline film, with well-defined grain boundaries.

The power factor values start degrading for the Bi_2Te_3 films deposited at T_{sub} = 300 °C on all substrates. This is mainly due to the sharp increase in the electrical resistivity of the films. The increase of resistivity for Bi_2Te_3 films deposited at $T_{sub} > 270$ °C is caused by re-evaporation of Te from the substrate at these higher deposition temperatures and generation of defects in the crystal structure, opposing the effect of larger grain size.

Similar behavior has been observed for Bi_2Te_3 films deposited on SiO_2/Si substrates as discussed in Section 4.4.1. The maximum Seebeck coefficient is still obtained at T_{sub} = 270 °C, which results in optimum power factor.

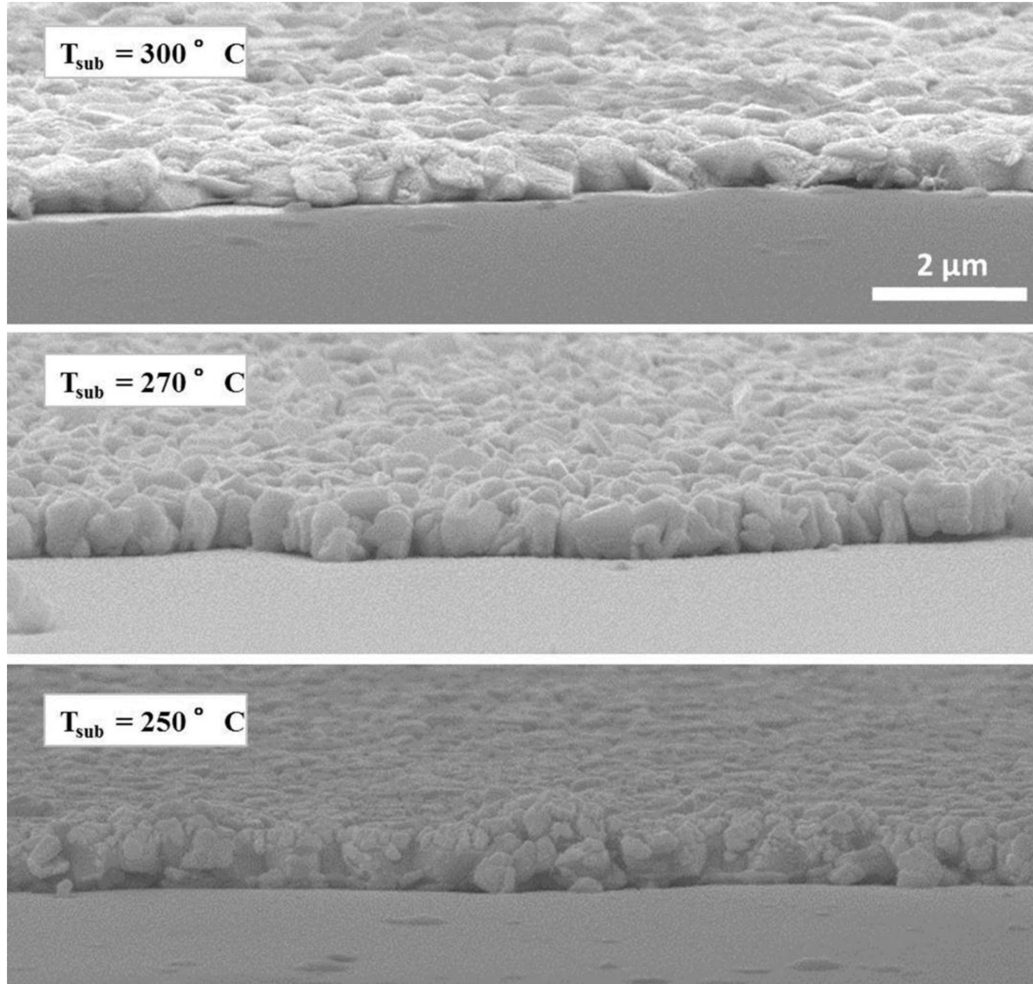


Figure 4.10 Cross-section SEM micrographs of the co-evaporated Bi_2Te_3 material on oxide substrate at various temperatures.

The cross-section SEM micrographs of the co-evaporated Bi_2Te_3 material on oxide substrate in Figure 4.10 show transformation of the film crystal structure by temperature. Similarly, at low deposition temperatures, grains are small and TE film has an amorphous crystal structure. At T_{sub} = 270 °C, grain boundaries become more clear, the grain size increases and TE properties enhance. As mentioned before, at higher deposition temperature (T_{sub} = 300 °C), re-evaporation of Te makes the film grainy and resistivity increases abruptly (ρ = 72.2 μΩ-m).

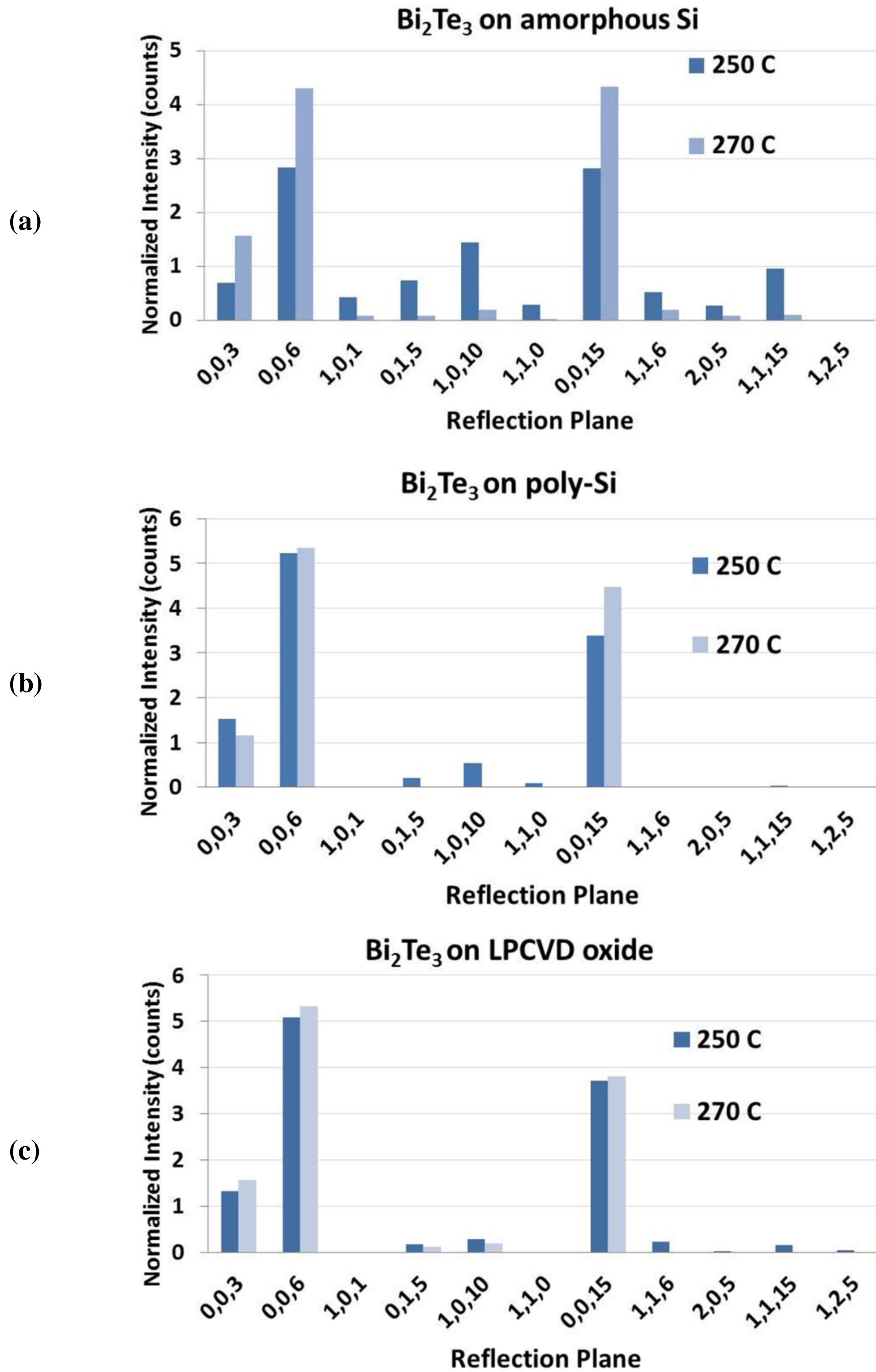


Figure 4.11 Normalized diffraction pattern of the Bi_2Te_3 films on (a) amorphous Si, (b) poly-Si, and (c) LPCVD oxide substrates.

Similar behavior has been observed for Bi_2Te_3 films deposited on amorphous Si, poly-Si

and glass substrates with optimal TE properties at T_{sub} = 270 °C and $FR_{(Bi:Te)}$ = 1:3. Changing FR between 1.5 and 3.0 does not have noticeable effect on the atomic concentrations of Bi and Te, indicating re-evaporation of tellurium. Because of this phenomenon, the atomic percentage of Te in all films deposited at different temperatures does not significantly exceed 60%.

Normalized diffraction patterns of Bi_2Te_3 films on amorphous Si, poly-Si, and LPCVD oxide substrates are shown in Figure 4.11(a), (b) and (c). For all substrates, the position of the peaks agrees with the Powder Diffraction File reference for Bi_2Te_3. It can be seen that the diffraction peaks corresponding to *(0,0,l)* planes are more pronounced and their intensity increases with higher deposition temperature. The high intensity of these peaks indicates a preference for *c*-axis orientation. The peaks are dominant at 270 °C for all three substrates, which also corresponds to the optimal measured TE properties.

4.4.2. Effect of Substrate Material and Crystal Structure

Bi_2Te_3 thin films are deposited on LPCVD oxide, glass, amorphous Si amorphous Si, poly-Si and polyimide (Kapton®) and optimized over a range of substrate temperature and elemental fraction ratios. The effect of substrate material and crystallinity on characteristics of Bi_2Te_3 thin films is analyzed at the optimum point.

SEM micrographs of Bi_2Te_3 film surfaces and cross-section of these different substrates are shown in Figure 4.12, illustrating grain size and crystal structure variations. In addition, film properties at optimal deposition conditions on various substrates are summarized in the Table 4.5. All these films have compositions with Te atomic percentage of around 60%. Finally, the effect of substrate material and deposition temperature on power factor for thermal co-evaporation of Bi_2Te_3 thin film is

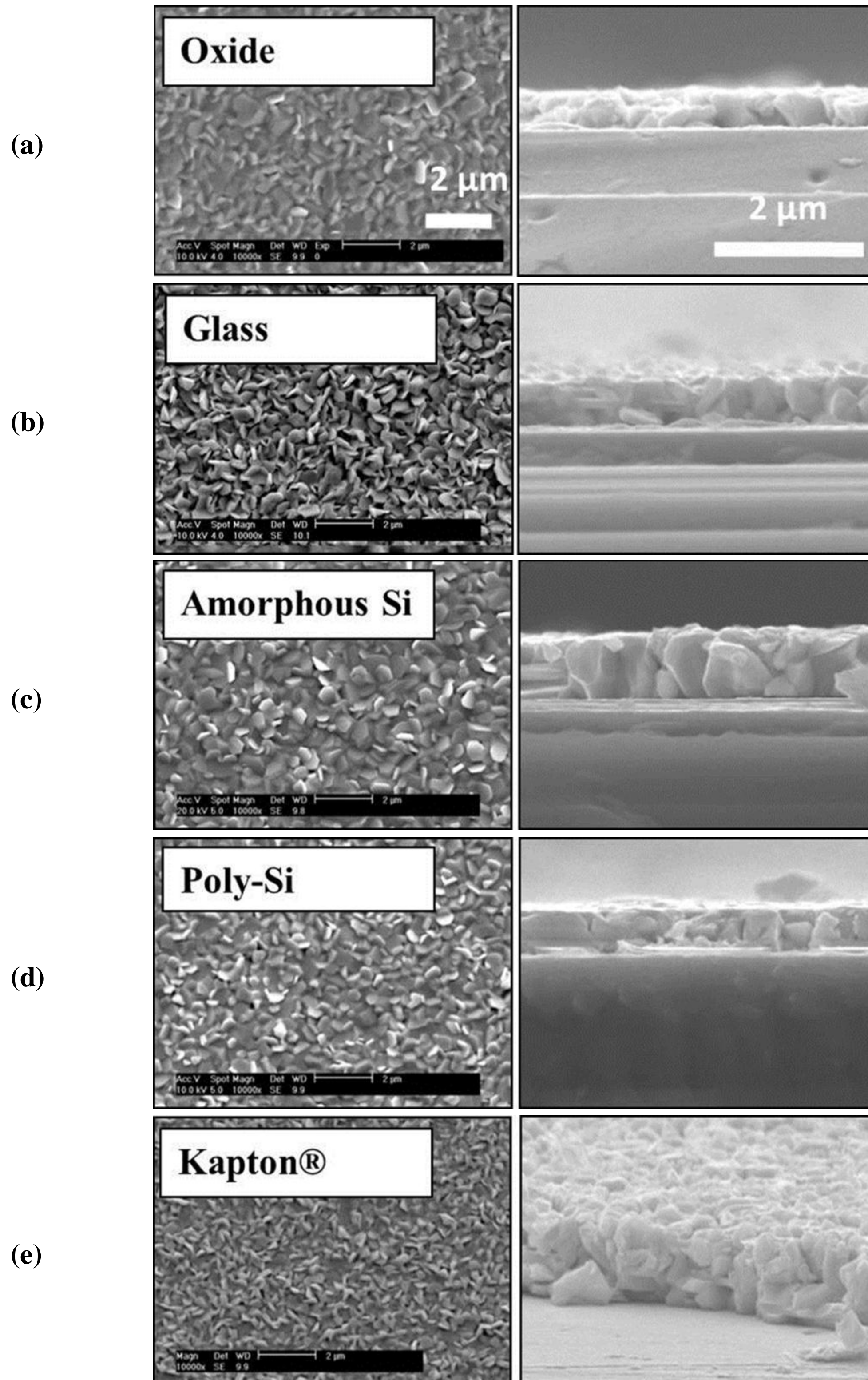


Figure 4.12 SEM micrographs of Bi_2Te_3 film surfaces and cross-section on different substrates at T_{sub}=270°C.

summarized in Figure 4.13.

Substrate	T_{sub}(°C)	FR(Bi:Te)	ρ (μΩ-m)	$α_s$ (μV/K)	$α_s^2/ρ$ (mW/K^{2}m)	At% (Bi:Te)
Polyimide (Kapton ®)	270	2:3	20	-250	3.12	38.5 : 61.5
Oxide	270	1:3	19.1	-210	2.31	39.1 : 60.9
Glass	270	1:3	14.5	-165	1.88	37.4 : 62.6
Poly-Si	270	1:3	10.5	-180	3.08	39.2 : 60.8
Amorphous Si	270	1:3	12.6	-178	2.51	40.1 : 59.9

Table 4.5 Bi_2Te_3 film properties at optimal deposition conditions on various substrates.

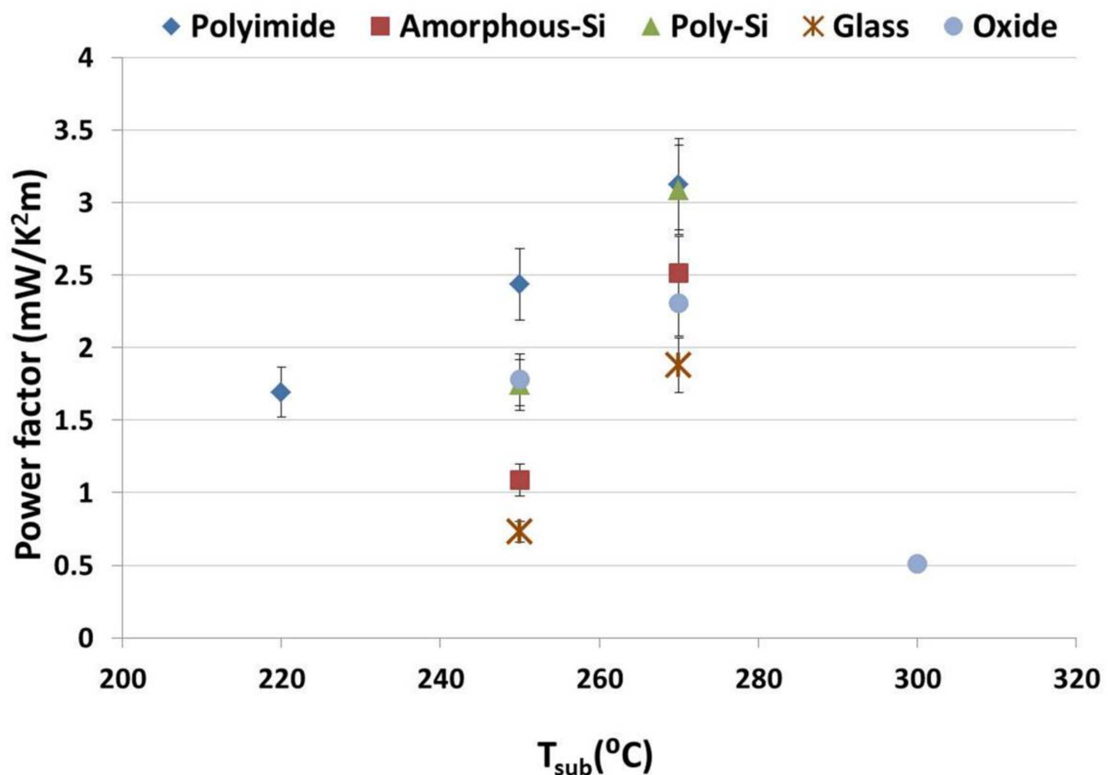


Figure 4.13 Effect of substrate material and deposition temperature on power factor for thermal co-evaporation of Bi_2Te_3 thin films.

The reasons behind variation of Bi_2Te_3 film characteristics are analyzed in the following

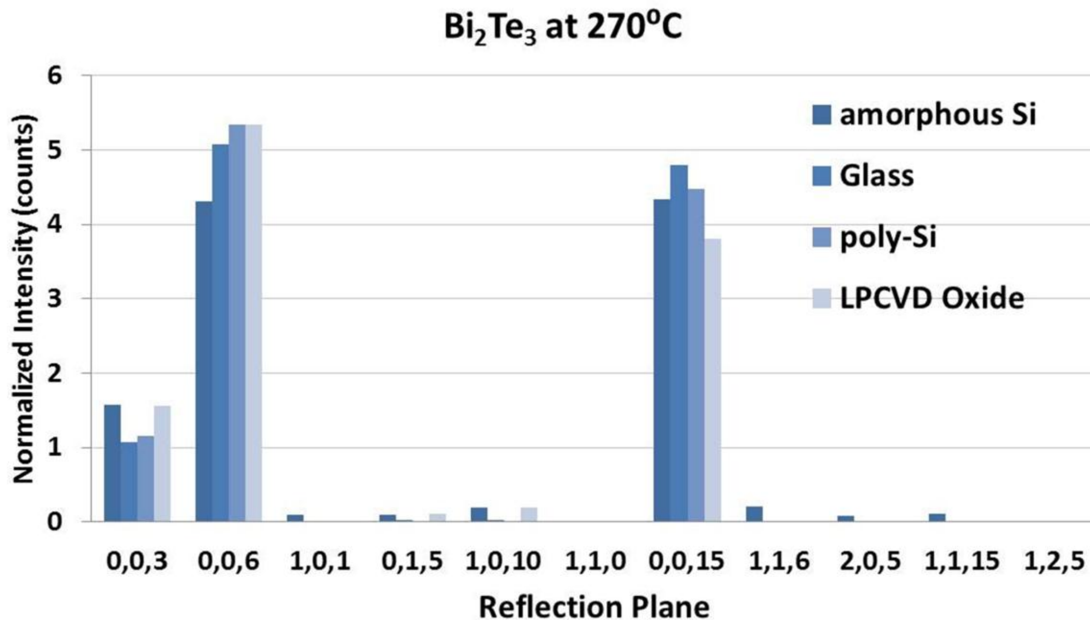


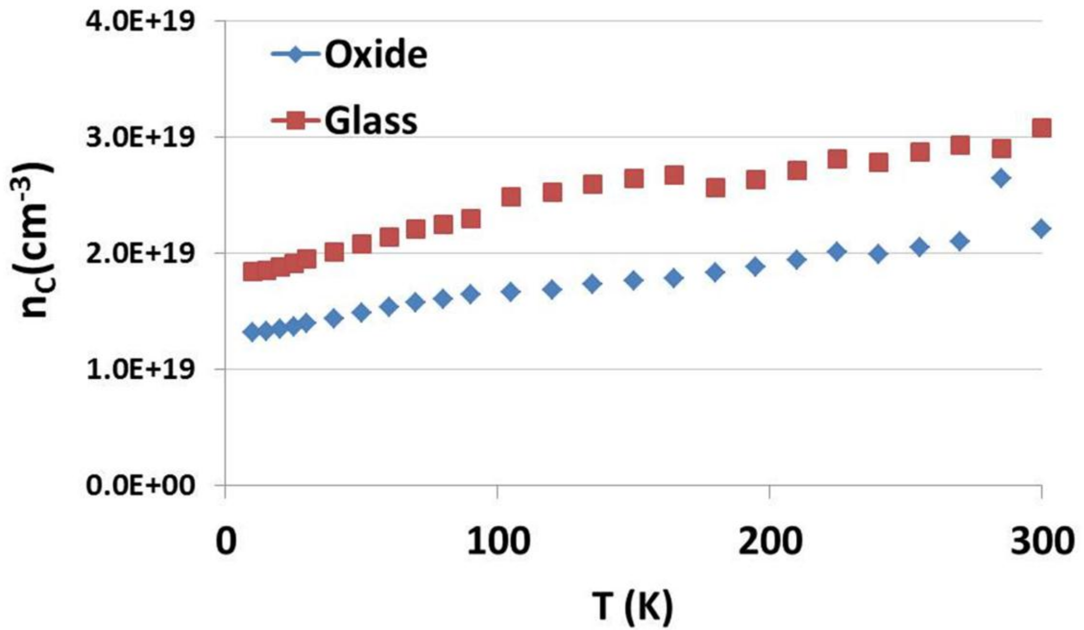
Figure 4.14 X-ray diffraction patterns for Bi_2Te_3 films deposited at optimal T_{sub} for various substrates.

subsections.

The crystal structure and orientation of Bi_2Te_3 film on various substrates are deduced from the XRD patterns and SEM micrographs. The diffraction patterns show that Bi_2Te_3 films deposited at optimal T_{sub} on all substrate have preferred *c*-orientation (Figure 4.14).

4.4.2.1. Substrate Crystal Structure: Oxide vs. Glass

Silicon dioxide and glass substrates are basically the same material with different crystal structures. The difference of TE film properties on these substrates can be explained based on the lower thermal conductance of thick glass wafer compared to the oxide layer. Therefore, the actual substrate temperature at the inset of TE film deposition could be higher on oxide compared to glass. Higher substrate temperature on oxide causes an increase of TE film grain size. Larger grain size results in lower carrier concentration, leading to higher Seebeck coefficient and resistivity of TE film on the oxide substrate.



Substrate	ρ (μΩ-m)	α_s (μV/K)	R_q (nm)
Glass	14.5	-165	87.1
Oxide	19.1	-210	40.1

Figure 4.15 Hall effect measurement of Bi_2Te_3 samples on oxide and glass substrates. TE properties in this table are repeated from the data in table 4.4.

The Hall effect measurement of Bi_2Te_3 samples confirms the above statements about carrier concentration (n_c) on oxide and glass substrates (Figure 4.15).

AFM analysis of Bi_2Te_3 film on both substrates, as shown in Figure 4.16, demonstrates higher surface roughness and out-of-plane grains on the glass substrate. This effect could be due several reasons: (1) the higher atomic percentage of Te, which in turn degrades TE properties of the Bi_2Te_3 film and (2) the faster TE film growth on glass substrate due to lower surface temperature and thus less chance for atoms to find their minimum energy state.

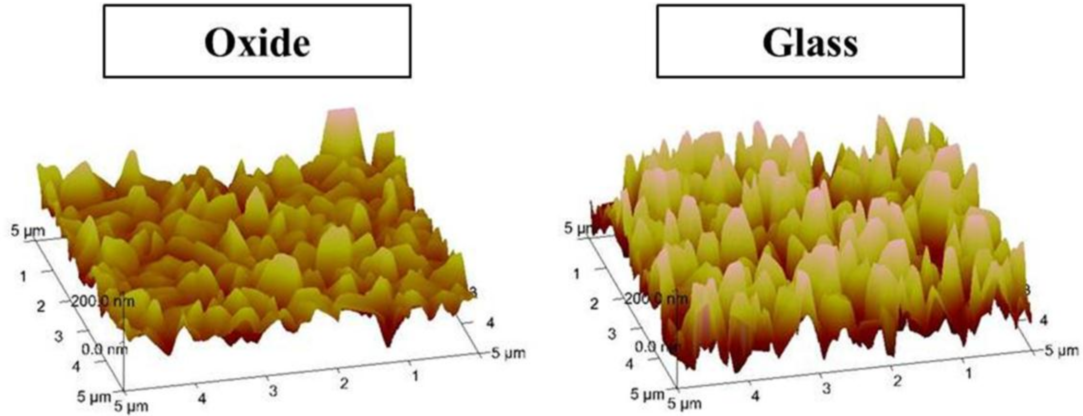
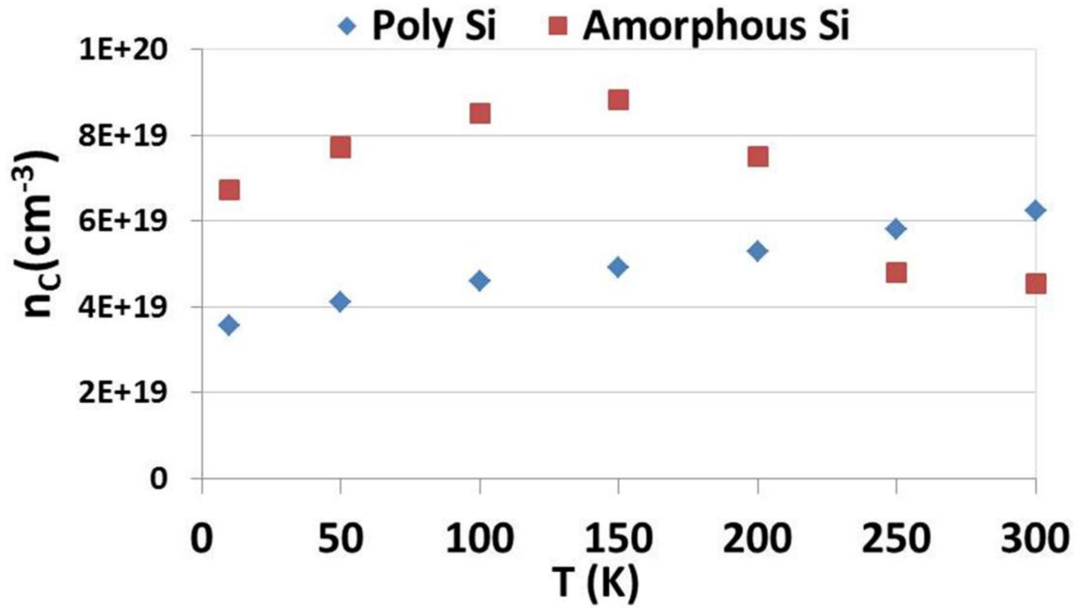


Figure 4.16 AFM analysis of Bi_2Te_3 film on oxide and glass substrates.

4.4.2.2. Substrate Crystal Structure: Amorphous Si vs. Poly-Si

Another study of the substrate crystallinity effect on TE characteristics is carried out by co-evaporation of Bi_2Te_3 films on amorphous Si and poly-Si substrates. These Bi_2Te_3 films have similar morphology and comparable TE properties. The TE film grain size is slightly smaller on the poly-Si layer, resulting in higher carrier concentration. Hall coefficient measurement shows similar carrier concentration on both substrates around room temperature. However, Hall effect measurements at temperatures below 250 K shows higher carrier concentration for Bi_2Te_3 film on amorphous Si compared to poly-Si (Figure 4.17). The decrease of Bi_2Te_3 carrier concentration on amorphous Si with measurement temperature is not usual and can be due to noisy measurement at temperatures > 200 K. It is necessary to repeat the Hall coefficient measurement for samples on amorphous Si to better understand the characteristics variation trend.

4.4.2.3. Substrate Material: Oxide vs. Polyimide (Kapton®)



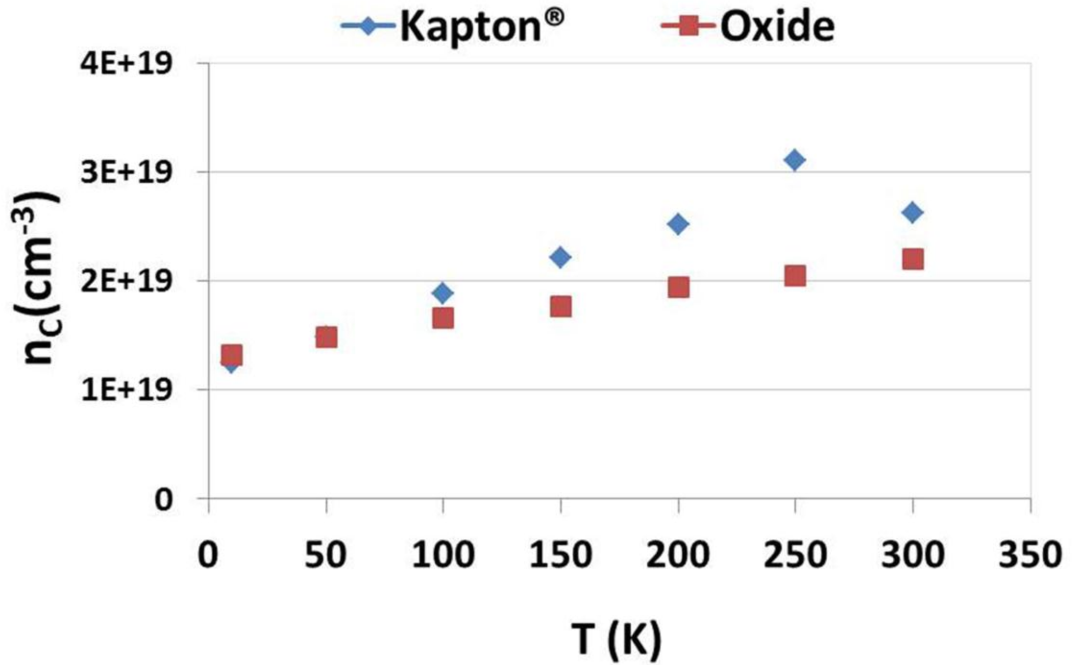
Substrate	ρ (μΩ-m)	α_s (μV/K)	R_q (nm)
Poly Si	10.5	-180	55
Amorphous Si	12.6	-178	44.1

Figure 4.17 Hall effect measurement of Bi_2Te_3 samples on poly-Si and amorphous Si substrates. TE properties in this table are repeated from the data in Table 4.4.

The study on the effect of substrate materials is further investigated by comparing Bi_2Te_3 films on two completely different substrates: oxide and Kapton®.

The morphology of Bi_2Te_3 samples on these two substrates is different; however, they exhibit similar TE electrical resistivity. The difference in grain size could be due to lower thermal conductance of the 25-µm Kapton® sheet compared to the thin oxide layer and therefore a higher temperature at the onset of TE film deposition for SiO_2/Si substrates.

SEM micrographs in Figure 4.12 demonstrate that the grain size increases and a more crystalline structure is found in the Bi_2Te_3 thin film on the oxide substrate. Both samples have carrier concentration of ~ 2.5×10^{19} cm^{-3} around room temperature (Figure 4.18).



Substrate	ρ (μΩ-m)	α_s (μV/K)	R_q (nm)
Polyimide (Kapton ®)	20	-250	-
Oxide	19.1	-210	40.1

Figure 4.18 Hall effect measurement of Bi_2Te_3 samples on Kapton® and oxide substrates. TE properties in this table are repeated from the data in table 4.4.

Therefore, the higher Seebeck coefficient of Bi_2Te_3 film on Kapton® could not be justified by the change of grain size and carrier concentration.

4.4.3. Discussion

Thin film morphology and orientation are affected by the substrate temperature. In general, the grain size of co-evaporated Bi_2Te_3 films increases with substrate temperature. This phenomenon is due to higher surface mobility and clustering of atoms on the surface when more thermal energy is available during film growth.

The Seebeck coefficient also increases with growing grain size due to its inverse dependence on the carrier concentration. By increasing the grain size, the carrier concentration decreases, resulting in higher Seebeck coefficient. Furthermore, defects at grain boundaries found at low deposition temperatures increase carrier concentration while mobility is reduced due to carrier scattering. As the grain size grows, carrier concentration decreases, resulting in higher electrical resistivity, but the enhancement in mobility will compensate for the increase in resistance. Therefore, depending on whether the reduction in carrier concentration or the increase in mobility is dominant, electrical resistivity could increase or decrease with deposition temperature.

The SEM micrographs and the normalized XRD patterns reported in this section indicate an increase in crystalline quality of the Bi_2Te_3 films with the increase of T_{sub}. The maximum obtained power factors are 3.08 and 3.12 mW/K^2 for the Bi_2Te_3 films deposited at T_{sub} = 270°C on poly-Si and Kapton® substrates, respectively. This is higher than the power factor values previously reported at the University of Michigan [51], but not as high as the Bi_2Te_3 thin film performance reported in [15,98].

Based on the limited number of characterizations performed, significant effect of substrate material on the TE properties of Bi_2Te_3 film is observed. Several factors such as the condensation flux, lattice mismatch, interfacial layers and the sticking coefficients of evaporated elements to the substrate play important roles in determining the morphology and properties TE films on different substrates. Due to limited data about the formation of Bi_2Te_3 film on a substrate and the interfacial layers, no conclusion can be drawn on the physical and chemical reasons behind the effect of substrate material. However, this study together with the reproducibility of TE properties by thermal co-evaporation

enables us to determine the Bi_2Te_3 thin film optimal deposition conditions on any given substrate for a specific microsystem.

4.5. Optimal Deposition Parameters for Sb_2Te_3 Films

Antimony telluride films with the thickness of ~ 1 μm are deposited on different substrates, at various substrate temperatures. Elemental FR has been slightly varied to obtain film with stoichiometric composition.

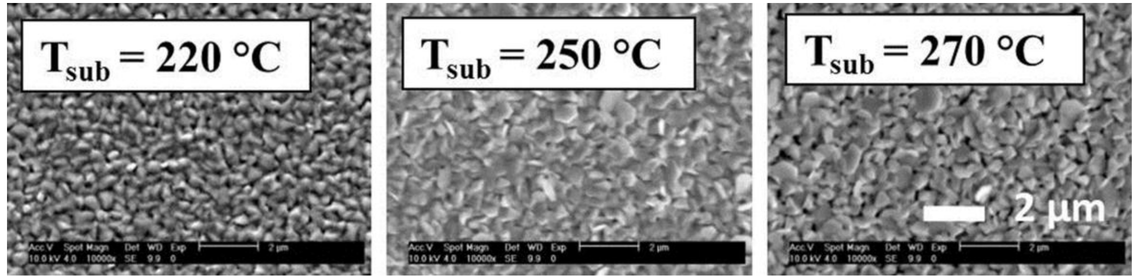
4.5.1. Effect of Substrate Temperature and Film Composition

Antimony telluride films with the thickness of ~ 1 μm ± 20% are co-evaporated. The effects of substrate temperature and film composition are investigated to optimize film properties for each of the studied substrates. The deposition temperature for Sb_2Te_3 thin films varies between 180, 200, 220, 250 and 270°C. Furthermore, the elemental fraction ratio, $FR_{(Sb:Te)}$, is set to 1:3, 2:3 and 2.5:3 to find the optimal composition [33].

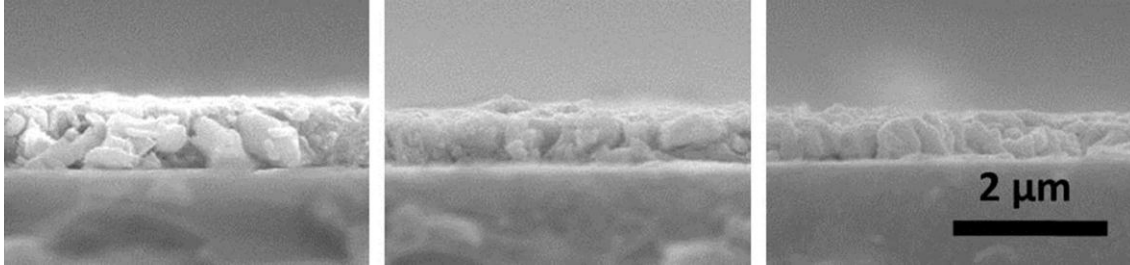
Figure 4.19 shows the surface and cross-section SEM micrographs of select Sb_2Te_3 samples deposited on SiO_2 /Si substrates with similar FRs at T_{sub}= 220, 250 and 270 °C.

The Seebeck coefficients of Sb_2Te_3 films are positive indicating that they are *p*-type materials. This coefficient increases to its maximum value with T_{sub} at 250 °C.

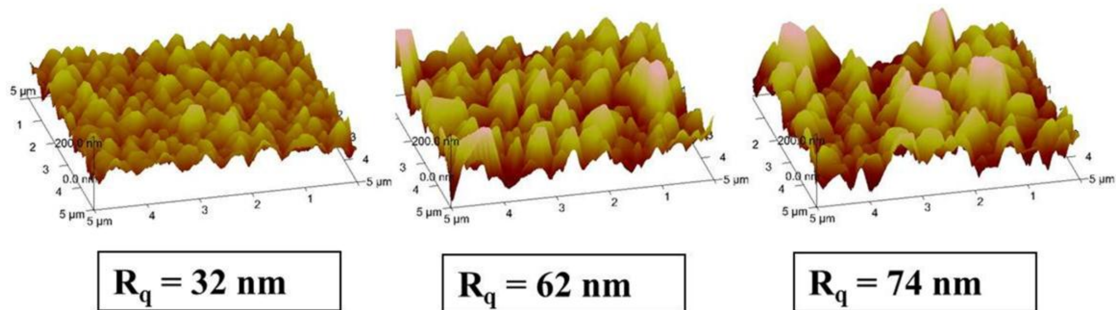
As shown in Table 4.6, at T_{sub} = 220 °C, film composition is proportional with the elemental evaporation $FR_{(Sb:Te)}$= 1:3 and the film thickness is higher than the expected value, indicating excess tellurium material accumulation on the substrate; Te re-evaporation does not occur at low deposition temperatures. The large atomic percentage of Te will result in reduction of Seebeck coefficient. Since carrier concentration and grain size decrease, the resistivity of the Sb_2Te_3 film is increased.



(a)



(b)



(c)

Figure 4.19 (a) Surface SEM micrographs of Sb_2Te_3 films deposited on SiO_2/Si substrate at various temperatures. (b) Cross-sectional images of these films. (c) AFM images of Sb_2Te_3 thin film surface roughness.

The XRD pattern of the Sb_2Te_3 sample on oxide at T_{sub} = 220°C in Figure 4.20 shows high peak intensity for the (1,0,0), (1,0,1), (1,0,2) and (1,1,0) planes, which confirms the presence of metallic tellurium in addition to Sb_2Te_3 alloy.

The variation of Sb_2Te_3 Seebeck coefficient with temperature is less than that of Bi_2Te_3 films. This lower sensitivity to deposition temperature can be due to the higher background carrier density of Sb_2Te_3 compound. Sb_2Te_3 has similar crystal structure to Bi_2Te_3, but the weaker bond between Sb and Te layers causes Sb atoms to usually occupy

Te lattice positions, leading to antisite defects [60].

The maximum power factor for Sb_2Te_3 thin film on SiO_2/Si substrate is 1.05 mW/K^2 m

T_{sub}	FR(Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^2m)	At% (Sb:Te)
220	1:3	39.4	172.5	0.755	24.1 : 75.9
250	1:3	32.2	184.2	1.053	38.4 : 61.6
270	1:3	28.6	170	1.010	41.3 : 58.7

Table 4.6 Measured optimum TE properties of co-evaporated Sb_2Te_3 films deposited on oxide substrates at T_{sub} = 220, 250 and 270 °C.

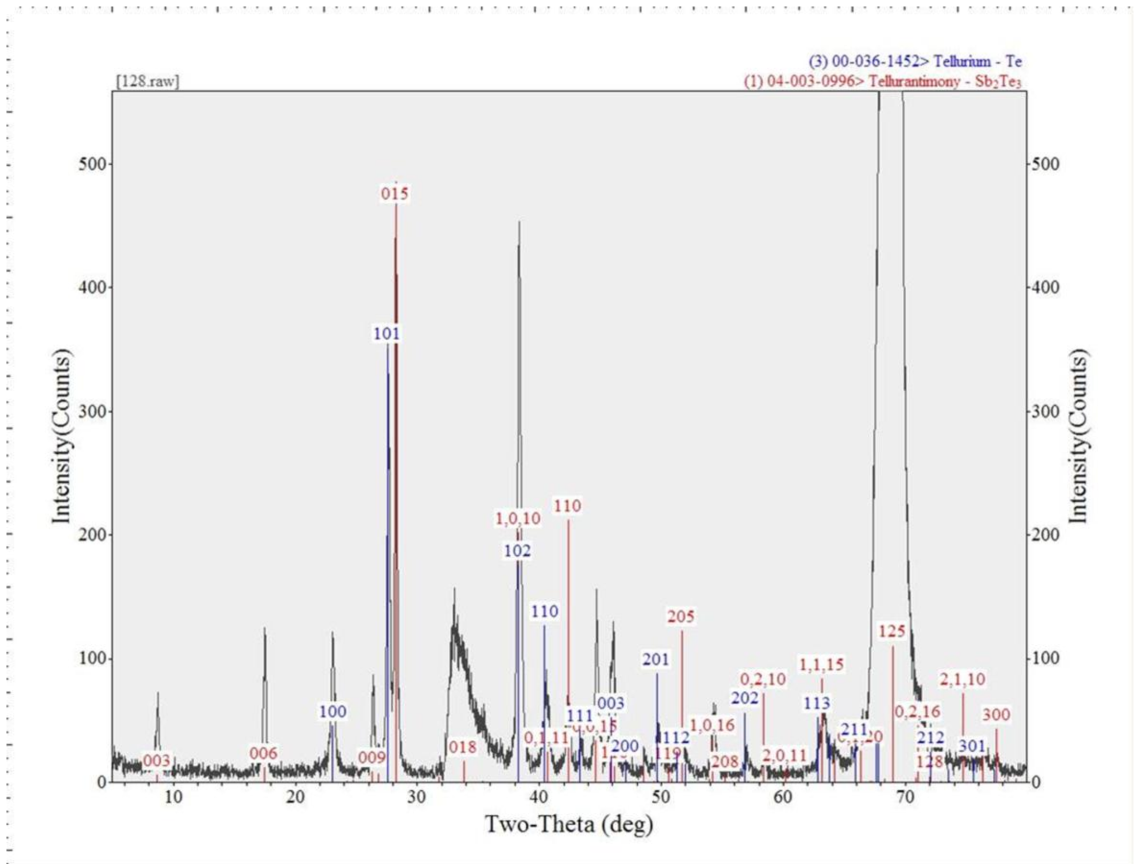


Figure 4.20 XRD pattern of Sb_2Te_3 thin film deposited on oxide substrate at T_{sub} = 220°C shows the presence of metallic tellurium in a sample with high (~76%) Te atomic percentage.

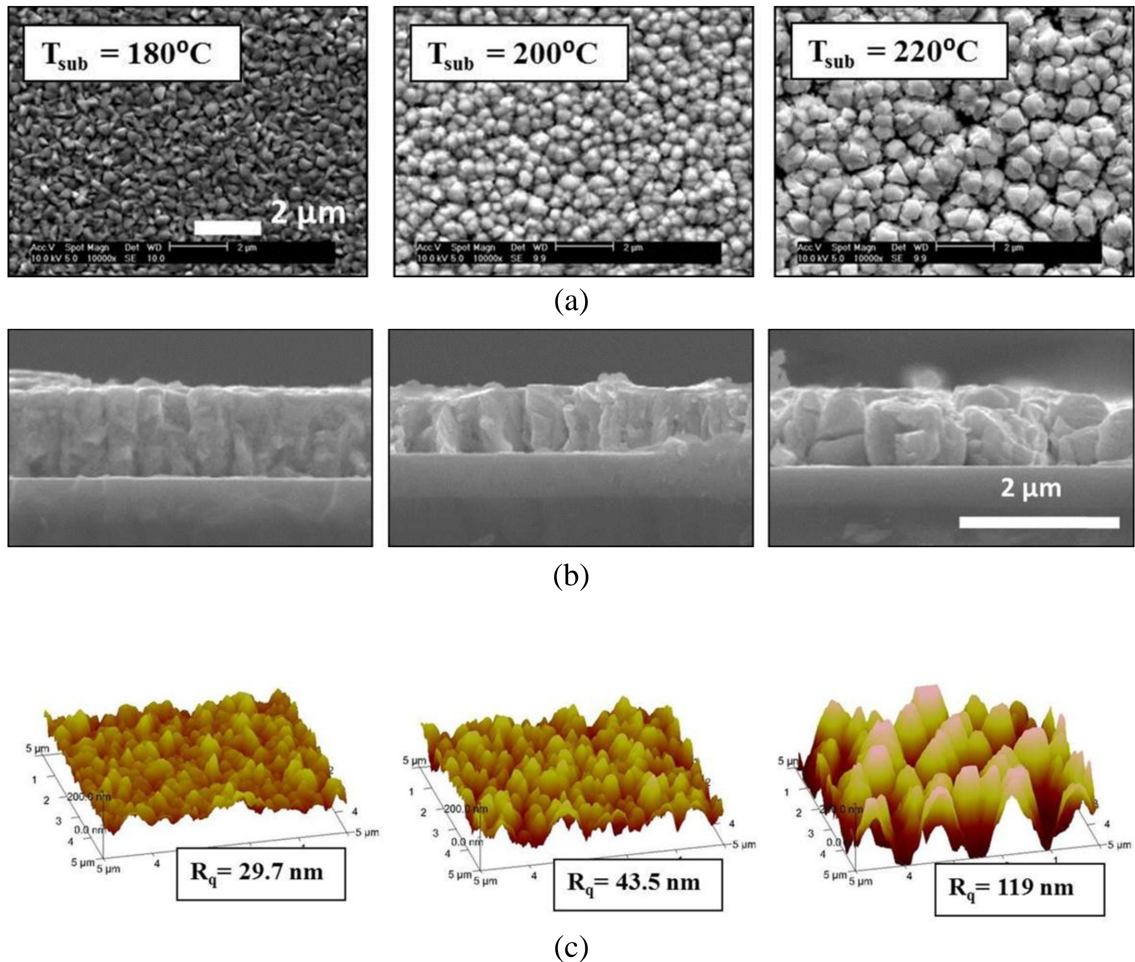


Figure 4.21 (a) Surface SEM micrographs of Sb_2Te_3 films deposited on amorphous Si substrate at various temperatures. (b) Cross-sectional images of these films. (c) AFM images of Sb_2Te_3 thin film surface roughness.

deposited at T_{sub} = 250°C with $FR_{(Bi:Te)}$ = 1:3 and has Te atomic percentage close to the stoichiometric value compared to the samples deposited at other substrate temperatures (Table 4.6). Increasing the substrate temperature further causes re-evaporation of Te from the substrate, and thus creates point defects in the crystal structure and discontinuities in the film. The surface SEM image of Sb_2Te_3 thin film deposited at T_{sub} = 270°C shows many voids as predicted.

The AFM analysis of Sb_2Te_3 samples as shown in Figure 4.19(c) demonstrates that the surface roughness increases with substrate temperature during deposition. In general,

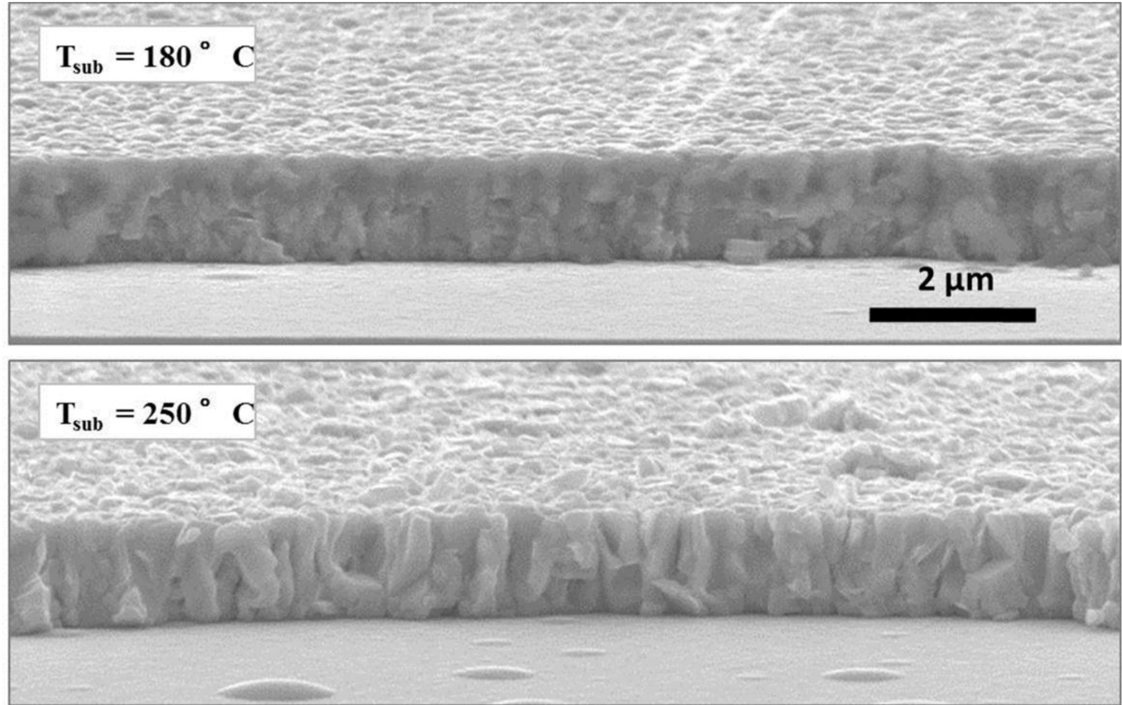
Sb_2Te_3 thin films exhibit poor adhesion and stress related problems compared to Bi_2Te_3 thin films, and this will be discussed further in section 4.5.3.

The surface and cross-section SEM micrographs of the co-evaporated Sb_2Te_3 films on amorphous Si substrate and the surface roughness analysis are shown in Figure 4.21. At higher deposition temperatures (T_{sub} > 200 °C), cross-section SEM micrographs clearly illustrate cracks and film delamination from the substrate. Furthermore, a large number of voids are observed in the top surface SEM images of Sb_2Te_3 deposited at 200 and 220°C. The Sb_2Te_3 thin films co-evaporated at T_{sub}= 220°C on amorphous Si and glass start peeling off from the substrate after unloading the samples from the deposition chamber. The delamination of the Sb_2Te_3 films does not occur for samples deposited at T_{sub}= 200°C, however the TE film is easily removed by applying a piece of scotch tape, demonstrating poor adhesion. AFM analysis of these samples confirms the significant growth of grain size and surface roughness at higher T_{sub}.

Properties of Sb_2Te_3 films deposited on amorphous Si substrate are summarized in Table 4.7. The electrical resistivity of Sb_2Te_3 film at T_{sub} = 220 °C is quite high due to poor adhesion and film discontinuity due to the aforementioned voids at this temperature. Improved adhesion of Sb_2Te_3 thin films on oxide, poly-Si and polyimide substrates

T_{sub} (°C)	FR (Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At%(Sb:Te)	R_q (nm)
180	2:3	29.5	135	0.618	41.6 : 58.4	29.7
200	2:3	42.7	162	0.615	42.2 : 57.8	43.5
220	2:3	144	175	0.213	37.6 : 62.4	119

Table 4.7 Properties of Sb_2Te_3 films deposited on amorphous Si substrate



T_{sub} (° C)	FR(Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	$\alpha_s^2/\rho k$ (mW/K^{2}m)	At% (Sb:Te)
180	2:3	51.8	162	0.51	35.5 : 64.5
250	2:3	32.2	195	1.18	40.1 : 59.9

Figure 4.22 Cross-section SEM micrographs and properties of co-evaporated Sb_2Te_3 films on poly-Si substrate at various temperatures.

compared to glass and amorphous Si enables their co-evaporation at higher T_{sub}.

As shown earlier in this section, despite constant evaporation FR for Sb_2Te_3 samples on oxide, the substrate temperature during deposition has a considerable effect on the film composition. At higher temperatures, the film composition is proportional to the elemental evaporation $FR_{(Sb:Te)}$= 1:3, with a higher thickness than the expected value.

As discussed in section 4.5.1, these observations indicate excess tellurium material accumulation on the substrate and its re-evaporation does not occur at low deposition temperature (T_{sub} = 220 °C). Similar behavior is observed and studied for Sb_2Te_3 deposited at T_{sub} = 180 and 250 °C on poly-Si as shown in Figure 4.22. Cross-sectional

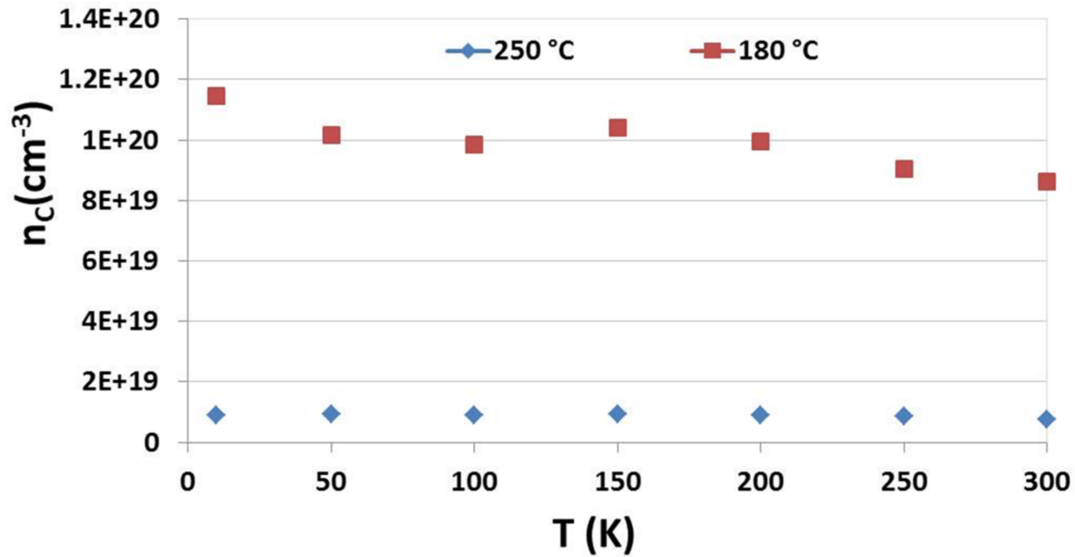


Figure 4.23 Hall effect measurement shows carrier concentration of Sb_2Te_3 samples on poly-Si as a function of measurement temperature for substrate temperatures of 180°C and 250 °C.

SEM micrographs of these samples in this figure demonstrate the transition of Sb_2Te_3 thin film morphology from an amorphous structure with blurry grain boundaries at 180°C to a polycrystalline structure with larger grains at 250 °C.

Hall coefficient measurement of Sb_2Te_3 samples on poly-Si indicates an increase of carrier concentration for large atomic percentage of Te at lower deposition temperatures and consequently reduced Seebeck coefficient and higher resistivity (Figure 4.23).

The composition of the Sb_2Te_3 film on polyimide is very sensitive to the evaporation fraction ratio, $FR_{(Sb:Te)}$. The film co-evaporated with $FR_{(Sb:Te)}$=2:3 has low Te atomic percentage (52.98%), small grain size and, as a result, low Seebeck coefficient. At the same deposition temperature (T_{sub} = 250 °C) and $FR_{(Sb:Te)}$=1:3, the film is rich in Te (atomic percentage = 74.25%), and thus has larger grain size, high Seebeck coefficient and high resistivity. Adjusting the elemental evaporation FR to achieve stoichiometric Te atomic percentage (~ 60%) is challenging for these samples.

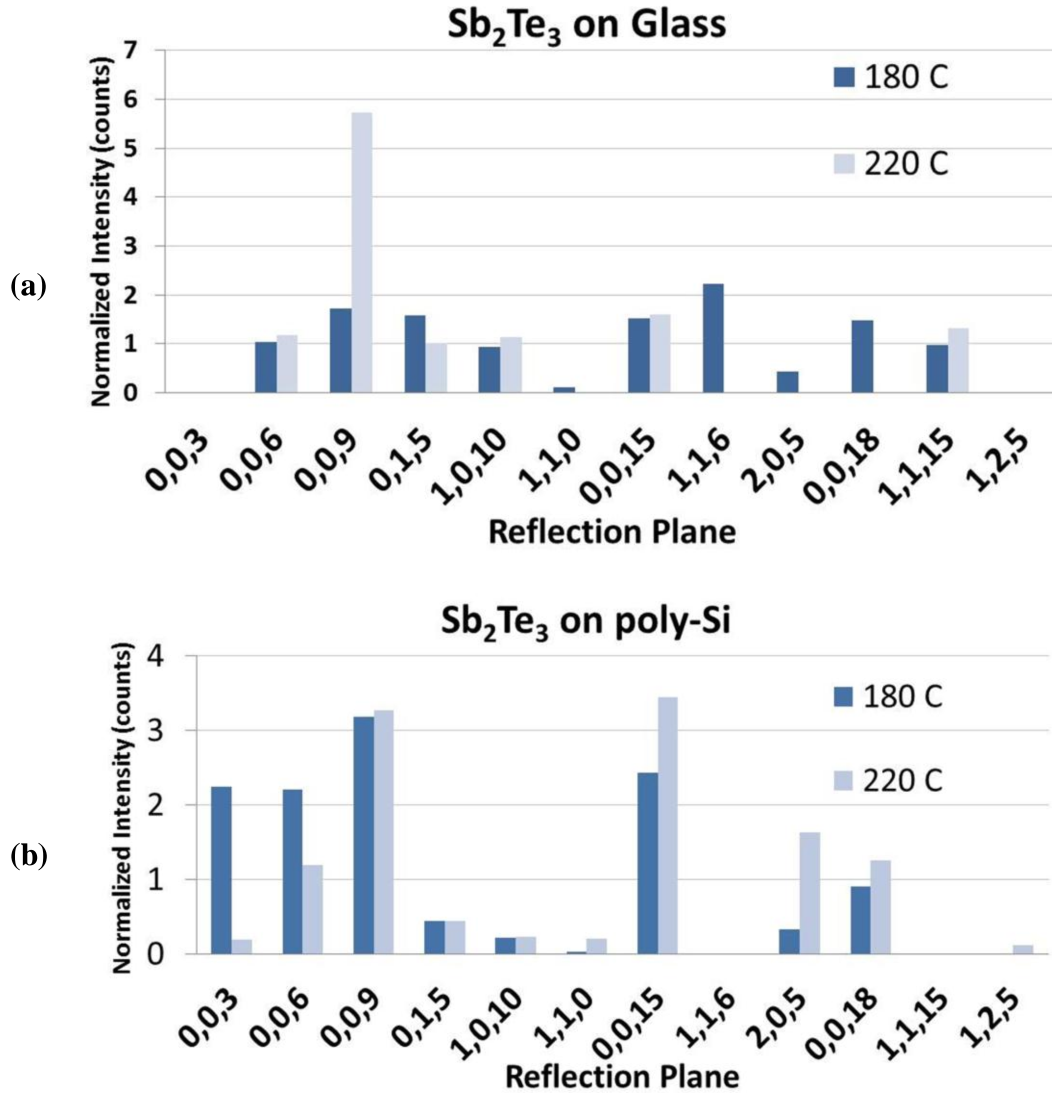


Figure 4.24 Normalized diffraction pattern of the Sb_2Te_3 films on (a) glass, and (b) poly-Si substrates.

Normalized diffraction patterns of Sb_2Te_3 films on glass and poly-Si substrates are shown in Figure 4.24(a) and (b). Position of the peaks agrees with the Powder Diffraction File reference for Sb_2Te_3, and indicates less preferential *c*-orientation compared to Bi_2Te_3 samples. It can be seen that the preferred *c*-axis orientation increases at higher T_{sub}. The normalized diffraction pattern of Sb_2Te_3 film on oxide in Figure 4.25 shows that as T_{sub} increases, peaks become sharper, indicating higher crystalline quality.

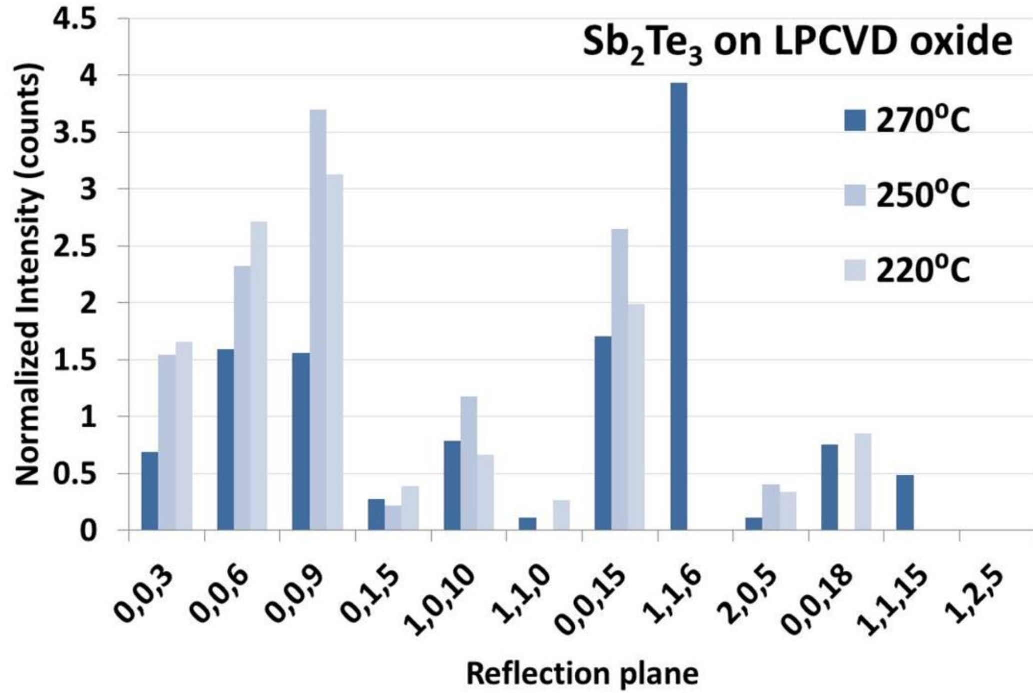


Figure 4.25 Normalized diffraction pattern of Sb_2Te_3 e film on oxide for different temperatures.

4.5.2. Effect of Substrate Material and Crystal Structure

Sb_2Te_3 thin films are deposited on LPCVD oxide, glass, amorphous Si, poly-Si and polyimide (Kapton®) and are optimized over a range of substrate temperatures and elemental fraction ratio. The effect of substrate material and crystallinity on the characteristics of Sb_2Te_3 thin films is analyzed at their optimum point.

Since Sb_2Te_3 films on amorphous Si and glass have high stress and adhesion problems, their co-evaporation has been performed at lower substrate temperature, resulting in relatively poor TE quality and non-stoichiometric composition. It is evident that there are problems with Sb_2Te_3 sticking to amorphous Si and glass substrates at higher temperatures. Co-evaporated Sb_2Te_3 films on polyimide (Kapton®) have better adhesion, but high stress levels for samples deposited at $T_{sub} > 200$ °C, causing the Kapton® sheets

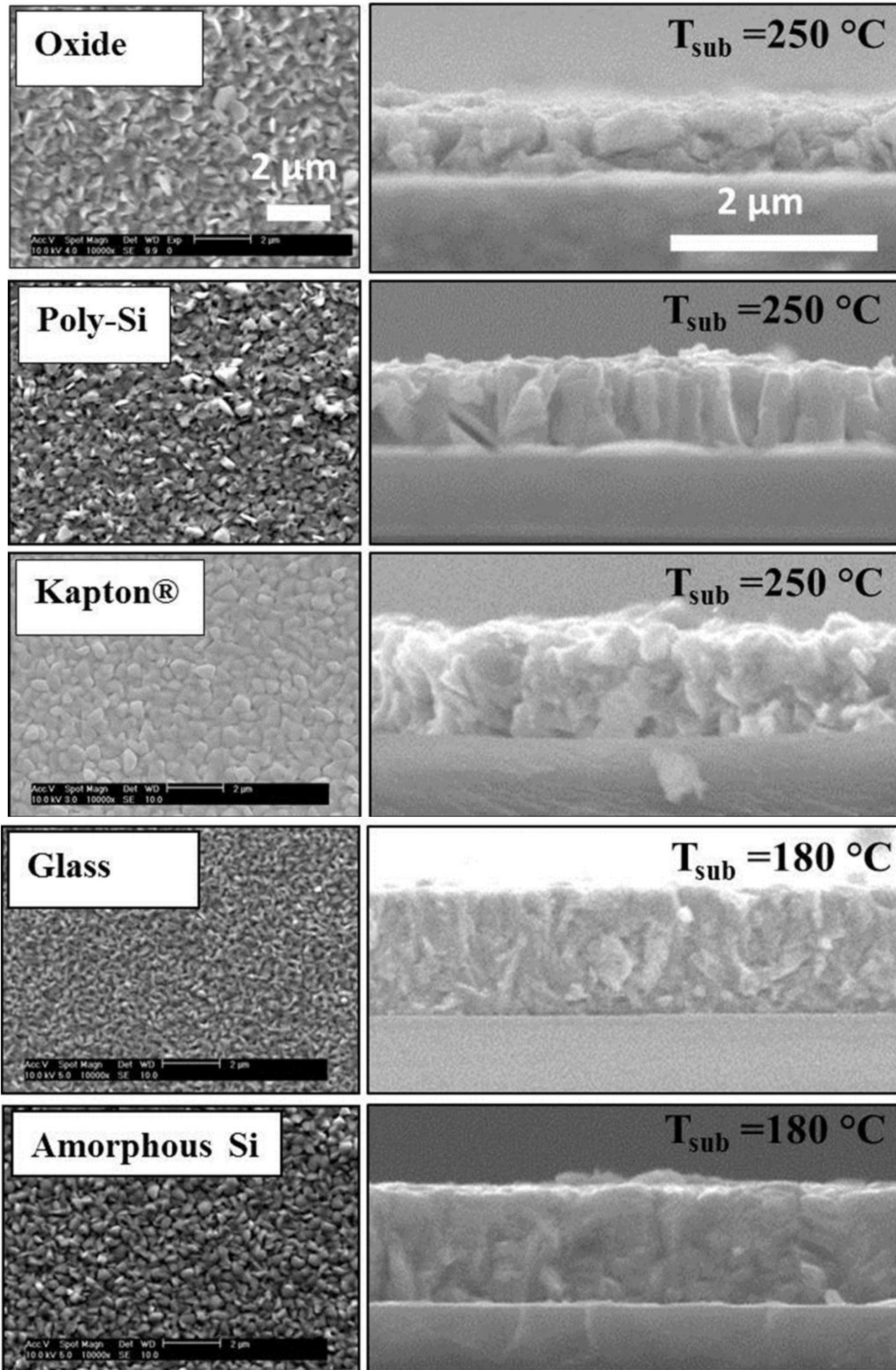


Figure 4.26 SEM micrographs of the Sb_2Te_3 film top surface and cross-section on various substrates.

Substrate	T_{sub} (°C)	FR(Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Sb:Te)
Polyimide (Kapton®)	250	2:3	10.8	85	0.67	47.1 : 52.9
Oxide	250	2:3	21	157	1.17	40.4 : 59.6
Poly-Si	250	2:3	32.2	195	1.12	40.1 : 59.9
Glass	180	2:3	48	177	0.65	32.7 : 67.3
Amorphous Si	180	2:3	47.2	165	0.58	38.6 : 61.4

Table 4.8 Properties of optimum Sb_2Te_3 films deposited on various substrates.

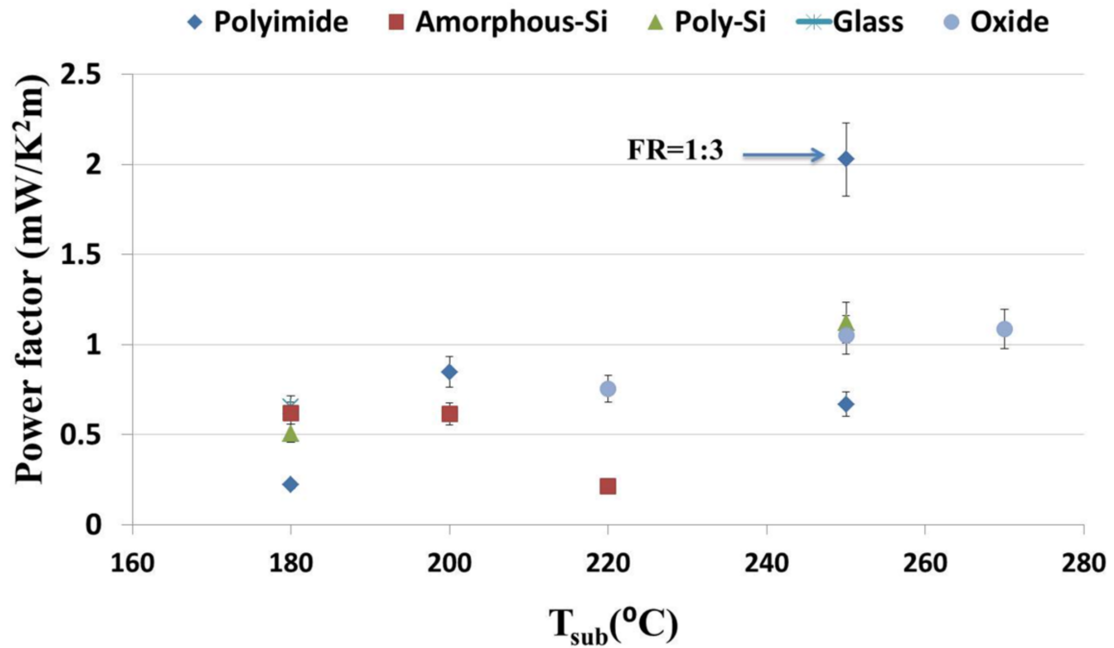


Figure 4.27 Thermoelectric power factor of Sb_2Te_3 film as a function of substrate temperature and material. ($FR_{(Sb:Te)}$=2:3 for all data points except one.)

to roll immediately after releasing from the carrier Si wafer.

SEM micrographs of the Sb_2Te_3 film top surface and cross-section on different substrates are shown in Figure 4.26, indicating the variation of grain size and crystal structures.

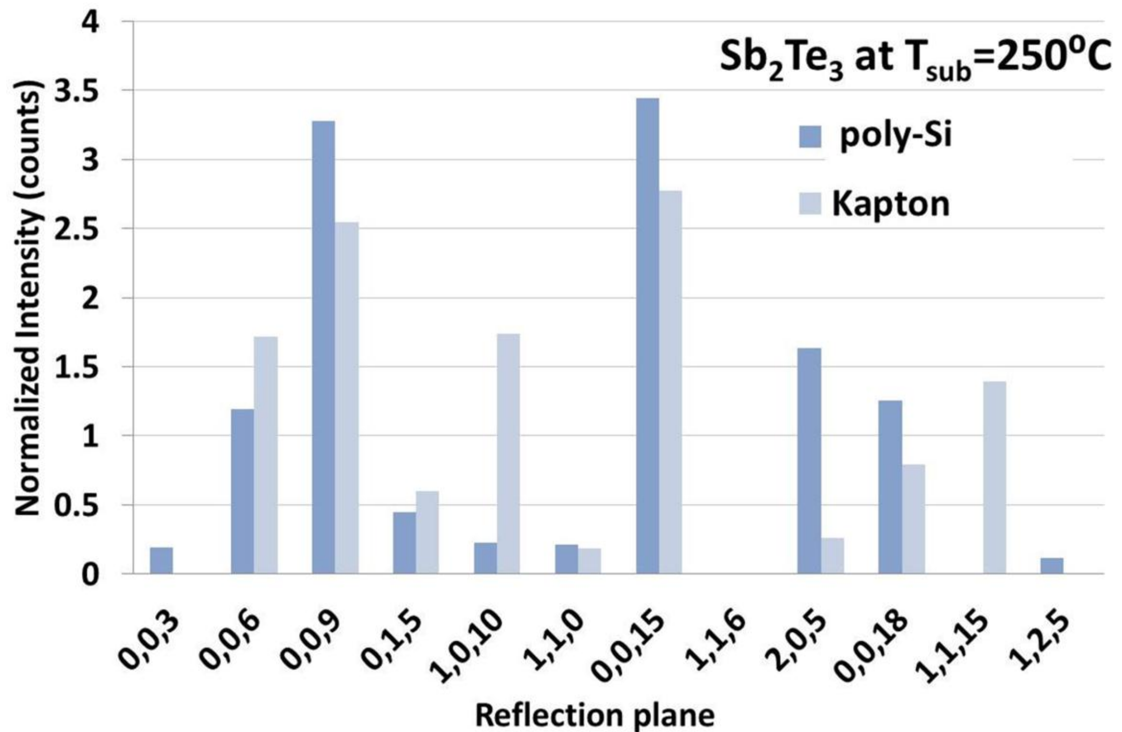


Figure 4.28 X-ray diffraction pattern of Sb_2Te_3 films on poly-Si and Kapton® at 250°C.

Table 4.8 summarizes the optimal properties achieved for Sb_2Te_3 films on different substrates. Most of the Sb_2Te_3 films with optimum power factor have Te atomic percentage of around 60%.

The thermoelectric power factor of Sb_2Te_3 films as a function of substrate temperature and substrate material are illustrated in Figure 4.27. The optimum deposition temperature for these films is ~ 250°C. However, TE properties could not be measured for Sb_2Te_3 samples that have poor adhesion at this temperature, including films deposited on amorphous Si and glass substrates. Therefore, TE properties are measured at lower deposition temperatures (T_{sub} < 250 °C) for Sb_2Te_3 thin films on these substrates.

The diffraction patterns of Sb_2Te_3 films on select substrates at T_{sub} = 250 and 180 °C are shown in Figure 4.28 and Figure 4.29, respectively. At optimal deposition condition (T_{sub} = 250 °C and FR=2:3), the *c*-axis is the preferred orientation for the Sb_2Te_3 crystal

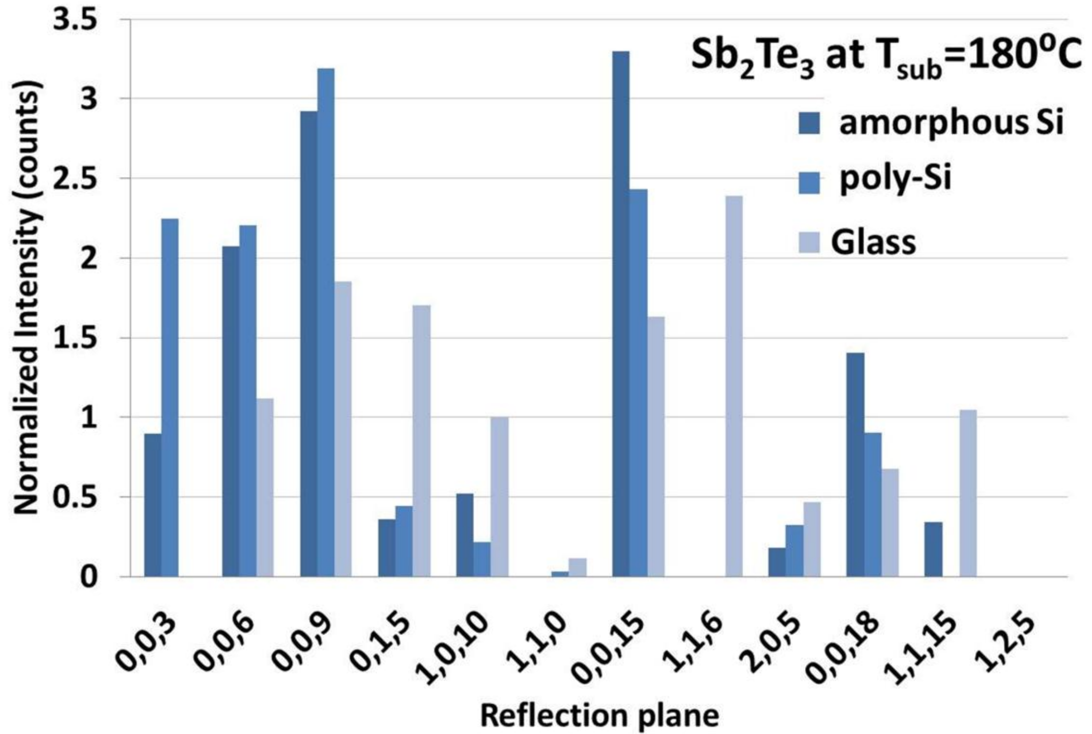


Figure 4.29 X-ray diffraction pattern of Sb_2Te_3 films on amorphous Si, poly-Si, and glass at 180°C.

structures grown on poly-Si, while crystals grown on polyimide are more randomly oriented.

The XRD patterns also show that at Te atomic percentage of ~ 60% for Sb_2Te_3 on poly-Si substrate, relative intensity of the peaks corresponding to (*00l*) orientation is higher compared to the peaks on Kapton®. For Sb_2Te_3 film on Kapton® with Te atomic percentage of ~53%, the Sb_2Te_3 film obtains a more polycrystalline structure with higher relative peak on Kapton® compared to poly-Si, corresponding to (0,1,5) and (1,0, 10) planes. This effect can also be seen in the cross-section SEM image of Sb_2Te_3 film on Kapton® in Figure 4.26

Similar behavior is observed for the Sb_2Te_3 film deposited on glass at T_{sub} = 180 °C with atomic percentage of Te > 60%. The Sb_2Te_3 film on glass has less preferred *c*-orientation

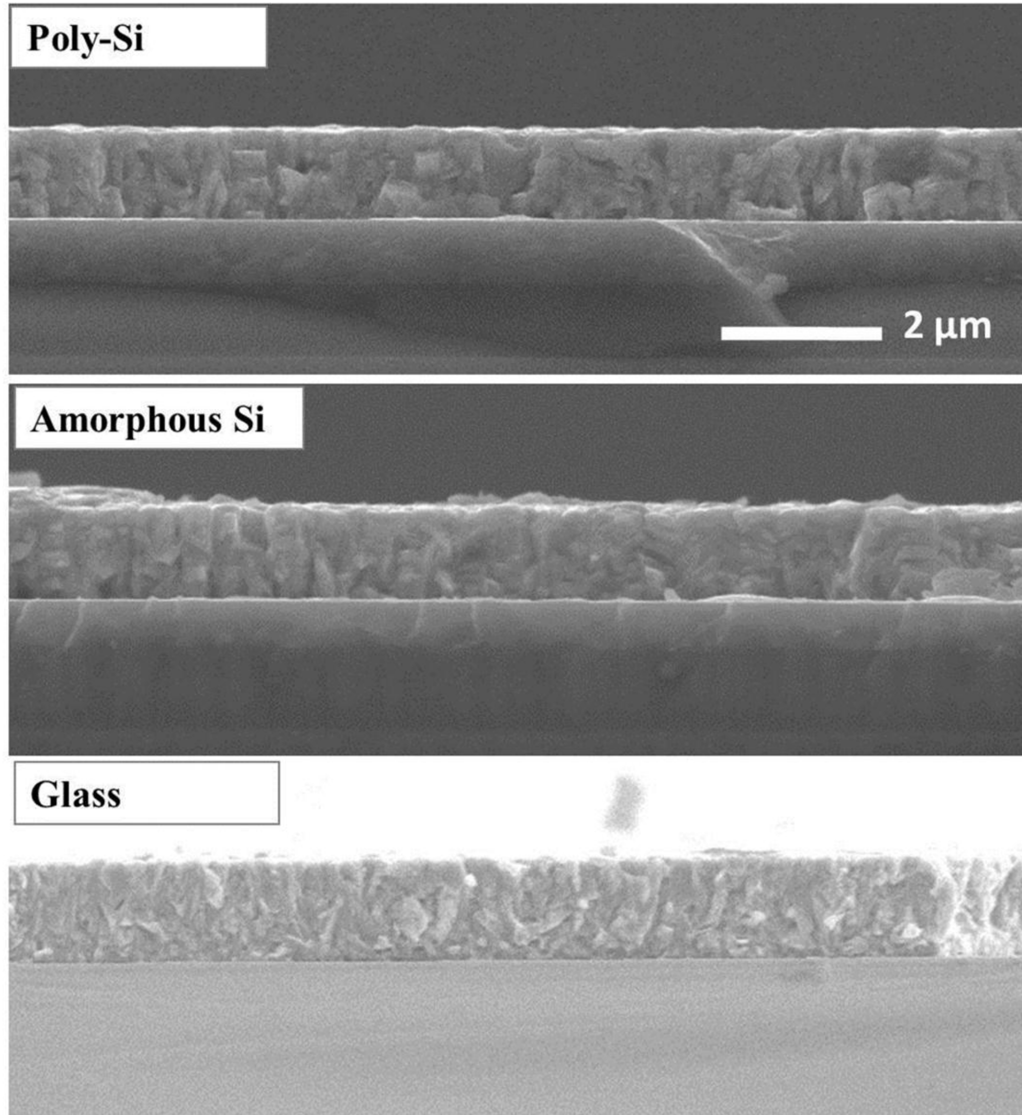
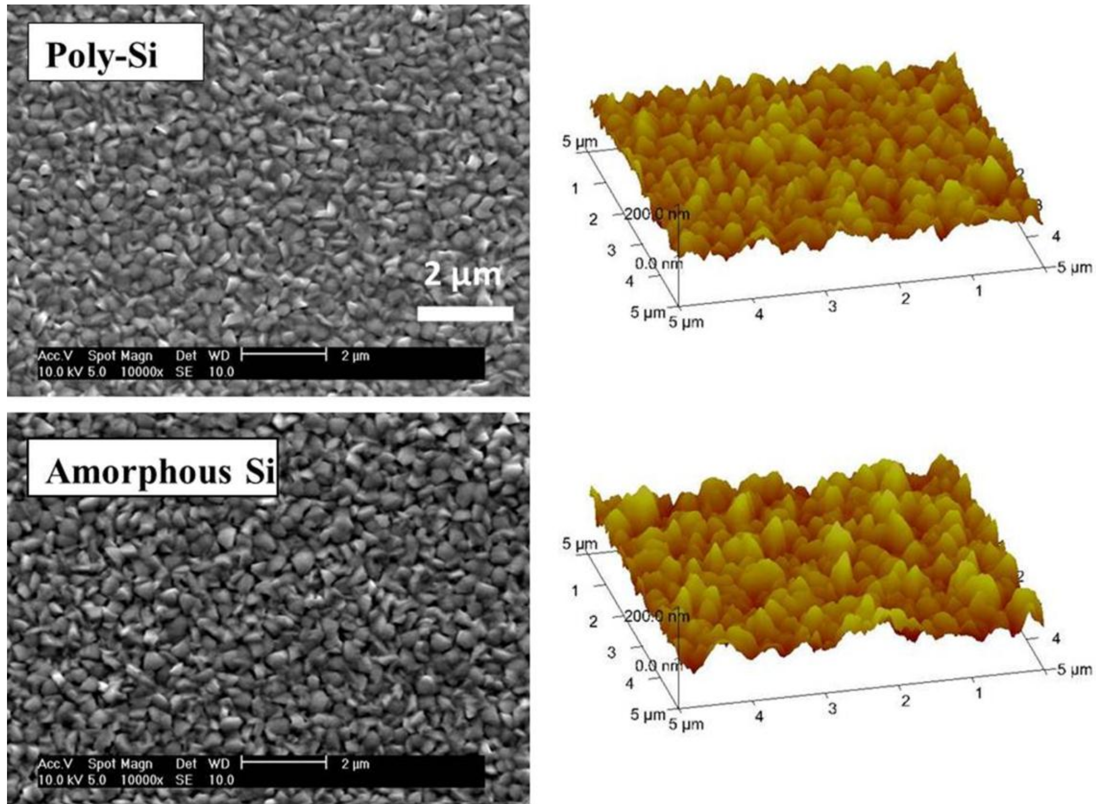


Figure 4.30 Cross-section SEM of Sb_2Te_3 films on poly-Si, amorphous Si and glass substrates at T_{sub} = 180 °C.

and higher relative peaks for the (0,1,5), (1,0, 10) and (2,0,5) planes compared to the films on amorphous Si and poly-Si (Figure 4.29 and Figure 4.30).

4.5.2.1. Substrate Crystal Structure: Amorphous Si vs. Poly-Si

As mentioned before, a study of the substrate crystal structure effect of Sb_2Te_3 film optimal characteristics could not be carried out due to delamination of TE film from amorphous Si substrates at high deposition temperatures. Instead, the comparison has



Substrate	ρ (µΩ-m)	α_s (µV/K)	R_q (nm)
Poly Si	51.8	162	24
Amorphous Si	47.2	165	29.7

Figure 4.31 SEM micrograph, AFM and TE properties of the Sb_2Te_3 film deposited on poly-Si and amorphous Si at T_{sub} = 180°C. TE film properties on amorphous Si in this table are repeated from the data in Table 4.7.

been done for Sb_2Te_3 thin film co-evaporated at T_{sub} = 180 °C. At low substrate temperatures, Sb_2Te_3 films exhibit poor TE properties and similar morphology on both substrates (Figure 4.31).

Hall coefficient measurement shows high carrier concentration of ~ 9×10^{19} cm^{-3} for both samples around room temperature and consequently comparable Seebeck coefficient and resistivity values. Similar to Bi_2Te_3 films, it can be concluded that the crystallinity of

T_{sub}	$FR_{(Sb:Te)}$	ρ (μΩ-m)	α_s (μV/K)	$\alpha_s^2/\rho k$ (mW/K^{2}m)	At% (Sb:Te)
250	1:3	18.9	195	2.03	25.8 : 74.2
250	1.5:3	24.1	186	1.43	27.7 : 72.3
250	2:3	10.8	85	0.67	47.1 : 52.9

Table 4.9 Properties and composition of Sb_2Te_3 thin film deposited on Kapton® substrate at T_{sub} = 250°C with different $FR_{(Sb:Te)}$

substrate does not have significant effect on Sb_2Te_3 film TE characteristics. However, it has some effects on Sb_2Te_3 thin films mechanical properties such as adhesion and stress.

4.5.2.2. Substrate Material: Oxide vs. Polyimide (Kapton®)

As shown in Figure 4.26 and Table 4.7, Sb_2Te_3 films co-evaporation on oxide and Kapton® substrates at similar deposition conditions of T_{sub} = 250°C and FR=2:3 have very different morphology and TE properties.

Despite the effect of Kapton® lower surface temperature as discussed in Section 4.4.2.3, it seems the most important factor influencing Sb_2Te_3 films variation on the two substrates is the sticking coefficient of evaporated elements. Measured film composition shows that for a fixed $FR_{(Sb:Te)}$, the sticking coefficient of Te to Kapton® is lower than that of Te to oxide substrate. Therefore, Sb_2Te_3 film on Kapton® is rich in Sb and non-stoichiometric. The excess of Sb results in higher carrier concentration and Seebeck coefficient and resistivity reduction. The Hall effect measurement of Sb_2Te_3 samples in Figure 4.32 confirms the carrier concentration trend on both substrates.

The co-evaporation of Sb_2Te_3 film on Kapton® at T_{sub} = 250°C is examined with $FR_{(Sb:Te)}$=1:3 and 1.5:3 to adjust the composition. The EDS analysis shows that by reducing the elemental fraction ratio of Sb, the Sb_2Te_3 thin films become rich in tellurium

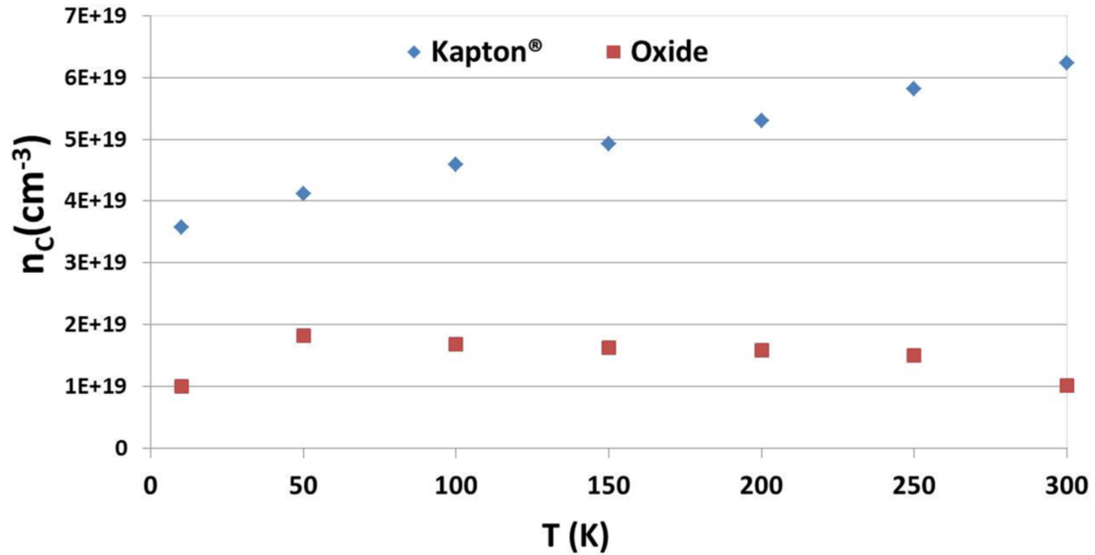


Figure 4.32 Carrier concentration of Sb_2Te_3 samples on Kapton® and oxide at T_{sub} = 250°C.

(Table 4.12). The XRD pattern of these samples in Figure 4.33 shows the presence of metallic tellurium with high peak intensity for (1,0,1), (1,0,2) and (1,1,0) planes.

4.5.3. Sb_2Te_3 Thin Film Co-evaporation Challenges

Sb_2Te_3 thin films are subject to large mechanical stresses under some deposition conditions. At the film/substrate interface, local stress depends on the internal stress due to thermal expansion coefficient mismatch and also due to elastic moduli mismatch. This interface sometimes fails due to delamination or brittle film fracture. Adhesion of a thin film on a substrate is critically dependent on the chemical nature, cleanliness, and microscopic topography of the substrate surface. It is possible to enhance the adhesion of the film to the substrate by increasing the kinetic energy of the incident particles. When the stored elastic energy in the film due to internal stresses is higher than the adsorption energy, the film has a tendency to peel off [88].

Sb_2Te_3 thin films exhibit high stress, poor adhesion and in some cases delamination from the substrate. Several approaches are examined to improve adhesion of Sb_2Te_3 especially

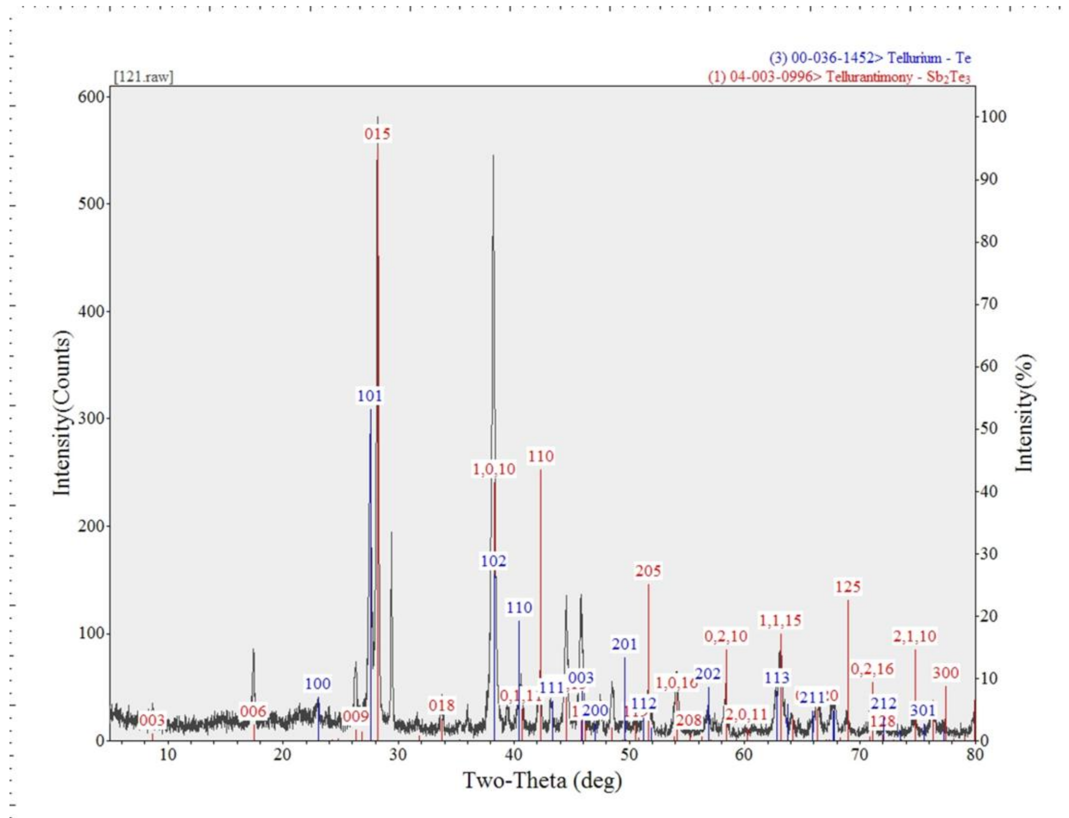


Figure 4.33 XRD pattern of Sb_2Te_3 thin film deposited on Kapton® at T_{sub} = 250°C and $FR_{(Sb:Te)}$=1:3. Peaks corresponding to metallic Te are observed.

for films deposited at higher substrate temperatures.

4.5.3.1. Pre-Evaporation Substrate Treatment

Sb_2Te_3 thin films have high stress and poor adhesion to the substrates compared to Bi_2Te_3 films. The very weak adherence of the Sb_2Te_3 film to glass and amorphous Si substrates results in TE film cracks and delamination. While high stress of the Sb_2Te_3 film on other substrates like poly-Si causes issues for successive processes on the samples as discussed in section 4.1. A series of standard cleaning process followed by *in situ* RF plasma etching is performed on substrates before thermal co-evaporation of Sb_2Te_3. The cleaning process is summarized in the following steps:

1. Piranha clean for 10 minutes.

2. DI water rinse of wafers for 2 minute.
3. Hydrofluoric (HF) dip for 1 minute in a 10:1 HF bath (DI H_2O:HF = 10:1).
4. DI water rinse of the wafers for 5 minutes.
5. Rinse and dry the wafers using the QDR tool.

These steps remove organic and metal contaminants from the surface of the wafers and are performed in the Lurie Nanofabrication Facility (LNF) at the University of Michigan. The TE material deposition tool is located outside of the LNF cleanroom facility. So, after loading the wafer inside the deposition chamber another cleaning step is performed to remove any possible contaminants created on the wafer surface occurring during the wafer transfer. The *in situ* wafer cleaning is accomplished by the inert gas plasma etching capability of Lab 18 thermal evaporation tool as discussed in Section 3.2. RF plasma cleaning is carried out for five minutes using Argon gas at a pressure of 25 mTorr.

After the cleaning process, Sb_2Te_3 thin films are co-evaporated on poly-Si and glass substrates at T_{sub} = 250°C. Deposited Sb_2Te_3 films on pre-evaporation treated substrates show noticeable improvement in adhesion. These TE films are not delaminated from the substrate after unloading from the processing chamber. No cracks or peeling are observed in the thin film. The improved adhesion of Sb_2Te_3 film is also examined by trying to remove it with a piece of scotch tape and later by polishing of the TE films.

Substrate	T_{sub} (°C)	FR(Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Sb:Te)
Pre-Evap. Treated Poly-Si	250	2:3	10.7	101	0.95	44.3 : 55.7
	250	1.5:3	23.3	167	1.2	40.9 : 59.1
Poly-Si	250	2:3	32.2	195	1.12	40.1 : 59.9
Pre-Evap. Treated Glass	250	2:3	35.2	175	0.87	37.1 : 62.9
Glass	180	2:3	48	177	0.65	32.7 : 67.3

Table 4.10 TE properties of Sb_2Te_3 thin film on cleaned and RF plasma etched poly-Si substrates with different evaporation FRs.

The TE properties of Sb_2Te_3 thin film on cleaned and RF plasma etched poly-Si substrates are summarized in Table 4.10. It should be noted that by adjusting $FR_{(Sb:Te)}$, TE properties of the Sb_2Te_3 film on pre-evaporation treated substrates becomes comparable to those for Sb_2Te_3 film on un-cleaned poly-Si substrate at T_{sub} = 250 °C. Meanwhile, its mechanical properties such as high stress and poor adherence to the substrate have improved significantly. This makes it feasible to polish these films. Table 4.10 also shows that after pre-evaporation substrate treatment it is possible to deposit Sb_2Te_3 on glass substrates at a higher temperature without causing TE film delamination. Furthermore, the TE properties of Sb_2Te_3 film on glass at T_{sub} = 250 °C improve compared to those at T_{sub} = 180 °C. Mechanical characteristic of Sb_2Te_3 film before and after substrate treatment are summarized in Table 4.11.

4.5.3.2. TE Film Deposition on a Thin Layer of Chrome

An alternative approach for increasing the adhesion between the TE film and the substrate is depositing a thin layer of a different material with good adhesion to both the

Substrate	T_{sub} (^{o}C)	Sb_2Te_3 film delamination	Cracks in Sb_2Te_3 film	Scotch tape film adhesion test	Sb_2Te_3 film polishing
Pre-Evap. Treated Poly-Si	**250**	**No**	**No**	**Good**	**Successful**
Poly-Si	**250**	**No**	**Yes**	**Poor**	**Not possible**
Pre-Evap. Treated Glass	**250**	**No**	**No**	**Good**	**Successful**
Glass	**250**	**Yes**	**Yes**	**Poor**	**Not possible**
Glass	**180**	**No**	**Yes**	**Average**	**Not possible**

Table 4.11 Mechanical characteristics of Sb_2Te_3 thin film before and after the substrate treatment process.

film and substrate. The thin intermediate layer should not introduce adverse effects on TE properties. Chrome has been used as an adhesion layer in the semiconductor industry. It also has been shown that addition of Cr causes an enhancement in the power factor of Bi_2Te_3 [45]. NiCr is also used successfully in a flexible thermoelectric power generator [69].The increase of Cr doping in manganese silicides TE materials leads to reduction of electrical resistivity and Seebeck coefficient by as much as 15% and 5%, respectively, and as a result the power factor value is enhanced [64]. Therefore, the effect of a Cr adhesion layer for Bi_2Te_3 and Sb_2Te_3 thin film co-evaporation is investigated in our work as well.

For this study, a Cr layer with thickness of 200 Å is deposited on the Si substrate. Ideally, Cr deposition should be performed right before TE material co-evaporation and in the same high-vacuum chamber. However, since Cr deposition process has not been calibrated in the KJL thermal evaporation tool, deposition is done in a different tool. Subsequently, the Si wafer with Cr layer is transferred to the thermal evaporation system for TE materials. Since the wafer is taken out from the high-vacuum chamber and is

Substrate	TE Material	T_{sub} (°C)	FR (Bi/Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Bi/Sb:Te)	Cracks in TE film	Adhesion test
Cr/poly-Si	Bi_2Te_3	270	1:3	11.2	-172	2.64	41.8 : 58.2	No	Good
Poly-Si	Bi_2Te_3	270	1:3	10.5	-180	3.08	39.2 : 60.8	No	Average
Cr /poly-Si	Sb_2Te_3	250	2:3	24.4	152	0.95	40.4 : 59.6	No	Good
Poly-Si	Sb_2Te_3	250	2:3	32.2	195	1.12	40.1 : 59.9	Yes	Poor

Table 4.12 Thermoelectric and mechanical properties of Bi_2Te_3 and Sb_2Te_3 thin films with and without the underlying Cr layer.

exposed to atmosphere pressure, oxide and other contamination might exist on the deposited Cr layer. Therefore, before co-evaporation of the TE material, RF plasma etching process is run for ~ 5 minutes to clean the substrate surface, which also result in thinning of the Cr layer.

TE materials deposition conditions and their corresponding TE properties with and without existence of the thin Cr layer are summarized in Table 4.12. Since deposited TE thin films are not very thick (< 1 μm TE film vs. < 100 Å of Cr), the effect of Cr layer parallel resistance must be taken into account when calculating the actual in-plane resistivity of TE films.

Electrical resistivity of Cr thin film is ρ_{Cr} = 0.13 μΩ-m and during the RF plasma cleaning of the substrate, the thickness of Cr layer further decreases (< 100 Å). Assuming the final thickness of the Cr layer is about 50 Å, the actual resistivity of Bi_2Te_3 and Sb_2Te_3 thin films are calculated and reported in Table 4.12. These calculated values (ρ_{BiTe} = 11.2 μΩ-m and ρ_{BiTe} = 24.4 μΩ-m) are higher than the measured resistivity of the TE samples (6.7 μΩ-m for Bi_2Te_3 and 14.3 μΩ-m for Sb_2Te_3) using the 4-Point Probe tool

because of the low resistance of the underlying Cr layer. The Seebeck coefficient values reported in Table 4.9 are measured directly without considering the effect of underlying Cr layer.

Measured properties demonstrate that TE properties of Bi_2Te_3 and Sb_2Te_3 thin films on Cr layer/poly-Si degrade slightly compared to those of films deposited directly on poly-Si. However, the improved adhesion of Sb_2Te_3 on Si substrate for high deposition temperatures (T_{sub} = 250 °C) makes TE film co-evaporation on a thin underlying Cr layer beneficial for many applications.

4.5.4. Polishing Process of Bi_2Te_3/Sb_2Te_3 Thin Films

(Bi,Sb)Te-based binary TE films, especially those deposited at high substrate temperatures tend to have a very rough surface and high electrical resistivity. The polishing of TE thin films has been investigated to reduce the surface roughness, to smooth ragged surfaces and to planarize the top surface of TE film. The TE film surface planarization makes the deposition of successive layers over TE material feasible for many microsystems applications. Electrical resistivity measurement of TE film samples before and after the polishing process shows the reduction of electrical resistivity with decreasing the surface roughness.

Polishing of TE films is performed with a Logitech PM2A Lapper in the LNF Wet Chemistry laboratory. And the process is summarized in the following steps:

1. Mounting TE samples on the glass carrier:
   - 1.1. The glass carrier is cleaned with a wipe and acetone and both sides of it are inspected for possible nicks and scratches.
   - 1.2. The glass carrier (rough side up) is placed on a press that is mounted on the hot

plate (at 50 – 60 °C).

1.3. A thin layer of wax is spread on the carrier, and samples are placed on the wax layer with the side to be lapped facing up.

1.4. A wipe is placed on top of the samples to avoid sticking to the press. Then the press arm is released on the samples. The pressure is applied for ~ 8 minutes to ensure flat mounting of the samples.

1.5. The press arm is raised and the glass carrier with the attached samples is released. The carrier should be cooled down to room temperature before the next steps.

1.6. Excess wax on top of the samples is gently removed by swabbing the surface with xylene. Excess particles are blown off using a N_2 gun.

2. Lapping:

2.1. The Lapping tool is cleaned and operated as described in the Standard Operating Procedure (SOP) for the Lapper/Polisher.

2.2. 0.3 µm slurry (the smallest available slurry size) is used for polishing TE films.

2.3. The amount of jig force on the samples should not exceed 0.5 kg. This amount of force removes ~ 0.4 µm of TE film per minute.

2.4. TE polished samples are checked every 30 seconds. The lapping time should not exceed 2 minutes for the TE films with thickness of ~ 1 µm.

2.5. After polishing the thin film, the glass wafer is removed, rinsed with DI water and dried.

3. Ultrasound Cleaning

3.1. Samples are placed in the ultrasound cleaner to remove the residues produced

during the lapping process.

3.2. The ultrasound tank is filled with DI water and the glass carrier is placed in the container and the cleaning is performed for ~ 3 minutes.

3.3. After checking the TE film surface under microscope, the samples are detached from the glass carrier.

3.4. The hot plate is set to appropriate temperature to melt the wax and then the sample is gently pushed off the glass carrier with a Teflon tweezers.

Polishing of the TE film is examined on both Bi_2Te_3 and Sb_2Te_3 samples. The surface of Bi_2Te_3 thin film becomes shiny after ~ 1 minute of lapping, while Sb_2Te_3 thin films

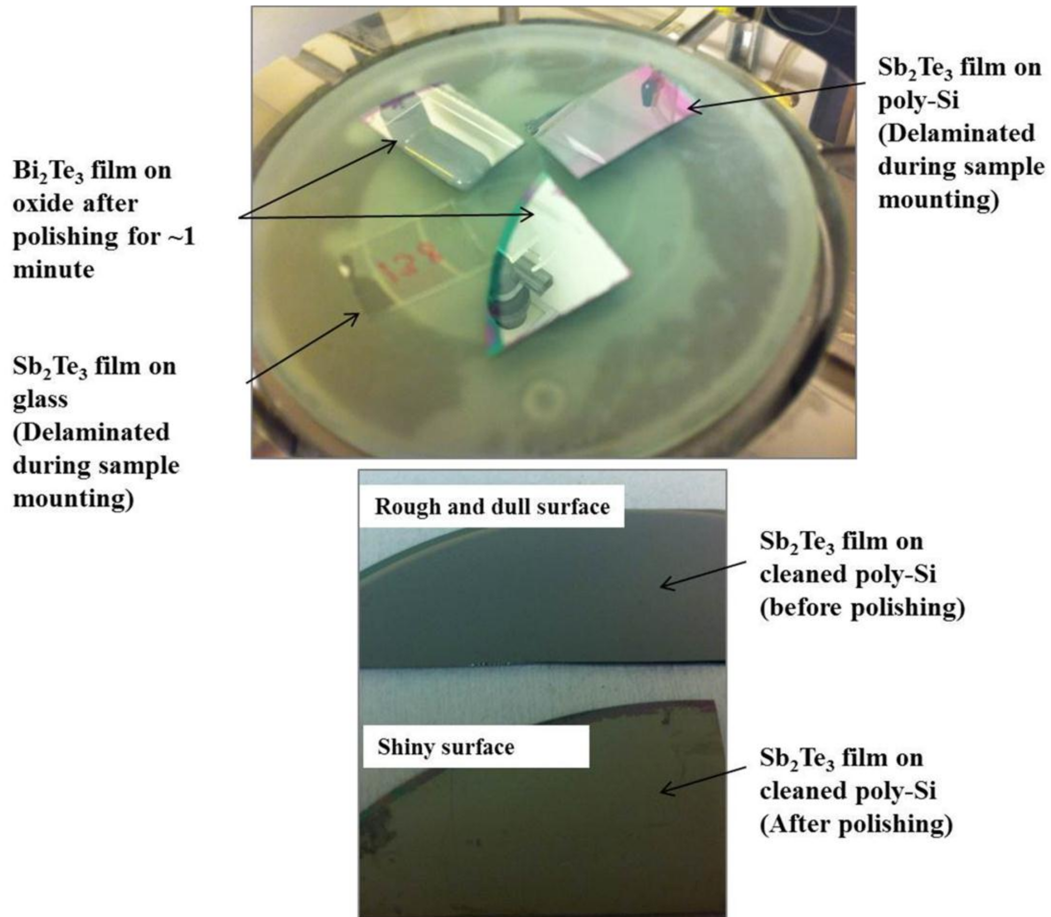


Figure 4.34 Polishing of Bi_2Te_3 and Sb_2Te_3 TE thin films.

TE Material	Substrate	Thickness (µm)		R_q(nm)	
		Before Polish	After Polish	Before Polish	After Polish
Bi_2Te_3	Poly-Si	0.98	0.33	52	7.5
Sb_2Te_3	Poly-Si (Cleaned)	1.33	0.88	40	7.8

Table 4.13 The effect of polishing on TE film thickness and surface roughness.

delaminated from the substrate during the mounting step due to poor adhesion to the substrate (Figure 4.34).

Table 4.13 shows the effect of polishing on TE film thickness and surface roughness for both Bi_2Te_3 and Sb_2Te_3 thin films.

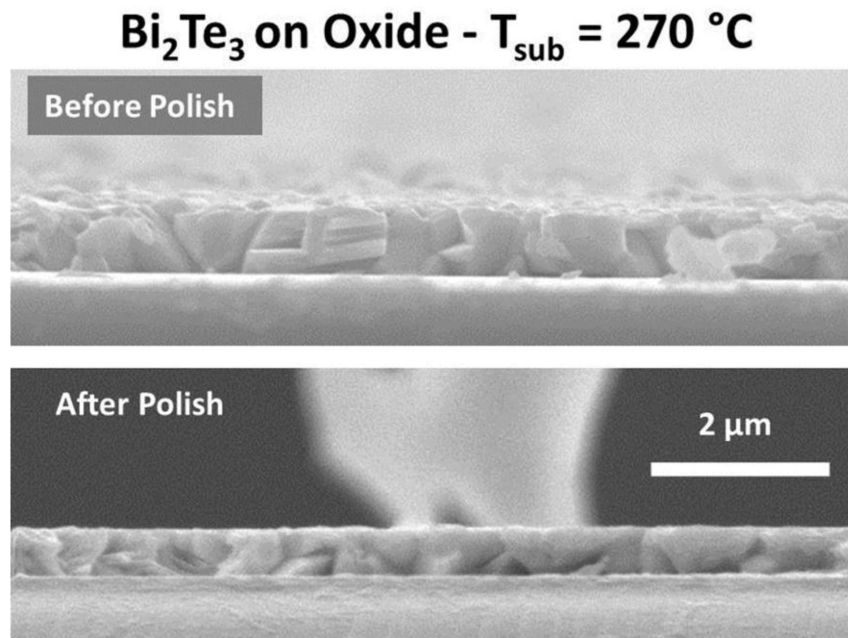


Figure 4.35 Cross-sectional SEM micrographs of Bi_2Te_3 thin films on oxide substrate before and after polishing.

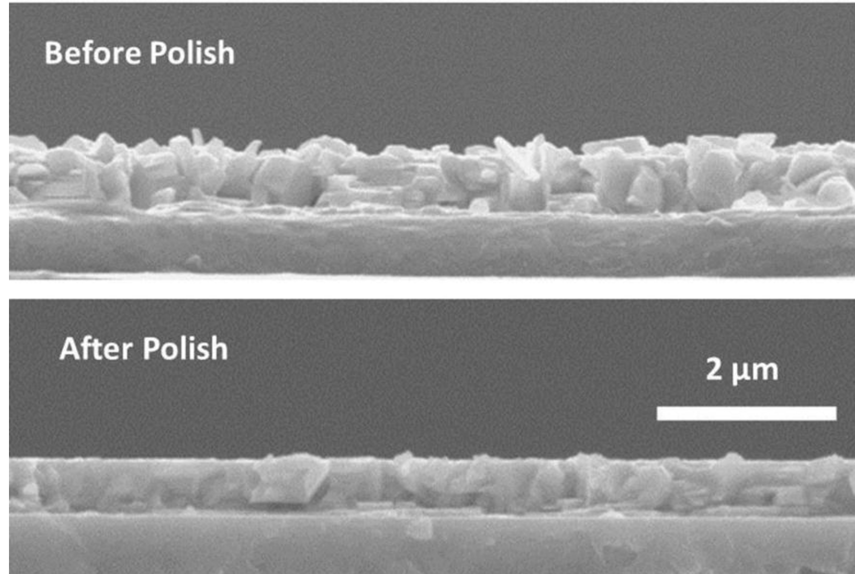


Figure 4.36 Cross-sectional SEM micrographs of Sb_2Te_3 thin films on oxide substrate before and after polishing.

Cross-sectional SEM micrographs of Bi_2Te_3 thin film on Oxide substrate before and after polishing process are shown in Figure 4.35. Successive runs of polishing on Sb_2Te_3 deposited on prepared substrates are carried out successfully. Cross-sectional SEM micrographs of Sb_2Te_3 thin film on cleaned poly-Si substrate before and after polishing

TE Material	Substrate	T_{sub} (°C)	FR (Bi/Sb:Te)	Resistivity Before Polishing (µΩ-m)	Resistivity After Polishing (µΩ-m)
Bi_2Te_3	Oxide	270	1:3	30.4	28.1
Bi_2Te_3	Poly-Si	270	1:3	20.5	19.4
Sb_2Te_3	Poly-Si (Cleaned)	250	2:3	10.2	9.5
Sb_2Te_3	Poly-Si (Cleaned)	250	1.5:3	23.3	21.0

Table 4.14 Electrical resistivity of TE films before and after polishing.

process are shown in Figure 4.36.

The lapping process is performed on several samples, resulting in a consistent electrical resistivity decrease of ~ 5-10% in both Bi_2Te_3 and Sb_2Te_3 thin films (Table 4.14).

4.6. Summary

This chapter presented the optimization of binary (Bi,Sb)Te-based thin films prepared by thermal co-evaporation. The effect of substrate material and crystallinity on the TE film characteristics has been investigated. The substrate material, temperature, and film composition are found to be the most important parameters affecting TE film performance. Optimum power factors for *n*-type Bi_2Te_3 films are obtained on poly-Si and Kapton® substrates for T_{sub} = 270 °C and tellurium concentration of about 60%. For *p*-type Sb_2Te_3, optimum power factors belong to the films deposited on oxide and poly-Si substrates at T_{sub} = 250 °C and tellurium concentration of about 60%. It is observed that composition of Sb_2Te_3 film is very sensitive to the substrate material and substrate temperature during deposition. In general, co-evaporation of Sb_2Te_3 is more complicated than Bi_2Te_3 material and it is difficult to optimize thermoelectric and mechanical properties of Sb_2Te_3 thin films. Several issues in Sb_2Te_3 deposition have been studied and possible solutions were proposed and investigated. Two methods for improving the adhesion of Sb_2Te_3 thin films, namely substrate surface treatment and Cr layer deposition, were presented. Polishing of TE thin films has been investigated to reduce the surface roughness and to planarize the surface of TE film. Moving beyond deposition of binary alloys, the development of ternary (Bi,Sb)Te-based thermoelectric thin films by thermal co-evaporation is introduced and studied in Chapter 5.

Chapter 5

Deposition of (Bi,Sb)Te-based Ternary Thin Films by Thermal Co-evaporation

In Chapter 2, it was demonstrated that a good thermoelectric material with high figure-of-merit (ZT ~ 1) could lead to good performance in TE coolers and generators. It is well known that the best materials for room temperature TE applications are narrow band-gap energy semiconductors (E_g < 0.2 eV) such as (Bi,Sb)Te-based alloys [25]. These materials have been shown to have a high figure-of-merit, ZT ~ 0.8, in bulk form [76].

Increasing the Seebeck coefficient and decreasing electrical resistivity and thermal conductivity increase the value of Z ($\alpha^2/\rho\kappa$). It is possible to change the Seebeck coefficient and electrical resistivity by variation of carrier concentration. However, decreasing the free carrier concentration results in an increase both in the Seebeck coefficient and electrical resistivity. Therefore, the carrier density has to be optimized to attain the maximum value of power factor ($\alpha^2\sigma$). The other approach to increase the figure-of-merit, which has been of significant research interest during the recent years, is minimizing the thermal conductivity [76]. As discussed in previous chapters, thermal conductivity is composed of both electron and lattice thermal conduction. Electron thermal conduction depends on carrier concentration and carrier mobility. It is inversely

related to the electrical resistivity and is defined by Wiedemann-Franz law ($\kappa_e = \frac{LT}{\rho}$), where L is the Lorentz number and T is the absolute temperature. Therefore decreasing the contribution of electron thermal conduction will result in higher electrical resistivity. As a result it is not possible to minimize electron thermal conduction without causing an adverse effect on the material power factor. However, the phonon thermal conduction component depends only on lattice properties. Forming mixed crystals such as $(Bi_{1-x}Sb_x)_2Te_3$, as shown in [76], is one approach for reducing lattice thermal conduction. This is due to a reduction in the mean free path of phonons without a similar reduction in the mean free path of the charge carriers.

As shown in Figure 5.1, in these mixed compounds, the lowest lattice thermal conduction

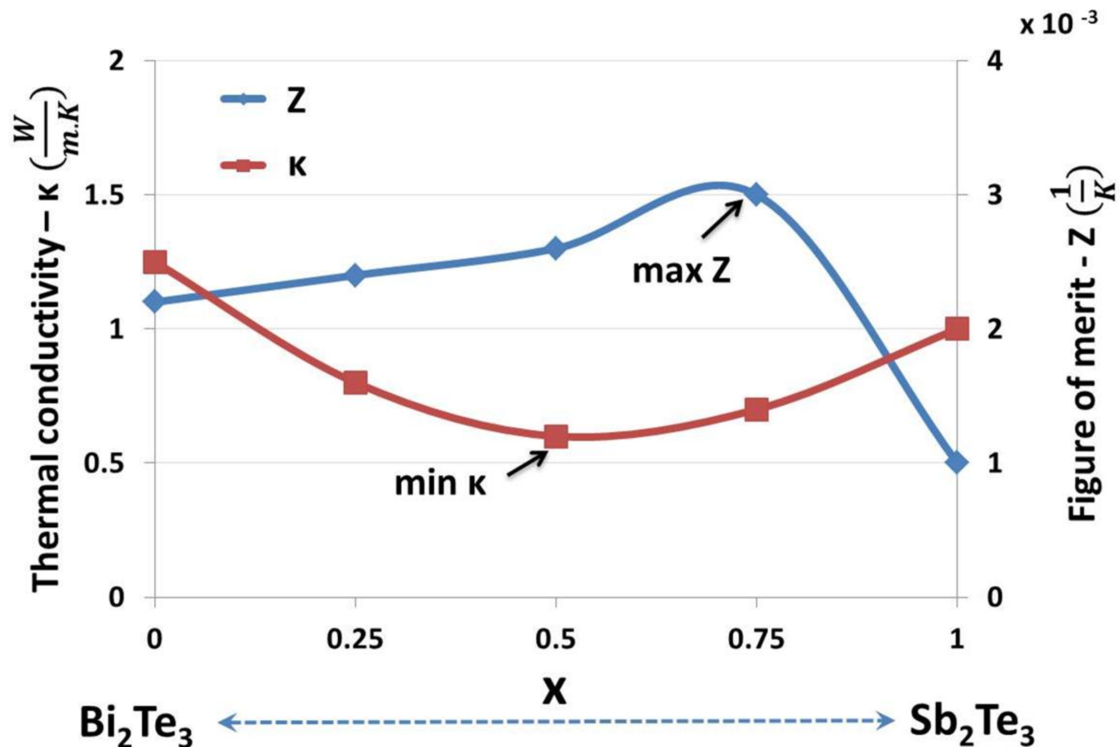


Figure 5.1 TE figure-of-merit and lattice thermal conductivity for $(Bi_{1-x}Sb_x)_2Te_3$ single crystals as a function of composition x (reproduced from [76])

is expected to happen at the point of maximum disorder (x = 0.5) of both Bi_2Te_3 and Sb_2Te_3 compounds. Interestingly, the maximum figure-of-merit in ternary $(Bi_{1-x}Sb_x)_2Te_3$ materials occurs at the x=0.75 composition instead of x=0.5. This point corresponds to the optimum carrier concentration in such mixed crystal materials. $Bi_{0.5}Sb_{1.5}Te_3$ has been proven to be a *p*-type TE material with $ZT \approx 1$ at room temperature. The crystal structure is composed of atomic layers in the order of Te(1)-Sb-Te(2)-Bi-Te(1) layers oriented along the *c*-axis. The Te layers are stacked together by weak van der Waals forces.

In *n*-type ternary alloys, alloying Bi_2Te_3 with Bi_2Se_3 greatly reduces the high sensitivity of *n*-type binary Bi_2Te_3 TE properties to the atomic ratio of Bi and Te, in addition to

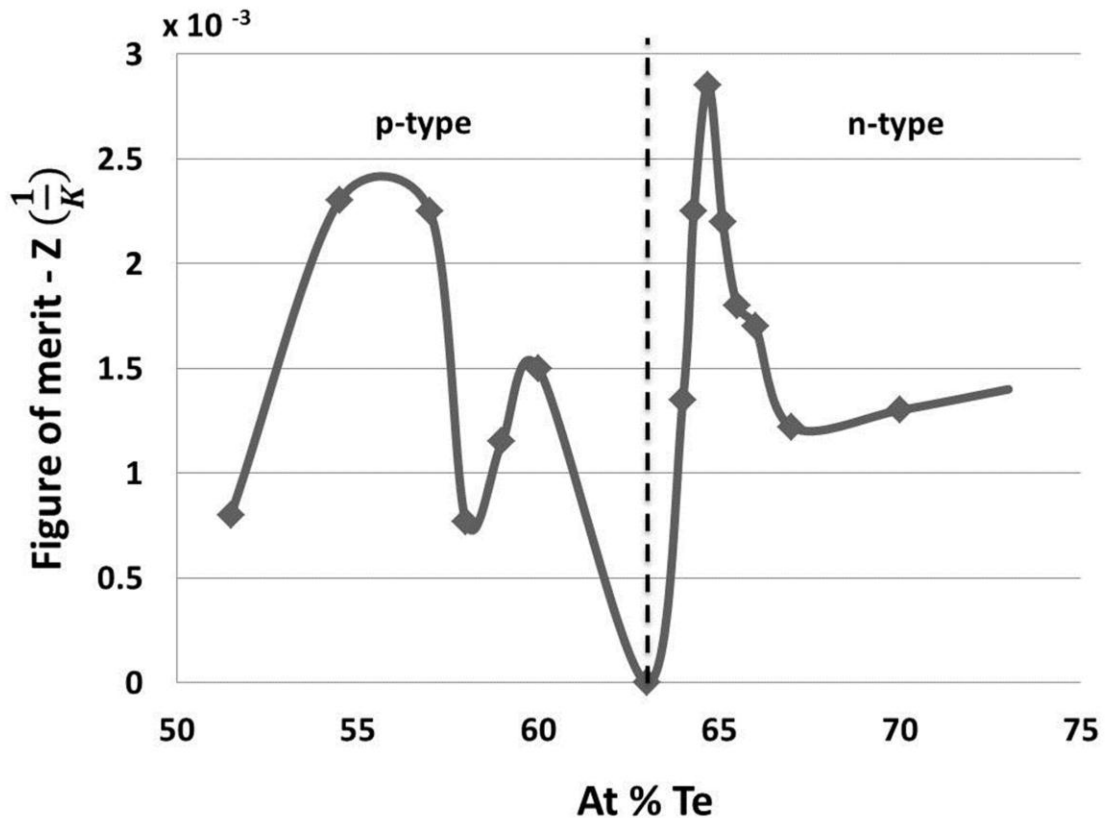


Figure 5.2 Figure-of-merit vs. the liquidus composition for both *n*- and *p*-type Bi_2Te_3 (reproduced from [27])

lowering lattice thermal conduction. Figure 5.2 illustrates that precise control of the stoichiometric deviation is necessary to obtain an optimum value of *Z* in *n*-type binary Bi_2Te_3 material [27]**.** In the case of the $Bi_2(SeTe)_3$ materials, increasing the energy gap reduces the influence of minority carriers and results in a less critical range for optimal figures-of-merit [76]. Properties of some of the state-of-the-art ternary bulk materials are reported in Chapter 2.

5.1. Thermal Co-evaporation of $(BiSb)_2T_3$ Thin Films

Many commercial macro-scale TE devices have used bulk $(Bi,Sb)_2Te_3$ for *p*-type and $Bi_2(Te,Se)_3$ for *n*-type due to their higher figure-of-merit compared to binary alloys. Because of the high performance of ternary TE alloys in the bulk form, investigation of their thin films characteristics and understanding of the transport properties can have a great impact for applications of the TE films in micro devices. In this work we investigate polycrystalline ternary $(Bi_{0.25}Sb_{0.75})_2Te_3$ thin film is as a *p*-type TE material.

5.1.1. Deposition Techniques

Various techniques have been used to develop thermoelectric thin films and deposit them on the desired substrates. Selected deposition techniques, namely flash evaporation [22,31,89,92], sputtering [71], ECD [63,75,86], MBE [17] and MOCVD [35,68] for ternary and quaternary TE thin films, along with material performance parameters are described in section 2.3. Here, the performance of ternary thin films prepared by different deposition techniques is discussed in more detail.

Deposition of *n*-type $Bi_2Te_{2.7}Se_{0.3}$ and *p*-type $Bi_{0.5}Sb_{1.5}Te_3$ targets on the glass and Al_2O_3 substrates by direct current magnetron sputtering is reported in [9]. It was found that the

composition of the sputtered thin films is close to the sputtering target. The highest power factors are 1.2 mW/K^2m for *n*-type film and 1.0 mW/K^2m for *p*-type film after annealing at 250 and 300 °C, respectively.

In [30], *n*-type $(Bi_2Te_3)_{0.9}(Bi_2Se_3)_{0.1}$ and *p*-type $(Bi_2Te_3)_{0.25}(Sb_2Te_3)_{0.75}$ thin films were prepared on polyimide substrate by a flash evaporation technique. TE properties before annealing were $Z=0.21\times10^{-3}$ K^{-1} for *n*-type and $Z=0.17\times10^{-3}$ K^{-1} for *p*-type. After annealing at 250 °C in a He atmosphere, the value of Z increased to 3.2×10^{-3} K^{-1} for *n*-type and 1.6×10^{-3} K^{-1} for *p*-type. Flash evaporation was used to deposit *n*-type $Bi_2Te_{2.4}Se_{0.6}$ thin film on glass [79]. The power factor of the samples was increased to 0.2 mW/K^2m after annealing at 200 °C for 1 hour. *P*-type $Bi_{0.4}Sb_{1.6}Te_3$ thin films with preferred *c*-axis orientation were deposited by the flash evaporation technique, too [89]. The results revealed that the grain growth and the crystal structure along the *c*-axis are enhanced as the annealing temperature and duration increases. The *p*-type $Bi_{0.4}Sb_{1.6}Te_3$ thin films annealed at 300 °C exhibit the highest TE power factor of 0.35 mW/K^2m.

N-type $Bi_2(Te_{1-x}Se_x)_3$ thin films with x = 0, 0.2, 0.4, 0.6, 0.8, and 1.0 were developed by thermal evaporation of the synthesized bulk materials [87]. The interesting result of this study was that, the introduction of Se into Bi_2Te_3 did not lead to figure-of-merit enhancement, while *ZT* was increased significantly by annealing of the low resistivity samples.

As discussed so far, the thin film deposition techniques for ternary thermoelectric compounds, including sputtering, flash evaporation, thermal evaporation and pulsed laser deposition, all encounter difficulty obtaining thin films with stoichiometric composition. The deposition temperature, atmosphere, post-annealing process, as well as the substrate

have major effects on the quality of the ternary films.

By far, most $Bi_{0.5}Sb_{1.5}Te_3$ thin films were prepared on crystalline substrates at room temperature and annealed at high temperatures. The XRD pattern of $Bi_{0.5}Sb_{1.5}Te_3$ samples has shown that as-grown thin film exhibits amorphous structure. It was found that the $Bi_{0.5}Sb_{1.5}Te_3$ thin films crystallized in the rhombohedral structure with space group *R*3*m* after annealing. The annealing process could enhance the crystallinity of samples by removing defects such as voids, grain boundaries, dislocations, stress, which, in turn, improved the electrical properties of the films.

The development of $Bi_{0.5}Sb_{1.5}Te_3$ thin film on amorphous substrates without post-deposition annealing seems to be quite challenging. In this work $(BiSb)_2Te_3$ ternary films are developed and characterized for the first time by the co-evaporation technique. To the best of our knowledge, no other works have investigated and reported results on ternary alloys prepared by the thermal co-evaporation technique. This chapter demonstrates a low-cost, simple, and reliable co-evaporation technique for depositing high figure-of-merit ternary TE films, which will open up new ways to pursue novel micro-scale applications of thermoelectrics.

5.1.2. Experiments

An initial study of ternary film co-evaporation is performed by deposition of *p*-type $(BiSb)_2Te_3$ films with thickness of ~ 1 μm ± 20% on LPCVD poly-silicon substrate. Co-evaporation of ternary films is performed at various substrate temperatures with fixed elemental evaporation rates. Pure material sources (99.999% Bi, Sb shots and Te powder) for each element in the ternary compound were used in the thermal co-evaporation system. These alloys are deposited at T_{sub} = 160, 200 and 240 °C with $FR_{(Bi:Sb:Te)}$ = 0.5:1.5:3.

Measurements have shown that the Seebeck coefficients of $(BiSb)_2Te_3$ films are positive, indicating that the films are *p*-type. Figure 5.3 compares the binary Sb_2Te_3 film and the ternary $(BiSb)_2Te_3$ film co-evaporated on Si substrate at T_{sub} = 160 °C. The difference in morphology and grain structure of binary and ternary TE samples is illustrated using surface and cross-section SEM micrographs. The grain size of $(BiSb)_2Te_3$ is significantly smaller than the binary *p*-type material deposited at the same substrate temperature. Smaller grain size in the ternary material crystal structure results in higher boundary scattering of charge carriers. The ternary thin film usually has a shiny surface and exhibits good adhesion to the poly-Si substrate.

As a result, the carrier mobility decreases and there is a sharp increase in electrical resistivity of these alloys compared to binary Te-based materials. The cross-section SEM

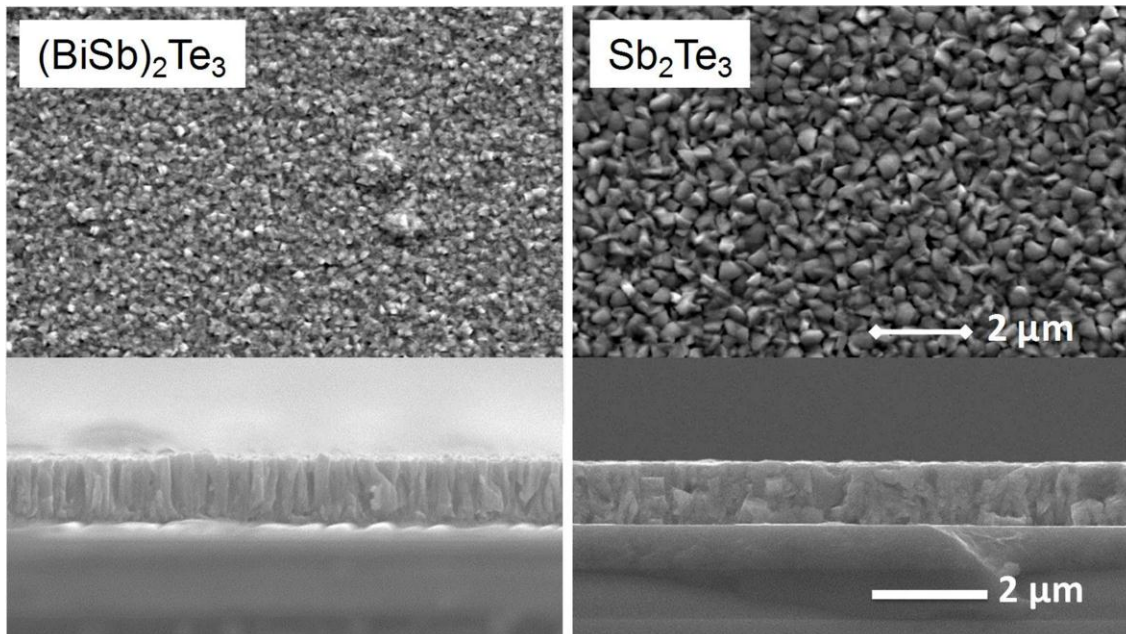


Figure 5.3 Grain size of p-type ternary $(BiSb)_2Te_3$ is much smaller than p-type binary Sb_2Te_3 deposited at same T_{sub}=160 °C on Si substrate.

T_{sub}	FR (Bi:Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Bi:Sb:Te)	Average Roughness (nm)
160	0.5:1.5:3	162	85	0.045	10.4:27.8:61.8	21.1
200	0.5:1.5:3	169	113	0.075	7.4:28.9:63.7	45.2
240	0.5:1.5:3	161.7	75	0.038	8.2:30.6:61.2	89.6

Table 5.1 Characteristics of $(BiSb)_2Te_3$ films on Si substrate at various temperatures.

of these films also demonstrate the preferred *c*-oriented columnar crystal structure of $(BiSb)_2Te_3$ film, in contrast to the randomly oriented grain in the polycrystalline structure of Sb_2Te_3 thin film. In a material with columnar crystals oriented in the same direction, transport properties depend on the orientation of the grain. The strong anisotropy characteristic of these crystal structures can be another reason for poor TE properties in planar direction.

5.1.3. Effect of Substrate Temperature

The effect of deposition temperature on the co-evaporated $(BiSb)_2Te_3$ films is analyzed by surface and cross-section SEM micrographs and AFM measurements, and shown in Figure 5.4. Characteristics of these films on Si substrate are summarized in Table 5.1. As we increase the substrate temperature, the grain size and surface roughness of the film increases. All films exhibit very high resistivity (> 100 μΩ-m) and low Seebeck coefficient (~ 100 μV/K). The high electrical resistivity of $(BiSb)_2Te_3$ samples is not affected by the deposition temperature and roughness of the films [34].

The X-ray diffraction (XRD) patterns of TE samples are compared to bismuth antimony telluride and silicon powder profile as shown in Figure 5.5. The XRD study shows high peak intensity for the (0,1,5), (1,0,10) and (2,0,5) planes, but no significant increase in *c*-

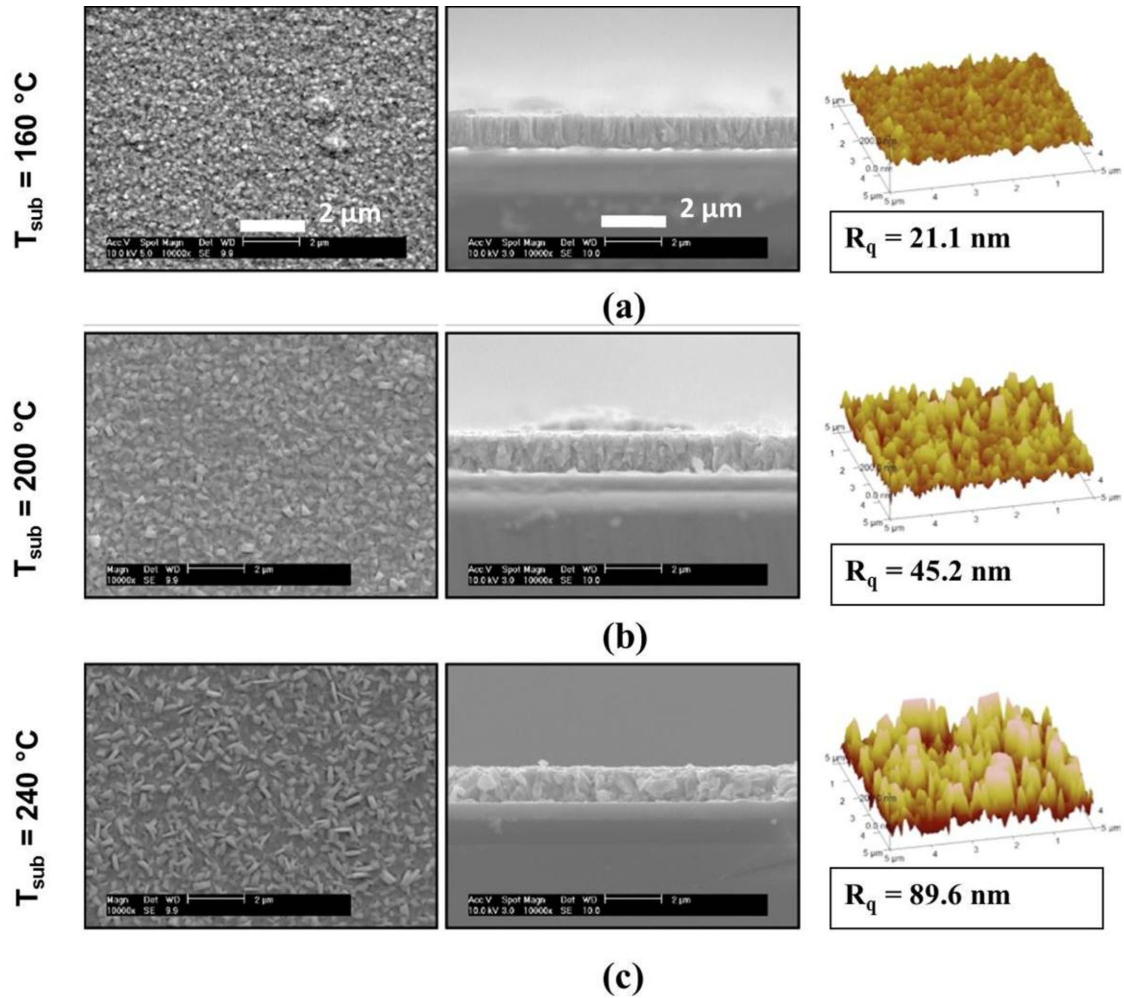


Figure 5.4 Deposition of $(BiSb)_2Te_3$ films on Si substrate at various temperatures.

axis orientation with increasing temperature.

$(BiSb)_2Te_3$ thin films have very poor power factor compared to binary (Bi,Sb)Te-based TE films. The maximum power factor achieved is 75 $\mu W/K^2m$, which is more than an order of magnitude less than that of antimony telluride. The cause of the reduction in Seebeck coefficient can be due to modified electronic structure and/or additional carrier doping during the film growth. However, a reduction in lattice thermal conductivity is also expected due to increased phonon scattering at the interfaces.

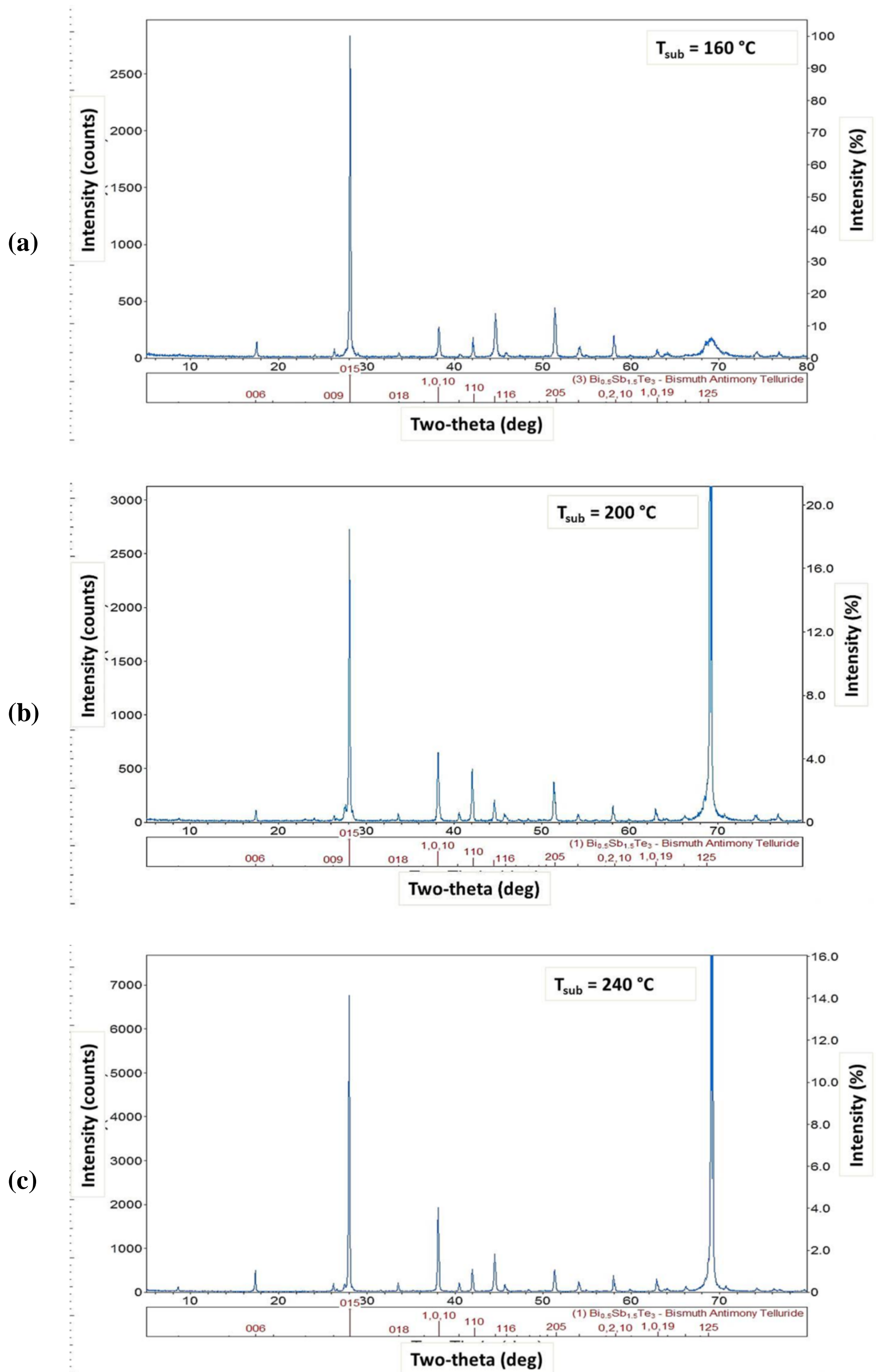


Figure 5.5 XRD of $(BiSb)_2Te_3$ films co-evaporated on Si at different substrate temperatures.

Substrate	ρ (μΩ-m)	At% (Bi:Sb:Te)	Avg. Roughness (nm)
Oxide	206	8.3:32.2:59.5	82.2
Glass	74.4	9.3:33.2:57.5	18.2
Amorph-Si	162	10.4:27.8:61.8	21.1

Table 5.2 Characteristics of (BiSb)2Te3 films on various substrate at $T_{sub} = 160^oC$.

5.1.4. Co-evaporation of $(BiSb)_2Te_3$ on Different Substrates

In addition to the silicon substrate, $(BiSb)_2Te_3$ thin films were co-evaporated on silicon

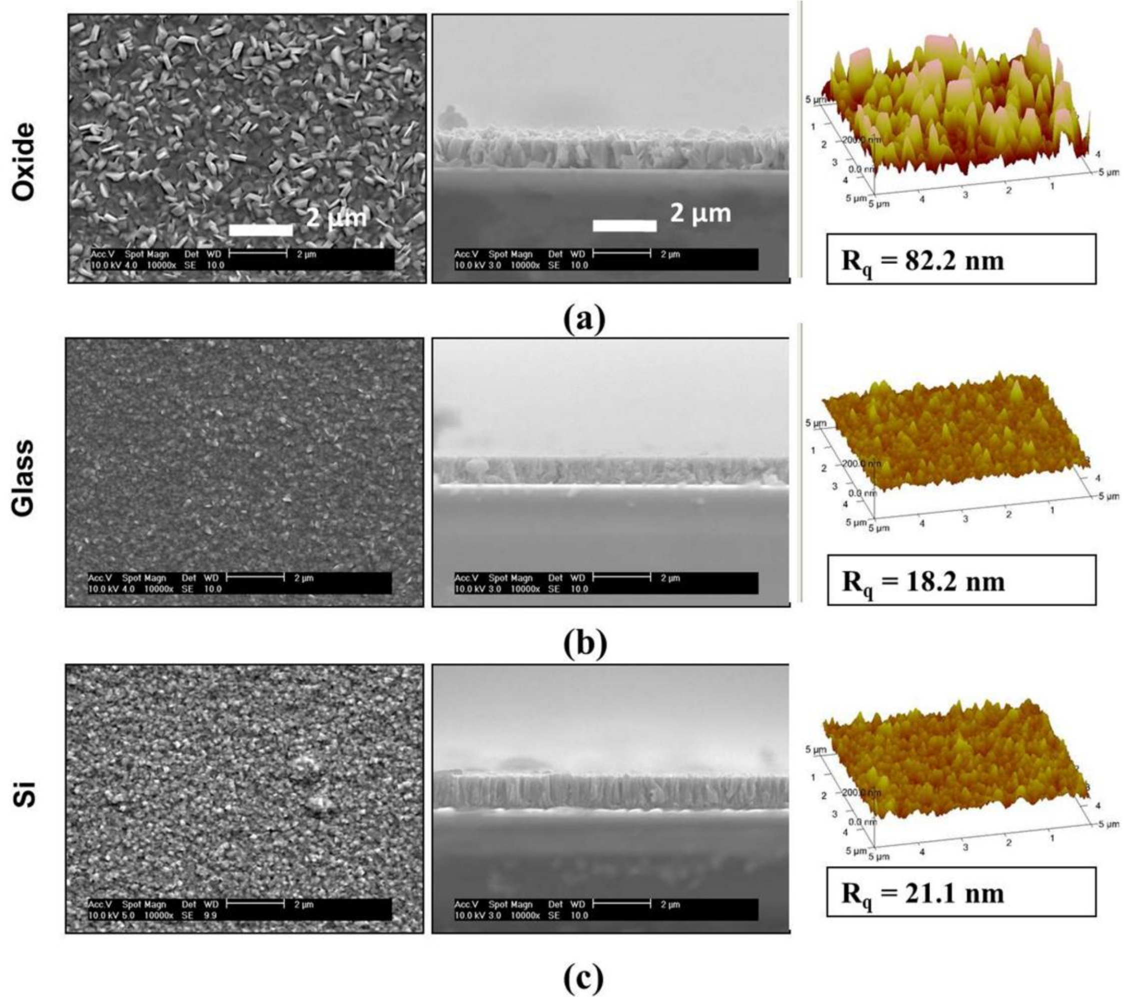


Figure 5.6 Deposition of $(BiSb)_2Te_3$ films on various substrates at $T_{sub} = 160^o C$

dioxide and glass substrates at T_{sub} = 160 °C. However, the films deposited on all three substrates exhibit rather poor TE properties as shown in Table 5.2. It should be noted that characteristics of the film deposited on the oxide substrate are quite different from the other two samples.

As can be seen in Figure 5.6, thin films morphology and crystal structure are different on oxide, as the ternary film deposited on this substrate shows large and randomly oriented grains. The maximum power factor for ternary $(BiSb)_2Te_3$ films is 0.26 mW/K^{2}m on glass substrate, at T_{sub}=160°C with Seebeck coefficient of 140 μV/K, electrical resistivity of 74.4 μΩ-m.

Diffraction patterns of these samples in Figure 5.7 confirm that $(BiSb)_2Te_3$ film on glass and Si substrates have more preferred *c*-axis orientation, but all films have very strong peak intensity for the (0,1,5) plane.

5.2. Summary

There is complete solid solubility between Bi_2Te_3 and Sb_2Te_3 compounds. Alloying these two compounds can improve the TE material figure-of-merit above the reported values for binary compounds due to thermal conductivity reduction via mass defect scattering.

In this chapter, deposition of (Bi,Sb)Te-based ternary films is investigated for the first time by co-evaporation. The analysis of first co-evaporated $(BiSb)_2Te_3$ thin films on Si substrates exhibits poor TE properties. The maximum power factor of $(BiSb)_2Te_3$ ternary TE film on Si is 75 μW/K^{2}m. Increasing the substrate temperature during deposition does not seem to enhance TE film performance, despite changing its morphology. The atomic percentages of the ternary films elements are somewhat off from the stoichiometric

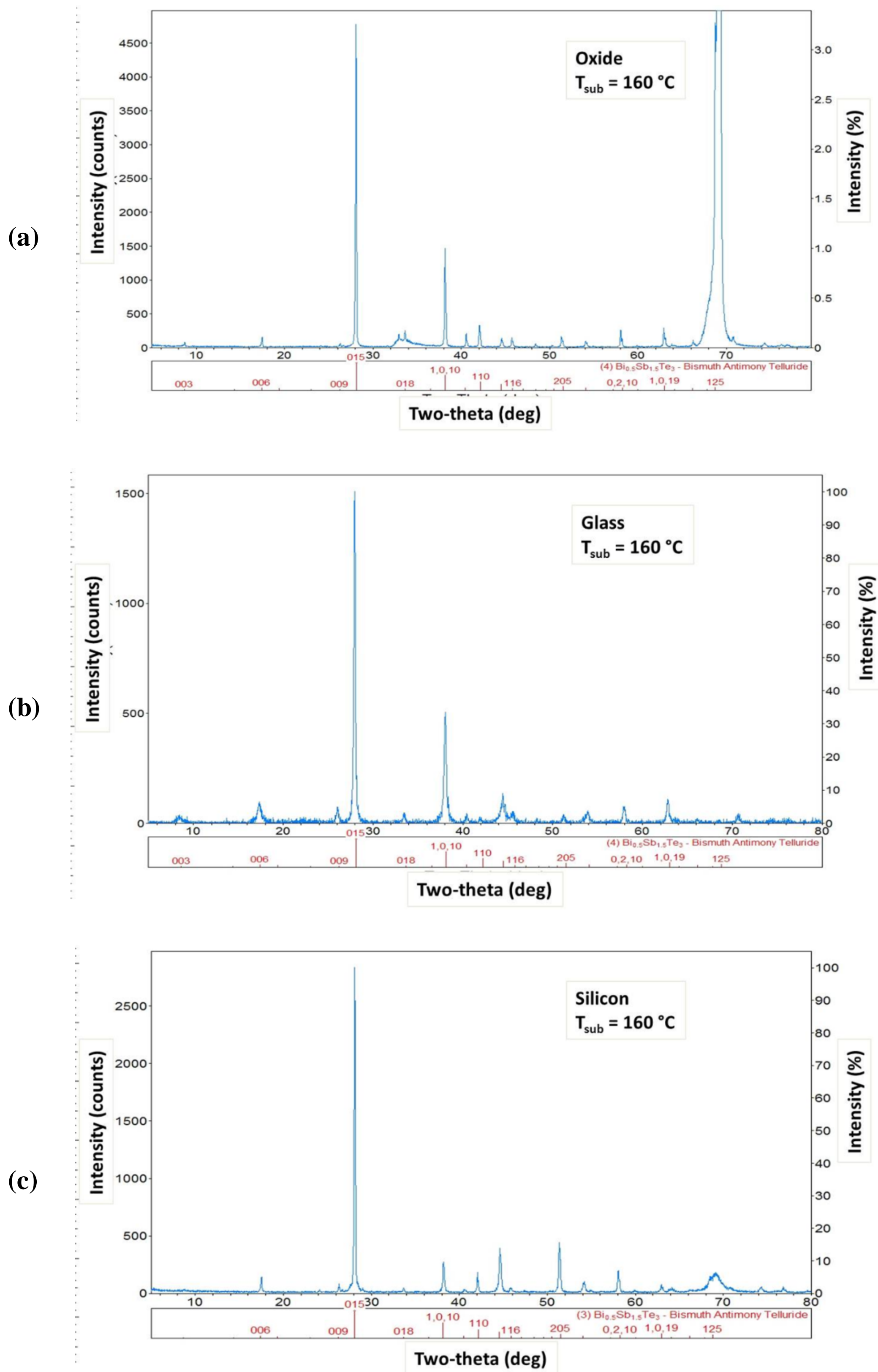


Figure 5.7. XRD of $(BiSb)_2Te_3$ films co-evaporated various substrates at $T_{sub} = 160\ ^oC$

composition. For the co-evaporated $(BiSb)_2Te_3$ thin films, the grain size is extremely small, the grain boundaries are dense, and the dominant orientation is normal to the (0,1,5) planes.

As deposition temperature goes up, the average grain size increases and the density of grain boundaries is reduced. This should affect the resistivity of the sample. However, no change in resistivity or new orientation of grains in $(BiSb)_2Te_3$ thin films co-evaporated at higher substrate temperature is observed. The reason for this is still unclear. The highest power factor for ternary $(BiSb)_2Te_3$ films is 0.26 mW/K^2m on glass substrate, at T_{sub}=160°C with Seebeck coefficient of 140 μV/K, electrical resistivity of 74.4 μΩ-m.

Based on other works, post deposition annealing seems to be a necessary step to optimize these films. Due to the high vapor pressure of tellurium, annealing is usually carried out in a pure gas atmosphere, such as in Argon or Helium or in a Te-rich environment to prevent re-evaporation. Annealing can cause re-crystallization and grain growth, reduce the structural defect concentration and thus improve charge carrier transport through the film [2].

Chapter 6

Characterization of Metal-Bismuth/Antimony Telluride Electrical Contact Resistivity

In order to maintain compatibility of thermoelectric coolers and generators with micro systems and CMOS processes, the size of TE devices needs to be scaled down. As a result, the role of electrical resistance between the contact metal and the TE thin film becomes important in determining the TE device performance. With the decrease of TE element length in micro-scale thermoelectric devices, the transport of heat and electrical current is affected by the electron-phonon non-equilibrium at TE/metal interfaces [19]. As the size of these devices decreases, the TE/metal contact electrical resistance becomes comparable with the electrical resistance of the TE element. Contact resistance increases the total electrical resistance of the TE device, generates Joule heating at the junctions, adds to the thermal load at the cold junction, and, as a result, considerably degrades efficiency.

The maximum acceptable level of contact resistivity for optimal TE micro-device performance has been investigated previously [43,44,95]. For instance, Gross *et al.* showed that the effect of contact resistance (R_c) is minimal for values of less than 1×10^{-9} $\Omega \cdot m^2$ in planar micro-coolers. As R_c increases, the cold stage temperature slowly

Reference	Gupta, et al. [44]	Gross, et al. [43]	Birkholz, et al. [4]	Foucaran, et al. [30]	Böttner, et al. [7]	Carmo, et al. [14]	This Work
Contact metal	Ni or Co	Cr/Au	Ag/Ni	Cu/Ni	Ag/Ni	Al/Ni	**Ti/Ni, Ti/Pt and Cr/Au**
TE material	Bi_2Te_3	Bi_2Te_3 and Sb_2Te_3	Bi_2Te_3 and $Bi_{0.64}Sb_{1.36}Te_3$	$(Bi_2Te_3)_{0.9}(Bi_2Se_3)_{0.1}$ and $(Bi_2Te_3)_{0.25}(Sb_2Te_3)_{0.75}$	Bi_2Te_3 and $(BiSb)_2Te_3$	Bi_2Te_3 and Sb_2Te_3	**Bi_2Te_3 and Sb_2Te_3**
Contact resistance ($\Omega\cdot m^2$)	10^{-11} (TLM)	1.03×10^{-8} (Fitted data)	10^{-9}	5×10^{-7}	10^{-10} (Fitted data)	2×10^{-7}, n-type 5×10^{-7}, p-type (TLM)	**10^{-8}-10^{-9}**
Additional treatment	*In situ* Ar sputter cleaning /annealing at 100°C	Novel layout of contact areas	Additional layer of Bi on Ni	Annealing at 250°C for 15 min	Additional layer of Bi on Ni	None	None

Table 6.1 Comparison of various contact metal materials.

approaches 300 K and performance degrades significantly for R_c values of more than 1×10^{-7} $\Omega\cdot m^2$ [43]. Therefore, it is crucial to properly characterize TE/metal interfaces and determine the optimal contact metal and shapes to achieve minimum contact resistivity.

TE film deposition on top of a metal often does not leave any gap at the interface. But different lattice parameters of the materials enforce some strain between the layers, which may lead to dislocation of atoms and formation of defects. This strain can also cause variations in stoichiometry of TE compounds, as well as diffusion of metal into the semiconductor. These surface defects greatly affect the transport of heat and electricity through the interface.

Since Bi_2Te_3/Sb_2Te_3 compounds are small band gap semiconductors, it is theoretically possible to obtain very low contact resistance ($\leq 10^{-11}$ $\Omega\cdot m^2$) for an ideal contact [95]. However, real metal–semiconductor interfaces are far more complex. In practice, R_c is the result of impurities, variations in the crystal structure, interface defects, and diffusion

of metal into semiconductor. Optimization of metal and contact shape, surface preparation, and annealing are important to achieve a near ideal contact. Table 7.1 summarizes contact metal-TE film materials, preparation techniques, and the resulting resistivity values in previous works [4,7,14,43,95] as well as this work.

6.1. Contact Metal Material

As shown in Table 7.1, various materials can be used as contact metals in micro TE modules. Nickel has been used as the contact metal of choice for bulk TE devices [54,76]. It is usually used as a diffusion barrier against penetration of solder and contact electrode (usually copper) into bismuth/antimony telluride.

Because of nickel's low diffusion into (Bi,Sb)Te-based bulk materials and its good contact resistivity, it has been chosen as the contact metal with TE thin films in micro devices. Other materials such as Co, Ag, Al, and Au have also been used as the metal contact with (Bi,Sb)Te-based thin films. Previous works at the University of Michigan used Au as the metal contact for fabrication of micro TE coolers [43]. Since co-evaporation of (Bi,Sb)Te-based thin films is not performed directly after metallization, it is not possible to use metals that oxidize easily, such as Ni, as the contact metal in such processes before surface treatment. Therefore, lower contact resistance could be achieved with noble metals such as Au or Pt.

Although various metals have been utilized as the contact layer in micro TE devices, there is no concise comparison between performances of different contact metals. The final conclusion about the best contact metal with lowest contact resistivity to Bi_2Te_3/Sb_2Te_3 thin films can only be made if all these metals are examined together under the same processing conditions. This investigation is the main focus of this chapter.

6.2. Contact Metal Shape

Actual contact resistance of an ohmic contact between a metal and a semiconductor always deviates considerably from its specific contact resistance. This deviation is mainly due to the current crowding effect along the edges of the metal contact. The field intensity along these edges is stronger than under the metal's inner part, which enhances the field emission of electrons [28].

One of the effective methods to reduce this effect is to increase the periphery of contacts, which leads to an increase in the ratio of effective contact area to total metal contact area. This behavior is easy to explain as the tendency of current crowding decreases with decreasing contact area, and saturates until a limited effective area is reached. In addition, if the contact area is reduced, the interface transition resistance and the series resistance will be reduced as well, leading to reductions in the effect of current crowding along the contact periphery. Given the limited area for contacts in micro devices, in order to increase the periphery of the contact, various metal contact shapes, such as rectangular with stripes (or fingers) and holes, as shown in Figure 6.1, are introduced. The narrower the strips and the more the number of holes become in the rectangular contact, the smaller the contact resistance achieved.

It is crucial to determine the optimal contact metal and shapes to achieve minimum contact resistivity. This chapter introduces novel material-shape combinations for minimization of electrical contact resistivity between Bi_2Te_3/Sb_2Te_3 thin films and various contact metals in micro-thermoelectric devices.

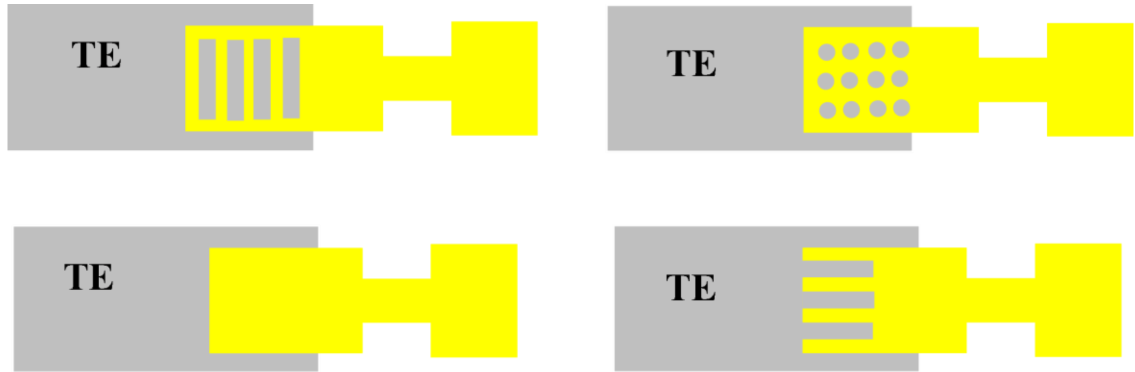


Figure 6.1 Various metal shapes to increase periphery of contacts.

6.3. Structures for Contact Resistivity Measurement

Contact resistance values were obtained using two different measurement techniques, which yielded similar results: the cross-bridge Kelvin resistor (CBKR), and the transmission line method (TLM).

It is desirable to measure metal-semiconductor contact resistivity by minimizing the contribution of these materials' bulk or sheet resistance. The four-terminal Kelvin test structure also known as the cross-bridge Kelvin resistance (CBKR) measurement technique meets this requirement [81]. In principle, this method allows the contact resistivity to be measured without being affected by the underlying semiconductor or the metal contact.

The basic structure of CBKR for metal-TE film is illustrated in Figure 6.2. Electric current is passed between contacts 1 and 2, and the voltage is measured between contacts 3 and 4. There are three voltage drops between contacts 1 and 2: the voltage between metal contact 1 and TE film, the voltage across TE film, and the voltage between TE film and contacts 2 and 3. A high input impedance voltmeter, for measuring the voltage V_{34}, allows very little current flow between contacts 3 and 4. Hence, V_{34} is solely due to the

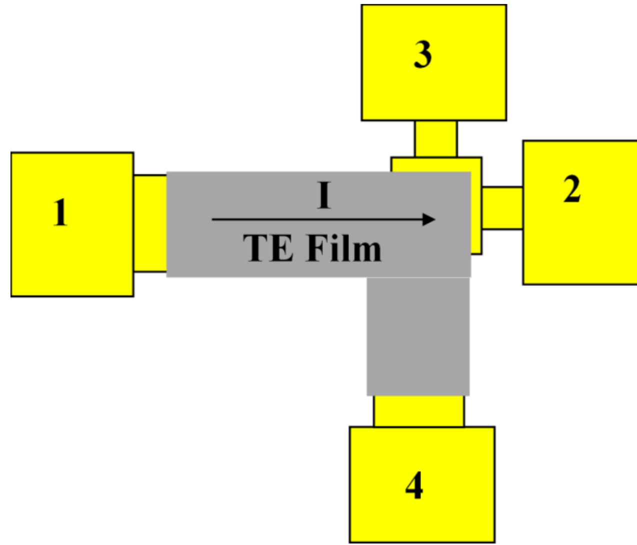


Figure 6.2 Cross-bridge Kelvin resistance (CBKR) measurement setup for metal-TE films contact resistance measurement.

voltage drop across the contact metal-TE film interface. Therefore, the contact resistance can be measured based on the following equation:

$$R_C = \frac{V_{34}}{I} \tag{6.1}$$

The metal-TE film contact resistance can also be evaluated using the transmission line method (TLM). The TLM test structure consists of a block of TE thin film and a series of metal contact pads with the same dimensions, spread at different intervals d_1, d_2, d_3, ...

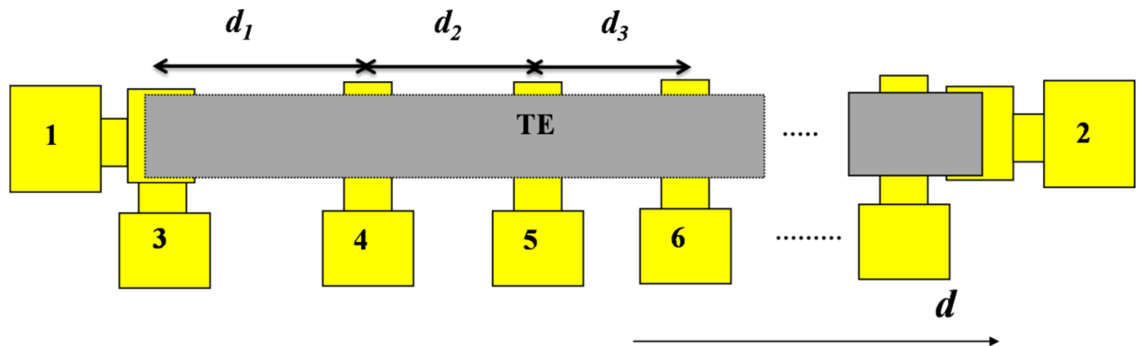


Figure 6.3 Transmission line method (TLM) measurement setup for metal-TE films contact resistance measurement.

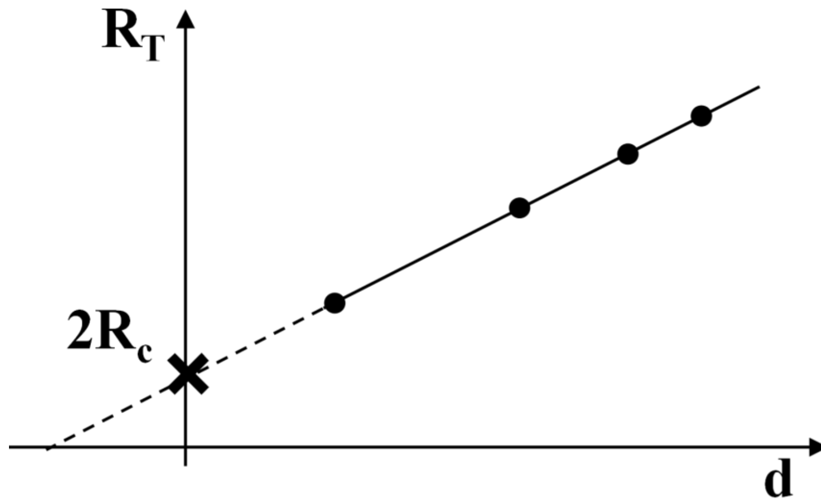


Figure 6.4 Linear extrapolation of R_T to derive R_c value.

and so on, as shown in Figure 6.3.

Electrical current is passed between contacts 1 and 2, and the voltage drop is measured between contact 3 and the consecutive contact pads (*V_{34}, V_{35}, V_{36}, ...)*. The total resistance at each of these intervals is calculated using the measured voltage and current values. Resistance is given by the following equation:

$$R_{Ti} = 2R_C + R_{TEi} \qquad R_{TEi} = \rho_{TE}\frac{d_i}{A} \ , \qquad (6.2)$$

where d_i is the distance between voltage measurement contacts. Linear extrapolation of R_T to the intercept (d=0) gives the approximate contact resistance value ($2R_c$), as shown in Figure 6.4.

6.4. Fabrication Process

This section presents the fabrication process of structures to investigate contact resistance for different metal types and contact shapes. An overview of the fabrication process is

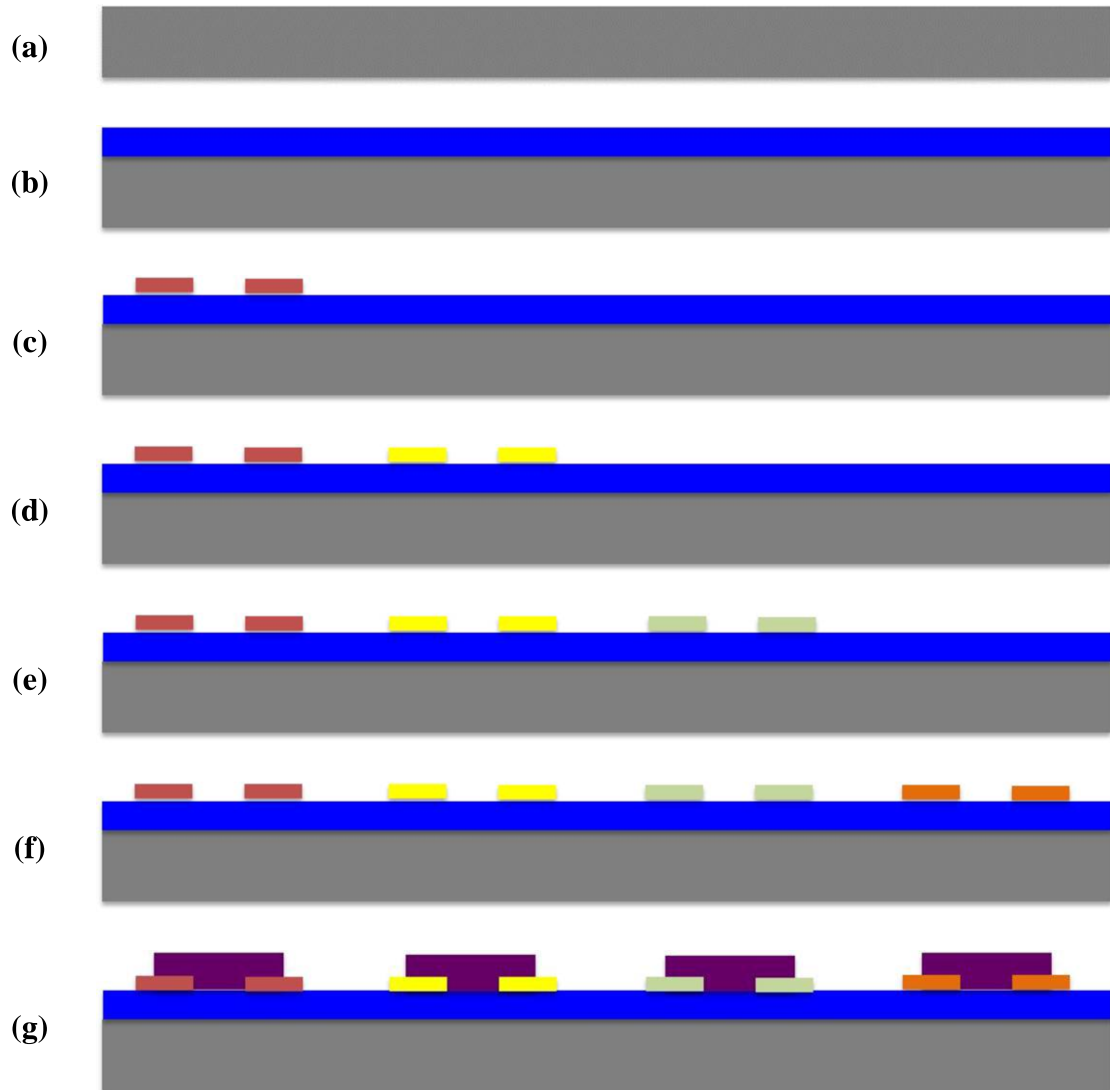


Figure 6.5 Process flow: (a) 500 µm thick silicon wafer (b) LPCVD oxide deposition (c) Deposition of 1st metal on oxide – lift-off process (d) Deposition of 2nd metal on oxide (e) Deposition of 3rd metal on oxide (f) Deposition of 4th metal on oxide (g) TE film deposition through shadow-mask

presented in Figure 6.5. All processing steps described in the following subsections are performed in the Lurie Nanofabrication Facility (LNF) at the University of Michigan. The fabrication process consists of three different masks, one used for the metal test structures, and two for processing of the shadow masks.

6.4.1. Test Structures Substrate

The test structures for metal-TE film contact resistivity characterization compare four different metals. The fabrication process consists of only one metal mask and four lithography steps. An LPCVD Silicon Dioxide layer with ~ 1 μm thickness is deposited on a Si wafer as an insulation layer (Figure 6.5(a)). Then the processing steps including lithography, metal evaporation, and lift-off are performed to define the test structures for each metal type. These three steps are repeated four times to complete the processing of the test structure wafer (Figure 6.5(b), (c), (d), and (e)). After the first metallization run, since there is only one metal mask, the wafer must be adjusted horizontally to match the alignment marks for adjacent metal patterns in each lithography step.

Several different metals, including Au, Pt, Ni, and Al have been deposited in this process and compared with each other. Thin layers of Cr or Ti were used as the metal adhesion layers under Au and Pt/Ni, respectively. Three novel contact structures, as shown in Figure 6.1, have been introduced in this work, in addition to the conventional solid metal shape.

6.4.2. Shadow Mask

Integrating TE thin films with the test structure wafers described in the previous section can be quite challenging due to several reasons. It is not possible to pattern TE thin films using lift-off or etching. Due to the high deposition temperatures of TE materials ($T_{sub} >$ 200 °C), photoresists cannot be used in the thermal evaporator. The photoresist required for lift-off will burn at such high temperatures, resulting in distorted patterns. Besides, the co-evaporation chamber will be contaminated with burnt photoresist residues. Etching TE thin film in order to create the patterns is also very difficult and almost impossible for small features. The TE thin film adhesion to the substrate is not strong enough to survive

the etching process and results in film delamination. The wet etching process of Bi_2Te_3/ Sb_2Te_3 materials has been examined using aqua regia (nitric acid and hydrochloric acid with the ratio of 1:3) solution with photoresist as the etching mask. The results show that the wet etch process is very isotropic and creates a considerable undercut. Even if the TE film does not peel off from the substrate during the etching process, it usually results in a very rough TE film surface. Therefore, TE film etching is not suitable to pattern micro-scale features in the test structure.

To address these issues, shadow-masks are fabricated and utilized to pattern TE thin films. The shadow-mask fabrication is a two-mask process on a silicon wafer. First a photo mask is used to pattern wide cavities on the backside of the wafer. The cavities on the back of the Si wafer are etched to a depth of about 350 μm using Deep Reactive-Ion Etching (DRIE) tool. The second photo mask, which is the desired pattern of TE film on the test structures, is used for the lithography of the wafer's front side. Subsequently, TE film patterns are etched through to the cavities to make through-wafer holes [42]. Deep cavities are created on the backside of the Si wafer, surrounding the TE film patterns, in order to reduce the interference of the shadow-mask with the TE material during co-evaporation, especially since the material sources are not located directly below the center of the wafer.

The shadow-mask and the test structure wafers are aligned manually using alignment marks. There are four holes machined both in the shadow-mask and processed wafer, which must overlap when the wafers are aligned. These two wafers are then attached to each other by inserting a stainless steel machine screw bolt and nut into the holes.

After the shadow mask for TE film pattern is aligned and fixed to the test structure wafer,

they are loaded in the thermal evaporator. Then Bi_2Te_3 or Sb_2Te_3 thin films are deposited at their optimal co-evaporation condition on the processed wafer through the shadow mask. When the TE film co-evaporation process is completed, the wafer must be allowed to stay in the processing chamber until it cools down to room temperature. It is necessary to wait before unloading the wafer to avoid thermal shock stress in the TE thin film. Then the wafer is transferred from the deposition chamber to the load lock, unloaded and prepared for contact resistivity characterization.

6.5. Results and Analysis

The top view of the completed contact resistivity characterization wafer is shown in Figure 6.6. The structures for two different contact resistivity measurement methods, for

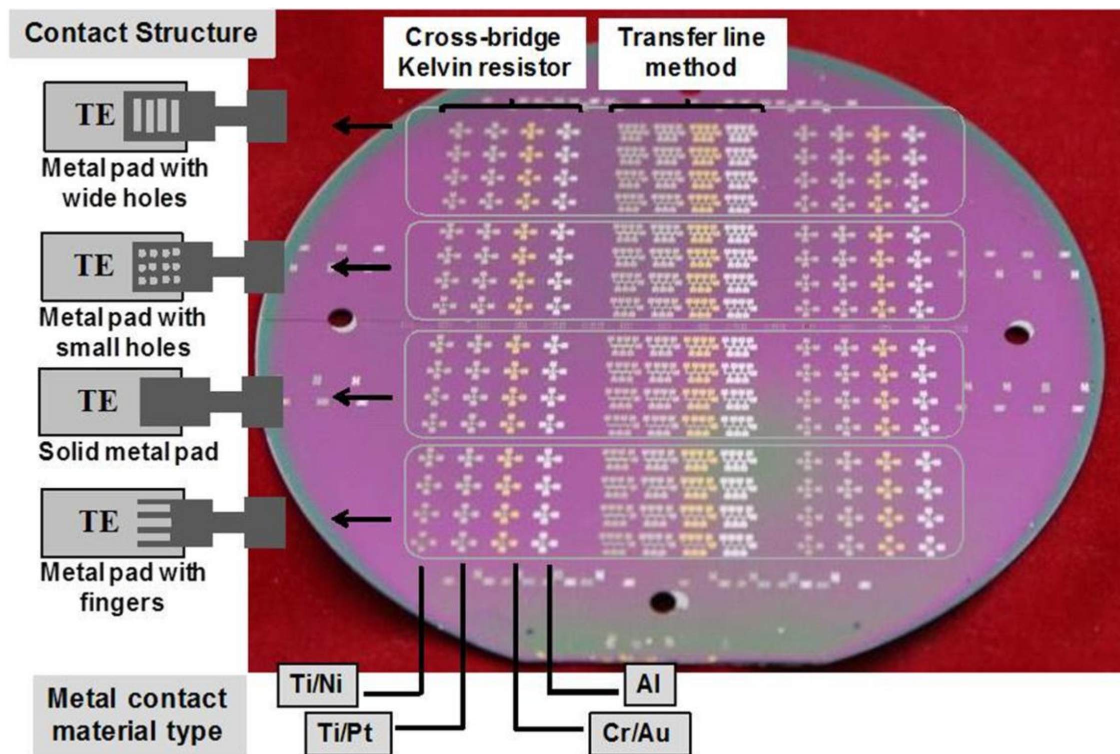
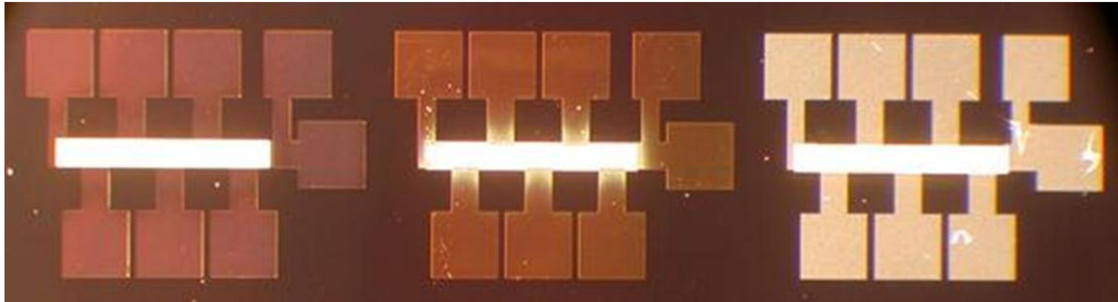
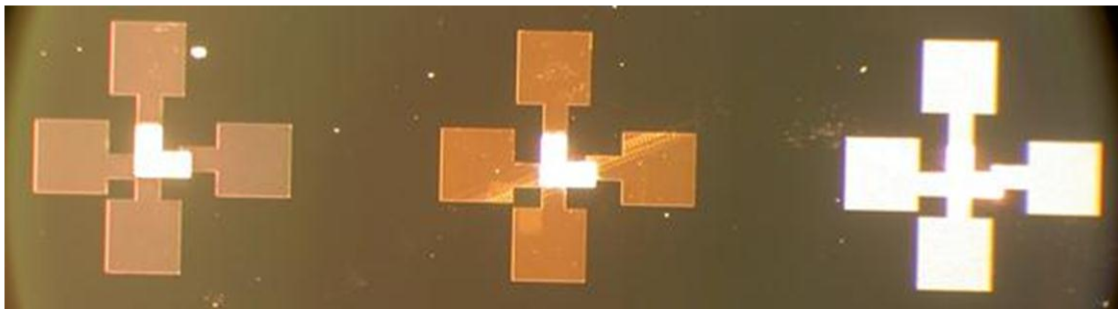


Figure 6.6 View of a processed wafer used for metal-TE contact resistivity charaterization.



(a)



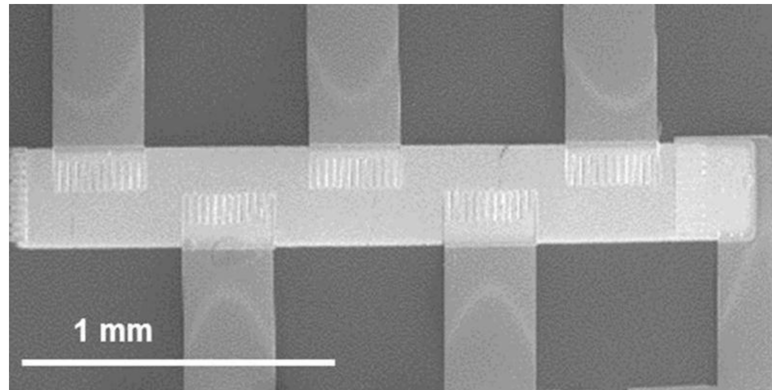
(b)

Figure 6.7 Structures for two different methods of contact resistance measurement: (a) TLM and (b) CBKR. Three different metal types are shown (from left to right: Ni, Au, Pt).

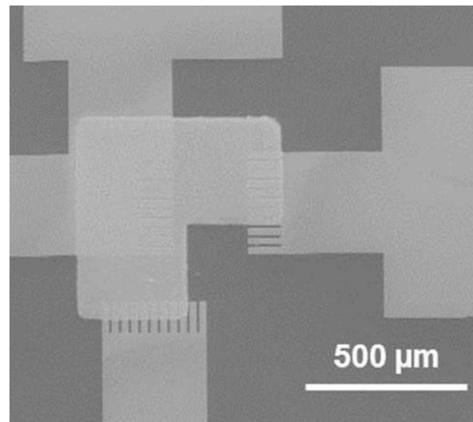
four different metal combinations, and four metal contact structures are highlighted in the figure. Figure 6.7 further illustrates structures for two measurement methods on three different metals, namely Ni, Au, and Pt.

Figure 6.8 (a) shows the top surface SEM image of a TE film on metal contacts with fingers for the TLM method. Figure 6.8(b), shows a CBKR-method device. Here, the contact structure is more visible due to a minor misalignment of the shadow mask and the processed wafer, which lead to a misalignment between TE thin film and the metal contacts in some devices. The cross-sectional SEM image of contact resistance test structure in Figure 6.8(c) shows silicon dioxide, metal, and TE thin film layers for Cr/Au metal contact.

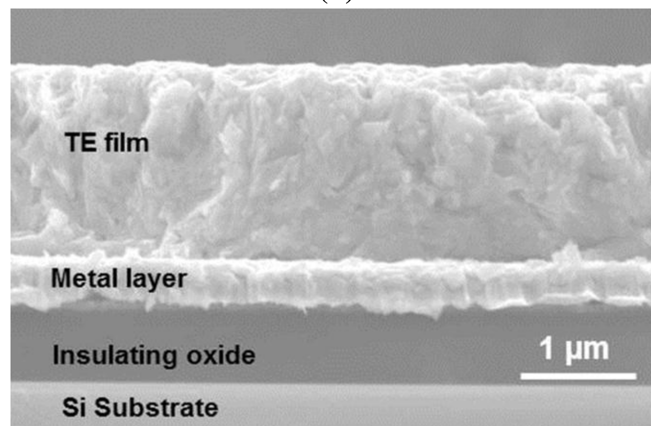
Measurements are taken at several different current levels and the average values of the



(a)



(b)



(c)

Figure 6.8 (a) Top surface SEM image of the TE film over metal contact pads with fingers in TLM method. (b) Misalignment in CBKR method shows the contact shape clearly. (c) Cross-section of Cr/Au metal-TE film contact.

two methods are shown in Figure 6.9. The results show that increasing the contact region periphery (*e.g.*, with fingers and holes) reduces resistivity. However, the choice of metal is the dominant factor in determining contact resistivity. Adhesion between Al metal and

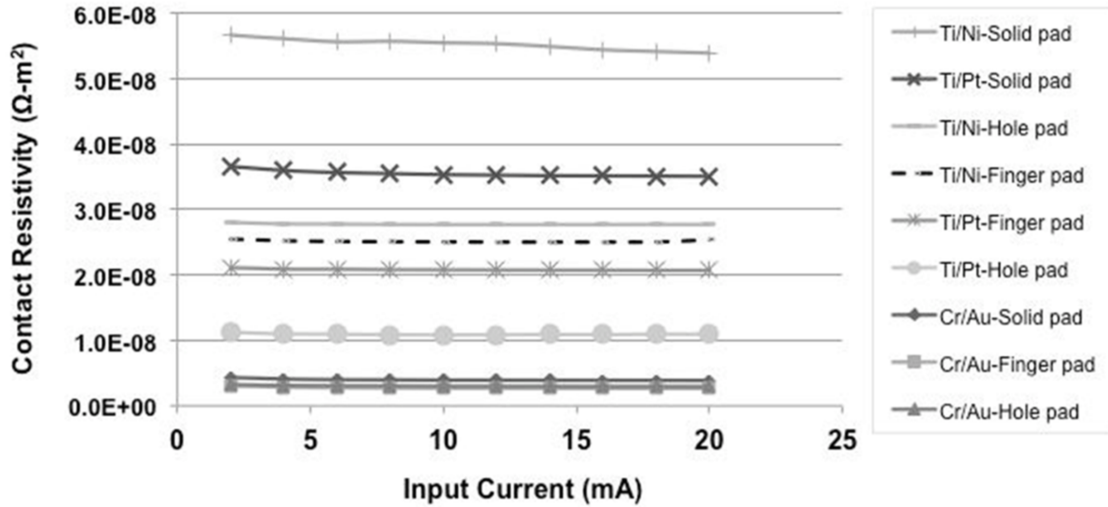


Figure 6.9 Comparison of metal/TE film contact resistivity for different metal types and contact structures. Cr/Au metal layers have the lowest contact resistance, and structures with longer contact edges (i.e. pads with finger and holes) result in lower resistivity than contacts with solid pads.

TE film was quite poor, resulting in very high contact resistivity. Cr/Au metal contacts with fingers and holes resulted in the lowest R_c values of ~ 3×10^{-9} $\Omega\cdot m^2$. These values are lower than those previously reported [14,30,43], and are very close to the optimal requirements of thermoelectric devices. It is important to note that these values have been achieved without any special surface processing or post-deposition annealing. In this work, since TE thin film deposition is the final step of the process, it is likely that a thin oxide/contamination layer on the Ni metal film leads to high resistivity values, which, necessitates *in situ* cleaning of the metal surface before TE deposition to reduce contact resistance.

The new thermal evaporation system at the University of Michigan has the capability of *in situ* RF plasma etching. The *in situ* cleaning of Ni metal before Bi_2Te_3 TE film deposition results in the reduction of contact resistivity. The initial contact resistivity measurement of Ni contact with solid shape shows performance improvement from ~

5.5×10^{-8} $\Omega\cdot m^2$ to ~ 7×10^{-9} $\Omega\cdot m^2$. Electrical contact resistance is reduced after performing *in situ* surface cleaning, which removes hydrocarbon and oxide contaminants a in high vacuum chamber.

In addition, formation of a favorable intermetallic phase at the interface is found to contribute to lower contact resistance. The extended heat treatment allows for a more complete interfacial reaction to form nickel telluride, resulting in better electrical properties. The extensive diffusion causes a reduction in the effective thickness of the substrate, which improves electrical conductivity since nickel telluride is more conductive than bismuth telluride. There would however be a negative impact to thermal conductivity since the presence of the intermetallic compound reduces the effectiveness of the thermoelectric material for maintaining a temperature difference between the cold and hot sides [54].

6.6. Summary

One of the main challenges in thermoelectric thin film microsystems compared to bulk material devices is the increasing adverse effect of contact resistance. It increases the total electrical resistance of the device and degrades the efficiency. In this chapter test structures with novel material-shape combinations are introduced and fabricated for minimization of electrical contact resistivity between (Bi,Sb)Te-based TE thin film and metal contacts. The lowest contact resistance value, R_c ~ 3×10^{-9} $\Omega\cdot m^2$, is achieved by Cr/Au contact with finger and/or holes structure and satisfies the requirement for many micro-scale thermoelectric devices. The *in situ* RF plasma cleaning of Ni contact before TE material deposition is shown to reduce the value of contact resistivity.

Chapter 7
Conclusion and Future Directions

While there has been much recent work on thin film deposition of (Bi,Sb)Te-based thermoelectric materials, few efforts have resulted in effective demonstration of these films in microsystems. Most of the existing work has focused on basic process characterization or on increasing the thermoelectric figure-of-merit. However, there are many fundamental challenges in thermoelectric thin film development and integration, which need to be addressed for these films to become practically useful. This dissertation seeks to address these needs in a comprehensive way by demonstrating thermal co-evaporation as a low-cost, high-throughput, CMOS-compatible method to develop high quality binary (Bi,Sb)Te-based thin films on various substrates. In addition, deposition of advanced thermoelectric thin films, such as ternary $(BiSb)_2Te_3$ alloys, by thermal co-evaporation has been proposed and investigated for the first time.

While integrating TE thin films in microsystems, the contact resistance between TE material and metal contacts become comparable with the electrical resistivity of TE film and it degrades device performance. Therefore, characterization and minimization of metal-TE film electrical contact resistance becomes a very important step in developing TE micro-scale devices. The specific contributions of this work are:

- Co-evaporation of Bi_2Te_3 and Sb_2Te_3 materials are characterized and optimized

on different substrates. The effect of substrate material and deposition conditions on binary TE film morphology, composition, and transport properties are investigated.

- Several challenges for Sb_2Te_3 thin film deposition, such as high stress and poor adhesion, have been addressed. Possible solutions to enhance characteristics of Sb_2Te_3 films have been introduced and studied.
- Telluride-based ternary films have been developed and characterized for the first time using the co-evaporation technique.
- Design and fabrication of test structures to study and minimize the metal-TE film contact resistance are presented. Novel material-shape combinations for the metal contacts are investigated in order to determine the best choice for TE microsystem applications.

Characteristics and TE properties of binary (Bi,Sb)Te-based TE films are optimized on several different substrates. Maximum achieved power factors for *n*-type Bi_2Te_3 films are 3.08 and 3.12 mW/K2m on poly-Si and Kapton® substrates at T_{sub}= 270 °C, respectively. For *p*-type Sb_2Te_3 films, optimum power factors are 1.17 and 1.12 mW/K^2m on oxide and poly-Si substrates at T_{sub}= 250 °C, respectively. Optimum (Bi,Sb)Te-based binary films have tellurium atomic percentage of about 60%.

The performance of $(BiSb)_2Te_3$ ternary thin films developed by thermal co-evaporation is comparably inferior to the reported figure-of-merit values for ternary thin films prepared by other techniques. The maximum power factor obtained for $(BiSb)_2Te_3$ films is 0.26 mW/K^2m on glass substrate at T_{sub}=160°C with Seebeck coefficient of 140 μV/K, and electrical resistivity of 74.4 μΩ-m. However, since thermal evaporation is a low-cost and simple deposition technique, further study on the optimization of co-evaporated

(Bi,Sb)Te-based ternary alloys can contribute greatly to thermoelectric thin film applications in microsystems.

The lowest contact resistance value, $R_c \sim 3 \times 10\text{-}9\ \Omega \bullet m^2$, is achieved by Cr/Au contact with finger and/or holes structure. This low contact resistance satisfies the requirement for many micro-scale thermoelectric devices and is particularly important as it has been achieved without any special surface processing or post-deposition annealing

7.1. Future Directions

The most important challenge to fabricate novel thermoelectric micro-scale devices is reliable deposition of high quality thermoelectric materials on a variety of substrates. Further research is necessary to optimize the co-evaporation conditions for binary and especially ternary (Bi,Sb)Te-based TE film for specific device structure. Since the grain size of ternary thin film is smaller than that of binary TE films, the effect of post-deposition annealing to improve the power factor of $(BiSb)_2Te_3$ should be investigated.

Moreover, the thermal co-evaporation of *n*-type $Bi_2(SeTe)_3$ ternary and quaternary thin films need to be explored due to their superior thermoelectric performance. Selenium (Se) has a lower melting point than the Bi, Sb and Te and optimizing the substrate temperature to avoid re-evaporation of Se may be a challenge. The use of *in situ* RF power during deposition to promote good structural film quality, and/or post-deposition annealing, possibly in a Se-rich or Te-rich environment created in the process chamber can be explored.

Apendix A Design and Fabrication of a Thermoelectric Energy Scavenger for Powering Hybrid Insects

A.1. Introduction

There has been a growing interest in technologies involving implantation of micro-devices inside an insect's body to control its locomotion. These hybrid insects are essentially human-controllable robots that use live insect's muscle actuators for movement. They can be used for various behavioral studies on insects such as communication, mating and flight energetics as well as physical access to locations not easily accessible to humans or terrestrial robots. The implantation on these insects is done at an early stage of their life, such as the caterpillar or pupa stage. The tissue development in later stages of the insect's life heals the area around the micro-device and forms a stable and reliable tissue-machine interface.

However, power provisioning for flight control and remote sensing micro-systems on these hybrid insects is one of the most challenging development issues. For example, the average power consumption of the microcontroller, used in [78] to drive both neural and visual stimulators, is about 250 μW. Using batteries for this purpose has a number of limitations, such as relatively large size, heavy weight, and limited lifetime. Experiments in [79] and [80] show lifetimes of up to 60 minutes with batteries weighing 350 mg on

large Mecynorrhina torquata beetles weighing about 8 grams. Clearly this lifetime will not be sufficient for many applications. Furthermore, considering that these beetles can usually fly with an additional load of only 20-30% of body weight and that the main circuitry could weigh in the order of 1-2 gram, there will also be a limitation on the weight and capacity of the utilized battery. In addition, due to the lack of easy access to the hybrid insect after deployment, batteries cannot be replaced or recharged in the field.

In general, growth of micro-scale implantable electronic systems has increased the demand for on-site, small volume, and replacement-free energy sources as an alternative to conventional electrochemical batteries. On-site energy scavenging techniques from various environmental sources including ambient heat, solar energy, and vibrations have been introduced as efficient and promising approaches. Likewise, the idea of harvesting electrical energy from beetles' body sources, thermal and mechanical activities, and their surroundings (e.g. solar) has drawn significant attention and several energy harvesting methods have been proposed to replace batteries in hybrid insects [1,32].

Among various energy scavenging techniques, micro thermoelectric generators (micro-TEGs), which convert waste heat to electrical energy, are becoming more popular. The operation of TEGs is based on the Seebeck effect, which converts temperature difference directly into electric potential difference. This thermoelectric (TE) voltage is generated when there is a temperature difference across the junction of two different metals or semiconductors. Despite the high cost and low efficiency of TEGs, their reliability due to the absence of moving parts and their silent operation makes them the platform of choice in many energy scavenger systems.

The focus of this work is to investigate the feasibility of using the body heat generated by

beetles as an energy source, even in the absence of light and vibration. Specific design and characteristics of an implantable TEG are studied to facilitate its functionality and implantation in beetles. Several approaches to build both lateral and vertical micro-TEGs by micromachining TE materials have been developed in the past [3,13,38,73,86,94]. The performance of these devices depend both on their structure and TE material figure-of-merit, *ZT*, a unit-less value defined as $ZT = \alpha_s^2 T/\rho\kappa$, where α_s is the Seebeck coefficient (μV/K), ρ is the electrical resistivity (μΩ·m), sκ is the thermal conductivity (mW/m·K), and T is the absolute temperature (in Kelvin). These generators mainly utilize bulk and thin film BiTe-based alloys, which are known to be the best TE materials around room temperature with high ZT values, due to their high Seebeck coefficient, low electrical resistivity and relatively low thermal conductivity. Although thin films have been shown to be the best option for micro-systems, they still have fairly low figures of merit compared to bulk BiTe-based TE materials. Furthermore, the maximum thin film thickness prepared by evaporation or sputtering is limited to about 4 μm, which is not optimal for many micro-TEG designs. To overcome these drawbacks we employed bulk TE material wafers with higher figure of merit and thickness of about 200 μm in the generator fabrication. Specifically, the contributions of this work are as follows:

- Design and fabrication of a TE energy scavenging micro-system that is capable of using an insect's body as the heat source.
- Use of flexible materials, which greatly simplifies implantation on the insect and enables successful bonding between the insect's body tissues and the device.
- Several considerations in the physical design of the device to minimize its thermal conductivity and maintain the temperature difference between the two sides of the

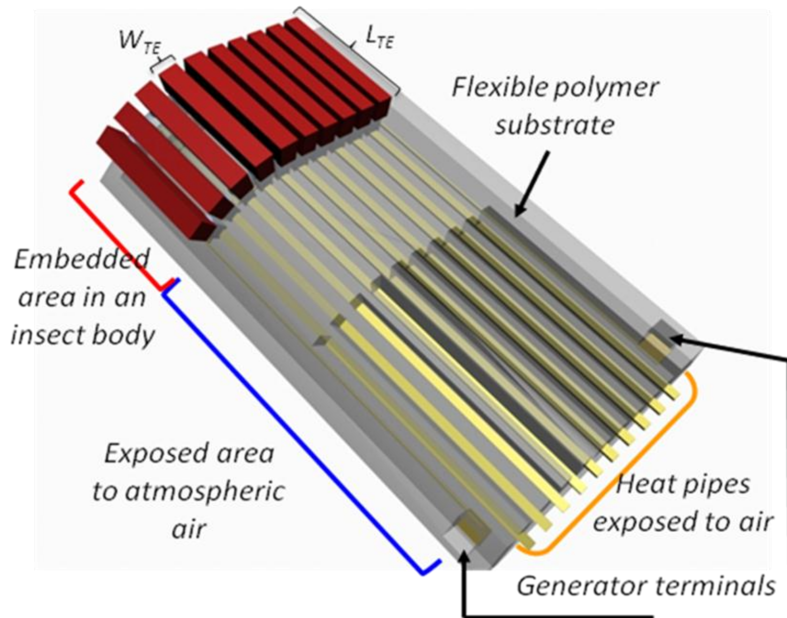


Figure A.1 3-D illustration of an implantable micro-TEG. L_{TE} and W_{TE} are the length and width of the TE legs, respectively.

thermocouple.

A.2. Design Process of an Implantable Micro-TEG

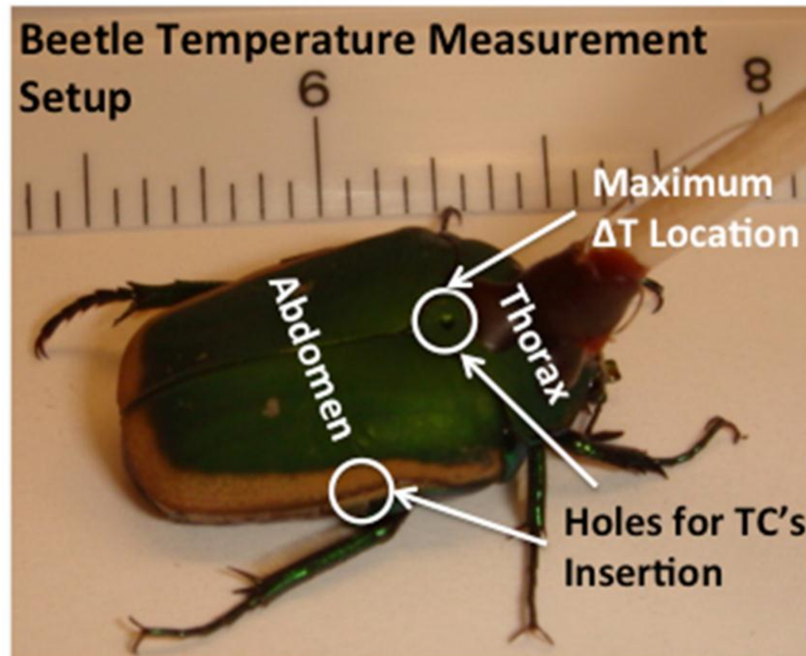
Design decisions were made after close examination of various characteristics of beetles including body temperature changes, body volume, implantation stability and fabrication limits of bulk TE materials. Figure A.1 shows a 3-D illustration of the designed micro-TEG. It consists of multiple TE legs made of Bi_2Te_3/Sb_2Te_3 alloy bulk material, with high TE figure of merit, which are connected thermally in parallel and electrically in series and are laid on a thin polymer substrate. The low thermal conductivity of the substrate material and the integrated cavities underneath the TE legs increase the thermal isolation between hot and cold sides through the substrate. Metal lines embedded in the polymer substrate connect the TE material legs and function as the other element of the thermocouple. The TE legs and metal lines are separated by a polymer layer and in order

to electrically connect them at the hot and cold junctions, holes are fabricated in the polymer and then filled with conductive epoxy. Metal heat pipes are extended from the cold junctions all the way to the air-exposed area. These pipes are designed to keep the cold side of the micro-TEG at ambient, maintaining the temperature difference between the two ends of the TE leg. Resistive temperature sensors are integrated in the device substrate to measure the hot and cold junction temperatures. An important feature of this micro-TEG is the flexibility of its polymer substrate. This allows the beetle's tissue to grow around the device after implantation at the pupa state.

A.2.1. Beetles as the TEG Heat Source

A beetle's body temperature can rise several degrees during the course of its flight [67]. Temperature distributions over several locations on beetles' bodies were measured to locate the optimal implantation position for the micro-TEG. Body-temperature measurements were made in the dorsal thoracic muscles and the ventral abdomen area by inserting a J type thermocouple (iron - copper) with wire diameter of 76 µm and 0.4% error limit. In both cases a small hole, about 0.5 mm in diameter, was carefully made in the cuticle with a needle and the thermocouple junction was inserted to a depth of about 3 mm and sealed in place with epoxy. The beetles were not anaesthetized during the insertion process, but a stick was attached to their back with glue to hold them in place. The whole process of making holes and inserting the thermocouples did not seem to have any adverse effect on the beetles' life. For the beetles tested here, their life span was not affected by the piercing procedure.

Ambient temperature, measured immediately before the experiments, was between 21-22°C. After the insertion of thermocouples the beetle's body temperature rose about 5-



Location	Number of beetles	Ambient Temperature (°C)	Maximum T_{body} during Flight (°C)
Dorsal Thorax	8	22	33
Abdomen	8	22	28

Figure A.2 Beetle's body temperature measurement setup. The inset table shows the measurement results.

6°C and then dropped slowly back to the original temperature. This initial rise of temperature in beetles might be due to heat the organs produce to control their body temperature while encountering an external object. During flight, the abdomen and dorsal thorax muscle temperatures reached 28°C and 33°C, respectively. Most beetles did not fly continuously for a long time. However for those that did fly for a longer period, body temperature increased at the beginning of flight and then remained constant. As shown in Figure A.2, the maximum body-ambient temperature difference was about 11°C, measured on the back of the beetles close to the wing base.

After studying the beetle body temperature rise during flight and determining the position for maximum body-ambient temperature, additional experiments were required to assess

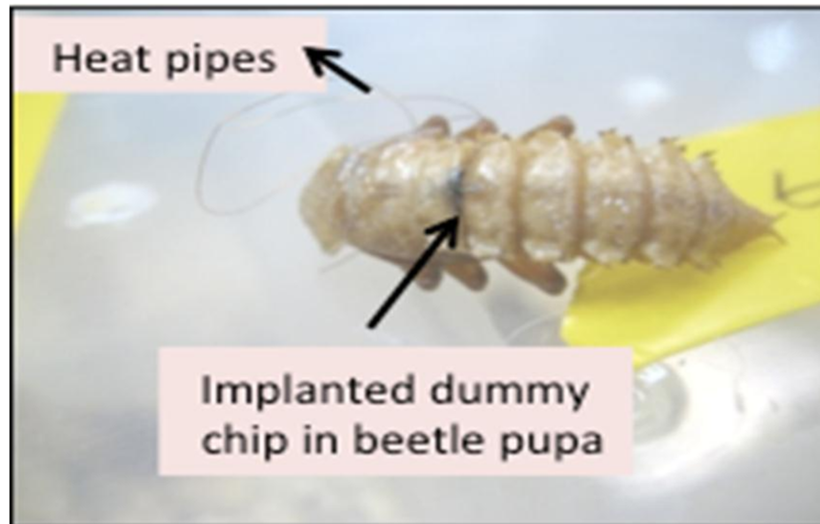
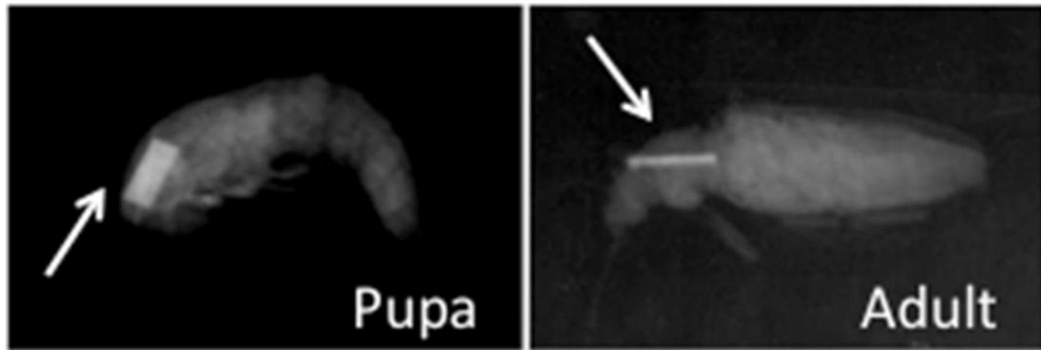


Figure A.3 Implanted dummy chip inside beetle pupa body.

the possibility of implanting micro-devices inside the beetle body. Various silicon and glass chips were implanted inside the beetles' bodies during the pupa stage to study developmental stability as well as optimal placement and size of the generator device.

The following process was used to fabricate the implantable dummy chips: First a thin layer of gold was deposited on 500 μm thick glass and Silicon wafers. Then the wafers were insulated with Parylene and diced into chips with footprints of 4×1 mm^2 and 4×2 mm^2. Finally, several metal wires were connected to the chips using a wire-bonder. These wires represent the heat pipes which were later fabricated in the actual generator device. The chips were carefully implanted in the dorsal and ventral abdomen/thorax area of the pupas, while the attached metal wires were extended out of their bodies (Figure A.3). The survival rate of the pupas with chips implanted in their back was about 80%, while placing the chips in the ventral abdomen resulted in body malformation and serious defects. Figure A.4 shows X-ray images of the implanted chips at both pupa and adult life stages along with a summary of pupas' survival rate the dummy chip implant location.



Implanted chip type	Location	Number of pupas	Survival rate
Si/Glass chip	Dorsal	5	80
	Ventral	5	40

Figure A.4 X-ray images of silicon/glass chips implant in beetle pupa and adult, summary of implant survival % based on the location.

A.2.2. Analytical Modeling

The micro-TEG design can be optimized for maximum power by modeling device parameters (Figure A.5). The Seebeck effect [76] governs the operation of TEGs for converting waste heat to electrical energy. Equations (A.1) and (A.2) show the

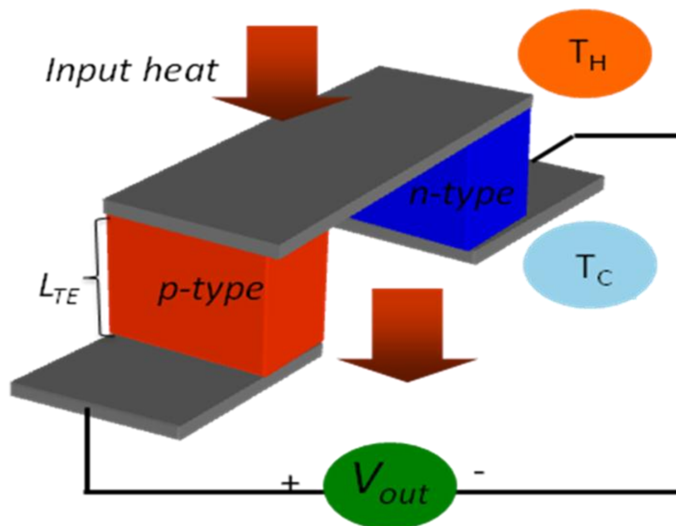


Figure A.5 Schematic of a simple thermoelectric generator. L_{TE} is the length of the TE legs.

dependence of the generated open-circuit voltage and power on the Seebeck coefficient difference of the *p/n* type TE materials (α_p - α_n), the temperature difference between hot and cold junctions (T_h - T_c), the number of thermocouples (n) and the generator's internal electrical resistance (R_g) for a simple TEG structure. The maximum output power is achieved when the load resistance connected to the generator equals the generator internal electrical resistance.

$$V_{out}=n(\alpha_p-\alpha_n)(T_h-T_c) \quad \textbf{(A.1)}$$

$$P_{out}=n^2(\alpha_p-\alpha_n)^2(T_h-T_c)^2/4R_G$$ $$P_{out} = n^2(\alpha_p-\alpha_n)^2(T_h-T_c)^2/4R_g$$ **(A.2)**

The temperature difference (T_h - T_c) depends on the internal thermal conductance of the generator device and the heat input to the system. Analysis of the optimal output power dependence on the design parameters and material properties has been performed. The proposed micro-TEG is fabricated on a polymer substrate with integrated air cavities underneath the TE elements to reduce thermal loss through the supporting substrate material.

A thermal network model is developed in MATLAB considering Peltier cooling/heating, Joule heating, contact resistances and thermal conduction through TE legs, metal lines, polymer substrate, and air cavities.

To achieve maximum output power, the optimization parameters are: (1) TE leg dimension aspect ratios, (2) thermal conduction through the substrate, and (3) the number of TE elements in the micro-TEG area. However, the bulk TE material mechanical properties, beetle body size and implantation experiment results enforce limitations on the number of TE elements and their dimensions in the optimization process.

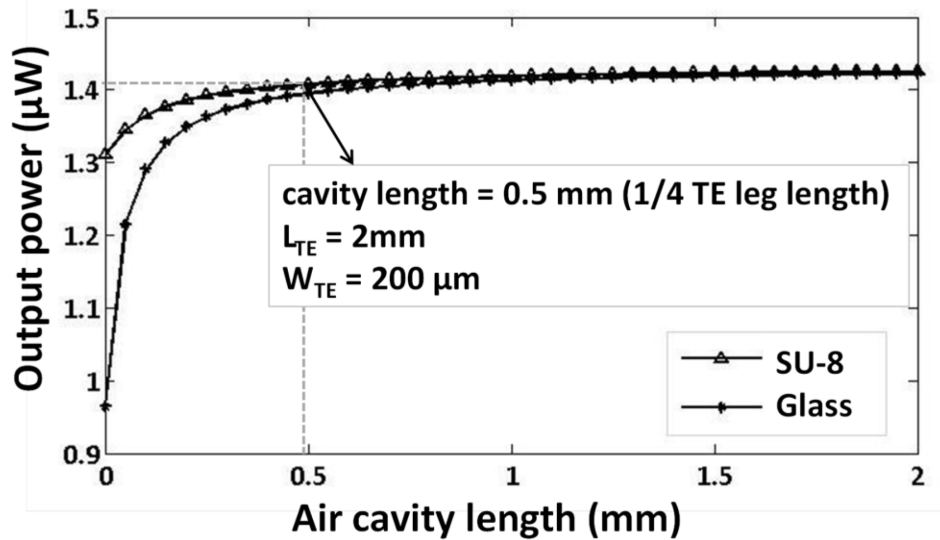


Figure A.6 Predicted effect of the substrate material and air cavity length on the micro-TEG output power. L_{TE} and W_{TE} are the length and width of the TE legs, respectively.

Figure A.6 shows the effect of the substrate material and the length of integrated air cavities below the TE elements on the optimal output power. As can be seen, lower thermal conductance of SU-8 polymer compared to glass makes it a better choice to use for the device substrate. The effect of cavity length is more pronounced on the glass substrate. With a TE leg length of 2 mm in this design, reducing the cavity length below 0.5 mm has an adverse effect on the generator output power.

Figure A.7 shows the influence of TE leg dimensions on the generator performance. According to this model, increasing the length and decreasing the width of the TE legs result in higher micro-TEG output power. However, due to dicing constraints of the bulk TE material, it is very difficult to fabricate very long and narrow TE legs. Therefore, the width and length of the TE legs are limited to 200 μm and 2 mm, respectively. Furthermore, the maximum area of the implantable dummy chips inside beetle pupas is 4×2 mm^2. As a result, despite the fact that increasing the number of TE elements results

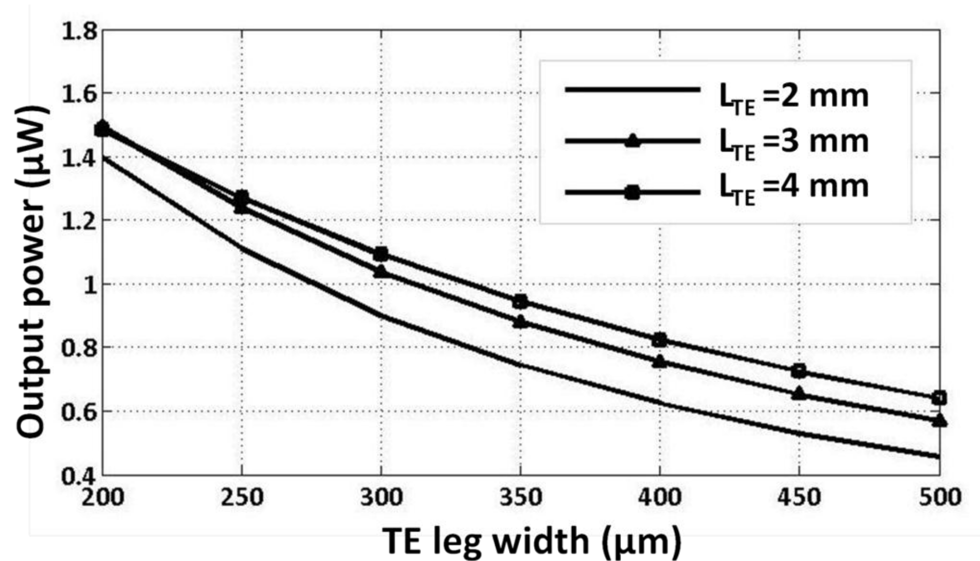


Figure A.7 Predicted effect of TE leg dimensions – length (L_{TE}) and width (W_{TE}) – on micro-TEG power generation.

in higher output voltage and power, a micro-TEG design with the maximum chip dimensions can only include 16 TE legs.

A.3. Material Properties

Several different materials are used in the proposed generator design. Electrical, thermal and mechanical properties of these materials need to be determined in order to model and optimize the micro-TEG device. Table A.1 summarizes these characteristics.

Material Properties	Ref.	Seebeck (µV/K)	Resistivity (µΩ·m)	Thermal Conductivity (W/m·K)
Bulk n-type $(Bi_2Te_3)_{90}(Bi_2Se_3)_{10}$	[93]	-202	10.5	1.3
Bulk p-type $(Bi_2Te_3)_{25}(Sb_2Te_3)_{75}$	[93]	214	11.5	1.3
Au	[62]	1.79	2.44×10^{-2}	318
SU-8	this work	N/A	N/A	0.26
Air	[62]	N/A	N/A	0.025

Table A.1 Properties of the materials used in the proposed micro-TEG design

The properties of Cr/Au metal layer have been characterized thoroughly before [14]. Some of the properties of the SU-8 polymer have also been reported previously [15]. The most important property of this material, needed for the generator device modeling, is its thermal conductivity. Thermal conductivity of the SU-8 layer has been measured using a setup similar to [37]. In the proposed measurement setup, a sample composed of the SU-8 layer on top of a Si support substrate is mounted between a heat sink and an integrated micro-heater. Thermal resistance is calculated by dividing the measured heater power and the temperature difference across the SU-8 sample after reaching thermal equilibrium. The parasitic thermal resistance from the setup substrate is eliminated using a differential measurement method. SU-8 samples with various thicknesses are deposited on the Si substrate. Assuming all measurement parameters except the SU-8 layer thickness are constant, thermal resistance of the SU-8 can be calculated with high accuracy. The measurement results show a thermal conductivity of 0.26 W/m·K for SU-8, which is close to the values reported for this polymer in [100].

Figure of merit, *ZT*, defines the TE material's ability to efficiently generate electrical energy and is dependent on the material's Seebeck coefficient, electrical resistivity and thermal conductivity. Thin film TE materials can provide significant advantages in size, cost, flexibility and circuit integration of micro-scale TE devices. However, there have been several issues with thin films' reliable integration on micro-devices and with their performance compared to bulk TE materials [18,20]. For this design, bulk n and p-type TE material were provided by Marlow Industries Inc. [37] in the form of 200 μm thick and 1-inch diameter wafers. Bulk BiTe-based alloys are known to be the best TE

materials around room temperature and have *ZT* of about 0.85 [101].

A.4. Technology and Fabrication

Figure A.8 illustrates the fabrication process flow of a flexible micro-TEG. This process involves three photolithography steps, followed by the attachment of a bulk Bi_2Te_3/Sb_2Te_3 piece to the polymer substrate and elimination of the excess TE material with a dicing saw to create individual TE legs.

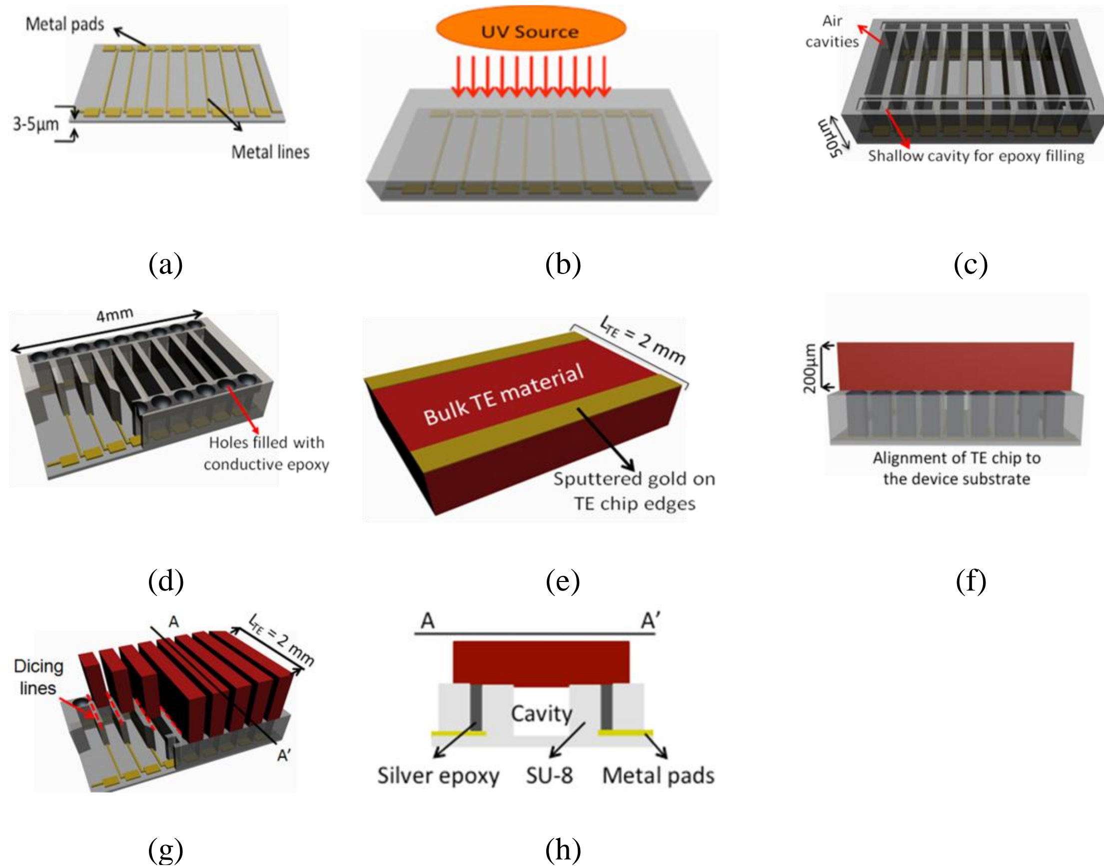


Figure A.8 Fabrication process flow of the micro-TEG: (a) Patterned metal on thin SU-8 layer on a supporting Si substrate (not shown); (b) Lithography process on the thick SU-8 layer; (c) 50-µm patterned SU-8 layer including holes and cavities; (d) Filling the holes with conductive epoxy; (e) Sputtering a thin layer of gold on the edges of TE material piece; (f) TE piece alignment and attachment to the substrate; (g) Dicing of the attached TE material piece to form TE legs; (h) Cross section of a TE leg over a cavity. The device is completed by releasing the structure from the supporting Si substrate.

First, a 200 Å thick Ti sacrificial layer is deposited on a 4-inch Si wafer. This Si wafer is used as the carrier wafer for the following fabrication steps and will be released at the end of processing. Subsequently, a 5-µm polymer layer (SU-8 10) is spun, prebaked, exposed, post-baked and developed to form the platform for metal patterns. A 1000 Å layer of Cr/Au metal is then deposited on the thin SU-8 layer in a thermal evaporator. Metal contact pads, lines, heat pipes and resistor temperature sensors are patterned after the first lithography step and etching the excess Cr/Au layer on top of the thin polymer (Figure A.8(a)). Next, a 50 µm thick SU-8 2025 is spun on.

After prebaking, a second lithography step is performed to create through-holes and cavities in the SU-8 mold. The through-holes are aligned to the underlying gold metal pads. Cavities with a length of about 1 mm are designed and fabricated below each TE leg in the SU-8 mold to decrease the thermal conduction through the substrate (Figure A.8(c)). After post-baking and developing of the 50 µm SU-8 layer, the holes and cavities appear in the device substrate. In order to make sure that SU-8 mechanical properties do not change during later thermal processing steps, the wafer is baked at about 150ºC for 5 minutes. Next, the holes in the SU-8 mold are filled with conductive epoxy, providing electrical connections between the bulk TE material and the contact pads (Figure A.8(d)). This step is performed by wetting a tiny needle with conductive epoxy and filling the holes carefully under a microscope. Since these holes are quite small and filling is performed manually, there is a possibility of electrical shorts between adjacent metal pads or TE legs due to the conductive epoxy overflow. To address this issue, a very shallow cavity is fabricated around the through-holes. This prevents the epoxy spreading to other parts of the device, except for the area around the holes.

Excessive conductive epoxy between adjacent through-holes is removed later in the dicing step.

Subsequently, a 2×4 mm^2 piece of TE material is carefully aligned and attached to the polymer substrate (Figure A.8(f)) and the whole wafer is baked at 150ºC in vacuum for an hour to cure the conductive epoxy. One of the major concerns in this process is the high contact resistance between the conductive epoxy and TE material pieces. To reduce the contact resistivity and create a metallic contact, TE pieces are masked with Aluminum foil strips and then a very thin layer of gold is sputtered on their edges before attachment to the substrate (Figure A.8(e)). The thin layer of sputtered gold reduces the contact resistance between the TE material and conductive epoxy significantly. After curing the epoxy, a dicing saw is used to create individual TE elements. The bonding between TE material and conductive epoxy is very strong and is capable of holding TE legs in place during the dicing process (Figure A.8(g)). Bulk Bi_2Te_3/Sb_2Te_3 wafers are extremely fragile and require special care during the process. Dicing is done using a 50-µm thick blade with optimized cutting speed and depth. The depth of dicing has been set so that the blade does not damage the underlying metal lines during this step. In addition, the 50-µm thick SU-8 layer protects metal patterns from the blade during the dicing process. Finally, the completed devices are released from the supporting Si substrate by dissolving the sacrificial Ti layer.

A micro-TEG composed of 12 TE legs/gold lines thermocouples with an embedded area of 4×2 mm^2 and exposed area of 6×4 mm^2 is shown in Figure A.9. After releasing the device from the carrier Si wafer, the exposed area including heat pipes and terminal pads becomes mechanically flexible. The implanted area of the device is also fabricated on a

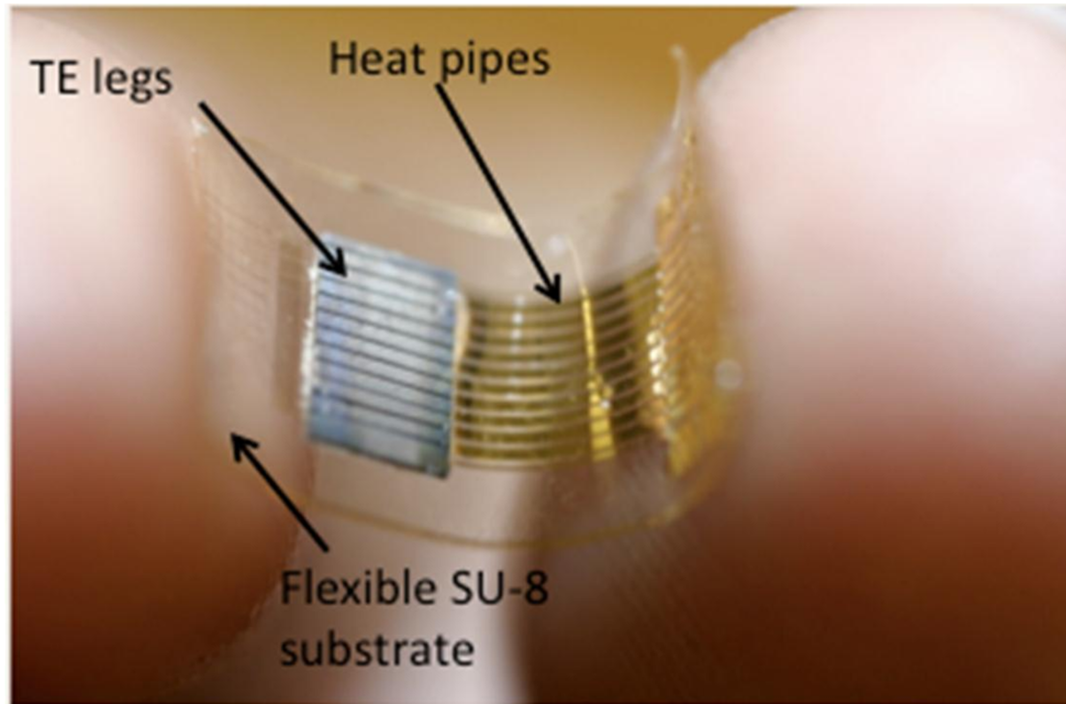
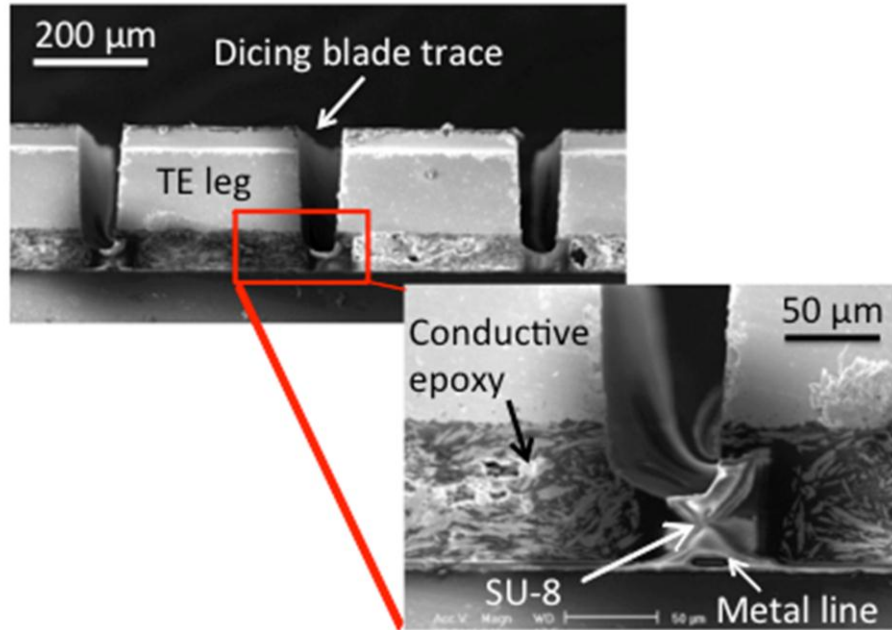


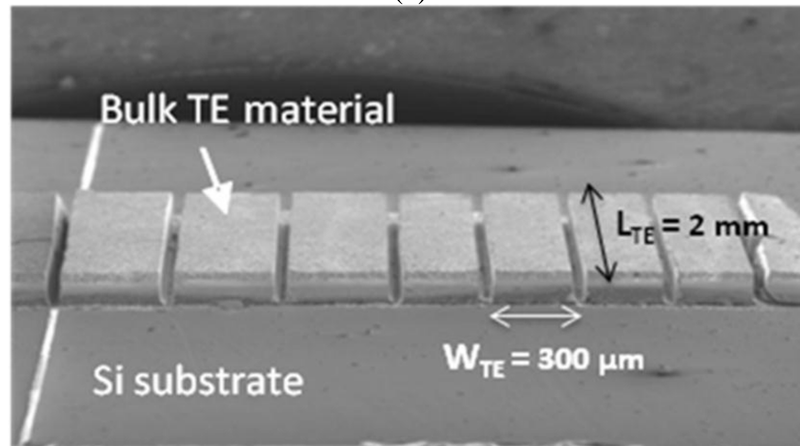
Figure A.9 Flexibility of the micro-TEG device after release from Si carrier wafer. TE legs and heat pipes on the SU-8 substrate are shown.

flexible polymer substrate. However, due to the brittle nature of the bulk TE material, it is not as flexible as the exposed area. Since the implantation experiment has been done with rigid dummy chips, the fabricated flexible micro-TEGs can also be implanted inside pupas with no complications.

Figure A.10(a) shows SEM images of the micro-TEG cross-section at the hot/cold junction, demonstrating the electrical contact between TE legs and metal pads by conductive epoxy. It also shows the dicing blade trace in the thick SU-8 layer, with no damage to the metal lines. The dicing limits of the bulk TE material are investigated by reducing the width of TE legs. A SEM image of the diced TE material piece is shown in Figure A.10(b). Several dicing experiments and characterization indicate that cracking occurs in TE legs as their width decreases below 250 μm.



(a)



(b)

Figure A.10 (a) SEM images of the cross-section of micro-TEG legs at the hot/cold junctions, contact between metal pads, conductive epoxy and TE legs (inset) (b) SEM image of bulk TE material dicing limit.

A.5. Experimental Results

The fabricated micro-TEGs are tested and characterized using the test setup shown in Figure A.11. An external platinum micro-heater is attached to the polymer substrate at the hot junction of the micro-TEG thermopiles. When the input voltage applied to the

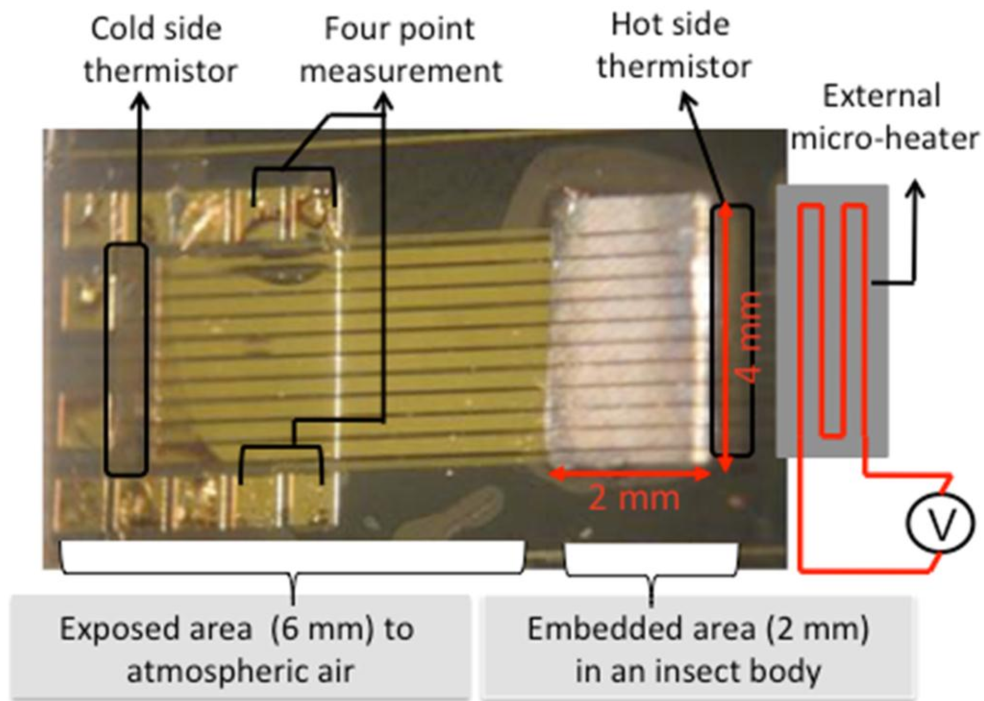


Figure A.11 A schematic representation of the micro-TEG measurement setup with the micro-heater placed on the hot side.

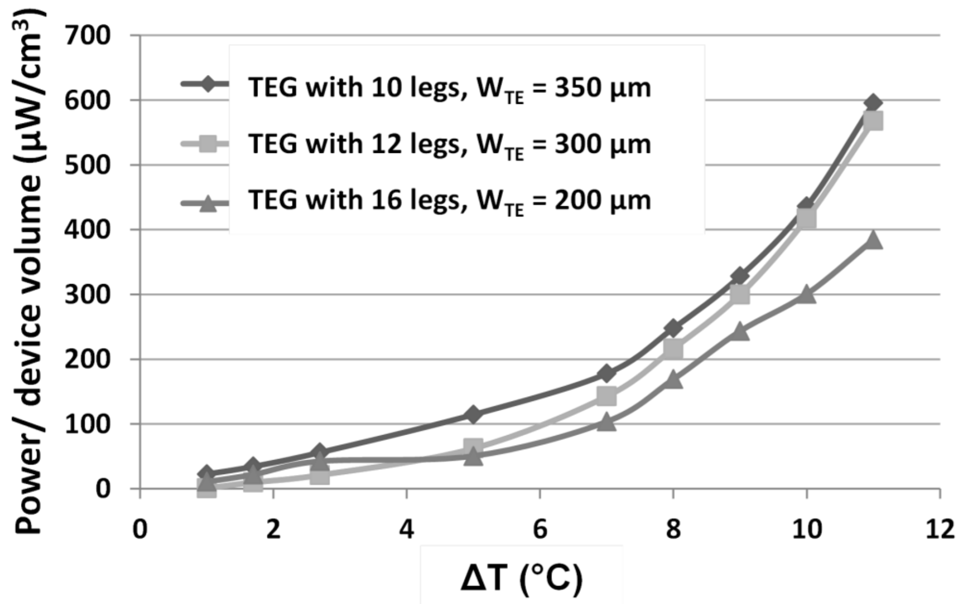
ports of the micro-heater increases, the temperature of the heater and as a result the temperature on the hot side of TE legs rises.

The micro-TEG, still attached to the Si carrier wafer, is placed on a probe station during the measurements, while the extended heat pipes are released and exposed to the ambient temperature. Therefore, the temperature on the cold side of the generator legs remains approximately constant due to the effect of the heat pipes. The absolute temperature change on both sides of the TE legs are measured with the integrated resistor temperature sensors. Integrated resistors with nominal resistance around 1 kΩ are fabricated near the hot and cold sides of the micro-TEGs. The changes in the resistance of these sensors are measured with a four-point probe configuration. Knowing the temperature coefficient of the Cr/Au integrated resistors; the resistance change can be translated into a temperature

change.

While increasing the input voltage to the external micro-heater, the temperature change is observed as an increase in the measured resistance. The thermally insulating polymer substrate, the cavities beneath the TE legs and the extended heat pipes keep the cold side temperature significantly lower than the hot side of the generator. However, due to parasitic thermal conduction through the substrate, metal lines, and TE legs, the temperature on the cold side of the generator still rises a few degrees above ambient temperature. Therefore, fabricating an integrated temperature sensor on the cold side of the generator is necessary to calculate the precise temperature difference along the TE legs of the device. The resistive temperature sensors are fabricated underneath the thick SU-8 layer, while the TE elements are placed above this layer. Therefore, the calculated temperatures based on resistance changes might be slightly different from the actual temperatures on the hot and cold sides. Two external thermocouples are attached to the micro-TEG substrate on both sides of the TE legs. These thermocouples are connected to a digital thermometer to measure and verify the temperature difference in the generator during measurements. This external temperature measurement setup demonstrates that the temperature difference measured by the integrated resistor sensors has an accuracy of about ±0.5 to 1ºC.

The output voltage and internal resistance of the micro-TEG are measured using the generator terminal pads while the micro-heater increases the temperature difference between hot and cold sides of the device. The maximum output power of the generator is calculated based on the measured voltage and internal resistance assuming load matching. The measured values show that the generator output voltage increases almost linearly



Implanted area (mm^2)	Exposed area (mm^2)	ΔT (°C)	Number of TE Legs	Measured Max Power (μW)	Power/ device volume ($\mu W/cm^3$)
8 (2×4)	24 (6×4)	11	16	1.2	600
			12	0.88	440
			10	0.64	320

Figure A.12 Performance comparison among TEG devices with different numbers of TE legs.

with the temperature difference, while the internal resistance of the device does not change significantly. The internal electrical resistance of the micro-TEG is defined by the material properties and dimensions. Although the TE properties of Bi_2Te_3/Sb_2Te3 are temperature dependent, the change is not considerable within the room temperature and beetle body temperature range for this application. Therefore, it was reasonable to assume constant electrical and thermal properties for micro-TEG materials, while calculating the output power based on the generator model.

Several micro-TEGs with 10, 12, and 16 TE legs have been fabricated and tested using

the described measurement setup. Figure A.12 shows the average generated power densities of these micro-TEGs versus the applied temperature difference. The power density of the micro-TEG was determined by dividing the device output power by the effective embedded volume of 2 mm^3. Harvested power values are in close agreement with the predicted output power values in the analytical model. These results demonstrate the functionality of the fabricated thermal scavenger over the temperature range produced in beetles. The highest measured output power of all tested devices with an 11ºC temperature difference, which is the beetle's maximum body-ambient temperature difference during its flight, is around 1.2 μW. Figure A.12 also shows the influence of the number of TE legs and their dimensions on generator performance. The micro-TEG output power is proportional to the sqaure of the number of TE elements; therefore, increasing W_{TE}, which results in fewer TE legs in the limited generator area, has an adverse effect on the device performance. Furthermore, wider TE legs increase the thermal loss through the TE material and lower the temperature difference between the two ends of the generator. The micro-TEG with 16 narrow TE legs has higher output power than the generators with fewer and wider TE legs. However, as mentioned in Section A.4, due to the brittle nature of Bi_2Te_3/Sb_2Te_3 alloys and dicing blade dimension limits, it is quite difficult to make a micro-TEG with the same effective embedded area and higher number of TE legs. Only a few generator devices with 16 TE legs survived the final dicing step of the fabrication process, while almost all of the micro-TEGs with 10 and 12 TE legs remained intact after dicing.

A.6. Discussion

Although the power generated by the fabricated micro-TEG is much less than the

required power for implanted devices compared to other available energy harvesting methods [1,82] with the use of right circuitry, it can store the generated power and use it in the absence of light and vibration. It can also be used as the required start-up power for another harvester. The proposed micro-TEG in this work weighs around 20 mg and can generate a power density of 60 μW/g at 11ºC temperature difference in the measurement setup. Implanting this generator inside the beetle may reduce its efficiency, since the whole device including both hot side and cold side are inside the body. However, with careful implantation, the cold side can be placed very close to the body's exterior surface. Furthermore, the high thermal conduction of metal heat pipes compared to the beetle tissues assures lower temperature on the cold side of the TEG.

During the testing process, the micro-TEG device was still attached to the carrier wafer and even though the thermal conduction of the underlying Si substrate was higher the effective thermal conductance of the device, the metal heat pipes which were detached from the substrate managed to maintain the temperature difference between hot and cold junctions. Therefore the measurement setup represents a highly accurate model of in-vivo testing, and it proves that the micro-TEG can be functional after implantation. The efficiency of the presented generator can be further improved by increasing the number of TE legs. Mechanical limitations of bulk TE material for fabrication of micro-scale devices have motivated the enhancement of material properties of thin films for utilization in the next generations of micro-TEGs. We have been working on TE thin film co-evaporation techniques because of the relatively high film quality, simple, repeatable, and flexible deposition technology, and the compatibility with *in situ* film patterning by shadow mask. Also, using a different flexible material such as Kapton (polyimide) or

PDMS instead of SU-8 as the generator substrate will enhance the flexibility of the whole device for implanting applications.

A.7. Conclusion

In this work, we designed and successfully fabricated and tested a new integrated micro-TEG with bulk Bi_2Te_3/Sb_2Te_3 legs. Our analysis shows that the output power density depends on the number of TE legs, their dimension and substrate design. This mechanically flexible micro-TEG with 16 TE legs is able to achieve a generated power of 1.2 μW from an 11ºC temperature difference. This device has demonstrated power generation capability at the maximum temperature difference produced during beetles' flight. The measurement results were in close agreement with the analytical analysis prediction. Target beetles showed a survival rate of 80% after chip implantation at the pupa state.

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