

**FLEXIBLE DIGITAL-INTENSIVE WIRELESS  
RECEIVERS IN NANOMETER CMOS**

by

David T. Lin

A dissertation submitted in partial fulfillment  
of the requirements for the degree of  
Doctor of Philosophy  
(Electrical Engineering)  
in The University of Michigan  
2012

Doctoral Committee:

Associate Professor Michael P. Flynn, Chair  
Assistant Professor James W. Cutler  
Assistant Professor David D. Wentzloff  
Assistant Professor Zhengya Zhang

© David T. Lin

---

2012

## ACKNOWLEDGEMENTS

Thank you to all of my colleagues, friends, and family for making different, but equally important contributions to my research and to my nearly six-year-long journey as a doctoral student.

I have been very fortunate to have the opportunity to conduct research in Professor Michael Flynn's group. Professor Flynn has given me a tremendous amount of guidance on research topics and advice on both high-level engineering problems and implementation details. My fellow group members have repeatedly amazed me with their knowledge, friendliness, and willingness to help each other, even when they were running on nothing more than two hours of sleep and three cups of coffee. I want to thank Aaron Rocca, Andres Tamez, Chun Lee, Chunyang Zhai, Dan Shi, Hyo Gyuem Rhew, Hyungil Chae, Ivan Bogue, Jaehun Jeong, Jeffrey Fredenburg, Jongwoo Lee, Jorge Pernillo, Joshua Kang, Junyoung Park, Li Li, Mark Ferriss, Mohammad Ghahramani, Nick Collins, and Shahrzad Naraghi for sharing their technical expertise and for their friendship. I've enjoyed the many random conversations we've had at the strangest times of the day.

I have also had the pleasure of working with and benefitting from the help of many students, faculty, and staff in the EECS department. My officemates in the circuits office have been great company during tape-outs over the last two years. Professor David Wentzloff shared his RF circuits and systems knowledge and helped with receiver modeling. Professor Zhengya Zhang shared his digital testing expertise, to which he

always added a friendly and well-needed reminder to balance research and life. Joel VanLaven in DCO provided excellent CAD and computing support, which allowed me to focus my efforts on research.

I want to thank my friends for adding relaxation to my life as a graduate student. I enjoyed the weekend get-togethers with David Huang, Jeff Hao, Jin Hu, Li Li, Min Kim, and Rach Liu. I especially want to thank Bernadette Chan, Grace Chen, and Rach Liu for our discussions and reflections about all things important and unimportant in life.

Lastly, I want to thank my mom, brother, and sister for their love and support. Their positive influence guided me toward the pursuit of an advanced degree and their encouragement helped me succeed in enduring and prevailing over the challenges that I encountered while pursuing my doctorate.

## TABLE OF CONTENTS

<b>ACKNOWLEDGEMENTS .....</b>	<b>ii</b>
<b>LIST OF TABLES .....</b>	<b>viii</b>
<b>LIST OF FIGURES .....</b>	<b>ix</b>
<b>LIST OF ABBREVIATIONS .....</b>	<b>xiii</b>
<b>ABSTRACT .....</b>	<b>xv</b>
<b>CHAPTER</b>	
<b>1. INTRODUCTION.....</b>	<b>1</b>
1.1 Background .....	1
1.2 Introduction to Discrete-Time Filters.....	4
1.3 Summary of Research Work .....	6
1.3.1 List of Key Contributions .....	8
1.4 Thesis Outline .....	8
<b>2. ANALOG DISCRETE-TIME FILTERING IN THE SARFILTER ADC .....</b>	<b>10</b>
2.1 Flexible Filtering SAR ADC Receiver Architecture.....	10
2.2 Charge-Sharing to Create Analog Discrete-Time Filters .....	10
2.3 DT FIR Filter.....	11
2.4 DT IIR Filter.....	12
2.5 Constraints on DT Filtering Configuration .....	13
2.6 Interleaved Sampling and SAR Conversion.....	15

2.6.1 SARfilter ADC DT Filtering Strategy.....	19
2.7 Capacitor Mismatch .....	20
2.8 DT Filter Noise.....	21
2.9 System Requirements .....	23
2.9.1 SNR Requirement.....	23
2.9.2 Anti-Alias Filtering .....	23
2.9.3 Front-end Linearity.....	24
2.10 Flexible SARfilter ADC Receiver Summary .....	26
<b>3. DISCRETE-TIME SPECTRUM-SENSING AND ADAPTIVE FILTERING</b>	<b>27</b>
3.1 Spectrum-Sensing Receiver .....	27
3.2 Benefits of Targeted Spectrum-Adaptive Filtering.....	28
3.3 Bandpass Subsampling for Spectrum-Analysis .....	30
3.4 Calculation of Power from the Output of the Spectrum-Analysis Filter.....	31
3.5 Accurate Frequency Tuning of the Spectrum-Analysis Filter .....	35
3.6 Creation of the DT Spectrum-Analysis Passband .....	37
3.7 Digitally-Controlled Spectrum-Sensing and Adaptive Filtering.....	42
3.8 Capacitor Mismatch and Sampling Jitter .....	43
3.9 Spectrum-Sensing Guided Reconfigurable Notch Filter.....	44
3.10 Spectrum-Sensing Receiver Summary .....	47
<b>4. RECEIVER PROTOTYPES.....</b>	<b>48</b>
4.1 Flexible Wideband Receiver with Reconfigurable Filtering SAR ADC .....	48
4.1.1 Architecture .....	48
4.1.2 SARfilter ADC .....	50

4.1.3 Ideal Receiver Filter Response .....	52
4.2 DT Spectrum-Sensing Receiver with Adaptive Filtering .....	52
4.2.1 Switched-Capacitor Amplifiers .....	53
4.2.2 Filtering SAR ADC (“SARfilter” ADC).....	54
4.2.3 Receiver Filtering Strategy .....	55
<b>5. PROTOTYPE MEASUREMENT RESULTS.....</b>	<b>57</b>
5.1 Flexible SARfilter ADC Receiver.....	57
5.1.1 Measured Filter Response .....	59
5.1.2 Packet Tests .....	60
5.2 DT Spectrum-Sensing Receiver with Spectrum-Adaptive Filtering.....	63
5.2.1 Spectrum-Sensing and Adaptive Filtering.....	64
<b>6. WIRELESS DEMONSTRATION SYSTEM .....</b>	<b>66</b>
6.1 System Overview .....	67
6.2 Receiver Daughter-Board.....	67
6.3 FPGA-based Baseband Demodulator.....	68
6.4 Image Reception Demonstration .....	72
<b>7. CONCLUSION.....</b>	<b>74</b>
7.1 Summary of Contributions .....	74
7.1.1 List of Key Contributions.....	75
7.2 Future Research Directions .....	76
7.2.1 Filtering SAR ADC with Less Filtering Overhead .....	76
7.2.2 Different Approaches to Spectrum-Sensing.....	77
7.2.3 DT Spectrum-Sensing for Cognitive Radios.....	77

7.2.4 New Approaches to RF Subsampling RX.....	78
<b>APPENDIX.....</b>	<b>79</b>
<b>BIBLIOGRAPHY.....</b>	<b>81</b>



## LIST OF TABLES

Table 3–1. Input and output rates and frequency response characteristics of the spectrum-analysis filter.....	37
Table 3–2. Effects of mismatch and jitter on the spectrum-analysis filter, simulated over 500 runs.....	44
Table 3–3. Switch numbers of the active sampling switches of the SS-guided notch filter during each time step, as a function of the filter mode. For time step 1, sampling alternates between the “a” and “b” switches.....	46
Table 5–1. Measured performance of the wideband receiver with reconfigurable DT. FIR/IIR filtering SAR ADC.....	62
Table 5–2. Summary of parameters and measurements of the spectrum-adaptive receiver. ....	65

## LIST OF FIGURES

Figure 1–1. Simplified high-level block diagram of the flexible receiver architecture, which replaces separate baseband filters with a filtering SAR ADC. ....	2
Figure 1–2. Simplified high-level block diagram of the spectrum-sensing receiver architecture, in which a spectrum-sensing system scans for the largest interferer over a 55MHz range and selects the optimal rejection mode of a simple reconfigurable filter. ...	2
Figure 1–3. Examples of simple DT FIR and IIR filters, where $f_s$ is the sampling rate of the filter. The blue circle indicates the frequency of an FIR filter zero and the blue X indicates the frequency of FIR filter poles.....	5
Figure 2–1. Simplified high-level block diagram of the flexible filtering SAR ADC receiver architecture. The ADC filters its input with an <i>analog</i> discrete-time (DT) filter <i>before</i> performing SAR A/D conversion. ....	10
Figure 2–2. Sampling of $V_{in1}$ onto $C_a$ and $V_{in2}$ onto $C_b$ and subsequent charge-sharing of $C_a$ and $C_b$ result in a weighted sum of the inputs.....	11
Figure 2–3. The DT filter response is created by selectively-sampling onto the SAR ADC capacitors over multiple cycles, and then charge sharing before SAR A/D conversion. ....	12
Figure 2–4. Schematic and timing diagram of the SARfilter ADC differential half-CDAC setup that implements the DT filter described by (2.3). The filtering operations in the other half-CDAC are identical. ....	14
Figure 2–5. Diagram of a unit capacitor cell and the switches that implement the SARfilter ADC.....	16
Figure 2–6. Interleaved sampling and SAR operations require the ADC to cycle through: (1) sampling onto MSBa, SAR with MSBb and LSB (top), (2) sampling onto LSB (middle), (3) sampling onto MSBb, SAR with MSBa and LSB (bottom), and (4) sampling onto LSB (middle). Some inactive switches are omitted.....	17
Figure 2–7. An example of the FIR component of a SARfilter ADC DT filter, with $f_{clk} = 80\text{MS/s}$ and $f_{conv} = 5\text{MS/s}$ . Interleaving increases $f_{conv}$ and allows placement of a filter notch at all multiples of 5MHz that are less than $f_{clk}$ . These notches reject interferers (light gray) that would otherwise alias onto a narrowband wanted signal at DC.....	20

Figure 2–8. Simulated yield of combined DT and amplifier pole filters with the frequency response shown in Figure 4–4 and DT contribution described by (2.8), for  $f_{clkFIR} = 80\text{MSps}$ ,  $f_{conv} = 5\text{MSps}$ , and amplifier poles at 6MHz and 30MHz. Only FIR filter mismatch (without interleaving) is modeled and each data point represents 1,000,000 mismatch configurations. The FIR capacitor banks are created from unit-sized capacitors. A configuration passes if it achieves the required rejection in bands centered at all multiples of 5MHz from 10MHz to 70MHz that are (a) 0.6MHz or (b) 2.0 MHz wide. . 21

Figure 2–9. PER resulting from demodulation of a wanted signal of 208-bit long packets, as a function of the relative power of an aliasing interferer. Both the wanted and interfering signals are compliant to the 2450MHz band of 802.15.4. .... 24

Figure 3–1. Simplified high-level block diagram of the spectrum-sensing receiver architecture. The spectrum-adaptive filtering system is highlighted in blue. .... 27

Figure 3–2. Diagram of conventional filtering (top) compared to spectrum-adaptive filtering (bottom). A conventional filter needs to attenuate all out-of-band frequencies with a relatively complex filter (18-tap analog DT FIR shown). A spectrum-adaptive filter uses spectrum-sensing to detect the largest interferers and configures a simpler filter (6-tap shown) to attenuate these interferers. The power and area savings scale approximately with the tap length..... 29

Figure 3–3. Bandpass subsampling refers to sampling at a rate proportional to a signal’s passband bandwidth. A bandpass filter first attenuates the out-of-band signals before subsampling occurs (top). The power contained within the subsampled signal (bottom) approximates the original signal well, even when aliasing occurs, as long as the filter adequately attenuates out-of-band signals. .... 30

Figure 3–4. Column (a) plots the IF spectrum of three different MSK modulated interferers (black) and the frequency response of an example spectrum-analysis filter (gray) centered at 20MHz. Column (b) plots the filtered and sub-sampled I/Q signals at the output of the spectrum-analysis filter and their complex envelope. Column (c) plots the 50<sup>th</sup> and 95<sup>th</sup> percentile boundaries of the error percentage (3.4) of the average measured signal power, as a function of the number of samples accumulated, N, over 5000 sets of randomized data in the MSK modulated interferer signal..... 33

Figure 3–5. Plots of the bandpass spectrum-analysis filter when configured to the lowest and highest center frequencies, 15MHz and 70MHz, respectively. A digital controller performs spectrum-sensing with this filter by sweeping the passband’s center frequency from 15 to 70MHz and inspecting the in-band power at each frequency. Aside from the attenuation caused by the TIA pole, the passband has equal bandwidth and gain at all center frequencies. .... 35

Figure 3–6. One of the identical I and Q branches of the four-stage DT bandpass spectrum-analysis filter, including the filter response of each stage. The combined response (lower-right plot) shows that the spectrum-analysis filter and the TIA pole together create a distinct power detection passband. .... 37

Figure 3–7. The integrator and the buffers in the spectrum-analysis filter are simple source-degenerated differential pairs. The integrator consists of five identical stages in parallel, each of which can be turned on or off to adjust the total transconductance. .... 38

Figure 3–8. The frequency responses of different cascaded combinations of the spectrum-analysis filter stages. Pole-zero cancellation between stages 2 and 3 create a power detection passband at  $0.1f_s$  and undesirable passbands at  $nf_s \pm 0.1f_s$ ,  $n=1,2,3,\dots$ . The integration “sinc” of the 1<sup>st</sup> stage attenuates the undesirable passbands, as shown in the cascaded response of stages 1, 2, and 3. .... 39

Figure 3–9. Frequency response of the spectrum-analysis filter when set to a center frequency of 50MHz. The gray line plots the response when the capacitors and sampling clocks are ideal and the colored lines overlay 50 different non-ideal configurations with  $\sigma_{\Delta C/C} = 0.05$  and  $\sigma_{\text{jitter}} = 30\text{ps}$ . The power detection passband remains well-defined in the presence of non-idealities. .... 43

Figure 3–10. Ideal frequency responses of the four modes of the SS-guided notch filter. The gray shaded areas indicate the frequencies that each mode targets. Table 5–2 summarizes the FIR filter coefficients and target attenuation frequencies. .... 45

Figure 3–11. Differential half-circuit schematic of the SS-guided reconfigurable DT FIR notch filter. The filter consists of six time-interleaved channels, each with 22 unit capacitors per half-circuit. Two capacitors connect to both  $V_{in}^{+/-}$  to implement negative filter coefficients and four capacitors are duplicated (gray background) to facilitate simultaneous sampling and read-out of the 1<sup>st</sup> FIR tap. .... 46

Figure 4–1. Diagram of the SARfilter ADC receiver, consisting of a wideband front-end, 2x LO divider, simple baseband amplifiers, and SAR ADCs with embedded configurable DT filtering. .... 48

Figure 4–2. Die photo of the SARfilter ADC receiver. .... 49

Figure 4–3. Simplified diagram of a unit capacitor cell of the filtering SAR ADC. Minimum size MiM capacitor and switches are used within the cell. Figure 2–5 shows a more complete schematic. .... 50

Figure 4–4. An example ideal combined filter response of the SARfilter ADC receiver and its DT FIR/IIR and amplifier pole components. The DT contribution is described by (2.8). .... 51

Figure 4–5. Architecture of the spectrum-adaptive receiver prototype. The spectrum-sensing path (bottom) scans to detect large interferers and automatically selects the optimal rejection mode of the reconfigurable DT notch filter. .... 53

Figure 4–6. Die photo of the spectrum-adaptive receiver. .... 54

Figure 4–7. Frequency response of the SARfilter ADC when it is configured to implement (4.1). .... 55

Figure 5–1. RF input power necessary to achieve a fixed ADC dynamic range of 4-bits (ENOB) with an $f_{carrier} + 1\text{MHz}$ tone input, as the carrier and LO frequencies vary from 500MHz to 3.6GHz. Supplies are fixed at 1V.....	58
Figure 5–2. Measured no-filter mode filter response and ideal and measured filter responses of the DT filter described by (2.8), when $f_{clk}=80\text{MS/s}$ , $f_{conv}=5\text{MS/s}$ (top) and by (5.1) when $f_{clk}=100\text{MS/s}$ and $f_{conv}=5\text{MS/s}$ (bottom).....	59
Figure 5–3. Measured packet error rate (PER) and frame error rate (FER) as a function of signal power and interferer power (relative to a fixed wanted signal power) for the 915MHz and 2450MHz bands of IEEE 802.15.4 and IEEE 802.11. Each test point represents the error rate calculated from 250 received packets. The gray line indicates the maximum PER or FER allowed by the standards.....	60
Figure 5–4. Measured combined frequency responses of the receiver, which includes the TIA pole; the SS-guided filter disabled, overlaid with the filter configured to one of four attenuation modes; and the SARfilter ADC filter. The gray shaded areas indicate the frequencies targeted by each mode of the SS-guided filter. ....	63
Figure 5–5. Measured minimum power of an FM interferer, with 1MHz deviation and 50kHz rate, that activates the four modes of the spectrum-adaptive filter. The power levels resemble inverted power detection passband frequency responses (Figure 3–5)...	64
Figure 5–6. Measured relative power vs. frequency offset of an FM interferer, with 1MHz deviation and 50kHz rate, at which the receiver achieves 1% PER when receiving RF modulated IEEE 802.15.4 2450MHz band packets with -85dBm power. Interferer rejection improves by an average of 9.4dB when the SA filter is enabled. ....	64
Figure 6–1. High-level diagram of the wireless receiver visual demonstration system. .	66
Figure 6–2. Demomonstration system with the receiver IC mounted on a daughter-board, which is connected to an off-the-shelf Xilinx FPGA development board.....	68
Figure 6–3. Measured modulated digital baseband outputs of the receiver at 4MS/s (a) and the resulting internal signals of the MATLAB demodulator as it processes the bitstreams (b), (c). The demodulator synchronizes to the packet’s synchronization header and digitally corrects phase offset (d). The FPGA demodulator is similarly implemented. ....	70
Figure 6–4. As the FPGA demodulator receives and demodulates each packet, the pixel information contained in the payload is updated on a monitor. The leftmost image is a test pattern, which is replaced pixel-by-pixel with the image. ....	72

## LIST OF ABBREVIATIONS

A/D	analog-to-digital
ADC	analog-to-digital converter
AM	amplitude modulation
BER	bit error rate
BPSK	binary phase-shift keying
CCK	complementary code keying
CDAC	capacitive digital-to-analog converter
CMOS	complementary metal-oxide-semiconductor
CT	continuous-time
DAC	digital-to-analog converter
DSP	digital signal processing
DSSS	direct-sequence spread spectrum
ENOB	effective number of bits
FIR	finite impulse response
FPGA	field-programmable gate array
GFSK	Gaussian frequency-shift keying
GSM	Global System for Mobile Communications
HT	high-throughput
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IIR	infinite impulse response
LNA	low noise amplifier
LO	local oscillator
LSB	least significant bit
LUT	lookup table
MSB	most significant bit

MSK	minimum-shift keying
NF	noise figure
OFDM	orthogonal frequency-division multiplexing
O-QPSK	offset quadrature phase-shift keying
PCB	printed circuit board
PER	packet error rate
PHY	physical (OSI layer)
QAM	quadrature amplitude modulation
RF	radio frequency
SA	spectrum-adaptive
SAR	successive approximation register
SC	switched-capacitor
SDR	software-defined radio
SNDR	signal to noise and distortion ratio
SNR	signal-to-noise ratio
SOC	system on a chip
SPI	serial peripheral interface
SS	spectrum-sensing
TIA	transimpedance amplifier
VGA	variable gain amplifier

## **ABSTRACT**

### **FLEXIBLE DIGITAL-INTENSIVE WIRELESS RECEIVERS IN NANOMETER CMOS**

by

David T. Lin

Chair: Michael Flynn

Wireless receivers designed in nanometer CMOS processes should take advantage of the strengths of more fundamentally digital topologies and intelligent digital control of analog circuitry. As congestion in the radio spectrum increases, receivers would also benefit from low-power, intelligent filters for interference rejection. Such filters would enable wireless devices on a limited power budget to efficiently share limited spectral resources. Analog discrete-time (DT) filters together with digital control show promise because the capacitors and switches that these filters consist of benefit from device scaling and because easily configurable digital sampling clocks determine their frequency responses.

This work introduces wireless receivers in 65nm CMOS that demonstrate the capabilities of analog DT filters coupled with intelligent digital control. The first receiver replaces conventional filtering stages with a SAR ADC that embeds a highly-integrated



DT FIR/IIR filter with programmable FIR tap length and coefficients. Interleaving of the SAR and DT filter sampling processes in this ADC maximizes the conversion rate and facilitates IIR filtering. The prototype receiver supports several standards and bands and exceeds the sensitivity and jammer resistance requirements of both the 915MHz and 2450MHz bands of IEEE 802.15.4, while consuming 4.0mW and 5.5mW, respectively. The second receiver introduces intelligent spectrum-adaptive (SA) filtering. The SA filter performs spectrum-sensing in an auxiliary signal path to detect interferers over a 55MHz range, and then selects the optimal filtering mode of a reconfigurable DT notch filter in the receiver's main signal path to suppress the strongest detected interferer. The auxiliary spectrum-sensing path isolates the power of interferers using a DT spectrum-analysis bandpass filter and calculates the power contained in the filter's output using simple DSP. A calibrated on-chip ring-oscillator drives the sampling clocks of the spectrum-analysis filter and enables accurate definition and tuning of the center frequency of its passband. In IEEE 802.15.4 2450MHz packet tests with SA filtering enabled, this receiver achieves  $\geq +55$ dB rejection of +25 to +65MHz FM interferers.

## **CHAPTER 1**

### **Introduction**

#### **1.1 Background**

Modern wireless devices must operate with an ever increasing number of communication standards and bands. Wireless receivers that use a narrowband front-end and continuous-time (CT) analog filters [1], [2] perform well for the standards that they target, but cannot easily adapt to multiple standards. The performance of a narrowband front-end degrades outside of the frequencies for which it is designed. CT baseband filters do not scale well with process, are difficult to reconfigure, and are sensitive to process mismatch. The rapidly changing wireless communication landscape makes such rigid design approaches undesirable. At the same time, there is a need for receiver architectures that take advantage of nanometer digital CMOS processes.

Over the last decade, research has led to several techniques to enable software-defined radios (SDR). Many of these techniques are based on analog discrete-time (DT) finite impulse response (FIR) and infinite impulse response (IIR) filters that are implemented by sampling an input signal onto capacitors and then manipulating the stored charge. These charge-domain filters have been explored for a wide variety of uses and for many different wireless standards. In [3] and [4], integration of the signal current onto I and Q capacitors over multiple clock cycles, together with charge-sharing with history capacitors, implements a sub-sampler with a complex band-pass response. The authors of

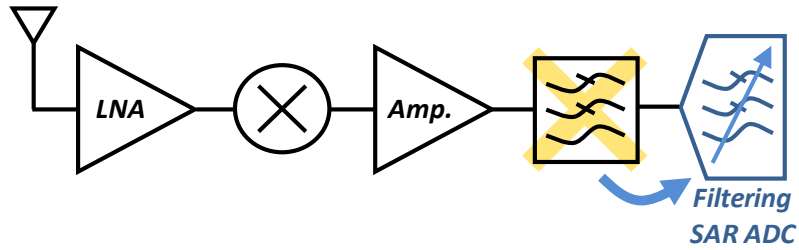


Figure 1–1. Simplified high-level block diagram of the flexible receiver architecture, which replaces separate baseband filters with a filtering SAR ADC.

[5] discuss an RF sampling Bluetooth receiver, in which analog DT filters decimate an initially high sampling rate while rejecting aliases. In order to take advantage of both simple analog CT and DT filters, [6] proposes down-converting IEEE 802.11g and GSM signals to baseband and then filtering with simple analog filters before applying analog DT filtering. Other SDR innovations complement analog DT techniques, such as a highly linear front-end with tunable analog filters [7] and RF/IF bandpass filtering using frequency-translated baseband impedances [8].

The first part of this dissertation introduces a flexible, digital-intensive receiver architecture (Figure 1–1) based on a modified SAR ADC that achieves both digitization and reconfigurable, robust, and scaling-friendly filtering. The filtering SAR ADC

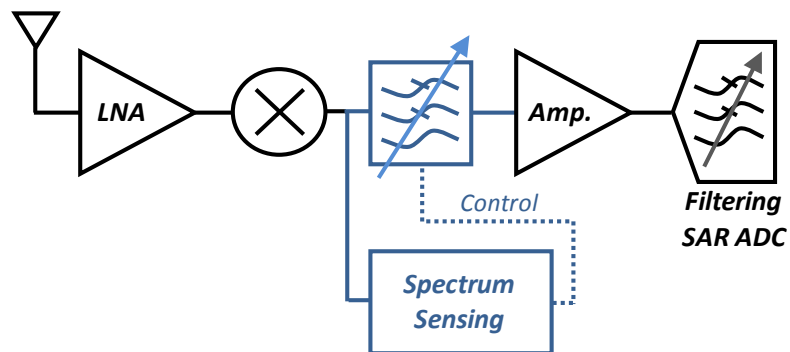


Figure 1–2. Simplified high-level block diagram of the spectrum-sensing receiver architecture, in which a spectrum-sensing system scans for the largest interferer over a 55MHz range and selects the optimal rejection mode of a simple reconfigurable filter.

replaces the separate filters and ADC of a conventional receiver and enables the creation of a highly-integrated flexible wireless receiver. This receiver architecture improves on existing analog DT filtering techniques by introducing a more integrated, more area-efficient, and more power-efficient DT filtering architecture. The second part of this dissertation introduces an architecture that improves the filtering SAR ADC architecture by introducing spectrum-adaptive filtering after the mixer (Figure 1–2). This architecture combines robust, low-power DT spectrum-sensing (SS), specialized for detecting large interferers, with a reconfigurable filter to adaptively filter strong interferers. By optimizing the filter in response to changing operating conditions, the receiver uses fewer circuit resources and less power.

Without spectrum-sensing (SS), we would have to overdesign the filters to attenuate all potential interferers at all times, even if we can reasonably expect only a limited number of intermittent, simultaneous interferers. Empirical studies of spectrum occupancy in populated areas [9], [10] show that spectrum usage ranges widely from <10% in many bands to nearly constant occupancy in broadcast television and cellular bands. In low occupancy bands, the low likelihood of simultaneous, high-power interferers and their changing frequencies suggest that targeted, spectrum-adaptive (SA) filtering can fulfill a receiver's interferer rejection needs. In high occupancy bands with mobile, sporadic transmitters, such as cellular bands, a SA filter can greatly reduce the attenuation required of a conventional filter by adaptively rejecting the strongest interfering signals transmitted by nearby sources.

Many of the existing spectrum-sensing techniques are specialized for cognitive wireless networks [11], such as IEEE 802.22 or 802.11af, which require high-sensitivity

detection of licensed users. The spectrum-sensing method discussed in [12] implements configurable and precise sensing bandwidth in an auxiliary signal path with a digitally-driven analog correlator. The method discussed in [13] measures power in the main signal path with an energy detector that rectifies the baseband signal. Because this detector relies on the filters in the main path to select the measurement band, the measurements are limited to the channel being received. The authors of [14] propose digital domain spectrum sensing, which requires a high-speed, high-resolution ADC and anti-aliasing filtering to digitize the entire band of interest. None of these approaches are appropriate for use as a spectrum-analyzer in a spectrum-adaptive (SA) filtering implementation, because their power and complexity would eliminate the potential gains in power and area of replacing a conventional filter with the SA filter. We instead realize SA filtering by creating a robust, low-power *analog* DT spectrum-sensing technique to detect strong interferers, and then adapting the attenuation profile of a reconfigurable filter in response to the detected interferers.

## **1.2 Introduction to Discrete-Time Filters**

Many different applications make use of discrete-time filters. The financial community refers to DT filters as moving averages and calculates these averages to perform technical trend analysis of stock prices, gross domestic product, and other financial and economic indicators [15]. Designers of analog television sets refer to DT filters as comb filters and use them to combine information from neighboring scan lines, in order to improve image quality [16].

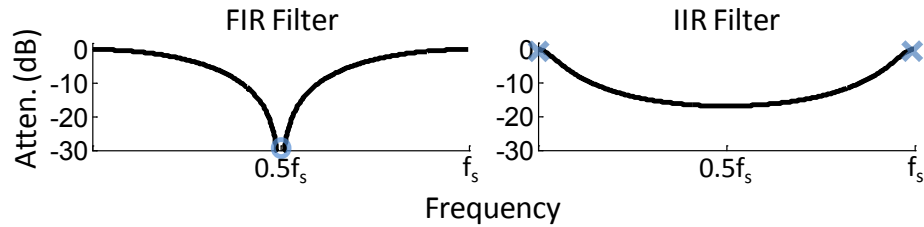


Figure 1–3. Examples of simple DT FIR and IIR filters, where  $f_s$  is the sampling rate of the filter. The blue circle indicates the frequency of an FIR filter’s zero and the blue Xs indicates the frequency of FIR filter’s poles.

DT filters are formed by scaling and summing together delayed versions of the input and output of the filter. A finite impulse response (FIR) DT filter only sums together delayed and scaled inputs. This filter generates zeros or notches. For example, the left plot in Figure 1–3 shows the frequency response of the following 2-tap FIR filter with equal tap coefficients:

$$y[n] = 0.5x[n] + 0.5x[n - 1]. \quad (1.1)$$

This filter creates zeros at  $(n + 0.5)f_s$ , where  $n = 0, 1, 2, \dots$  and  $f_s$  is the sampling rate of the filter. The blue circle in the plot indicates the frequency of the filter’s zero. An infinite-impulse response (IIR) DT filter sums delayed and scaled *outputs* in addition to inputs (i.e. the filter has feedback). This filter generates poles. For example, the right plot in Figure 1–3 shows the frequency response of the following IIR filter:

$$y[n] = 0.5x[n] + 0.5y[n - 1]. \quad (1.2)$$

This filter creates poles at  $nf_s$ , where  $n = 0, 1, 2, \dots$ . The blue Xs in the plot indicate the frequencies of the filter’s poles. The number of terms in the  $y[n]$  summation and the weight and delay of each term determine the number and frequencies of poles and zeros in the frequency response.

DT filters are typically implemented in the digital-domain because their implementation requires three basic operations: (1) delay, (2) weighting, and (3) addition. Digital circuits and microprocessors can efficiently perform these operations. But digital filtering can involve a prohibitive amount of power, complexity, and area in the signal preconditioning circuitry. The capture of an unfiltered signal requires significant oversampling with a high resolution ADC, in order to prevent aliasing of interferers and to digitize a weak wanted signal in the presence of a strong interferer. We instead implement DT filters in the sampled analog domain to circumvent these downsides of digital domain DT filters. Nonetheless, synthesized digital logic still contributes significantly to the efficient operation of analog DT filters in the proposed receiver architectures. The logic intelligently controls the attenuation of the filters in response to operating conditions and generates the sampling clocks that enable the filters to easily reconfigure.

### **1.3 Summary of Research Work**

We pursue the creation of an intelligent, spectrum-sensing reconfigurable receiver in two steps. First, we create a flexible wireless receiver architecture based on a modified SAR ADC that achieves both filtering and digitization. This 65nm CMOS receiver demonstrates reconfigurable filtering techniques without the complexities of spectrum-sensing and real-time adaptive filtering. The receiver consists of a wideband front-end, simple baseband amplifiers, and a reconfigurable analog DT filter that is embedded *within* a SAR ADC (“SARfilter ADC”). The embedded DT filter reuses the capacitors in the capacitive DAC (CDAC) of the ADC for filtering and reduces to need for CT baseband filtering. A SAR ADC consists of switches, capacitors, and a comparator, so

this leads to excellent scalability and conversion efficiency [17], [18] at the moderate resolutions and speeds necessary for many wireless standards. Compared to a separate DT filtering stage, the embedded DT filter eliminates resampling of charge from the filtering capacitors to the ADC and the associated resampling noise. This configurable SARfilter ADC receiver supports carrier frequencies ranging from 500MHz to 3.6GHz and functions with multiple communication standards and bands by adjusting its sampling rate and DT filter parameters. Its performance is verified with packets compliant to the 915MHz and 2450MHz bands of the IEEE 802.15.4 standard and the IEEE 802.11 standard.

We then improve the SARfilter ADC architecture by supplementing the receive chain with a spectrum-adaptive (SA) filter after the mixer and TIA, in order to detect and adaptively reject large interferers *before* additional amplification causes distortion. This spectrum-adaptive receiver architecture takes advantage of low-power analog discrete-time (DT) spectrum-sensing, which combines the scaling-friendly and robust charge-domain filtering concept with active digital control of the DT filter sampling clocks. The DT spectrum-sensing circuitry operates concurrently with the main receive path circuitry, in an independent, auxiliary path. It isolates the power within frequency bands of interest with analog DT decimation filters that also reject aliases, which permits the use of low-speed, low-resolution A/D conversion and simple digital post-processing to calculate the power of the interferers. We demonstrate SA filtering in a complete flexible receiver, consisting of a wideband front-end, transimpedance amplifier (TIA), a DT spectrum-sensing system, a four-mode SS-guided analog DT notch filter, switched-capacitor (SC) amplifiers, and a 7-bit SARfilter ADC that performs additional filtering and digitization.



The performance of SA filtering in the prototype is verified by receiving IEEE 802.15.4 packets in the presence of interferers that are offset 15MHz to 70MHz from a wanted signal.

### *1.3.1 List of Key Contributions*

- DT filtering SAR ADC (Chapter 2)
  - DT FIR/IIR filtering, embedded within a SAR ADC, with programmable tap length and coefficients
  - Interleaved FIR selective-sampling and SAR processes
- DT spectrum-sensing with adaptive filtering (Chapter 3)
  - DT spectrum-sensing detects interferers using DT spectrum-analysis bandpass filters and simple DSP
  - Calibrated on-chip oscillator accurately defines the frequency of the spectrum-analysis filter's passband
  - Real-time, digital selection of the optimal interferer rejection mode of the reconfigurable filter

## **1.4 Thesis Outline**

The following chapters describe the theoretical background, circuit prototypes, test systems, and measurement results of the digital-intensive analog DT wireless receiver architectures. Chapter 2 describes how sampling onto capacitors and charge-sharing implements analog DT filters and how the SARfilter ADC embeds such a filter. The latter part of the chapter analyzes how IEEE 802.15.4 2450MHz band specifications translate to receiver requirements. Chapter 3 describes the theory and implementation of the proposed DT spectrum-sensing system, non-idealities in the filters used to isolate interferer power, and how spectrum-sensing complements reconfigurable filtering to

adaptively filter interferers. Chapter 4 describes the implementation details of the SARfilter ADC receiver and spectrum-adaptive receiver prototypes. Chapter 5 describes the measurement results of the two receiver prototypes. Chapter 6 describes a wireless demonstration system of the receiver prototypes that receives and displays images encoded within IEEE 802.15.4 RF packets. Chapter 7 offers concluding remarks and recommends future research projects.

## CHAPTER 2

### Analog Discrete-Time Filtering in the SARfilter ADC

#### 2.1 Flexible Filtering SAR ADC Receiver Architecture

The flexible filtering SAR ADC (“SARfilter ADC”) architecture replaces dedicated baseband filtering stages with a filtering SAR ADC. Figure 2–1 shows a simplified high-level block diagram of the receiver, which features an LNA, direct down-conversion mixer, amplifier, and SAR ADC with embedded, reconfigurable *analog* DT FIR and IIR filtering. The ADC samples its input onto its capacitive DAC (CDAC), similar to a conventional SAR ADC, and manipulates the sampled charge to implement filtering *before* performing SAR analog-to-digital (A/D) conversion. The embedded, reconfigurable filter simplifies the receive chain before the ADC and allows the receiver to function with standards that have different signal bandwidths.

#### 2.2 Charge-Sharing to Create Analog Discrete-Time Filters

The fundamental operation in an analog DT filter is the sharing of sampled charge. A

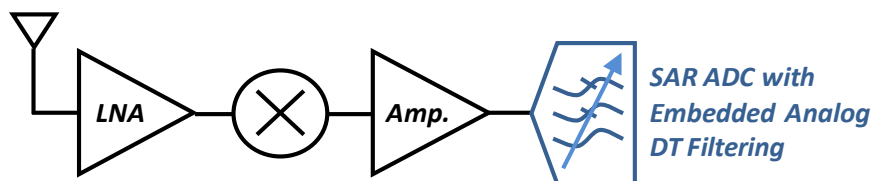


Figure 2–1. Simplified high-level block diagram of the flexible filtering SAR ADC receiver architecture. The ADC filters its input with an *analog* discrete-time (DT) filter *before* performing SAR A/D conversion.

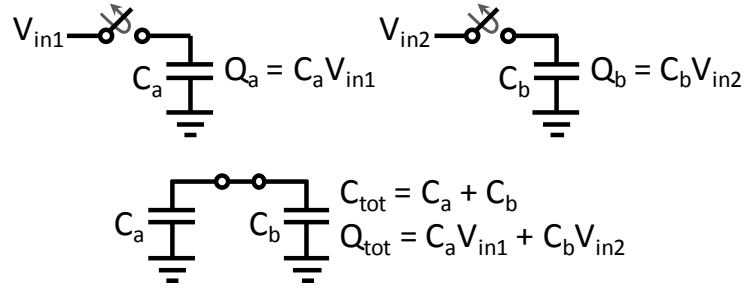


Figure 2–2. Sampling of  $V_{in1}$  onto  $C_a$  and  $V_{in2}$  onto  $C_b$  and subsequent charge-sharing of  $C_a$  and  $C_b$  result in a weighted sum of the inputs.

simple example, shown in Figure 2–2, quantifies the charge and voltage when two capacitors are charge-shared. Capacitor  $C_a$  samples  $V_{in1}$  and holds charge  $Q_a$  and capacitor  $C_b$  samples  $V_{in2}$  and holds charge  $Q_b$ . Shorting together of the two capacitors results in total capacitance and charge of  $C_{tot}$  and  $Q_{tot}$ , respectively, and in the following voltage,  $V_{out}$ , on the combined capacitors:

$$V_{out} = \frac{C_a}{C_a + C_b} V_{in1} + \frac{C_b}{C_a + C_b} V_{in2}. \quad (2.1)$$

$V_{out}$  is a weighted sum of the sampled inputs, which suggests that sampling and charge-sharing can perform the delay, scaling, and summation operations that are necessary to implement a DT filter.

### 2.3 DT FIR Filter

To the create an embedded DT FIR filter, we sample onto sections of the CDAC array of a SAR ADC over multiple clock cycles and then charge-share the DAC capacitors [19]. For example, Figure 2–3 shows that for an  $m$ -tap FIR filter, we first divide the CDAC into  $m$  capacitor groups. Then the input signal is sampled onto each of the  $m$  groups over  $m$  clock cycles. Since this multi-cycle selective-sampling process stores charge proportional to the input onto each group of capacitors, each group represents an

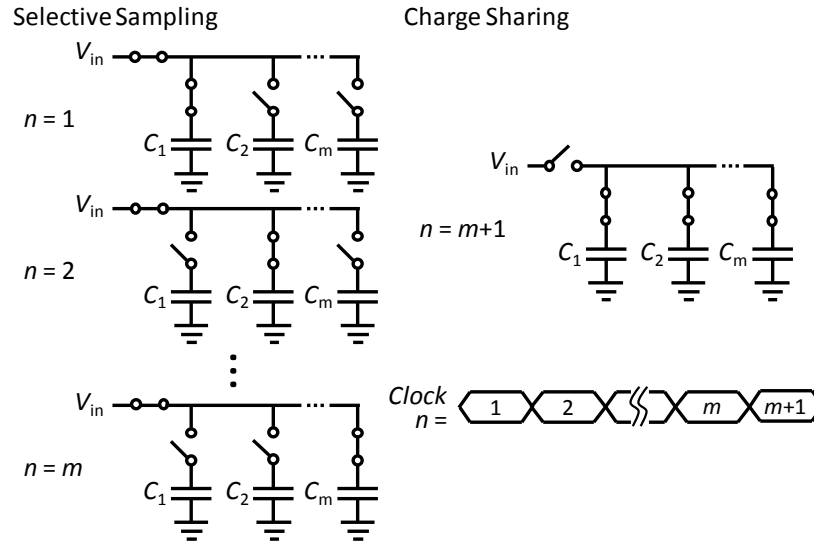


Figure 2–3. The DT filter response is created by selectively-sampling onto the SAR ADC capacitors over multiple cycles, and then charge sharing before SAR A/D conversion.

FIR filter tap. Therefore, we set the size of each FIR filter tap coefficient by scaling the relative size of each capacitor group. Finally, we short the capacitors together in the  $m+1$  clock cycle to average the stored charge and generate an FIR filtered sample of charge. The conventional SAR algorithm uses the CDAC to perform a 7-bit binary search to digitize this filtered charge sample.

## 2.4 DT IIR Filter

We add a history capacitor,  $C_H$ , that is never reset to the CDAC to implement an IIR filter. We begin by considering the simplest form of IIR filtering (i.e. not combined with FIR filtering), where we first sample a voltage,  $V_{in}$ , onto the entire CDAC capacitance,  $C_S$ , and then charge-share  $C_S$  with  $C_H$ . When this sampling and charge-sharing process repeats, the resulting charge on  $C_S$  is IIR filtered because charge-sharing with  $C_H$  adds a decreasing fraction of the previous samples to the current sample. The voltage,  $V_{out}$ , and

frequency response,  $H(z)$ , that correspond to the filtered charge on the  $n^{\text{th}}$  clock period is described as follows:

$$V_{out}(n) = r_S V_{in}(n) + r_H V_{out}(n-1), \text{ where } r_S = \frac{C_S}{C_S + C_H}, r_H = \frac{C_H}{C_S + C_H} \quad (2.2)$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{r_S}{1 - r_H z^{-1}}$$

Eq. (2.2) shows that charge-sharing with  $C_H$  creates a pole at DC and the distance of the pole from the unit circle depends on the relative sizes of  $C_S$  and  $C_H$ . A relatively larger  $C_H$  compared to  $C_S$  results in a sharper pole. Because this is a DT filter, the pole repeats at integer frequency multiples of the rate at which  $C_S$  is charge-shared with  $C_H$ ,  $f_{clkIIR}$ .

## 2.5 Constraints on DT Filtering Configuration

The IIR response described by (2.2) is correct only if the ratios  $r_H$  and  $r_S$  remain constant during every charge-share, which means that the size of  $C_S$  must remain fixed. This is always true for the previously described simple IIR example. But when we combine IIR filtering with the selective-sampling process of an FIR filter, we must configure the filter coefficients to ensure a constant  $C_S$ . We clarify this point with the following example, in which we explain how to implement the filter described by (2.3) in a 7-bit SAR ADC, with the schematic and timing diagram shown in Figure 2-4.

$$H(z) = \frac{1}{192} (b_1 z^{-16} + b_2 z^{-15} + \dots + b_{16} z^{-1}) \quad (2.3)$$

$$1 - \frac{2}{3} z^{-4}$$

$$[b_1 \ b_2 \ b_3 \ b_4] = [b_5 \ b_6 \ b_7 \ b_8] = [b_9 \ b_{10} \ b_{11} \ b_{12}] = [b_{13} \ b_{14} \ b_{15} \ b_{16}] = [3 \ 5 \ 5 \ 3]$$

The 16-tap FIR component of this DT filter, with repeating coefficients  $[3 \ 5 \ 5 \ 3]$ , is one of many FIR filters that the reconfigurable SARfilter ADC can implement.

The following description explains the setup of the CDAC array to implement the example and the timing of the switches. Figure 2–4 shows a  $32C_u$  history capacitor,  $C_H$ , on the right side of the schematic and the 64 unit capacitors,  $C_u$ , in the differential half-CDAC of a 7-bit differential SAR ADC that need to be sampled onto before SAR conversion. To implement FIR filtering, we first divide these 64 capacitors into four banks of  $16C_u$  each (i.e. banks A, B, C, and D in Figure 2–4), which gives us more flexibility to choose the FIR filter coefficients. This is because each entire  $16C_u$  bank is equivalent to  $C_S$  in the simple IIR example described by (2.2), in the sense that each bank is charge-shared in turn with  $C_H$  to implement the IIR filter. The capacitors within each  $16C_u$  bank are further divided into subgroups that correspond to the repeating FIR tap coefficients [3, 5, 5, 3] in (2.3), because each bank must implement the same FIR filter when it is charge-shared with  $C_H$ .<sup>1</sup> In this way, charge-sharing an entire  $16C_u$  bank with

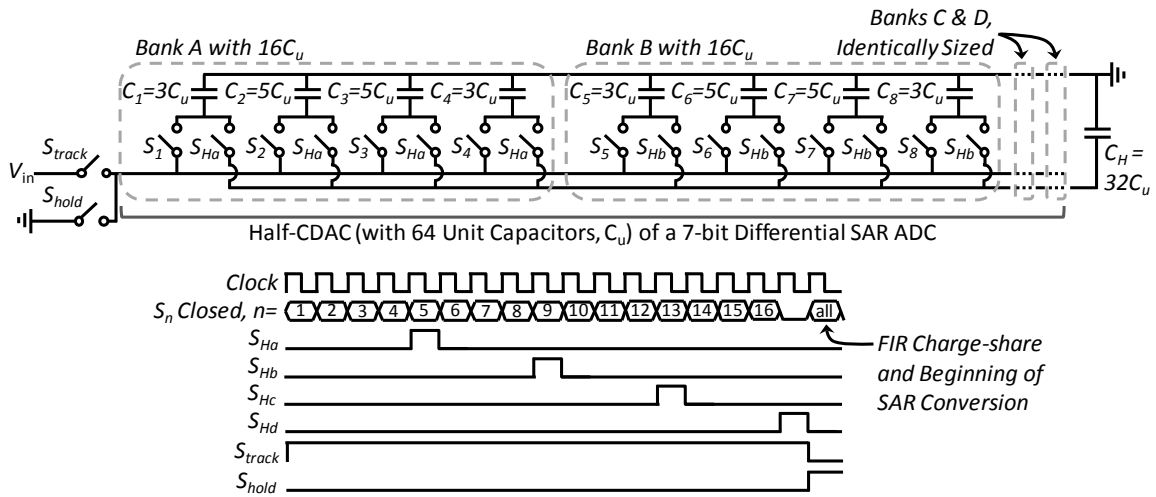


Figure 2–4. Schematic and timing diagram of the SARfilter ADC differential half-CDAC setup that implements the DT filter described by (2.3). The filtering operations in the other half-CDAC are identical.

<sup>1</sup> This DT filtering example can be viewed as a cascade of 4-tap FIR filtering with coefficients [3 5 5 3], then IIR filtering, and then 4-tap FIR filtering with coefficients [1 1 1 1]. Therefore, each bank must have the same filter coefficients in order to correctly implement the first filter in the cascade.

$C_H$  keeps  $C_S$  constant, as required for IIR filtering, but the tap coefficients within the bank can be unequal (e.g. 3 and 5 above). Selective-sampling of  $V_{in}$  onto the subgroups of bank A, through switches  $S_1, S_2, S_3$ , and  $S_4$  in Figure 2–4, implements the first four taps of the 16-tap FIR filter. These four samples then charge-share with  $C_H$  through switches  $S_{Ha}$  to implement the IIR filter response, while selective-sampling onto bank B through switch  $S_5$  happens at the same time. After this selective-sampling and IIR charge-sharing process occurs for all four banks (A, B, C, and D), these banks charge-share through switches  $S_1$ - $S_{64}$  to combine the filtered samples of charge on the four banks into a single sample. The conventional SAR ADC algorithm then digitizes this combined sample.

In the analog DT filtering process described above, the IIR filtering rate differs from the FIR filtering rate,  $f_{clkFIR}$ . As before, the lowest frequency pole of the IIR filter is located at DC and the poles of this DT filter repeat every  $2\pi$ ; that is, at integer frequency multiples of the rate at which  $C_S$  is charge-shared with  $C_H$ ,  $f_{clkIIR}$ . Eq. (2.4) describes  $f_{clkIIR}$ , where  $m$  is the number of selective samples that is collected before charge-sharing with  $C_H$ .

$$f_{clkIIR} = \frac{f_{clkFIR}}{m} \quad (2.4)$$

In the example above, charge-sharing with  $C_H$  occurs after every 4<sup>th</sup> sample, which results in a DT IIR pole that repeats every  $f_{clkIIR} = f_{clkFIR}/4$  and is represented by the  $z^{-4}$  term in the denominator of (2.3).

## 2.6 Interleaved Sampling and SAR Conversion

Selective-sampling for the embedded DT FIR filter takes multiple clock cycles and therefore reduces the conversion rate of the SAR ADC,  $f_{conv}$ . We first analyze the reduced



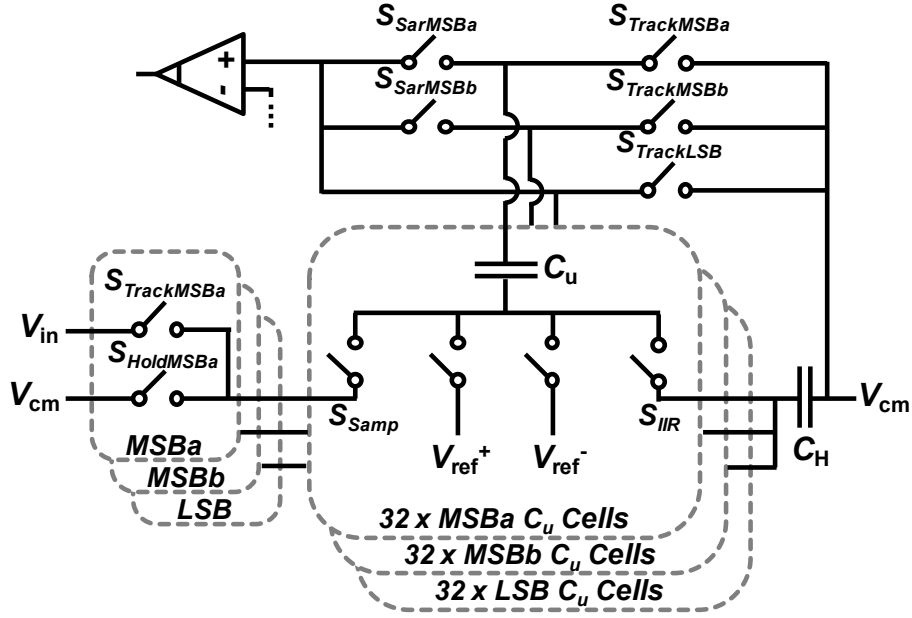


Figure 2–5. Diagram of a unit capacitor cell and the switches that implement the SARfilter ADC.

rate, and then introduce interleaving of the selective-sampling and SAR conversion processes to counteract this reduction. The following analysis derives  $f_{conv}$  as a function of the filter and SAR conversion parameters and the frequency of a master clock,  $f_{clk}$ , which specifies the underlying unit-sampling period. As indicated by  $S_n$  in the timing diagram of Figure 2–4, selective-sampling requires as many periods as the number of filter taps,  $n_{tap}$ . And as indicated by  $S_{Hd}$ , IIR charge-sharing requires one extra period between sampling and SAR conversion. In (2.5),  $n_{IIR}$  represents this extra period. SAR ADC conversion requires as many periods as ADC bits,  $n_{SAR}$ . Without employing any special techniques, the embedded filtering reduces the 7-bit ADC conversion rate,  $f_{conv}$ :

$$f_{conv} = \frac{f_{clk}}{(n_{tap} + n_{IIR} + n_{SAR})} = \frac{f_{clk}}{(n_{tap} + 1 + 7)} = \frac{f_{clk}}{(n_{tap} + 8)}. \quad (2.5)$$

We introduce interleaving of the sampling and SAR conversion processes to

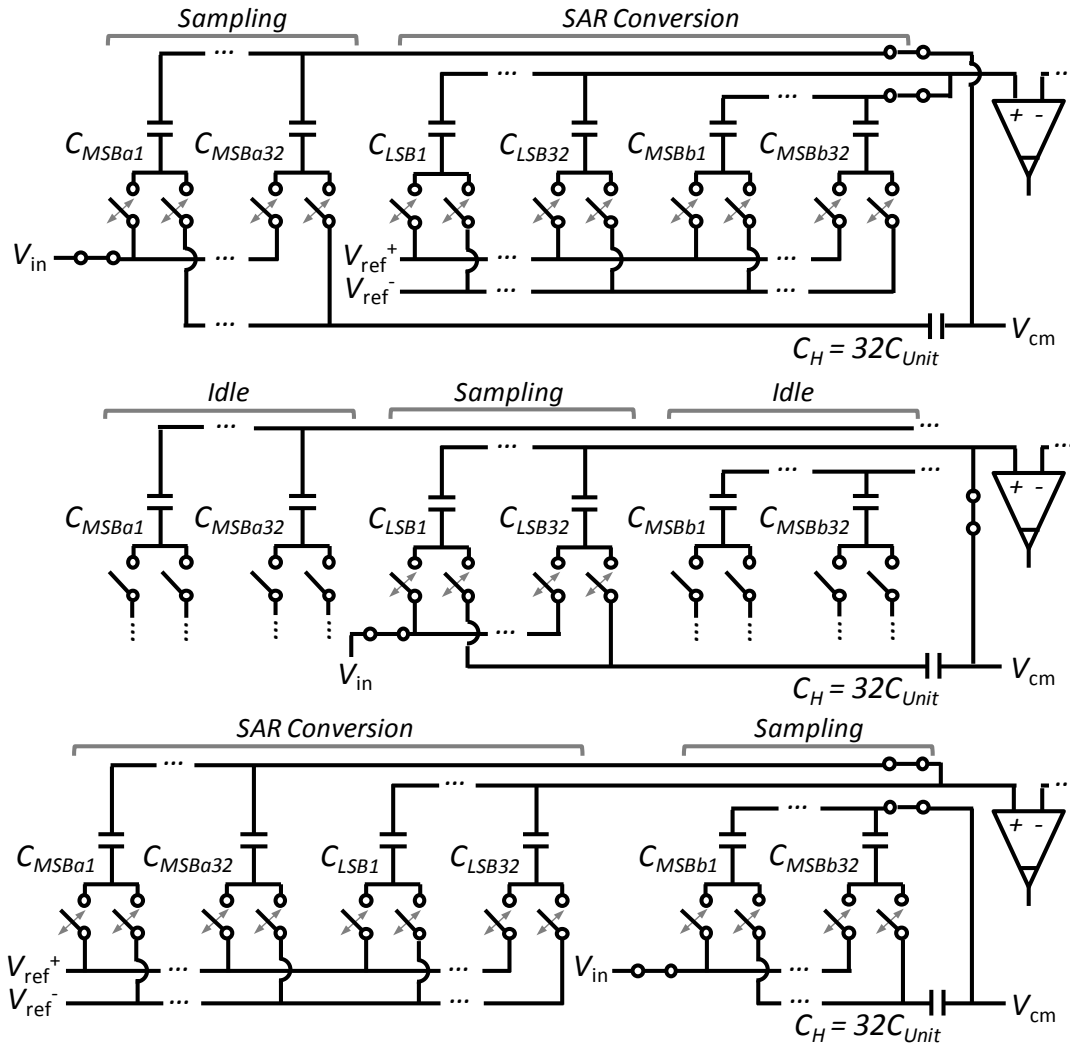


Figure 2–6. Interleaved sampling and SAR operations require the ADC to cycle through: (1) sampling onto MSBa, SAR with MSBb and LSB (top), (2) sampling onto LSB (middle), (3) sampling onto MSBb, SAR with MSBa and LSB (bottom), and (4) sampling onto LSB (middle). Some inactive switches are omitted.

counteract the reduction in  $f_{conv}$  due to the filtering. Figure 2–5 and Figure 2–6 show the modifications that we make to the traditional SAR ADC architecture to implement interleaved filtering. The CDAC in the prototype 7-bit ADC consists of 96  $C_u$  cells, instead of 64  $C_u$  cells, per differential half-circuit. These 96  $C_u$  cells are equally divided

into an LSB bank and two MSB banks, MSBa and MSBb.<sup>2</sup> MSBa and MSBb are duplicates and implement interleaved sampling and SAR operations over four multi-cycle phases. In the first of four phases, we selectively sample the first  $n_{tap}/2$  taps of an  $n_{tap}$  FIR filter onto the MSBa bank while SAR conversion digitizes the previously sampled and filtered charge on the MSBb and LSB banks (top of Figure 2–6). In phase 2, we selectively sample the remaining  $n_{tap}/2$  taps onto the LSB bank (center of Figure 2–6). In phase 3, SAR conversion digitizes the filtered charge on the MSBa and LSB banks while we selectively sample the first  $n_{tap}/2$  taps for the next conversion cycle onto MSBb (bottom of Figure 2–6). In phase 4, we once again sample the remaining  $n_{tap}/2$  taps onto the LSB bank (center of Figure 2–6) and the process repeats. IIR charge-sharing occurs periodically throughout this interleaved sampling process in the same way as Figure 2–4 shows for non-interleaved sampling.

Figure 2–5 shows the extra switches required for interleaving. Each bank (i.e. MSBa, MSBb, and LSB) has dedicated  $S_{Track}$  and  $S_{Hold}$  switches because, as described above, each bank participates in sampling and SAR at a different time. The  $S_{SarMSBa}$  and  $S_{SarMSBb}$  switches between the MSB capacitors and the comparator isolate MSBa from the comparator while MSBb participates in SAR conversion and vice versa. In each  $C_u$  cell, the  $S_{Samp}$  switch between  $V_{in}$  and  $C_u$  implements selective-sampling for FIR filtering. The  $S_{IIR}$  switch between  $C_H$  and each  $C_u$  cell creates a charge-sharing path for IIR filtering.

Interleaving increases the conversion rate:

$$f_{conv} = \frac{f_{clk}}{\max\left(\frac{n_{tap}}{2}, n_{IIR}+n_{SAR}\right) + \frac{n_{tap}}{2}} \quad (2.6)$$

---

<sup>2</sup> “MSB” here refers to the CDAC capacitors that are switched to determine the MSB-1 bit in a differential SAR ADC.

In the *max* term in the denominator,  $n_{tap}/2$  accounts for the time spent on interleaved selective-sampling and  $n_{IIR}+n_{SAR}$  accounts for the time spent on IIR charge-sharing and SAR conversion (phases 1 and 3 above). This term takes the greater (i.e. *max*) of the number of clock periods spent: (1) selectively sampling the first half of the FIR filter taps,  $n_{tap}/2$ , onto one of the two MSB banks and (2) IIR charge-sharing and SAR conversion with the *other* MSB bank and the LSB bank. The second term in the denominator represents the time spent selectively sampling the second half of the FIR filter taps onto the LSB bank (phases 2 and 4 above). Eq. (2.7) simplifies (2.6) by substituting typical values of the variables. The first expression in (2.7) substitutes  $n_{SAR}$  of 7 for a 7-bit ADC and  $n_{IIR}$  of 1 for the one extra clock cycle spent on IIR charge-sharing immediately before SAR conversion ( $S_{Hd}$  in Figure 2–4). The second expression assumes that the FIR filter has at least 16 taps,  $n_{tap} \geq 16$ , so that  $n_{tap}/2 \geq 8$  in the *max* expression.

$$f_{conv} = \frac{f_{clk}}{\max\left(\frac{n_{tap}}{2}, 8\right) + \frac{n_{tap}}{2}} = \frac{f_{clk}}{n_{tap}} \quad (2.7)$$

### 2.6.1 SARfilter ADC DT Filtering Strategy

The improvement in  $f_{conv}$  that interleaving achieves enables the creation of an FIR filter with enough notches to be placed at all of the alias frequencies of a wanted signal that is direct down-converted to DC. For example, the 16-tap filter shown in Figure 2–7 uses interleaving to achieve  $f_{conv}$  of 5MS/s with a filter sampling rate,  $f_{clk}$ , of 80MS/s. A 16-tap FIR filter creates 15 notches, such that a notch can be placed at  $m \cdot f_{conv}$ , where  $m=1,2\dots15$ , which are the frequencies that would otherwise alias onto a narrowband signal at DC. The 1<sup>st</sup> unwanted pass-band of the DT FIR filter occurs at

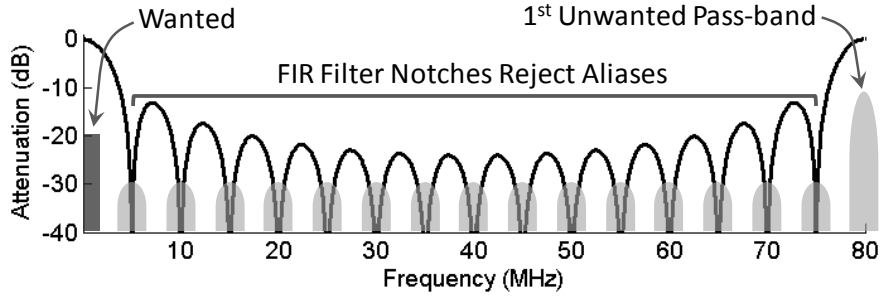


Figure 2–7. An example of the FIR component of a SARfilter ADC DT filter, with  $f_{clk} = 80\text{MS/s}$  and  $f_{conv} = 5\text{MS/s}$ . Interleaving increases  $f_{conv}$  and allows placement of a filter notch at all multiples of 5MHz that are less than  $f_{clk}$ . These notches reject interferers (light gray) that would otherwise alias onto a narrowband wanted signal at DC.

$f_{clk}=16\cdot f_{conv}=80\text{MHz}$ . At this relatively high frequency, the amplifier poles in the prototype receiver provide adequate alias rejection of approximately 30dB.

## 2.7 Capacitor Mismatch

Analog DT filters are robust to variation and mismatch in filter capacitor sizes. Unlike continuous-time filters, the relative sizes of capacitors define the zero and pole locations. When process variation identically scales the sizes of all of the filter capacitors, the DT frequency response does not change. Also, simulations show that DT filters are robust to capacitor mismatch. Figure 2–8 shows the simulated yield of the filter response described by (2.8) (and shown in Figure 4–4) as a function of unit capacitor mismatch.

$$y(n) = \frac{1}{48} [x(n-1) + x(n-2) + \dots + x(n-16)] + \frac{2}{3} y(n-4) \quad (2.8)$$

Typical amounts of capacitor mismatch minimally impact the rejection of this filter. As shown in Figure 2–8(a), the filter achieves 40dB rejection in a 0.6MHz bandwidth centered at all multiples of 5MHz from 10MHz to 70MHz (see figure caption) with nearly perfect yield for mismatch of less than 10%  $\sigma_{\Delta C/C}$ . The filter also achieves 35dB

rejection over a 2MHz bandwidth with very high yield, even when mismatch is 20%  $\sigma_{\Delta C/C}$ .

## 2.8 DT Filter Noise

Multi-cycle FIR selective-sampling results in the same total sampled noise as sampling in a conventional SAR ADC, where the input is sampled onto the entire CDAC

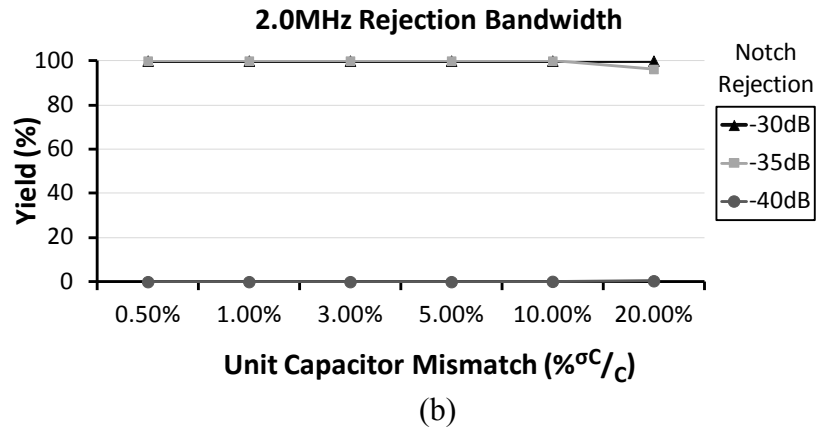
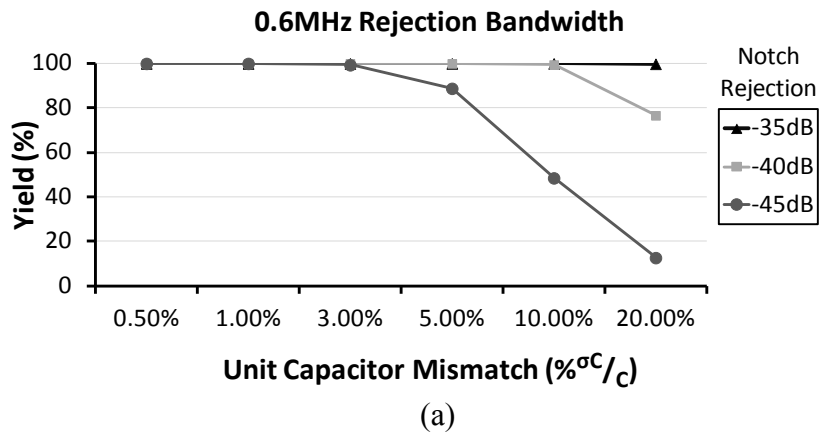


Figure 2–8. Simulated yield of combined DT and amplifier pole filters with the frequency response shown in Figure 4–4 and DT contribution described by (2.8), for  $f_{clkFIR} = 80\text{MSps}$ ,  $f_{conv} = 5\text{MSps}$ , and amplifier poles at 6MHz and 30MHz. Only FIR filter mismatch (without interleaving) is modeled and each data point represents 1,000,000 mismatch configurations. The FIR capacitor banks are created from unit-sized capacitors.

A configuration passes if it achieves the required rejection in bands centered at all multiples of 5MHz from 10MHz to 70MHz that are (a) 0.6MHz or (b) 2.0 MHz wide.

at once. To see this, consider the total noise that results from sampling onto two capacitors sized  $xC$  and  $yC$  and then charge-sharing of these capacitors:

$$\overline{v_n^2} = \frac{kT}{xC} \left( \frac{x}{x+y} \right)^2 + \frac{kT}{yC} \left( \frac{y}{x+y} \right)^2 = \frac{kT}{(x+y)C}. \quad (2.9)$$

Sampling in a single clock period onto the same total capacitance,  $(x+y)C$ , results in an equal amount of sampled noise power:

$$\overline{v_n^2} = \frac{kT}{(x+y)C}. \quad (2.10)$$

Although (2.9) analyzes two-step selective-sampling, additional selective-sampling capacitors and steps result in the same outcome.

The DT IIR filter requires charge-sharing of the sampling capacitance with a history capacitor, which introduces additional noise onto the sampling capacitor.<sup>3</sup> The amount of additional noise is solved as  $kT/C$  noise, where  $C$  is the series combination of  $C_S$  and  $C_H$ , followed by capacitive division to determine the component of this noise that is left on  $C_S$ .

$$\overline{v_{n,IIR}^2} = \frac{kT}{C_S \left( 1 + \frac{C_S}{C_H} \right)} \quad (2.11)$$

In practical filter implementations,  $C_H$  is 1-3 times larger than  $C_S$ , in order to maintain a good balance between out-of-band attenuation and in-band signal droop. Therefore, IIR filtering approximately doubles the sampled noise.

---

<sup>3</sup> A noisy charge-sharing switch redistributes charge between the two connected capacitors. In FIR charge-sharing, the SAR ADC digitizes the *total* charge on  $C_S$ , so charge redistribution does not change the digital output. In IIR charge-sharing, the SAR ADC digitizes the resulting charge on  $C_S$ , so the digital output includes the effect of charge redistribution between  $C_S$  and  $C_H$  due to noise.

## 2.9 System Requirements

The wideband front-end and SAR ADC with embedded, configurable DT filters permit the prototype wireless receiver to function with many communication standards and bands. It is insightful to approximate system requirements for the 2450MHz band of IEEE 802.15.4 [20] and see how this flexible receiver performs.

### 2.9.1 SNR Requirement

Assuming an ideal demodulator, achieving 1% PER requires a minimum signal-to-noise ratio,  $SNR_{minIdeal}$ , of -2.2dB at the demodulator input [21]. The maximum allowable noise figure,  $NF_{max}$ , of the receiver is then calculated from the IEEE 802.15.4 2450MHz band's required sensitivity of -85dBm, thermal noise within a 2MHz bandwidth,<sup>4</sup> and  $SNR_{minIdeal}$ :

$$NF_{max} = -85dBm + 174dBm - 63dB + 2.2dB = 28.2dB \quad (2.12)$$

Although other receiver non-idealities such as aliasing, non-linearity, filter in-band droop, and non-ideal demodulation consume part of this 28.2dB margin, enough margin remains to permit the use of a relatively high NF wideband LNA.

### 2.9.2 Anti-Alias Filtering

Aliasing interferers minimally degrades PER as long as filters attenuate their power to slightly below the power of the wanted signal. As shown in Figure 2–9 for the 2450MHz band of 802.15.4, the power of an interferer that aliases completely onto the wanted signal has to be at least 1.8dB less than the power of the wanted signal. With additional

---

<sup>4</sup> For simplicity, the bandwidth of the receiver is assumed to equal the chip rate of 2Mchip/s. The majority of the power of the MSK modulated signal lies within this bandwidth [36].



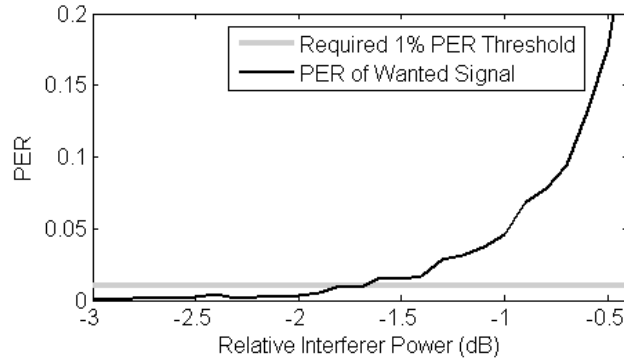


Figure 2–9. PER resulting from demodulation of a wanted signal of 208-bit long packets, as a function of the relative power of an aliasing interferer. Both the wanted and interfering signals are compliant to the 2450MHz band of 802.15.4.

1-2dB attenuation of the interferer, its effect becomes negligible because the demodulator can synchronize to the correct packet header.

The analog DT pre-filter in the SARfilter ADC provides most of the alias rejection in this receiver. For the 2450MHz band of 802.15.4, the specified adjacent ( $\pm 5\text{MHz}$ , +0dB) and alternate ( $\pm 10\text{MHz}$ , +30dB) interferers alias completely onto the wanted signal when the conversion rate of the ADC,  $f_{conv}$ , is 5MHz. Since the power of the aliased signal should be at least  $\approx 2\text{dB}$  less than the power of the desired signal, the adjacent and alternate interferers must be attenuated by more than 2dB and 32dB, respectively.

### 2.9.3 Front-end Linearity

The SARfilter ADC receiver architecture replaces the explicit filtering stages before the ADC with a DT filter embedded in the SAR ADC. The poles of the baseband amplifiers provide limited but sufficient attenuation (i.e.  $\approx 10\text{dB}$ ) to keep the required  $\text{IIP}_3$  within reasonable bounds. We estimate the required  $\text{IIP}_3$  levels due to blocker induced gain compression and intermodulation.

A calculation of gain compression due to an interferer tone results in the following required  $IIP_3$  to limit gain compression to -1dB:

$$IIP_3 = P_{int,-1dB} + 12.6dB. \quad (2.13)$$

$P_{int,-1dB}$  is the power of the *interferer* that causes 1dB of gain compression of the *wanted* signal. As an example, we calculate the required  $IIP_3$  for the 2450MHz band of 802.15.4 based on the specified wanted signal power of -82dBm and the +30dB/±10MHz interferer power of -52dBm for the jammer resistance tests [20]. The lowest frequency pole of 6MHz of the transimpedance amplifier that follows the mixer attenuates the interferer by ≈6dB, so  $P_{int,-1dB}$  is -58dB and the required  $IIP_3$  is -45.4dBm.

A calculation of the intermodulation interference generated by two interferer tones, where  $2f_{int1} = f_{int2}$ , results in the following required  $IIP_3$ , where  $s_{in}$  is the wanted tone amplitude,  $s_{int1/2}$  are the interferer tone amplitudes, and  $IM_3$  is the ratio of the intermodulation product amplitude to  $s_{in}$ :

$$IIP_3 = \sqrt{\frac{x_{int1}^2 x_{int2} s_{in}^2}{IM_3}}, \text{ where } x_{int1} = \frac{s_{int1}}{s_{in}}, x_{int2} = \frac{s_{int2}}{s_{in}}. \quad (2.14)$$

As an example, we again calculate the required  $IIP_3$  for the 2450MHz band of 802.15.4. The lowest frequency pairs of in-band interferers that can intermodulate onto the wanted signal are at ±5MHz/±10MHz and ±10MHz/±20MHz. The standard specifies relative jammer powers of +0dB and +30dB for the ±5MHz and +10MHz interferers, respectively, so we also assume a relative power of +30dB for the ±20MHz interferer. Therefore, the higher-powered 2<sup>nd</sup> interferer pair limits the  $IIP_3$ . The effect of the intermodulation product is similar to aliasing (Figure 2–9), so we assume that an  $IM_3$  of -10dB is more than adequate. The pole of the transimpedance amplifier that follows the mixer attenuates the ±10MHz/±20MHz interferers by ≈6dB/≈11dB, respectively.

Application of the  $-82\text{dBm } s_{in}$  specified in the jammer resistance tests and the attenuated  $\pm 10\text{MHz}/\pm 20\text{MHz}$  interferers to (2.14) results an  $\text{IIP}_3$  of  $-43.5\text{dBm}$ .

These sample calculations show that the attenuation provided by the poles of the baseband amplifiers sufficiently limits the required  $\text{IIP}_3$ , so that we can replace alternating stages of baseband amplification and filtering with the SARfilter ADC.

## **2.10 Flexible SARfilter ADC Receiver Summary**

The flexible SARfilter ADC receiver takes advantage of an embedded, reconfigurable analog DT filter in the SAR ADC to reject interferers. This type of filter creates zeros and poles in its frequency response by sampling an input over multiple clock cycles onto different capacitors and then charge-sharing the stored charge. The frequency response of the embedded filter is programmable by changing the FIR tap length and coefficients and the sampling rate of the filter. FIR selective-sampling reduces the conversion rate of the ADC, so half of the CDAC is duplicated to enable support of interleaved sampling and SAR conversion processes. The SARfilter ADC together with a RF front-end that supports a wide range of carrier frequencies (section 4.1.1) creates a flexible wireless receiver that supports communication standards that operate at different carrier frequencies and channel bandwidths.

## CHAPTER 3

### Discrete-Time Spectrum-Sensing and Adaptive Filtering

#### 3.1 Spectrum-Sensing Receiver

Filters in receivers are typically designed to reject worst case interferers. When a receiver operates in an environment where interferers are not present or are relatively weak, the implementation and operation of this filter unnecessarily consumes area and power. Instead, we propose spectrum-adaptive (SA) filtering that combines a DT spectrum-sensing (SS) system [22] with a simpler SS-guided reconfigurable notch filter. Figure 3–1 shows a simplified high-level block diagram of the spectrum-sensing receiver, which consists of an LNA, direct down-conversion mixer, TIA, spectrum-adaptive filtering system (blue), amplifiers, and a filtering SAR ADC. Spectrum-adaptive filtering uses analog DT spectrum-analysis filters and simple DSP to scan for strong interferers from 15MHz to 70MHz and automatically adjust the frequency of two closely spaced

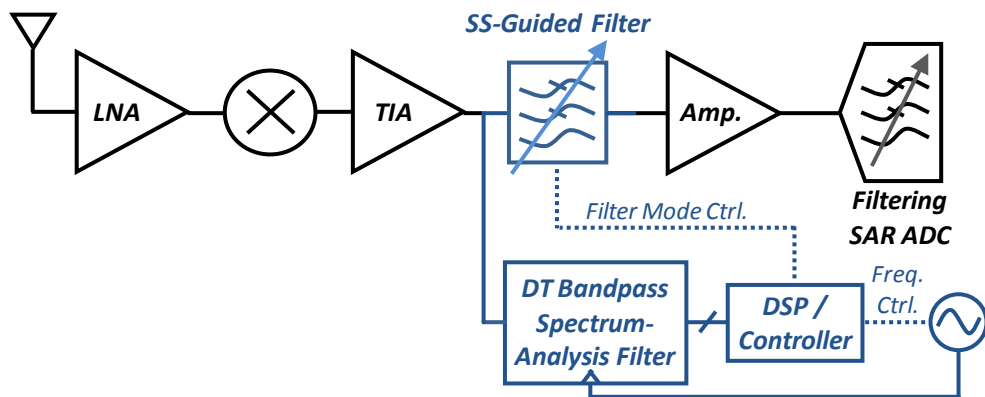


Figure 3–1. Simplified high-level block diagram of the spectrum-sensing receiver architecture. The spectrum-adaptive filtering system is highlighted in blue.

analog DT FIR zeros of the SS-guided filter to attenuate the strongest detected interferer. A calibrated on-chip ring oscillator accurately defines the spectrum-analysis filter's passband frequency and enables digital frequency control. Filtering in the analog DT domain eliminates high-speed, high-resolution ADCs that digital spectrum-analysis would otherwise require. Analog DT filters [23], which consist of switches and capacitors (i.e. no op-amps), are also advantageous because switches function well in nanometer CMOS and the filter response is well-defined by capacitor matching and clocking and is independent of process variation.

### **3.2 Benefits of Targeted Spectrum-Adaptive Filtering**

Spectrum sensing and adaptive filtering enables more energy and area efficient filtering of strong, time and frequency varying interferers than conventional, fixed filtering. Figure 3–2 compares possible conventional and spectrum-adaptive *analog* DT filter configurations in a wireless receiver. The dark gray bar represents a wanted signal, the striped bars represent strong interferers, the dotted bar represents weak interferers, the light gray line plots the frequency response of an analog DT FIR filter, and the blue circles indicate the locations of the FIR zeros. Analog DT filters are charge-domain FIR and IIR filters that are implemented by sampling onto different sections of a capacitor bank over multiple cycles and passively charge-sharing the sampled charge. In the conventional filtering case (top of Figure 3–2), the filter implements a fixed frequency response. Therefore, the filter must create a large number of zeros in order to attenuate potential interferers across the entire frequency band of interest. This example plots an 18-tap FIR filter. In the spectrum-adaptive filtering case (bottom of Figure 3–2), a robust,

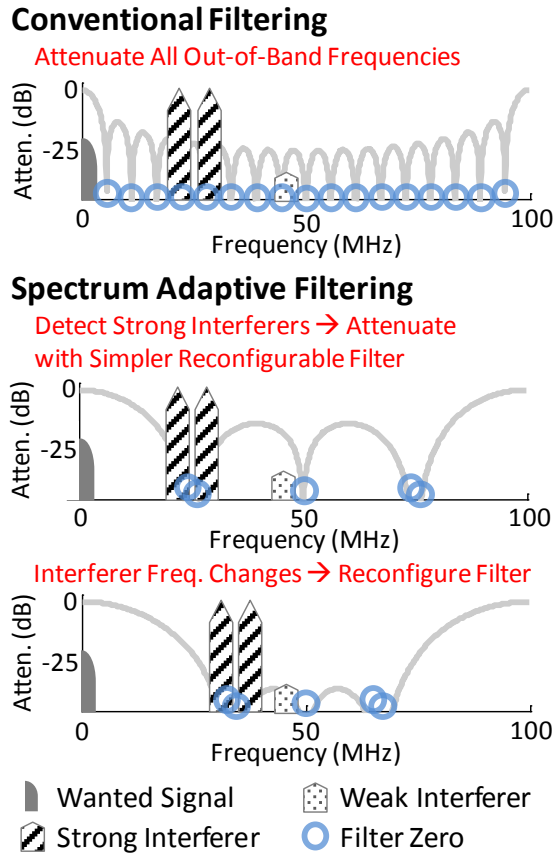


Figure 3–2. Diagram of conventional filtering (top) compared to spectrum-adaptive filtering (bottom). A conventional filter needs to attenuate all out-of-band frequencies with a relatively complex filter (18-tap analog DT FIR shown). A spectrum-adaptive filter uses spectrum-sensing to detect the largest interferers and configures a simpler filter (6-tap shown) to attenuate these interferers. The power and area savings scale approximately with the tap length.

scaling-friendly, and low-power DT spectrum-sensing system detects the frequency of strong interferers. A digital controller processes this information and configures the FIR zero locations of a simpler 6-tap FIR filter to coincide with the interferer and achieve equivalent or better rejection. When the frequency of the interferer changes, as shown in the bottom plot of Figure 3–2, the spectrum-adaptive filter reconfigures its zero locations to continue to optimally reject the interferer. The weak interferers, which do not cause distortion issues when amplified, are allowed to pass through this filtering stage without

significant attenuation and are filtered further down the receive chain. The area and power of an analog DT filter scales approximately with the FIR tap length, so the spectrum adaptive filter achieves approximately three times smaller area and lower power usage with the example filters shown in Figure 3–2.

### 3.3 Bandpass Subsampling for Spectrum-Analysis

The DT bandpass spectrum-analysis filter in Figure 3–1 performs bandpass subsampling, which refers to the process of sampling a high-frequency (i.e. IF or RF) bandpass signal at a sampling rate proportional to its passband bandwidth, instead of proportional to the frequency of its highest-frequency content. For a signal with bandwidth of less than  $B$  that is properly positioned in frequency [24], uniform sampling only needs to occur at a rate of  $2B$  in order to achieve alias-free down-conversion of the signal.

We adapt bandpass subsampling for interferer detection in our analog DT spectrum-

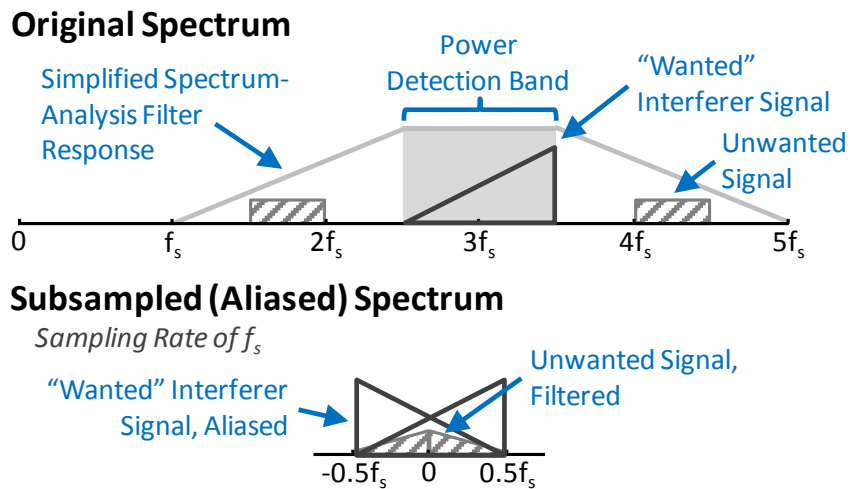


Figure 3–3. Bandpass subsampling refers to sampling at a rate proportional to a signal’s passband bandwidth. A bandpass filter first attenuates the out-of-band signals before subsampling occurs (top). The power contained within the subsampled signal (bottom) approximates the original signal well, even when aliasing occurs, as long as the filter adequately attenuates out-of-band signals.

analysis filter by relaxing the bandwidth and frequency positioning requirements, since measuring the power within select bands for spectrum-sensing purposes does not require alias-free subsampling. Figure 3–3 shows a simplified diagram of a possible spectrum of interest. The dark gray triangle represents a wanted<sup>5</sup> interferer signal that lies within a power detection band ranging from  $2.5f_s$  to  $3.5f_s$ , within which we want to measure signal power. The striped bars represent unwanted signals outside of the detection band. In order to measure the power of the wanted interferer signal, we first attenuate signals outside of the detection band with a bandpass “spectrum-analysis filter” (light-gray line). Then we subsample the signal at a rate of  $f_s$ , which causes the signal at higher frequencies to fold into the frequencies  $-0.5f_s$  to  $0.5f_s$ . Although subsampling aliases the wanted interferer signal and corrupts the signal’s content, it accurately down-converts the signal’s power to baseband. The partially attenuated unwanted signal also folds into the frequencies  $-0.5f_s$  to  $0.5f_s$  and introduces error in the measured power. This error is acceptable as long as the bandpass filter attenuates the power of the signals outside of the detection band to less than the minimum desired power measurement resolution.

### 3.4 Calculation of Power from the Output of the Spectrum-Analysis Filter

For the purposes of spectrum-sensing, we use simple DSP to calculate the average signal power,  $P_{avg}$ , at the bandpass filtered discrete-time outputs of the I and Q spectrum-analysis filters. The outputs varies with time, as a function of the original IF waveform and how it aliases to baseband during the subsampling process. The power of a DT signal,  $x[n]$ , is defined as [25]

---

<sup>5</sup> “Wanted” here refers to the interferers that lie within the power detection passband.



$$P_{avg} = \lim_{N \rightarrow \infty} \frac{1}{2N + 1} \sum_{n=-N}^N |x[n]|^2. \quad (3.1)$$

For simplicity, we assume that  $x[n] = 0$  for  $n \leq 0$ . Also,  $x[n]$  represents the outputs of the I and Q channels of the spectrum-analysis filter,  $x_I[n]$  and  $x_Q[n]$ , respectively, so we can rewrite (3.1) as

$$P_{avg} = \lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=1}^N (x_I[n]^2 + x_Q[n]^2). \quad (3.2)$$

Eq. (3.2) states that the average power,  $P_{avg}$ , contained within the power detection band at IF is the sum of the squared I and Q outputs of the spectrum-analysis filter, divided by the number of samples in the sum,  $N$ , for  $N$  approaching infinity. The accuracy of  $P_{avg}$  improves as  $|x[n]|^2 = x_I[n]^2 + x_Q[n]^2$  is accumulated for more samples, but a good estimate of power can be calculated even for practical accumulation lengths. We define  $P_{avg,N}$  as the average power when  $|x[n]|^2$  is accumulated over a finite number of samples,  $N$ :

$$P_{avg,N} = \frac{1}{N} \sum_{n=1}^N (x_I[n]^2 + x_Q[n]^2). \quad (3.3)$$

The necessary number of samples to accumulate depends on the modulation, bandwidth, and center frequency of the signals contained within the power detection passband. The quantity  $|x[n]|$  is the complex envelope,  $e[n]$ , of the signal at the output of the spectrum analysis filter. If a signal is constant-envelope modulated (e.g. FM, QPSK, MSK, etc.), has bandwidth less than the bandwidth,  $B$ , of the spectrum-analysis filter, and has proper carrier frequency alignment relative to the subsampling rate to prevent aliasing, the complex envelope,  $e[n]$ , is constant and  $P_{avg}$  calculation only needs to include one sample to be accurate (i.e.  $P_{avg,1} = P_{avg}$ ). But if the signal, is amplitude

modulated (e.g. AM, QAM, etc.), has bandwidth exceeding B, or aliases during subsampling,  $e[n]$  varies with time and  $P_{avg}$  calculation requires summation over many samples. We define  $err_P[N]$  to quantify the percentage error between  $P_{avg,N}$  and  $P_{avg}$  as a function of N:

$$err_P[N] = \frac{|P_{avg,N} - P_{avg}|}{P_{avg}} \times 100. \quad (3.4)$$

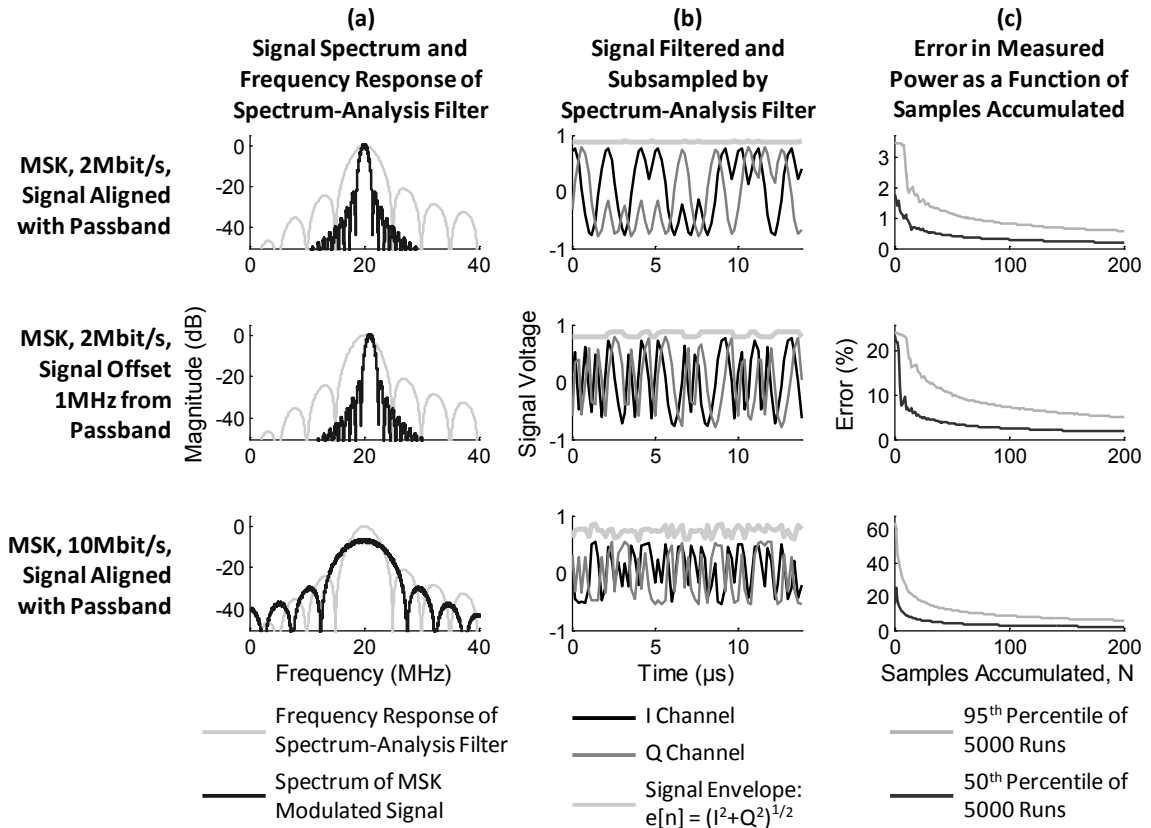


Figure 3–4. Column (a) plots the IF spectrum of three different MSK modulated interferers (black) and the frequency response of an example spectrum-analysis filter (gray) centered at 20MHz. Column (b) plots the filtered and sub-sampled I/Q signals at the output of the spectrum-analysis filter and their complex envelope. Column (c) plots the 50<sup>th</sup> and 95<sup>th</sup> percentile boundaries of the error percentage (3.4) of the average measured signal power, as a function of the number of samples accumulated, N, over 5000 sets of randomized data in the MSK modulated interferer signal.

As examples, Figure 3–4 illustrates the operation of the spectrum-analysis filter and the resulting  $err_P[N]$  for three different signals. The 1<sup>st</sup> and 2<sup>nd</sup> signals, plotted in the 1<sup>st</sup> and 2<sup>nd</sup> rows, are MSK modulated with bit rate,  $r_b$ , of 2MS/s and center frequencies,  $f_c$ , of 20MHz and 21MHz, respectively. The 3<sup>rd</sup> signal, plotted in the 3<sup>rd</sup> row, is MSK modulated with  $r_b$  of 10MS/s and  $f_c$  of 20MHz. Column (a) overlays the spectrum of these MSK signals (black) and the frequency response of a bandpass spectrum-analysis filter (gray) with a subsampling rate of 5MS/s and  $f_c$  of 20MHz. Section 3.6 below describes the filter’s implementation. The spectrum of the first two signals lies mostly within the filter’s bandwidth, but only the 1<sup>st</sup> of the two has a center frequency that allows subsampling to occur without aliasing. The spectrum of the 3<sup>rd</sup> signal exceeds the filter’s bandwidth, so the “skirts” of the signal alias onto the main lobe after subsampling. Column (b) plots the bandpass filtered and subsampled I and Q channels of the MSK signals (i.e. the output of the spectrum analysis filter) and their complex envelope,  $e[n]$ . As expected,  $e[n]$  of the 1<sup>st</sup> signal remains nearly constant and  $e[n]$  of the other two signals varies with time. Column (c) plots the 50<sup>th</sup> and 95<sup>th</sup> percentile boundaries of  $err_P[N]$ <sup>6</sup> (3.4), simulated over 5000 sets of randomized MSK-modulated data. Measurement of the average power of the 1<sup>st</sup> signal, whose spectrum remains accurately defined after filtering and subsampling, achieves 95<sup>th</sup> percentile  $err_P$  of less than 3.5% with only 1 accumulation (i.e.  $N=1$ ). The 2<sup>nd</sup> and 3<sup>rd</sup> signals, however, exhibits significant measurement error for low  $N$  and do not achieve 95<sup>th</sup> percentile  $err_P$  of less than 10% until  $N$  exceeds 51 and 74, respectively. Increasing  $N$  further results in diminishing improvements to the measurement accuracy and also comes at the cost of increasing the measurement time. These simulations confirm that spectrum-sensing based

---

<sup>6</sup> The simulation assumes that  $P_{avg} \approx P_{avg,5000}$  when calculating  $err_P[N]$ .

on DT bandpass subsampling and digital  $P_{avg}$  calculation achieves a moderate level of measurement accuracy that is sufficient for spectrum-adaptive filtering of large interferers. We limit  $N$  to 64 in our prototype, which achieves 95<sup>th</sup> percentile  $err_P$  of 1.0%, 9.0%, and 10.7% with the 1<sup>st</sup>, 2<sup>nd</sup>, and 3<sup>rd</sup> signals in this example, respectively.

### 3.5 Accurate Frequency Tuning of the Spectrum-Analysis Filter

We introduce DT spectrum-analysis filtering that achieves an easily and accurately tunable center frequency of the power detection passband,  $f_{PB}$ . The passband is always located at *one-tenth* of a clocking frequency,  $f_{s,osc}$ , that an on-chip ring-oscillator generates. This fixed relationship between  $f_{s,osc}$  and  $f_{PB}$  allows a digital spectrum-sensing controller to reliably control the passband’s center frequency by controlling the ring-oscillator’s frequency. Moreover, the oscillator’s frequency is accurately tunable by setting digital frequency-control inputs on 7-bit capacitive DACs (CDACs) that load the

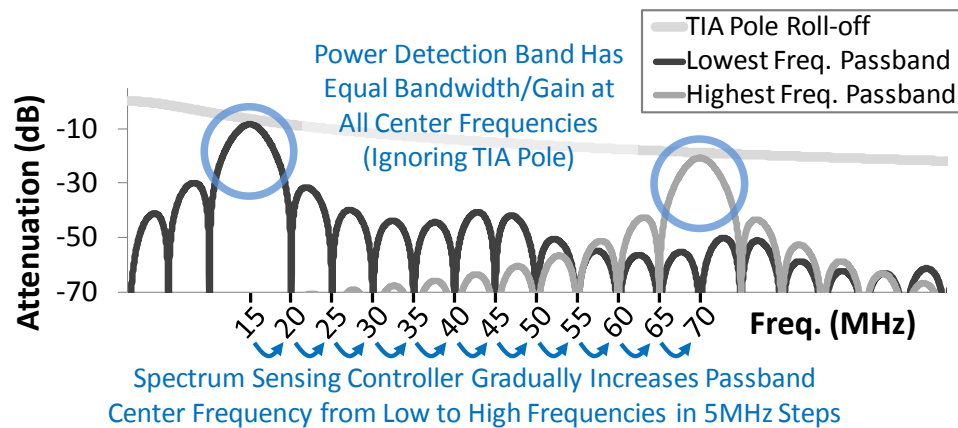


Figure 3–5. Plots of the bandpass spectrum-analysis filter when configured to the lowest and highest center frequencies, 15MHz and 70MHz, respectively. A digital controller performs spectrum-sensing with this filter by sweeping the passband’s center frequency from 15 to 70MHz and inspecting the in-band power at each frequency. Aside from the attenuation caused by the TIA pole, the passband has equal bandwidth and gain at all center frequencies.

outputs of the inverters in the oscillator. We calibrate the CDAC input value that sets each desired oscillation frequency by measuring  $f_{s,osc}$  off-chip and storing the associated frequency-control word into an on-chip look-up table. Figure 3–5 plots the frequency response of the spectrum-analysis filter when  $f_{PB}$  is set to its lowest and highest frequencies of 15MHz and 70MHz, respectively. In order to perform spectrum-sensing across the 15 to 70MHz band, the controller gradually increases  $f_{PB}$  in 5MHz steps (by increasing  $f_{s,osc}$ ). At each center frequency, the filter’s bandpass frequency response isolates the power of the interferers that lie within its passband and subsamples it to baseband, where it is digitized for  $P_{avg,N}$  (3.3) calculation in the digital domain. Since  $f_{PB}$  is one-tenth of  $f_{s,osc}$ , typical calibration inaccuracy or open-loop drift of  $f_{s,osc}$  of less than 3MHz (at constant operating temperature) results in a 10x smaller frequency offset of the passband.

In the receive chain, spectrum-sensing and the SS-guided notch filter are located after a mixer and a TIA that loads the mixer. The controller adjusts the spectrum-analysis filter’s parameters at each center frequency to ensure that the passband’s bandwidth and gain remains constant, when disregarding the attenuation of the TIA pole, as shown in Figure 3–5. The gain of the spectrum-analysis filter’s detection band decreases with increasing frequencies when including the attenuation of the TIA pole. This decrease is desirable, because the signals that reach the input of the auxiliary spectrum-sensing path should mirror those that enter the SS-guided notch filter. This way, spectrum-adaptive filtering correctly identifies and attenuates the largest interferer that would otherwise create distortion in the amplifiers that follow the SS-guided notch filter.

### 3.6 Creation of the DT Spectrum-Analysis Passband

Figure 3–6 shows one of the identical I and Q branches of the four-stage DT spectrum-analysis filter and an example frequency response for each stage when  $f_{s,osc}$  is 250MHz. The four filtering stages together generate notches and poles that create a distinct power detection passband at  $f_{s,osc}/10$ . Table 3–1 summarizes the sampling rates and frequency

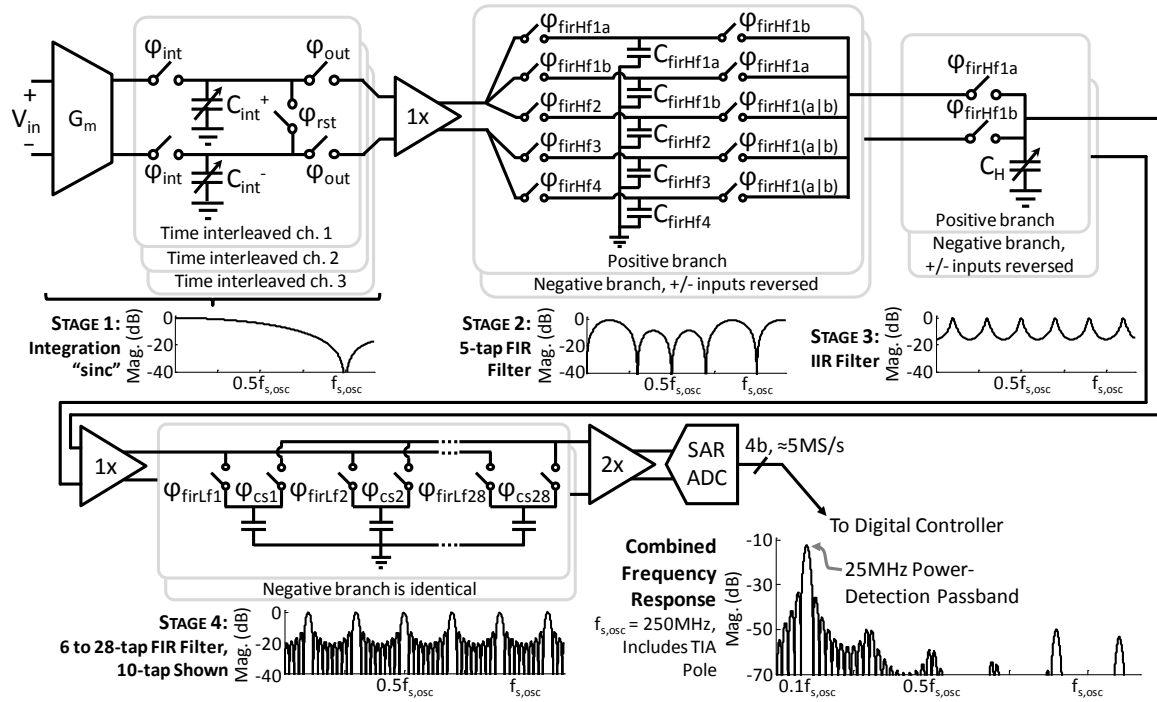


Figure 3–6. One of the identical I and Q branches of the four-stage DT bandpass spectrum-analysis filter, including the filter response of each stage. The combined response (lower-right plot) shows that the spectrum-analysis filter and the TIA pole together create a distinct power detection passband.

Stage	Rate In	Rate Out	Frequency Response
1	$f_s$	$f_s$	sinc-like, notches at $n \cdot f_s$ , $n=1,2,3\dots$
2	$f_s$	$f_s/5$	zeros at DC, $0.3f_s$ , $0.5f_s$ , $0.7f_s$ , $f_s\dots$
3	$f_s/5$	$f_s/5$	poles at $0.1f_s$ , $0.3f_s$ , $0.5f_s\dots$
4	$f_s/5$	$f_s/140$ to $f_s/30$ ,	zeros at 0, 5, 10MHz... except at $0.1f_s$ , $0.3f_s$ , $0.5f_s\dots$
Combined	$f_s$	always $\approx 5\text{MS/s}$	power detection passband at $f_s/10$

Table 3–1. Input and output rates and frequency response characteristics of the spectrum-analysis filter.

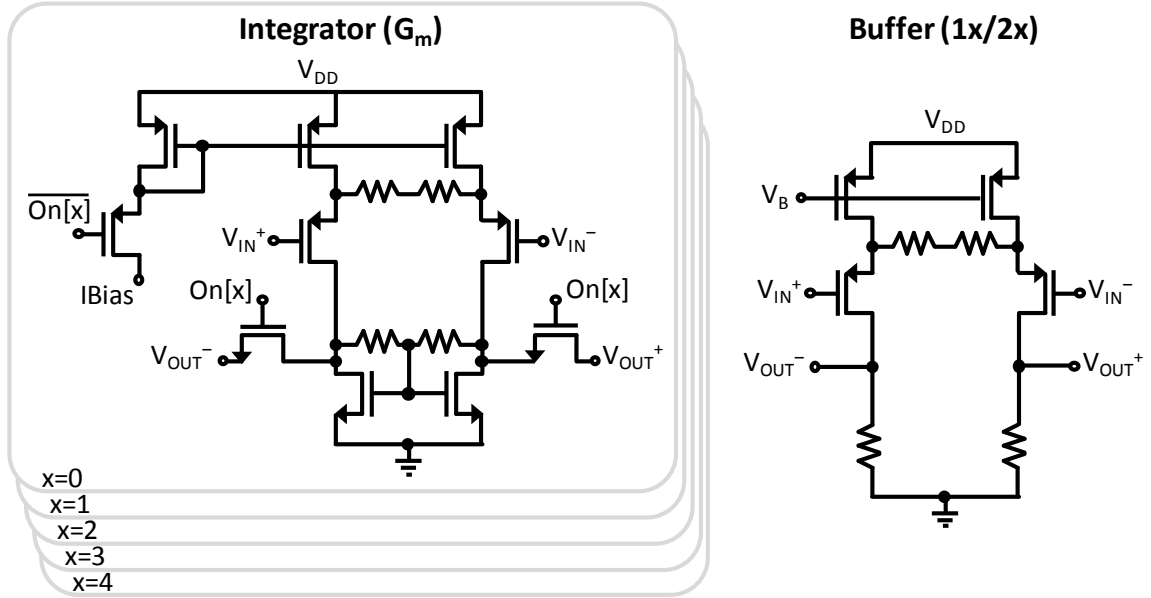


Figure 3–7. The integrator and the buffers in the spectrum-analysis filter are simple source-degenerated differential pairs. The integrator consists of five identical stages in parallel, each of which can be turned on or off to adjust the total transconductance.

responses of the four stages. The  $G_m$  stage and the buffers (i.e. 1x, 2x) between the stages are all simple, open-loop differential pairs with source degeneration, as shown in Figure 3–7. The  $G_m$  stage consists of five differential pairs in parallel, each of which can be enabled or disabled by toggling its corresponding  $On[x]$  bit, in order to change the total transconductance.

The cascade of the first three stages in the spectrum-analysis filter (Figure 3–6) creates a well-defined power detection passband at  $0.1f_{s,osc}$ . In the 1<sup>st</sup> stage, integration sampling creates a lowpass sinc-like response with notches at all multiples of  $f_{s,osc}$  and the normalized transfer function

$$H_{int}(f) = sinc\left(\frac{f}{f_{s,osc}}\right) = \frac{\sin\left(\pi \frac{f}{f_{s,osc}}\right)}{\pi \frac{f}{f_{s,osc}}} \quad (3.5)$$

Integration sampling requires resetting of  $C_{int}^{+/-}$  before sampling occurs and additional time to transfer the sampled charge to the capacitors in the 2<sup>nd</sup> stage (Figure 3–6).<sup>7</sup> Therefore, we time-interleave three identical channels to permit simultaneous sampling, outputting, and resetting. The 5-tap FIR filter of the 2<sup>nd</sup> stage creates zeros at DC,  $0.3f_s$ ,  $0.5f_s$ ,  $0.7f_s$ ,  $f_s$ ... and the IIR filter of the 3<sup>rd</sup> stage creates poles at  $0.1f_s$ ,  $0.3f_s$ ,  $0.5f_s$ ..., as shown in Figure 3–6 and summarized in Table 3–1. Figure 3–8 plots the cascaded responses of the first three stages of the spectrum-analysis filter, to emphasize how these filters create a distinct power detection passband at  $f_{PB} = 0.1f_{s,osc}$ . Pole-zero cancellation between the 2<sup>nd</sup> and 3<sup>rd</sup> stages (black line) leaves the wanted lowest frequency pole of the IIR filter intact and rejects the 2<sup>nd</sup>, 3<sup>rd</sup>, and 4<sup>th</sup> lowest frequency poles. The 5<sup>th</sup> and 6<sup>th</sup> poles also remain intact, because the frequency response of the DT filter repeats at the sampling rate,  $f_{s,osc}$ . Integration sampling creates notches at multiples of  $f_{s,osc}$  (thick light-

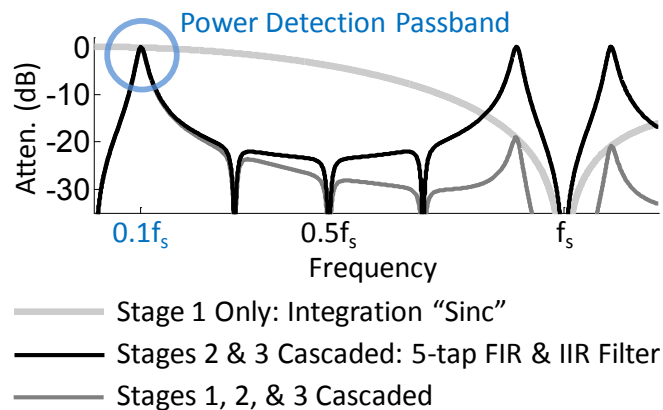


Figure 3–8. The frequency responses of different cascaded combinations of the spectrum-analysis filter stages. Pole-zero cancellation between stages 2 and 3 create a power detection passband at  $0.1f_s$  and undesirable passbands at  $nf_s \pm 0.1f_s$ ,  $n=1,2,3$ .... The integration “sinc” of the 1<sup>st</sup> stage attenuates the undesirable passbands, as shown in the cascaded response of stages 1, 2, and 3.

<sup>7</sup> If  $C_{int}^{+/-}$  is not reset at the beginning of each integration cycle, the charge samples accumulate and result in the creation of an FIR filter with equal tap coefficients [4]. While we considered using this version of analog DT FIR filtering to create the 2<sup>nd</sup> filter stage in Figure 3–6, implementing precise non-unity filter taps by relative sizing of capacitors is more robust than by relative sizing of transconductances.



gray line), which attenuate these unwanted high-frequency poles. As a result, the cascade of the three filtering stages (medium-gray line) exhibits a sharp bandpass response centered at  $0.1f_{s,osc}$ . In addition, the TIA pole (response not shown) further attenuates the unwanted high-frequency passbands and significantly reduces aliasing of high-powered interferers located near these passbands to  $0.1f_{s,osc}$ .

The FIR and IIR filters together implement the transfer function

$$H_{stg23}(z) = \frac{\frac{1}{1+x_{IIR}}(0.31+0.19z^{-1}-0.19z^{-3}-0.31z^{-4})}{1+\frac{x_{IIR}}{1+x_{IIR}}z^{-5}}, \quad (3.6)$$

$$\text{where } x_{IIR} = 11.86 \times 10^{-9}f_{s,osc} - 0.34,$$

or equivalently,

$$y[n] = \frac{1}{1+x_{IIR}} (0.31x[n] + 0.19x[n-1] - 0.19x[n-2] - 0.31x[n-3]) - \frac{x_{IIR}}{1+x_{IIR}} y[n-5]. \quad (3.7)$$

The 1<sup>st</sup> through 4<sup>th</sup> terms within the parenthesis in the numerator of (3.6) correspond to the 1<sup>st</sup>, 2<sup>nd</sup>, 4<sup>th</sup>, and 5<sup>th</sup> taps (the 3<sup>rd</sup> tap is 0), respectively, of the 2<sup>nd</sup> stage 5-tap FIR filter of Figure 3–6. The input is sampled onto capacitors  $C_{firHf1a/b}$  to  $C_{firHf4}$  in clock periods 1, 2, 4, and 5, respectively, and then the capacitors are charge-shared together to create a filtered sample of charge. Therefore, each  $C_{firHf}$  capacitor is sized in proportion to the weight of its corresponding filter tap coefficient. This filter creates zeros at DC,  $0.3f_{s,osc}$ ,  $0.5f_{s,osc}$ ,  $0.7f_{s,osc}$ ,  $f_{s,osc}$ .... Since sampling takes five clock cycles, this filter also decimates the sampling rate by 5x. The top two capacitors,  $C_{firHf1a}$  and  $C_{firHf1b}$ , shown in the 2<sup>nd</sup> stage of Figure 3–6 both implement the 1<sup>st</sup> filter tap, which allows one capacitor to begin input sampling for the next filtering cycle while the other charge-shares. The negative coefficients in the FIR filter are implemented by sampling the negative input onto the

positive half-circuit (and vice versa) through the  $\phi_{firHf3}$  and  $\phi_{firHf4}$  connections (2<sup>nd</sup> stage of Figure 3–6). The polarity to the input of the negative half-circuit is reversed. The terms in the denominator of (3.6) represent the 3<sup>rd</sup> stage IIR filter, which is implemented by connecting the IIR history capacitor,  $C_H$ , to the FIR capacitors when they charge-share. This combines a fraction of the FIR filter’s current output with past outputs and creates poles at  $0.1f_{s,osc}$ ,  $0.3f_{s,osc}$ ,  $0.5f_{s,osc}$ .... The  $z^{-5}$  delay reflects the decimated  $f_{s,iir} = f_{s,osc}/5$  charge-sharing rate between the FIR and IIR filters. The polarity of the connection between the two filters reverses in each subsequent charge-share to reflect subtraction of the  $y[n-5]$  term in (3.7) (or equivalently addition of the  $z^{-5}$  term in (3.6)); the  $\phi_{firHf1a}$  and  $\phi_{firHf1b}$  connections in the 3<sup>rd</sup> stage implement this reversal. Similar to the FIR filter, the polarity to the input of the negative half-circuit is reversed. We fix the output rate of the spectrum-analysis filter at  $\approx 5$ MS/s. This slow rate enables power-efficient, low-speed analog-to-digital conversion and digital power calculation (section 3.4 above). We accomplish this by implementing a variable rate FIR decimation filter in the 4<sup>th</sup> stage of the spectrum-analysis filter (Figure 3–6) to reduce the sampling rate to  $\approx 5$ MS/s for all  $f_{s,osc}$ . This filter implements the transfer function

$$H_{stg4}(z) = \frac{1}{n_{tapFirLf}} \left( 1 + z^{-1} + z^{-2} + z^{-3} + \dots + z^{-(n_{tapFirLf}-1)} \right), \quad (3.8)$$

where  $n_{tapFirLf}$  is the number of FIR taps and ranges from 6-taps for  $f_{s,osc}$  of 150MHz (i.e. 15MHz passband) to 28-taps for  $f_{s,osc}$  of 700MHz (i.e. 70MHz passband). For example, for  $f_{s,osc}$  of 250MHz shown in Figure 3–6, the 2<sup>nd</sup> stage decimates the rate 5x, from 250MS/s to 50MS/s, and the 4<sup>th</sup> stage decimates the rate an additional 10x in 10-tap mode, from 50MS/s to 5MS/s. Stage 4 of Figure 3–6 shows the frequency response of

this filter when it is set to the 10x decimation, 10-tap mode.<sup>8</sup> Because the decimation filter's tap length scales with  $f_{s,osc}$ , its passband lobe at  $f_{PB}=f_{s,osc}/10$  exhibits equal bandwidth for all  $f_{s,osc}$ . Furthermore, as  $f_{s,osc}$  (and  $f_{PB}$ ) increases, the controller decreases  $C_{int}^{+/-}$  in the 1<sup>st</sup> stage to keep the gain constant, since the integration gain scales proportionally with the integration period. The controller also increases  $C_H$  in the 3<sup>rd</sup> stage to keep bandwidth constant, since the IIR bandwidth scales proportionally with  $f_{s,iir}=f_{s,osc}/5$ . In the lower-right corner of Figure 3–6, a plot of the frequency response of the spectrum-analysis filter, with  $f_{s,osc}$  set to 250MHz, cascaded with the TIA pole shows that the combined attenuation strongly rejects all frequencies outside of the power detection passband at 25MHz.

### 3.7 Digitally-Controlled Spectrum-Sensing and Adaptive Filtering

The spectrum-adaptive filtering system uses the digital controller to interpret the output of the spectrum-analysis filter and select the optimal mode of a SS-guided reconfigurable notch filter (Figure 3–1). First, a 4-bit,  $\approx 5$ MS/s SAR ADC in each of the I and Q channels of the filter (Figure 3–6) digitizes the bandpass filtered output. The sampling rate is approximate because the on-chip oscillator that clocks the ADC is frequency calibrated but not frequency locked. The controller, which is clocked by an accurate, external clock source, oversamples the ADC output to bridge the two clock domains and then calculates  $N \cdot P_{avg,N}$  (3.3), for selectable  $N \leq 64$ , to measure the average interferer power contained within each passband. It makes this measurement for every

---

<sup>8</sup> The frequency response shown for the 4<sup>th</sup> stage in Figure 3–6 is bandpass with passbands at  $f_{s,iir}/2 = f_{s,osc}/10$ , but (3.8) describes a lowpass FIR filter. This is because alternating reversals of the sampling polarity in the 3<sup>rd</sup> stage IIR filter is equivalent to multiplying by  $e^{j\pi n} = \{-1, 1, -1, 1, \dots\}$ , which frequency shifts the signal by  $\pi = f_{s,iir}/2$ . Stage 4 plots the frequency response of the FIR decimation filter *with respect to the input* to the spectrum-analysis filter. In isolation, the FIR decimation filter would exhibit a lowpass response.

frequency bin from 15 to 70MHz, in 5MHz steps, and then directs the SS-guided notch filter to reject the interferer bin with the greatest measured power.

### 3.8 Capacitor Mismatch and Sampling Jitter

The power detection passband of the spectrum-analysis filter exhibits little variation in its target gain, center frequency, and bandwidth in the presence of capacitor mismatch and sampling clock jitter. We see this robustness to mismatch and jitter in simulations of a simplified model of the filter.<sup>9</sup> Figure 3–9 plots the frequency response of the spectrum-analysis filter for  $f_{s,osc}$  of 500MHz and greatly exaggerated capacitor mismatch of 0.05 and sampling clock jitter of 30ps. The thick light gray line plots the ideal frequency response, onto which colored lines overlay plots of 50 different non-ideal configurations. The power detection passband remains well defined, although non-idealities limit attenuation outside of the passband to  $\approx 50$ dB and imperfect pole-zero cancellation at 150,

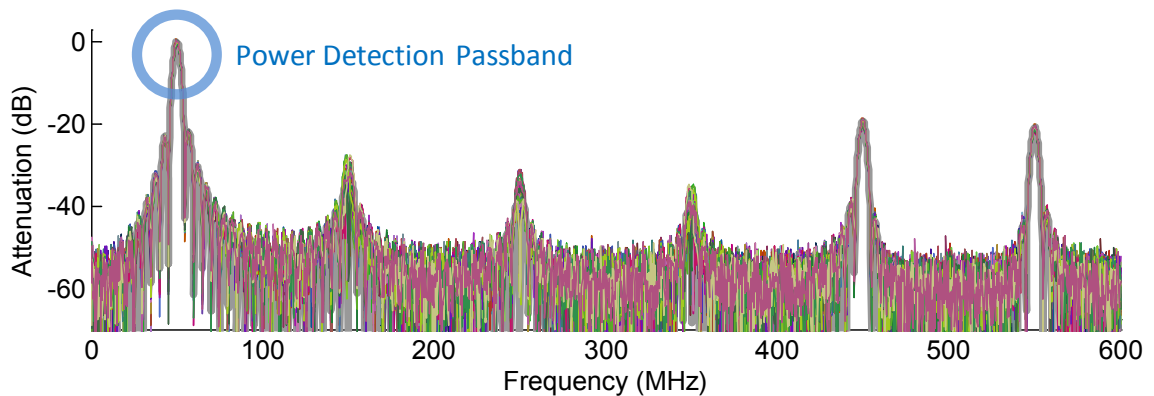


Figure 3–9. Frequency response of the spectrum-analysis filter when set to a center frequency of 50MHz. The gray line plots the response when the capacitors and sampling clocks are ideal and the colored lines overlay 50 different non-ideal configurations with  $\sigma_{\Delta C/C} = 0.05$  and  $\sigma_{\text{jitter}} = 30$ ps. The power detection passband remains well-defined in the presence of non-idealities.

<sup>9</sup> The model makes the following simplifications: (1) omits the effect of time interleaving and instead assumes that outputting and resetting happens instantaneously, (2) omits sampling non-idealities aside from jitter, (3) applies the stated mismatch to each capacitor shown in Figure 3–6, regardless of size.

250, and 350MHz results in 6-8dB less attenuation than expected. Table 3–2 summarizes the effect of mismatch and jitter on passband gain, center frequency, and bandwidth, measured over 500 different non-ideal configurations. Mismatch ranges from 0.01 to 0.10 and jitter ranges from 10ps to 50ps. In all cases, mismatch and jitter negligibly effect the definition of the passband. This is because the frequency of the calibrated on-chip ring-oscillator (i.e.  $f_{s,osc}$ ), not capacitor sizes, sets the passband’s center frequency. It is also because mismatch and jitter most significantly affects the frequency and the depth of the FIR filter zeros. The resulting changes to the frequency response occur in close proximity to those zeros and, therefore, far from the passband.

Controlled Variables		Effect on the Power Detection Passband		
Capacitor Mismatch: $\sigma$ ( $^{\Delta C}/C$ )	Sampling Jitter: $\sigma$ (ps)	Peak Gain, Normalized to Mean: $\sigma$	Center Frequency: mean (MHz) and $\sigma$ (kHz)	-3dB Bandwidth: mean (MHz) and $\sigma$ (kHz)
.01	0	0.0072	50.0375/0	3.2620/10.8
.05	0	0.0360	50.0364/2.2	3.2587/52.2
.1	0	0.0683	50.0358/3.2	3.2528/102.0
0	10	0.0001	50.0373/18.5	3.2597/2.8
0	30	0.0003	50.0462/32.5	3.2569/4.3
0	50	0.0005	50.0496/43.4	3.2527/6.6
.05	30	0.0336	50.0428/33.7	3.2514/49.4

Table 3–2. Effects of mismatch and jitter on the spectrum-analysis filter, simulated over 500 runs.

### 3.9 Spectrum-Sensing Guided Reconfigurable Notch Filter

Spectrum-adaptive filter detects the largest interferer in the 15 to 70MHz range and selects the mode of a reconfigurable *analog* DT notch filter that most strongly attenuates this interferer. As a proof-of-concept of this idea, we integrate a SS-guided, four-mode, 6-tap analog DT FIR filter into the receive chain after the mixer and the TIA that loads the mixer. Figure 3–10 plots the frequency response of the four filtering modes and

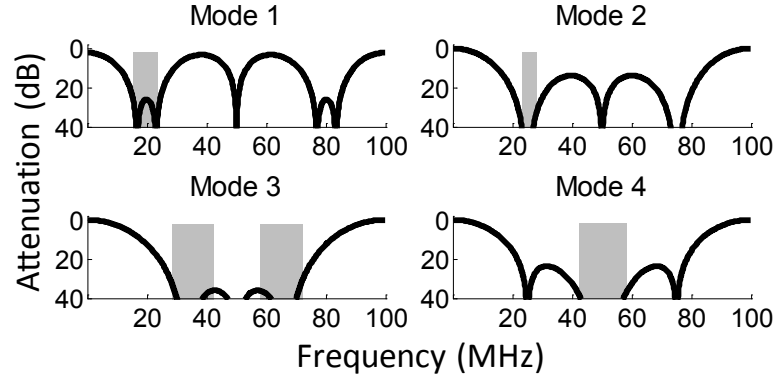


Figure 3–10. Ideal frequency responses of the four modes of the SS-guided notch filter. The gray shaded areas indicate the frequencies that each mode targets. Table 5–2 summarizes the FIR filter coefficients and target attenuation frequencies.

highlights the frequencies that each mode attenuates with gray shading. Each mode, from 1 to 4, targets progressively higher frequencies. Figure 3–11 shows a schematic of a differential half-bank of this filter, which consists of 22 unit capacitors and switches in each time-interleaved channel. Similar to the FIR filters in the spectrum-analysis filter (Figure 3–6), we create this 6-tap FIR filter by sampling over six clock periods onto capacitors of different sizes, formed by grouping together unit capacitors, and then charge-sharing the capacitors. Since a 6-tap filter inherently decimates the rate by 6x, we time-interleave six channels to achieve equal input and output rates. Table 3–3 indicates which sampling switches are turned on during each time step and Table 5–2 summarizes the FIR tap coefficients that each mode implements. Either 16 or 18 unit capacitors are active in the different filter modes, which provide additional flexibility in designing zero locations without increasing the number of unit capacitors in the bank. The switches  $\phi_{samp5}^{+/-}$  and  $\phi_{samp14}^{+/-}$  (Figure 3–11) connect two capacitors to both the positive and negative inputs, in order to implement the negative coefficients in mode 1. The four extra

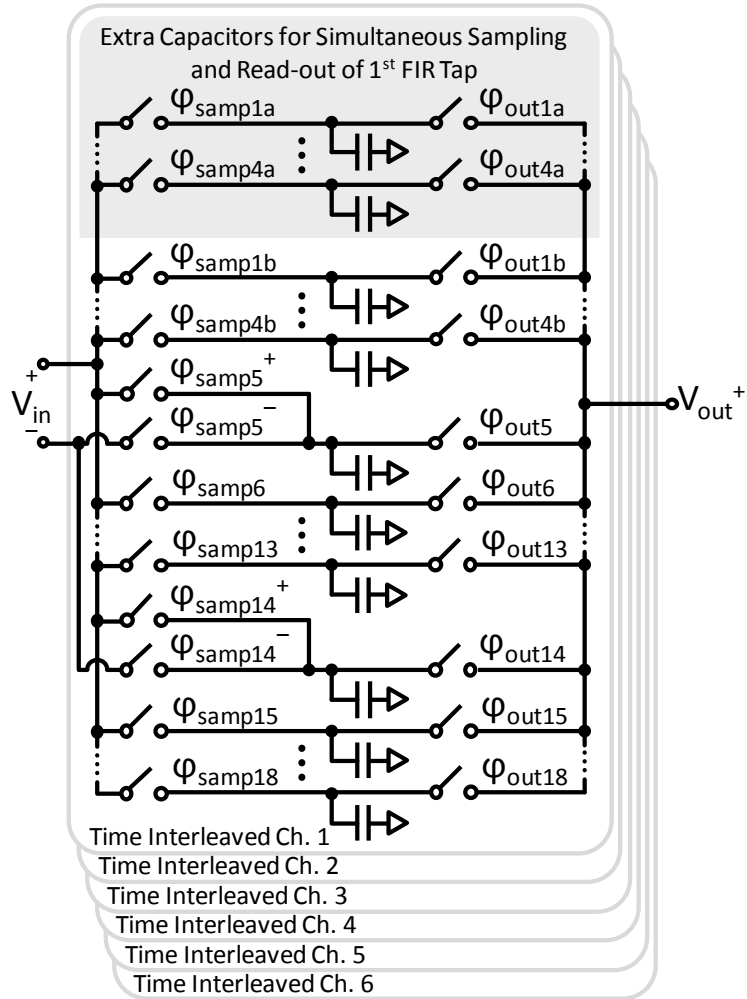


Figure 3–11. Differential half-circuit schematic of the SS-guided reconfigurable DT FIR notch filter. The filter consists of six time-interleaved channels, each with 22 unit capacitors per half-circuit. Two capacitors connect to both  $V_{in}^{+/-}$  to implement negative filter coefficients and four capacitors are duplicated (gray background) to facilitate simultaneous sampling and read-out of the 1<sup>st</sup> FIR tap.

Filter Mode	Time Step					
	1	2	3	4	5	6
1	1-4	5	6-9	10-13	14	15-18
2	2-3	4-5	6-9	10-13	14-15	16-17
3	1	2-4	5-9	10-14	15-17	18
4	2	3-5	6-9	10-13	14-16	17

Table 3–3. Switch numbers of the active sampling switches of the SS-guided notch filter during each time step, as a function of the filter mode. For time step 1, sampling alternates between the “a” and “b” switches.

capacitors shaded in gray, 1a-4a in addition to 1b-4b, allow the “a” capacitors to begin sampling the 1<sup>st</sup> tap of the next filter cycle, while the “b” capacitors charge-share with the other capacitors and vice versa.<sup>10</sup>

### 3.10 Spectrum-Sensing Receiver Summary

The spectrum-sensing receiver integrates a DT spectrum-adaptive filtering system into the receive chain after the mixer and TIA, as shown in Figure 3–1. Spectrum-adaptive filtering combines DT bandpass spectrum-analysis filters with simple digital post-processing to detect the strongest interferer located within the 15 to 70MHz range, and then reject the interferer in real-time with a four-mode SS-guided notch filter. The adaptive filter enables the receiver to respond to a changing operating environment and eliminates the need to over-design a conventional, fixed filter, which would require two to four times more area and power to reject the same interferer.

---

<sup>10</sup> We only interleave the 1<sup>st</sup> filter tap. When the 2<sup>nd</sup> filter tap uses capacitors 2-4 (modes 3 and 4), we arbitrarily sample onto the “b” capacitors and leave the “a” capacitors idle.



## CHAPTER 4

### Receiver Prototypes

#### 4.1 Flexible Wideband Receiver with Reconfigurable Filtering SAR ADC<sup>11</sup>

##### 4.1.1 Architecture

The SARfilter ADC receiver prototype [26] consists of direct conversion I and Q channels, each of which features a SAR ADC with embedded DT filtering (“SARfilter ADC”). The embedded filter achieves more than 30dB of interferer attenuation, even at small frequency offsets from the wanted signal, which simplifies the baseband amplifiers by requiring that they only attenuate at high frequencies.

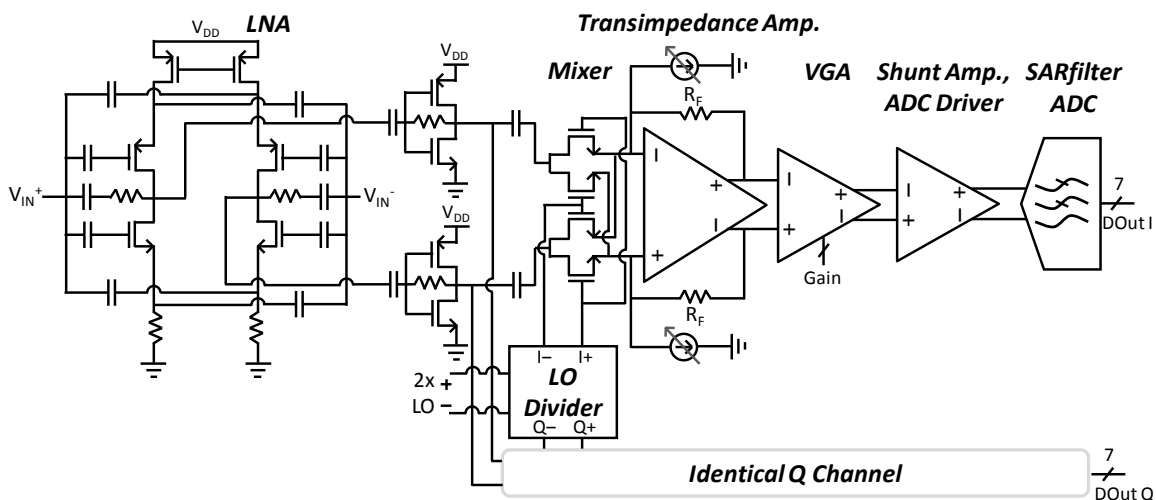


Figure 4–1. Diagram of the SARfilter ADC receiver, consisting of a wideband front-end, 2x LO divider, simple baseband amplifiers, and SAR ADCs with embedded configurable DT filtering.

<sup>11</sup> In this collaborative project, Li Li designed the LNA, mixer, transimpedance amplifier, and baseband amplifiers.

Figure 4–1 shows the receiver architecture. No inductors are used, in order to support a wide range of carrier frequencies, to minimize circuit area, and to maintain compatibility with digital CMOS processes. The wideband LNA [27] with differential inputs, each matched to  $50\Omega$ , achieves low-power and wideband operation by connecting two common-gate and two shunt feedback stages in parallel. Self-biased inverters buffer the output of the LNA and sink current through a passive switching NMOS mixer into a transimpedance amplifier. The use of a passive mixer minimizes flicker noise and second order non-linearity [6], [28]. A 2x LO divider [29] drives the mixers with non-overlapping, differential I/Q LO clocks from a differential 2x LO clock input. Self-mixing of the LO signal and device mismatch in the front-end and baseband amplifiers can create a DC offset. Binary weighted current DACs generate counteracting voltages by sourcing current through the feedback resistors,  $R_F$ , of the transimpedance amplifier. The output of the transimpedance amplifier first enters a variable gain amplifier (VGA) with a five-level digitally-controlled load resistance, which enables the gain to span a range of 25dB. The VGA output drives a shunt-connected amplifier and a pseudo-

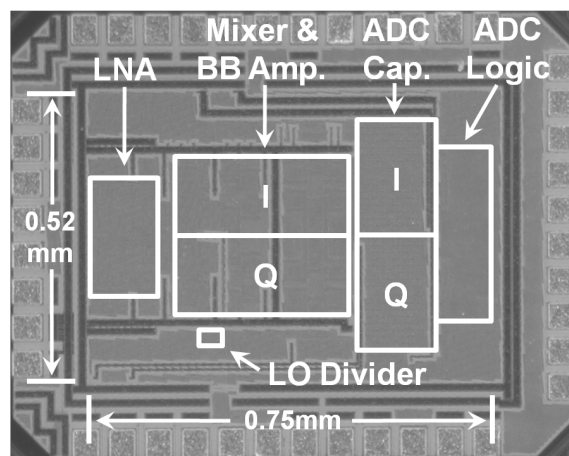


Figure 4–2. Die photo of the SARfilter ADC receiver.

differential ADC driver. The two lowest poles of the amplifiers are set at approximately 6MHz and 30MHz. The SARfilter ADC then filters the output of the driver with an embedded DT filter and outputs a 7-bit digital signal. This filter attenuates interferers by more than 30dB *before* A/D conversion, so unlike a digital domain filter, it does not suffer from quantization error and can perform anti-aliasing. Figure 4–2 shows a die photo of this receiver.

#### 4.1.2 SARfilter ADC

The 7-bit SARfilter ADC filters the signal with an embedded, software-configurable analog DT filter before it performs SAR conversion. As described in Chapter 2, the embedded filter reuses the capacitive DAC (CDAC) of the SAR ADC to implement FIR and IIR filtering, because the CDAC already contains the key components of an analog DT filter—capacitors and switches. Because of this simple switch and capacitor implementation, the filter’s power consumption, sampling rate, and area usage benefit from process scaling and the filter’s frequency response is easily reconfigurable by modifying the digital clocks that drive the sampling switches. The filter also interleaves

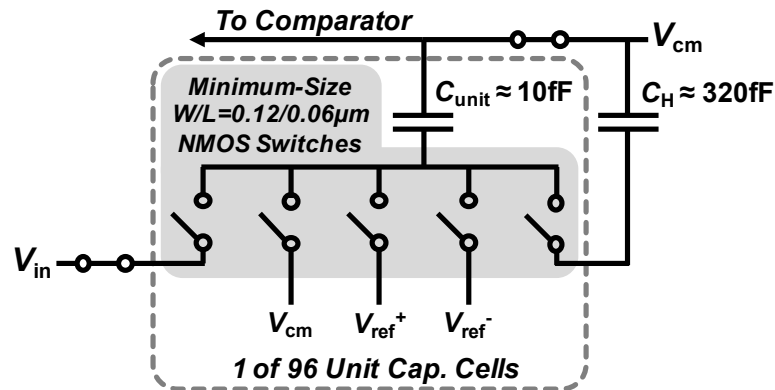


Figure 4–3. Simplified diagram of a unit capacitor cell of the filtering SAR ADC. Minimum-size MiM capacitor and switches are used within the cell. Figure 2–5 shows a more complete schematic.

the sampling and SAR conversion processes, in order to increase the ADC’s conversion rate.

Figure 4–3 shows a simplified schematic of the unit capacitor cell in the CDAC of the SAR ADC. Each differential half-circuit of the ADC contains 96 of these cells, divided equally between the MSBa, MSBb, and LSB banks of section 2.6. Each cell contains a minimum-size  $\approx 10\text{fF}$  MiM capacitor, which is neither  $kT/C$  noise-limited nor mismatch-limited. Each cell also contains five minimum-size switches with W/L of  $0.12\mu\text{m}/0.06\mu\text{m}$ , which is larger than the switch size that 7-bit RC settling accuracy requires. The 96 unit capacitors charge-share with a history capacitor,  $C_H$ , sized 32-times larger, which results in the IIR filtering response shown in Figure 4–4.

The unit capacitors are physically placed in an approximate common-centroid layout, with respect to how the embedded FIR filter typically groups together unit capacitors to form tap coefficient subgroups (section 2.5). This placement mitigates mismatch in the tap coefficient sizes due to process doping gradients. In addition, the corresponding MSBa and MSBb capacitors (i.e.  $\text{MSBa}_1$  and  $\text{MSBb}_1$ ,  $\text{MSBa}_2$  and  $\text{MSBb}_2$ , etc.), which duplicate each other in the interleaved sampling and SAR processes (section 2.6), are physically placed adjacent to each other to reduce mismatch due to distance effects.

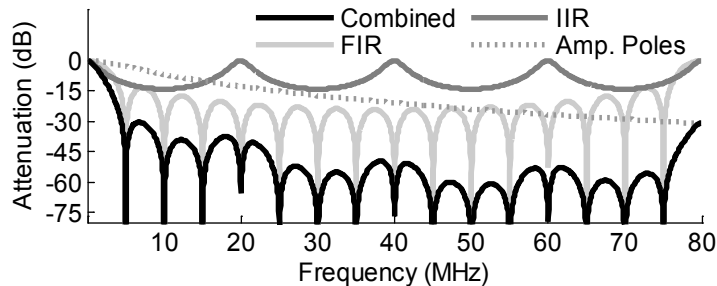


Figure 4–4. An example ideal combined filter response of the SARfilter ADC receiver and its DT FIR/IIR and amplifier pole components. The DT contribution is described by (2.8).

### 4.1.3 Ideal Receiver Filter Response

The complete filter response of the SARfilter ADC consists of DT and baseband amplifier pole components. As an example, Figure 4–4 plots an ideal complete filter response and its components for one of many selectable DT filter configurations. (Figure 5–2 below plots the measured response.) In this example,  $f_{clk}$  is 80MHz and  $f_{conv}$  is 5MS/s. The DT components are described by (2.8), which quantifies an FIR filter with 16 equal tap coefficients and IIR charge-sharing (with  $C_H$ ) after every 4<sup>th</sup> sample. The amplifier poles in the prototype receiver are located at approximately 6MHz and 30MHz and provide high frequency attenuation. The FIR filter creates narrowband anti-aliasing notches at multiples of  $f_{conv}$  (5MHz, 10MHz, 15MHz...). Packet tests (section 5.1.2 below) use this 16-tap FIR filter because its notches are ideally placed to attenuate aliases, as described in section 2.6.1 and shown in Figure 2–7. The IIR filter poles provide wideband attenuation at all frequencies except DC and multiples of  $4f_{conv}$  (20MHz, 40MHz, 60MHz...). Of these IIR poles, the pole at DC is the most important one because it attenuates at relatively low frequencies, where the amplifier poles provide little attenuation.<sup>12</sup> Together, the filters very effectively reject aliasing interferers.

## 4.2 DT Spectrum-Sensing Receiver with Adaptive Filtering<sup>13</sup>

The prototype spectrum-sensing receiver uses DT spectrum-sensing to detect large interferers and select the optimal rejection mode of a reconfigurable filter in real-time. Chapter 3 describes the operating principles and functional details of DT spectrum-sensing, the digital controller, and the SS-guided reconfigurable filter, which together

---

<sup>12</sup> The IIR filter provides >11dB attenuation from 5MHz to 15MHz, as shown in Figure 4–4.

<sup>13</sup> In this collaborative project, Li Li designed the LNA, mixer, and transimpedance amplifier and Hyungil Chae designed the buffer and switched-capacitor amplifiers.

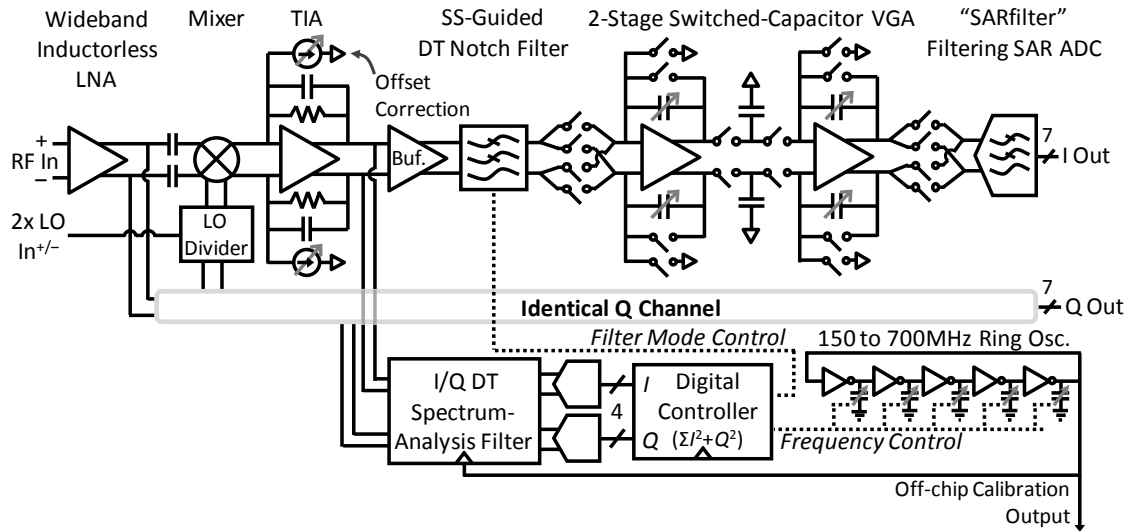


Figure 4–5. Architecture of the spectrum-adaptive receiver prototype. The spectrum-sensing path (bottom) scans to detect large interferers and automatically selects the optimal rejection mode of the reconfigurable DT notch filter.

create a spectrum-adaptive filter. We demonstrate the new spectrum-adaptive (SA) filtering technique in a flexible direct conversion receiver (Figure 4–5) that combines the SA filter with a wideband front-end, TIA, SC amplifiers, and a 7-bit SARfilter ADC with embedded DT filtering. The wideband LNA drives current through the mixer and into a TIA. Current DACs source counteracting currents through the TIA’s feedback resistors to remove DC offsets. The TIA drives the  $G_m$  stage (Figure 3–7) in the SS path (Figure 4–5, lower branch) and the reconfigurable SS-guided DT FIR notch filter through a buffer in the main signal path (Figure 4–5, upper branch). Figure 4–6 shows a die photo of the 65nm CMOS receiver prototype.

#### 4.2.1 Switched-Capacitor Amplifiers

Two stages of switched-capacitor variable-amplifiers (VGAs), located after the SS-guided DT notch filter (Figure 4–5), amplify the received signal by 21dB to 35dB.

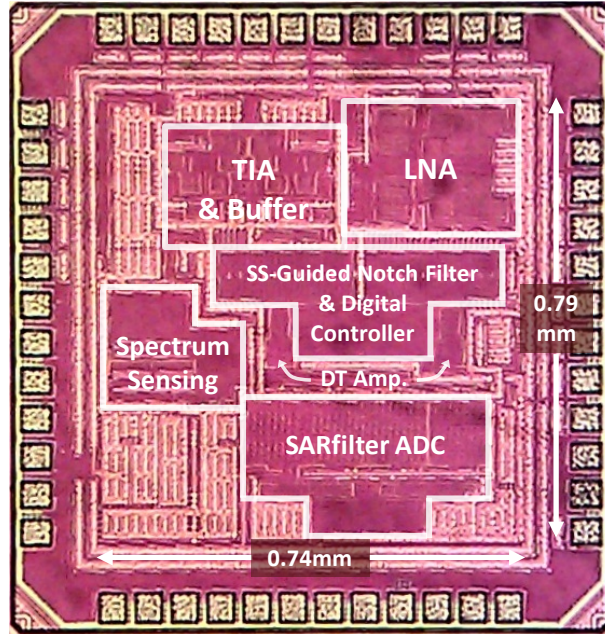


Figure 4–6. Die photo of the spectrum-sensing receiver.

Digitally-tunable capacitances in the 1<sup>st</sup> stage scale proportionally to the number of active unit capacitors in each notch filter mode to preserve gain and also to compensate for 2.2dB of loss at DC in mode 1 (Figure 3–5) of the notch filter, which is the lowest-frequency mode that targets interferers located from 15 to 23MHz. Digitally-tunable capacitances in 2<sup>nd</sup> stage implement variable gain. Chopping switches at the input and output of the 1<sup>st</sup> and 2<sup>nd</sup> stages, respectively, reduce 1/f noise.

#### 4.2.2 Filtering SAR ADC (“SARfilter” ADC)

A modified version of the SARfilter ADC (Chapter 2) filters and digitizes the output of the 2<sup>nd</sup> SC amplifier stage. Similar to the implementation in the first receiver prototype, the ADC embeds a reconfigurable lowpass analog DT FIR/IIR filter within a SAR ADC to order to attenuate interferers before performing 7-bit digitization. The FIR filter in the ADC is created by interleaving SAR conversion with multi-cycle sampling of

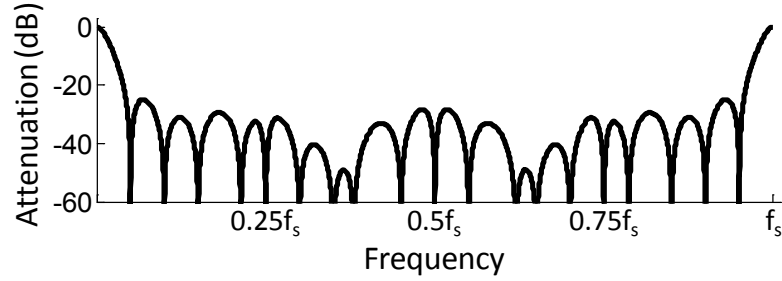


Figure 4–7. Frequency response of the SARfilter ADC when it is configured to implement (4.1).

the input onto the capacitive DAC of the ADC. The IIR filter is created by intermediate charge-sharing of these samples with a history capacitor. Boot-strapped sampling switches [30] in this modified ADC implementation allows the receive chain to operate at with a common mode voltage near mid-rail. In prototype measurements, we set the reconfigurable filter to implement the transfer function

$$H(z) = \frac{\frac{1}{192}(b_0 + b_1 z^{-1} + \dots + b_{19} z^{-19})}{1 - \frac{2}{3} z^{-4}}, \text{ where} \quad (4.1)$$

$$[b_0 \ b_1 \ b_2 \ b_3 \ b_4] = [b_5 \ b_6 \ b_7 \ b_8 \ b_9] =$$

$$[b_{10} \ b_{11} \ b_{12} \ b_{13} \ b_{14}] = [b_{15} \ b_{16} \ b_{17} \ b_{18} \ b_{19}] = [3 \ 3 \ 4 \ 3 \ 3].$$

The 20-tap FIR component of the filter decimates the input by 20x, and along with the IIR filter, lowpass filters the input with the frequency response shown in Figure 4–7.

#### 4.2.3 Receiver Filtering Strategy

The spectrum-adaptive receiver implements three filters that each serves a different purpose. The TIA pole attenuates high-frequency interferers, particularly those that would otherwise pass through the high-frequency passbands located at multiples of the sampling frequency of the SS-guided filter and the SARfilter ADC. The SS-guided filter attenuates large interferers offset 15 to 70MHz from the wanted signal that would otherwise distort the SC amplifiers. The lowpass SARfilter ADC attenuates all remaining



interferers outside of the channel bandwidth and ensures that decimation by the embedded analog DT filter introduces negligible aliasing.

## CHAPTER 5

### Prototype Measurement Results

#### 5.1 Flexible SARfilter ADC Receiver

A prototype flexible receiver with broadband LNA and mixers, amplifiers, and SARfilter ADCs is implemented in a 1P9M 65nm CMOS process with MIM capacitors. Measurements confirm that the wideband front-end supports communication standards with a wide range of carrier frequencies and that the SARfilter ADC achieves low-power reconfigurable DT interferer rejection and digitization. Table 5–1 summarizes the measured performance of the receiver when operating in the maximum gain setting, in order to determine the best achievable sensitivity. Assuming minimal input loss from a matched RF source, which is reasonable given the measured  $S_{11}$  of -10.5dB, the maximum gain from the RF input to the ADC input is approximately 60dB. The receiver achieves a NF of approximately 6dB, which we determine by assuming perfect LNA input matching and comparing  $50\Omega$  source noise with the measured variance of the ADC output code when input-referred to the LNA input. The frequency response of the DT filter can be digitally modified by configuring the number of taps in the FIR filter from 16 to 64 and the size of each coefficient from 0 to  $6C_u$ . The ADC supports conversion rates as high as 21.25MS/s when the 16-tap filter described by (2.8) is enabled, which corresponds to  $f_{clk}$  of 340MS/s. The measured power consumption of the entire receiver is

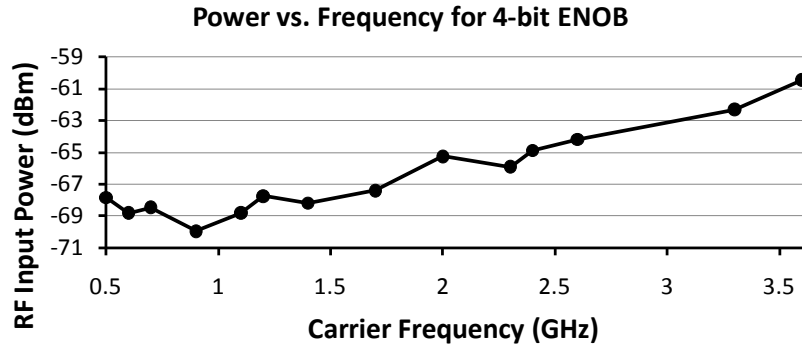


Figure 5–1. RF input power necessary to achieve a fixed ADC dynamic range of 4-bits (ENOB) with an  $f_{carrier} + 1\text{MHz}$  tone input, as the carrier and LO frequencies vary from 500MHz to 3.6GHz. Supplies are fixed at 1V.

3.98mW, 5.51mW, and 9.47mW for the 915MHz and 2450MHz bands of IEEE 802.15.4 and the DSSS PHY of IEEE 802.11, respectively.

The receiver supports RF carrier frequencies ranging from 500MHz to 3.6GHz. Figure 5–1 quantifies this capability by plotting the necessary *RF input* power to achieve a fixed *ADC output* dynamic range of 4-bit ENOB (25.84dB SNDR) as a function of the carrier frequency. The RF input power ranges from -70 to -60.5dBm.<sup>14</sup> These measurements reflect the achievable sensitivity at a given RF carrier frequency. For example, the ADC output achieves 25.84dB SNDR at 2.4GHz with a -66dBm RF input. This implies that the output can achieve the required -2.2dB SNDR for the 2450MHz band of IEEE 802.15.4 [21] with an RF input power of -94.04dBm (i.e. -66dBm-25.84dB-2.2dB), which is consistent with the measured sensitivity of -92dBm (Section 5.1.2 below).

<sup>14</sup> At lower frequencies, the coupling capacitor between the LNA and mixer impedes the signal. At higher frequencies, the output power of the LO divider decreases, which reduces the conversion gain of the mixer.

### 5.1.1 Measured Filter Response

Figure 5–2 overlays the measured and ideal frequency responses at the output of the ADC. The measured frequency response plots the down-converted power of a swept single-tone RF input. The top and bottom plots show the measured frequency responses when 16-tap (2.8) and 20-tap (5.1) DT filters are configured, respectively.

$$y(n) = \frac{1}{192} [3x(n-1) + 3x(n-2) + 4x(n-3) + 3x(n-4) + 3x(n-5) + \dots + 3x(n-20)] + \frac{2}{3}y(n-5) \quad (5.1)$$

The “no filter” measurements represent the attenuation provided by the baseband amplifier poles. Although the tap lengths of the two filters differ,  $f_{conv}$  is set to 5MS/s in both configurations by choosing  $f_{clk}$  of 80MS/s and 100MS/s for the 16-tap and 20-tap filters, respectively. The 20-tap filter benefits from a higher unwanted pass-band

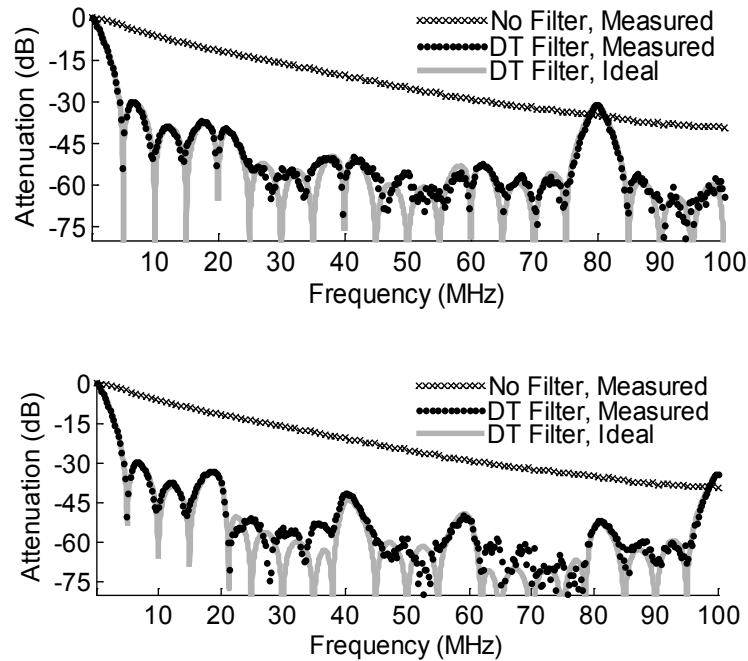


Figure 5–2. Measured no-filter mode filter response and ideal and measured filter responses of the DT filter described by (2.8), when  $f_{clk}=80\text{MS/s}$ ,  $f_{conv}=5\text{MS/s}$  (top) and by (5.1) when  $f_{clk}=100\text{MS/s}$  and  $f_{conv}=5\text{MS/s}$  (bottom).

frequency of 100MHz, instead of 80MHz, at the cost of higher power consumption. When combined with amplifier pole attenuation, both configurations attenuate aliasing interferers and adjacent channels at frequencies higher than  $f_{conv}$  by more than 30dB.

### 5.1.2 Packet Tests

We verify the entire receiver by measuring error rates using IEEE 802.15.4 and IEEE 802.11 compliant packets. Matched filter demodulation with digital phase correction is performed off-chip. The IEEE 802.15.4 tests are performed as required by the specifications [20], except that only the 20 byte payload is analyzed for bit errors.<sup>15</sup> As shown in the last two rows of Table 5–1,  $f_{conv}$  is set such that the specified interferers are centered at  $f_{conv}$  or  $2f_{conv}$ . This frequency plan demonstrates that the DT filter sufficiently attenuates interferers when they alias completely onto the desired signal. The IEEE

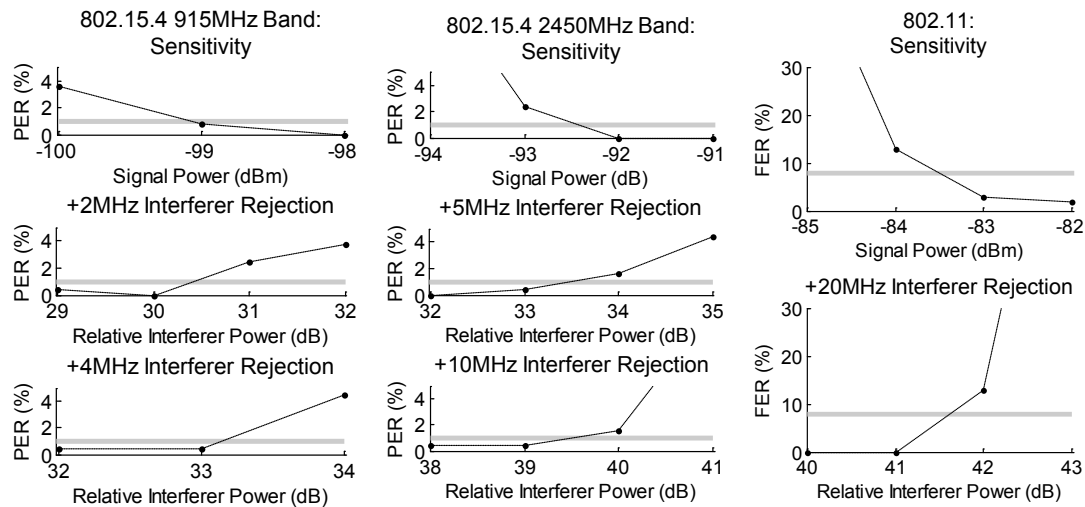


Figure 5–3. Measured packet error rate (PER) and frame error rate (FER) as a function of signal power and interferer power (relative to a fixed wanted signal power) for the 915MHz and 2450MHz bands of IEEE 802.15.4 and IEEE 802.11. Each test point represents the error rate calculated from 250 received packets. The gray line indicates the maximum PER or FER allowed by the standards.

<sup>15</sup> Omission of the 6 byte header from error analysis results in <0.2dB error in measured sensitivity.

802.11 test parameters are chosen to be similar to the specified DSSS PHY requirements [31].  $F_{conv}$  is set equal to the chip rate and the interferer is set to the channel frequency that is closest to  $2f_{conv}$ . The desired signal is IEEE 802.11 compliant at a 1Mbps (11Mchip/s) data rate and framed with a 1024 octet payload. The results of packet testing are plotted in Figure 5–3 and summarized in Table 5–1. The receiver achieves a measured sensitivity of -99dBm and +30dB and +33dB adjacent and alternate channel interferer rejection with packets compliant to the 915MHz band of IEEE 802.15.4. It achieves -92dBm sensitivity and +33dB and +39dB adjacent and alternate channel interferer rejection with packets compliant to the 2450MHz band of IEEE 802.15.4. This measured performance exceeds the requirements of the IEEE 802.15.4 standard. In IEEE 802.11 tests, the receiver achieves -83dBm sensitivity and rejects a +20MHz, +41dB unframed interferer that is 802.11 coded and modulated at 1Mbps (11Mchip/s).

Technology		65nm 1P9M w/MIMCAP
Active Area		0.24mm <sup>2</sup>
Carrier Frequency Range		500MHz to 3.6GHz
Maximum Gain, from LNA input to SARfilter ADC input		≈60dB
S <sub>11</sub>		< -10.5dB
Noise Figure		≈6dB
IIP3, in-band, from LNA input to SARfilter ADC input		-45dBm
ENOB, maximum amplifier gain		≈5b, incl. front-end and baseband amplifier noise and distortion
Maximum $f_{conv}$ , Eq. (2.8) DT Filter		21.25MS/s
Configurable Filter Tap Length / Weight		16 to 64 / 0 to 6C <sub>unit</sub>
Power Eq. (2.8) DT Filter	Analog	5.24mW @ 1.0V 2.79mW @ 0.85V
	Digital	2.16mW @ 1.0V, $f_{conv}$ =11MS/s 0.65mW @ 0.9V, $f_{conv}$ =5MS/s 0.30mW @ 0.9V, $f_{conv}$ =2MS/s
	Clocks, LO Divider	2.07mW, 4.82GHz 2xLO 0.89mW, 1.82GHz 2xLO
	Total	9.47mW, 802.11 5.51mW, 802.15.4 2450MHz 3.98mW, 802.15.4 915MHz
802.11, Eq. (2.8) DT Filter, $f_{conv}$ =11MS/s		Sensitivity of -83dBm Rejection of +20MHz, +41dB unframed interferer
802.15.4 2450MHz, Eq. (2.8) Filter, $f_{conv}$ =5MS/s		Sensitivity of -92dBm Rejection of +5MHz, +33dB and +10MHz, +39dB interferers
802.15.4 915MHz, Eq. (2.8) Filter, $f_{conv}$ =2MS/s		Sensitivity of -99dBm Rejection of +2MHz, +30dB and +4MHz, +33dB interferers

Table 5–1. Measured performance of the wideband receiver with reconfigurable DT. FIR/IIR filtering SAR ADC.

## 5.2 DT Spectrum-Sensing Receiver with Spectrum-Adaptive Filtering

The prototype achieves 55.8dB gain and supports carrier frequencies from 600MHz to 3.4GHz. Figure 5–4 plots the combined frequency response of the receiver, which includes the attenuation of the TIA pole; the SS-guided filter disabled, overlaid with the filter enabled in one of four modes (Figure 3–10 and Table 5–2); and the SARfilter ADC. The combined filter achieves >52dB attenuation in the target frequency bands of all four SS-guided filter modes. In packet tests compliant to IEEE 802.15.4, we stimulate the receiver with RF packets and identify the power level that achieves 1% packet error rate (PER). As summarized in Table 5–2, the receiver exceeds the sensitivity and interferer rejection requirements of both the 2450MHz and 915MHz bands.

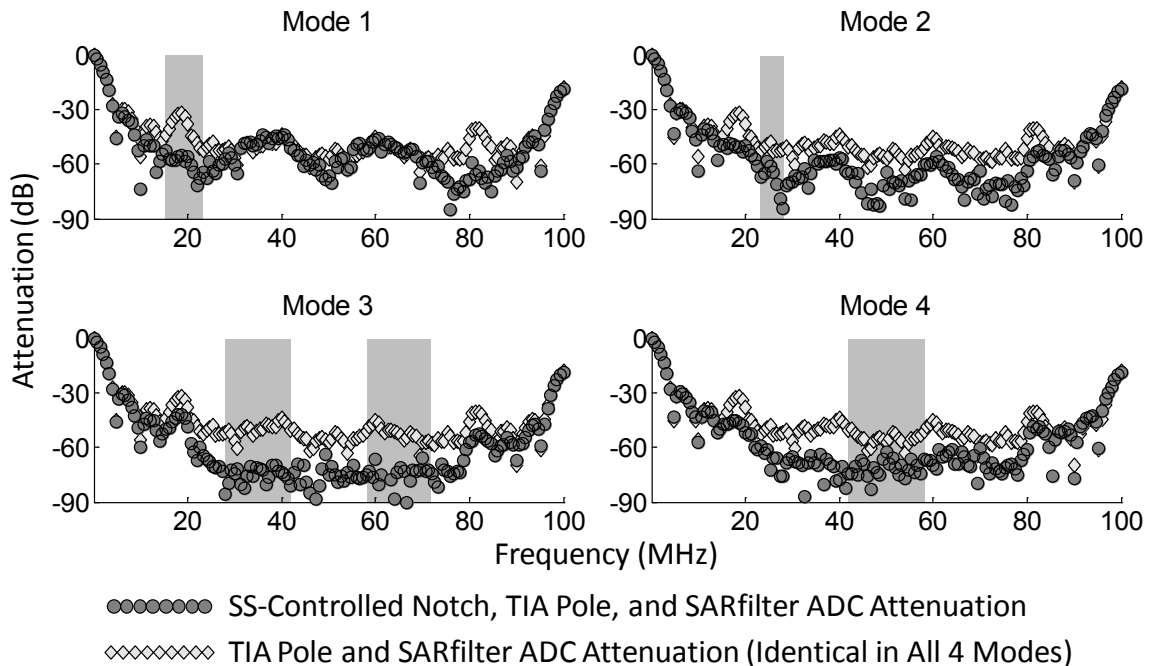


Figure 5–4. Measured combined frequency responses of the receiver, which includes the TIA pole; the SS-guided filter disabled, overlaid with the filter configured to one of four attenuation modes; and the SARfilter ADC filter. The gray shaded areas indicate the frequencies targeted by each mode of the SS-guided filter.



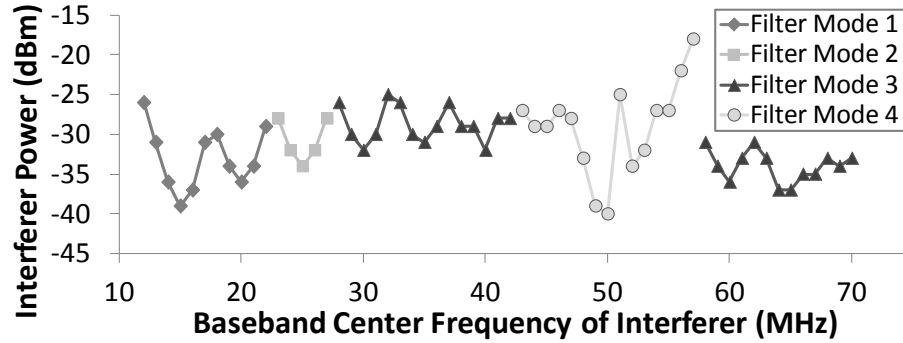


Figure 5–5. Measured minimum power of an FM interferer, with 1MHz deviation and 50kHz rate, that activates the four modes of the spectrum-adaptive filter. The power levels resemble inverted power detection passband frequency responses (Figure 3–5).

### 5.2.1 Spectrum-Sensing and Adaptive Filtering

Figure 5–5 plots the measured minimum required power of an FM modulated interferer to activate the different spectrum adaptive filtering modes and shows that the controller sets the correct mode at all center frequencies. The power levels resemble inverted frequency responses of the spectrum-sensing power detection band (Figure 3–5). In SA filtering tests using 802.15.4 packets (Figure 5–6), the receiver achieves +55dB to +63dB rejection of a +25MHz to +65MHz FM interferer when SA filtering is enabled, which averages to 9.4dB more rejection compared to when SA filtering is disabled. SA

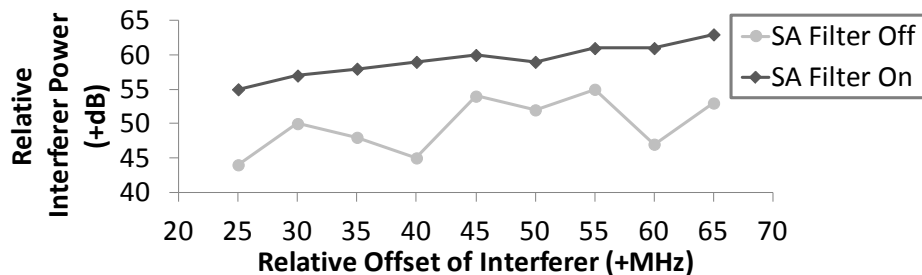


Figure 5–6. Measured relative power vs. frequency offset of an FM interferer, with 1MHz deviation and 50kHz rate, at which the receiver achieves 1% PER when receiving RF modulated IEEE 802.15.4 2450MHz band packets with -85dBm power. Interferer rejection improves by an average of 9.4dB when the SA filter is enabled.

filtering achieves this improvement by detecting the FM interferer and reconfiguring the SS-guided notch filter to the mode that best attenuates the interferer.

Technology	65nm 1P9M w/MIMCAP	
Active Area	0.39mm <sup>2</sup>	
Carrier Frequency Range	600MHz to 3.4GHz	
Max Gain	55.8dB	
IIP3	-38dBm	
SS Sweep Duration	≈121μs for 25MHz to 65MHz sweep, 64 samples per bin	
SS-Guided Notch Filter Mode, FIR Coefficients, and Target Attenuation Bands	1: [4 -1 4 4 -1 4], 15-23MHz 2: [2 2 4 4 2 2], 23-28MHz 3: [1 3 5 5 3 1], 28-42MHz & 58-70MHz 4: [1 3 4 4 3 1], 42 to 58MHz	
SARfilter ADC FIR Filter	Tap Length: 16 to 64, Weight: 0 to 6C <sub>unit</sub>	
Power, 1.0V Except for 0.9V Digital	Analog	6.82mW
	Digital: Controller, Notch Filter & SARfilter ADC Clocks	3.41mW, $f_{conv}=5MS/s$ , 20-tap SARfilter ADC FIR filter 1.31mW, $f_{conv}=2MS/s$ , 16-tap SARfilter ADC FIR filter
	LO Divider	1.94mW, 4.8GHz $2xf_{LO}$ 0.90mW, 1.8GHz $2xf_{LO}$
	Spectrum Sensing	2.93mW
	Total	802.15.4 2450MHz band: 15.1mW 802.15.4 915MHz band excluding SS (not supported for $f_{conv}=2MS/s$ ): 9.0mW
	IEEE 802.15.4 Sensitivity & Interferer Rejection	2450MHz, $f_{conv}=5MS/s$
	915MHz, $f_{conv}=2MS/s$	-100dBm +2MHz, +29dB; +4MHz, +31dB

Table 5–2. Summary of parameters and measurements of the spectrum-adaptive receiver.

## CHAPTER 6

### Wireless Demonstration System<sup>16</sup>

A complete wireless receiver system [32] combines the first receiver prototype [26] with a real-time FPGA-based baseband demodulator to create a full-functioning wireless visual demonstration system. The demonstration showcases a system built around the flexible SARfilter receiver IC (section 4.1), which captures a RF input and outputs I/Q digital baseband bitstreams. A custom digital baseband demodulator implemented on a FPGA performs real-time digital phase correction, symbol timing acquisition, and

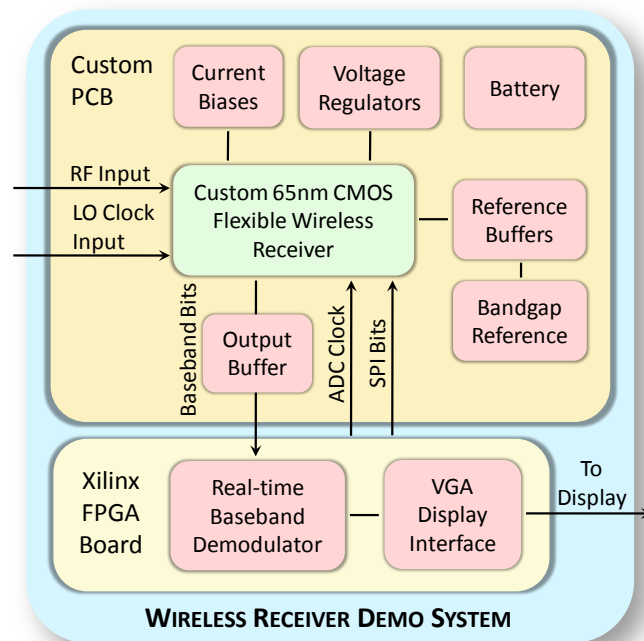


Figure 6–1. High-level diagram of the wireless receiver visual demonstration system.

<sup>16</sup> In this collaborative project, Ming-Hao Wang coded the demodulator on the FPGA; John Bell designed the video interface, the interface between the blocks on the FPGA, and the image coding scheme; and Li Li designed the LNA, mixer, and baseband amplifiers in the custom flexible wireless receiver IC.

demodulation of 802.15.4 2450MHz band packets. Additional custom FPGA logic interfaces the demodulator to a video driver, in order to create a complete hardware demonstration system that receives, demodulates, and displays images.

## **6.1 System Overview**

The system is a complete wireless receiver, as shown in Figure 6–1, except that an off-board clock source provides the mixer LO. The SARfilter receiver IC is mounted on a custom PCB daughter-board alongside off-the-shelf support components. The daughter-board is mounted on a Xilinx FPGA development board. The demonstration system receives packetized RF image data in IEEE 802.15.4 2450MHz band format. Custom logic on the FPGA digitally corrects phase offset, acquires symbol timing information, and then demodulates the baseband bitstream output from the receiver. The FPGA buffers and sends the demodulated data to a video driver for display through a VGA interface. The FPGA also provides the receiver with digital configuration bits over an SPI bus and an ADC clock. Figure 6–2 shows the custom receiver daughter-board on which the receiver IC and the support electronics are mounted and the FPGA development board.

## **6.2 Receiver Daughter-Board**

The daughter-board is a custom 4-layer FR-4 PCB that generates all of the supplies and biases for the custom receiver IC. Two AAA batteries power the daughter-board; the supplies are tapped from one or both batteries depending on the required voltage.

A linear regulator supplies 1V to the three voltage domains on the chip: clock, analog, and digital. The three domains are isolated with  $\pi$ -filters. The current biases for the

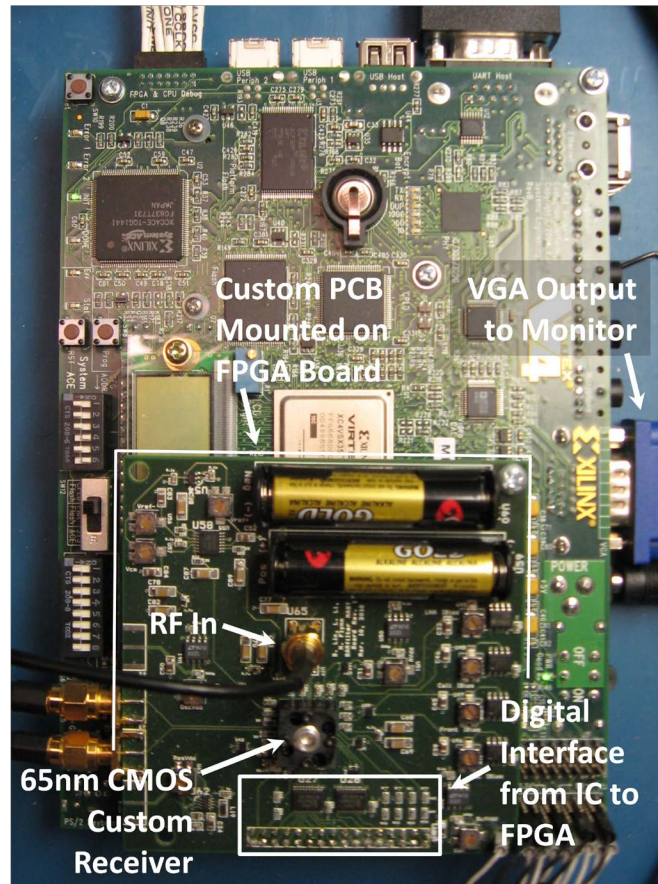


Figure 6–2. Demonstration system with the receiver IC mounted on a daughter-board, which is connected to an off-the-shelf Xilinx FPGA development board.

receiver are provided by current source ICs. The voltage references for the SAR ADC are generated by resistively dividing the output of a bandgap reference, and then buffering the divided voltages with op-amps in unity gain feedback.

### 6.3 FPGA-based Baseband Demodulator

A Xilinx ML402 Virtex-4 (XC4VSX35) FPGA development board interfaces between the receiver and the user. The receiver IC captures an RF signal containing 802.15.4 2450MHz band demonstration image packets and outputs I/Q modulated baseband to a custom real-time digital baseband demodulator on the FPGA. The demodulator digitally synchronizes the phase and symbol timing of the baseband bitstream, and then

demodulates the corrected bitstream. As the bitstreams containing the next image pixels are processed by the demodulator, the previously demodulated pixel color and location data are buffered and sent through custom interface logic to a video driver on the FPGA board. The video driver displays the image on a computer monitor through a VGA interface (Figure 6–2), which verifies the successful interoperability of a long chain of signal processing hardware spanning the entire receiver system. A digital clock manager (DCM) module on the FPGA converts a 100MHz crystal clock source on the development board to a 64MHz sampling and SAR clock for the ADC. With a 16-tap filter enabled, this clock rate results in an ADC conversion rate of 4MS/s. The FPGA also sets the control bits of the receiver IC.

The baseband demodulation algorithm for the 2450MHz band of IEEE 802.15.4 is initially designed and evaluated in MATLAB, and then ported to a real-time digital logic implementation on the FPGA. As the first demodulation step, the digital baseband demodulator corrects the phase offset in the I/Q waveforms. As an example of the correction process, Figure 6–3(a) shows sixteen symbols per channel of measured modulated baseband I/Q output from the SARfilter ADC at 4MS/s per channel. The resulting internal signals of the demodulator are shown in (b), (c), and (d). The raw output exhibits a phase offset that results from the phase difference between the up- and down-conversion LO clocks, which is digitally corrected. A frequency offset can likewise be corrected with minor modifications to the correction procedure, but is unnecessary because the test setup locks the frequency of the up-converter in the RF signal source to the LO clock source that drives the down-conversion mixer in the receiver.

The demodulator first removes the DC offset and scales the signal to a desired amplitude. It then performs (complex) matched filtering of the received bitstream to the packet's synchronization header (SHR). The magnitude of the filter output is shown in Figure 6–3(c) for a bitstream that contains 3 consecutive packets, as seen by the correlation peaks. This matched filter serves three purposes:

1. Peaks in the magnitude identify the presence of a packet.
2. The peak magnitude location provides symbol timing information.
3. The relative energy in the I and Q channels at the peak magnitude location identifies the phase offset.

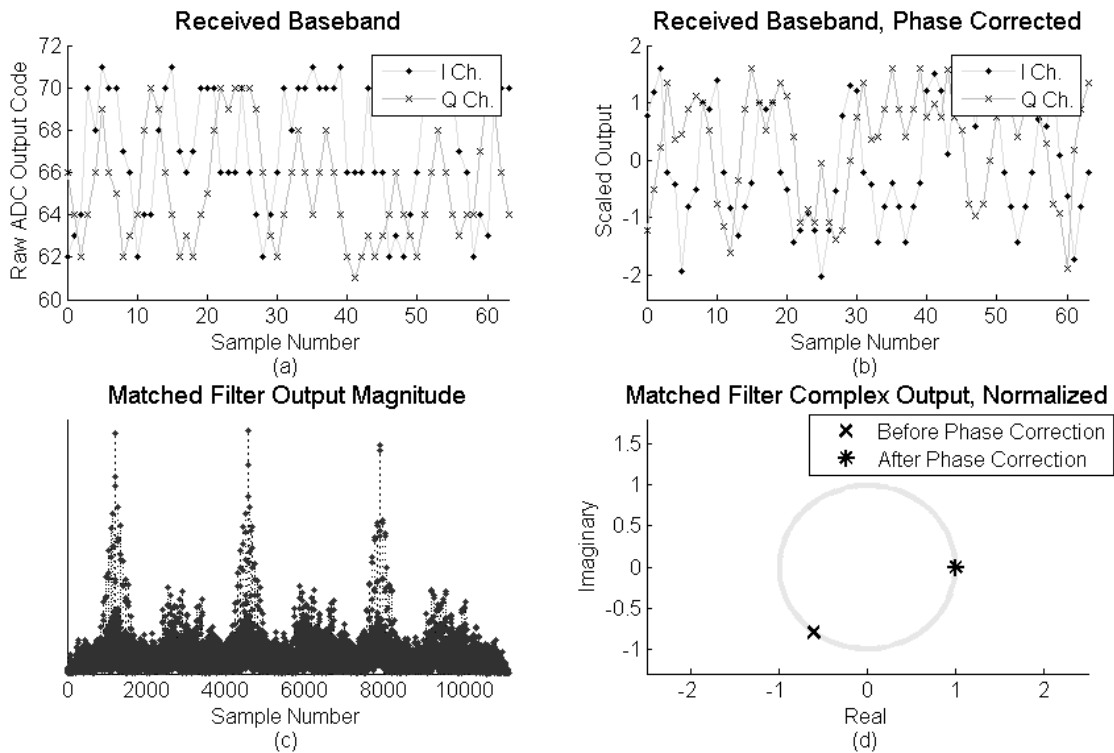


Figure 6–3. Measured modulated digital baseband outputs of the receiver at 4MS/s (a) and the resulting internal signals of the MATLAB demodulator as it processes the bitstreams (b), (c). The demodulator synchronizes to the packet’s synchronization header and digitally corrects phase offset (d). The FPGA demodulator is similarly implemented.

The 3<sup>rd</sup> point above is depicted Figure 6–3(d), in which the energy of the I (real) and Q (imaginary) channels at the peak magnitude location is normalized to unit magnitude and plotted on the complex plane. The phase offset,  $\varphi$ , in this example is approximately  $-127^\circ$  before phase correction and is reduced to a negligible value by multiplying the (complex I/Q) input bitstream by  $e^{-j\varphi}$ . The phase corrected samples are shown in Figure 6–3(b). If a frequency offset also exists, it can be observed as a linearly changing phase offset and can be corrected by match filtering to subsets of the SHR (e.g. 1<sup>st</sup> third, 2<sup>nd</sup> third, then 3<sup>rd</sup> third). The frequency offset can then be calculated from the output phase ramp and corrected.

For demodulation [33], the samples are weighed by half-sine pulse shapes and summed over each symbol period to determine a corresponding chip value. Groups of chips are then compared to the 16 known 2450MHz band spreading codes to determine the symbol that is closest in (Hamming) distance. Implementing 16 parallel matched filters that work on the ADC output at the sample level (i.e. soft decoding) [34] can achieve better performance, but the implemented demodulator works at the chip level in order to keep the complexity reasonable.

The demodulator design developed in MATLAB is mapped to a digital logic implementation on a Xilinx Virtex-4 SX35 FPGA. The FPGA demodulator is similar to the MATLAB implementation. The most significant functional difference is it identifies the SHR by searching for an output magnitude that exceeds a preset threshold, since it is impractical to buffer and process a large number of the matched filter outputs at once. The implementation on the FPGA, including the demodulator, serial (RS232 to SPI) interface, and video driver interface, utilizes 53% of the total registers and 82% of the 4



input LUTs. Only 3% of the dedicated DSP48 blocks are used, so more general logic resources can be made available for other uses by mapping a greater portion of the matched filter to the dedicated DSP resources.

#### 6.4 Image Reception Demonstration

In an end-to-end hardware demonstration, a modified NI LabVIEW MSK script uses a National Instruments PXI-5671 2.7GHz vector signal generator to generate RF image packets. The script is modified to generate IEEE 802.15.4 2450MHz band compliant packets with payload bits that contain the color and location of each pixel of the image. The payload is prefixed with a 10 symbol (or 40 bit or 320 chip) synchronization header (SHR), spread to chips, modulated with half-sine pulse shaped O-QPSK (MSK) [33], and then up-converted to 2.4GHz.

The receiver IC captures and processes the RF image packets and outputs modulated 7-bit digital I/Q baseband bitstreams. An ADC conversion rate of 4MS/s is used (instead of 5MS/s in the packet tests described in section 5.1.2), in order to lessen resource usage on the FPGA. Custom logic on the FPGA demodulates this modulated baseband bitstream, retrieves the payload, and buffers the image pixels onto Block RAM on the Virtex-4 chip. As the pixels are buffered, additional custom logic on the FPGA sends the

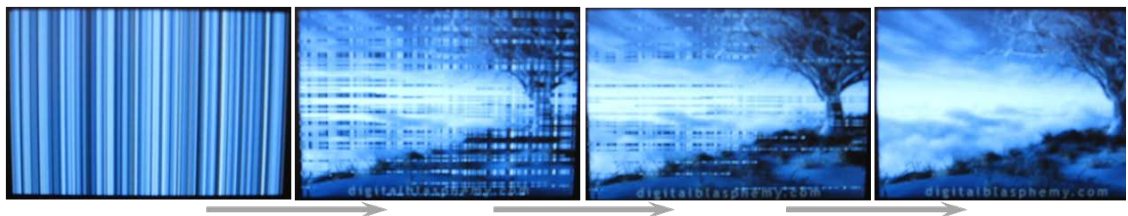


Figure 6–4. As the FPGA demodulator receives and demodulates each packet, the pixel information contained in the payload is updated on a monitor. The leftmost image is a test pattern, which is replaced pixel-by-pixel with the image.

reconstructed image to an Analog Devices video driver chip on the development board. The driver chip displays the image to a computer monitor through a VGA interface (Figure 6–4). shows pictures of the received image as it is demodulated and displayed pixel-by-pixel. The leftmost picture is a test pattern, which is replaced with the transmitted image as the FPGA receives and demodulates each packet.

## CHAPTER 7

### Conclusion

#### 7.1 Summary of Contributions

We demonstrate flexible, digital-intensive wireless receiver architectures that exploit CMOS scaling driven improvements to the power, density, and speed of digital logic, switches, and capacitors. The SARfilter ADC receiver replaces separate baseband filtering stages with a filtering SAR ADC. This ADC combines a modified CDAC with software-programmable digital clocking. The digital clocking drives multi-cycle selective-sampling of the input and charge-sharing of the stored charge to achieve embedded, reconfigurable FIR and IIR DT filtering. Interleaved selective sampling and SAR conversion processes counteract the reduction to the conversion rate that multi-cycle sampling causes. The FIR component of the DT filter supports tap length and coefficients ranging from 16 to 64 and 0 to  $6C_{unit}$ , respectively. In addition, the IIR history capacitor charge-shares with groups of the FIR samples, so that the FIR tap coefficients within the groups can be unequal. The SARfilter ADC, with its embedded filtering, greatly simplifies the design of the baseband receive chain and enables the receiver to support standards with different carrier frequencies and channel bandwidths.

The spectrum-adaptive receiver enhances the reconfigurable filter with real-time, intelligent digital control of the filter's frequency response, based on feedback from DT spectrum-sensing. Spectrum-adaptive filtering uses low-power and robust analog DT

spectrum-analysis filters and simple DSP to scan for strong interferers over a 55MHz range and automatically select the optimal rejection mode of a reconfigurable filter. The calibrated on-chip ring oscillator accurately defines the spectrum-analysis filter's passband frequency and enables digital frequency tuning. The digital controller adjusts the spectrum-analysis filter's capacitor sizes and decimation rate to maintain constant passband gain and bandwidth at all center frequencies. Spectrum-adaptive filtering allows the receiver to adapt to its operating conditions, eliminates the need to overdesign for worst-case conditions, and also eliminates the filtering complexity, power consumption, and area use associated with overdesign. The improved flexibility and scalability and the reduced complexity, power consumption, and area use that the SARfilter ADC and spectrum-adaptive receiver architectures achieve support their integration into next-generation wireless transceiver SOCs.

#### *7.1.1 List of Key Contributions*

- Filtering SAR ADC, integrated into the flexible receiver prototype (section 5.1)
  - Embedded DT FIR/IIR filtering with programmable tap length and coefficients
  - Interleaved FIR selective-sampling and SAR processes counteract the reduction to the ADC's conversion rate that multi-cycle sampling causes
  - IIR charge-sharing of FIR samples in groups permits unequal FIR tap coefficients within the groups
- DT spectrum-sensing with adaptive filtering, integrated into the spectrum-sensing receiver prototype (section 5.2)
  - DT spectrum-sensing bandpass subsamples interferers using robust, analog DT spectrum-analysis filtering and calculates the interferers' power using simple, low-power, fixed-rate DSP

- Calibrated on-chip oscillator accurately defines the frequency of the spectrum-analysis filter’s power detection passband
- Digital controller processes the spectrum-sensing system’s output to select the optimal interferer rejection mode a reconfigurable filter in real-time

## **7.2 Future Research Directions**

### *7.2.1 Filtering SAR ADC with Less Filtering Overhead*

The filtering SAR ADC described in Chapter 2 spends as many clock cycles selectively sampling the input, to implement FIR filtering, as the number of FIR filter taps. Reuse of previously sampled charge when generating the next FIR output is not feasible when FIR summation is implemented through charge-sharing, because no easy method exists to remove the oldest charge sample from the capacitor array before adding a new charge sample. But FIR summation can also be implemented by connecting the capacitors in series to sum the sampled voltages. The original sampled charge remains on the capacitors when they are disconnected from each other, so a new FIR filtered output can be generated by removing the capacitor that contains the oldest charge sample from the series array, sampling the current input onto this capacitor, and then reconnecting this capacitor to the series array to sum the charge and create the next FIR output. FIR summation by series connection also has the added benefit of amplifying the input. Making the series connection requires a switch between the top plate of each selective-sampling capacitor bank and the bottom plate of another bank, such that the banks can form a series “stack.” If the parasitic capacitance of individual sampling switches is prohibitively large, the capacitors can also be grouped together in parallel first, to implement “addition” through charge-sharing, and then the parallel banks can be

connected in series, to implement addition through voltage summation. In this implementation, each entire parallel-connected bank needs to sample new inputs during each output cycle.

### *7.2.2 Different Approaches to Spectrum-Sensing*

A spectrum-analyzer that runs many different spectrum-sensing methods in parallel can benefit from the strengths of each method. For example, faster spectrum-sensing is achievable by first inspecting the spectrum with a faster coarse-accuracy SS technique, then using a slower moderate-accuracy SS technique to more accurately analyze a smaller frequency range. Multiple parallel super-regenerative receivers [35], each calibrated and tuned to sense a different frequency band, can potentially perform coarse-accuracy SS. In order to keep the area of the super-regenerative receivers small, simple oscillators with tunable loop gain would suffice, such as a phase-shift oscillator [36]. The DT spectrum-sensing method discussed in Chapter 3 performs moderate-accuracy SS. Its sensing speed can be improved by performing a SAR-like binary search in frequency using DT spectrum-analysis filters with power-of-two differences in bandwidth between subsequent search iterations.

### *7.2.3 DT Spectrum-Sensing for Cognitive Radios*

The implementation of DT spectrum-sensing in this work targets detection of large interferers. Developing methods of high-sensitivity signal detection are vital to enabling radios that comply to new cognitive radio standards, such as IEEE 802.22 and IEEE 802.11af [37], [38], [39]. The sensitivity of DT spectrum-sensing can be increased to approach the specified requirements of these standards by preceding the spectrum-

analysis filter with high-gain, low-noise amplifiers; improving the noise and sampling accuracy of active stages within the filter; and increasing the resolution of the ADC that digitizes the spectrum-analysis filter's output.

#### *7.2.4 New Approaches to RF Subsampling RX*

We use the spectrum-analysis filter to isolate interferer power contained within its narrow passband, but it can potentially also filter and subsample wanted signals at IF and RF. The filter response does not have a flat passband, which limits its usefulness to narrowband signals. A possible method of mitigating this non-ideality is to filter the wanted signal with multiple bandpass filters with closely spaced center frequencies, and then combine the different spectral bands in the digital domain. Challenges to implementing this technique include low-power generation of sampling clocks with small differences in frequency, gain and delay mismatch between different paths, and selection of subsampling frequencies to prevent aliasing.

## **APPENDIX A**

### **Common Wireless Communication Standards**

Common wireless communication standards, such as IEEE 802.15.4 and IEEE 802.11, are used during the development and testing of the receiver prototypes. Table A-1 summarizes the key requirements that are specified by several common wireless communication standards. Sensitivity and interference rejection are two requirements from these standards that helped guide our design decisions in the area of noise, dynamic range, and filter frequency response. Sensitivity is defined as the minimum signal power at the RF input of the receiver that allows the demodulator to achieve an error rate below a specified threshold. Interference rejection is defined as the power and frequency offset of an interfering signal, relative to the wanted signal, that also allows the demodulator to achieve an error rate below the same specified threshold. Section 2.9 above analyzes simple cases of how these requirements translate to receiver noise figure and filter attenuation.



Specification	Wireless Communication Standard				
	Bluetooth v3.0 Basic Rate [40]	IEEE 802.15.4 915MHz [20]	IEEE 802.15.4 2450MHz [20]	IEEE 802.11-2007 (HR/DSSS PHY) [31]	IEEE 802.11n-2009 (HT PHY) [41], [42]
Carrier Freq. (MHz)	2402 to 2480	906 to 924	2405 to 2480	2412 to 2462	2412 to 2462
Data Rate	1Mb/s	40kb/s, spread to 600kchip/s	250kb/s, spread to 2Mchip/s	11Mb/s	600Mb/s max: 40MHz channel, 4 streams
Modulation	GFSK	BPSK	O-QPSK (MSK)	8-bit CCK	OFDM, 64-QAM for max rate
Sensitivity (dBm)	-70 @ 1% BER	-92 @ 1% PER of 208-bit packet	-85 @ 1% PER of 208-bit packet	-76 @ 1% FER, frame with 8192-bit PDSU	-61 @ 10% PER for max rate, packet with 32768-bit PDSU
Interferer Rejection, Relative Power (dB) @ Freq. Offset (MHz)	-11 @ 0 +0 @ 1 +30 @ 2 +40 @ ≥ 3 +9 @ image	+0 @ 2 +30 @ 4	+0 @ 5 +30 @ 10	+35 @ ≥ 25	-2 @ 40 +14 @ 80 for max rate

Table A-1. Summary of key requirements specified in common wireless communication standards.

## BIBLIOGRAPHY

- [1] Z. Xu, S. Jiang, Y. Wu *et al.*, "A Compact Dual-Band Direct-Conversion CMOS Transceiver for 802.11a/b/g WLAN," *IEEE ISSCC Dig. Tech. Papers*, pp. 98-99, Feb. 2005.
- [2] W. Kluge, F. Poegel, H. Roller *et al.*, "A Fully Integrated 2.4GHz IEEE 802.15.4 Compliant Transceiver for ZigBee Applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 1470-1479, Feb. 2006.
- [3] S. Karvonen, T. Riley, and J. Kostamovaara, "A Low Noise Quadrature Subsampling Mixer," *IEEE Int. Symp. on Circuits and Systems*, pp. 790-793, May 2001.
- [4] S. Karvonen, T. Riley, S. Kurtti, and J. Kostamovaara, "A Quadrature Charge-Domain Sampler With Embedded FIR and IIR Filtering Functions," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 507-515, Feb. 2006.
- [5] R. Staszewski, K. Muhammad, D. Leipold *et al.*, "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278-2291, Dec. 2004.
- [6] R. Bagheri, A. Mirzaei, S. Chehrazi *et al.*, "An 800-MHz–6-GHz Software-Defined Wireless Receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860-2876, Dec. 2006.
- [7] J. Borremans, G. Mandal, V. Giannini, T. Sano, and M. Ingels, "A 40nm CMOS highly linear 0.4-to-6GHz receiver resilient to 0dBm out-of-band blockers," *IEEE ISSCC Dig. Tech. Papers*, pp. 62-64, Feb. 2011.
- [8] A. Mirzaei, H. Darabi, and D. Murphy, "A Low-Power Process-Scalable Superheterodyne Receiver with Integrated High-Q Filters," *IEEE ISSCC Dig. Tech. Papers*, pp. 60-61, Feb. 2011.

- [9] (2010, Sept. 3). *General Survey of Radio Frequency Bands – 30 MHz to 3 GHz (ver. 2.0)* [Online]. Available: [http://www.sharedspectrum.com/wp-content/uploads/2010\\_0923-General-Band-Survey-30MHz-to-3GHz.pdf](http://www.sharedspectrum.com/wp-content/uploads/2010_0923-General-Band-Survey-30MHz-to-3GHz.pdf)
- [10] T. M. Taher, R. B. Bacchus, K. J. Zdunek, and D. A. Roberson, "Long-term Spectrum Occupancy Findings in Chicago," *IEEE Int. Symp. Dynamic Spectrum Access Networks (DySPAN)*, pp. 100-107, May 2011.
- [11] C. Ghosh, S. Roy, and D. Cavalcanti, "Coexistence Challenges for Heterogeneous Cognitive Wireless Networks in TV White Spaces," *IEEE Wireless Communications*, pp. 22-31, Aug. 2011.
- [12] J. Park, T. Song, J. Hur *et al.*, "A Fully Integrated UHF-Band CMOS Receiver With Multi-Resolution Spectrum Sensing (MRSS) Functionality for IEEE 802.22 Cognitive Radio Applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 258-268, Jan. 2009.
- [13] M. Kitsunezuka, Kodama H., N. Oshima *et al.*, "A 30-MHz–2.4-GHz CMOS Receiver With Integrated RF Filter and Dynamic-Range-Scalable Energy Detector for Cognitive Radio Systems," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, May 2012.
- [14] P. Malla, H. Lakdawala, K. Kornegay, and K. Soumyanath, "A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT  $\Delta\Sigma$  ADC for 802.11n/WiMAX Receivers," *IEEE ISSCC Dig. Tech. Papers*, pp. 496-497, Feb. 2008.
- [15] *Wikipedia: Moving average* [Online]. Available: [http://en.wikipedia.org/wiki/Moving\\_average](http://en.wikipedia.org/wiki/Moving_average)
- [16] *Bamboo AV: Information About TV Comb Filters* [Online]. Available: <http://www.bambooav.com/information-about-tv-comb-filters.html>
- [17] J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 246-247, Feb. 2007.
- [18] P. Harpe, C. Zhou, X. Wang, G. Dolmans, and H. de Groot, "A 30fJ/conversion-step 8b 0-to-10MS/s asynchronous SAR ADC in 90nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 388-389, Feb. 2010.

- [19] J. Kang, D. T. Lin, L. Li, and M. P. Flynn, "A Reconfigurable FIR Filter Embedded in a 9b Successive Approximation ADC," *IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 711-714, Sept. 2008.
- [20] *Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs)*, IEEE Standard 802.15.4, 2006.
- [21] S. Lanzisera and K. S. J. Pister, "Theoretical and Practical Limits to Sensitivity in IEEE 802.15.4 Receivers," *IEEE Int. Conf. on Electronics, Circuits, and Systems*, Dec. 2007.
- [22] D. T. Lin, H. Chae, L. Li, and M. P. Flynn, "A 600MHz to 3.4GHz Flexible Spectrum-Sensing Receiver with Spectrum-Adaptive Reconfigurable DT Filtering," *IEEE RFIC Symp.*, Jun. 2012.
- [23] J. Yuan, "A Charge Sampling Mixer with Embedded Filter Function for Wireless Applications," *Proc. 2nd Int. Conf. on Microwave and Millimeter Wave Technology*, pp. 315-318, Sept. 2000.
- [24] R. G. Vaughan, N. L. Scott, and D. R. White, "The Theory of Bandpass Sampling," *IEEE Trans. Signal Process.*, pp. 1973-1984, Sept. 1991.
- [25] J. G. Proakis and D. G. Manolakis, "Discrete-Time Signals and Systems," in *Digital Signal Processing*. Upper Saddle River: Pearson Education, 2007, ch. 2, p. 46.
- [26] D. T. Lin, L. Li, S. Farahani, and M. P. Flynn, "A Flexible 500MHz to 3.6GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21MS/s SAR ADC," *IEEE Custom Integrated Circuits Conf. (CICC)*, Sept. 2010.
- [27] S. Wang, A. Niknejad, and R. Brodersen, "Design of a Sub-mW 960-MHz UWB CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2449-2456, Nov. 2006.
- [28] S. Chehrazi, A. Mirzaei, and A. A. Abidi, "Noise in Current-Commutating Passive FET Mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 2, pp. 332-344, Feb. 2010.
- [29] M. Camus, B. Butaye, L. Garcia *et al.*, "A 5.4mW 0.07mm<sup>2</sup> 2.4GHz Front-End Receiver in 90nm CMOS for IEEE 802.15.4 WPAN," *IEEE ISSCC Dig. Tech.*

- Papers*, pp. 368-369, Feb. 2008.
- [30] M. Dessouky and A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched opamp circuits," *Electronic Letters*, vol. 35, no. 1, pp. 8-10, Jan. 1999.
- [31] *Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications*, IEEE Standard 802.11, 2007.
- [32] D. T. Lin, L. Li, J. Bell, M. Wang, and M. P. Flynn, "A Flexible Wireless Receiver System with a 7b 21MS/s Filter SAR ADC," *IEEE ISSCC/DAC Student Design Contest*, Feb./Jun. 2011.
- [33] F. Xiong, *Digital Modulation Techniques*, 2nd ed. Boston, MA: Artech House, 2006, pp. 207-226.
- [34] J. G. Proakis and M. Salehi, "Linear Block Codes," in *Digital Communications*. Boston: McGraw-Hill, 2008, ch. 7, pp. 424-445.
- [35] J. Chen and M. P. Flynn, "A Fully Integrated Auto-Calibrated Super-Regenerative Receiver in 0.13- $\mu$ m CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1976-1985, Sept. 2007.
- [36] E. L. Ginzton and L. M. Hollingsworth, "Phase-Shift Oscillators," *Proc. Inst. Radio Eng. (IRE)*, vol. 29, no. 2, pp. 43-49, Feb. 1941.
- [37] C. Ghosh, S. Roy, and D. Cavalcanti, "Coexistence Challenges for Heterogeneous Cognitive Wireless Networks in TV White Spaces," *IEEE Wireless Communications*, vol. 18, no. 4, pp. 22-31, Aug. 2011.
- [38] K. Shin, H. Kim, A. W. Min, and A. Kumar, "Cognitive Radios for Dynamic Spectrum Access: From Concept to Reality," *IEEE Wireless Communications*, vol. 17, no. 6, pp. 64-74, Dec. 2010.
- [39] C. Sum, H. Harada, F. Kojima, Z. Lan, and R. Funada, "Smart Utility Networks in TV White Space," *IEEE Communications Magazine*, vol. 49, no. 7, pp. 132-139, Jul. 2011.
- [40] *Specification of the Bluetooth System*, Core Version 3.0 + HS, 2009.

[41] *Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications*, IEEE Standard 802.11n, 2009.

[42] *Wikipedia: IEEE 802.11n-2009* [Online]. Available:  
[http://en.wikipedia.org/wiki/IEEE\\_802.11n-2009](http://en.wikipedia.org/wiki/IEEE_802.11n-2009)