

Low-Power RF Integrated Circuits for Wireless Sensor Network Synchronization and Communication

by

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To everyone who encouraged me through the years

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Chapter 1

Introduction

1.1. The Future of Computing

1.1.1. Computing Trends

Computers today have changed dramatically from the mainframes decades ago. As computing has become increasingly ubiquitous, it is becoming difficult to remember a time when our phones weren't smart or when families shared a single computer at home. Based on Bell's Law [1], wireless sensor networks (WSNs) are perceived as the next big step in this decades-long trend toward smaller, more ubiquitous computing.

According to Bell's Law, a new class of computers will become the dominant market force approximately every decade [1]. Bell defines a computer class as a set of computers with a similar cost, programming environment, network, and user interface, where each class undergoes a standard product life cycle of growth and decline. Based on prior market trends, a new computer class has come into existence approximately every decade, and each successive class has had a 100x reduction in volume (Fig. 1.1). In addition, each successive class has resulted in a reduction in unit cost and an increase in volume of production [2].

In the 1950s, mainframes were the dominant computer class. Each mainframe consumed large rooms, and their cost limited their use to only one unit per enterprise. Mainframes were eventually overtaken by mini computers in the 1960s and then

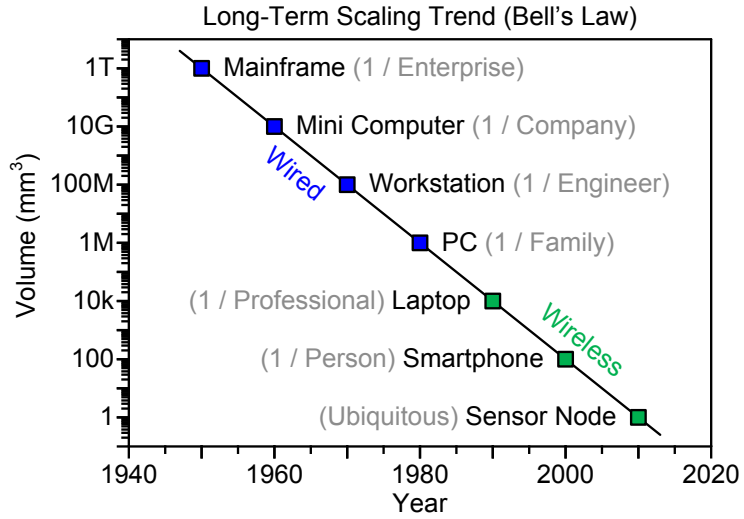


Fig. 1.1. The long-term trend in computer scaling over the years [1].

workstations in the 1970s. By the 1980s personal computers (PCs) were entering family homes, and the 1990s saw laptops become the first wireless computer class. Today, smartphones have become the first truly personal computing class, and they fit in the palm of your hand. Assuming the trends in Bell's Law continue, then the next computer class is expected to be even smaller and more ubiquitous—the class of cubic-mm-scale wireless sensor nodes.

1.1.2. Wireless Sensor Networks

The goal of wireless sensor networks (WSNs) is straightforward—to sense the environment around them. Each node in the network is made up of components to process, sense, and communicate with other nodes in the network (Fig. 1.2). WSNs offer several advantages over wired networks, which can be costly, impractical, or obtrusive in many situations. As a result, there is significant interest in wireless sensor networks for a variety of applications [3]-[15].

Numerous surveys have been conducted in the past decade, which provide a good introduction to the application space for WSNs [3]-[8]. The surveys from [3]-[6], in

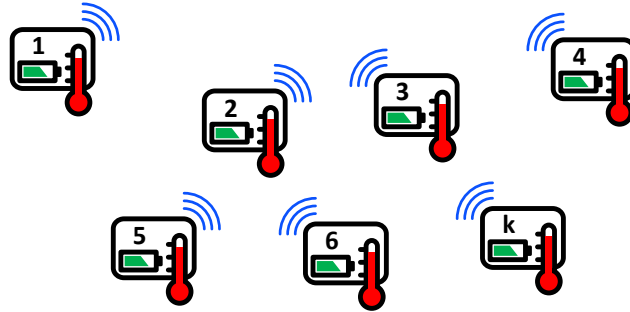


Fig. 1.2. Conceptual block diagram of a wireless sensor network with temperature sensing.

particular, give a good overview of the entire application space and highlight some of the many sensor networks that have been implemented in hardware. They also compare and contrast various testbeds and enumerate some of the challenges for realizing WSNs discussed throughout this chapter. While the applications discussed in these works vary widely, several topics have garnered particular interest, including: environmental, military, industrial, and biomedical applications. Several recently reported systems are highlighted below.

CSIRO [7] developed a WSN for the environmental tracking of livestock. The network tracks the movement of cattle, so that ranchers can better control pasture usage and also identify sick steer before disease spreads across an entire herd. The network consists of sensor node collars mounted on each steer along with several base stations placed at fixed locations around the ranch. The relative size of cattle suggests small node size is not of particular importance; however, small unit cost is important, as well as long node lifetimes of a year or more.

A long lifetime turns out to be very important for many industrial applications as well. Among them, [9] has proposed a system to monitor pressure in an oil pipeline for signs of leakage. A sensor network is required because oil pipelines cover vast distances, making

human monitoring infeasible. Furthermore, pipelines are often located in remote regions, such that a lifetime of several years is desired. A second sensor network measures the corrosion of steel rebar used in concrete bridges [10]. Because the nodes are embedded into the concrete, a lifetime of years is essential. Volume, however, is less important, though each node must be reasonably sized to maintain the structural integrity of the bridge. A third sensor network measures the seismic activity on bridges and other structures for infrastructure health monitoring [11]. A final group has developed an in-tire pressure monitor to measure vehicle load and tire wear-out [12]. Due to the gradient forces inside the wheel well, the size of the node is restricted to a volume of approximately 1cm^3 . As a result, the system must be highly integrated. In addition, the node must be designed with a long lifetime because frequent access to the inside of a tire is impractical.

Based on observations from recently published patient health systems, long device lifetimes and small unit volumes are also crucial for many biomedical applications. For example, an intraocular pressure monitor was developed by [13], which measures pressure within the eye in order to diagnose glaucoma. The system is completely integrated into a 1.5mm^3 volume, making system integration and volume significant challenges. Finally, because the system must be implanted into the eye, a lifetime of weeks is desired. Another group has developed a highly integrated node for real-time electrocardiogram (ECG) measurements and wireless readout [14]. The main node occupies a volume on the order of 1cm^3 , excluding the sensor patches which must be placed across the chest. Unlike many of the other systems, an ECG only requires a lifetime of a few hours, though this ECG node has a 200hr battery life. Finally, a

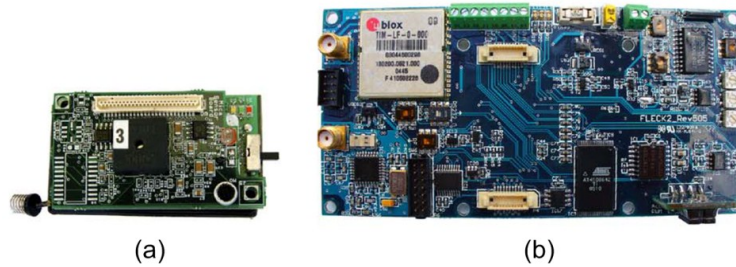


Fig. 1.3. Examples of recent wireless sensor nodes (a) Mica Mote and (b) Fleck 3 [7].

glucometer was created by [15] to measure glucose from tear ducts. The node is built onto the surface of a contact lens, but the circuit core is all contained within a 1mm^3 volume. In this particular case, lifetime is not a problem, however, because the system rectifies a 2.4GHz signal for power. Nonetheless, the system must be low power, so that it can survive off of wirelessly rectified power. The wireless signal also must be low power to ensure patient health and safety.

While the wireless sensor networks surveyed vary widely in application, it is readily apparent that they universally benefit from longer node lifetimes, smaller unit volumes, and reduced cost. In addition, long-term deployments and small unit volumes are often necessary to satisfy the underlying feasibility of a particular application. The simultaneous desire for long lifetimes and small volumes, however, creates significant integration challenges as well as considerable energy constraints on system design. Ultimately, these challenges must be resolved in order for WSNs to become a reality.

1.2. Wireless Sensor Nodes

1.2.1. Anatomy of Conventional Sensor Nodes

The first step toward mm-scale wireless sensor nodes is presented in [3]-[7]. The nodes are composed of multiple components on a printed circuit board (PCB) as shown in Fig. 1.3. The nodes consistently use commercial-off-the-shelf (COTS) components, and

as a result, the PCBs measure several centimeters on a side. While energy usage and lifetime are a concern, they have little noticeable impact on the design other than the choice of low-power COTS components with a sleep mode. Thus, the nodes typically consist of a battery, voltage regulator, processor, sensor, and communication radio with external antenna and crystal oscillator (Fig. 1.4). The memory and clock are provided within the commercial processor, and solar cells are added to the system when long lifetimes are required for the application. Because many of these attributes mimic those found in the smartphone class of computers, these initial wireless sensor nodes constitute only the first step toward cubic-mm-scale computing.

1.2.2. Component Trends & Challenges

As wireless sensor nodes continue to evolve, we must overcome the challenge of building smaller nodes that use less energy. Therefore, we must examine each component in the system and identify which components consume the most power and area. Then, we can propose solutions which will have a meaningful impact on overall system volume and lifetime. In this section, we discuss the challenges associated with the integrated circuits, antenna, oscillator, sensors, solar cells, and batteries of the system.

The most straightforward and simplest solution to reduce node volume, however, is to remove components. When removing components is impossible, component functionality can sometimes be achieved with alternative methods that require less volume or energy. Each of these design decisions, however, has trade-offs that must be analyzed.

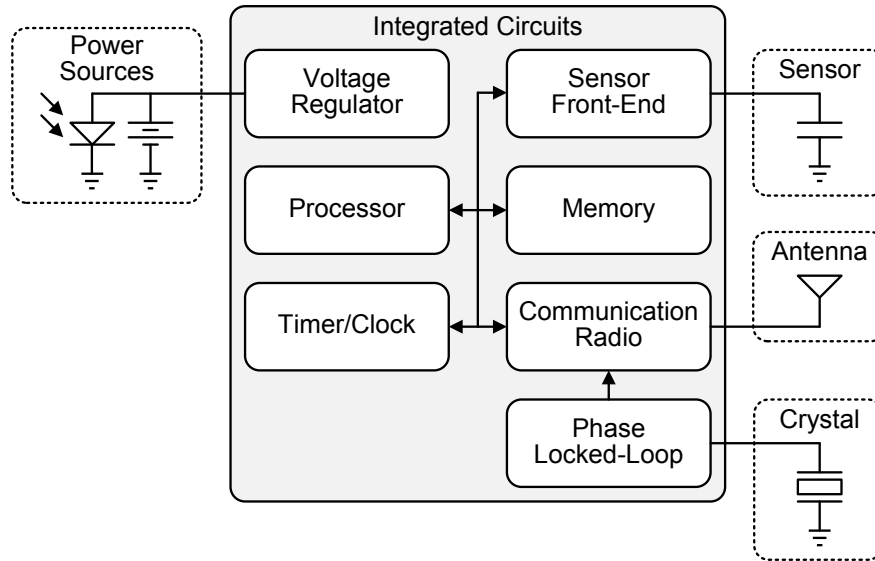


Fig. 1.4. System block diagram of a recent wireless sensor node.

Integrated Circuits

One possible concern is the integrated circuit (IC) components. Fortunately, modern CMOS ICs, with the help of process scaling, are capable of providing the desired circuit functionality while still fitting within a cubic-mm form-factor [12]-[19]. To further reduce area requirements, several IC blocks can be integrated onto a single die to create a system-on-chip (SoC) [14],[19]. Unfortunately, the process requirements for many circuit components, such as processor and radio, differ; therefore, the one-size-fits-all approach of SoCs cannot yield the optimal system performance (i.e. minimal energy usage). In order to achieve optimal performance while maintaining small volumes, several recent integrated systems employ a stacked die approach, which provides the design freedom to select the optimal process for each layer [13],[16]-[18]. Thus, it is not the ICs that pose the greatest challenge to node scaling; it is the other components in the system, namely the antenna, oscillator, sensor, solar cell, and battery.

Table 1.1. Monopole antenna length ($\lambda/4$) in various frequency bands.

Frequency (Hz)	434M	915M	2.45G	3.1G	10.6G	24.1G	61.3G
Band	ISM	ISM	ISM	UWB	UWB	ISM	ISM
Antenna (mm)	173	82	31	24	7	3	1

Antenna

The size of an antenna is dependent on many factors, but one of the most important factors is the operating frequency of the communication radio. For example, a basic monopole antenna sized for optimal radiation efficiency will have a length of $l = \lambda/4$, where λ is the wavelength of the wireless signal. Wavelength relates to the center frequency of the wireless channel, f , and the speed of light, c , through the expression $\lambda = c/f$. Therefore, $l = \lambda/4 = c/(4f)$, and antenna length is inversely proportional to operating frequency. Table 1.1 shows the length of the antenna at several common frequencies bands from 400MHz to 60GHz. Of these sample bands, 1mm-scale antennas only exist above 10GHz, and a $\lambda/4$ monopole antenna is not truly 1mm long until the frequency increases to 60GHz. As a result, center frequency must be increased to 10GHz or more to satisfy volume requirements of cubic-mm systems. This result also suggests a need for higher frequency systems than commonly used in wireless communication today. Many of today's networks operate at frequencies from 850MHz to 2.4GHz. This includes commercial cellular and Wi-Fi networks, as well as many current WSNs.

Choosing to increase center frequency creates a couple of important trade-offs. First, the path loss in the wireless channel increases. As a result, more signal power is lost for a fixed communication distance. Second, the circuits that operate at these higher frequencies will consume more power. These circuits include the communication radio

and local oscillator. Therefore, reducing power consumption in both of these components is critical.

Local Oscillator

A local oscillator (LO) typically consists of a crystal oscillator and phase-locked loop (PLL) (Fig. 1.3), and for a number of reasons the typical LO is one block often removed from wireless sensor nodes. First, a crystal oscillator is bulky, which makes system integration difficult. The smallest commercial crystal oscillator available today is 2.0 x 1.6 x 0.8mm [20]. The bigger problem though is scaling. The size of crystal oscillators has scaled far more slowly than CMOS devices due to inherent physical properties of the crystals. In addition, crystal oscillators consume considerable power. The crystal oscillator from [20] provides a 13-52MHz oscillation frequency while consuming 3.4mW. With a 32.768kHz oscillator however, the power consumption is reduced to 3.4 μ W but the dimensions increase to 3.6 x 2.8 x 1.5mm [21]. A PLL adds even more power. While one recently published PLL consumes only 260 μ W using a 20MHz reference [22], it was designed specifically for WSNs and has a frequency accuracy of only 0.25%. Typical PLLs consume 1.2mW or more [23]-[24]. Ultimately, the combination of large volume requirements and high power consumption make PLL-based LOs undesirable for WSNs. Fortunately, alternative solutions exist.

The crystal oscillator and phase-locked loop can be replaced with a FBAR or BAW oscillator [12],[25]-[27]. FBAR oscillators in particular have been demonstrated that require relatively little area and consume less than 100 μ W [25]-[27]. Nonetheless, the need for an external component like a FBAR resonator can still be prohibitive in certain applications. Circuit solutions, such as LC or ring oscillators, are alternatives that

eliminate the need for external components, but clock accuracy and stability suffer [28]-[29]. In addition, power consumption can still be a concern, so a final option is to remove the LO entirely. The communication radio then utilizes self-mixing to down-convert a received signal to baseband and a pulsed oscillator to up-convert the signal for transmission. Removing the LO does have significant repercussions, which are discussed later, but it also results in the lowest power and smallest volume solution.

Sensors

The sensor is another component that can consume considerable power and area, but unfortunately, the system requirements for a sensor are highly application specific, which makes a general discussion regarding sensor design more difficult. It is safe to say that the size and power consumption of the sensor should be reduced in so far as possible. At the same time, there is no point in designing a sensor network with sensors that are unable to provide the desired measurements. As a result, sensor requirements may dictate a significant portion of the major system design decisions, like battery capacity and node volume.

Many sensors have been developed along with their read-out circuits, which satisfy the requirements of cubic-mm sensor networks. For example, an intraocular pressure monitor was developed by [13], which is completely integrated into a 1.5mm^3 volume and can be operated indefinitely. The contact lens for a glucose monitor from [15] is almost entirely packaging for the sensor. Meanwhile, numerous CMOS-based sensors for temperature measurement and event detection (i.e. an imager) also have been developed that meet the system requirements of cubic-mm sensor networks [30].

Solar Cells & Energy Harvesters

The need for solar cells or other energy harvesters is dictated by the operating environment, lifetime requirements, and power consumption of a node for a particular application. Fortunately, the area penalty of solar cells is small because they can be integrated into a die stack. Unfortunately, the power harvested from the cell is proportional to the area and efficiency of the cell. The highest reported efficiency of an unconcentrated monocrystalline silicon solar cell is 25% [31]. Assuming a cell with that efficiency and an area of 1mm^2 , then the solar cell will only produce 1mW of power at solar noon on a sunny day (AM1.5 or $1000\text{W}/\text{m}^2$ of solar insolation). In this case, the solar cell is a separate die; however, for improved integration the solar cell can be integrated into a SoC, but the efficiency decreases to 10-12% [17]. In both cases, we are assuming the node will receive consistent outdoor sun, but that depends heavily on the application. It is far more likely the harvested energy per day is reduced by some scaling factor either from the node being indoors or only seeing intermittent sunlight. So while a solar cell can improve node lifetime, a very careful use case model must be developed to ensure the node has sufficient energy for sustained operation.

Battery

Finally, a battery is required for many applications, but the limitations in energy density of modern batteries create significant challenges for cubic-mm sensor nodes. Fortunately, millimeter-scale batteries exist (Fig. 1.5) [32]. Unfortunately, the capacity of mm-scale batteries is low because capacity scales with volume. For a $1.375 \times 0.85 \times 0.15\text{mm}$ custom lithium-ion (Li-ion) battery from Cymbet, the capacity is only $1\mu\text{Ah}$ (Fig. 1.6), and the maximum discharge current is only $10\mu\text{A}$ [32]. The average power

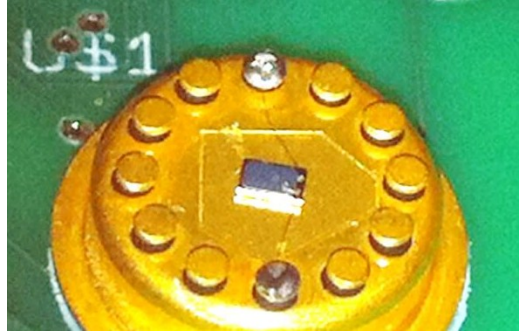


Fig. 1.5. Custom 1µAh Cymbet micro-battery setup for testing.

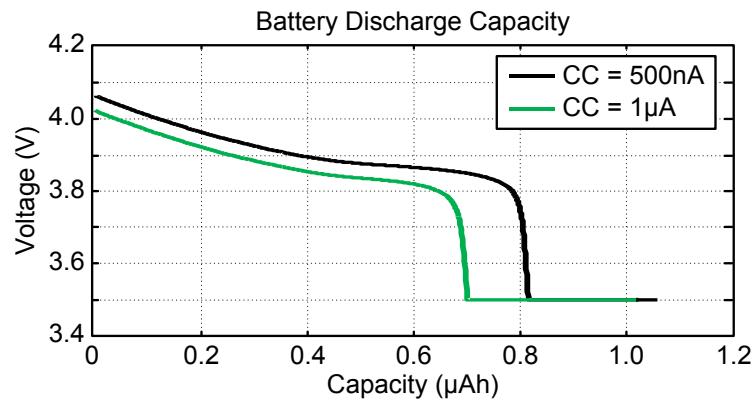


Fig. 1.6. Measured discharge curve of the 1µAh Cymbet micro-battery.

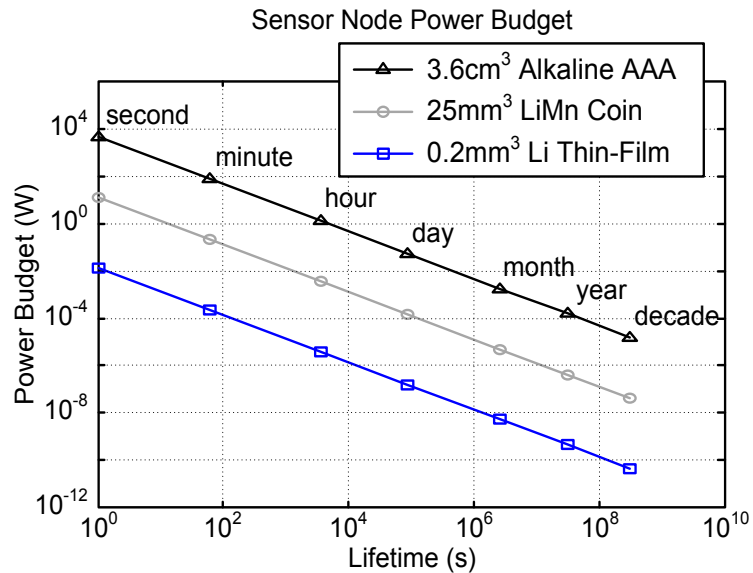


Fig. 1.7. Power budget available vs. desired lifetime for different battery cells [30].

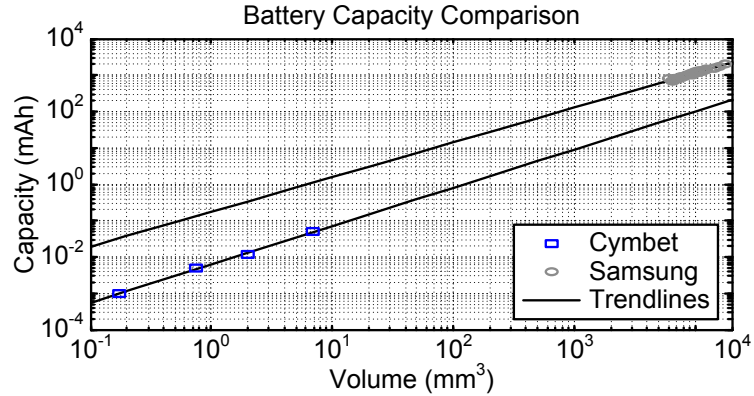


Fig. 1.8. Li-ion capacity comparison of Cymbet micro-batteries vs. commercial prismatic batteries.

consumption therefore must be 1nW or less for a one year node lifetime (Fig. 1.7)—far less than the active power of most circuits. As a result, for a node to survive a year the node either must be duty-cycled heavily or capacity must improve significantly.

We would like to increase capacity, so first we would like to know if micro-batteries perform as well as more traditional Li-ion cells. Fig. 1.8 compares the capacity of several lithium-ion prismatic cells of different volumes. Some of the cells are micro-batteries from Cymbet and have volumes of less than 1mm³ [32]. The other cells come from Samsung, which manufactures batteries for cellular phones, laptop computers, and other electronics [33]. Trend lines were superimposed over the data to illustrate the battery capacity of each type of cell, and based on this data, micro-batteries have an order-of-magnitude lower unit capacity than those with larger volumes. This reduction is likely a result of packaging and the ion membrane—both of which consume a higher percentage of the total volume in a small battery. So while capacity could be improved, the nodes would remain energy-constrained.

While battery capacity has grown over the years, nodes likely will remain energy-constrained for the foreseeable future. Fig. 1.9 shows the long-term growth in battery

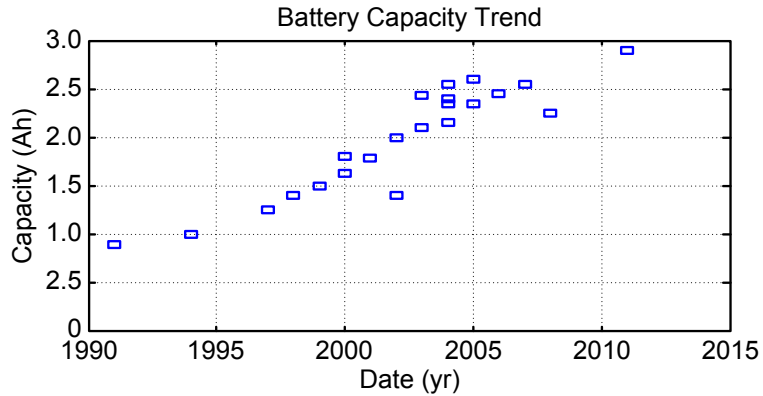


Fig. 1.9. Long-term growth in capacity of cylindrical Li-ion batteries since the first commercial Li-ion.

capacity for commercial Li-ion cells since their first introduction by Sony in 1991. In the past 20 years, battery capacity for cylindrical 18650 cells has only increased by a factor of three [34]-[49] while transistor count has increased by more than a factor of 1000 in the same time frame according to Moore’s Law. While the increase in battery capacity has been steady, heavily duty-cycled circuit operation and harvested energy will be necessary for long-term node survival.

The exception is the few applications that don’t require batteries. These systems rely on wireless power transfer from near-field coupling or RF rectification to enable the circuit elements on the node [15]. As a result, the node remains off until energy is available. These types of networks do not take measurements until requested by a user because a user serves as the aggregator. A common example is keycard access for room entry using passive RFID technology. In this example, the card reader radiates energy to the card, which provides a code to the reader before it grants access to the room. As another example, the glucometer in [15] only takes measurements when a patient or healthcare worker requests the data. In both cases, the measurements aren’t automatic, and a human being is integral to the operation of the network.

Table 1.2. Power consumption comparison of sensor node components.

Component	Active Power	References
Processor and Memory	297nW	[19]
Sensor & Sensor Front-End	Application Specific	Not Applicable
High-Accuracy Timer	49.5mW	[29]
Low-Accuracy Timer	1pW-80 μ W	[50]-[56]
Crystal Oscillator	3.4 μ W-3.4mW	[20],[21]
Phase-Locked Loop	260 μ W-9.1mW	[22]-[24]
FBAR Oscillator	22 μ W-89 μ W	[25]-[27]
Communication Radio	400 μ W-29mW	[12],[14],[28],[58],[59]

Unfortunately, a battery is required for many applications, and that battery has insufficient energy to operate a sensor node continuously for its desired lifetime. For a lifetime of one year, the average power available from a sub-cubic-mm battery is only 1nW (Fig. 1.7)—well below the active power consumption of most circuits. To alleviate this problem, energy usage must be reduced. The radio and oscillators easily dominate system energy usage if they are operated continuously to maintain synchronization (Table 1.2). Thus, reducing the power required to maintain synchronization between nodes can greatly improve node lifetime, making synchronization an important concern for cubic-mm WSNs [57].

1.2.3. Anatomy of Future Sensor Nodes

Cubic-millimeter wireless sensor nodes with long lifetimes are desired for many applications. Unfortunately, many current sensor nodes [3]-[7] have a volume of on the order of 10cm³ to 100cm³, giving them many design attributes consistent with the

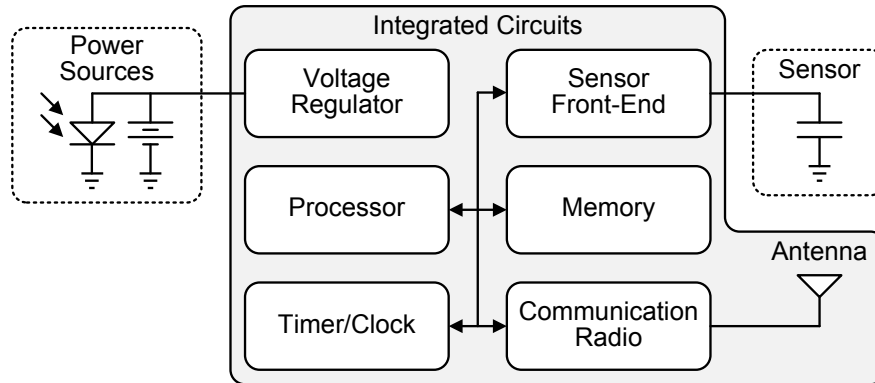


Fig. 1.10. System block diagram of a future wireless sensor node.

smartphone class of computers. In effect, these sensor nodes are just the first step toward the smaller, more pervasive computers envisioned for wireless sensor networks.

An intermediate step has also emerged, which consists of sensor nodes with volumes on the order of 1cm^3 [2],[12],[14]. They are characterized by the fact that they use fewer COTS components. In addition, the volume and lifetime goals necessitate the use of application specific ICs (ASICs) optimized for low-power operation. This intermediate class of sensor nodes may be sufficient for some applications, but they would still universally benefit from system improvements made for smaller nodes.

The final step creates wireless sensor nodes which are truly a new class of computers [13],[15]-[18]. They have volumes on the order of 1mm^3 , dictated by the intended application. In addition, this new class of computers is heavily design-constrained, both in terms of volume and energy availability. As a result, significant design challenges must be addressed; fortunately however, the solutions also will benefit larger, less-constrained systems. Specifically, these less-constrained systems still benefit from lower costs and improved lifetimes.

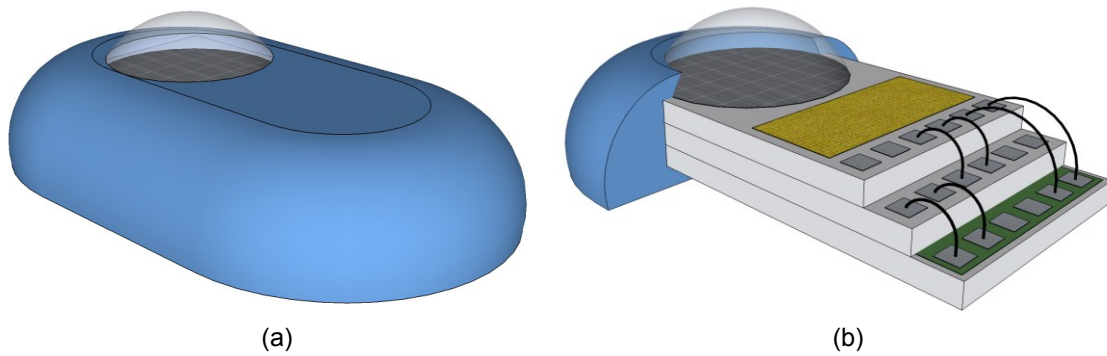


Fig. 1.11. Conceptual system diagram of a cubic-mm sensing platform (a) encapsulated and (b) with the encapsulation cut-away.

Cubic-mm-scale wireless sensor nodes are highly integrated. The node still consists of many of the same components from Fig. 1.4, but several changes exist (Fig. 1.10). The future system will communicate wirelessly at a higher frequency to reduce the size of the antenna. The node will employ a stacked die configuration, including battery, solar cell, and sensor (Fig. 1.11), but the PLL and crystal oscillator will be removed to save energy and area. The battery is smaller and won't have sufficient energy to sustain continual operation for long lifetimes, so energy harvesting from a solar energy or some other energy source is necessary. In addition, everything must be duty-cycled; however with the radio duty-cycled, synchronization becomes a significant problem.

1.3. Synchronization for Wireless Communication

Synchronization is critical to the overall functionality and power budget of a wireless sensor network. The nodes must be on and communicating at the same time in order to be able to talk to one another. If the communication radio and timer remain on continuously they consume significant amounts of energy and will quickly drain the battery (Table 1.2). Recently reported communication radios consume at least $400\mu\text{W}$ for the receiver and more for the transmitter [12],[14],[28],[58],[59]. While solar harvesting can improve

the power budget to 10nW [13], the nodes remains severely energy-constrained. At the same time, the power budget for a one year lifetime is only 1nW (Fig. 1.7). As a result, continuous wireless communication is impractical for an energy-constrained node, and the radio must be heavily duty-cycled, spending most of its time in the off-state. Duty-cycling, however, makes synchronized communication among nodes in the network challenging while still minimizing energy usage.

1.3.1. Sleep-Mode Power Consumption

The total power budget again of a sensor node is 1nW for a one year lifetime (Fig. 1.7). Therefore, the node must be heavily duty-cycled, and everything in the system needs to have a low-power sleep state. This includes the communication radio. Many of the recently published communications radios, however, don't report a sleep power [12],[28],[58],[59], and it is expected that the sleep power of these is on the order of microwatts. At the same time, it is critical to design for low leakage power in the radio because components with higher active power require better I_{on}/I_{off} current ratios. With an overall power budget of 1nW, the budget for the radio should be less than 100pW while in its sleep state. Additional power also must be given to other components in their sleep states, but the majority of the power budget must go toward maintaining synchronization.

1.3.2. Timer

The traditional (and perhaps obvious) approach to reducing average power consumption is to duty-cycle the communication radio and schedule communication using a high-accuracy on-node timer. High-accuracy timers can be implemented in several different ways, but an external crystal oscillator would be one of the most accurate. Because an external crystal requires significant volume, it creates integration

challenges for future cubic-mm nodes. In addition, the power consumption of traditional crystal oscillators is high (3.4mW) [20]; however, a recent 32.768kHz crystal oscillator was published that consumes only 6nW [60]. Other than crystal oscillator, high-accuracy timers also can be implemented in CMOS [29]. To achieve high accuracy however, the circuits require significant tunability, which increases their power consumption to 49.5mW. As a result, a high-accuracy timer can be better accomplished using a 6nW crystal oscillator than with CMOS circuits alone, and duty-cycling the communication radio with a high-accuracy timer can provide significant improvement in the total synchronization energy. Using a 6nW crystal oscillator may stay within the power budget of some applications, but the average power must be reduced further for applications requiring multi-year lifetimes.

While less accurate timers are not desired, they do keep time while consuming less power and less area in CMOS. Ultimately, the goal is to maximize accuracy—in terms of rms jitter per cycle or PVT variation—for a given power consumption. Several different topologies have been proposed, but the most common are tuned ring oscillators or relaxation oscillators [50]-[53]. More importantly, several timers have been reported with sub-nanowatt power consumption [54]-[56], making one year node lifetimes possible when the nodes are heavily duty-cycled.

This synchronization scheme does have risks. The use of a less accurate timer results in more accumulated drift between nodes before radio wake-up, so in order for two nodes to synchronize, one node must remain on for the entire drift period. If the nodes are unable to synchronize during the scheduled wake-up period, there is no way for the nodes to resynchronize without considerable time and energy. These difficulties escalate as the

number of nodes in the network grows because no global signal exists across the network to maintain synchronization. A global signal would eliminate the long drift between nodes and ensure network-wide synchronization. If the global signal is wireless, then synchronization can be maintained using a wake-up receiver.

1.3.3. Wake-Up Receiver

Wake-up receivers (WRXs) are designed to wake-up and synchronize a wireless sensor network using a custom beacon signal. The WRXs allow the nodes in a network to operate in a lower power sleep mode most of the time. Once a wake-up signal is detected, the WRX awakens the dormant sensor node and initiates wireless communication based on higher network policies [61].

While WRXs increase node complexity and node volume, several receivers have been demonstrated which consume significantly less power than conventional communication radios [62]-[64]. Because most of these receivers consume less than $100\mu\text{W}$, WRXs have garnered significant interest for synchronization. They often have a sensitivity of -70dBm to -80dBm , and while reduced sensitivity decreases communication range, it also saves power. The receivers also employ simpler architectures to reduce power consumption with many WRXs designed for on-off keying (OOK) or pulse-position modulation (PPM).

A traditional WRX remains on continuously during sleep mode, waking-up the node after a signal is broadcast within the WSN (Fig. 1.12a). As a result, a WRX enables fully asynchronous, interrupt-based communication, eliminating drift between nodes. Using a WRX reduces synchronization energy in comparison with an always-on communication radio.

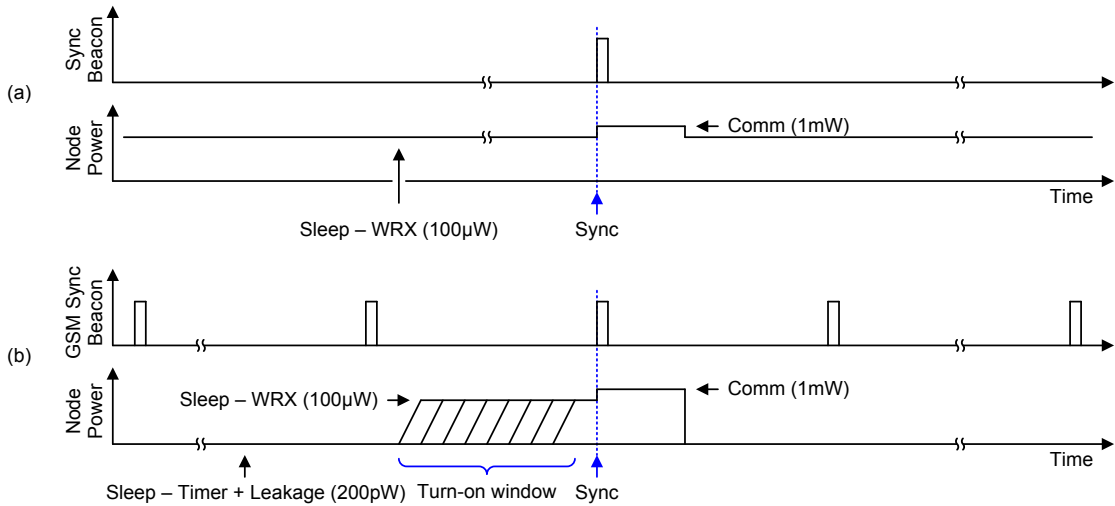


Fig. 1.12. WSN synchronization (a) with an always-on wake-up receiver and (b) with a duty-cycled wake-up receiver.

There are four major disadvantages of WRX-based synchronization. First, to utilize this synchronization technique, the wake-up signal must be generated *within the sensor network*, requiring additional power for its transmission. Second, they add system complexity. Third, the receivers are susceptible to interference from other devices within the unlicensed bands in which they communicate. Finally, WRXs exceed the power budget available from cubic-mm batteries for long lifetimes.

1.3.4. Clock-Harvesting Receiver

With the pervasiveness of today's wireless standards, it is conceivable for a wake-up receiver to detect *an existing signal*, simultaneously eliminating the need to generate the beacon and conserving total energy in the network. We call this special type of receiver a clock-harvesting receiver (CRX). Using an existing signal, however, limits design flexibility in the wireless sensor network that could be used to better integrate the receiver with the rest of the system. Fortunately, there are many existing wireless

standard, such as Wi-Fi, broadcast TV, or cellular signals, which can be considered as a possible wake-up source.

The clock-harvesting receiver can be duty-cycled to further reduce synchronization energy as part of a tiered synchronization strategy. By coarsely duty-cycling the CRX with a sub-nanowatt timer, the CRX can be fully-powered only momentarily around the incoming clock edges. During the remaining time a CRX is asleep, so the receiver should be designed with a $<100\text{pW}$ sleep mode. By aligning each node to the arrival of the next harvested clock edge, the entire WSN is synchronized and may selectively enable communication radios based on higher-layer network policies (Fig. 1.12b).

1.4. Contributions of this Work

This research seeks to address the challenges of synchronization and communication in wireless sensor networks (WSNs) with wireless integrated circuit solutions. Nodes in these sensor networks are often energy-constrained, and the energy consumed to maintain synchronization often dominates the overall energy budget. While on-node, high-accuracy timers are the traditional approach, they require high power components like crystal oscillators and PLLs.

Much of my research instead focuses on a new wireless method of synchronizing a WSN—the clock-harvesting receiver. The clock-harvesting receiver is designed to extract a synchronization beacon from ambient wireless signals. Fortunately, with the pervasiveness of wireless technology today, ambient wireless signals exist virtually everywhere. My research analyzes the potential of several different wireless standards to act as a synchronization beacon for a sensor network. Since commercial wireless signals broadcast the synchronization signal, the signal no longer has to be generated in the

network, which saves energy. In addition, signals generated by wireless standards have known periodicity. As a result, communication can be scheduled, and a clock-harvesting receiver can be duty-cycled and only awoken shortly before the arrival of the next synchronization beacon. Finally, two prototype receivers were designed, fabricated, and tested to prove the applicability of this method.

My research also analyzes the challenges associated with wireless communication for a cubic-mm scale system. The small volume of such a system means a small battery. Unfortunately, small batteries are peak current limited, which heavily constrains the design of the wireless radio. The small volume also means that the antenna must be integrated onto the IC, and crystal-based synchronization is not an option. With these constraints, a complete energy analysis is presented. In addition, a prototype transceiver was designed and fabricated along with a prototype receiver. Test results for the receiver included.

A summary of my contributions is as follows:

- An analysis of existing wireless standards for their potential as a reliable and robust clock source for synchronizing a network using a low-power receiver architecture (Chapter 2)
- A demonstration of two fabricated RFICs which can harvest a clock from two different wireless standards (Chapter 3 and Chapter 4)
- A communication protocol and ultra-wideband (UWB) receiver architecture that meets the energy constraints of cubic-mm systems and peak power constraints of micro-batteries (Chapter 5)

- A demonstration of a fabricated receiver for a cubic-mm-scale system (Chapter 6)

Chapter 2

Potential Sources for a Harvested Clock

A clock-harvesting receiver (CRX) is designed to harvest a wake-up signal from an existing wireless standard for the purpose of synchronizing a wireless sensor network. By harvesting this signal from an existing wireless standard, the energy for wake-up comes from *outside of* the WSN. Since the standards were not designed for asynchronous wake-up, all harvested signals occur periodically, and the periodicity of the signal creates a clock if properly detected by the CRX. Because wireless standards were not designed for low-power synchronization however, not all wireless standards can be readily utilized as a clock source. The attributes of an ideal clock source are enumerated in Section 2.1, and later sections describe potential clock sources derived from several existing wireless standards, such as the GSM and 3G CDMA standards.

2.1. Attributes of an Ideal Harvested Clock Source

To realize low-power synchronization with a wake-up radio from an existing wireless standard, the beacon signal should satisfy several basic criteria. First, the signal should be pervasive so that a networked node placed anywhere on the globe can receive it. Second, the signal should be high-power to reduce the gain requirements in the wake-up radio along with the power consumption. Third, the beacon should have some component that repeats at a relatively low frequency so that it can be easily harvested as a wake-up

signal. Finally, the synchronization signal should be simple to demodulate in order to simplify the receiver and minimize power consumption.

2.2. Time Code Standards

The National Institute of Standards and Technology (NIST) broadcasts three different wireless signals across the United States specifically for time synchronization. They are provided by the WWVB, WWV, and WWVH radio stations [65]. Since these signals are intended for radio-controlled synchronization, they have many attributes which make them ideal clock sources for a clock-harvesting receiver. Thus, many commercial products already exist which utilize one or more of them. Accurate time is maintained at NIST using an atomic clock. As a result, radios which receive these signals often are called “atomic clocks”—though incorrectly [66]-[67].

2.2.1. NIST WWVB

The NIST WWVB radio station broadcasts a signal designed specifically to provide a clock reference across the United States for clocks and wristwatches. Thus, it is a great synchronization source for general purpose applications. The WWVB signal has the easiest demodulation scheme of any of the existing wireless standards considered as a clock source, and unlike the WWV and WWVH radio stations, this radio station broadcasts only encoded clock information. NIST operates the station out of Fort Collins, CO, so that the signal can be received anywhere in the continental United States, along with portions of Canada and Mexico.

The WWVB radio station radiates a 50kW signal that operates at a 60kHz carrier frequency [65]. Time information is encoded in pulse-width modulated (PWM) binary coded decimal (BCD) format at a data rate of 1b/s (Fig. 2.1). Thus, each decimal number

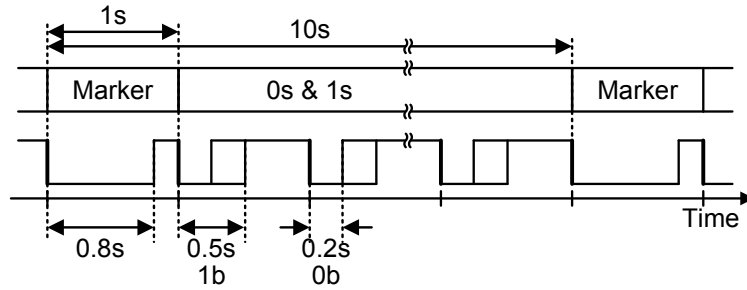


Fig. 2.1. The pulse-width modulated time code for the WWVB radio station. Marker bits occur once every 10s with zero bits and one bits during the other seconds.

is encoded as four binary bits, most significant bit first. The transmitted time code repeats once every minute and includes date (year, day), time (hour, minute, second), and flags (DST, leap year, leap second, etc.). Data is encoded as one of three possible bits (0-bit, 1-bit, and marker bit). At the start of each second, the transmitted power falls 10dB. Full signal power is restored 200ms, 500ms, or 800ms later to indicate the 0-bit, 1-bit, or marker bit, respectively. Marker bits are transmitted once every 10s on the 9's (9s, 19s, ..., 59s) as well as at the beginning of each minute (0s), such that two markers bits are transmitted together to indicate the end of one frame and the beginning of the next.

Most timing uncertainty is derived from path delay (20ms) and the on-time marker (1ms) [66]. Fortunately, sensor networks consume a small fractional area of the total broadcast area of the signal (a sensor network is much smaller than the size of the US), so local path delay variations are negligible. Therefore, the expected time uncertainty of a network based on this standard would be approximately 1ms if we can ignore additional delay in the digital signal processor (DSP).

Based on the format of the WWVB time code, several different clocks could be extracted. Perhaps the standard solution would be to demodulate the time code and extract coordinated universal time (UTC). Extracting the time code, however, requires a

receiver and DSP remain on for one minute or more in order to collect an entire frame. By demodulating UTC, nodes can schedule communication and periodically check the current time based on higher network policies. Thus, extreme duty-cycling ratios of days, weeks, months, or years would be feasible so long as latency is not a concern.

Alternatively, a receiver could be used to extract just the clock edges without attempting to determine the time code. This could be accomplished in several different ways, but the simplest approach would be to capture the falling edges which occur every second. This signal then could be used as a negative edge-triggered clock within the wireless sensor node. In reality, this approach could utilize the same commercial receiver designed for a traditional radio-controlled clock. These receivers consume as little as $132\mu\text{W}$ and have sensitivities of -115dBm [68].

Unfortunately, the NIST WWVB signal has a few disadvantages that make it a less ideal clock source for wireless sensor networks. First, the antenna is large. Because the center frequency is only 60kHz , commercial antennas are implemented using a parallel LC network with ferrite core inductor to help reduce the overall antenna size. Even so, the commercial antennas vary in size from 15mm to 100mm in length [69]-[70]. Second, the center frequency is too low for some of our lab equipment, including the network analyzer, which made the testing of our initial COTS prototype far more challenging. Third, the received signal strength is highly dependent on the time-of-day and weather conditions. According to the recommended design practices provided by NIST, commercial designs should plan to synchronize during dark path hours (when it is dark in both Fort Collins, CO and the clock's location) to best ensure a successful synchronization attempt [67]. In addition, they recommend that manufacturers attempt to

synchronize for a full *five* minutes before deciding that synchronization failed. Based our lab measurements, we verified that the received signal is not consistent, even for commercial systems. We purchased and tested several different units in Ann Arbor, and all of them produced inconsistent clock outputs. Finally, the low center frequency in combination with low received power creates a surprising circuit design challenge because flicker noise dominates in that regime.

While the atomic clock signal from the WWVB station has many advantages, the disadvantages create significant problems for small, low-power wireless sensor networks. If size, power, and reliability are of less concern, then the WWVB signal can serve as an excellent source for a harvested clock.

2.2.2. NIST WWV and WWVH

Unlike the WWVB radio station, the WWV and WWVH stations broadcast more than just a time code to the general public. As a result, these stations are less commonly used for radio-controlled clocks. Nonetheless, the time code standard embedded within their signals is continuous and relatively easy to harvest for synchronization [65]. Like the WWVB signal, the WWV and WWVH signals are operated by NIST and have a coverage area that includes most of the United States. The WWV tower is located in Fort Collins, CO, while the WWVH tower is located in Kihei, HI on the island of Maui.

Beyond the time code, the WWV and WWVH radio stations broadcast four major time and emergency information services each hour. First, the stations generate standard audio frequencies. Second, they broadcast tones announcing each 10-second, 1-minute, and 1-hour. Third, they transmit voice announcements of the current time each minute, and finally, they announce other emergencies and alerts [65]. Because of these other

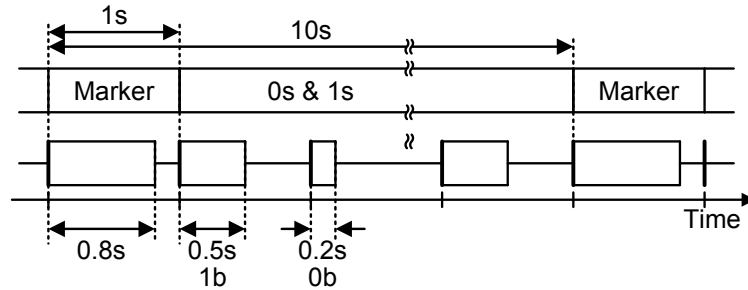


Fig. 2.2. The pulse-width modulated time code for the WWV and WWVH radio stations. Marker bits occur once every 10s with zero bits and one bits during the other seconds.

services, the time code signal is broadcast on a 100Hz subcarrier, which places the signal below the voice frequency band.

Both stations broadcast on the 2.5, 5, 10, and 15MHz carrier with the WWV radio station also broadcasting on the 20MHz carrier frequency. Thus, the signals can be received on shortwave radios. The stations employ double-sideband amplitude modulation which simplifies the necessary architecture for the receiver because an image-reject filter is not required.

The time code for WWV and WWVH signals are very similar to the code employed on the WWVB radio station. The time code follows binary coded decimal (BCD) format and has a bit rate of 1b/s. Each frame lasts for one minute and consists of time and date information in UTC. Data is pulse-width modulated as 0-bits, 1-bits, and position marker bits. Unlike WWVB however, each bit is identified by the length of time the signal is pulsed from the start of each second (Fig. 2.2). Finally, markers bits occur every 10s, and no pulse is transmitted on the first second of every minute.

Unfortunately, WWV and WWVH signals present a couple of practical challenges for sensor network synchronization. First, the broadcast power is less than the WWVB radio station, only 5-10kW versus 50kW. As a result, the received signal strength of the

Table 2.1. Global time code services.

Station	Frequency (kHz)	Country	Controlling Organization
BPC	68.5	China	National Timer Service Center (NTSC)
DCF77	77.5	Germany	Physikalisch-Technische Bundesanstalt (PTB)
JJY	40, 60	Japan	National Institute of Information and Communications Technology (NICT)
MSF	60	UK	National Physical Laboratory (NPL)

WWVB signal is typically better. In addition, LF signals, such as the WWVB signal, often follow a more stable propagation path as opposed to HF signals, such as the WWV and WWVH signals [65].

If signal strength is not a concern, however, then both of these signals could provide a good clock source for WSN synchronization. The time code is broadcast continuously and occupies a different portion of the electromagnetic spectrum from other signals broadcast concurrently on the channel. Because the time code exists at a fixed frequency offset from these other signals, it can be isolated after down-conversion using a simple low-pass filter. Like the WWVB signal, the time code itself can be demodulated to achieve synchronization, or the start of each pulse can be determined using an envelope detector and comparator.

2.2.3. Global Time Codes

The United States is not the only country with a time code standard. In fact, China, Germany, Japan, and the United Kingdom all have separate, though similar, time code standards. Like the standard operated in the United States, they employ PWM signals with BCD from low frequency carriers. As a result, the clocks could be harvested in a

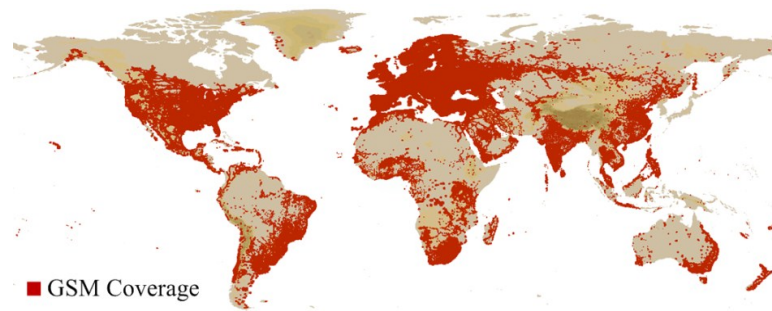


Fig. 2.3. The 2009 Global System for Mobile Communications (GSM) worldwide coverage map, excluding 3GSM coverage [75].

similar manner as the WWVB station. Table 2.1 provides a summary and comparison of each of the standards.

2.3. GSM Standard

Of the existing wireless standards, GSM is particularly well-suited to provide the synchronization source. It has extensive worldwide coverage (Fig. 2.3), and within the GSM standard, a broadcast channel exists in every cell to synchronize mobile devices and provide other services. If a wireless sensor network were deployed within a cell, such that every node could receive the same GSM broadcast signal, then each wake-up radio would harvest the same clock, with mismatch only from differences in propagation delay. For a sensor network with a 100m diameter, this mismatch error would be less than $1\mu\text{s}$. Furthermore, the harvested clock would have the accuracy of the GSM cell reference oscillator.

GSM is a worldwide standard for wireless telephony and data communication. The standard exists in four major frequency bands worldwide with physical carrier channels of 200kHz. The basic control services, such as frequency correction (FCCH) and broadcast control (BCCH), are provided together on a single radio frequency channel called the BCCH carrier [71]. Because these services are fundamental to network

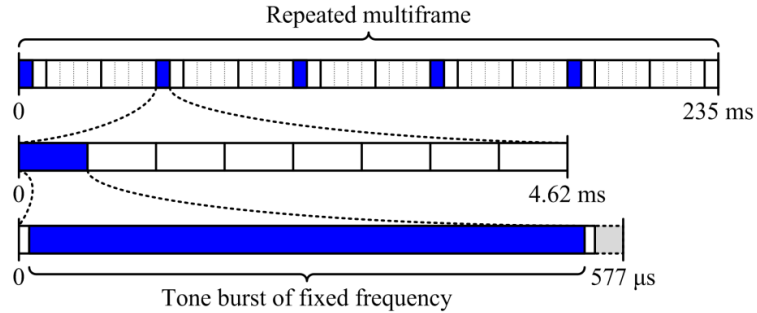


Fig. 2.4. The organization of the broadcast control channel carrier, which consists of repeated multiframes with a tone burst generated at a fixed frequency during five of the timeslots.

management, the BCCH carrier exists on every GSM cell worldwide, including newer GPRS- and EDGE-enabled cells. Thus, this signal is a good target for the wake-up of a wireless sensor network.

2.3.1. Broadcast Channel

GSM is modulated using Gaussian minimum shift keying (GMSK) as well as several other modulation schemes with pseudo-GMSK spectrums. Signals are divided into multiframes, which repeat approximately every 235ms (Fig. 2.4). During each multiframe on the BCCH carrier, a frequency correction signal is transmitted in five periodic bursts, called frequency correction bursts (FBs). During a FB a pure sinusoidal tone is broadcast by the GSM base station. This tone burst lasts for roughly 550 μ s at an offset frequency of 67.7kHz above the center frequency of the BCCH carrier. The rest of the time the BCCH carrier transmits modulated data, spreading the transmitted power over a broader spectrum. Therefore, during a FB a peak in the power spectral density (PSD) of the BCCH carrier can be observed at the FB offset frequency (Fig. 2.5). This FB repeats continuously at a repetition rate of 21Hz. By filtering around the FB offset frequency, a signal will be observed that looks like an amplitude modulated tone, repeating at 21Hz.

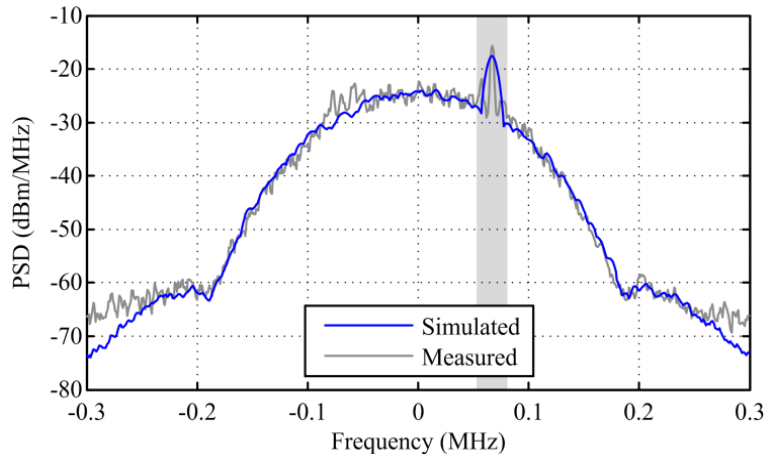


Fig. 2.5. Power spectral density (PSD) versus frequency for simulated and measured broadcast signals. The tone generated during a frequency correction burst is indicated in the highlighted region.

Since an amplitude modulated signal can be detected with a relatively simple demodulation technique, this signal is well-suited for low-power synchronization.

2.3.2. Guard Period

GSM modulates data in bursts. As a result, dead time exists between each burst called the guard period. Because a guard period is fundamental to the underlying packet format of the protocol, a guard period exists on every GSM channel, no matter the channel utilization. Signals in GSM are divided into time slots which last for approximately $577\mu\text{s}$. Of that time, a typical burst will last for $550\mu\text{s}$, and the guard period will last for $27\mu\text{s}$. If the energy in the entire 200kHz channel is measured over time, the channel looks like an amplitude-modulated signal with a repetition rate of roughly 1.7kHz. Since amplitude modulation does not require a complex receiver architecture, the signal would be a good clock source for network synchronization.

In addition, neighboring GSM channels often are synchronized to one another in time; thus, it should be possible to extract a clock from the entire FCC block of spectrum. If the block of spectrum is sufficiently wide, then a high-quality factor filter could be used to

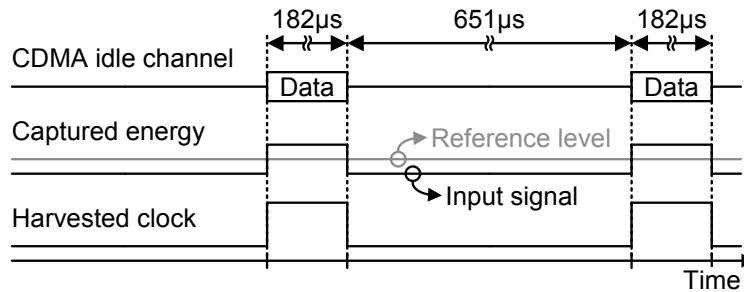


Fig. 2.6. CDMA signaling and clock extraction vs. time. Data during idle slots in 3G CDMA standard is on-off keyed.

select the entire band, and a receiver could energy-detect the entire band to generate 1.7kHz clock.

2.4. CDMA Standard

The 3G CDMA standard, formally the CDMA2000 EV-DO family of standards, uses a pseudo-random code to spread the transmitted signal into 1.25MHz channels [72]. Power is adjusted on the broadcast side to ensure a constant channel power, simplifying receiver detection. The standard employs time-division multiplexing, dividing channels into slots (Fig. 2.6). During idle slots, MAC and pilot data is the only information transmitted—no user data. Thus, the channel looks like an on-off keyed signal with an on-period of 182µs and an off-period of 651µs. A digital output pulse then can be generated by capturing the energy in the channel over time and comparing it to a reference level. Because slots run continuously on the CDMA channel, a sequence of digital pulses is seen at the output, creating a 1.2kHz clock (Fig. 2.7).

When users are present, the active slots assigned to a user are interpolated, so that idle slots exist on an occupied channel. Thus, only channels at full utilization don't have idle slots. Fortunately, this event is extremely rare because full channel utilization is not desired by the wireless carriers as well.

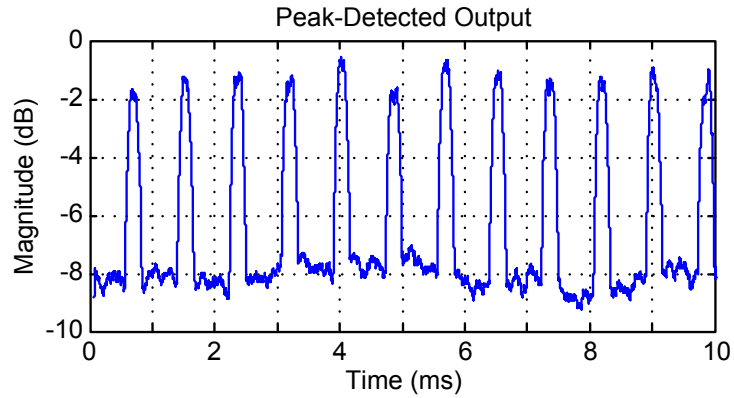


Fig. 2.7. Measured CDMA channel from Verizon Wireless vs. time using a prototype receiver with Matlab filtering.

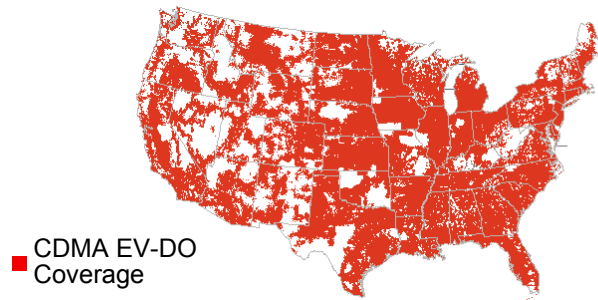


Fig. 2.8. Verizon Wireless 3G CDMA US coverage map [76].

The 3G CDMA standard is a pervasive signal, making it a good option for sensor network wake-up. Seven major bands exist worldwide, including the 850MHz and 1900MHz bands in the United States. The 1900MHz band was selected for this CRX based on signal strength measurements in our lab. Many major worldwide markets have 3G CDMA coverage, including the US and China. The US coverage map for 3G CDMA from Verizon Wireless is shown in Fig. 2.8.

2.5. Bluetooth Standard

Bluetooth is a wireless standard that operates in the 2.4GHz ISM band for personal area networks (PANs). While the standard is used extensively worldwide, the maximum coverage area of each Bluetooth network is small. Several different modes exist in the

standard; the major variants include the basic rate (BR), enhanced data rate (EDR), alternate MAC/PHY (AMP), and low energy (LE) modes. Of these variants, the LE mode is the newest, and it is designed specifically for low energy communication as the name suggests. As a result, this variant is best-suited for WSNs and provides a good clock source under certain operating conditions [73].

The Bluetooth LE (BLE) standard modulates data using Gaussian frequency-shift keying (GFSK), where a binary one is represented by a positive frequency shift and a binary zero is represented by a negative frequency shift. Furthermore, the standard states that the frequency-shift between a binary zero and one must always be greater than 185kHz. The bit rate and symbol rate are 1Mb/s and 1MS/s, respectively, while the band consists of 40 channels with each channel spaced 2MHz apart [73]. Because of the large frequency separation between channels and the reasonable frequency deviation between bits, it is possible to detect bits using a relatively low-power receiver.

In addition, all channel packets begin with a preamble of either 10101010b or 01010101b which provides a training sequence for synchronization within the standard. That sequence follows a minimum interframe space (IFS) of 150 μ s from the prior frame. Thus, a BLE-based clock-harvesting receiver could be designed to detect the known training sequence following a dead period in order to create a periodic clock.

Unfortunately, the time between frames is unknown, which makes scheduled communication difficult. Frames have variable length, and long dead periods of more than 30s can exist on the channel before communication resumes. The ISM band also does not provide an ideal clock source because the band is unlicensed. Therefore, other users could interfere with the desired Bluetooth radio. Finally, the coverage area of a

Bluetooth network is small, so one must ensure that a transmitter is placed in the proximity of the WSN so that it can be used for synchronization. Thus, a Bluetooth radio is unlikely to provide a reliable wake-up source unless the Bluetooth network have been specifically designed and positioned for use by a WSN. In that case, Bluetooth could provide an excellent source for sensor network wake-up.

2.6. ZigBee (IEEE 802.15.4) Standard

The IEEE 802.15.4 standard, commonly referred to as ZigBee, operates in several different unlicensed bands for use in PANs. Within the United States, the bands include the 900MHz, 2.4GHz, and 3.1-10.6GHz unlicensed spectrum [74]. In addition to operating in several bands, several different modulation schemes are permitted within the standard, including O-QPSK, BPSK, ASK, CSS, UWB, and GFSK. Each of these modulation schemes employs spreading codes for robustness against interferers as well. While the large number of options for a physical channel provides flexibility, it also adds complexity. Nonetheless, the standard has several synchronization services that can be exploited for WSN synchronization.

A coordinator provides synchronization services to other devices within a ZigBee network, and for beacon-enabled PANs, the coordinator broadcasts a beacon frame at fixed periodic intervals, which can be readily detected for use as a possible clock. The beacons mark the beginning of a superframe. Superframes have a programmable active period, which consists of 16 slots. In addition, a coordinator can add an inactive period to the superframe to conserve energy in the coordinator. As a result, a coordinator can guarantee an amplitude-modulated signal exists on the channel. That signal will have a

known inactive period in which no power is broadcast in the channel and a known start time at which the next superframe begins.

This solution has three important advantages. First, it does not require de-spreading by the receiver, which saves power. Second, the inactive period and overall superframe period are programmable, which provides design flexibility. Finally, having multiple frequency bands provides additional design flexibility.

Unfortunately, channel interference and communication range could be a problem in many applications. Like Bluetooth, ZigBee utilizes unlicensed spectrum; thus, interference is a concern because low-power receivers, like a clock-harvesting receiver, have simple demodulation schemes which makes them susceptible to interferers. Communication range is another significant limitation. The coverage area of a PAN is small. As a result, one must ensure that a transmitter is placed in the proximity of the WSN so that it can be used for synchronization. If both of these issues are resolvable however, then a beacon-enabled ZigBee PAN could provide an excellent synchronization source.

2.7. Summary

Table 2.2 summarizes the various standards that have been discussed in this chapter. Each standard is compared based on their operating frequency in the United States, the relative size of their network, the attributes of the harvested-clock signal, and the difficulty in implementing a useful clock-harvesting receiver. Of the time codes standards operated by NIST, the WWVB signal is designed solely for synchronization and should have higher signal strength; as a result, it would be easier to implement a receiver that reliably harvests a clock from that signal. Of the PAN networks, ZigBee is the only one

Table 2.2. Summary of potential wireless standards as harvested-clocks.

Standard	Center Frequency	Network Size	Harvested-Clock		Difficulty to Implement
			Source	Frequency	
WWVB	60kHz	US	Time Code	17mHz	Easy
WWVB	60kHz	US	Pulse Edge	1Hz	Easy
WWV/WWVH	5, 10, 15, & 20MHz	US	Time Code	17mHz	Moderate
WWV/WWVH	5, 10, 15, & 20MHz	US	Pulse Edge	1Hz	Moderate
GSM	850, 1900MHz	Cell	Broadcast	21Hz	Easy
GSM	850, 1900MHz	Cell	Guard Period	1.7kHz	Easy
CDMA	850, 1900MHz	Cell	Idle Slot	1.2kHz	Easy
Bluetooth	2400MHz	PAN	Training	Unknown	Hard
ZigBee	900, 2400MHz	PAN	Beacon	Variable	Moderate

with a controllable beacon rate. Thus, it would offer a more reliable clock source than Bluetooth.

Chapter 3

GSM-Based Clock-Harvesting Receiver

This chapter presents the results of a GSM-based clock-harvesting receiver (CRX) capable of extracting a 21-Hz clock embedded within the GSM standard for the wake-up of a wireless sensor network. The receiver is designed to replace an accurate on-node timer or wake-up receiver for synchronization. By harvesting the clock from a pre-existing and pervasive source, the WSN does not have to generate it within the network. In addition, the CRX can be heavily duty-cycled for use in a tiered synchronization strategy to greatly reduce synchronization energy. The receiver has a sub-100pW sleep mode in order to satisfy the power budget limitations set by a cubic-mm battery and the long lifetime requirements of many wireless sensor node applications. It is the first clock-harvesting receiver ever reported and therefore the first based on a GSM standard. Finally the functionality of two clock-harvesting receivers was verified by extracting a clock from the broadcast channel of a local cell tower.

3.1. Introduction

Wireless sensor networks (WSNs) are perceived as the next big step in a decades-long trend toward smaller, more pervasive computing. For many applications, long lifetimes are desired from small sensor nodes. As a result, low power consumption is critical.

A typical sensor node consists of five major components: a communication radio, a microprocessor, a battery, a timer, and sensors. Unfortunately, the battery often has

insufficient energy to operate a sensor node continuously for its desired lifetime. To alleviate this problem, energy usage must be reduced. The radio and timer easily dominate system energy usage when operated continuously for the purposes of synchronization. Thus, reducing the power consumed to maintain synchronization can greatly improve node lifetime [57]. The traditional (and perhaps obvious) approach to reducing average power consumption is to duty-cycle the communication radio and schedule communication using a high-accuracy on-node timer. To achieve high-accuracy, however, requires a high-power timer, resulting in only marginal improvement in the total synchronization energy.

An alternative approach replaces the accurate on-node timer with an always-on wake-up receiver (WRX) [62],[63]. WRXs allow the nodes in a WSN to operate in a low-power sleep mode and use a wireless signal to wake the nodes up. A traditional WRX remains on continuously during sleep mode, waking-up the node after a signal is broadcast within the WSN (Fig. 1.12a). As a result, a WRX enables fully asynchronous, interrupt-based communication.

To further conserve energy in the WSN by eliminating the need to broadcast a high-power wake-up beacon, a wake-up receiver can instead harvest a digital clock from an existing wireless standard such as Wi-Fi, broadcast TV, or cellular signals. We call this a clock-harvesting receiver (CRX). If all nodes in a WSN harvest and synchronize to the same existing wireless signal, then by transitivity they will be synchronized to each other. Furthermore, TV and cellular signals are broadcast at high power and from antennas placed high above earth ground. Therefore, the signals span long distances and can be used to synchronize very sparse WSNs.

This paper presents a CRX designed to extract a 21Hz clock from a synchronization signal embedded within every broadcast channel (BCH) of the GSM mobile phone standard for the wake-up of a WSN. The clock-harvesting receiver can be duty-cycled to further reduce synchronization energy as part of a hierarchical synchronization strategy. By coarsely duty-cycling the CRX (with an on-node $<1\text{nW}$ program-and-hold timer for example [54]), the CRX can be fully-powered only momentarily around the 21Hz GSM clock edges. During the remaining time the CRX is asleep, so the receiver is designed with a $<100\text{pW}$ sleep mode. By aligning each node to the arrival of the next GSM-harvested clock edge, the entire WSN is synchronized and may selectively enable communication radios based on higher-layer network policies (Fig. 1.12b).

3.2. System Overview

This section provides an overview of GSM-based synchronization, the system operation of the CRX and its architecture, and intermediate frequency selection.

3.2.1. GSM-Based Synchronization

GSM was selected as a wake-up source because it provides a pervasive and practical signal for use in WSN wake-up. GSM is a global standard (Fig. 2.3) that covers much of the inhabited world. A single broadcast channel (BCH) exists per provider on each GSM cell, and that channel operates at a dedicated frequency. Furthermore, channels in neighboring cells are allocated frequencies that minimize adjacent-channel interference, simplifying filter requirements (Fig. 3.1). Based on RSSI measurements throughout our 5-story building, the typical received power of a BCH ranges from -65dBm to -95dBm , with the strongest being in the 1900-MHz band [77].

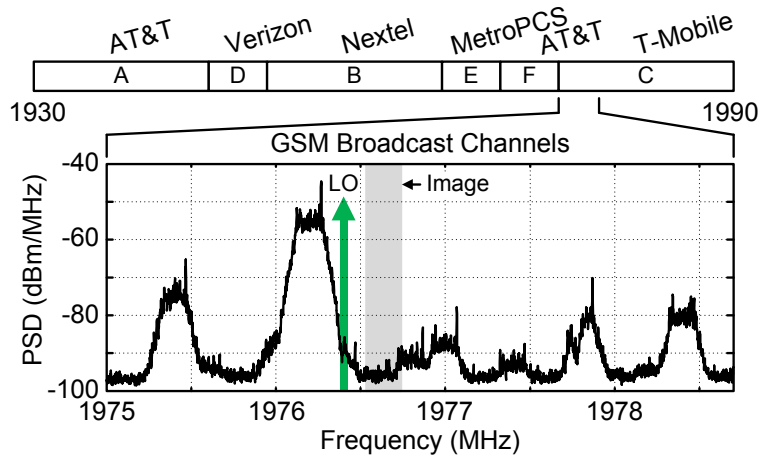


Fig. 3.1. GSM broadcast channels (BCHs) measured in our lab. These BCHs sit in the 1900-MHz band operated by T-Mobile, and they are spaced such that they don't interfere with each other.

3.2.2. System Operation

Fig. 3.2 outlines the operation of the receiver in time. The GSM standard employs Gaussian minimum-shift keying (GMSK) and other modulation schemes with pseudo-GMSK spectrums to modulate bursts of data in time [71]. Approximately every 46ms, a pure sinusoidal tone is transmitted on the GSM broadcast channel. This tone burst lasts for $577\mu\text{s}$ at an offset frequency of 67.7kHz from the center of the channel; otherwise, data is transmitted with a spectrum occupying the entire 200kHz channel. The bandpass filters (BPFs) in the CRX are tuned to overlapping halves of this BCH. When modulated data is transmitted by a GSM cell, the power is spread over the entire channel, passing equal signal levels through each offset BPF. During a tone burst, however, the signals captured along the two filter paths will differ. This difference in signal energies can then be detected, toggling the clock output.

3.2.3. System Architecture

The system architecture of the proposed CRX (clock-harvesting receiver) is outlined in Fig. 3.3. An off-chip SAW filter selects the entire 1900-MHz band, such that any GSM

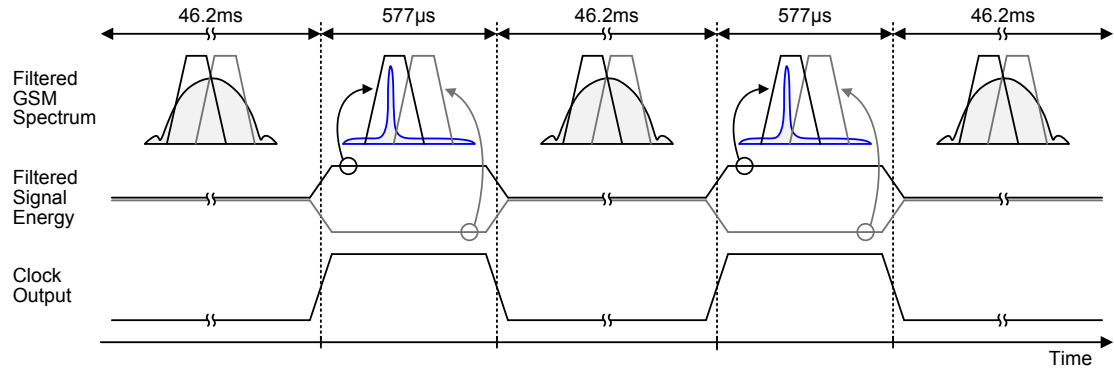


Fig. 3.2. Operation of a broadcast channel in time.

broadcast channel operating in the band can serve as a clock source. The input is amplified and down-converted to an intermediate frequency (IF) of 250kHz. Channel selection is done by using different fixed local oscillator (LO) frequencies and filtering at IF. Fixed- and variable-gain amplifiers at IF provide gain control. Following amplification, the signal is split into two paths, each with two G_m -C BPF stages that perform sub-channel selection. Each path then amplifies and envelope detects the signal. The voltages at the output of each ED are applied to a hysteretic comparator, generating a digital clock output from the harvested GSM signal.

3.2.4. Intermediate Frequency Selection

In a typical cellular network, the strongest channels in one geographic location do not sit in adjacent frequency channels (Fig. 3.1). Based on lab measurements, the worst case is an 800kHz separation between high-power channels; thus, a low IF of 250 kHz was selected. The IF is low enough that the image created from down-conversion lies in a low-power adjacent channel. A low IF also lowers the quality factor requirements on the BPFs, decreasing power consumption. At the same time, the IF is high enough such that flicker noise remains low.

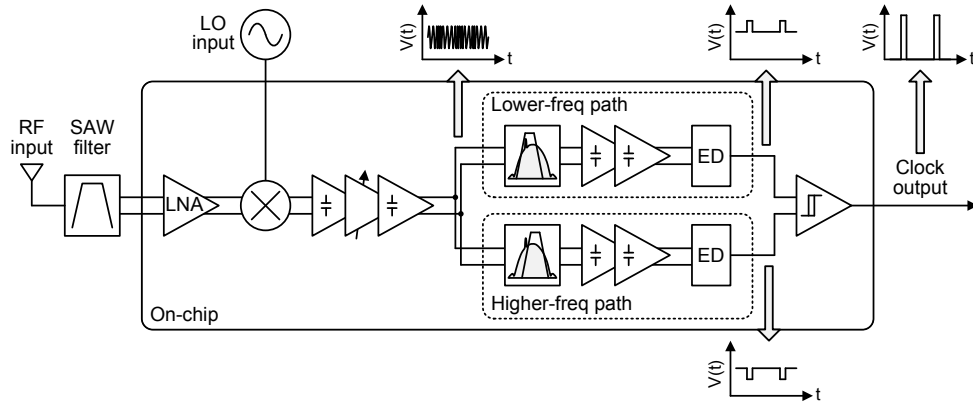


Fig. 3.3. System block diagram of the clock-harvesting receiver.

3.3. Bandpass Filter Model

In this clock-harvesting receiver, a digital clock output is generated during the intermittent tone bursts of the selected GSM broadcast channel (BCH). The tone burst is detected using filters tuned to different portions of the BCH. Therefore, optimizing the frequency response of these filters is critical to the functionality of this receiver.

Initially, we proposed the filter strategy in [78]. One filter captures the entire channel, while the other filter captures a very narrow band centered at the frequency of the tone burst. Unfortunately, the energy required to realize the narrowband filter in integrated circuits was prohibitive for a low-power system, so an alternative filter strategy was adopted. The new filter strategy uses BPFs tuned to overlapping halves of the GSM channel. They are optimized to equalize the received power during spectrally-wide data transmission and tuned to maximize received power differences during the tone bursts.

To determine the optimal characteristics of the BPFs, GMSK data was generated in MATLAB, and the bandwidths of ideal Butterworth filters were swept for several different filter orders. Then, the clock error rate (CER), defined as the number of clock errors over the expected number of clock outputs, was recorded. Based on simulations

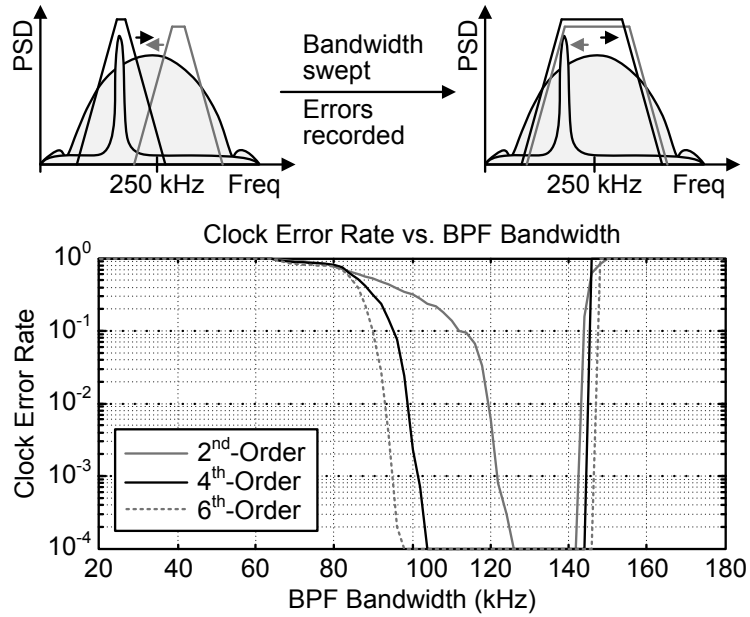


Fig. 3.4. Simulated clock error rate versus the bandwidth of each bandpass filter.

shown in Fig. 3.4, 6th-order BPFs would allow for the largest variation in bandwidth while still having less than a 10^{-4} CER. At the same time, 6th-order filters, when realized with actual circuits, would require more power and system complexity than lower-order filters. Fourth-order BPFs, therefore, provide a good trade-off between bandwidth, power, and complexity. Simulations predict that less than 10^{-4} CER is achievable with filter bandwidths between 104kHz and 144kHz. The actual filter bandwidths for this receiver were then tuned to 121kHz and 118kHz for the lower-frequency and higher-frequency paths based on these simulations.

3.4. Circuit Design

The system block diagram of the clock-harvesting receiver is shown in Fig. 3.3. The circuits in the receiver provide four primary functions: band selection and down-conversion, gain, clock detection, and sleep-power minimization.

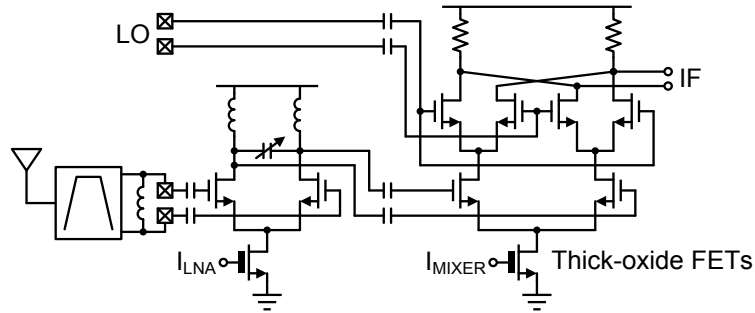


Fig. 3.5. RF front-end, including SAW filter, LNA, and mixer.

3.4.1. RF Front-End

The RF front-end consists of a SAW filter, low-noise amplifier (LNA), and a mixer (Fig. 3.5). The SAW filter serves two primary functions. First, the filter serves as a balun for single-to-differential conversion from the antenna to the differential inputs of the receiver. Second, the filter serves as a bandpass filter for the downlink side of the 1900-MHz band (also called the PCS band). The GSM standard separates the uplink side of the 1900-MHz band for mobile-phone-to-base-station communication from the downlink side of the band for base-station-to-mobile-phone communication. To prevent possible saturation of the RF front-end from the uplink side of the 1900-MHz band, the uplink portion is rejected by the filter. The filter is designed to match to 50Ω single-ended at the input and 100Ω differential at the output.

To reduce active power in the receiver, the system has only one RF gain stage before mixing down to a low IF. The RF inputs are AC-coupled on-chip directly to an unmatched fully-differential low-noise amplifier with inductive loading (Fig. 3.5). The inductors are sized to maximize their impedance in the band-of-interest, and a varactor was added in order to tune center frequency. The varactor is sized to account for process variation while still passing every channel in the 1900-MHz band. The LNA is fully-differential in order to provide common-mode rejection, simplify biasing, and shut-off

the bias current in sleep mode. While a single-ended implementation would require half the power in active mode for equal gain, higher active power was traded for lower sleep-mode power consumption with the use of a thick-oxide FET for current biasing.

The LNA output is AC-coupled to a double-balanced Gilbert-cell mixer (Fig. 3.5). A Gilbert mixer provides good common-mode rejection and also has less RF and LO feedthrough than a single-ended implementation. The remaining RF and LO feedthrough is attenuated by the IF gain stages. Headroom is a challenge, but the problem is mitigated with the use of low threshold voltage devices for the RF and LO inputs and moderately sized load resistors. As with the LNA, the bias current of the fully-differential mixer can be shut-off in sleep mode with the use of a thick-oxide FET.

The local oscillator is generated off-chip and is used to select the desired GSM broadcast channel. The bandpass filters at IF have a measured tuning range that allows for up to 161ppm in frequency drift from the LO while still maintaining proper receiver functionality. In addition, the broadcast channels at a given geographic location can be measured with either a spectrum analyzer or a mobile phone in field test mode. The desired BCH then can be determined, so that a fixed LO can be used with the CRX. Based on these specifications, a low-power local oscillator should be feasible. For example, FBAR-based fixed-frequency LOs consuming less than 100 μ W have been reported [25]-[27], which could be used to target a specific GSM broadcast channel.

3.4.2. Baseband Gain Stages

Once the signal is at IF, amplification is provided by four differential fixed-gain amplifiers (FGAs) and one variable-gain amplifier (VGA). Each fixed-gain amplifier consists of low-threshold voltage input FETs, resistive loads, and split-source with

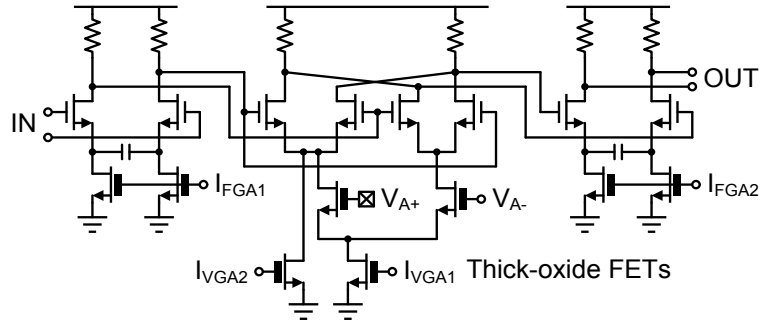


Fig. 3.6. Baseband amplifiers, including two fixed-gain amplifiers and one VGA.

capacitive-coupling (Fig. 3.6) [62],[64]. To reduce noise, the first FGA after the mixer is sized differently from later gain stages. The first gain stage has a simulated bias current of $3\mu\text{A}$ and load resistance of $167\text{k}\Omega$. Later gain stages, on the other hand, have a simulated bias current of $1\mu\text{A}$ and load resistance of $500\text{k}\Omega$. The gain stages are biased in weak inversion, which provides good gain efficiency (g_m/I_D) and linearity. The simulated gain for all stages is 13dB .

The split-source capacitor is placed between the input source terminals of the FGA. The capacitor creates a bandpass response to the gain, resulting in no DC gain and eliminating accumulated offset voltages. Without accumulated offset voltages, common-mode feedback becomes unnecessary.

Because the intermediate frequency is only 250kHz , resistive loading provides ample bandwidth, while also making DC-coupling possible. Precise sub-channel filtering is performed in the Gm-C bandpass filters further down the signal path, so the passband of these FGAs must extend below and above the frequencies of interest. As a result, the lower-cutoff frequencies are set to 25kHz for the first gain stage and 27kHz for the later gain stages based on simulations. The upper-cutoff frequencies are set to 11MHz and 17MHz , respectively.

The topology of the variable-gain amplifier is very similar to that of a double-balanced Gilbert mixer or an analog multiplexer [79]; however, this topology adds a current source for one of the input differential pairs (Fig. 3.6) and is based on an unfolded version of [79]. Gain is varied by changing the voltage difference between V_{A+} and V_{A-} . Only one of these voltages (V_{A+}) is set off-chip, while the other is fixed on-chip. High-threshold NFETs were used for the gain inputs (V_{A+} and V_{A-}) in order to provide a larger input tuning range, so that a fixed off-chip voltage tuning can provide stable on-chip gain.

To understand the operation of this VGA, it is easiest to first ignore the second current source (I_{VGA2}). In this case and when V_{A+} and V_{A-} are equal, equal currents are steered through each input differential pair, producing equal gain. Each differential pair, however, shares a single pair of resistive loads with inputs 180° that are out-of-phase. As a result, the voltages cancel, and the gain is $0V/V$ ($-\infty$ dB). Therefore, as V_{A+} ramps from rail-to-rail while V_{A-} is held constant, the gain decreases until V_{A+} and V_{A-} are equal, then increases again—a non-monotonic response. A non-monotonic response makes external tuning needlessly difficult. To address this, a second tail current (I_{VGA2}) is added. The second current source ensures that the left differential pair always has more current than the right pair, so that the gain increases monotonically with V_{A+} . For this VGA, the first current source is set to $1\mu A$ in simulation, and the second current source is set slightly larger.

3.4.3. Filtering and Clock Extraction

To detect the clock embedded in the GSM standard, the amplified IF signal is split into two sub-channels: a lower-frequency path and a higher-frequency path. Each signal

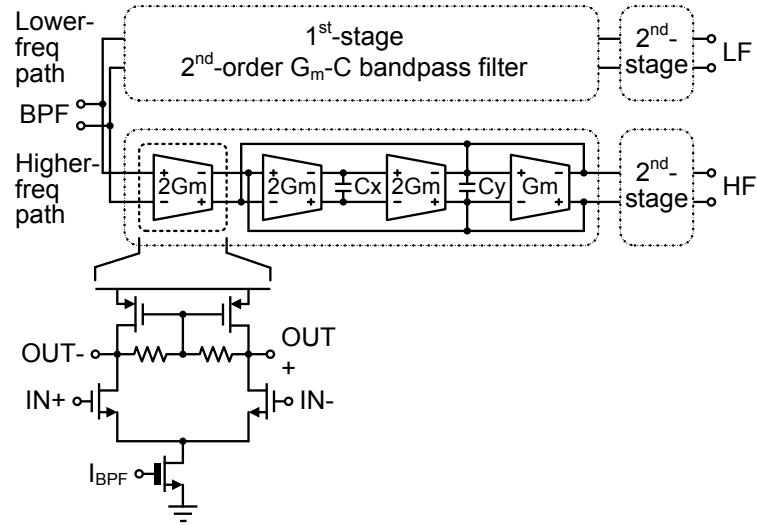


Fig. 3.7. Two-stage bandpass filters for the lower-frequency and higher-frequency paths. The higher-frequency path has a 2-stage G_m -C bandpass filter tuned to overlapping halves of a GSM broadcast channel.

Each G_m -C stage consists of a differential 2nd-order filter with unit transconductors for better matching. The unit transconductors consist of differential pairs with PMOS load and resistive CMFB for self-biasing (Fig. 3.7). Each unit consumes only 200nA. Very large resistance is achieved by using reverse-biased FETs. In addition, one self-biasing network is shared by all unit transconductors connected to the same differential signals. In other words, two self-biasing networks exist per G_m -C bandpass filter stage; one network across C_x and the other across C_y . The capacitors in each path and for each stage are sized to provide a Butterworth response, and unit MIM capacitors are used for better matching. The magnitude response of each BPF is tuned to equalize the received power through overlapping halves of the GSM channel during data bursts and to maximize received power differences during tone bursts.

The bandwidths of the BPFs along the lower- and higher-frequency paths are 121kHz and 118kHz, respectively. They are optimally determined by system simulations to

minimize the clock error rate (CER), defined as the number of clock errors over the expected number of clock outputs (Fig. 3.4) [78]. Additionally, the use of two wideband filters decreases quality factor requirements over the detection method we originally proposed in [78], reducing the power required to filter the GSM channel.

The BPFs produce nominal gain in order to reduce active power. Each Gm-C BPF stage consists of seven unit transconductors. At 200nA/unit-Gm the transconductors don't generate significant gain, but each stage still draws more current than a single FGA. Thus, additional gain was generated after filtering using two FGAs for each path.

The signal powers in the lower- and higher-frequency paths are converted to DC through two passive envelope detectors (EDs). The EDs have differential inputs and single-ended output, and each ED draws 100nA. The 21-Hz harvested clock has pulses with 577 μ s duration. Therefore, large 100pF capacitors are connected to ground in order to decrease bandwidth and slow the response at the output of each ED. To eliminate instantaneous differences at the output of the EDs, the two paths are capacitively-coupled together with a 50pF capacitor, so that high frequency signal components are shorted between the outputs.

The received signal powers through the lower-frequency and higher-frequency paths are compared using a 2-stage continuous-time comparator with programmable hysteresis (Fig. 3.8). The ED outputs are directly coupled to the input PFETs of the comparator. The load of the first stage of the comparator creates hysteresis, which prevent spurious switching of the output. The load consists of a combination of cross-coupled and diode-connected NFETs. The relative drive strength of the cross-coupled and diode-connected NFETs sets the hysteresis levels. Additional parallel NFETs can be digitally-enabled with

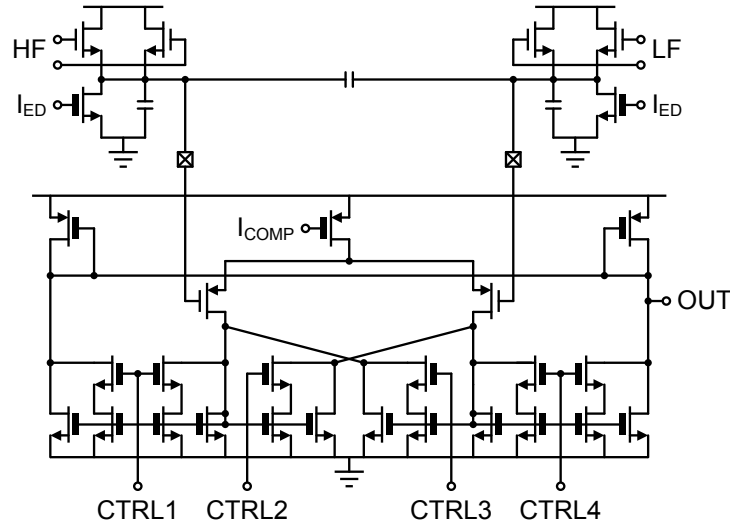


Fig. 3.8. Envelope detectors and continuous-time comparator.

four NMOS switches in order to adjust the initial hysteresis levels either up or down. The second stage provides differential-to-single-ended conversion as well as additional gain. Finally, the harvested 21-Hz clock output is sent through a buffer to be driven off-chip.

3.4.4. Sleep-Power Minimization

In heavily duty-cycled operation, sleep-mode energy dominates active-mode energy; however, most recently published low-power radios do not report sleep-mode power in their designs. In this CRX, thick-oxide tail devices were added to every stage in the receiver's signal path and its bias generation in order to minimize sleep-mode leakage currents (Fig. 3.5 - Fig. 3.8). Using thick-oxide tail devices, however, increases active-mode energy due to the larger headroom requirements for the high-threshold voltage devices. In this case, 300mV of additional headroom was used for the tail devices, increasing active power by 30% but reducing sleep power by more than two orders of magnitude. Sizing of the thick-oxide devices was done to maximize the ratio between active-mode and sleep-mode current.

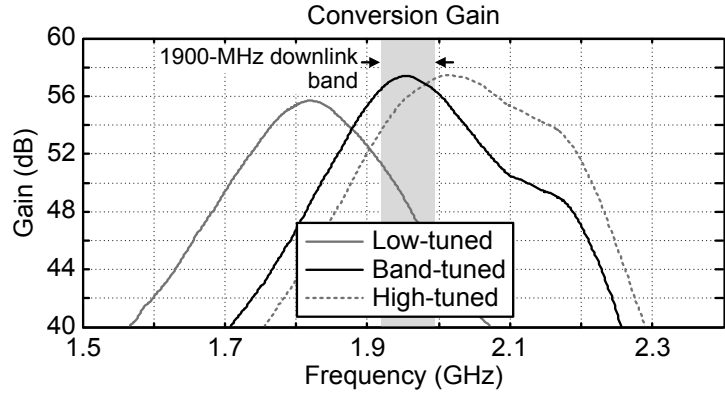


Fig. 3.9. Conversion gain for different tunings of the varactor.

3.5. Measurement Results

The clock-harvesting receiver was fabricated in a 0.13 μ m CMOS process with MIM capacitors. The entire receiver operates from a single 1V supply. The conversion gain of the CRX is shown in Fig. 3.9 at three differently tuned varactor voltages in the LNA. The peak conversion gain measured at sensitivity is 57dB, and gain-control is achieved by tuning the VGA and the tail bias currents of each stage. The measured bandwidth of the LNA is 140MHz.

The center frequency of the receiver was measured across varactor voltage for three die (Fig. 3.10). The center frequency plotted corresponds to the frequency at which conversion gain peaked for each varactor voltage. The LNA for each die can be tuned with the varactor over a worst-case frequency range of 1.83 to 2.01GHz. Therefore, all three die can be tuned over the entire downlink side of the 1900-MHz band, enabling the selection of any broadcast channel in the US.

The BPFs for the lower- and higher-frequency paths are critical to the overall functionality of the CRX. Their magnitude response is measured at the output of the envelope detectors (Fig. 3.11). The bandwidths of the BPFs along the lower- and higher-

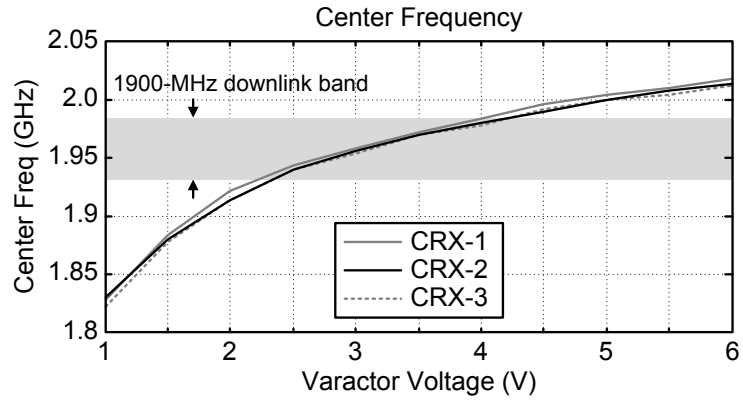


Fig. 3.10. Center frequency across varactor voltage for multiple die.

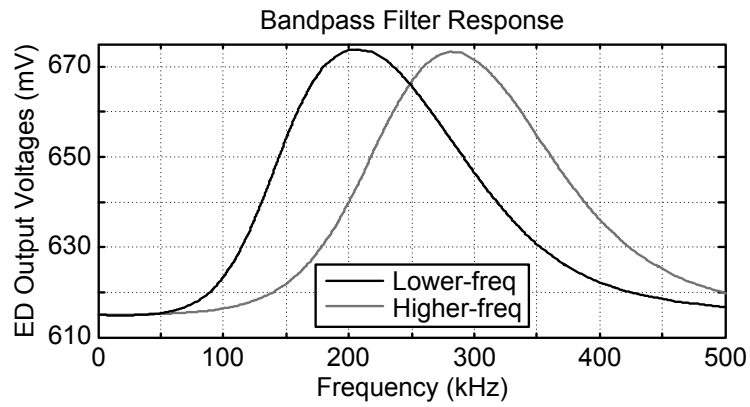


Fig. 3.11. Magnitude response of the bandpass filters.

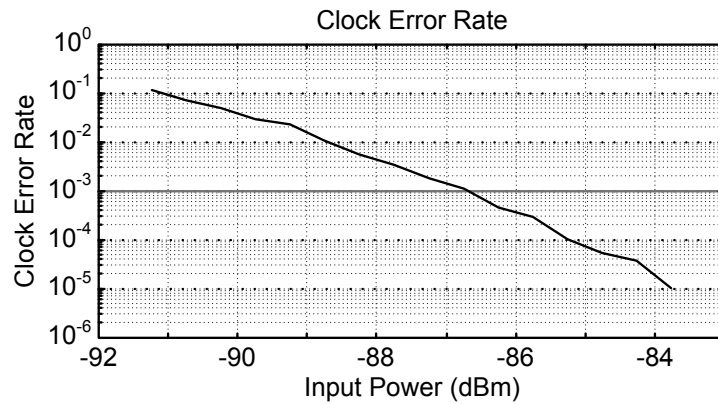


Fig. 3.12. Clock error rate vs. input power.

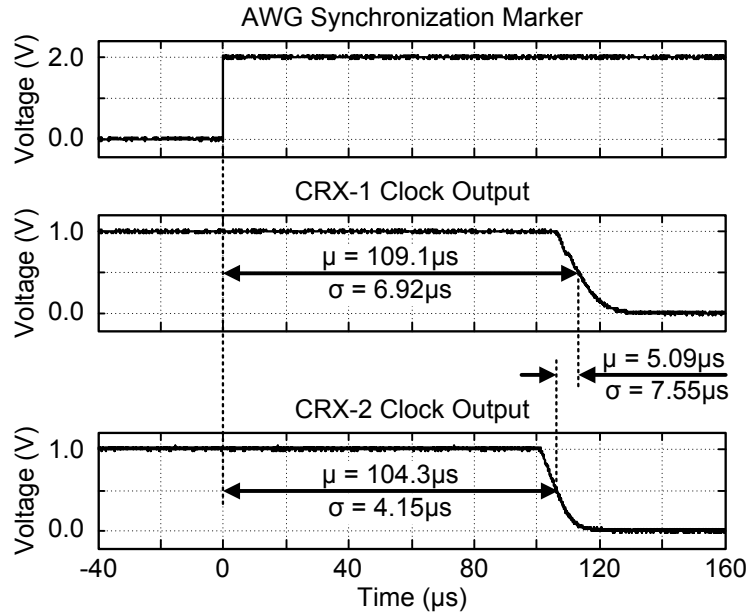


Fig. 3.13. Delay and jitter measurements of two clock-harvesting receivers.

frequency paths are 121kHz and 118kHz, respectively, based on system simulations to minimize the clock error rate (Fig. 3.4). Additionally, both the bandwidth and center frequency of each filter is tunable in order to change the intermediate frequency if necessary.

The measured CER (clock error rate) versus input power is shown in Fig. 3.12. At a CER of 10^{-3} , the peak sensitivity is -87dBm with a total power consumption of 126 μ W, of which the front-end consumes 98 μ W and the baseband consumes 28 μ W. At a reduced sensitivity of -60dBm while maintaining 10^{-3} CER, the total power consumption of the receiver can be reduced to 67 μ W. Proper operation was verified at input powers up to -5dBm. In sleep mode, the leakage power of the system is 81pW.

The path delay and clock jitter were measured for two different die (Fig. 3.13). A pseudo-GSM broadcast channel was generated on an arbitrary waveform generator (AWG), then up-converted and sent into the two clock-harvesting receivers. At the start

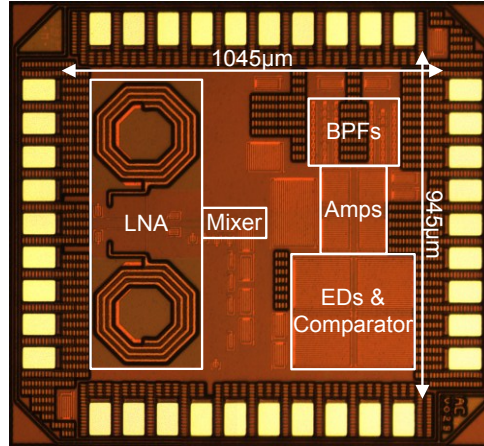


Fig. 3.14. Die photo.

of each tone burst, a synchronization marker was generated by the AWG. Delay and jitter were then recorded. From this setup, the average delay in clock output is $109\mu\text{s}$ for CRX-1, and $104\mu\text{s}$ for CRX-2, which is predominately due to the slow response of the EDs. The measured jitter at peak sensitivity is $57\mu\text{s}$. At higher signal powers, the jitter reduces to approximately $7\mu\text{s}$ worst case. The average chip-to-chip time difference is $5.1\mu\text{s}$ with a jitter of $7.6\mu\text{s}$, which suggests that network synchronization can be achieved with better than $50\mu\text{s}$ accuracy ($6\sigma+\mu$). The start-up time from sleep mode to active mode is roughly $500\mu\text{s}$, limited by slewing at the ED outputs.

The core circuit area occupies approximately 0.99mm^2 (Fig. 3.14). The area is dominated by inductors for the LNA and capacitors for the EDs.

The signal-to-interference ratio (SIR) was measured for interfering GSM signals in neighboring channels (Fig. 3.15). A broadcast channel was generated at a fixed frequency while a second interfering channel was generated at a frequency up to 800kHz above or below the BCH frequency. The SIR was varied until the CER reached 10^{-3} . Based on measured BCH allocations in the lab, interfering BCHs reside at least 800kHz away from the target BCH (Fig. 3.1). The worst case SIR is -14dB at this frequency offset. Thus, the

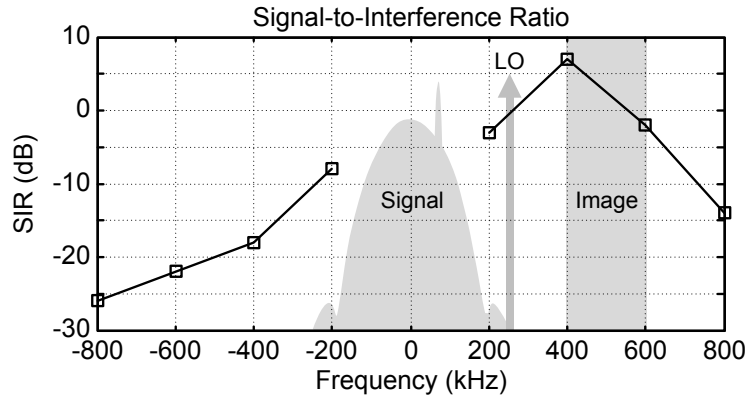


Fig. 3.15. Signal-to-interference ratio for neighboring broadcast channels.

highest power BCH always can be harvested by the CRX, assuming a typical GSM channel allocation policy.

To illustrate how a WSN could be synchronized using CRXs, two clocks were harvested simultaneously from the 1976.2MHz GSM broadcast channel of a local tower (T-Mobile) using two CRXs placed 10cm apart on a table. The resulting clock outputs are shown in Fig. 3.16. The envelope detected outputs for one CRX are shown in the figure as well. During wideband bursts, the envelope-detected outputs are approximately equal as expected. During the tone burst however, the ED outputs differ, toggling the comparator output of both receivers. The photo of the test setup is shown in Fig. 3.17. Both CRXs extracted the real GSM clocks in our lab using small monopole antennas.

This clock-harvesting receiver is compared with several recent wake-up receivers and low-power communication receivers for WSNs, and the active power consumption is plotted versus sensitivity (Fig. 3.18). The active power for other works excludes power for the local oscillator when possible or applicable to create a more fair comparison with this work. A detailed performance summary is provided in Table 3.1 along with a comparison to a few select WRXs.

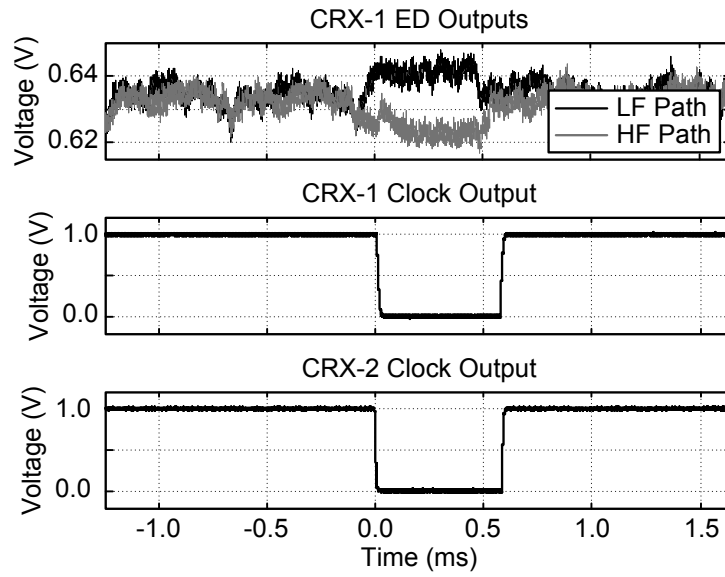


Fig. 3.16. Simultaneously harvested-clocks of two CRXs from a local GSM broadcast channel.

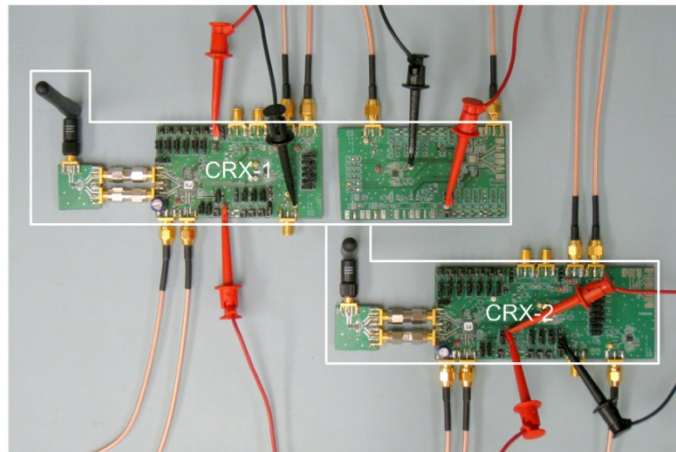


Fig. 3.17. Setup of two CRX debug boards receiving a real GSM signal in our lab.

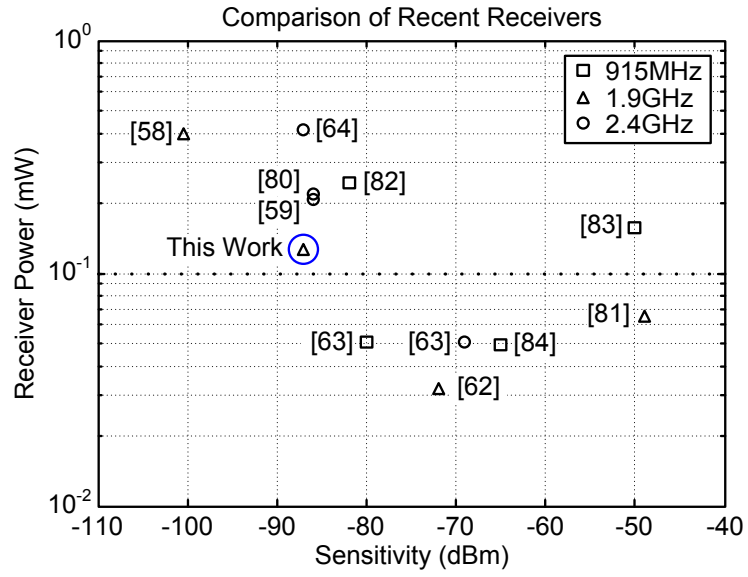


Fig. 3.18. Comparison of power consumption vs. sensitivity of recent low-power receivers.

Table 3.1. Measured receiver performance and comparison.

	This Work		[62]	[63]	[64]
Process	0.13 μ m		90nm	90nm	65nm
Type of RX	Clock-harvest		Wake-up	Wake-up	Wake-up
V _{DD}	1.0V		0.5V	0.5V	1.2V
Area	0.99mm ²		0.1mm ²	0.36mm ²	0.2mm ²
Sensitivity (@ 10 ⁻³ BER)	-87dBm		-72dBm	-80dBm	-87dBm
P _{Active} P _{Sleep}	126 μ W	81pW	52 μ W	51 μ W	415 μ W
P _{Front-End}	98 μ W	56pW	8 μ W	51 μ W	199 μ W
P _{Baseband}	28 μ W	25pW	24 μ W		
Jitter (@ Sensitivity)	57 μ s		N/A	N/A	N/A
Gain _{Conversion}	57dB		Unknown	Unknown	61dB
Center Freq	1.9GHz		2GHz	915MHz, 2.4GHz	2.4GHz
t _{Start-Up}	500 μ s		Unknown	Unknown	Unknown
LO Accuracy	161ppm		10 ⁵ ppm	N/A	5x10 ³ ppm

Chapter 4

CDMA-Based Clock-Harvesting Receiver

This chapter presents the results of a CDMA-based clock-harvesting receiver (CRX) for the wake-up and synchronization of a wireless sensor network (WSN). Unlike the receiver reported in Chapter 3, this clock-harvesting receiver extracts a 1.2kHz clock embedded within the 3G CDMA standard. In addition, this CRX harvests its clock from the on-off keyed idle slots of the CDMA standard using energy-detection. As a result, the receiver does not require a high-frequency local oscillator, providing a complete circuit solution. Removing the LO also reduces volume requirements, which makes it easier to integrate this receiver into future small-scale sensor nodes. Like the previously discussed GSM-based CRX, this receiver is designed for low-power, heavily duty-cycled operation with a low-power on-node timer. The receiver consumes less than 100pW while asleep, so that it can operate within the power budget of a cubic-mm sensor node with a desired lifetime of a year. It is the second clock-harvesting receiver ever reported and the first based on a CDMA standard.

4.1. Introduction

As discussed in Chapter 1, society has been witness to and participant in an on-going computing revolution as new classes of computing technology have displaced older technologies as the dominant market force—from mainframes decades ago to smartphones today. With the rise of each new class of computing technology, the systems

have become smaller and more ubiquitous than the last [1]. As this trend continues, wireless sensor networks (WSNs) are widely perceived as the next major class of computing technology. WSNs have garnered interest for a variety of potential applications, including infrastructure and health monitoring [8],[11]. These applications, however, require sensor nodes with both long lifetimes and small volumes, which results in highly energy-constrained systems.

To alleviate this problem, energy usage must be reduced in the sensor node. In particular, the energy used by the communication radio and system clock can easily dominate overall system energy usage when operated continuously. Since both components maintain synchronization between nodes across the WSN, reducing their power consumption can greatly improve node lifetime [57].

The standard approach to reducing synchronization energy in a low-power wireless device is to duty-cycle the communication radio and schedule communication using a high-accuracy on-node timer. One alternative solution is to replace constant on-node, high-accuracy timing with network-wide synchronization using a wake-up receiver (WRX) [62]-[64]. Unfortunately, a WRX assumes that a high-power wake-up beacon is readily available, which can be detected across the entire WSN. For applications spanning large distances such as structural health monitoring on bridges [11], this may be unreasonable for the energy-constrained network. Therefore, it would be advantageous to use a wake-up receiver for interrupt-based communication while eliminating the need to broadcast the wake-up beacon from within the energy-constrained WSN. Fortunately, with the pervasiveness of modern wireless standards, a wake-up receiver can instead

harvest a digital clock from an existing wireless standard, creating a clock-harvesting receiver (CRX).

This chapter presents the first CRX designed to harvest a 1.2kHz clock embedded within the idle slot of the 3G CDMA mobile phone standard. Unlike the GSM-based CRX we previously reported in Chapter 3, this receiver does not require a local oscillator to extract the CDMA-based clock, providing a complete circuit solution. Like the previously published CRX, the receiver is designed to be coarsely duty-cycled and only awoken momentarily around the incoming clock edges from the CDMA broadcast. With a harvested clock edge, the nodes in the WSN are synchronized and may selectively enable communication radios based on higher-layer network policies.

4.2. System Overview

This section describes the relevant attributes of the 3G CDMA standard that are utilized in the operation of this CRX. This section then provides an overview of the system architecture employed to harvest a clock from the standard.

4.2.1. System Operation

This receiver extracts a clock from the 3G CDMA standard for the wake-up of a WSN. The 3G CDMA standard, formally the CDMA2000 EV-DO family of standards, uses a pseudo-random code to spread the transmitted signal into 1.25MHz channels [72]. Power is adjusted on the broadcast side to ensure a constant channel power, simplifying receiver detection. The standard employs time-division multiplexing, dividing channels into slots (Fig. 2.6). During idle slots, MAC and pilot data is the only information transmitted—no user data. Thus, the channel looks like an on-off keyed signal with an on-period of 182 μ s and an off-period of 651 μ s. A digital output pulse then can be

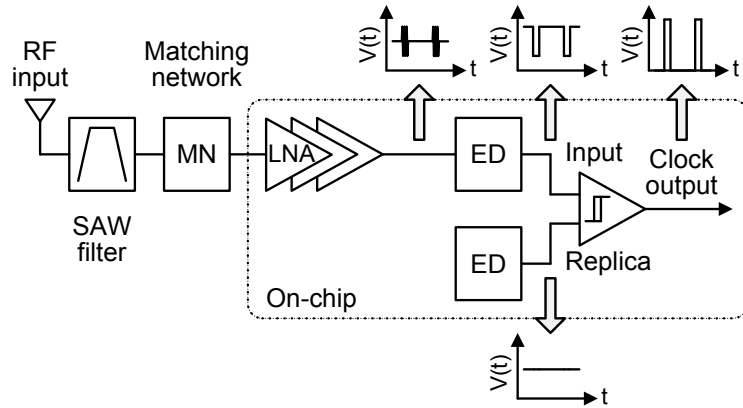


Fig. 4.1. Block diagram of the clock-harvesting receiver.

generated by capturing the energy in the channel over time and comparing it to a reference level. Because slots run continuously on the CDMA channel, a sequence of digital pulses is seen at the output, creating a 1.2kHz clock. When users are present, the active slots assigned to a user are interpolated, so that idle slots exist even on an occupied channel. Thus, only channels at full utilization don't have idle slots. Fortunately, this event is extremely rare because it is not desired by the wireless carrier as well.

The 3G CDMA standard is a pervasive signal, making it a good option for sensor network wake-up. Seven major bands exist worldwide, including the 850MHz and 1900MHz bands in the United States. The 1900MHz band was selected for this CRX based on signal strength measurements in our lab. Many major worldwide markets have 3G CDMA coverage including the United States, China, and India. The US coverage map for 3G CDMA from Verizon Wireless is shown in Fig. 2.8.

4.2.2. System Architecture

The proposed clock-harvesting receiver has the system architecture depicted in Fig. 4.1. The received signal is passed through an off-chip filter, which selects the desired portion of the 1900MHz PCS band. The single-ended signal then is sent through a

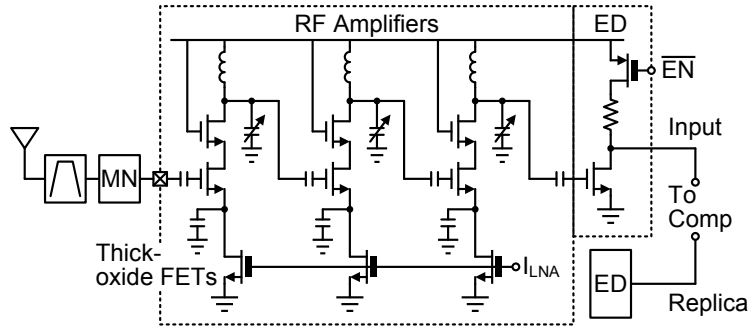


Fig. 4.2. Schematic of the cascoded RF amplifiers and the envelope detectors. Every current path includes a thick-oxide tail FET for low leakage currents while asleep.

matching network onto the chip. Next, the signal goes through three cascaded RF amplifiers, which can be tuned to provide gain control. After amplification, the signal is down-converted directly to DC using an envelope detector (ED). The ED along the main signal path provides the input to the hysteretic comparator, while a replica ED provides the reference signal. The comparator output is a digital clock harvested from a 3G CDMA signal.

4.2.3. Frequency Selection

A narrowband filter with high quality factor is required for the proper functionality of this receiver. The filter must select only the desired 3G CDMA channels, while rejecting all other channels in the 1900MHz PCS band in order to prevent saturation of the receiver front-end. Based on laboratory measurements for our area, the desired 3G CDMA channels make up an entire FCC-defined block of spectrum in the PCS band. Thus, the filter can be relatively wideband and realizable.

While this system architecture does place significant design requirements on the filter, there are several advantages to this approach. First, the filter itself can be a passive element, requiring no power from the energy-constrained node. Second, an energy-detection-based receiver eliminates the need for a high-frequency LO which is required in

the GSM-based CRX presented in Chapter 3 [85]; therefore, a filter is the only additional component required. Finally, typical RF systems often require off-chip filtering anyway in order to prevent saturation of the receiver front-end, leaving node complexity unchanged.

4.3. Circuit Design

The circuits in this clock-harvesting receiver have four major functions: RF gain, down-conversion, clock detection, and sleep-power minimization.

4.3.1. Block Selection & RF Gain

A filter with high quality factor selects the desired block of spectrum before sending the signal to an external matching network and then on-chip (Fig. 4.2). The matching network is employed to maximize power delivered to the receiver and provide additional channel selectivity over typical on-chip solutions. The network consists of a series capacitor and a shunt inductor. Once the signal arrives on-chip, it is AC-coupled directly to the input of a single-ended RF amplifier with LC load. The input amplifier is one of three identically sized RF amplifiers which together provide the RF gain for the receiver. The amplifiers are cascoded to reduce Miller effects at the input node of each stage as well as reduce feed-through between stages. A single-ended implementation is employed to save power. Current biasing is accomplished with the use of thick-oxide tail FETs for low leakage current in sleep mode. To prevent gain degeneration in the RF amplifiers, capacitors were added to create an AC-short across the biasing FETs. The LC load is implemented with a varactor to provide center frequency tuning.

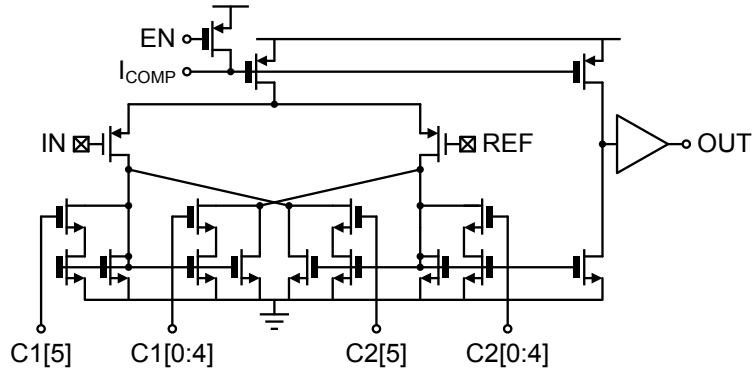


Fig. 4.3. Schematic of the continuous-time hysteretic comparator.

4.3.2. Down-Conversion

The receiver directly down-converts the RF signal to DC using an envelope detector for energy detection (Fig. 4.2). The ED is implemented using a single-ended common source amplifier, and down-conversion is achieved by utilizing the inherent squaring relationship found in the drain current expression, where $i_D \propto v_{GS}^2$. The squaring effect results in direct conversion to DC. As a result, a local oscillator is not required in this receiver, which saves energy by not having to generate a RF signal on-chip. In addition, removing the LO makes the system smaller for cubic-mm sensor nodes, as discussed in Chapter 1.

For duty-cycled operation, a thick-oxide header is placed above the load resistor. When the receiver is on, the header adds finite resistance; however, this on-resistance is small relative to the load resistance, so that it has no effect on performance. When the receiver is asleep, however, the thick-oxide FET is turned-off, and the header stops current flow to ensure low sleep-mode power consumption.

4.3.3. Clock Detection and Harvesting

The down-converted signal is sent into a two-stage continuous-time comparator with hysteresis for clock harvesting (Fig. 4.3). Two additional inverters on the comparator

output buffer the output and drive the clock off-chip. The comparator inputs are set by matched envelope detectors to ensure equal input voltages, and large capacitors are placed on the input nodes of the comparator to prevent spurious switching at the output. Like the other circuit blocks in the receiver, the replica ED, comparator, and output buffer all use thick-oxide FETs to minimize power consumption while asleep. The comparator is disabled in sleep-mode by pulling I_{COMP} to the positive supply rail with a PMOS keeper. The hysteresis levels are tunable from 12 digital control bits.

4.3.4. Sleep-Power Minimization

This receiver is designed to operate as part of a tiered synchronization strategy along with a low-power timer. When the CRX is heavily duty-cycled, however, sleep-mode energy dominates active-mode energy. Thus, thick-oxide tail devices were added to every stage in the receiver in order to minimize sleep-mode leakage currents (Fig. 4.2). Using thick-oxide tail devices, however, increases active-mode power by more than 20% due to the additional headroom requirements for high-threshold voltage devices. Thus, sizing of the thick-oxide devices was done to maximize the ratio between active-mode and sleep-mode current.

4.4. Measurement Results

The clock-harvesting receiver was fabricated in a $0.13\mu\text{m}$ CMOS process with varactors, MIM capacitors, and inductors. The conversion gain of the receiver with an external matching network is plotted versus frequency in Fig. 4.4 at three different input powers. Due to the non-linear down-conversion of the ED, the gain through the receiver varies with input power. The S_{11} of the receiver is better than -10dB in the 1900MHz band due to the matching network, and the center frequency of the receiver is tuned to

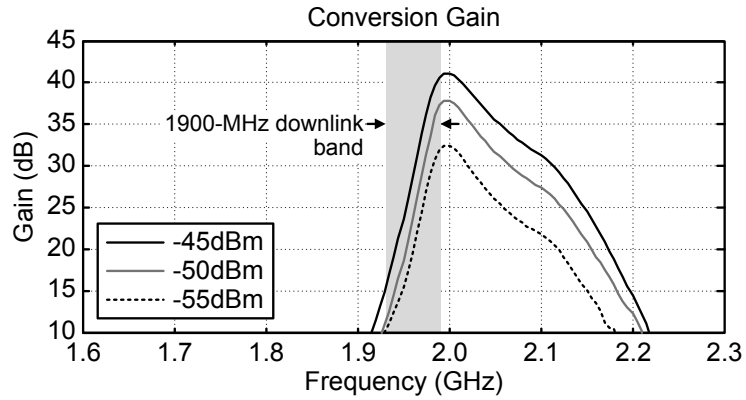


Fig. 4.4. Conversion gain for different receive powers.

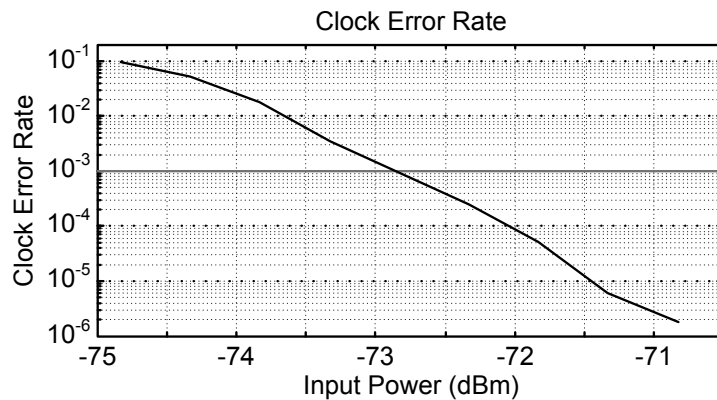


Fig. 4.5. Clock error rate vs. input power.

maximize gain in the 1900MHz band. Consequently, it is tuned to the upper edge of the band. With an input signal of -50dBm, the peak conversion gain is 37dB.

The clock error rate (CER) of the CRX is shown in Fig. 4.5, where the CER is defined as the number of clock errors divided by the expected number of clock outputs. At 10^{-3} CER, the sensitivity is -73dBm based on the average measured power of an idle slot using an Agilent U2000A Power Sensor. More specifically, the received power is -67dBm during the 182 μ s of pilot and MAC data followed by 651 μ s of no received signal power (Fig. 2.6) per the 3G CDMA standard, yielding an average received power of -73dBm. The CRX has a total power consumption of 298 μ W. The front-end consumes

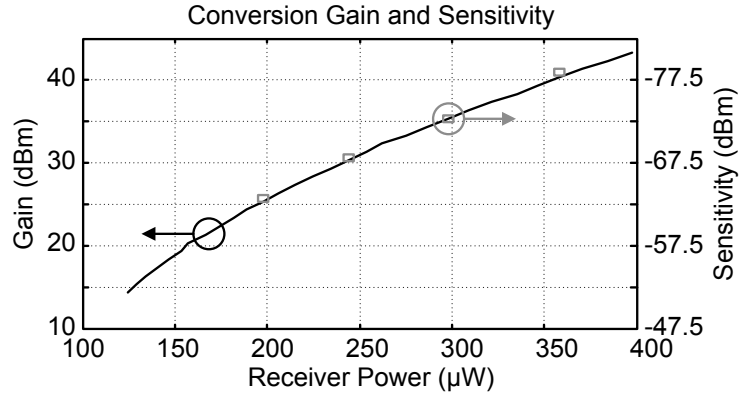


Fig. 4.6. Receiver gain and sensitivity at 10^{-3} CER vs. active power.

295μW, which accounts for the vast majority of the power consumed in the receiver, while the envelope detectors and comparator consume 2.3μW and 0.5μW, respectively. The measured rms jitter at peak sensitivity is 7μs, and the delay through the receiver is 27μs.

The CRX power consumption can be adjusted using the tail bias currents of the RF gain stages. As power consumption varies, the gain and sensitivity of the receiver also vary due to the non-linearity of the squaring mixer (Fig. 4.6). Furthermore, the receiver is gain-limited, so the gain and sensitivity scale together. The black curve in Fig. 4.6 is the measured gain of the receiver as power consumption varies. This curve also represents the expected sensitivity of the CRX for the same power consumption. Sensitivity was measured at four different power levels marked by the gray boxes. Thus, the desired trade-off between power consumption, gain, and sensitivity for a particular usage model can be determined using Fig. 4.6. In addition, a closed-form expression with the power consumed by the CRX, P , can be used to predict receiver sensitivity, S , with an R^2 value of better than 0.99.

$$S = -24.52 \ln(P) + 66.7. \quad (4.1)$$

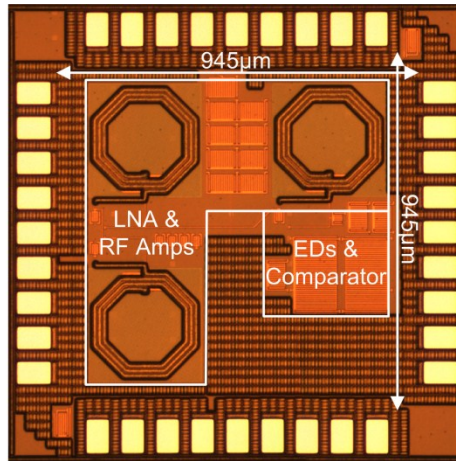


Fig. 4.7. Die photo.

where P is in μW and S is in dBm .

Proper operation was verified at input powers up to -4dBm , which corresponds to the maximum deliverable power from our vector signal generator. The measured leakage power of the system is just 44pW in sleep mode, and the start-up time from sleep mode to active mode is approximately $80\mu\text{s}$.

The receiver operates from a single 0.75V supply, and the core circuit area occupies approximately 0.89mm^2 (Fig. 4.7). The comparator hysteresis levels can be configured via 12 control bits, which can be varied from -12mV to $+28\text{mV}$ on the positive edge transition and -9mV to $+32\text{mV}$ on the negative edge transition. No additional bias signals or circuits are required. A harvested-clock output from the CRX is shown in Fig. 4.8 along with voltage levels on the envelope detector outputs. Measured receiver performance is summarized in Table 4.1 and compared with recent wake-up and clock-harvesting receivers.

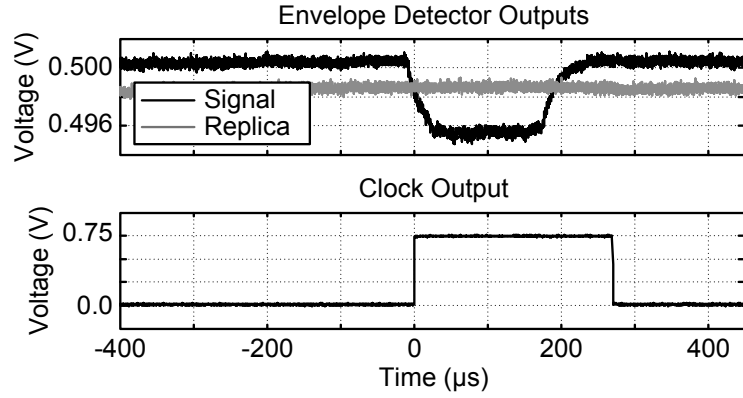


Fig. 4.8. Harvested-clock from a 3G CDMA channel.

Table 4.1. Measured receiver performance and comparison.

	This Work		[62]	[85]	
Process	0.13 μ m		90nm	0.13 μ m	
Type of RX	Clock-harvest		Wake-up	Clock-harvest	
V_{DD}	0.75V		0.5V	1.0V	
Area	0.89mm ²		0.1mm ²	0.99mm ²	
Sensitivity	-73dBm		-72dBm	-87dBm	
$P_{Active} P_{Sleep}$	298 μ W	44pW	52 μ W	126 μ W	81pW
$P_{Front-End}$	295 μ W	39pW	8 μ W	98 μ W	56pW
$P_{Baseband}$	3 μ W	5pW	24 μ W	28 μ W	25pW
LO Accuracy	N/A		10 ⁵ ppm	161ppm	
Start Time	80 μ s		Unknown	500 μ s	

Chapter 5

Communication Protocol and for an Energy-Constrained Radio

A communication radio is an integral part of a cubic-mm-scale wireless sensor node. Because these nodes are also highly energy-constrained, a careful analysis of the many design trade-offs is necessary in order to develop a functioning, energy-balanced system. This chapter specifies all of the necessary attributes for a communication radio that can be operated within the limitations of a cubic-mm form-factor and a micro-battery. Based on these system constraints, a communication protocol was developed that permits duty-cycled operation between every bit, including synchronization bits.

5.1. Design Constraints

In order to develop a real communication radio for cubic-mm systems, it is necessary to first enumerate constraints on the system. In this way, the problem becomes bounded, and several important design decisions can be made. While some of these constraints are perhaps self-evident, they are defined in order to be thorough. In addition, several constraints initially discussed in Chapter 1 are presented here. They are included with this chapter for completeness and to tailor the discussion to this specific system.

5.1.1. Total Node Volume

The first significant constraint on the design of communication radio is the volume of the node. For a cubic-mm sensor node, the total volume is 1mm^3 for everything. A

conventional sensor node typically includes a solar cell, battery, processor, memory, sensor, radio, antenna, and crystal oscillator. At such a small volume, each component volume in the node must be minimized. In addition, a stacked die approach becomes necessary. An alternative approach, such as a printed circuit board, would be too large, and a system-on-chip precludes the designer from optimizing each die layer for the specific requirements of each component in the system.

Several factors bound the dimensions of the sensor node. These include the crystal oscillator, battery, die thickness, antenna length, and pads. The smallest commercial crystal oscillator available today measures 2.0mm x 1.6mm x 0.8mm [20]. Thus, the total volume of the crystal oscillator alone is 2.56mm^3 , so it is not an option.

The micro-battery available from Cymbet measures 1.375mm x 0.85mm x 0.15mm with two contact points along the top near one of the 0.85mm edges [32]. Meanwhile, die can be thinned to about 0.05mm. At least three die are required for the node: solar cell & sensor, processor & memory, and radio & antenna. Thus, the total thickness of these die comes to 0.15mm. Adding battery thickness and 0.01mm for bonding adhesive between each layer, then the total thickness of the sensor node comes to 0.33mm.

The length of the antenna plays a major role in its overall performance. At this scale we simply want to maximize its length because antenna gain is reduced by operating farther away from the $\lambda/4$ frequency. In addition, RF gain efficiency improves as center frequency decreases. On one extreme, if the antenna measures only 1mm in length, then $\lambda/4$ frequency of the antenna is 75GHz. On the other extreme, if the antenna measures 4mm, then the frequency reduces to 18.8GHz. Fortunately, several bands of unlicensed

spectrum exist nearby. These include the ISM band at 2.4GHz, the UWB spectrum up to 10.6GHz, the ISM band at 24GHz, and the ISM band at 61GHz.

Pads are required along one edge to connect between die in the stack. Connections are necessary for the battery supply voltage, a regulated digital supply voltage, a ground connection, and a 2-wire communication protocol. These connections require 10 pads; one pad to bond up to the next higher layer, and one to bond down to next lower layer. Assuming a minimum 70 μ m pad pitch plus some additional space for edge spacing and possibly extra pads, then the minimum width along the pad edge is 0.9mm.

Taking into account all of the factors above, a 2.7mm x 1.1mm x 0.33mm sensor node provides a practical trade-off. 0.33mm provides enough height for multiple stacked circuit die as well as the battery. 1.1mm provides enough width to connect 10 pads along the edge of the die and leave room a bit of room for additional pads if necessary. In addition, it provides a practical aspect ratio for the ICs. Finally, 2.7mm maximizes the length of the on-chip antenna as much as possible while staying within the overall 1mm³ form-factor.

5.1.2. Battery Current Draw

The second major constraint on the system is the maximum current draw from the micro-battery. The radio must operate within the specifications of a micro-battery which limits current draw to 10 μ A [32]. Recent receivers, meanwhile, consume on the order of 100 μ A, even for low-power wake-up receivers [62]-[64]. Therefore, the radio will need to be duty-cycled. While the radio is asleep, charge can be stored onto a capacitor which the radio must draw from while it is awake.

5.1.3. Battery Supply Voltage

Lithium-ion micro-batteries have a 3.0-4.2 range in supply voltage that creates another constraint on the system. There are two main options to resolve this issue. One option is to step-down the voltage, and the other option is to operate directly at the battery voltage, while keeping in mind that the system is severely current-limited.

While step-down voltage regulation can be accomplished on-chip, it is not very efficient, less than 80% [30],[89]. In other words, at least 20% of the available power is being consumed as heat and does nothing useful for the system. Also, the output load capacitors for regulators are typically much larger than allowed in a cubic-mm system. Without off-chip capacitors, the total load capacitance will be relatively small, which limits the potential loading on the output to maintain stability. Switching converters do offer one advantage; the step-down voltage ratio results in a step-up current ratio.

The alternative is to operate directly from the battery voltage. Some isolation is still necessary between the battery and radio, however. The isolation circuit must limit current from the battery, so that the battery is protected when more than $10\mu\text{A}$ is drawn by the radio. Fortunately, the efficiency of a current limiter should be much greater than 80% as less than 720mV are dropped across the isolation circuit from a battery at a nominal voltage of 3.6V. Due to the severe constraints of the battery, the radio must operate from the battery voltage to save energy.

5.1.4. Local Oscillator

Another constraint is the local oscillator. As determined earlier, a crystal oscillator cannot fit within a cubic-mm form-factor; thus, it must be eliminated to satisfy integration requirements. While an on-chip PLL would still be helpful, an external loop

filter is not possible because of volume constraints. A VCO could still be generated on-chip, but it would have to be free-running. In addition, a VCO consumes considerable power because a large signal is required to commutate the mixer.

For a transmitter, larger signals are delivered to the output. As a result, a VCO might be a reasonable solution for the transmit side, but the receive side would be better to implement using an energy-detection-based receiver. This type of receiver is amenable to on-off keying (OOK) and pulse-position modulation (PPM). Fortunately, both modulation schemes improve integration and simplify the receiver, which can save energy.

5.1.5. Baseband Clock

The quality of the baseband clock is critical to the overall design of the radio. Without a crystal reference, an on-chip clock must be used for bit-level timing. Unfortunately, on-chip clocks have limited accuracy, which results in drift between the transmitter (TX) and receiver (RX). Therefore, synchronization is limited by the accuracy of the clock. In addition, the clock must be low power because it cannot be duty-cycled during a packet. Based on previously published on-chip clocks [50]-[53], an accuracy of 1% was considered achievable and assumed for the design.

5.1.6. Center Frequency

The operating frequency of the radios is important for the overall link budget. Antenna gain is reduced by operating away from the $\lambda/4$ frequency, and these losses in the antenna result in higher gain requirements in the transmitter and receiver. From the discussion on volume earlier in this chapter, the length of the antenna was set to 2.7mm; thus, the $\lambda/4$

frequency is 28GHz, and the closest operating frequencies are 2.4GHz (ISM), 10GHz (UWB), and 24GHz (ISM).

While the antenna is one important factor, power consumption in the radio increases when operating at higher center frequencies. In addition, higher frequencies have greater attenuation through the wireless channel over the same distance.

5.1.7. Process Technology

The fabrication process constrains the design of the transceiver in several fundamental ways. First, the process must have a high f_t , so gain is possible at the center frequency. In addition, the gain efficiency (g_m/I_D) must be high, so that high gain is achievable while consuming less power. Finally, the noise efficiency (N/I_D) should be low in order to improve receiver performance. Since SiGe processes are known to have better performance in all of these categories than Si processes, only SiGe processes were considered.

To determine the best process technology for this transceiver, several BiCMOS processes in SiGe are compared in Table 5.1 [86],[90]-[96]. The selected process should be able to operate in the range of the battery voltage, which makes 8HP less desirable. At the same time, 8HP has the highest f_t for both high-performance and high-breakdown NPN transistors. The f_t is sufficient for all of the technologies, however—even if current is constrained to only 100 μ A to better match the current limitations in the receiver. All of the processes have MIM capacitors available for the on-chip storage capacitor, but the capacitors in the 8WL and 7WL processes are higher density. Low leakage current FETs are necessary to support the requirements of the radio, making 7HP and 7WL better choices. Of these processes, however, only 8HP and 7WL have a consistent run schedule

Table 5.1. Comparison of BiCMOS SiGe processes.

	IBM 8HP	IBM 8WL ^a	IBM 7HP ^a	IBM 7WL
Feature Size	0.13 μm	0.13 μm	0.18 μm	0.18 μm
Num of Metals Layers	6 (7 ^a)	8	7	7
MIM Capacitance	1fF/ μm^2	4.1fF/ μm^2	1fF/ μm^2	4.1fF/ μm^2
<i>Regular V_T NMOS</i>				
Supply Voltage	1.2V	1.2V	1.8V	1.8V
Off Current	300pA/ μm	300pA/ μm	<80pA/ μm	19pA/ μm
<i>Max I/O V_T NMOS</i>				
Supply Voltage	2.5V	3.3V	3.3V	3.3V (5.0V ^a)
Off Current	10pA/ μm	30pA/ μm	<1pA/ μm	0.3pA/ μm
<i>High-Performance NPN</i>				
V_{CE} Breakdown	1.77V	2.4V	2.0V	3.3V
Off Current	<1pA/ μm	<1pA/ μm	<1pA/ μm	<1pA/ μm
Peak f_t	200GHz	103GHz	120GHz	60GHz
Max f_t @100 μA	95GHz	70GHz	64GHz	42GHz
<i>High-Breakdown NPN</i>				
V_{CE} Breakdown	3.55V	4.7V	4.75V	6.0V
Off Current	<1pA/ μm	<1pA/ μm	<1pA/ μm	<1pA/ μm
Peak f_t	57GHz	54GHz	35GHz	29GHz
Max f_t @100 μA	54GHz	51GHz	31GHz	28GHz

^aNot an available option through MOSIS.

of multi-project wafers (MPWs) through MOSIS. As a result, 8WL and 7HP are not viable options because of their limited availability without assuming the high cost of a

dedicated run. Based on all of these constraints, the IBM 7WL process was selected for the design and fabrication of the transceiver.

5.1.8. Sleep Timer

A low-power timer is the only component in a wireless sensor node to remain on continuously. It must keep time, so that a node knows when to wake-up and communicate to other nodes in the network. The accuracy of these timers, however, is relatively poor. Based on the limitations of these timers, however, 196ms of synchronization uncertainty can be expected after 1hr [55]. Assuming a worst case of just 3σ , two nodes could wake-up approximately 600ms apart every hour.

5.2. Initial Design Analysis

Ideally, the radio could operate continuously on the capacitor alone for an entire packet. By doing so, synchronization between the TX and RX is simplified. Unfortunately, this is not possible because the on-chip capacitance is too small.

As an example, let's consider the capacitance in the IBM 0.18um BiCMOS process [86] which is modern and has several different capacitors available, including MOS, vertical-natural (VN), and MIM capacitors. Assuming 100% fill of these capacitors, the total capacitance is approximately 40nF on a 2.7mm x 1.1mm die. At a discharge current of only 100 μ A from a 3.6V supply, the capacitor would be fully discharged in 1.44ms. Even under these completely unrealistic conditions, the radio must be duty-cycled because 1.44ms is well below the timing uncertainty of the sleep timers (600ms when waking-up every hour).

For a more realistic approximation, pads, inductors, transistors, and density rules will limit the actual amount of area that can be filled with capacitors. A conservative

approximation assumes only 20% fill for MIM capacitors and no MOS or VN capacitors. Based on these assumptions, the on-chip storage capacitor reduces to 2.5nF.

As an additional comment, the maximum discharge current of the battery ($10\mu\text{A}$) is much less than the discharge current of the radio ($>100\mu\text{A}$). As a result, the battery cannot appreciably recharge the storage capacitor while the radio is on since the battery can extend on-time by less than 10%. Thus, the battery recharge current is ignored for much of this analysis when the radio is on.

5.3. Impulse Radio UWB

Impulse-radio ultra-wideband (IR-UWB) is well-suited to the design requirements of a communication radio in an energy-constrained system. IR-UWB is naturally duty-cycled, so that the radio can be put to sleep between incoming pulses which would allow the storage capacitor to recharge.

On the transmit side, a transmitter is only on for a 2ns pulse—4ns when including turn-on and turn-off time. While the average current must remain just $10\mu\text{A}$, the peak current can increase up to the duty-cycling ratio (on-time / off-time). Similarly for the receiver, the average current is still $10\mu\text{A}$, but the peak current is dictated by the ratio of time the receiver is on to the time it's off.

Having chosen UWB, the center frequency is set to 10GHz for three reasons. First, the ISM bands at 2.4GHz and 24GHz are narrow and have a small fractional bandwidth making them a bad choice for UWB. Second, maximum performance of the antenna occurs at 28GHz, so the lower-end of the UWB spectrum makes less sense. Finally, path loss is less in the wireless channel and the circuits are lower power by not operating in the 60GHz band.

5.4. Communication Protocol

The communication protocol must live within the constraints established above. In particular, the radios must employ one of a couple different modulation schemes: either on-off keying or pulse-position modulation. In addition, the transmitter and receiver must be duty-cycled between incoming pulses and operate on an average current of only $10\mu\text{A}$ from the battery. With this information, we can begin to develop a communication protocol.

5.4.1. Peak Currents

The peak on-currents of the transmitter and receiver are dictated by different factors. Since the on-time of the TX is fixed at 4ns , the data rate determines the maximum peak current. A limit is reached only once the entire storage capacitor is discharged in the 4ns on-window. Assuming a 2.5nF capacitor, C_{TOT} , the current in the transmitter would be defined as

$$I_{TX} = \frac{C_{TOT}V_{CAP}}{t_{TX}} = \frac{(2.5\text{nF})(3.6\text{V})}{4\text{ns}} = 2.3\text{A}, \quad (5.1)$$

where I_{TX} is the transmitter current, t_{TX} is the transmitter on-time, and V_{CAP} is the voltage drop on the capacitor. The 2.3A from (5.1) is impractical, however. On a more practical level, the limit is closer to 100mA .

Determining the peak current of the receiver, however, is more complicated. The on-time of the receiver is determined by the accuracy of the baseband clocks because the receiver must remain on long enough to ensure reception of the transmitted pulse (Fig. 5.1). If the transmitter and receiver have different baseband clock frequencies, then the clocks will accumulate some phase difference and slowly drift apart each cycle. The receiver, however, must remain on for the entire drift period. If the drift accumulates

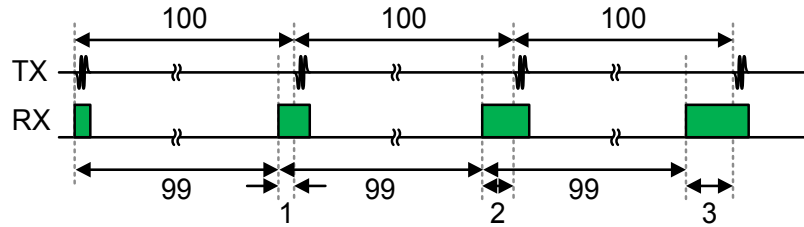


Fig. 5.1. Bit-level turn-on time of the receiver when the receiver clock is 1% faster than the transmitter clock. The transmitted pulses are not being tracked by the receiver.

linearly with time, then the receiver must remain awake longer if it has been asleep longer. The percent of time that the RX must remain on however is constant. As a result, the duty-cycling ratio of the RX is actually constant, equal to the accuracy of the baseband clocks, and independent of data rate. This can be summarized in the following expression:

$$RXDutyCyclingRatio = \frac{RXOnTime}{TimeBetweenPulses} = \frac{Drift / Cycle}{ClockPeriod} = ClockAccuracy. \quad (5.1)$$

5.4.2. Pulse Tracking

For the RX to remain synchronized with the TX, the RX must track the arrival of the transmitted pulses so that phase differences do not accumulate (Fig. 5.2). Alternatively, the receiver can remain awake for longer which will drain the battery faster (Fig. 5.1).

In an ideal system, the RX is turned-on for only a short window around the arrival of a pulse. If the incoming pulse arrives early, then the RX must adjust the turn-on window for the next pulse, so that synchronization is maintained and the duty-cycling ratio remains constant.

To track the arrival of pulses, the on-window of the receiver can be divided into bins with more bins providing greater time granularity (Fig. 5.2). If a pulse arrives early at the RX, then it will be detected in an earlier bin. Likewise, a late pulse will be detected in a later bin.

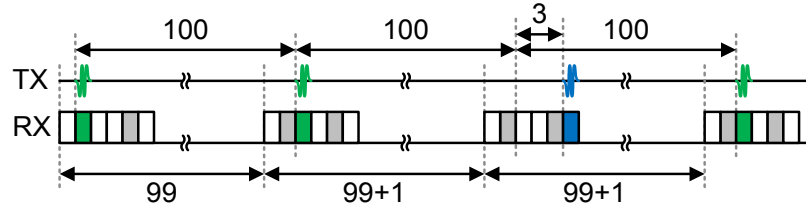


Fig. 5.2. Bit-level turn-on time of the receiver when the receiver clock is 1% faster than the transmitter clock. The transmitted PPM pulses are being tracked by the receiver to maintain synchronization and a constant duty-cycling ratio of 6%.

5.4.3. Baseband Architecture

To detect early, on-time, or late pulses, the receiver must be able to sample the output at a rate higher than the data rate. One of the simplest solutions is to increase the frequency of the baseband clock and implement a counter along with a finite state machine (FSM). The FSM then counts the number of cycles since the last pulse arrived, turns on the receiver when appropriate, and samples the output each clock cycle. By sampling the output multiple times between pulses, the FSM is able to detect early and late pulses in bins the size of the baseband clock period.

Expressed as a percentage, a bin is then the clock frequency divided by the pulse rate. Assuming baseband clocks are accurate to within 1% of each other, each bin only needs to be 1% of the overall pulse rate to ensure that the receiver is able to track early or late pulses. Thus, the baseband clock frequency should be set 100x faster than the pulse rate, and incoming pulses should arrive once every 100 cycles \pm 1 cycle.

5.4.4. Modulation Schemes

Implicit to this synchronization procedure is the continuous arrival of pulses so that the RX can maintain bitwise synchronization. There are at least three communication strategies that ensure a nearly continuous stream of pulses:

1. Use PPM which transmits a pulse every cycle (Fig. 5.3)



Fig. 5.3. Pulse-position modulation divides time into two timeslots for 0-bit and 1-bit. Those timeslots are sub-divided into three bins (early, on-time, and late) for clock tracking by the receiver.

2. Use OOK with a run-length limit of 1 zero
3. Use OOK with bits encoded as a sequence of two pulses (e.g. 0b = 01; 1b = 11)

It turns out that the operation of all three options is actually similar. In the case of option 1, the RX must remain on for 6 bins—early, on-time, and late bins for both a 0-bit and a 1-bit. In the case of option 2, the RX must remain on for 5 bins because a pulse is not transmitted every bit, so two early and two late bins are required. In the case of option 3, the RX must remain on for 5 bins just like option 2.

Of these communication strategies, option 1 was selected because it ensures one pulse per bit while also using less total energy than the other two options. With a run-length limit of 1 zero, option 2 is not practical. In actuality, the receiver would need to be on for more bins per bit in order to handle longer runs of zeros. Option 3, meanwhile, requires 0.83x less energy from the receiver each pulse but 1.66x more energy per bit (since two pulses form a bit). In addition, the transmitter must send 1.5x more pulses on average to encode the same number of bits.

5.4.5. Synchronization Header & Training Sequence

When a receiving node is first enabled, it is not synchronized with a transmitter, so it must search for the transmitter. As with synchronized receivers, the ratio of time an unsynchronized receiver can remain on is constant due to battery limitations. In order to

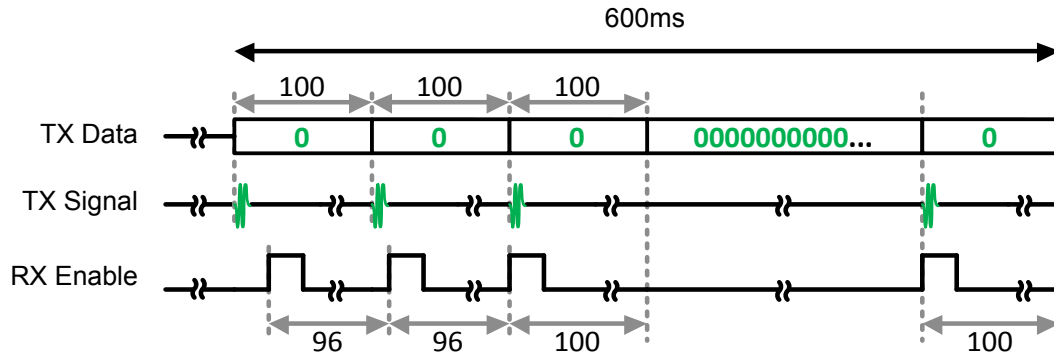


Fig. 5.4. Synchronization header of a new communication protocol for a current-constrained radio.

find the transmitted pulse, however, the receiver must rotate its on-window while being confident that it won't miss the transmitted pulse.

The simplest solution is to generate a training sequence which transmits a consistent stream of either 0-bits or 1-bits at the data rate (all 0-bits in this case). The receiver then can slowly shift the turn-on window with respect to the transmitter's clock until the transmitted pulses are found. With PPM, the RX can shift four bins per bit or 4% of the pulse rate while still accounting for clock mismatch (Fig. 5.4).

The duration of the training sequence must be long enough for two things to occur. First, the duration must allow the RX to slowly step through all possible windows with respect to the TX. With a shift of 4 bins per bit, it will take up to 25 bits to synchronize the RX and TX assuming no frequency misalignment on the baseband clocks. Assuming a worst case misalignment of 1%, the number of bits increases to 34.

Second, the duration must account for the wake-up uncertainty of the low-power timers on the TX and RX. Using the timer from [55], timer uncertainty is 196ms after 1hr. For 3σ of drift worst case, the synchronization header must last for 600ms to ensure communication with more than 99% certainty. A complete packet is shown in Fig. 5.5

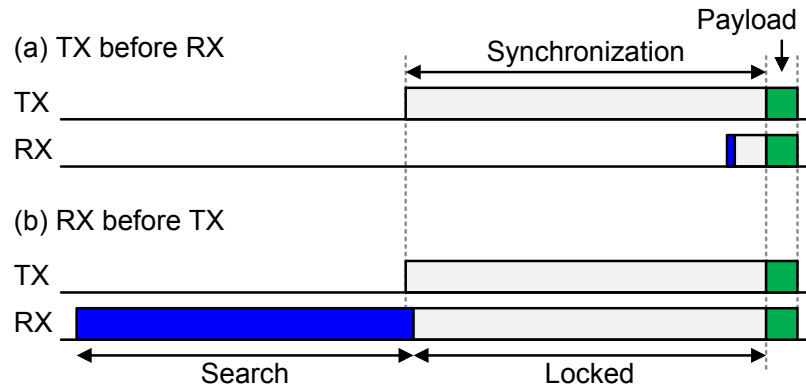


Fig. 5.5. A complete packet with wake-up uncertainty between transmitter and receiver. In scenario (a), the transmitter wakes-up first while in scenario (b), the receiver wakes-up first.

when TX wakes-up before RX or after. In both scenarios, synchronization is achieved before transmission of the payload.

5.4.6. Payload

The payload consists of a fixed number of bits, where the length payload is limited primarily by the amount of memory available in the FSM. For this system, a 512b payload was chosen (Fig. 5.6).

5.4.7. Start-of-Payload Identifier

To identify the end of the training sequence, a short sequence of identifiable bits is required. Since the training sequence consists of 0-bits, a single 1-bit can serve as the start-of-payload identifier. A longer sequence is optional. For this protocol, the start-of-payload identifier is placed at the beginning of the payload for design flexibility.

5.4.8. Data Rate

An optimal data rate which minimizes energy usage can be established based on the requirements for the training sequence and the payload. The training sequence lasts for a fixed length of time, not a fixed number of bits. As a result, a higher data rate simply increases the number of pulses generated by the transmitter. The receiver has a duty-cycle

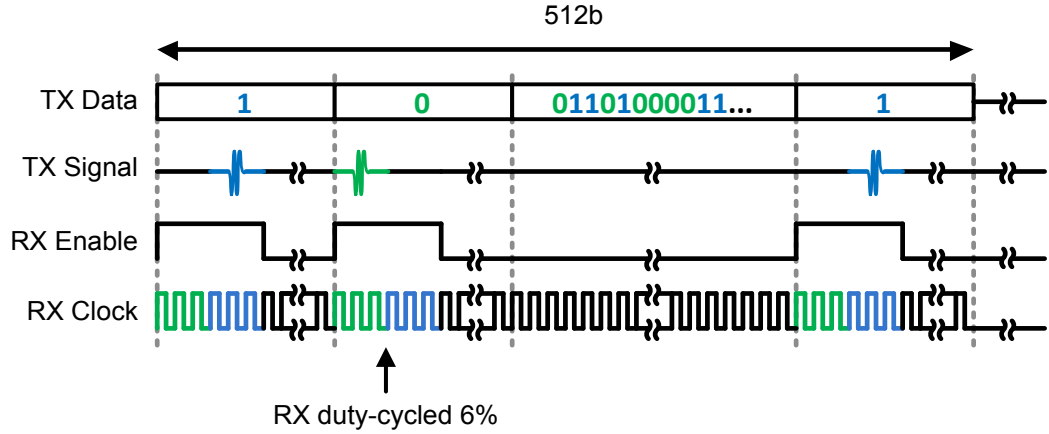


Fig. 5.6. Payload of a new communication protocol for a current-constrained radio. ratio of 6%, independent of data rate. Therefore, for the initial 600ms of synchronization, minimizing data rate minimizes energy usage.

Unlike the synchronization header, the payload has a fixed bit length. Therefore, the TX consumes a fixed amount of energy for a given payload length. The RX, on the other hand, stays on a constant 6% of the time. Therefore, a higher data rate is more energy efficient for the payload.

If synchronization dominates energy usage, then data rate should be minimized. Let's assume for the moment that this is the case. As data rate decreases, the turn-on window of the RX increases, and eventually, the voltage drop on the storage capacitor becomes too large. If the storage capacitor, C_{TOT} , has a capacitance of 2.5nF and the voltage drop, V_{CAP} , is 400mV, then the maximum on-window, t_{RX} , is given by

$$t_{RX} = \frac{C_{TOT}V_{CAP}}{I_{RX}}, \quad (5.2)$$

where I_{RX} is the peak current of the receiver. The peak receiver current then can be calculated based on the duty-cycling ratio as

$$I_{RX} = \frac{I_{BATT}}{\eta} = \frac{10\mu\text{A}}{6\%} = 167\mu\text{A}, \quad (5.3)$$

where I_{BATT} is the battery discharge current, and η is the duty-cycle ratio. The peak current of the receiver is $167\mu\text{A}$ and is independent of data rate. Relating the maximum on-window to the data rate, R , gives

$$t_{RX} = \frac{\eta}{R}. \quad (5.4)$$

By substituting (5.2) and (5.3) into (5.4) and rearranging terms, we find that the minimum data rate, R_{MIN} , is given by

$$R_{MIN} = \frac{I_{BATT}}{C_{TOT}V_{CAP}} = \frac{10\mu\text{A}}{(2.5\text{nF})(0.4\text{V})} = 10\text{kb/s}. \quad (5.3)$$

Therefore, the minimum data rate for the radio is completely independent of clock accuracy and peak receiver current. At a data rate of 10kb/s , 6000b are transmitted during the initial synchronization period which is much greater than the 512b payload. As a result, the initial assumption that synchronization dominates energy usage is valid, and the data rate was set to 10kb/s .

5.4.9. Summary

At this point, we have established a communication protocol for an UWB transceiver that employs PPM and satisfies the constraints of a micro-battery available to a cubic-mm sensor node. Between each pulse, the RX is disabled and then only enabled 6% of the time around each incoming pulse. The duty-cycling ratio is determined by the accuracy of the baseband clocks on the TX and RX. Based on this duty-cycling ratio, the peak current of the receiver is $167\mu\text{A}$, and it can be increased in only two ways. (1) The clock accuracy can be improved, and (2) the maximum discharge current of the battery can be

increased. The transceiver operates at a 10GHz center frequency to maximize performance of the antennas.

The data rate was set to 10kb/s in order to minimize the total energy usage for a packet. A packet consists of a training sequence for synchronization, a start-of-payload identifier, and a payload. The training sequence consists of a continuous stream of 0-bits which last 600ms or 6000 pulses. The start-of-payload identifier is a 1-bit sequence (1b) at the beginning of the 512 bit payload. At a 10kb/s data rate, the transmitter is limited to approximately 100mA over a 4ns period due to practical design limitation.

Chapter 6

10GHz Energy-Detection-Based IR-UWB Receiver

As the trend toward smaller more pervasive computers continues, radios are required to meet these stringent requirements. This chapter presents the design of a 10GHz impulse radio ultra-wideband (IR-UWB) receiver in 0.18 μm BiCMOS. The receiver is optimized for cubic-mm sensor nodes in a wireless sensor network (WSN). It has a high operating frequency to reduce the size of the antenna. It operates at the voltage range of a lithium-ion micro-battery, eliminating the need for a voltage regulator. In addition, the entire receiver, including bias currents, can be duty-cycled between received pulses, so that the average current draw from the battery is less than 10 μA . Thus, the receiver is capable of operating off of a local storage capacitor when active. Finally, the receiver employs energy-detection to down-convert the RF pulses to baseband—eliminating the need for a local oscillator, which saves volume and energy. Ultimately, this receiver meets all of the requirements for a cubic-mm wireless node.

6.1. Introduction & Motivation

Synchronization and integration are significant challenges that must be addressed if the trend toward highly-integrated cubic-mm-scale systems is to continue. As discussed in Chapter 1, the wireless radio often requires the most power of any component in a sensor node—putting significant strain on a micro-battery. Furthermore, the antenna and crystal oscillator can easily make the communication radio the largest component in the

sensor node. As a result, many design decisions must be made regarding the radio to improve integration and save energy. A complete discussion of these design decisions is presented in Chapter 5, though a summary of the conclusions follows.

First, the receiver must operate at a high center frequency, so that the antenna's dimensions can be reduced. Thus, a 10GHz center frequency was selected.

Second, the crystal oscillator must be eliminated to improve integration. Therefore, this receiver employs energy-detection. While this type of receiver is amenable to either on-off keying (OOK) or pulse-position modulation (PPM), this specific receiver was designed for PPM. Without a crystal, an on-chip clock is necessary for bit-level timing. An on-chip baseband clock has limited accuracy, however, which would result in drift between the transmitter (TX) and receiver (RX).

The receiver must operate within the specifications of a mm-scale battery. Lithium-ion batteries have a 3.0-4.2V range in supply voltage, and a custom battery from Cymbet limits current draw to 10 μ A [32]. As a result, the receiver must consume an average power of only 36 μ W at the nominal voltage, and peak currents above this must come from an on-chip storage capacitor.

Because the required average power is so low, the receiver must be duty-cycled and designed with a fast turn-on time and low leakage current. To enable low-power operation, impulse radio ultra-wideband (IR-UWB) is employed, so that the receiver can be duty-cycled between pulses. The pulses naturally provide time information, which can be used to maintain synchronization between the TX and RX.

While many recent receivers are designed to operate at 1V supplies and below [87]-[88], the voltage of a micro-battery is 3.0-4.2V. The efficiency of on-chip mm-scale

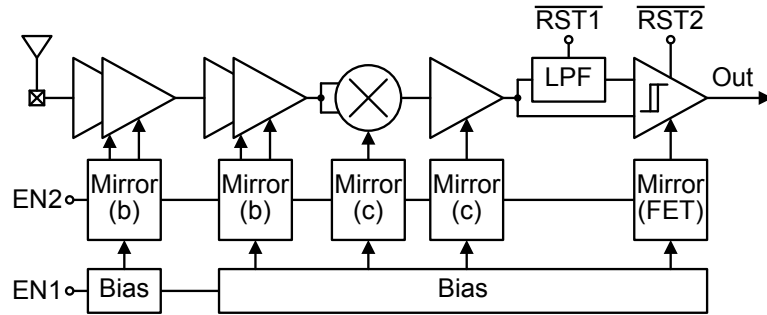


Fig. 6.1. System block diagram of signal path and biasing.

regulators is less than 80% [30],[89]. Higher efficiency, however, is achievable by operating near the battery voltage and only limiting current to protect the battery. Thus, the receiver should be designed in a process with appropriate devices so that it can operate across the entire supply range.

6.2. System Architecture

The proposed receiver amplifies and digitizes UWB pulses using the architecture shown in Fig. 6.1. Four RF gain stages amplify the incoming 10GHz UWB pulses before down-converting them to DC using a squaring mixer. The signal then is passed through a baseband gain stage before the signal path is split. Along one path, the UWB pulses are passed directly to the comparator while a low-pass filter (LPF) provides an auto-zeroed, DC-compensated reference level along the other path. A reset signal enables fast settling of the LPF for fast system turn-on. Finally, a continuous-time latching comparator with controllable hysteresis digitizes the incoming pulses and latches the output until it is reset at the next clock cycle.

6.3. System Operation

The receiver is designed to detect UWB pulses, which arrive periodically, for OOK or PPM. Between pulses, the receiver is duty-cycled to save energy. DC biasing is enabled

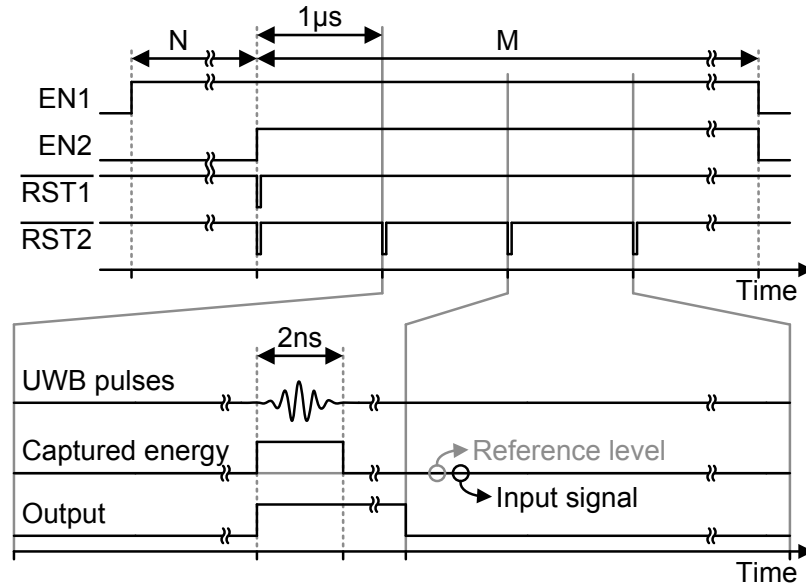


Fig. 6.2. Enable and reset signals required for proper receiver functionality. When pulses arrive, the energy is captured, which toggles the output until it is reset on the next clock edge.

in two steps (Fig. 6.1, Fig. 6.2). During the first step, the two bias networks are enabled by EN1. This bit separately enables the bias networks prior to enabling the rest of the system during a later clock cycle. This is done for stability reasons. If the DC bias networks are not stable, then the mirrored currents also will not be stable along with the gain, and regions of device operation. To ensure stability, the arrival of EN1 is tunable. The second step enables the current mirrors as well as the circuit blocks along the signal path using EN2. These blocks are designed with a turn-on time of less than 10ns. Once biasing is enabled, the LPF is reset by /RST1, which shorts out the RC network and zeroes the reference level to the current input level. Finally, the comparator output is reset by /RST2. The comparator must be reset at the beginning of every sampling window in order to reset the output low in case the output was latched high.

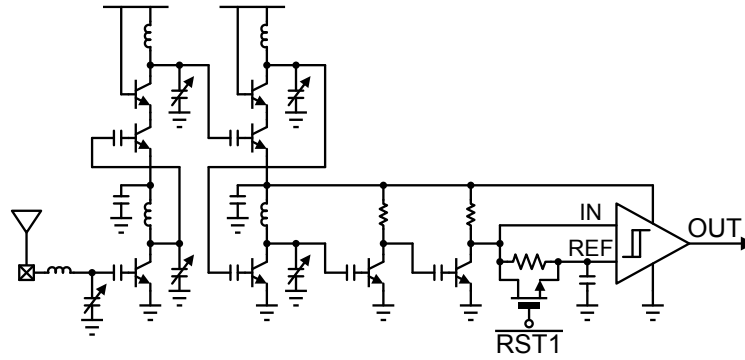


Fig. 6.3. Stacked circuit topologies along signal path.

6.4. Circuit Design

The receiver is designed with circuits that provide RF gain, down-conversion, and pulse detection for OOK or PPM communication. The analog circuits employ current reuse to save power and efficiently operate at the battery voltage. Finally, design decisions were made to ensure fast turn-on and minimize sleep power.

6.4.1. Gain & Down-Conversion

The circuit topologies along the signal path are shown in Fig. 6.3. The received RF signal is sent on-chip then amplified by four common emitter amplifiers with LC loads. The amplifiers use BJTs instead of FETs for higher gain efficiency (g_m/I_C). To improve stage-to-stage isolation and minimize feedthrough, cascoding is employed on the 2nd and 3rd gain stages. To reduce power consumption, all gain stages in the receiver are single-ended. Finally, load capacitance is adjustable via four binary-weighted control bits.

After RF amplification, the signal is self-mixed to DC using a common emitter amplifier with resistive load, while a second amplifier provides additional baseband gain. The two stages are AC-coupled together to simplify biasing, but this results in some lost signal energy. The wideband nature of UWB pulse, however, ensures that most of the energy is recovered.

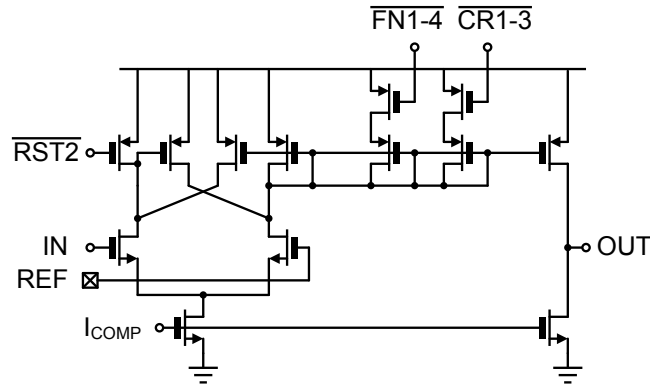


Fig. 6.4. Circuit topology of the latching comparator with tunable hysteresis.

6.4.2. Pulse Detection

The baseband signal then is passed to the input of a continuous-time hysteretic comparator for pulse detection. Low-pass filtering of the main signal path zeros the reference level to the same DC voltage as the input level (Fig. 6.3), and a switch across the resistor enables fast zeroing during turn-on.

The two-stage hysteretic comparator is shown in Fig. 6.4. The load on the first stage consists of cross-coupled devices which provide positive feedback and diode-connected FETs which provide controllable hysteresis levels from four fine control bits and three coarse bits. The comparator output latches high when a pulse is detected and remains high until the next clock cycle, which resets the output using $\overline{RST2}$. Finally, the comparator output passes through a level-shifter to ensure rail-to-rail swings on the fixed 1.2V supply used by the baseband processor.

6.4.3. Current Reuse & Biasing

The entire signal path of the receiver consists of two parallel current paths operating at the battery voltage (Fig. 6.3). Each current path consists of two stacked gain stages in order to reuse current and to better utilize the available headroom. Large capacitors are placed between the stacked stages to create an AC ground at 10GHz. While this stacked

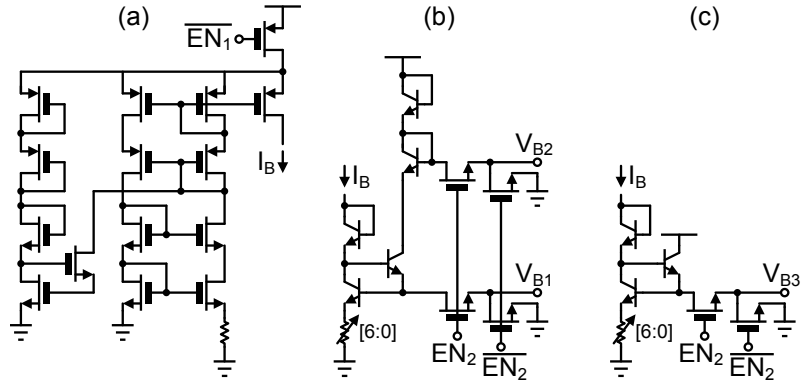


Fig. 6.5. (a) Constant- G_m bias circuit with (b)-(c) BJT mirrors.

configuration does improve efficiency, it also couples the current usage of the stacked gain stages with those referenced to ground.

Stacked gain stages also increase the complexity of the bias circuits, as shown in Fig. 6.5. Biasing is provided by two constant- G_m biases (Fig. 6.5a), two stacked BJT current mirrors (Fig. 6.5b), and two non-stacked BJT current mirrors (Fig. 6.5c). The constant- G_m bias circuits are designed to provide constant gain across temperature, and to reduce supply sensitivity, the circuits are cascoded.

The bias currents then get mirrored onto the BJT circuits in Fig. 6.5b-c. The mirrored current ratio is tuned via seven control switches which shunt across a stack of series resistors connected to the emitter of a BJT. Base current compensation is employed for better current matching, and diode-connected BJTs ensure sufficient headroom is left for the cascoded devices where necessary.

6.4.4. Digital Logic & Control

For four major reasons, the digital blocks in the receiver operate from a fixed 1.2V supply instead of the battery voltage. (1) 3.3V FETs are larger, which increases the area requirements for the digital logic. (2) Standard cells are only available for regular- V_T FETs. (3) Dynamic power consumption dominates in digital circuits. (4) Since digital

circuits consume less than $10\mu\text{W}$ on average, on-chip voltage regulation is possible with reasonable efficiency. As a result, area and energy usage can be reduced by operating digital circuits from a separate lower supply voltage.

Because the digital control circuitry for the analog blocks operates from a different supply voltage, all digital bits must be level-shifted between the two supply regimes. Level-shifting is accomplished using a conventional level converter topology with digital pseudo-differential inputs and a cross-coupled output load. To minimize leakage current, thick-oxide devices are used along the enable and reset signal paths because they must remain on continuously during a communication packet.

6.4.5. Sleep-Power Minimization & Receiver Turn-On

When the receiver is asleep, all DC-biases are grounded, which cuts off the current paths. By grounding V_{B1} and V_{B2} in particular (Fig. 6.5), we can isolate the large capacitors used as AC-ground nodes in the stacks. Current isolation prevents the capacitors from discharging, which saves energy and ensures a fast turn-on time between bits.

In addition, the receiver achieves low sleep-mode power consumption with the use of BJTs and thick-oxide FETs along all current paths. Between communication packets, the receiver goes into a deeper sleep by using a separate sleep signal which completely shuts down the system. In this mode, FET headers or footers disable all digital blocks.

6.5. Simulation Results

The UWB receiver was designed to function across both temperature and supply voltage variation. The constant- G_m bias circuits are designed to vary less than 2nA or 1% across the entire $3.0\text{-}4.2\text{V}$ supply voltage range (Fig. 6.6). The bias current variation is

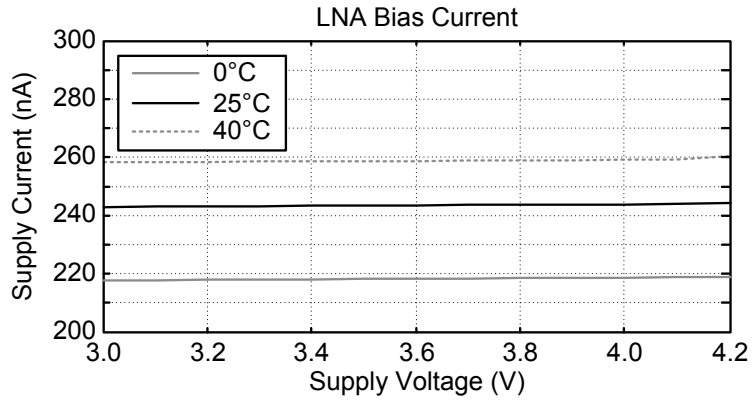


Fig. 6.6. Bias current of the LNA over supply voltage and temperature.

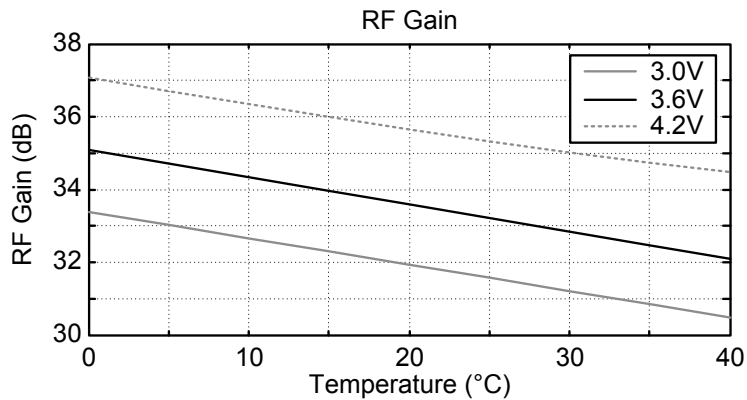


Fig. 6.7. RF gain over temperature for several different supply voltages.

minimized thanks to cascoding in the constant- G_m bias cell. As temperature increases, however, the constant- G_m bias current increases in order to maintain a nearly constant- G_m for better gain stability.

RF gain varies by approximately 3dB over a 40°C temperature variation for a given supply voltage (Fig. 6.7). Meanwhile, center frequency shifts by less than 100MHz over the same temperature range (Fig. 6.8). Gain and center frequency stability ensures continued communication over temperature. At the same time since current is varying, the system should be tuned for the expected operating conditions. For example, if the

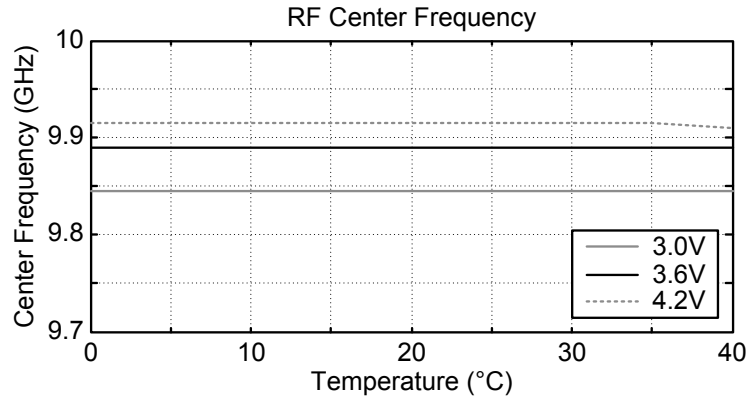


Fig. 6.8. Center frequency of RF gain stages for several different supply voltages.

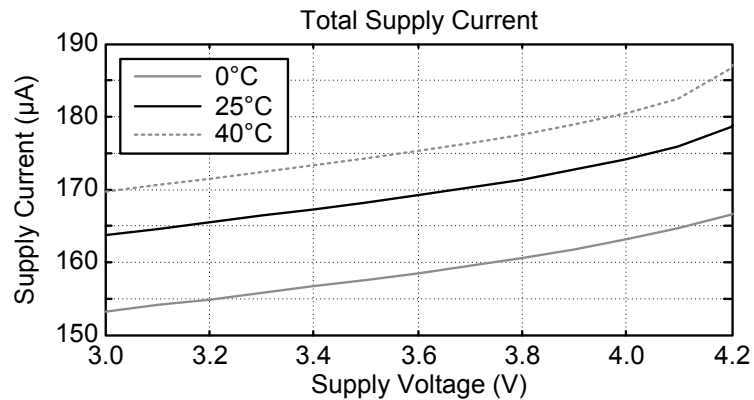


Fig. 6.9. Total current through the receiver over supply voltage and temperature.

system will be operating at higher temperatures, the current should be reduced to satisfy the constraints of the cubic-mm battery.

RF gain varies by less than 4dB due to changes in supply voltage while operating at a constant temperature (Fig. 6.7). This gain variation results from changes in supply current (Fig. 6.9). Though bias current is nearly constant across supply voltage variation, supply current increases with increasing supply voltage due to the finite Early voltage of the stacked NPN transistors that constitute most of this receiver.

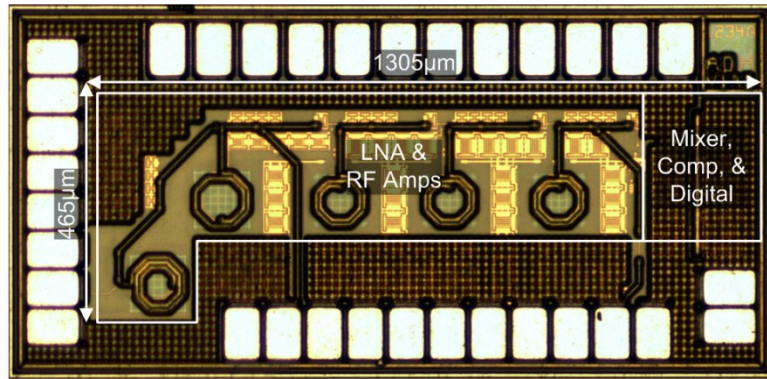


Fig. 6.10. Die photo of the UWB receiver.

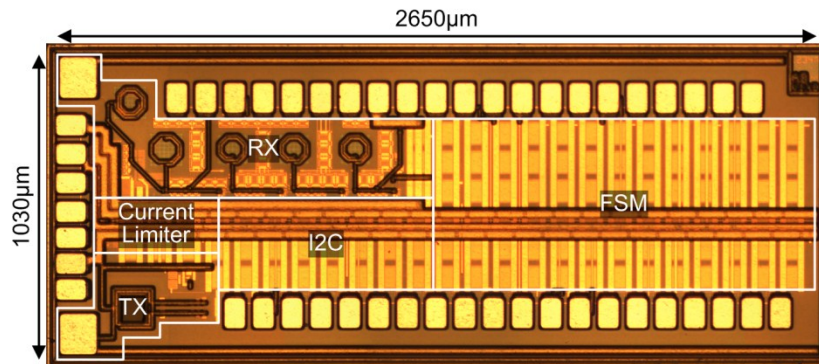


Fig. 6.11. Die photo of the complete UWB transceiver.

6.6. Measurement Results

This UWB receiver was fabricated in a $0.18\mu\text{m}$ BiCMOS process with inductors and MIM capacitors. The main signal path operates at a supply voltage of 3.3V , so that it can be directly powered by a lithium-ion battery without the need for voltage regulation. Digital processing and scan blocks operate at 1.2V to reduce dynamic power consumption. The current draw from the 1.2V supply is 92nA .

A die photo of the receiver is shown in Fig. 6.10, while the die photo of the combined transceiver is shown in Fig. 6.11. The receiver occupies 0.61mm^2 , which is dominated by five inductors. The transceiver, on the other hand, occupies 2.7mm^2 with most of the area consumed by the digital baseband—in particular, the finite state machine (FSM), scan chain, and I2C controller.

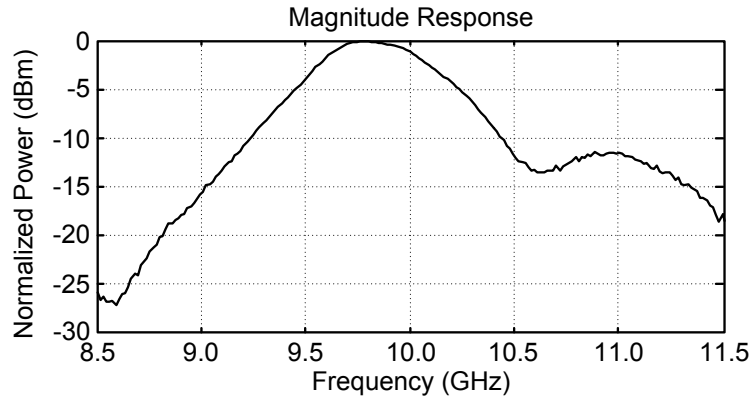


Fig. 6.12. Magnitude response of the receiver.

The magnitude response of the receiver is shown in Fig. 6.12. The center frequency is set to 9.8GHz to maximize performance; however, it can be tuned anywhere from 9.0GHz to 10.0GHz to ensure the center frequency of the receiver can be aligned with the transmitter. Conversion gain is impossible to measure with the available test structures, so the magnitude response has been normalized. The receiver has a bandwidth of greater than 500MHz which ensures that the entire signal power is received and amplified.

To measure sensitivity, an external FPGA from Opal Kelly was programmed with a modified finite state machine which mimics the operation of the FSM in the complete transceiver. Pulse-position modulation was implemented on the external FSM. A continuous stream of 1-bits were generated in an AWG, then up-converted to 9.8GHz and sent into the receiver. The output was sampled into six bins of 1 μ s each, where a 0-bit should occur in bins 0-2 and a 1-bit in bins 3-5. If the output went high in bins 0-2, then an error was recorded. Likewise, if the output remained low in bins 3-5, then an error was recorded. Based on this setup, the receiver has a measured sensitivity of -66dBm with a BER of 10^{-3} while consuming 548 μ W in active power. If duty-cycled, the average current draw would reduce to only 10 μ A which satisfies the constraints of a cubic-mm-scale Li-

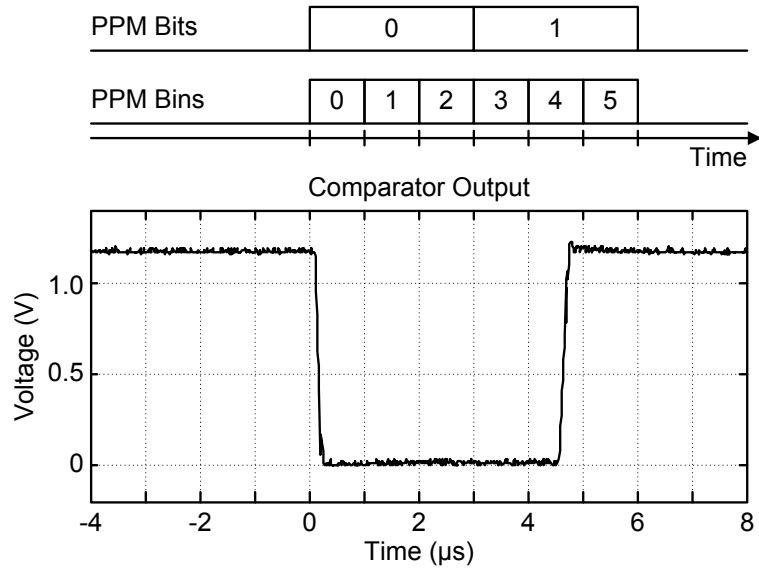


Fig. 6.13. Output of the receiver after reset at the start of bin 0. An UWB pulse is transmitted during bin 4.

ion battery. If the constraints from the battery change for other applications, then current in each stage can be increased to improve sensitivity if desired.

The output of the receiver is plotted in Fig. 6.13. In this case, an UWB pulse was transmitted during bin 4, or $4.5\mu\text{s}$ after the first reset signal is sent to the comparator. A delay of approximately 100ns exists between the reset signal and the output actually being reset low. Some of this delay is from the receiver; however, much of the delay is the result of the 8MHz bandwidth of the off-chip output buffer used in the test setup.

The data rate is 10kb/s, and the measured sleep power is 168pW, which compares favorably to other recently published UWB receivers [87]-[88]. Table 6.1 summarizes the performance of this receiver and compares it to other recently published state-of-the-art receivers.

Table 6.2 presents the link budget for the receiver under four different operating scenarios. In the first scenario, the gain from the on-chip antenna shown in Fig. 6.11 is used to calculate the maximum communication distance for the radio.

Table 6.1. Measured receiver performance and comparison.

	This Receiver	[87]	[88]
Process	0.18 μ m BiCMOS	90nm CMOS	90nm CMOS
Signaling	IR-UWB	IR-UWB	IR-UWB
Modulation	OOK / PPM	OOK / PPM	OOK / S-OOK
Center Frequency	9.0-10.0GHz	3-5GHz	3.6-4.3GHz
V _{DD}	3.3V	1.0V	0.9-1.0V
Area	0.61mm ²	5.46mm ²	1mm ²
Sensitivity (10 ⁻³ BER)	-66dBm	-76dBm	-66dBm
Active Power	548 μ W	22.7mW	3.9mW
Sleep Power	168pW	920 μ W	1.03mW
Data Rate	10kb/s	16Mb/s	1Mb/s

Unfortunately, that distance is less than 1cm, and near-field coupling applies. Communication distance remains less than 1cm even if 4mm-long wire antenna is bonded to the RX and TX pads in Fig. 6.11, and the expected communication distance is 4cm for an isotropic antenna based on the measured performance of the receiver.

For comparison, simulated receiver performance is shown in the same table with a 4mm-long wire antenna. Based on simulation results, the expected communication distance improves to approximately 0.8m. This improvement in communication distance is the result of the relatively poor measured sensitivity of the receiver.

Table 6.2. Link budget for several different antennas.

	Budget 1	Budget 2A	Budget 2B (Simulated)	Budget 3
Antenna Type	On-Chip	Wire / Hair	Wire / Hair	Isotropic
Antenna Gain	-34dBi	-10dBi	-10dBi	0dBi
TX Peak Radiated Power	5dBm	5dBm	5dBm	5dBm
Pulse Length	2ns	2ns	2ns	2ns
TX Avg Radiated Power	-42dBm	-42dBm	-42dBm	-42dBm
RX Sensitivity	-66dBm	-66dBm	-112dBm ^a	-66dBm
Link Margin	0dB	0dB	0dB	0dB
Center Frequency	9.8GHz	9.8GHz	9.8GHz	9.8GHz
Maximum Distance	<1cm	<1cm	0.8m	4cm

^aAverage sensitivity for the simulated receiver with -65dBm peak sensitivity.

Chapter 7

Conclusion

As current computing trends continue, wireless sensor networks are widely perceived as the next major step in the decades-long trend toward smaller more pervasive devices. Volume constraints on these new systems for many applications results in significant energy constraints that must be resolved in order to improve node lifetimes. Unfortunately, energy sources, such as the battery and solar cell, have been slow to improve. As a result, energy must be conserved in the sensor node by reducing the power consumption of the circuit components. While significant progress has been made in processors, timers, and memories, wireless synchronization and communication remain the highest energy tasks in a wireless sensor node. Therefore, this thesis has investigated a new method of synchronizing a sensor network using existing ambient wireless signals and proposed a new communication protocol which enables duty-cycled operation of a communication radio in order to conserve energy.

Many of today's ambient wireless signals are pervasive, making them a good potential source for synchronizing a wireless sensor network. The advantage of this approach is that the synchronization signal is generated outside the network, saving energy. A survey was conducted on many common wireless standards to determine their viability as a clock source. Because we would like to extract the source using a low-power receiver, a good clock source is high-power, pervasive, periodic, and easy to demodulate. If all of

these conditions are met, then a low-power clock-harvesting receiver (CRX) should be realizable.

To demonstrate the viability of this clock-harvesting technique, two separate clock-harvesting receivers were designed, fabricated, and tested. The first clock-harvesting receiver was designed to extract a 21Hz clock embedded within the GSM standard. By harvesting the clock from a pre-existing and pervasive source, the WSN does not have to generate it within the network. The receiver was fabricated in an IBM 0.13 μ m process. It operates in the 1900MHz band and extracts a clock the GSM broadcast signal which exists on every cell worldwide. The receiver has a sensitivity of -87dBm with a 10^{-3} clock error rate (CER) while consuming only 126 μ W. It has a sleep power consumption of 81pW so that it can be duty-cycled as part of a tiered synchronization strategy to further reduce synchronization energy. This receiver is the first clock-harvesting receiver ever reported and therefore the first based on a GSM standard. Finally, the functionality of two clock-harvesting receivers was verified by extracting a clock from the broadcast channel of a local cell tower.

The second clock-harvesting receiver was designed to extract a 1.2kHz clock from the 3G CDMA standard. Unlike the first CRX, this receiver harvests its clock from the on-off keyed idle slots of the CDMA standard using energy-detection. Therefore, this receiver does not require an external local oscillator (LO), improving integration for future small-scale sensor nodes. The receiver was fabricated in an IBM 0.13 μ m process and extracts a 3G CDMA signal from the 1900MHz band. The receiver consumes 298 μ W while in active mode and has a sensitivity of -73dBm with a 10^{-3} CER. Like the GSM-based CRX, this receiver is designed for tiered synchronization, consuming only 44pW while asleep.

The relevant design constraints for a communication radio in a cubic-mm sensor node were analyzed, and a new communication protocol has been proposed. Due to volume constraints, a crystal oscillator is not an option and the antenna must be small, pushing the operating frequency higher. The micro-battery imposes a $10\mu\text{A}$ current limit on the system. As a result, the radio must be duty-cycled so that it can draw higher peak currents while giving a storage capacitor time to recharge. Due to the duty-cycled nature of the radio, IR-UWB was selected. The communication protocol relies on pulse-position modulation, so that the receiver has a constant stream of pulses to track the frequency misalignment between the radios due to the limitations of low-power, on-chip clocks. During the synchronization header, the communication protocol has a training sequence, enabling duty-cycled operation by both the transmitter and receiver. Based on system constraints, a 10kb/s data rate was found to minimize energy usage in the system.

An IR-UWB receiver was demonstrated that is designed for this new communication protocol. As a result, the receiver is optimized for operation in an energy-constrained cubic-mm sensor node. The receiver was fabricated in a $0.18\mu\text{m}$ BiCMOS process and operates at a 10GHz center frequency to improve the performance of a small antenna. It operates at the voltage range of a lithium-ion micro-battery and can be duty-cycled between bits, so that the average current draw from the battery is less than $10\mu\text{A}$. It employs energy-detection and has a measured sensitivity of -66dBm while consuming only $548\mu\text{W}$ when awake and 168pW while asleep.

References

- [1] G. Bell, "Bell's Law for the Birth and Death of Computer Classes," *Commun. ACM*, vol. 51, no. 1, pp 86-94, Jan. 2008.
- [2] T. Nakagawa *et al.*, "1-cc Computer: Cross-Layer Integration with UWB-IR Communication and Locationing," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 964-973, Apr. 2008.
- [3] I.F. Akyildiz *et al.*, "A Survey of Sensor Networks," *IEEE Commun. Mag.*, pp. 102-114, Aug. 2002.
- [4] K. Romer and F. Mattern, "The Design Space of Wireless Sensor Networks," *IEEE Wireless Commun.*, vol. 11, no. 6, pp. 54-61, Dec. 2004.
- [5] D. Puccinelli and M. Haenggi, "Wireless Sensor Networks: Applications and Challenges of Ubiquitous Sensing," *IEEE Circuits Syst. Mag.*, vol. 5, no. 3, pp. 19-31, 2005.
- [6] J. Yick, B. Mukherjee, and D. Ghosal, "Wireless Sensor Networks Survey," *J. Comput. Networks*, vol. 52, no. 12, pp. 2292-2330, Apr. 2008.
- [7] P. Corke *et al.*, "Environmental Wireless Sensor Networks," in *Proc. IEEE*, vol. 98, no. 11, pp. 1903-1917, Nov. 2010.
- [8] B.H. Calhoun *et al.*, "Body Sensor Networks: A Holistic Approach from Silicon to Users," in *Proc. IEEE*, vol. 100, no. 1, pp. 91-106, Jan. 2012.
- [9] M. Meribout, "A Wireless Sensor Network-Based Infrastructure for Real-Time and Online Pipeline Inspection," *IEEE Sensors J.*, vol. 11, no. 11, pp. 2966-2972, Nov. 2011.
- [10] B. Carkhuff and R. Cain, "Corrosion Sensors for Concrete Bridges," *IEEE Instr. Meas. Mag.*, vol. 6, no. 2, Jun. 2003.
- [11] R.A. Swartz and J.P. Lynch, "Strategic Network Utilization in a Wireless Structural Control System for Seismically Excited Structures," *J. of Structural Engineering*, pp. 597-608, May 2009.
- [12] M. Flatscher *et al.*, "A Bulk Acoustic Wave (BAW) Based Transceiver for an In-Tire-Pressure Monitoring Sensor Node," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 167-177, Jan. 2010.

- [13] G. Chen *et al.*, "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *ISSCC Dig. Tech. Papers*, pp. 310-311, Feb. 2011.
- [14] T.H. Teo *et al.*, "A 700- μ W Wireless Sensor Node SoC for Continuous Real-Time Health Monitoring," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2292-2299, Nov. 2010.
- [15] Y. Liao, H. Yao, B. Parviz, and B. Otis, "3 μ W wirelessly powered CMOS glucose sensor for an active contact lens," *ISSCC Dig. Tech. Papers*, pp. 38-39, Feb. 2011.
- [16] G. Chen *et al.*, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," *ISSCC Dig. Tech. Papers*, pp. 288-289, Feb. 2010.
- [17] B.A. Warneke *et al.*, "An Autonomous 16 mm³ Solar-Powered Node for Distributed Wireless Sensor Networks," *Proc. IEEE Sensors*, vol. 2, pp. 1510-1515, 2012.
- [18] Y. Lee *et al.*, "A Modular 1mm³ Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting," *ISSCC Dig. Tech. Papers*, Manuscript, Feb. 2012.
- [19] S. Hanson, M. Seok, Y.-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, "A low-voltage processor for sensing applications with picowatt standby mode," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, Apr. 2009, pp. 1145-1155.
- [20] "Temperature Compensated Crystal Oscillators (TCXO) Surface Mount Type TCXO (LSI Type)," Kyocera Corp., Product Spec., KT2016 Series, 2012.
- [21] "Crystal Oscillator 32.768kHz," Epson Toyocom, Product Spec., SG-3030LC, 2012.
- [22] S. Drago *et al.*, "A 200 μ A Duty-Cycled PLL for Wireless Sensor Nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, Jul. 2010, pp. 1305-1315.
- [23] H.-J. Lee, A.M. Kerns, S. Hyvonen, and I.A. Young, "A Scalable Sub-1.2mW 300MHz-to-1.5GHz Host-Clock PLL for System-on-Chip in 32nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 96-97, Feb. 2011.
- [24] Y. Park and D.D. Wentzloff, "An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS," *IEEE Custom Integ. Circuits Conf.*, Oct. 2011.
- [25] Y.H. Chee, A.M. Niknejad, and J. Rabaey, "A Sub-100 μ W 1.9-GHz CMOS Oscillator Using FBAR Resonator," *IEEE Symp. Radio Freq. Integ. Circuits*, pp. 123-126, Jun. 2005.

- [26] J. Shi and B.P. Otis, "A Sub-100 μ W 2GHz Differential Colpitts CMOS/FBAR VCO," *IEEE Custom Integ. Circuits Conf.*, Oct. 2011.
- [27] A. Nelson *et al.*, "A 22 μ W, 2.0GHz FBAR Oscillator," *IEEE Symp. Radio Freq. Integ. Circuits*, Jun. 2011.
- [28] B.W. Cook, A.D. Berny, A. Molnar, S. Lanzisera, and K.S.J Pister, "An ultra-low power 2.4GHz RF transceiver for wireless sensor networks in 0.13 μ m CMOS with 400mV supply and an integrated passive RX front-end," *ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 1460-1469.
- [29] M.S. McCorquodale *et al.*, "A 0.5-to-480 MHz self-referenced CMOS clock generator with 90 ppm total frequency error and spread-spectrum capability," *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 524–525.
- [30] G. Chen, S. Hanson, D. Blaauw, and D. Sylvester, "Circuit Design Advances for Wireless Sensing Applications," in *Proc. IEEE*, vol. 98, no. 11, pp. 1808-1827, Nov. 2010.
- [31] M.A. Green *et al.*, "Solar Cell Efficiency Tables (Version 39)," *Prog. Photovolt.: Res. Appl.*, vol. 20, no. 1, pp. 12-20, Jan. 2012.
- [32] Cymbet Corp., *EnerChip Smart Solid State Batteries*, (2012, Feb. 6) [Online]. Available: <http://www.cymbet.com/products/enerchip-solid-state-batteries.php>.
- [33] Samsung SDI, *Prismatic Rechargeable Battery*, (2012, Feb. 6) [Online]. Available: <http://samsungsdi.com/battery/prismatic-rechargeable-battery.jsp>.
- [34] Y. Nishi, "Lithium Ion Secondary Batteries; Past 10 Years and the Future," *J. Power Sources*, vol. 100, no. 1-2, pp. 101-106, Nov. 2001.
- [35] A.H. Zimmermann and M.V. Quinzio, "Performance of SONY 18650-HC Lithium-Ion Cells for Various Cycling Rates," Aerospace Corp., El Segundo, CA, Tech. Rep. TR-2010(8550)-5, Jan. 2010.
- [36] S. Hossain *et al.*, "Lithium-Ion Cells for Aerospace Applications," in *Proc. 32nd Intersociety Energy Conversion Eng. Conf.*, vol. 1, pp. 35-38, Aug. 1997.
- [37] "CGR18650: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650, Apr. 1998.
- [38] "CGR18650H: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650H, Apr. 1999.
- [39] "CGR18650HM: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650HM, Jan. 2000.

- [40] "CGR18650HG: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650HG, Jan. 2000.
- [41] "CGR18650A: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650A, Apr. 2002.
- [42] "CGR18650C: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650C, Mar. 2004.
- [43] "CGR18650D: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650D, Nov. 2004.
- [44] "CGR18650DA: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650DA, Apr. 2006.
- [45] "CGR18650E: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650E, Jan. 2007.
- [46] "CGR18650CG: Cylindrical Model," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650CG, Dec. 2008.
- [47] "NCR18650 Lithium Ion," Panasonic Corp., Rolling Meadows, IL, Product Spec., NCR18650/6.11V1, 2011.
- [48] "NCR18650A 3.1Ah Lithium Ion," Panasonic Corp., Rolling Meadows, IL, Product Spec., CGR18650CH/3.11V1, 2011.
- [49] "Panasonic Batteries Energy Catalog," Panasonic Corp., Rolling Meadows, IL, Product Spec., PIC-PanBat-FY11-PanaEnergyCatalog, 2011.
- [50] K. Choe *et al.*, "A Precision Relaxation Oscillator with a Self-Clocked Offset-Cancellation Scheme for Implantable Biomedical SoCs," *ISSCC Dig. Tech. Papers*, pp. 402-403, Feb. 2009.
- [51] F. Sebastiano *et al.*, "A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks," *IEEE J. Solid-State Circuits*, vol. 46, no.7, pp. 1544-1552, Jul. 2011.
- [52] V. D. Smedt *et al.*, "A 66 μ W 86 ppm/ $^{\circ}$ C Fully-Integrated 6 MHz Wienbridge Oscillator with a 172 dB Phase Noise FOM," *IEEE J. Solid-State Circuits*, vol. 44, no.7, pp. 1990-2001, Jul. 2009.
- [53] J. Lee *et al.*, "10 MHz 80 μ W 67 ppm/ $^{\circ}$ C CMOS Reference Clock Oscillator with a Temperature Compensated Feedback Loop in 0.18 μ m CMOS," *IEEE Symp. VLSI Circuits*, pp. 226-227, Jun. 2009.

- [54] Y-S. Lin, D. Sylvester, and D. Blaauw, "A 150pW Program-and-Hold Timer for Ultra-Low Power Sensor Platforms," *ISSCC Dig. Tech. Papers*, pp. 326-327, Feb. 2009.
- [55] Y. Lee *et al.*, "A 660pW Multi-Stage Temperature-Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization," *ISSCC Dig. Tech. Papers*, pp. 46-47, Feb. 2011.
- [56] Y-S. Lin, D. Sylvester, and D. Blaauw, "A sub-pW timer using gate leakage for ultra low-power sub-Hz monitoring systems," *IEEE Custom Integ. Circuits Conf.*, Oct. 2007.
- [57] B.H. Calhoun *et al.*, "System Design Principles Combining Sub-Threshold Circuits and Architectures with Energy Scavenging Mechanisms," *IEEE Int. Symp. Circuits Syst.*, pp. 269-272, Jun. 2010.
- [58] B. Otis, Y.H. Chee, and J. Rabaey, "A 400 μ W-RX, 1.6mW-TX Super-Regenerative Transceiver for Wireless Sensor Networks," *ISSCC Dig. Tech. Papers*, pp. 396-606, Feb. 2005.
- [59] J. Ayers, N. Panitantom, K. Mayaram, and T.S. Fiez, "A 2.4GHz Wireless Transceiver with 0.95nJ/b Link Energy for Multi-Hop Battery-Free Wireless Sensor Networks," *IEEE Symp. VLSI Circuits*, pp. 29-30, Jun. 2010.
- [60] D. Yoon, D. Blaauw, and D. Sylvester, "A 5.58nW 32.768kHz DLL-Assisted XO for Real-Time Clocks in Wireless Sensing Applications," *ISSCC Dig. Tech. Papers*, Manuscript, Feb. 2012.
- [61] E.-Y.A. Lin, J.M. Rabaey, and A. Wolisz, "Power-efficient rendez-vous schemes for dense wireless sensor networks," *Proc. IEEE Int. Conf. Commun.*, vol. 7, Jun. 2004, pp. 3769-3776.
- [62] N.M. Pletcher, S. Gambini, and J.M. Rabaey, "A 2GHz 52 μ W Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture," *ISSCC Dig. Tech. Papers*, pp. 524-525, 633, Feb. 2008.
- [63] X. Huang *et al.*, "A 2.4GHz/915MHz 51 μ W Wake-Up Receiver with Offset and Noise Suppression," *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb. 2010.
- [64] S. Drago *et al.*, "A 2.4GHz 830pJ/bit Duty-Cycled Wake-Up Receiver with -82dBm Sensitivity for Crystal-Less Wireless Sensor Nodes," *ISSCC Dig. Tech. Papers*, pp. 224-225, Feb. 2010.
- [65] M.A. Lombardi, "NIST Time and Frequency Services," US National Institute of Standards and Technology, Boulder, CO Special Pub., 432, Apr. 2003.
- [66] M.A. Lombardi, "How Accurate is a Radio Controlled Clock," *Horological J.*, Mar. 2010, pp.108-111.

- [67] M.A. Lombardi, *et al.*, “WWVB Radio Controlled Clocks: Recommended Practices for Manufacturers Consumers,” US National Institute of Standards and Technology, Boulder, CO Special Pub., 960-14, Aug. 2009.
- [68] “CME6005 Receiver IC,” C-MAX Time Solutions GmbH, Heilbronn, Germany, Product Spec., CME6005, Rev. A8, Mar. 2007.
- [69] “CMA-MF-15NP Multi-frequency Antenna,” C-MAX Ltd., Kowloon Bay, Kowloon HK, Product Spec., CMA-MF-15NP, Rev. A.3.1, May 2007.
- [70] “CMA-60-100 Clock Antenna,” C-MAX Time Solutions GmbH, Heilbronn, Germany, Product Spec., CMA-60-100, Rev. A4, May 2007.
- [71] European Telecommunications Standards Institute, *Global System for Mobile Communications*, Tech. Spec., 145 Series, v. 8.0.0.0, Release 8, Feb. 2009.
- [72] “Physical Layer for cdma2000 High Rate Packet Data Air Interface Specification,” *3rd Generation Partnership Project 2 (3GPP2)*, Tech. Spec., C.S0024-200-C, Ver. 2, Jul. 2011.
- [73] Bluetooth Special Interest Group, “Specification of the Bluetooth System,” Std, ver. 4.0, Jun. 2010.
- [74] IEEE Standards Association, “IEEE Standard for Local and Metropolitan Area Networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs),” Std., 802.15.4-2011, Sep. 2011.
- [75] GSM Association, *GSM World Coverage 2009*, (2009, Sept. 10), *GSM World (2009-A ed.)*, [Online]. Available: http://www.coveragemaps.com/gsmposter_world.htm.
- [76] Verizon Wireless, *Coverage Locator*, (2011, Nov. 30), [Online]. Available: <http://www.verizonwireless.com/b2c/CoverageLocatorController>.
- [77] “RSSI Sub – AT&T – 2G Phone,” C Squared Systems, Manchester, NH, Measurement Data, University of Michigan – EECS – Floor 1-4, Nov. 2008.
- [78] J.K. Brown and D.D. Wentzloff, "Harvesting a Clock from a GSM Signal for the Wake-Up of a Wireless Sensor Network," *IEEE Intl. Symp. Circuits Syst.*, pp. 1500-1503, Jun. 2010.
- [79] C.-H. Wu, C.-S. Liu, and S.-L. Liu, “A 2GHz CMOS Variable-Gain Amplifier with 50dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet,” *ISSCC Dig. Tech. Papers*, pp. 484-485, 541, Feb. 2004.
- [80] J. Ayers, K. Mayaram, and T.S. Fiez, “An Ultralow-Power Receiver for Wireless Sensor Networks,” *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1759-1769, Aug. 2010.

- [81] N. Pletcher, S. Gambini, and J. Rabaey, "A 65 μ W 1.9GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Nodes," *IEEE Custom Integ. Circuits Conf.*, pp. 539-542, 2007.
- [82] J. Ayers, K. Mayaram, and T.S. Fiez, "A 0.4 nJ/b 900MHz CMOS BFSK Super-Regenerative Receiver," *IEEE Custom Integ. Circuits Conf.*, pp. 591-594, 2008.
- [83] Y. Han *et al.*, "An Ultra Low Power BPSK Receiver and Demodulator Based on Injection-Locked Oscillators," *IEEE Trans. Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1339-1349, 2011.
- [84] M. Lont *et al.*, "Ultra-Low Power FSK Wake-up Receiver Front-End for Body Area Networks," *IEEE Symp. Radio Freq. Integ. Circuits*, Jun. 2011.
- [85] J.K. Brown and D.D. Wentzloff, "A 1900MHz-Band GSM-Based Clock-Harvesting Receiver with -87dB Sensitivity," *IEEE Symp. Radio Freq. Integ. Circuits*, Jun. 2011.
- [86] IBM Microelectronics Division, "BiCMOS7WL Design Manual," Essex Junction, VT, Prod. Spec., V1.8.0.0, ES#70P3341, EC#L86943, Jan. 2011.
- [87] D.C. Daly *et al.*, "A Pulsed UWB Receiver SoC for Insect Motion Control," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 153-166, Jan. 2010.
- [88] M. Crepaldi *et al.*, "An Ultra-Wideband Impulse-Radio Transceiver Chipset Using Synchronized-OOK Modulation", *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2284-2299, Oct. 2011.
- [89] Y.K. Ramadass *et al.*, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter with Digital Capacitance Modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, Dec. 2010.
- [90] IBM Microelectronics Division, "BiCMOS8HP Design Manual," Essex Junction, VT, Prod. Spec., V1.1.0.0, ES#70P3264, EC#J97129, Jul. 2007.
- [91] IBM Microelectronics Division, "BiCMOS-8HP Model Reference Guide," Prod. Spec., V1.1.2.0HP, Aug. 2010.
- [92] IBM Microelectronics Division, "BiCMOS8WL Design Manual," Essex Junction, VT, Prod. Spec., V1.2.0.0, ES#39X6068, EC#L94449, Dec. 2009.
- [93] IBM Microelectronics Division, "BiCMOS-8WL Model Reference Guide," Prod. Spec., V1.2.0.0, Nov. 2009.
- [94] IBM Microelectronics Division, "BiCMOS 7HP Design Manual," Prod. Spec., V2.2.0.0, ES#75H3488, EC#J77708, Nov. 2004.

- [95] IBM Microelectronics Division, "BiCMOS7HP Model Reference Guide," Prod. Spec., V2.2.2.0, Mar. 2006.
- [96] IBM Microelectronics Division, "BiCMOS-7WL Model Reference Guide," Prod. Spec., V1.8.1.0, Mar. 2011.