Amorphous In-Ga-Zn-O Thin-Film Transistor for High Resolution Active Matrix Flat Panel Displays and Imagers

by

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For my family
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ABSTRACT

Amorphous In-Ga-Zn-O Thin-Film Transistor for High Resolution Active Matrix Flat Panel Displays and Imagers

by

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Chair: Jerzy Kanicki

There is considerable interest in adapting amorphous Indium-Gallium-Zinc-Oxide thin-film transistors (a-IGZO TFTs) in such applications as active matrix flat panel displays (AM-FPDs) and imagers (AM-FPIs), because of their high mobility (> 10 cm²/V·sec) in the amorphous phase, low off-current (< 10⁻¹³ A) and suitability for low temperature fabrication. So far much of the research efforts on a-IGZO TFTs have been focused on improving the a-IGZO material properties as well as the gate dielectric/a-IGZO interface.

However, the electrical performance of TFTs is also influenced by the TFT structures. In this study, the characteristics of the double gate (DG) coplanar homojunction a-IGZO TFTs are investigated. The coplanar homojunction a-IGZO TFT has a good ohmic source/drain (S/D) junction. With DG structure, a high on-current and steep subthreshold swing (100 mV/dec) are achieved without any changes in the off-current by applying the same voltage on the bottom and top gates. The dynamic control of TFT’s threshold voltage is also demonstrated by applying various voltages on the top gate. To explain these phenomena, analytic models of DG a-IGZO TFTs
are developed based on device physics. Furthermore, this study shows that the illumination ($200 \leq \lambda \leq 2400$ nm) and bias-temperature stabilities are enhanced in comparison to traditional single gate a-IGZO TFTs. The superior electrical properties and stability of the DG a-IGZO TFT make it possible strong candidates for use in pixel circuits of future high resolution AM-FPDs and AM-FPIs.
CHAPTER I

Introduction

The development of a digital broadcasting system and high speed network led to growing demands for large size displays with high resolution, resulting in flat panel displays (FPD) becoming a mainstream technology. With FPD technology, a display unit has the advantages of being lightweight and occupying little space while also having the capabilities of a large size displaying area. A number of different FPD technologies have been introduced in the market, such as the active matrix liquid crystal display (AM-LCD), plasma display panel (PDP), active matrix organic light emitting display (AM-OLED) and electronic-ink (e-ink). Among these technologies, the (AM-LCD) has been the most successful and is expected to occupy nearly 80 % of the entire consumer FPD market at the year of 2012. [33]

The AM-LCD is composed of the cover glass, liquid crystal layer and active-matrix backplane (or backplane in short) and its schematic drawing is shown in Figure 1.1(a). The cover glass is a glass plate at the front, including red-green-blue (RGB) color filters, a polarizer and a transparent common electrode. Indium-Tin-Oxide (ITO) is widely used for the common electrode that is electrically connected to the ground. The active-matrix backplane consists of a array of the thin-film transistor (TFT) pixel circuits, which directly control the charges on each pixel in the liquid-crystal. Because of the switching action of TFTs, only the selected pixel receives a charge, and
the interference by the neighboring pixels is eliminated. As a result, the resolution of AM-LCDs can be dramatically increased in comparison to passive–matrix displays. The current market dominant product of AM-LCDs has a pixel numbers around three millions (\( = 1920 \times 1080 \times 3\text{(RGB)}\)). Accordingly, TFTs are fundamental building blocks for state-of-the-art FPDs. The back polarizer is located on the backside of the backplane and the directions of front and back polarizers are perpendicular each other, providing normally black screen. Finally, the cover glass and backplane are assembled, forming a flat panel containing the liquid crystal layer in between. The orientation of the liquid crystal, which is controlled by the TFT, determines the transparency of the pixel. The TFT array in the backplane is sketched in Figure 1.2(a) and its unit pixel circuit is shown in 1.2(b).

\section*{1.1 Limitations of a-Si:H TFT Backplane Technology for Future High Resolution Display}

The circuit schematic of AM-LCD’s unit pixel is given in Figure 1.2(b). \( C_{ST} \) is the storage capacitance and \( C_{LC} \) is the internal capacitance of the liquid crystal. The driving scheme of AM-LCD is drawn in Figure 1.3. When the TFT turns ON for the gate selection time \( (t_{sel}) \), the voltage signal on the data line \( (V_{DATA}) \) is stored/written in \( V_{ST} \) node. Thus, the desired value for \( V_{ST} \) is same as \( V_{DATA} \). Since there are presence of the resistance and capacitance (RC) in the circuit, this writing process does not occur immediately, and encounter some delay. The voltage on \( V_{ST} \) node is written by, [80]

\[
V_{ST} = V_{DATA} \left( 1 - e^{-\frac{t}{RC}} \right)
\]

where \( V_{DATA} \) is the data voltage (signal), \( t \) is time. \( R \) and \( C \) are the total resistance and capacitance for the writing process, respectively. From Equation 1.1, when \( t =
Figure 1.1: The schematic cross sectional view of a typical active matrix liquid crystal display (AM-LCD) panel and its microscopic top view; The pixel makes white color when three sub-pixels (red, green, blue sub-pixels) are fully on. [53]
Figure 1.2: The array schematic of AM-LCDs backplane and its unit pixel circuit. The TFT turns on for the gate selection time ($t_{sel}$) and the data signal ($V_{DATA}$) is stored/written in $V_{ST}$ node.

Figure 1.3: Driving scheme of the AM-LCD pixel circuit for different gate-selection time ($t_{sel}$): (a) The charging time ($t_{charge}$) is smaller than $t_{sel}$; (b) $t_{charge}$ is larger than $t_{sel}$.
Figure 1.4: Different gate-selection time, calculated from Equation 1.3, for various resolutions and refresh rates. The terminologies for the different resolutions are tabulated in Table 1.1

5·RC, $V_{ST}$ reach 99.3% of $V_{DATA}$. Therefore, the required time to charge $V_{ST}$ node (i.e. pixel charging time, $t_{charge}$) is about 5·RC. If $t_{sel}$ is shorter than $t_{charge}$, $V_{ST}$ has not enough time to reach $V_{DATA}$, resulting in the writing error. This situation is shown in Figure 1.3(b) Therefore, the following is the ground rule of the pixel design.

$$t_{sel} > t_{charge} = 5 \cdot RC$$  \hspace{1cm} (1.2)

and the gate selection time, $t_{sel}$, is calculated by the following equation.

$$t_{sel} = \frac{\text{Frame Time}}{\frac{1}{\text{Refresh Rate}} \cdot \text{Number of Pixels in Vertical}}$$
$$= \frac{\text{Frame Time}}{\text{Number of Pixels in Vertical} \cdot \text{Refresh Rate}}$$  \hspace{1cm} (1.3)

The $t_{sel}$ for the different resolutions and refresh rates are illustrated in Figure 1.4.
Table 1.1: Terminologies for the different display resolution

<table>
<thead>
<tr>
<th>Terminology</th>
<th>Resolution (Horizontal × Vertical)</th>
<th>Number of Pixels</th>
<th>Number of Sub-pixels</th>
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<tr>
<td>High Definition (HD)</td>
<td>1366 × 768</td>
<td>1,049,088</td>
<td>3,147,264</td>
</tr>
<tr>
<td>Full HD (FHD)</td>
<td>1920 × 1080</td>
<td>2,073,600</td>
<td>6,220,800</td>
</tr>
<tr>
<td>Ultra HD (UHD or 4K2K)</td>
<td>3840 × 2160</td>
<td>8,294,400</td>
<td>24,883,200</td>
</tr>
<tr>
<td>Super High Vision (8K4K)</td>
<td>7680 × 4620</td>
<td>35,481,600</td>
<td>106,444,800</td>
</tr>
</tbody>
</table>

The R and C are described as

\[ R = R_{DATA} + R_{TFT-ON} \quad \text{and} \quad C = C_{ST} + C_{LC} + C_{p-TFT} + C_{p-DATA}. \]  \hspace{1cm} (1.4)

\( C_{p-TFT} \) is the parasitic capacitance of TFT and \( C_{p-DATA} \) is the parasitic capacitance of the data line, mainly contributed by the crosssectional area between gate and data lines. \( R_{DATA} \) is the resistance of the data line and \( R_{TFT-ON} \) is an ON-state resistance of TFT. \( R_{TFT-ON} \) is estimated as

\[ R_{TFT-ON} = \frac{V_{DS}}{I_D} = \frac{1}{W/L C_G \mu_{eff} (V_{GS} - V_{TH})} \]  \hspace{1cm} (1.5)

where \( W \) and \( L \) are TFT’s channel width and length, respectively. \( V_{GS} \) and \( V_{TH} \) are gate voltage and threshold voltage the TFT.

The hydrogenated amorphous silicon (a-Si:H) TFT has demonstrated great success in the active-matrix backplane. For a typical pixel circuit with a-Si:H TFTs, \( C_{ST} + C_{LC} \approx 0.5 \) pF, \( R_{TFT-ON} \approx 1.3 \) MΩ \( (W/L = 3, \mu_{eff} = 0.5 \text{ cm}^2/\text{V} \cdot \text{sec}, V_{GS-V_{TH}} = 10 \text{ V}, C_G \approx 30 \text{ nF/cm}^2) \) and \( R_{DATA} \approx 50\text{kΩ} \) for the data line on a 55-inch display \( \text{(Molybdenum / Aluminum / Molybdenum tri-stacked metal)} \). The corresponding \( t_{charge} \) is about 4.3 μsec. The parasitic capacitances are not considered in this calculation. When they are taken into consideration, \( t_{charge} \) would have an increased values. Moreover, \( R_{DATA} \) generally increases with the screen size. Since
$t_{\text{charge}}$ is smaller than $t_{\text{sel}}$ for FHD with 120 Hz ($t_{\text{sel}} = 7.5 \, \mu\text{sec}$), a-Si:H TFT is suitable with FHD with 120 Hz. However, since $t_{\text{charge}}$ is slightly larger than $t_{\text{sel}}$ of UHD with 120 Hz ($t_{\text{sel}} = 3.8 \, \mu\text{sec}$), the fabrication of UHD and 120 Hz displays with a-Si:H TFT is challenging. As the year of 2012, the AM-LCDs with FHD resolution, 120 Hz resolution and 55 inch in diagonal size are available in commercial market. Some engineering prototypes of UHD are demonstrated.

The future technology trends of the AM-LCDs include larger screens (over 80 inches in diagonal), and higher resolution (beyond FHD). [54, 55] Furthermore, to suppress the motion blur effect in the higher resolution, the higher frame rate (120 or 240 Hz) is necessary. [110] Lastly, three-dimensional (3D) displays have appeared on the market. The frame rates is required to be doubled because a 3D display must project at least twice pictures alternately for the left and right eyes. (240 or 480 Hz) [56]

To address $t_{\text{charge}}$ issue on the future trends, many research efforts have been devoted to reduce the RC delay. For example, the resistance would be reduced by introducing copper data line. [67, 28] The gate planarization is developed not only for the reduction of the parasitic capacitances but also the line resistance. [60] However, the reduction of $R_{\text{TFT-ON}}$ is limited by $\mu_{\text{eff}}$, which is inherent characteristics of the TFT’s channel material. Ban et al. calculated the required $\mu_{\text{eff}}$ for the future display trends and concluded that a-Si:H TFTs does not fulfill the mobility requirement of the display beyond the Full HD and 120 Hz. [45, 8] The required mobility for different resolutions and refresh rates are summarized in Figure 1.5 In summary, new TFT materials for the higher field effect mobility around $10 - 20 \, \text{cm}^2/\text{V} \cdot \text{sec}$ or even higher are desired for future displays.

In addition to the popularization of AM-LCD, the active matrix organic light emitting display (AM-OLED) is emerging as another mainstream technology. It is expected to be a competitor of the AM-LCD in the near future. The simple circuit
Figure 1.5: Graphical summary of required field effect mobility, $\mu_{eff}$, for future displays; reorganized based on [45]

schematic of AM-OLEDs is shown in Figure 1.6. Unlike the AM-LCD, OLEDs require high current because OLED pixels emit light by electrical current injection (i.e. an OLED is a current-driven device). [70] Therefore, the driving TFT ($T_{DR}$ in Figure 1.6) for the AM-OLED must be capable of high-current driving. [94] In addition, even a small fluctuation of TFT parameters, such as threshold voltage ($V_{TH}$), results in an unacceptable difference in the brightness of OLED pixels. Jeong et al. reported that a variation in $V_{TH}$ of only 0.1V changes the OLED’s luminance by 16 %. [36] Therefore, the new material of TFTs having a high field effect mobility and better electrical stability (lower $\Delta V_{TH}$) are highly desired for AM-OLEDs.

Even though a poly-crystalline silicon TFT (poly-Si TFT) has a larger mobility (around 100 cm$^2$/V·sec), due to the recrystallization process during the manufacturing, there is an issue of high cost manufacturing. The recrystallization is typically done by the excimer-laser annealing (ELA). Moreover, due to a grain boundary of
poly-crystalline material, the uniformity of TFT’s performance is not always acceptable for the display application. [29, 44] Therefore, there is an increasing demand for a new TFT material to achieve the above mentioned requirements.

1.2 Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors (a-IGZO TFTs)

Even though the crystalline silicon (c-Si) has a mobility over 500 cm$^2$/V·sec, a typical field effect mobility of a-Si:H TFTs is only 0.5 - 1.0 cm$^2$/V·sec. The origin of the mobility degradation in a-Si:H TFT is associated with the intrinsic nature of the chemical bonding: covalent bonds between Si atom’s sp$^3$ hybrid orbitals. The Si atom is crystallized into the diamond structure through the sp$^3$ hybrid orbital, in which each atom has four nearest neighbor Si atoms. Since the sp$^3$ orbital has strong directivity, the bonding angle fluctuation by the disorder in the amorphous phase significantly alters the energy band structure and the density of states and creates deep tail-states.
Figure 1.7: Shapes of electron orbitals: (a) n-s orbital (b) n-p orbitals, and (c) n-sp$^3$ hybrid orbitals (one s orbital and three p orbitals), where n is the principle quantum number. The shape of sp$^3$ orbital is directional, however, that of s orbital is isotropic.

Therefore, the carrier transport is controlled by hopping between localized tail-states, rather than the band conduction, and resulting in mobility degradation. [95]

On the other hand, an amorphous oxide semiconductor (AOS) has a mobility similar to that of the corresponding crystalline phase. These features are completely different from those of the covalent semiconductors. The bottom of the conduction band in the oxide semiconductors that has high ionicity is primarily composed of spatially spread metal n-s orbitals with an isotropic shape, where n is the principal quantum number. Moreover, direct overlap among the surrounding metal n-s orbitals is possible. It is expected that the delocalized s orbitals of heavy metal cations would form a largely dispersed conduction band with a small electron effective mass, resulting in high-mobility amorphous oxide conductors. The difference in shapes between s and sp$^3$ orbitals is sketched in Figure 1.7.

The magnitude of this overlap among the n-s orbitals is insensitive to distorted metal-oxygen-metal (M-O-M) chemical bonds that intrinsically exist in amorphous
Figure 1.8: Schematic orbital drawing: (a) crystalline covalent semiconductor, (b) amorphous covalent semiconductor, (c) crystalline metal oxide semiconductor, and (d) amorphous metal oxide semiconductor (credit of Nomura et al. [81])

materials. [32, 82] The AOS, therefore, exhibits a large mobility in amorphous phase, which is similar to those of the corresponding crystalline phase. [81] Figure 1.8 illustrates the atomic structure of oxide semiconductors in its crystalline and amorphous phase and its comparison to the covalent-bond semiconductor, such as Silicon.

ZnO – ZnO TFTs have been regarded as the representative of oxide semiconductors – has been studied intensively for channel layers in TFTs after their first development in 1960’s. [9] However, it is recognized that ZnO TFTs still have shortcomings preventing them from being adopted for AM-FPI and AM-FPD applications. For example, the channels of ZnO TFTs are polycrystalline even if deposited at room temperature. Therefore, the field-effect mobilities and long-term stability suffer from
grain-boundary problems, similar to the grain boundary issues observed in polycrystal-
line silicon (poly-Si) TFTs. [29, 44]

To change ZnO materials into an amorphous phase, Orita et al. tried incorporating
In$_2$O$_3$ into ZnO. [82] Since it is known that In$_2$O$_3$ tends to be formed in an amorphous
phase, the combination of In$_2$O$_3$ and ZnO is expected to produce an amorphous phase.
Furthermore, In$^{3+}$ metal cations have a larger ionic radius (5-s) than a Zn$^{2+}$ cation,
resulting in a larger overlap between metal ions even in an amorphous phase. This
suggests that the incorporation of n-s orbitals with a large principal quantum number
(such as n > 4) is favorable for forming a greatly dispersed conduction band minima
(CBM), which leads to a high electron mobility. [78, 32] This is the reason why many
transparent conductive oxides, such as SnO$_2$ and Indium tin oxide (In$_2$O$_3$–SnO$_2$))
are composed of heavy post-transition metal cations such as In and Sn. [27] Another
reason of greatly dispersed CBM is found in ZnO. A short distance of Zn-Zn increases
the dispersion of CBM, resulting in high electron mobility.

Another requirement to be considered is that oxide semiconductors must have con-
trollable carrier concentrations since oxygen vacancies are easily formed and generate
excess of free electrons. To suppress the generation of the free carriers via the forma-
tion of oxygen vacancies, the incorporation of stronger metal-oxygen bonds would be
desirable. Therefore, it is essential to choose a material in which carrier concentration
can be controlled at a low level. It is known that Ga$^{3+}$ ion forms stronger chemical
bonds with oxygen than either Zn or In. [52] It is shown that incorporation of Ga$^{3+}$
is effective in suppressing carrier generation via oxygen vacancy in metal oxides. [31]

Finally, it has been confirmed in many labs, TFTs with a ternary compound of
In–Ga–Zn–O (or In$_2$O$_3$–Ga$_2$O$_3$–ZnO) have capabilities of achieving an amorphous
phase, high mobility, and high ON-OFF ratio. In a-InGaZnO TFTs, CBM is formed
by Indium’s 5-s orbital, and the valence band maxima (VBM) is primarily constructed
by Oxygen’s 2-p orbital. [14] The amorphous phase of a-IGZO is thermally stable
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$</td>
<td>$\approx 3.05$ eV</td>
<td>optical bandgap [18]</td>
</tr>
<tr>
<td>$E_a$</td>
<td>$\approx 26$ meV</td>
<td>activation energy [11]</td>
</tr>
<tr>
<td>$m_c$</td>
<td>$\approx 0.35 m_e$</td>
<td>conduction band effective mass [23]</td>
</tr>
<tr>
<td>$\mu_{band}$</td>
<td>$\approx 15$ cm$^2$/V·sec</td>
<td>band mobility in a-IGZO TFT (conduction band, estimated) [23]</td>
</tr>
<tr>
<td>$\mu_{eff}$</td>
<td>$5 - 20$ cm$^2$/V·sec</td>
<td>field effect mobility in a-IGZO TFT</td>
</tr>
<tr>
<td>$\sigma_{dark}$</td>
<td>$\approx 2 \times 10^{-5}$ S·cm$^{-1}$</td>
<td>dark conductivity of single crystal (sc) IGZO [61]</td>
</tr>
<tr>
<td>$\sigma_{photo}$</td>
<td>$\approx 5 \times 10^{-3}$ S·cm$^{-1}$</td>
<td>photo conductivity of sc IGZO) [61]</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>$&lt; 10^{-14}$ A</td>
<td>off current in a-IGZO TFT</td>
</tr>
<tr>
<td>$T$</td>
<td>$\sim 90%$</td>
<td>transmittance for $\lambda &gt; \sim 400$ nm [21]</td>
</tr>
</tbody>
</table>

Table 1.2: The characteristics of a-IGZO semiconductor

up to 500°C in air. [81] The In$_2$O$_3$/Ga$_2$O$_3$/ZnO ratio of 1:1:1 or 1:1:2, also called In$_2$Ga$_2$ZnO$_7$ and InGaZnO$_4$, respectively, so far have received the most available attention because of readily sputtering targets. The properties of a-IGZO semiconductor film and a-IGZO TFTs are summarized in Table 1.2.

### 1.3 Thesis Organization

This dissertation commences with discussions of the field effect mobility requirements for high resolution AM-FPD and -FPI. In Chapter II, the design consideration of a high-resolution imager is investigated and the mobility requirement is calculated for future AM-FPIs. Thanks to previous intensive research studies on a-IGZO TFTs, it has been empirically shown by many labs that a-IGZO TFTs with $\mu_{eff}$ over 10 cm$^2$/V·sec can be easily fabricated. So far much of the research efforts have been focused on improving the a-IGZO material properties as well as the gate dielectric/a-IGZO interface.

However, it is important to keep in mind that the electrical performance of TFTs is also influenced by the device structures such as the TFT dimensions and the configuration of gate electrodes. Therefore, in Chapter III, an in-depth study of the scaling dependency of a-IGZO TFTs is presented. For further enhancement of the electrical
characteristics of a-IGZO TFTs, double gate (DG) a-IGZO TFTs are introduced in Chapter IV. To provide a mathematical and physical background of DG a-IGZO TFTs, the equations for the transfer characteristics, sub-threshold swing, and saturation voltage are analytically developed based on the device physics in Chapter V. The validity of the developed model is proven by comparison to the experimental results. In Chapter VI, the instability of the DG a-IGZO TFT are discussed. Lastly, conclusions and recommendations for further research are given in Chapter VII.
CHAPTER II

Design of High Resolution Active Matrix Flat Panel Imagers

As discussed in § 1.1, a-Si:H TFT active-matrix backplane has demonstrated great success in its applications to large area active matrix flat panel displays (AM-FPDs). Since the development of the concept of the active-matrix backplane, the active-matrix backplane has been adapted in the field of active matrix flat panel imagers (AM-FPIs) by substituting the liquid-crystal cell or organic light-emitting diode with a light-sensing element such as a photodiode. The active-matrix backplane are very useful for medical imaging because the imager can have a size comparable with that of a human body. The manufacturing process of a-Si:H TFTs allows them to be deposited on a large substrate, making them ideal for medical imaging, such as radiography. The AM-FPIs with the a-Si:H TFT backplane can facilitate radiology compared with the traditional film approach by enabling digital image processing and handling. The a-Si:H TFTs backplane on a 20-inch-diagonal substrate with up to $2304 \times 3200$ pixels at $127 \, \mu m$ pixel pitch have been developed for radiology and are currently in mass production. [105] The pictures and technical specifications of the commercialized flat panel imager are shown in Figure 2.1.

As shown in this figure, even though the AM-FPIs with a-Si:H TFT backplane technology has been shown to be successful when applied to radiology, the AM-FPIs
for mammography or tomosynthesis, however, are still under developing. Mammography refers to X-ray radiology used for investigating the breast cancer of symptomatic patients, and tomosynthesis is a three dimensional mammography that reconstructs a series of two dimensional mammography images taken from different viewing angles. As an extension of mammography, tomosynthesis may offer better detection rates. An interested object of radiology is a bone or bone detail with a typical size of 0.5 mm. In contrast, tomosynthesis has to detect cancer cells that are only 50 - 100 \( \mu \text{m} \) in its size. Hence, tomosynthesis requires a 50 \( \mu \text{m} \) pixel pitch. Furthermore, in tomosynthesis, a rapid sequence of \( N \) images is obtained when the X-ray source sweeps through different angular views of the object. Since the total dose of X-rays to the breast must be kept the same as that in regular mammography or radiography, the exposure used for each image of tomosynthesis is \( 1/N \). \( (N \geq 25) \) \[111\] Therefore, the readout speed and sensitivity should be \( N \) times larger than the mammography.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Samsung (Xmaru 1717)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Matrix</td>
<td>PPS with a-Si:H TFT</td>
</tr>
<tr>
<td>Field of view</td>
<td>( 43 \text{ cm} \times 43 \text{ cm} )</td>
</tr>
<tr>
<td>Pixel count</td>
<td>( 3072 \times 3072 )</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>( 147 \mu \text{m} \text{ (FF=unknown)} )</td>
</tr>
<tr>
<td>Detector</td>
<td>CsI:TI scintillator</td>
</tr>
<tr>
<td>Weight</td>
<td>13.4 kg</td>
</tr>
<tr>
<td>Dimension</td>
<td>( 50 \times 49.7 \times 4.5 \text{ cm} )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>dpx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Matrix</td>
<td>PPS with a-Si:H TFT</td>
</tr>
<tr>
<td>Field of view</td>
<td>( 29.3 \text{ cm} \times 40.6 \text{ cm} )</td>
</tr>
<tr>
<td>Pixel count</td>
<td>( 2304 \times 3200 )</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>( 127 \mu \text{m} \text{ (FF=0.57)} )</td>
</tr>
<tr>
<td>Detector</td>
<td>CsI:TI scintillator</td>
</tr>
<tr>
<td>Weight</td>
<td>unknown</td>
</tr>
<tr>
<td>Dimension</td>
<td>( 42.2 \times 30.8 \times 1.1 \text{ cm} )</td>
</tr>
</tbody>
</table>

Figure 2.1: Commercialized flat panel imagers for Radiography, and its technical specification \([74, 25, 105]\)
The requirements of the active-matrix backplane for radiography, mammography, and tomosynthesis are summarized in Table 2.1. [112]

<table>
<thead>
<tr>
<th></th>
<th>Radiography</th>
<th>Mammography</th>
<th>Tomosynthesis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Field of View (cm×cm)</td>
<td>35 × 43</td>
<td>18 × 24</td>
<td>18 × 24</td>
</tr>
<tr>
<td>Pixel Pitch (p) (µm×µm)</td>
<td>200 × 200</td>
<td>50 × 50</td>
<td>50 × 50</td>
</tr>
<tr>
<td>Pixel Count (ea. × ea.)</td>
<td>1750 × 2150</td>
<td>3600 × 4800</td>
<td>3600 × 4800</td>
</tr>
<tr>
<td>Readout Speed (Hz)</td>
<td>0.2</td>
<td>0.2</td>
<td>&gt;5</td>
</tr>
<tr>
<td>Dynamic Range (dB)</td>
<td>30</td>
<td>50</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 2.1: Requirements of different medical imaging methods

From the table, it is clearly shown that the backplane with the requirements of high-resolution (3,600 × 4,800), 60 dB dynamic range (DR), small pixel pitch (p = 50 µm) and 5 Hz operation needs to be developed for tomosynthesis. The smallest pitch of the commercialized unit in the market is still only 127 µm. There have been demonstrations of a 64 µm pixel pitch for research purpose. [86] This value is still 34% larger than the requirement. In this chapter, we studied the design consideration of the pixel circuit for those requirements.

2.1 Passive Pixel Sensor

2.1.1 Operation Principles and Layout of PPS

Passive pixel sensor (PPS) is the simplest structure and offers very compact and small pixel pitch. PPS shown in Figure 2.2(a) consists of a photodiode (PD) connected to a read transistor (T\textsubscript{READ}), and a storage capacitor (C\textsubscript{ST}). The difference from the pixel circuit of AM-LCDs is the photodiode, which is substituting liquid-crystal elements. The choice of PPS architecture as an initial point of the research is primarily due to its long standing history of use in AM-LCDs. It is passive in a sense that
TFT’s functions is as simple passive switching in this configuration. The example circuit schematic for \( N \times N \) pixels array is shown in Figure 2.2(b).

There are two modes of operation in PPS: [50]

- **Integration mode** \((t_{int})\): \( T_{READ} \) is open (OFF) and the signal charges generated by PD accumulates on \( C_{ST} \) (\( V_S \) node). The value of \( V_S \) is proportional to the amount of incoming illumination/radiation. During the integration period, the \( T_{READ} \) should be completely OFF and not conduct. However, a small leakage current of TFT still flows through the \( T_{SW} \) channel during \( t_{int} \). Thus, the voltage across the \( C_{ST} \) can be changed and the signal corruption arise from this change.

- **Readout/Reset mode** \((t_{read})\): Following the integration mode, \( T_{READ} \) is turned ON and the accumulated signal charges on \( C_{ST} \) are transferred to an external readout circuit via the data line. At the end of the readout period, the charge on \( C_{ST} \) is reset to zero and the pixel is ready for the next integration mode. In case of 3,600 \( \times \) 4,800 array and 5 Hz operation, one column (or data line) has 3,600 \( T_{READs} \). Every each of 3,600 \( T_{READ} \) must be scanned for one frame time. \((\frac{1}{5 \text{Hz}})\) Thereby, the allowed \( t_{read} \) for a single pixel’s \( T_{READ} \) is

\[
t_{read} = \frac{1/5 \text{ second}}{3600} = 55.5 \text{ } \mu\text{second}
\]

(2.1)

Since the TFT in PPS circuit is a simple switch, it does not provide any signal amplification. The example layout of PPS with a pixel pitch of 200 \( \mu \text{m} \) is given in Figure 2.3. The minimum feature size (i.e. design rule) of 10 \( \mu \text{m} \) is used for the drawn layout. The TFT’s \( W/L \) is 100/10 \( \mu \text{m} \). The line width of data and read line is 10 \( \mu \text{m} \).
Figure 2.2: (a) circuit schematic of unit PPS pixel, (b) PPS N×M array configuration
Figure 2.3: Example layout (a) and cross-sectional structure (b) of passive pixel sensor (PPS); the pixel pitch is 200 \( \mu \text{m} \). (a) and (b) is not in same scale.
2.1.2 Design of 50 µm Pixel-Pitch PPS with Enhanced Fill Factor

A fill factor (FF) is an important factor to be addressed for achieving a high resolution pixel array. FF is defined by the ratio of the photodiode’s area to the total pixel area.

\[ FF = \frac{\text{area of pixel electrode}}{\text{area of a unit pixel}} \] (2.2)

In standard in-plane structure of PPS, Figure 2.3(b), TFT is in the same level with image sensor. Thus, TFT must share the pixel area with photo diode. Therefore, a photodiode is placed next to the T\textsubscript{READ} and other bus lines, such as DATA, V\textsubscript{READ} and V\textsubscript{BIAS}. The placement of PD must be done with careful consideration of TFT area and the space to neighboring pixels. FF can be estimated from a given set of design rules using the following equation[87];

\[ FF = \frac{(p - g)^2 - A\textsubscript{TFT}}{p^2} \] (2.3)

where, p is pixel pitch, g is a gap between PDs in the nearest neighbor pixels, and A\textsubscript{TFT} is occupying area of TFT in the unit pixel. g would be around three times of the minimum feature size. For the PPS circuit in Figure 2.3 the minimum feature size of 10 µm is used, g is measured in 30 µm. A\textsubscript{TFT} 3,000 µm\(^2\) for T\textsubscript{SW} having W/L = 100/10 (µm/µm). In case of the minimum feature size with 5 µm , g would be 15 µm and A\textsubscript{TFT} is 750 µm\(^2\).

To validate equation 2.3, the estimated FF from equation 2.3 is compared with the empirical FF in Table 2.2 and Figure 2.4. The g and A\textsubscript{TFT} is chosen as 15 µm and 750 µm\(^2\), respectively. We can conclude that the two columns in Table 2.2, empirical and estimated values, show a reasonable correlation. From Figure 2.4, it is clearly shown that FF decreases along with pixel pitch, and FF is expected to be less than 50 % when p = 100 µm. Moreover, FF is converging into 0 % as the pixel pitch is
approaching into 50 µm, implicating that there is not enough area for the photodiode to be squeezed in the pixel layout. The standard in-plane PPS structure, therefore, is impracticable when the pixel pitch is around 50 µm. In in-plane PPS structure, the photodiode is sharing pixel area with the $T_{READ}$. This is the origin of decreased FF.

<table>
<thead>
<tr>
<th>Pixel Pitch</th>
<th>Empirical FF</th>
<th>Estimated FF</th>
<th>Reference</th>
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</thead>
<tbody>
<tr>
<td>508</td>
<td>0.84</td>
<td>0.90</td>
<td>[5]</td>
</tr>
<tr>
<td>224</td>
<td>0.86</td>
<td>0.79</td>
<td>[102]</td>
</tr>
<tr>
<td>127</td>
<td>0.57</td>
<td>0.63</td>
<td>[104]</td>
</tr>
<tr>
<td>97</td>
<td>0.45</td>
<td>0.52</td>
<td>[37]</td>
</tr>
</tbody>
</table>

Table 2.2: The comparison empirical fill factor (FF) and estimated FF for PPSs with different pixel pitch

In another approach to address the vanishing FF, the vertically stacked structure has been introduced. In comparison to the in-plane structure, the TFT and photodiode are constructed in different levels. By stacking the photodiode on the top
of TFT, it is possible for the photodiode to occupy the most of pixel area without obstruction with the TFT. (Figure 2.5(a)) FF in stacked PPS structure is described as:

\[
FF = \frac{(p - g)^2}{p^2}
\]  

(2.4)

and FF of the vertically stacked PPS is also compared with the in-plane PPS in Figure 2.4.

For PPS with \( p = 50 \mu m \), the vertically stacked PPS has estimated FF of 81% from Equation 2.4. Furthermore, the light-shield layer can be introduced without sacrificing FF. (see Figure 2.5(a)) Therefore, the light shield layer is embedded to prevent the active channel of the \( \text{T}_{\text{READ}} \) from the illumination. Although the light shield layer requires additional process steps, such as passivation layer and via-definition, it allows TFT’s leakage current to be kept lower during imager operation.

The vertical structure and layout of 50 \( \mu m \)-pixel-pitch PPS (vertically stacked) are shown in Figure 2.5 and the complete fabrication process steps are illustrated in Figure 2.6. Seven photo-mask process steps are required to fabricate a complete pixel structure including the light-shield and bottom electrode of a photodiode. The fork-shaped a-Si:H TFT (\( W/L = 40/5 \)) is used for \( \text{T}_{\text{SW}} \). The gate capacitance per unit area \( (C_G) \) 17.6 nF/cm² for 4000 Å-thick Si\(_3\)N\(_4\) gate dielectric layer and \( C_{ST} \) is 0.1 pF. The designed FF is 81%. The fabricated 128 \( \times \) 128 PPS imager with FF = 81% are shown in Figure 2.7

2.1.3 Limitation of PPS

Another important factor in the pixel circuit is electronic noise. There are three noise sources on PPS circuit; TFT’s thermal noise, TFT’s flicker noise and external amplifier’s noise. Among these three noise sources, it is known that the amplifier
Figure 2.5: Vertically stacked PPS structure with FF = 81%; (a) vertical cross-section and (b) layout

Noise is dominant. [112] The noise sources from the photodiode are not considered in this study. External amplifier’s noise can be determined by [79]

\[ N_{\text{amp}} = N_{\text{amp0}} + N_k C_d \]  

(2.5)

In Equation 2.5, the amplifier noise \( N_{\text{amp}} \) can be modeled as having a fixed noise component of the amplifier \( N_{\text{amp0}} \) in addition to capacitance dependent component \( N_k C_d \). \( N_{\text{amp}} \) and \( N_k \) are an amplifier’s characteristic constants. \( C_d \) is the capacitance loading at the amplifier’s input node, which mainly includes the parasitic capacitance on the data line, \( C_{\text{DATA}} \). (Figure 2.8) For the specific low-noise amplifier (Burr-Brown IVC102P), \( N_{\text{amp0}} \) is founded as 250 electrons and \( N_k \) as 15 electrons/pF.

[1] The dominant contribution to \( C_{\text{DATA}} \) is the capacitance from the overlap area between each gate line (\( V_{\text{READ}} \) and \( V_{\text{READ}} \)) and data line. From Table 2.1, for the tomosynthesis, there are 3600 pixels in one data line and each pixel has two overlap
Figure 2.6: Detailed fabrication steps of the vertically stacked PPS with the light shield capability.
Figure 2.7: The fabricated imager backplane with $128 \times 128$ PPS. The fill factor (FF) of 81% is achieved by the vertically stacked structure. (a) mask design for 4-inch substrate, (b) the picture of the fabricated $128 \times 128$ imager on a glass substrate, (c) the imager bonded with the flexible printed circuit (FPC), these FPCs will be connected the external readout circuits and (d) detailed microscopic top view of the fabricated PPS array.
area has 0.1 pF (= 2 \times C_G \cdot (5 \times 5 \ \mu m^2)) of capacitance.

\[ C_{DATA} = 360 \ \text{pF} (= 0.1 \times 3600) \]  

Finally, the noise from the external amplifier, \( N_{amp} \) is calculated as 5650 electrons. The minimum detectable number of electron \((N_{min})\) is 10 times more than \( N_{amp} \), therefore \( N_{min} = 5.65 \times 10^4 \) electrons. [112].

In addition, we need to find the maximum detectable number of electrons. \((N_{max})\)

Since PD should be remained in the reverse bias condition, \( V_S \) node on PPS cannot exceed \( V_{BIAS} - V_{ON-PD} \), where \( V_{ON-PD} \) is the turn-on voltage of PD. Also, the minimum \( V_S \) value is set to 0 V during the reset mode. The voltage range on \( V_S \) node is

\[ 0 \leq V_S \leq (V_{BIAS} - V_{ON-PD}) \]  

By assuming \( V_{ON-PD} < 1 \), \( V_{BIAS} = 20 \ \text{V} \) for a-Si:H TFT PPS circuit, the voltage range on \( V_S \) is roughly same as \( V_{BIAS} \).

\[ \Delta V_S = V_{BIAS} - V_{ON-PD} \approx V_{BIAS} \]  

27
The $\Delta V_S$ is corresponding to the maximum detectable number of charge ($N_{\text{max}}$).

From the parallel plate capacitor model, $Q = C \cdot V$.

$$N_{\text{max}} = \left| \frac{C_{ST} \times \Delta V_S}{q} \right| \text{ (electron)} \quad (2.9)$$

where $q$ is the electric charge of the single electron. $N_{\text{max}}$ is about $1.25 \times 10^7$ electrons for $V_{\text{BIAS}} = 20$ V and $C_{ST} = 0.1$ pF. The dynamic range (DR) of the pixel circuit is from $N_{\text{min}}$ to $N_{\text{max}}$. As calculated above, our designed 50 $\mu$m pitch PPS has the dynamic range of $5.65 \times 10^4 - 1.25 \times 10^7$ electrons. DR in the unit of dB is calculated by

$$\text{Dynamic Range (dB)} = 20 \times \log_{10} \frac{N_{\text{max}}}{N_{\text{min}}}$$

$$= 20 \times \log_{10} \frac{1.25 \times 10^7}{5.65 \times 10^4} = 46.89 \text{dB} \quad (2.10)$$

This value does not meet the tomosynthesis requirement. Moreover, once the other noise sources, which are not included here, take into the consideration, there is further reduction on the DR. The DR of the fabricated PPS with 50 $\mu$m pixel pitch is measured as about 40 dB, that is slightly smaller than the value in Equation 2.10.

While PPS pixel circuit has the advantage of being compact, amenable to smaller pixel pitch, ironically, the number of detectable signal charges are reducing with the smaller pixel pitch. In order to overcome this problem, an alternative pixel architecture, an active pixel sensor (APS), has been proposed in next section.

### 2.2 Active Pixel Sensor

To increase DR, the amplification of the input signal is necessary. In the APS, the signal voltage at the detector node is converted and amplified to current using an amplifier TFT, resulting in improved noise and/or readout-speed performance. In
The APS unit pixel consists of three transistors ($T_{RST}$, $T_{READ}$, and $T_{AMP}$), one storage capacitor ($C_{ST}$) and a photodiode. Contrast to a PPS, an APS consists of three TFTs, namely, reset, read, and amplifying TFT. ($T_{RST}$, $T_{READ}$, and $T_{AMP}$, respectively) [48] These three TFTs are shown in Figure 2.9. These increased number of TFTs will undermine the fill factor if in-plane structure are used. Therefore, the vertically stacked structure is utilized again, so three TFTs are embedded below the photodiode to provide the maximum fill factor. APS operation has three distinct periods: reset, integration and readout periods.

- **Reset mode** ($t_{reset}$): $T_{RST}$ is switched ON, the voltage on $V_S$ node is set to 0 V. The $T_{READ}$ is OFF in this period.

- **Integration mode** ($t_{int}$): Both $T_{RST}$ and $T_{READ}$ are OFF. During the integration time, $t_{int}$, photocurrent induced by PD accumulated in $C_{ST}$ and the accumulated charges increase the voltage on $V_S$ node. The $V_S$ is proportional to the amount of incident illumination/radiation. Again, $V_S$ cannot exceed $V_{BIAS} - V_{PD - ON}$ for the reversely biased PD. Therefore, the voltage range of $V_S$ node is same as Equation 2.7

- **Readout mode** ($t_{read}$): After integration, $T_{READ}$ is turned ON for the time, the output current ($I_{OUT}$) is flowing in to the external amplifier circuit. $I_{OUT}$ is determined by the gate voltage of $T_{AMP}$, which is same as $V_S$. $T_{AMP}$ is operating in the saturation regime. The $t_{read}$ in APS is same as Equation 2.1.
Figure 2.10: Example layout of active pixel sensor (APS); APS consists of three TFTs, one storage capacitor ($C_{ST}$) and five bus lines ($V_{BIAS}, V_{DD}, V_{READ}, V_{RESET}$ and Data line).

The example layout of APS with a pixel pitch of is shown in Figure 2.10.

2.2.1 APS Charge Gain

In contrast to PPS, APS can be designed to provide the charge gain to increase the pixel’s dynamic range. The charge gain in APS is defined by the ratio between the totally generated number of charges from APS pixel circuit ($Q_{APS}$) to the accumulated number of charges by the photodiode at $V_S$ node ($Q_{PD} = C_{ST} \cdot V_S$).

$$Q_{APS} = \text{Gain} \times Q_{PD} \quad \text{or} \quad \text{Gain} = \frac{Q_{APS}}{Q_{PD}} \quad (2.11)$$

The totally generated number of charges from APS is related to the output current ($I_{OUT}$) of $T_{AMP}$ and the readout time ($t_{read}$). Therefore, the charge gain by the amplifier TFT in APS is

$$\text{Gain} = \frac{Q_{APS}}{Q_{PD}} = \frac{I_{OUT} \times t_{read}}{C_{ST} \cdot V_S} \quad (2.12)$$
Since $T_{AMP}$ is operating in the saturation regime, and the saturation current of TFTs is described by

$$I_{OUT} = \frac{W}{2L} \mu_{eff} C_G (V_{GS} - V_{TH})^2$$  \hspace{1cm} (2.13)

where $V_{GS}$ is gate-to-source voltage of $T_{AMP}$ and $V_{GS} = V_S$. Thus, by using Equation 2.13, Equation 2.12 can be rewritten by

$$\text{Gain} = \frac{W}{2L} \mu_{eff} C_G (V_S - V_{TH})^2 \cdot t_{read} \cdot C_{ST} \cdot V_S.$$  \hspace{1cm} (2.14)

Or, if $V_{TH}$ is close to 0 V, Equation 2.14 is more simplified into Equation 2.15

$$\text{Gain} = \frac{W}{2L} \mu_{eff} \frac{C_G}{C_{ST}} V_S \cdot t_{read}.$$  \hspace{1cm} (2.15)

### 2.2.2 Requirement for High Resolution APS

As shown in Figure 2.10, one data line is crossing two gate lines ($V_{RESET}$ and $V_{READ}$) on each APS pixel. For 3600 pixels on one data line, $C_{DATA}$ is (see Equation 2.6)

$$C_{DATA} = 360 \text{ pF}$$  \hspace{1cm} (2.16)

and the number of noise electrons from the external amplifier is (Equation 2.5)

$$N_{amp} = N_{amp0} + N_k C_d = 5650 \text{ electron}$$  \hspace{1cm} (2.17)

The minimum detectable signal is at least ten times larger than

$$N_{min} \times \text{Gain} \geq 5.65 \times 10^4 \text{ electron}$$  \hspace{1cm} (2.18)
By equating Equation 2.15 and 2.18, the following equation is derived.

\[ N_{\text{min}} \times \left( \frac{W}{2L} \mu_{\text{eff}} \frac{C_G}{C_{ST}} V_S \cdot t_{\text{read}} \right) \geq 5.65 \times 10^4 \text{ electron} \quad (2.19) \]

When there are \( N_{\text{min}} \) electrons is corresponding to \( V_S = |N_{\text{min}} \cdot q/C_{ST}| \)

\[ N_{\text{min}} \times \frac{W}{2L} \mu_{\text{eff}} \frac{C_G}{C_{ST}} \frac{q \cdot N_{\text{min}}}{C_{ST}} \cdot t_{\text{read}} \geq 5.65 \times 10^4 \text{ electron} \cdot (2.20) \]

Next, we need to find \( N_{\text{max}} \). Since the voltage range of \( V_S \) in APS is same with that in PPS, the maximum detectable number of electrons is (Equation 2.9)

\[ N_{\text{max}} = \left| \frac{C_{ST} \cdot V_{\text{BIAS}}}{q} \right| \text{ electron} \cdot (2.21) \]

For the dynamic range requirement of 60 dB,

\[ \text{Dynamic Range (dB)} = 20 \times \log_{10} \frac{N_{\text{max}}}{N_{\text{min}}} = 60 \text{dB} \quad (2.22) \]

Therefore, \( N_{\text{max}} \) and \( N_{\text{min}} \) have to follow Equation 2.20, 2.21 and 2.22.

Furthermore, we can recognize from Figure 2.10 that TFT’s channel area is about 30 % of the pixel area (\( p^2 \))

\[ \text{channel area of three TFTs} = p^2 \times 0.30 = 3 \cdot (W \times L) \quad (2.23) \]

The storage capacitor is occupying 20 % of the pixel area and \( C_{ST} \) is using the same dielectric layer with the gate dielectric of TFTs

\[ C_{ST} = C_G \cdot (p^2 \times 0.20) \quad (2.24) \]

Equation 2.23 and 2.24 are named as a layout confinement.
For a-Si:H TFTs, the typical values of L, C_G and V_{BIAS} are 5 µm, 17.6 nF/cm^2 and 20 V, respectively. Computing Equation 2.20, 2.21, 2.22 2.23 and 2.24, the relation between the pixel pitch and the required \( \mu_{eff} \) of T_{AMP} is derived and summarized at Figure 2.11. In order to enable 50 µm pitch size, TFTs with the field effect mobility > 4.6 cm^2/V·sec and \( L = 5 \) µm is required. The mobility requirements would be relaxed for smaller \( L \). For example, if we set \( L = 3 \) µm, the field effect mobility of 1.8 cm^2/V·sec is enough. The APS architecture is currently used with complimentary metal-oxide-semiconductor (CMOS) technology. In CMOS image sensor (CIS), \( L \) can have very small value (\( L \leq 0.13 \) µm in the year of 2012 [20, 57]) and \( \mu_{eff} \geq 500 \) cm^2/V·sec. However, CMOS technology is not compatible with a large area AM-FPIs. Therefore, one possible solution is the new TFT technology with \( \mu_{eff} > 4.6 \) cm^2/V·sec. It has been experimentally shown that a-IGZO TFT with \( \mu_{eff} > 10 \) cm^2/V·sec can be easily fabricated even in the room temperature.
2.3 Summary

In this chapter, we investigated a vertically stacked structure for enhanced fill factor design. Even with the enhanced fill factor design, it was shown that PPS architecture is not adequate for a small pixel pitch, \( p = 50 \, \mu m \). This is because the number of signal charges (electrons) deceases with a reduced pixel pitch, while the noise level is rather constant. To address this issue, APS architecture includes the capability of on-pixel amplification. However, APS employs three TFTs and the circuit design of three TFTs in the limited pixel area is challenging. To achieve APS with 50 \( \mu m \) pixel-pitch and 60 dB dynamic range, the TFTs field-effect mobility should be larger than 4.6 \( \text{cm}^2/\text{V} \cdot \text{sec} \). The \( \mu_{\text{eff}} \) of a-Si:H TFTs is around 1 \( \text{cm}^2/\text{V} \cdot \text{sec} \) for larger channel length, \( L \geq 20 \, \mu m \), and \( \mu_{\text{eff}} \) is decreasing with smaller \( L \). From previous research [15, 47], it is shown that \( \mu_{\text{eff}} \) for \( L = 5 \, \mu m \) a–Si:H TFTs is around 0.3 - 0.5 \( \text{cm}^2/\text{V} \cdot \text{sec} \). Thus, a-Si:H TFTs are not adequate for the application. In summary, the TFTs with \( \mu_{\text{eff}} = 4.6 \, \text{cm}^2/\text{V} \cdot \text{sec} \) is necessary for the APS pixel circuit with 50 \( \mu m \) pixel-pitch and 60 dB. One possible TFT technology that can accomplish such requirement is a-IGZO TFT, that will be discussed in the next chapter.
CHAPTER III

Coplanar Homojunction a-IGZO Thin-Film Transistors and its Scaling Characteristics

As shown in Chapter 1.1, high resolution (beyond $1920 \times 1080$), high pixel density ($\geq 300$ pixels per inch, PPI), large panel size ($\geq 80$ inch) and a fast frame rate ($\geq 120$ Hz) have become key features of future technology in the area of active matrix flat panel displays (AM-FPD). The essential requisite for achieving these features is a high field-effect mobility $\mu_{\text{eff}}$ of thin-film transistors (TFTs). It is estimated that the 8K ultrahigh-definition ($7680 \times 4320$) television (Super High Vision or 8K4K TV) with 120 Hz of refresh rate requires $\mu_{\text{eff}}$ over $10 \text{ cm}^2/\text{V} \cdot \text{sec}$. [8] The high mobility requirement is also critical for the high resolution active matrix flat panel imager (AM-FPI), especially for the application of medical imaging. [96, 49] It is clearly shown that $\mu_{\text{eff}}$ over $4.6 \text{ cm}^2/\text{V} \cdot \text{sec}$ is required for tomosynthesis in Chapter II. The hydrogenated amorphous silicon (a-Si:H) TFTs are not adequate for such a high resolution application because $\mu_{\text{eff}}$ of a-Si:H TFTs has the range of $0.5 - 1 \text{ cm}^2/\text{V} \cdot \text{sec}$. [72, 85] In this regard, a-IGZO TFTs have received considerable attention as a possible replacement for a-Si:H TFTs. [65, 76, 42, 62] Thanks to previous intensive research studies on a-IGZO TFTs, it has been proved that a-IGZO TFTs with $\mu_{\text{eff}}$ over $5 \text{ cm}^2/\text{V} \cdot \text{sec}$ can be easily fabricated. [81, 59, 45]

Besides the mobility requirement, TFT miniaturization is another important fac-
tor for high pixel density applications. Since an allowed pixel size decreases as the PPI increases – the pixel size for 500 PPI is only 50.8 × 16.9 μm, for instance – the TFT needs to be scaled down along with the pixel size to be fitted inside of the pixel area. [3] This situation is even worse in active-matrix organic light emitting display (AM-OLED) because at least two TFTs must be squeezed in each pixel area. Furthermore, it is known that the miniaturization of TFTs improves the display performance by reducing the parasitic capacitance. Even though a-IGZO TFTs with an L smaller than 5 μm were previously reported by other groups [38], a systematic study of the scaling of a-IGZO TFTs has been lacking. Therefore, it is worthwhile to investigate the scaling characteristics of a-IGZO TFTs.

In this chapter, we present an in-depth study of the scaling dependency of coplanar homojunction a-IGZO TFTs. The coplanar homojunction a-IGZO TFTs investigated in this paper utilize a hydrogen doped a-IGZO source/drain (S/D) region, n+ a-IGZO, to achieve a low resistance S/D contacts. It was previously reported that this structure has the advantages of small S/D contact resistance and the capability of achieving a small L. [90] Therefore, the scaling characteristics for this type of a-IGZO TFT is worthwhile to be investigated.

3.1 Device Structure

A cross-sectional schematic of the fabricated TFT is shown in Fig. 3.1(a). The TFTs were fabricated on a Corning 1737 glass substrate. The Mo layer (100 nm) was sputtered as the gate electrode. Amorphous silicon oxide (a-SiO$_x$) layer (200 nm) was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 340 °C as a gate insulator. The a-IGZO film (30 nm) was D.C. sputtered and defined using a wet etching with diluted hydrochloric acid (HCl). The dilution ratio of deionized water (DI water) to HCl is 10 to 1. A 150 nm sputtered a-SiO$_x$ (has negligible hydrogen content) channel protection layer (CPL) was R.F. sputtered and patterned
by photolithography and dry etching. The CPL defines the TFTs length ($L$) and width ($W$). Figure 3.1(c) clearly shows the top view of the CPL taken under an optical microscope, showing the well-defined channel $W$ and $L$ of 60 and 10 $\mu$m, respectively.

A 300-nm-thick hydrogenated amorphous silicon nitride (a-SiN$_x$:H) and a 50-nm-thick a-SiO$_x$ are deposited sequentially in this order by PECVD at 250 °C as a protection layer on top of the CPL and a-IGZO (not covered with CPL) regions. During the a-SiN$_x$:H PECVD process, hydrogen present in the PECVD reactive chamber and/or in the hydrogen-rich a-SiN$_x$:H layer dopes the exposed a-IGZO region and increases its electrical conductivity. [89, 90] Effectively heavily hydrogen-doped a-IGZO regions outside of the CPL are formed to be used as source/drain (S/D) contact regions. Next, the source/drain contacts were formed in a top passivation layer by dry etching, followed by the sputtering of 100-nm-thick Mo source/drain electrodes defined by wet etching. In this structure, gate metal and S/D contact do not overlap (see the underlap in Figure 3.1(b)); although there is some overlap between the gate and the hydrogen doped S/D contact regions. There is separation of about 20 $\mu$m between CPL edge and S/D via edge. All lithographic patterning use S-1813 positive tone photoresist. Finally, the TFTs underwent a thermal annealing step at 270 °C in atmosphere at the end of the device process.

All measurements were carried out in a dark box using Agilent 4156C semiconductor parameter analyzer. The ideal metal-oxide-semiconductor field-effect transistors (MOSFET) drain current against gate-to-source voltage ($I_D$-$V_{GS}$) equation is used to extract the device parameters in the linear operation region: [75]

$$I = \mu_{eff}C_G\frac{W}{L}(V_{GS} - V_{TH})V_{DS} ,$$  

where $C_G$ is the capacitance per unit area of the gate insulator. The best linear fit
Figure 3.1: Schematic cross-sectional structure (a) and top view (b) of the coplanar homojunction a-IGZO TFT, and its macroscopic images. The detailed image for the channel area is shown in (c) and images including the probing pads in (d); CPL defines channel length (L) and width (W) of the TFT.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value (Lin.)</th>
<th>Value (Sat.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu_{\text{eff}}^\text{*}$ (cm$^2$/V·sec)</td>
<td>13.14</td>
<td>14.36</td>
</tr>
<tr>
<td>$V_{TH}^\text{*}$ (V)</td>
<td>0.74</td>
<td>0.30</td>
</tr>
<tr>
<td>S (mV/dec.)</td>
<td>124.34</td>
<td>104.45</td>
</tr>
<tr>
<td>$I_{OFF}$ (A)</td>
<td>$&lt; 10^{-13}$</td>
<td>$&lt; 10^{-13}$</td>
</tr>
<tr>
<td>ON/OFF ratio **</td>
<td>$\sim 10^7$</td>
<td>$\sim 10^9$</td>
</tr>
</tbody>
</table>

Table 3.1: Electrical properties of coplanar homojunction a-IGZO TFT with W/L = 60/10 \( \mu \)m, *extracted by 10% – 90% linear fitting method, **ON/OFF ratio is the drain current ratio between ON and OFF states

of $I_D$-$V_{GS}$ curves between 10% and 90% of maximum $I_D$ is used for $\mu_{\text{eff}}$ and $V_{TH}$ extraction. The $V_{TH}$ is the threshold voltage, and $V_{DS}$ and $V_{GS}$ are drain-to-source and gate-to-source voltage, respectively. For the saturation region ($V_{DS} = 15$ V), the following $I_D^{1/2}$-$V_{GS}$ equation is used: [75]

$$I_D^{1/2} = \sqrt{\frac{1}{2\mu_{\text{eff}}C_GW}} \frac{W}{L} (V_{GS} - V_{TH}) . \quad (3.2)$$

The sub-threshold swing ($S$) is defined as

$$S = \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1} \quad (3.3)$$

at around a maximum $\left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1}$ point. The leakage current, $I_{OFF}$, is defined as $I_D$ when $V_{GS} = -10$ V. The details for the parameter extraction are shown in Figure 3.2. The above equations are programmed in MATLAB software from MathWorks, Inc. and used for extracting all TFTs’ parameters. The TFTs over uniformly distributed six dies on the same substrate are selected as samples. The average and standard deviation values of the extracted parameters are used for the discussion later presented here.
Figure 3.2: Example of parameter extraction from the transfer characteristics of a-IGZO TFTs; (top) linear operation regime, $V_{DS} = 0.1$ V and (bottom) saturation operation regime, $V_{DS} = 15$ V
3.2 Channel Length Scaling

To study the channel length dependency of TFTs, the $I_D-V_{GS}$ and $I_D^{1/2}-V_{GS}$ curves with various $L_s$ (from 3 - 120 $\mu$m) are shown in Fig. 3.3. The $W$ is fixed at 60 $\mu$m. From Fig. 3.3, we conclude that all TFTs demonstrate normal TFT operation and that the TFT’s $I_D$ increases with decreasing channel length. This is in agreement with the ideal equations. (Equations 3.1 and 3.2)

Beside current-voltage curves, various TFT parameters should be investigated to understand the channel length dependency. The key parameters, such as $V_{TH}$, $\mu_{eff}$, $S$, and $I_{OFF}$, of TFTs are summarized as a function of $L$ in Fig. 3.3. With a shorter $L$, the $V_{TH}$ decreases and $S$ increases (i.e. becomes less steep). These changes become more severe when the TFT’s $L$ is smaller than 5 $\mu$m. Furthermore, it should be noted that small $L$ TFTs ($L < 5 \mu m$) work as a depletion mode ($V_{TH} < 0$ V) device while large $L$ TFTs ($L \geq 5 \mu m$) work as an enhancement mode ($V_{TH} > 0$ V) device in the
saturation region. The similar changes in $V_{TH}$ and $S$ have been easily observed in short channel MOSFETs which are not scaled properly. The off-current of a-IGZO TFTs does not change with a smaller channel length, while the off-current increases linearly in a-Si TFTs. [103] This is attributed to the low hole-density in a-IGZO material.

We describe the mobility variations associated with different channel lengths. The mobility of a-IGZO TFTs is almost constant in the linear region. However, the saturation region mobility increases in short channel length TFTs. The physical reason for the increase of mobility in the saturation region is that the high $V_{DS}$ bias increases the channel length modulation $\Delta L$, and decreases the effective channel length ($L_{eff} = L - \Delta L$). Moreover, the effect of $\Delta L$ becomes significant for small $L$ TFTs. This is equivalent to saying that the effective channel length is smaller than the physical channel length, the calculated $\mu_{eff}$ shows a higher value than what it actually should have. This difference gets larger as $L$ decreases. At this point, the mobility dependency of a-IGZO TFTs is worthwhile to compare with that of a-Si:H TFTs. Mobility degradation has been observed for short channel a-Si:H TFTs. This effect is due to the increased magnitude of the S/D resistance ($R_{SD}$) for short channel a-Si TFTs. [71, 51] However, in coplanar homojunction a-IGZO TFTs, such degradation due to high S/D resistance is not severe.

To confirm the low $R_{SD}$ in coplanar homojunction a-IGZO TFTs, $R_{SD}$ and channel length modulation ($\Delta L$) are extracted using the transmission line method (TLM) when $V_{GS} - V_{TH} \gg V_{DS}$. (also known as channel-resistance or current-voltage method) (Fig. 3.5): [16]

$$R_{TOT} = \frac{V_{DS}}{I_D} = 2 \times R_{SD} + \frac{L - 2 \times \Delta L}{\mu_{eff} C_G W (V_{GS} - V_{TH})} \quad (3.4)$$

In this measurement, a $V_{DS}$ of 0.1 V is used to satisfy the requirement of $V_{GS} - V_{TH}$
Figure 3.4: Channel length dependency of $V_{TH}$, $\mu_{eff}$, $S$, and $I_{OFF}$. The solid symbols and vertical bars represent the average and standard deviation and values, respectively. The samples over uniformly distributed six points on the 4-inch substrate are selected.
For our coplanar homojunction a-IGZO TFTs, the cross-point is located in the first (I) quadrant where $\Delta L$ is positive. This is equivalent to saying that $L_{\text{eff}} < L$, which implies that the S/D hydrogen doping region is horizontally diffused into the channel region and/or CPL patterns are shrunk from its drawn length during lithography or etching process. Similar observation was also made for self-aligned top gate TFTs, which have the shortened effective channel length. [76] The evaluated $2R_{SD}$ and $2\Delta L$ are 5.6 kΩ and 1.57 $\mu$m, respectively. These values are consistent with previously reported values. [90] Hence, we confirm that the a-IGZO region, not covered by CPL, makes good ohmic contacts with Mo and the width-normalized contact resistance ($R_{SD}W$) is 16.8 Ω·cm for $W = 60$ µm. It should be noticed that in the proposed TFT structure, the S/D contact area is composed of (i) overlap between gate metal and heavily doped a-IGZO region (n+ a-IGZO), (ii) n+ a-IGZO extension region to S/D metal and (iii) interface between S/D metal and n+ a-IGZO film.

To obtain further insights into short channel TFTs, we also investigated the
changes in the dimension-normalized transconductance \[ g^*_m = \partial (I_D \times L/W)/\partial V_{GS}, \]
\[ V_{DS} = 0.1 \text{ V}. \]\[ \]
The transconductance is plotted as a function of \( V_{GS} \) in Figure 3.6. For TFTs with \( L = 3 \text{ \( \mu \)m} \), the \( g^*_m \) reaches a maximum at the point of inflection of the \( I_D-V_{GS} \) curve, and then decreases. This decrease can be explained by two factors: degradation of \( \mu_{eff} \) as a function of an increasing transverse electric field across the gate dielectric and/or a voltage drop (\( V = I_D R_{SD} \)) associated with the large current. Since this phenomenon is not observed in large \( L \) TFTs, we conclude that this behavior is affected by the voltage drop. For TFTs with \( L = 5 \text{ \( \mu \)m} \), the \( g^*_m \) is rather constant under TFT's ON state.

In contrast, in TFTs with \( L = 120 \text{ \( \mu \)m} \), the \( g^*_m \) keeps increasing without having a maximum point, which has been commonly observed by many labs for a-IGZO TFTs. \[ 84, 41, 12 \] In other words, the \( \mu_{eff} \) of large \( L \) TFTs is a function of the gate voltage. \( ( \mu_{eff} = f(V_{GS}) ) \) Since the S/D region and a-IGZO channel have a same width in the coplanar homojunction TFTs, we do not expect any fringe field effect (also called edge effect), which can be observed in TFTs with long \( L \) or short \( W \). \[ 73 \]

In addition, we find that the maximum transition points of \( g^*_m \) are all similar (near 0 V). Therefore, the \( V_{TH} \) reduction in Fig. 3.4 is originated from the limitation of the linear extraction method of \( V_{TH} \). In short, the IR drop and charge trapping/scattering are the reasons of \( g^*_m \) degradation for short and long \( L \) TFTs, respectively. This implies that there is the optimum channel length, which has a minimized influence from those two effects, and the TFT will have the highest \( \mu_{eff} \) value at this point. From Fig. 3.4, we find that \( L = 5 \text{ \( \mu \)m} \) is the optimal point in the fabricated TFT structure.

When higher drain voltage (\( V_{DS} = 15 \text{ V} \)) is applied on TFTs, the \( V_{TH} \) reduction is more severe than at \( V_{DS} = 0.1 \text{ V} \). Furthermore, the degradation of \( S \) is clearly observed for TFTs with short \( L \). The \( V_{TH} \) reduction at higher \( V_{DS} \) and \( S \) degradation cannot be explained by the \( g^*_m \) discussed in the above paragraph. The similar
observations of $V_{TH}$ and $S$ changes, however, have been made in short channel MOS-FETs which are not scaled properly. From the scaling theory of transistors [19], it is known that the thickness of gate dielectric must decrease (equivalently increasing gate capacitance per unit area, $C_G$) with the same ratio of the channel length scaling, so maintaining the gate controllability even in shorten channel length. In addition, recent studies show that double-gate TFTs can have increased effective $C_G$ without decreasing the dielectric thickness. [6] The effect of different gate capacitance was studied by the device simulation using an ATLAS two-dimensional device simulator from Silvaco Inc. The previously reported simulation parameters for the density of states (DOS) are tabulated in Table 3.2 [35, 34]

Figure 3.7 shows the $V_{TH}$ and $S$ dependency of TFT having different gate capacitance: TFT-A and B correspond to TFTs with 200 and 100 nm thickness of the gate dielectric ($\text{SiO}_2$), respectively, and TFT-C represents the double gate TFT. The
<table>
<thead>
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<td>$N_{TA}$ (cm$^{-3}$eV$^{-1}$)</td>
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<td>(acceptor like) the density at the energy of the conduction band edge ($E_C$) of the exponential distribution</td>
</tr>
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<td>$W_{TA}$ (eV)</td>
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<td>(acceptor like) the characteristic decay energy for the exponential distribution</td>
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<tr>
<td>$N_{GA}$ (cm$^{-3}$eV$^{-1}$)</td>
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<td>(acceptor like) the density at the central energy ($E_0$) of the Gaussian distribution</td>
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<td>$W_{GA}$ (eV)</td>
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<td>The electron mobility</td>
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<td>$n_0$ (cm$^{-3}$)</td>
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<tr>
<td>$\Delta\phi$ (eV)</td>
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<td>The electron affinity of a-IGZO</td>
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</tbody>
</table>

Table 3.2: TCAD simulation parameters of a–IGZO TFTs used in this work

thickness for both the top and bottom gate dielectric is 200 nm for the double gate TFT. The channel length of TFTs is fixed at 2.5 μm. From the simulated I-V curves, the $V_{TH}$ and S are extracted in the same manner as described in § 3.1. As can be seen in Fig. 3.7, $V_{TH}$ reduction and S degradation is observed for TFT-A. However, the $V_{TH}$ reduction is improved for the structures of TFT-B and C. We expect that the increase of $C_G$ prevent the barrier lowering, which is induced by the drain voltage. The changes in S can be explained by the increased portion of source-to-drain electric field. From the two dimensional Poisson’s equation,

$$\frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} = \frac{\rho}{\varepsilon},$$

where $E_x$ and $E_y$ are the electric field in channel region in vertical (gate-to-channel) and horizontal (source-to-drain) directions, respectively. $\rho$ is the charge density per unit area at a given coordinate, x and y, and $\varepsilon$ is the permittivity at the given coordinate. For the same $C_G$, the first term ($\partial E_x/\partial x$) of Equation 3.5 is same for TFTs with different L, and its quantity is small for the sub-threshold regime. The second term ($\partial E_y/\partial y$) is negligible for long channel TFTs; in other words, $\rho$ is small and mostly controlled by the gate field. However, in case of TFTs with short L,
the second term becomes significant because $E_y$ is increasing as $L$ decreases. The increased quantity of the second term contributes a higher $\rho$, which is related to less steep $S$. However, the increased $C_G$ (or increased gate controllability) makes the first term dominant again and minimized the second term, which has $L$ dependency. This is consistent with the simulation results. Therefore, we conclude that specific TFT structure, such as double gate structure, or the thickness control of gate dielectric layer must be introduced for the short channel TFTs.

Lastly, the output characteristics of TFTs are shown in Fig. 3.8. It is observed that reducing the channel length below 5 $\mu$m results in an apparent deviation of the output characteristics from their solid saturation. In other words, the output resistance $r_{out}$ rapidly decreases for $L \leq 5$ $\mu$m. The $r_{out}$ is defined by the following
Figure 3.8: (dots) $I_D-V_{GS}$ and (solid line) output resistance are plotted for $L = 3, 7, 10, \text{ and } 120 \, \mu m$.

equation in the device saturation region:

$$r_{out} = \left( \frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \text{ (in saturation)} . \quad (3.6)$$

The channel length dependency of $r_{out}$ is summarized in Fig. 3.9 for a different $V_{GS}$. The $r_{out}$ is an important parameter for designing amplifiers. The common source amplifier or common drain amplifier can be used as a gate driver or amplifier in AM-FPDs or AM-FPIs. [3, 49, 40] Figure 3.10 shows the circuit schematics of common source and common drain N-TFT amplifiers. Since a-IGZO TFTs are unipolar in nature, an N-type circuitry is suitable rather than a complementary type

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circuitry. The voltage gain ($A_V$) of the common source and common drain amplifier are described as

$$A_v = -g_m\left(\frac{r_{out}}{R_D}\right) \quad \text{and} \quad A_v = \frac{g_m}{g_m + \frac{1}{\frac{r_{out}}{R_S}}} , \quad (3.7)$$

respectively. Therefore, a smaller $r_{out}$ results in a smaller gain. In the worst case, $r_{out} \ll R_D$ or $R_S$, the gain of the amplifier is mostly controlled by parasitic resistance ($r_{out}$) rather than design resistance ($R_D$ or $R_S$).

### 3.3 Channel Width Scaling

Similar analysis is done for various $W$s (from $10 \leq W \leq 120 \, \mu m$). $L$ is fixed at 10 $\mu m$. The device parameters of a-IGZO TFTs are shown in Figure 3.11. Although the channel width is varied from 1x to 12x channel width, we do not observe noticeable changes in the TFT parameters. Therefore, the channel width is not a serious design consideration because the channel width is larger than the length and is usually
Figure 3.10: Circuit schematics for n-TFT (a) common source amplifier and (b) common drain amplifier.

adapted in the circuit design.

3.4 Summary

In summary, we have studied the scaling characteristics of coplanar homojunction a-IGZO TFTs with 200 nm thick PECVD a-SiO$_x$. For long channel TFTs, the current reduced at low $V_{GS}$. In contrast, the current reduction occurs at high $V_{GS}$ for short channel TFTs. It would seem that the charge trapping/scattering and IR drop are at the origin of TFT channel length dependency. The 5 $\mu$m is the optimal L for TFT structure studied in this work without suffering these two degradations. However, this optimal channel length could be different for different TFT structures, such as different dielectric material/thickness and metal contacts. We did not observe any noticeable W dependency for coplanar a-IGZO TFTs.

In the case of TFTs with $L \leq 5 \mu$m, $r_{out}$ and S degrade rapidly and negative $V_{TH}$ is observed, and we conclude that is due to the weaken channel controllability of the gate for short channel TFTs. To achieve small L TFTs without any performance degradation, the gate dielectric should be scaled properly or a double-gate (DG) device structure must be used. From TCAD simulations, it is shown that either
Figure 3.11: Channel length dependency of $V_{TH}$, $\mu_{eff}$, $S$, and $I_{OFF}$. The solid symbols and vertical bars represent the average and standard deviation and values, respectively. The samples over uniformly distributed six points on the 4-inch substrate are selected.
the a-IGZO TFTs with the gate dielectric of 100-nm-thick SiO$_2$ or the double gate a-IGZO TFTs with the gate dielectric of 200-nm-thick SiO$_2$ is preferable for $L \leq 5 \mu$m. However, the reduced thickness of the gate dielectric layer may introduce other issues, such as the increased leakage current or reduced operating voltage. [39] In this regard, the DG coplanar homojunction a-IGZO TFTs are studied in the next chapter.
CHAPTER IV

Electrical Properties of Double Gate Coplanar
Homojunction a-IGZO Thin-Film Transistors

It is well known that the electrical performance of metal-oxide-semiconductor field
effect transistors (MOSFETs) is improved when a larger portion of the channel area is
controlled by additional gate electrodes. [7] When MOSFET’s channel length shrinks,
the controllability of the gate over the channel area reduces, while the source/drain’s
influence over the channel region increases. This leads to the short channel effects,
such as the threshold voltage roll-off, degraded subthreshold swing and drain-induced
barrier lowering (DIBL). To overcome the short channel effects, the double-gate or tri-
gate structure have been proposed in MOSFETs industry. The conceptual structures
of double- and tri-gate are shown in Figure 4.1. In such structures, the increased
number of gate electrodes are able to control the channel region (between the source
and drain) effectively, suppressing the short channel effects.

The double gate amorphous silicon (a-Si:H) TFTs have been proposed to provide
an effective light shielding to prevent the degradation of the TFT’s electrical proper-
ties under illumination. [96, 66] However, the presence of bias on the additional gate
electrode introduces unwanted increases in an a-Si:H TFT’s sub-threshold swing (S)
and off current (I_{OFF}). To address this problem, the additional gate electrode has
been grounded to provide stable circuit operation in a pixel array. [92, 49]
Several results on double gate (DG) a-IGZO TFTs have been recently reported. The device structures described in [99, 68, 17, 100] have defined the top gate but have left the bottom gate undefined, i.e. a common bottom gate is used in all reported TFTs. This type of device structure is simple to fabricate and somewhat useful for fundamental properties investigation. Since the undefined bottom gate (very often made of heavily doped silicon wafers) in such a device covers the whole substrate area, it is impossible to apply a different gate bias voltage on adjacent TFTs when large numbers of TFTs are fabricated on the same substrate. (Figure 4.2(a)) To investigate the usefulness of DG a-IGZO TFTs application to AM-FPD, a device structure with well-defined gates is required. This will allow us to apply independent gate bias voltage on both the top and bottom gate during the device properties investigation and/or pixel circuits operation. (Figure 4.2(b)) In [93], Son et al. described the DG a-IGZO TFT with defined top and bottom gate electrodes. In their structure, amorphous silicon nitride (a-SiNx) is used for the bottom gate insulator and amorphous silicon oxide (a-SiOx) is used for the top gate insulator. To take advantage of the DG structure, it is important to optimize the
Figure 4.2: Vertical cross-section of the double gate a-IGZO TFT with (a) common bottom gate and (b) defined bottom gate.

nature of the dielectrics and gate insulator/semiconductor interfaces used in such a device. Son et al. tried only to extend the gate dielectric technology developed for a-Si:H TFTs to a-IGZO TFTs without providing any proper device physics based justifications.

In this chapter, we describe the electrical characteristics of the DG coplanar homojunction a-IGZO TFT. In this structure, the top and bottom gate electrodes are defined, enabling the independent electrode biasing. The a-SiO\textsubscript{x} is used for both the top and bottom gate insulators, since it was shown in the past that the a-IGZO TFTs with a-SiO\textsubscript{x} gate dielectric exhibit better electrical performance and stability than the TFT with a-SiN\textsubscript{x}. [26] Herein we describe the superior electrical properties of DG coplanar homojunction a-IGZO TFT in the dark and under illumination conditions, in comparison to the single gate TFT. In addition, we discuss the device threshold voltage controllability through top gate voltage application. This method is referred to a dynamic control of the DG TFT threshold voltage.
4.1 Device Structure of Coplanar Homojunction Double-Gate (DG) a-IGZO TFTs

Figure 4.3 shows the schematic cross-section and microscopic top view of the DG coplanar homojunction a-IGZO TFT used in this work. The TFT’s bottom gate electrode was fabricated from sputtered molybdenum (100 nm) on a glass substrate. A PECVD was used to deposit the a-SiO$_x$ gate insulator (200 nm). The a-IGZO film (30 nm) was D.C. sputtered and defined using a wet etching with diluted hydrochloric acid. A 150 nm sputtered a-SiO$_x$ channel protection layer (CPL) was R.F. sputtered and patterned by photolithography and dry etching. The CPL defines the TFT width (W) and length (L). The CPL patterning was followed by a PECVD passivation of 300 nm thick a-SiN$_x$:H and 50 nm thick a-SiO$_x$ at the substrate temperature of 250 °C. Next the S/D contact vias were formed on top passivation layer by dry etching, followed by the sputtering and patterning of 100 nm-thick Mo source/drain electrodes. At the same time the Mo top gate is formed. A sufficient overlap (OV = 5 µm in Figure 4.3) between top and bottom gate electrodes is used in the TFT layout to avoid misalignment of the two gates during TFT fabrication. The gate misalignment could degrade on-current and sub-threshold slope due to reduced gate controllability. [106] However, too large overlap could increase the parasitic capacitance, which will worsen the TFT dynamic performance. Finally, the TFTs underwent a thermal annealing step at 270 °C in atmosphere at the end of the device process. The proposed circuit symbol of DG a-IGZO TFTs is proposed in Figure 4.4. The device structure except the Mo top gate is identical with the single-gate structure used in Chapter III. More experimental details about the TFT process can be found in § 3.1.

All the TFTs’ electrical transfer characteristics were measured using an Agilent 4156C with the source acting as the ground and a gate-to-source voltage ($V_{GS}$) sweeping from -10 to 15 V and from 15 to -10 V at 0.2 V intervals. The reverse direction
Figure 4.3: Schematic cross-sectional structure (a) and top view (b) of the double-gate (DG) coplanar homojunction a-IGZO TFT, and its macroscopic images. The detailed image for the channel area is shown in (c) and images including the probing pads in (d); CPL defines channel length (L) and width (W) of the TFT.
sweeping of $V_{GS}$ is used to check for device hysteresis. For the dynamic control of a threshold voltage ($V_{TH}$), we applied $V_{GS}$ on a top gate electrode ranging from -4 to 4 V at 2 V intervals during the transfer characteristics measurements.

Finally, we expose the top surface of TFTs (with and without gate electrode present) to Mercury-Xeon (Oriel 6291) arc lamp through a microscope via a fiber optic (with 10 mW/cm$^2$ of illumination). [24] The wavelength ($\lambda$) of the illuminated light has the spectral range from 200 to 2400 nm.

4.2 Experimental Results

4.2.1 Electrical Characteristics

Figure 4.5 and 4.6 show the transfer and output characteristics of the DG a-IGZO TFT with three different gate bias conditions. Figure 4.5(a) and (b) are measured by applying gate voltage only on top gate (TG) or bottom gate (BG), respectively, while the other gate is grounded. In Figure 4.5(c), identical gate voltage is applied and swept on both top and bottom gate electrodes at the same time. We call this device configuration: synchronized bias or double gate (DG) bias condition. In all three gate bias conditions, TFT demonstrates normal TFT operation. The Figure 4.6(b) shows details of the output curves for a small drain-to-source voltage ($V_{DS}$) region, $0 \leq$
\[ V_{DS} \leq 1 \text{ V}; \text{ no current crowding is found near the origin. Hence, it can be concluded from this data that the Mo/a-IGZO source/drain contact is ohmic in nature.} \] [47]

The electron affinity of Mo and undoped a-IGZO is 4.3 - 4.7 eV and 4.16 - 4.3 eV, respectively [23, 88]; hence expected Schottky barrier height for such contact is less than 0.4 eV.

To extract device parameters, such as field-effect mobility (\( \mu_{\text{eff}} \)) and threshold voltage (\( V_{TH} \)), the standard MOSFET drain current equation is used in the linear regime of the device operation. [22]

\[ I = \mu_{\text{eff}} C_G \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \quad (4.1) \]

where \( W \) and \( L \) are the channel width and length of the TFT, respectively. \( C_G \) is a gate insulator capacitance per unit area. Since measured transfer curves have very linear behavior, the linear fitting method based on 10% to 90% of maximum \( I_D \) is used. An example of the TFT parameter extraction is provided in § 3.1.

The gate capacitances of top gate (\( C_{TI} \)) and bottom gate (\( C_{BI} \)) insulator can be calculated using the thickness (\( t_{TI} \) or \( t_{BI} \)) and dielectric constant (\( \varepsilon_{TI} \) or \( \varepsilon_{BI} \)) of the top and bottom gate insulators, respectively.

\[ C_{TI} = \frac{\varepsilon_{TI}}{t_{TI}} \quad \text{and} \quad C_{BI} = \frac{\varepsilon_{BI}}{t_{BI}} \quad (4.2) \]

The gate capacitance of double gate (\( C_{DI} \)) cannot be simply defined. The gate voltages applied on top and bottom gate electrodes form channels on top and bottom sides of the a-IGZO thin film (Figure 4.7). Since these channels are connected together at source and drain electrodes, we consider the a-IGZO film as a single metal plate connecting top and bottom gate insulators in parallel. Hence the effective gate
Figure 4.5: Transfer characteristics of DG coplanar homojunction a-IGZO TFTs for three different bias conditions: (a) top gate, (b) bottom gate, and (c) double gate biasing.
Figure 4.6: Output characteristics of DG coplanar homojunction a-IGZO TFTs (a) for different bias conditions and (b) details shown for the $0 \leq V_{DS} \leq 1$ V
Figure 4.7: Gate capacitance diagram for the DG configuration and its equivalent diagram.

The capacitance of DG configuration is

\[ C_{DI} = C_{TI} + C_{BI} \]  

(4.3)

The values of \( C_{TI} \), \( C_{BI} \) and \( C_{DI} \) are given in Table 4.1. The \( \varepsilon \) values for a-SiO\(_x\) and a-SiN\(_x\) are 3\( \cdot \varepsilon_0 \) and 7\( \cdot \varepsilon_0 \), respectively. The thickness of bottom silicon oxide is 200 nm; the top gate insulator has a tri-layer structure: a-SiO\(_x\)/a-SiN\(_x\)/a-SiO\(_x\). The thickness of tri-layer is 150/300/50 nm, respectively. The capacitance of the tri-layer is calculated using three serially connected capacitors. The sub-threshold slope (S) can be extracted from the linear portion of the transfer characteristics, using following equation:

\[ S = \left( \frac{\partial \log I_D}{\partial V_{GS}} \right)^{-1} \]  

(4.4)

The drain current range from one order below to one order above around a maximum \((\partial \log I_D/\partial V_{GS})\) point is used to calculate S. For conventional single gate TFTs, S is
approximately given by:

\[ S \approx \ln 10 \cdot \frac{k_B T}{q} \cdot \left( 1 + \frac{C_{TSS} + C_{BSS}}{C_G} \right) \]  (4.5)

where \( k_B \) is the Boltzmann constant, \( T \) is the temperature in Kelvin, \( q \) is the electron charge. The \( C_{BSS} \) is a capacitance of the bottom channel interface state per unit area and is defined by \( C_{BSS} \equiv q \cdot N_{BSS} \) where \( N_{BSS} \) is the density of interface trap states. \( C_{TSS} \) and \( N_{TSS} \) are the symbols for the top channel interface. The average interface trap density per unit area can be calculated by assuming \( N_{SS}=N_{TSS}=N_{BSS} \). Using \( S \) value for TG and BG configuration (286 and 153 mV/decade), the calculated \( N_{SS} \) is about 6.0 and \( 5.4\times10^{10} \) eV\(^{-1}\) cm\(^{-2} \), respectively. Moreover, the \( S \) for DG configuration can be written as equation 4.6 because of \( C_G = C_{DI} = C_{BI} + C_{TI} \) (Equation 4.3) [2]

\[ S \approx \ln 10 \cdot \frac{k_B T}{q} \cdot \left( 1 + \frac{C_{TSS} + C_{BSS}}{C_{TI} + C_{BI}} \right) \]  (4.6)

From the measured value (\( S = 100 \) mV/decade), the Equation 4.6 leads to \( N_{SS} = 5.8\times10^{10} \) eV\(^{-1}\) cm\(^{-2} \) for DG configuration. We can conclude that a steeper \( S \) for DG configuration is due to the increased gate capacitance.

For more quantitative comparison, extracted TFT parameters for BG, TG and DG device configurations are tabulated in Table 4.1. From this data, we can conclude that the DG a-IGZO TFT with the double gate configuration has the best electrical performance in terms of smaller \( S \) and higher \( I_{ON} \). Since for DG bias condition, two channels, one on top and one bottom side of a-IGZO layer, are formed at the same time, steeper \( S \) and higher \( I_{ON} \) through increase of effective channel thickness are expected. [107] The \( I_{OFF} \) is independent of gate bias conditions and is below 0.1 pA. This low \( I_{OFF} \) is due to a very low hole density present in a-IGZO channel. We did not observe any p-channel behavior up to -20 V. The threshold voltage of the DG a-IGZO TFT is slightly higher in comparison to TG and BG TFTs.
Table 4.1: Extracted device parameters for double gate coplanar homojunction a-IGZO TFTs

In Figure 4.8 we show a comparison between the sum of on-current for TG and BG bias conditions, $I_{ON-TG}+I_{ON-BG}$, and on-current for DG bias condition, $I_{ON-DG}$. In linear region ($V_{DS} = 0.1$ V), the sum of $I_{ON-TG}$ and $I_{ON-BG}$ is comparable to $I_{ON-DG}$. However, in saturation region ($V_{DS} = 15$ V), $I_{ON-DG}$ is about 85% higher than the sum of $I_{ON-TG}$ and $I_{ON-BG}$. In addition, Figure 4.6(a) shows that the insufficient channel saturation takes place for DG bias condition in comparison to either TG or BG biasing condition. We speculated that, in linear region, top and bottom channels are formed separately at top and bottom interfaces, and two channels contribute to the increase of $I_{ON}$. In saturation region, interactions between top and bottom gate voltages confines the channels more strongly. Consequently, the DG TFT requires a higher $V_{DS}$ to reach drain saturation in comparison to TG or BG TFTs. Hence the on-current keeps increasing proportionally to $V_{DS}$ until the saturation will take place. Therefore the extended linear region causes an 85% increase in on-current of DG TFT.
4.2.2 Dynamic Control of the Threshold Voltage

In double gate TFT structure, it is expected that the threshold voltage can be affected by top gate bias condition. Therefore it is important to study the impact of the top gate voltage \( V_{TG} \) on DG a-IGZO TFT electrical properties. Figure 4.9 shows device transfer characteristics when different \( V_{TG} \) is applied. We observed parallel shift of the transfer curves in response to \( V_{TG} \) without any changes of \( S \) and \( I_{OFF} \).

To explain this observation, it is worth to compare our results with these obtained for DG a-Si TFTs. In the a-Si TFT, the magnitude of \( V_{TH} \) shift is smaller and \( S \) and \( I_{OFF} \) is decreasing for \( V_{TG} < 0 \) V. \([46, 99]\) We speculate that the absence of the hole accumulation layer in a-IGZO is responsible for this difference.

Non-existence of holes will make the formation of p-channel a-IGZO transistors impossible \([83, 58]\), and will allow for the electric field generated by \( V_{TG} \) to penetrate into the bottom channel. Consequently a mutual interaction between the electric field generated by \( V_{TG} \) and \( V_{BG} \) is possible. Hence \( V_{TG} \) will be responsible for a
Figure 4.9: Transfer characteristics of coplanar homojunction DG a-IGZO TFTs for various $V_{TG}$ values.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure4.9.png}
\end{figure}
band bending at bottom interface resulting in inhibition of the electron accumulation. Therefore, $V_{TH}$ is expected to shift to more positive direction in response to $V_{TG} < 0$ V. If the hole accumulation would be possible in a-IGZO, it will take place at the top interface and will block the electric filed generated by $V_{TG}$. Consequently, the bottom channel will be hardly affected by $V_{TG}$. [69] Moreover, the hole accumulation layer could change $I_{OFF}$ and $S$ by generating unwanted leakage current. There is no such change on $I_{OFF}$ and $S$ in DG a-IGZO TFTs.

For $V_{TG} > 0$ V, an electron accumulation layer can be formed at the top interface. However, once $V_{BG}$ sweeps from negative voltage, negative $V_{BG}$ is able to penetrate into the bottom interface and the interaction between $V_{TG}$ and $V_{BG}$ is allowed again (as was observed for $V_{TG} < 0$ V). The negative $V_{BG}$ depletes the electron accumulation layer at the top interface. As larger positive $V_{TG}$ is applied, more negative $V_{BG}$ is required to deplete the electron accumulation at the top interface. Therefore, $V_{TH}$ is expected to shift to more negative direction in response to $V_{TG} > 0$ V. Since the $V_{TH}$ shift is resulting from the interaction between the electric fields penetrating through the a-IGZO and the gate insulators, the magnitude of $V_{TH}$ shift should be related to the thickness of the a-IGZO and gate insulator.

Figure 4.10 summarizes the dependence between $V_{TG}$ and $V_{TH}$, extracted from Figure 4.9. As shown in the figure, the relationship between $V_{TG}$ and $V_{TH}$ is linear. Similar observation was already made for a-IGZO DG TFTs. [68, 99] The relationship between $V_{TH}$ and $V_{TG}$ can be derived from the simplified device structure shown in figure 4.11.

Applying Gauss’ law to the surface 1(Ι) yields

$$\varepsilon_{IGZO}E_2 - \varepsilon_{BI}E_1 = Q_{tB} + Q_{ch} \quad (4.7)$$
Figure 4.10: The $V_{TH}$ and S variation with the top gate voltages ($V_{TG}$) of coplanar homojunction DG a-IGZO TFTs. The symbols represent the measured data and the solid line represents the calculated curve using Equation 4.19.
Figure 4.11: Simplified cross-sectional view of the DG TFT and space charge distribution.
and from the surface 2 and 3(2 and 3), we can derive following equations:

\[ \varepsilon_{TI} \vec{E}_4 - \varepsilon_{IGZO} \vec{E}_3 = Q_{tT} \quad \text{and} \]
\[ \varepsilon_{TI} \vec{E}_4 - \varepsilon_{IGZO} \vec{E}_2 = Q_{tT}, \]

where \( Q_{tB} \) and \( Q_{tT} \) are trap density including surface bulk states at the bottom and top a-IGZO surface, respectively. \( Q_{ch} \) is mobile charge density of the a-IGZO film. \( \vec{E}_1, \vec{E}_2, \vec{E}_3 \) and \( \vec{E}_4 \) are electric field at the drawn points in Figure 4.11. As a next step, the difference of electric potential is expressed as the integral of electric field, \( E(y) = -dV(y)/dy. \)

\[
\int_{y_0}^{y} E(y) \, dy = V(y_0) - V(y) \tag{4.10}
\]

Integration of equation 4.10 from \( y_0 = -t_{BI} \) to \( y = 0 \) gives,

\[ t_{BI} \vec{E}_1 = (V_{BG} - \Delta \varphi_B) - V_{ch} \tag{4.11} \]

where \( V_{ch} \) is the voltage at the channel surface \( (y=0) \). Since \( C_{BI} = \varepsilon_{BI}/t_{BI} \), we can write,

\[ \frac{\varepsilon_{BI} \vec{E}_1}{C_{BI}} = (V_{BG} - \Delta \varphi_B) - V_{ch} \tag{4.12} \]

Also, the integration of Equation 4.10 from \( y_0 = 0 \) to \( y = t_{IGZO} + t_{TI} \) gives,

\[ \frac{\varepsilon_{TI} \vec{E}_4}{C_{TI}} + \frac{\varepsilon_{IGZO} \vec{E}_3}{C_{IGZO}} = V_{ch} - (V_{TG} - \Delta \varphi_T) \tag{4.13} \]

Here, \( \Delta \varphi_B \) and \( \Delta \varphi_T \) represent the work function difference of the a-IGZO film at top and bottom gate electrodes. If we substitute Equation 4.7, 4.8, 4.9 and 4.12 into 4.13,
When the TFT is turned on, we can let $Q_{ch} = 0$ and $V_{BG} = V_{TH}$. Therefore,

$$0 = -C_{BI}V_{TH} - \left( \frac{C_{TI}C_{IGZO}}{C_{TI} + C_{IGZO}} \right) V_{TG} - Q_{tB} - \frac{C_{IGZO}}{C_{TI} + C_{IGZO}}Q_{tT}$$

$$+C_{BI} \left( 1 - \frac{C_{TI}C_{IGZO}}{C_{BI}(C_{TI} + C_{IGZO})} \right) V_{ch} + C_{BI}\Delta Q_{B} + \frac{C_{TI}C_{IGZO}}{C_{TI} + C_{IGZO}}\Delta Q_{T}$$

(4.15)

Moving $-C_{BI}V_{TH}$ term to left side and dividing both sides by $C_{BI}$ and defining $\beta$ as

$$\beta = -\frac{C_{TI}C_{IGZO}}{C_{BI}(C_{TI} + C_{IGZO})}$$

(4.16)

then we obtain:

$$V_{TH} = -\beta V_{TG} - \frac{Q_{tB}}{C_{BI}} - \frac{\beta}{C_{TI}}Q_{tT} + (1 - \beta)V_{ch} + \Delta Q_{B} + \beta Q_{T}$$

(4.17)

The $\beta$ is the function of the capacitances, which is related to the a-IGZO and the gate insulator thickness. From the Table 4.1, the $C_{TI}$ and $C_{BI}$ are 9.5 nF/cm$^2$ and 17.7 nF/cm$^2$, respectively. And $C_{IGZO}$ is 295 nF/cm$^2$ for $\varepsilon_{IGZO} = 10\cdot\varepsilon_{0}$ and $t = 30$ nm, then we can calculate $\beta = -0.52$ for the device used in this work.

For more simplification, we define $V_{TH}(0)$ as

$$V_{TH}(0) = -\frac{Q_{tB}}{C_{BI}} - \frac{\beta}{C_{TI}}Q_{tT} + (1 - \beta)V_{ch} + \Delta Q_{B} + \beta Q_{T}$$

(4.18)

$V_{TH}(0)$ is considered as the TFT's threshold voltage for top gate voltage, $V_{TG} = 0$ V. Finally, the relation between $V_{TH}$ and $V_{TG}$ can be expressed in a simple linear
form,

\[ V_{TH} = V_{TH}(0) + \beta V_{TG} \] (4.19)

The solid line in Figure 4.10 represents Equation 4.19 for \( \beta = -0.52 \). The derived equation is in a good agreement with the experimental data. Similar observation has been made for DG a-IGZO TFT with \( L = 5 \mu m \). This good agreement between calculated and experimental data supports the proposed model shown in Figure 4.11.

According to Equation 4.16 \( \beta \) is dependent on the thickness of top/bottom gate insulators, and a-IGZO layer. If a-IGZO channel layer is very thin, Equation 4.16 is simplified to \( \beta = -C_{TI}/C_{BI} \) and \( \beta = -0.53 \) for the values of \( C_{TI} = 9.5 \) and \( C_{BI} = 17.7 \) nF/cm\(^2\), which is very close to experimental value of -0.52 obtained from Figure 4.10. Since a-IGZO film used in this work is very thin, therefore the shift of \( V_{TH} \) is expected to be mostly influenced by \( C_{TI} \) and \( C_{BI} \).

4.2.3 Illumination Stability

We also investigated the DG a-IGZO TFT characteristics under illumination. Figure 4.12(a) shows the a-IGZO transfer characteristic without a top gate, under illumination. We have shown in [24] that the illumination with \( \lambda < \lambda_{TH} \) generates the electron-hole pairs (EHP) that will affect the TFT electrical characteristics; the \( \lambda_{TH} \) is the threshold wavelength which is closely related to the optical bandgap. No major changes occur in the wavelength range, \( \lambda > 420 \text{ nm} \) (2.95 eV). A significant changes in \( I_{OFF} \), S and \( V_{TH} \) take place only for \( \lambda < 420 \text{ nm} \). We confirmed that, under illumination of the a-IGZO TFT without top gate, hysteresis, \( I_{OFF} \) and S are increasing; hysteresis (0V to 2 V), \( I_{OFF} \) (0.1 to 10 pA), and S (153 to 388 mV/decade). These results are in agreement with [24]. From this result it is clear that although a-IGZO is transparent in a given photon energy range, for its application to AM-FPD
the light shield is needed to prevent $I_{OFF}$ increase. In the DG TFT structure, top gate metal electrode, as shown in Figure 4.3, can serve as light shield and protect the channel area from the illumination. Figure 4.12(b) shows the DG TFT transfer characteristics in the dark and under broadband illumination. We note that the two curves are identical. Therefore, the introduction of the top gate effectively protects the channel area from illumination and maximizes the light stability of the double-gate a-IGZO TFTs. At the same time, the DG TFT provides superior electrical characteristics in comparison to the single gate TFT.

4.3 Summary

The double-gate coplanar homojunction a-IGZO TFT is fabricated and its electrical characteristics and stability are described. We confirmed that this device has a good ohmic S/D contact. Under DG bias conditions, the top and bottom gate electrodes form two conduction channel layers at the top and bottom interfaces. A high $I_{ON}$ and a steep $S$ are achieved without increasing $I_{OFF}$ and $\Delta V_{TH}$. We showed that the lack of the hole accumulation in the a-IGZO TFT is the basis for the linear dependence of the threshold voltage on top gate voltages, while other device parameters are unchanged. This linear relationship is verified by Gauss’s law using the proposed simplified DG TFT model. Additionally, the top gate is an excellent light shield, which ensures TFT stability under light illumination. The observed electrical properties and stability make the DG a-IGZO TFT a strong candidate for AM-FPI’s pixel circuits. To provide better understanding of the electrical characteristics of DG a-IGZO TFTs, the analytic model of the TFTs are investigated, based on device Physics in the next chapter.
Figure 4.12: Transfer characteristic of coplanar homojunction a-IGZO TFTs without and with top gate structure in the dark and under illumination.
CHAPTER V

Modeling of Current-Voltage Characteristics for Double-Gate a-IGZO TFTs

5.1 Introduction

As shown in Chapter IV, a double-gate (DG) a-IGZO TFT structure has both a bottom gate (BG) and a top gate (TG) electrode that can be biased differently. (see Figure 4.3) Moreover, it is found that DG a-IGZO TFT has a higher stability under light illumination. To understand the operation principle of DG a-IGZO TFT, a mathematical analysis based on device physics is needed. Abe et al. described the mathematical analysis of DG a-IGZO TFT for the condition when either TG or BG is biased at constant value, and concluded that the DG TFTs with a constant BG or TG bias have electrical performance comparable (or even worse in the saturation region) to the conventional single gate TFT. [2] To take advantage of the DG TFT, both TG and BG should be tied together (synchronized).

In this chapter, we present an extension of Abe’s previous work. We analyze the DG a-IGZO TFT’s characteristics for with synchronized bias condition. In the latter part of this chapter, the TFT parameters of the DG a-IGZO coplanar homojunction TFT, which are extracted in § 4.2.1, compared with the developed analytical model. In addition, a new pixel circuit based on a synchronized DG a-IGZO TFT is
introduced for active-matrix liquid crystal display (AM-LCD) application.

5.2 Double-Gate TFT Modeling

Figure 5.1 and 5.2 show a schematic cross section of a DG TFT with a channel length $L$ and channel thickness $t_s$. The mathematical derivation is based on the following assumptions: (i) (Constant Mobility) The mobility is constant during TFT operations; (ii) (Gradual Channel) The voltages vary gradually along the channel from the source to the drain; (iii) (Two-Dimension) The TFT is two-dimensional; The TFT does not have the channel width (W) dependency; (iv) (DC Measurements) The bias voltage or current can be changed only after the TFT is under equilibrium states; and (v) (Long Channel) There is no interaction between the source/drain electrodes. The above assumptions might not be always adequate for the field-effect transistors (FETs), such as a-IGZO TFTs. However, we believe that the model using these assumptions can successfully explain the electrical characteristics of conventional TFT, such as field-effect mobility ($\mu_{\text{eff}}$), threshold voltage ($V_{TH}$), and sub-threshold swing (S). The similar assumptions are also employed in the SPICE Level 1 model for the MOSFETs. [77]

5.2.1 On-Operation Region

From Figure 5.1, the surface charge density, $Q_S$, can be written as the sum of bottom and top surface charge density, $Q_{BS}$ and $Q_{TS}$, respectively.

$$ Q_S = Q_{BS} + Q_{TS} \quad (5.1) $$

From the parallel plate capacitor model;

$$ Q = C \cdot V \quad (5.2) $$
Therefore, the $Q_S$ can be written as

$$Q_S = C_{BI} (V_{BG} - V_{BTH0} - V(y)) + C_{TI} (V_{TG} - V_{TH0} - V(y)) \quad (5.3)$$

where $C_{BI}$ is the capacitances per unit area of the bottom insulator. $V(y)$ is the channel voltage at the position $y$, in the horizontal direction along the channel length from the source to drain. $V_{BTH0}$ and $V_{BG}$ correspond to the threshold voltages of the single gate TFT only with the bottom electrode and the bias voltage applied on the bottom gate electrode, respectively. The subscript $T$ is associated with the top electrode.

The voltage drop, $dV$, between $y$ to $y+dy$ is given by [4]

$$dV = \frac{I_D dy}{W \mu_{eff}|Q_S|} \quad (5.4)$$

By integrating Equation 5.4 for entire channel length (from $y = 0$ to $L$), $I_D = \int_{y=0}^{L} W \mu_{eff} dV$, the drain current ($I_D$) of the DG TFT is given by Equation 5.5.
Figure 5.2: Schematic cross-section of a DG TFT and space charge distribution (x-direction)
Over the length of the channel, the channel voltage varies gradually from the source voltage \( V(0) = 0 \) to the drain voltage \( V(L) = V_D \).

\[
I_D = \frac{W}{L} \frac{\mu_{eff}}{C_{BI} + C_{TI}} \left\{ C_{BI}(V_{BG} - V_{BTH0}) + C_{TI}(V_{TG} - V_{TTH0}) \right\}^2 \\
\times \left[ 1 - \left\{ 1 - \frac{(C_{BI} + C_{TI})V_D}{C_{BI}(V_{BG} - V_{BTH0}) + C_{TI}(V_{TG} - V_{TTH0})} \right\}^2 \right]
\]

(5.5)

Since \( V_G = V_{BG} = V_{TG} \), in synchronized DG operation, Equation 5.5 is simplified into Equation 5.6.

\[
I_D = \frac{W}{L} \frac{\mu_{eff}}{C_{BI} + C_{TI}} \left\{ (C_{BI} + C_{TI})V_G - (C_{BI}V_{BTH0} + C_{TI}V_{TTH0}) \right\}^2 \\
\times \left[ 1 - \left\{ 1 - \frac{(C_{BI} + C_{TI})V_D}{(C_{BI} + C_{TI})V_G - (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})} \right\}^2 \right]
\]

(5.6)

For more simplification, we define the double-gate capacitances per unit area \( C_{DI} \) and the threshold voltage of synchronized DG operation \( V_{DTH} \)

\[
C_{DI} = C_{BI} + C_{TI} \quad (5.7)
\]

\[
V_{DTH} = \frac{C_{BI}V_{BTH0} + C_{TI}V_{TTH0}}{C_{DI}} \quad (5.8)
\]

Then, \( I_D \) can be expressed as

\[
I_D = \frac{W}{L} \mu_{eff} C_{DI} \left( V_G - V_{DTH} \right)^2 \left[ \frac{2V_D}{V_G - V_{DTH}} - \left( \frac{V_D}{V_G - V_{DTH}} \right)^2 \right]
\]

(5.9)

If the TFT is under linear operation region, \( V_D \ll V_G - V_{DTH} \), the second order term for \( V_D \) is canceled out. Then, Equation 5.9 can be approximated into

\[
I_D = \frac{W}{L} \mu_{eff} C_{DI} (V_G - V_{DTH}) V_D
\]

(5.10)

Moreover, when \( V_D \) is larger than \( V_{SAT} (= V_G - V_{DTH}) \), which is derived from
Equation 5.1 with the channel pinch-off condition \((Q_S = 0\) and \(V(L) = V_D\)), the current does not increase further (saturated). Hence, the saturation current is

\[
I_D = \frac{W}{2L} \mu_{eff} C_{DI}(V_G - V_{DTH})^2
\]  

(5.11)

These equations are very similar to equations used for description of TFT electrical properties. \[95\]

### 5.2.2 Sub-threshold Region

The current in the sub-threshold region of FETs is described by Equation 5.12 \[101, 75\]

\[
I_D \sim \frac{W}{L} \mu_{eff} \left(\frac{k_B T}{q}\right)^2 \left(1 - e^{-\frac{qV_D}{k_B T}}\right) t_{eff} e^{\frac{q\phi}{k_B T}}
\]  

(5.12)

The effective channel thickness \((t_{eff})\) is defined as a distance from the channel/insulator interface. \(k_B\) and \(T\) are the Boltzmann’s constant and the absolute temperature, respectively. And, \(\phi\) is the potential voltage at the channel surface. From the definition of sub-threshold slope \((S)\),

\[
S \equiv \left(\frac{\partial \log_{10} I_D}{\partial V_G}\right)^{-1}
\]  

(5.13)

Therefore, it is necessary to find the relation between a surface potential \((\phi)\) and gate voltage \((V_G)\) in sub-threshold region. In Figure 5.2, applying Gauss’s laws to the surface 1 (①) and 2 (②) yields the following equations:

\[
\varepsilon_S \vec{E}_2 = C_{BI} V_{BOX} - qN_{BSS} \phi_B
\]  

(5.14)

\[
-\varepsilon_S \vec{E}_2 = C_{TI} V_{TOX} - qN_{TSS} \phi_T
\]  

(5.15)

81
where $N_{BSS}$ is bottom surface trap states in the unit of eV$^{-1}$cm$^{-2}$ and $\phi_B$ is the potential voltage at the bottom channel/insulator interface. $V_{BOX}$ is the potential difference across the bottom gate insulator. $V_{BOX} = (V_{BG} - V_{BFB}) - \phi_B$ where $V_{BFB}$ is the flat band voltage of the bottom gate electrode. Again, the subscript T is associated with the top electrode. $\varepsilon_s$ is the permittivity of a-IGZO semiconductor.

From Equation 5.14 and 5.15, we can derive the equation of a charge balance; $\sum Q = 0$.

$$C_{BI}V_{BOX} - qN_{BSS}\phi_B + C_{TI}V_{TOX} - qN_{TSS}\phi_T = 0$$

(5.16)

In synchronized bias condition, $V_G = V_{TG} = V_{BG}$ and we assume that same gate material is used for the top and bottom gate electrodes ($V_{FB} = V_{TFB} = V_{BFB}$). Thus, Equation 5.16 is rewritten as

$$(C_{BI} + qN_{BSS})\phi_B + (C_{TI} + qN_{TSS})\phi_T = (C_{BI} + C_{TI})(V_G - V_{FB})$$

(5.17)

As a next step, the difference of electric potential is expressed as the integral of the electric field $E(y) = -d\phi_B(y) / dy$, thus

$$\phi_B - \phi_T = \vec{E}_2 t_s = -\frac{C_{TI}(V_G - V_{FB}) - (C_{TI} + qN_{TSS})\phi_T}{\varepsilon_s} t_s$$

(5.18)

By substituting Equation 5.17 into 5.18, two relations for $\phi_B$ and $\phi_T$ are given
where $C_{BSS} \equiv qN_{BSS}$ and $C_S \equiv \varepsilon_S / t_S$;

$$\phi_B \approx \left\{ 1 + \frac{C TI C_S}{C_BI(C_{TI} + C_S + C_{TSS})} \right\} V_G$$

and

$$\phi_T \approx \left\{ 1 + \frac{C_{TI}(C_{BI} + C_S + C_{BSS})}{C_BIC_S} \right\} V_G$$

If the current mainly flows near the bottom interface, $I_D$ is given by

$$I_D \sim \frac{W}{\mu_{eff}} \left( \frac{k_B T}{q} \right)^2 \left( 1 - e^{-\frac{qV_D}{k_B T}} \right) t_{Beff} e^{\frac{q\phi_B}{k_B T}}$$

where $t_{Beff}$ is the effective channel thickness for the bottom channel. From the definition of $S$ (Equation 5.13) and Equation 5.21

$$S \equiv \left( \frac{\partial \log_{10} I_D}{\partial V_G} \right)^{-1} = \left( \frac{1}{I_D \ln 10} \frac{\partial I_D}{\partial \phi_B} \frac{\partial \phi_B}{\partial V_G} \right)^{-1}$$

$$\approx \left( \frac{I_D}{I_D \ln 10} \frac{q}{k_B T} \frac{\partial \phi_B}{\partial V_G} \right)^{-1} = \ln 10 \frac{k_B T}{q} \left( \frac{\partial \phi_B}{\partial V_G} \right)^{-1}$$

By substituting Equation 5.19 into 5.22, $S$ is obtained.

$$S \approx \ln 10 \frac{k_B T}{q} \frac{(C_{BI} + C_{BSS})(C_{TI} + C_S + C_{TSS}) + (C_{TI} + C_{TSS})C_S}{C_BI(C_{TI} + C_S + C_{TSS}) + C_{TI}C_S}$$
Then, if the $C_S$ is larger than other capacitances, $C_S \gg C_{TI}, C_{BI}, C_{TSS}$ and $C_{BSS}$

$$S \approx \ln 10 \frac{k_B T}{q} \frac{C_{DI} + C_{BSS} + C_{TSS}}{C_{DI}} = \ln 10 \frac{k_B T}{q} \left( 1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}} \right) \quad (5.24)$$

The a-IGZO TFT used in this work has $C_S=295$, $C_{TI}=9.5$, $C_{BI}=17.7$ and $C_{TSS}=C_{BSS}$ 9 nF/cm$^2$. From these values, we can conclude that the above assumption is reasonable.

Similarly, when $I_D$ mainly flows near the top interface, the current is given by

$$I_D \approx \frac{W}{L} \mu_{eff} \left( \frac{k_B T}{q} \right)^2 \left( 1 - e^{-\frac{qV_D}{k_B T}} \right) t_{eff} e^{\frac{q\phi_T}{k_B T}} \quad (5.25)$$

and

$$S \approx \ln 10 \frac{k_B T}{q} \left( \frac{\partial \phi_T}{\partial V_G} \right)^{-1} \approx \ln 10 \frac{k_B T}{q} \left( 1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}} \right) \quad (5.26)$$

Therefore, the $S$ of DG TFTs, when $V_G=V_{BG}=V_{TG}$, can be expressed by

$$S \approx S_0 \left( 1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}} \right) \quad (5.27)$$

The value of $S_0 = \ln 10 \cdot k_B T/q$ is around 60 mV at room temperature. If $S$ and $C_{DI}$ are known, the $N_{BSS}$ and $N_{TSS}$ values can be calculated from Equation 5.27.

### 5.3 Comparison with a Conventional TFT Model

The equations developed in the previous sections are summarized in Table 5.1. The equations for a conventional single gate TFT and the DG a-IGZO TFT with a single gate being biased (i.e., either the TG or BG constant bias is applied) are also tabulated in Table 5.1. The equation for DG a-IGZO TFTs with BG bias ($V_G = V_{BG}, V_{TG} = 0$) is adapted from Abe’s work [2] and the equations for TG bias condition
(\(V_G = V_{TG}, V_{BG} = 0\)) can be derived by replacing the subscripts B and T, which stand for bottom and top gate, respectively. Table 5.1 shows that the DG a-IGZO TFTs with the BG or TG bias have a reduced saturation mobility \(\mu_{eff}(Sat.)\) and reduced saturation voltage \(V_{SAT}\) and increased \(S\). The amount of these changes is related to the ratio between \(C_{BI}\) and \(C_{TI}\). In contrast, the DG TFTs with synchronized bias (\(V_G = V_{BG} = V_{TG}\)) does not suffer from any degradation. Moreover, it is worthy to note that the synchronized DG TFTs can be considered simply as conventional TFTs with a gate capacitance of \(C_{DI} = C_{BI} + C_{TI}\) and a threshold voltage of \(V_{DTH} = (C_{BI}V_{BTH} + C_{TI}V_{TTH}) / C_{DI}\).

To confirm the validity of the developed models, the TFT parameters of the coplanar homojunction DG a-IGZO TFT, which are extracted in § 4.2.1, compared with the developed analytical model. The TFT details about its fabrication, device structure and measurements can be found in § 4.1. The bottom gate insulator is a 200 nm thickness of silicon oxide and the top gate insulator is a stacked tri-insulator, structure of a-SiO\(_x\)/a-SiN\(_x\)/a-SiO\(_x\), with a thickness of each layer of 150/300/50 nm, respectively. The capacitance of the tri-layer structure is calculated using three serially connected capacitors. The values of \(C_{BI}\), \(C_{TI}\), and \(C_S\) are 17.7, 9.7 and \(295\) nF/cm\(^2\). The permittivity of \(4\cdot\varepsilon_0\), \(7\cdot\varepsilon_0\) and \(10\cdot\varepsilon_0\) are used for a-SiO\(_x\), a-SiN\(_x\), and a-IGZO, respectively, where \(\varepsilon_0\) is the permittivity of the air. The channel width/length (W/L) is \(60 / 10 \mu\text{m}\).

In the extraction of TFT parameters, \(S\) was defined as \(S = \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1}\) around a maximum \(\left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1}\) point. Since the constant mobility model is assumed in this work, \(V_{TH}\) and \(\mu_{eff}\) in the linear region were derived from a linear fitting to the \(I_D-V_G\) curve at \(V_D = 0.1\) V, and those in the saturation region were derived from a linear fitting to \(\sqrt{I_D-V_G}\) at \(V_D = 15\) V by using the equations shown in Table 5.1. The transfer characteristics (\(I_D-V_G\)) are measured in Figure 5.3 for three different bias conditions and the extracted device parameters from Figure 5.3 are summarized in
<table>
<thead>
<tr>
<th></th>
<th>Conventional Single Gate</th>
<th>Double Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>TG: $V_G = V_{TG}, V_{BG} = 0$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BG: $V_G = V_{BG}, V_{TG} = 0$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SG: $V_G = V_{BG} = V_{TG}$</td>
</tr>
<tr>
<td>$I_D$ (Lin.)</td>
<td>$\frac{W}{L}\mu_{eff} C_G (V_G - V_{TH}) V_D$</td>
<td>$\frac{W}{L}\mu_{eff} C_{TI} (V_{TG} - V_{TTH}) V_D$</td>
</tr>
<tr>
<td>$I_D$ (Sat.)</td>
<td>$\frac{W}{2L}\mu_{eff} C_G (V_G - V_{TH})^2$</td>
<td>$\frac{W}{2L}\mu_{eff} C_{TI} (V_{TG} - V_{TTH})^2$</td>
</tr>
<tr>
<td></td>
<td>$S_0 \left(1 + \frac{C_{BSS} + C_{TSS}}{C_G}\right)$</td>
<td>$S_0 \left(1 + \frac{C_{TI} + C_{BSS} + C_{TSS}}{C_{TI}}\right)$</td>
</tr>
<tr>
<td>Saturation Voltage ($V_{SAT}$)</td>
<td>$V_G - V_{TH}$</td>
<td>$\frac{C_{TI}}{C_{DI}} (V_{TG} - V_{TTH})$</td>
</tr>
<tr>
<td></td>
<td>$\mu_{eff}$</td>
<td>$\mu_{eff}$</td>
</tr>
<tr>
<td></td>
<td>$\mu_{eff}$</td>
<td>$\mu_{eff}$</td>
</tr>
<tr>
<td>Gate Capacitance</td>
<td>$C_G$</td>
<td>$C_{TI}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_{BI}$</td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>$V_{TH}$</td>
<td>$V_{TH} = V_{TH0} + \frac{C_{BI}}{C_{TI}} V_{BTH0}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{BTH} = V_{BTH0} + \frac{C_{TI}}{C_{BI}} V_{TH0}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DTH} = \frac{C_{BI} V_{BTH0} + C_{TI} V_{TH0}}{C_{DI}}$</td>
</tr>
</tbody>
</table>

Table 5.1: Summary of different TFT Models, developed in this work
Figure 5.3: Transfer characteristics of the DG a-IGZO TFTs for top-gate (TG), bottom-gate (BG) and synchronized-gate (SG) bias conditions.

Table 5.2. As shown in Table 5.1, the mobility in the linear region and the $\mu_{\text{eff-SAT}}$ with the SG bias should be identical for all three gate bias conditions while the extracted $\mu_{\text{eff-SAT}}$ for TG or BG being biased are proportionally decreased by the ratio of $C_{TI}/C_{DI}$ or $C_{BI}/C_{DI}$. From the $\mu_{\text{eff-SAT}}$ models and the capacitance in Table 5.1,

$$\mu_{\text{eff-SAT}}(TG) = \frac{C_{TI}}{C_{DI}} \mu_{\text{eff}} = 0.35 \mu_{\text{eff}}$$

$$\mu_{\text{eff-SAT}}(BG) = \frac{C_{BI}}{C_{DI}} \mu_{\text{eff}} = 0.65 \mu_{\text{eff}}$$ (5.28)

From Table 5.2, we confirmed that the measured $\mu_{\text{eff-SAT}}$ for TG or BG bias ($\mu_{\text{eff-SAT}}(TG) = 3.98$, $\mu_{\text{eff-SAT}}(BG) = 9.11$, and $\mu_{\text{eff}} = 12 \sim 13 \text{ cm}^2/\text{V}\cdot\text{sec}$) are decreased from $\mu_{\text{eff}}$ in linear region and that the amounts of the decrease are con-
consistent with Equation 5.28. In contrast, in the case of SG bias, the mobility in the saturation region is comparable to the values in the linear region. Therefore, the observed mobility degradations for TG and BG bias are mainly due to the applied constant bias on one gate electrode and their difference disappears when both top and bottom gate electrodes are connected together.

Furthermore, from the S value in Table 5.2, we can calculate the interface trap densities (N_{SS}), which are supposed not to be different for all three bias conditions discussed in this paper. It is assumed that the BG and TG interface trap capacitances are the same (C_{BSS} = C_{TSS}) for convenience; N_{SS} = N_{TSS} = N_{BSS}. The calculated N_{SS} is similar for three bias conditions (not supposed to be different), which supports the validity of our analytic models. The previously reported \( \mu_{eff} \) and N_{SS} for conventional single gate coplanar homojunction a-IGZO TFTs (12.4 cm\(^2\)/V⋅sec and 7.3 \times 10^{10} \text{eV}^{-1}\text{cm}^{-2}, \) respectively) [89] were also comparable with our results. The device structure and fabrication details of the single gate coplanar homojunction a-IGZO TFTs are identical to the TFTs analyzed in this paper.

Lastly, to verify \( V_{D-SAT} \) models, the \( I_D-V_D \) characteristics are shown in Figure 5.4. If we assume that the threshold voltages for different gate bias conditions are similar, \( V_{D-SAT} \) is mainly related to C_{TI} or C_{BI}. Therefore, it is clear that the

Table 5.2: Extracted parameters for DG a-IGZO TFT under different bias conditions

<table>
<thead>
<tr>
<th>( V_{TH} ) [V]</th>
<th>TG ( V_G=V_{TG}, V_{BG}=0 )</th>
<th>BG ( V_G=V_{BG}, V_{TG}=0 )</th>
<th>SG (Sync) ( V_G=V_{TG}=V_{BG} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \mu_{eff} ) [cm(^2)/V⋅sec.]</td>
<td>11.52</td>
<td>3.98</td>
<td>12.82</td>
</tr>
<tr>
<td>S [V/dec.]</td>
<td>0.290</td>
<td>0.153</td>
<td>0.100</td>
</tr>
<tr>
<td>( C_G ) [nF/cm(^2)]</td>
<td>C_{TI}=9.5</td>
<td>C_{BI}=17.7</td>
<td>C_{DI}=27.2</td>
</tr>
<tr>
<td>N_{SS} [eV^{-1}cm^{-2}]</td>
<td>6.0 \times 10^{10}</td>
<td>5.4 \times 10^{10}</td>
<td>5.8 \times 10^{10}</td>
</tr>
</tbody>
</table>
Figure 5.4: Output characteristics of the DG a-IGZO TFTs for TG, BG and SG bias conditions.

TFT saturation will take place earlier in the following sequence: the TG, BG and SG, respectively, in agreement with Figure 5.4. Hence, the proposed analytic models are in agreement with the measurement results.

5.4 Application to High Resolution AM-LCDs

Table 5.1 implies that DG a-IGZO TFTs with the synchronized bias condition can produce larger current and steeper sub-threshold swing without increasing the channel width/length ratio (W/L) and/or the quality of the a-IGZO film. In other words, the same amount of drain current and sharp ON-OFF switching can be achieved with even smaller W/L TFTs. This observation can be advantageous in a pixel circuit designs for future active-matrix liquid crystal displays (AM-LCDs). As shown in § 1.1, the future technology trends of AM-LCDs are higher resolution (i.e. ultra high definition; 7680 \times 4320 pixels), higher pixel density (over 300 pixels per inch), and refresh rate
(240 Hz or higher). To follow these trends, smaller and faster TFTs are required [8]. In this regard, the a-IGZO TFTs are considered as a leading approach for achieving high pixel density on large panel size because of its high mobility. [9] In addition, we believe that synchronized DG a-IGZO TFTs are more suitable than regular a-IGZO TFTs in terms of larger current in same W/L and steeper sub-threshold swing.

Figure 5.5 shows an example of the proposed pixel circuit with a synchronized DG TFT for AM-LCD. In this pixel, the switching transistor ($T_{SW}$) is in the shape of an inverted staggered structure with an additional gate electrode, the top gate (TG). Moreover, TG and BG are fully overlapped and tied together (synchronized) through the sync via. By introducing an additional gate electrode, the parasitic capacitance between the two gates and the source/drain overlap could be increased. However, DG TFTs can have a smaller W for the same amount of drain current. Therefore, a decrease in device W can possibly cancel out a possible increase in device capacitance.

Figure 5.5: Proposed AM-LCD pixel circuit (right top), layout (left) and vertical cross-section (right bottom) based on synchronized DG a-IGZO TFT.
5.5 Summary

The simple analytic models of DG a-IGZO TFTs with synchronized bias conditions are developed and compared with TG or BG only bias devices. From this work, we can conclude that the DG TFTs under the bias condition of $V_G = V_{BG} = V_{TG}$ can simply be considered as conventional TFTs with a gate capacitance of

$$C_{DI} = C_{BI} + C_{TI} \quad (5.29)$$

and a threshold voltage of

$$V_{DTH} = \frac{C_{BI} V_{BTH0} + C_{TI} V_{TTH0}}{C_{DI}}. \quad (5.30)$$

Furthermore, it is shown that the DG TFTs with TG or BG bias suffer from mobility and S degradations and have the decreased saturation voltage, $V_{SAT}$. Therefore, two gate electrodes need to be tied together to avoid such degradations. The developed models are compared with the measurement results of the DG coplanar homojunction a-IGZO TFTs. The congruence between the models and measurements suggest that the developed models can successfully explain the electrical behaviors of the DG a-IGZO TFTs. We believe that DG TFTs are a better choice than single gate TFTs for future AM-LCDs and suggest a new pixel circuit based on synchronized DG a-IGZO TFT. To ensure a robust product based on DG a-IGZO TFTs, it is essential to evaluate their electrical stability, which is investigated in the next chapter.
CHAPTER VI

Bias Instability of Double-Gate a-IGZO TFTs

There is considerable interest in adapting a-IGZO TFTs in such applications as AM-LCDs and AM-OLEDs. This is because of its higher mobility in amorphous phase and suitability for low-temperature fabrication. In addition, we have shown throughout previous chapters, that the double gate (DG) a-IGZO TFTs have better electrical and optical characteristics, compared with the single gate a-IGZO TFTs. However, to be adapted in the industry, its long term reliability must be ensured. Therefore, it is essential to evaluate the electrical stability of DG a-IGZO TFTs.

Although numerous results have been reported about the stability of single gate a-IGZO TFTs [22, 43, 98, 64, 30, 97], its origin and physical mechanism are still unclear. Furthermore, there are only very few results related to the stability of DG a-IGZO TFTs. Abe et al. reported the DG a-IGZO TFTs’ instability when either top or bottom gate electrode is grounded. [2] However, in Chapter V, we concluded that that DG a-IGZO TFTs with the synchronized bias condition can produce larger current and steeper sub-threshold swing without increasing the quality of the a-IGZO material. In the synchronized condition, top and bottom gate electrodes are connected together, so same voltage is applied on both gate electrodes.

Son et al. reported the characteristics of the negative bias-temperature-stress (NBTS) for the synchronized DG a-IGZO TFTs. According to [93], the threshold
voltage shifts ($\Delta V_{TH}$) of the synchronized DG a-IGZO TFTs are decreased from that of the single gate a-IGZO TFTs and it is concluded that the origin of this enhancement is due to the electric field compensation during the synchronized NBTS. The field compensation refers to the very small or no electric field on TFT’s channel area, because an identical voltages are applied on the top and bottom gate electrodes during the stress. The reduced $\Delta V_{TH}$ under the positive BTS (PBTS) are also reported. However, the authors did not explain why this enhancement occurs.

In AM-LCDs, the TFT functions as a simple switch with a low duty cycle (0.1 %), thus the TFT is under OFF state for the 99.9 % of the operation time. In other words, the gate voltage of TFTs is lower than the voltages on the source and drain electrodes for most of the time. Therefore, the TFTs’ characteristics under NBTS is important in AM-LCDs. However, a threshold voltage shifts of a few volts can be tolerated in AM-LCD’s operation because the TFTs work as a simple switching element.

In contrast, in the pixel operation of AM-OLEDs, the driving TFT ($T_{DR}$) is turned ON for most of time to supply the current on OLEDs. In other words, the positive bias are always applied on the gate of $T_{DR}$. Moreover, a small $V_{TH}$ variation on $T_{DR}$ directly changes the driving current, resulting in pixel’s brightness change. For example, Chen et al. reported that a variation in $V_{TH}$ of only 0.2V changes the OLED’s brightness up to 10 %. [13] The PBTS instability, therefore, is critical in the application of AM-OLEDs. In this chapter, we study the PBTS and NBTS characteristics of DG a-IGZO TFTs with the synchronized bias condition. Furthermore, the instability results are compared with those of regular single gate TFTs.

6.1 Device Structure

The coplanar homojunction a-IGZO TFTs are fabricated on a glass substrate (TFT grade glass). The fabricated TFTs in this chapter is structured similarly (but slightly
different) with the TFTs in Chapter III and IV. The detail process steps are described in the following. First of all, 100-nm-thick Mo gate electrode is sputtered as a bottom gate electrode and patterned by a dry etching using CF$_4$ and O$_2$ gases. The mixture ratio of CF$_4$ to O$_2$ is 70 to 30 sccm. The chamber pressure ($P_{chamber}$) and the etching time ($t_{etch}$) are 10 Pascal and 102 seconds, respectively. Next, the PECVD is used for depositing the 200-nm-thick Silicon oxide (SiO$_x$) as a bottom gate insulator. ($C_{BG} = 17.7$ nF/cm$^2$) The substrate temperature ($T_S$) is set to 400 °C during the deposition and 24 sccm of Silane (SiH$_4$) and 600 sccm of Nitrous oxide (N$_2$O) are used. The RF power, $P_{chamber}$ and deposition time ($t_{dep}$) are 360 W, 173 Pa and 112 seconds, respectively. Thus, the deposition rate of the bottom gate dielectric is 17.85 Å/sec.

The 40-nm-thick a-IGZO semiconductor film is D.C. deposited by Oxygen (O$_2$) reactive sputtering. ($O_2$/Ar = 16.3/108.7 sccm) The sputtering power of 300 W, $P_{chamber}$ of 0.5 Pa, $T_S$ of 120 °C are used. The $t_{dep}$ is 79 seconds. The distance between the sputtering target and the substrate is about 110 mm. The a-IGZO layer is patterned by a diluted Hydrochloric acid (HCl) for 30 seconds. The dilution ratio is 10 : 1. (D.I. water : HCl)

The channel protection layer (CPL; 300 nm) is deposited with a PECVD SiO$_x$. In order to minimize Hydrogen diffusion into a-IGZO channel, $T_S$ is set down to 285 °C and SiH$_4$ ratio over N$_2$O is reduced to 4 %. (16/400 sccm) The $t_{dep}$ is 233 seconds, resulting in the deposition rate of 12.87 Å/sec. The RF power and $P_{chamber}$ are same as those of the bottom gate dielectric. The CPL is dry etched with a gas mixture of CF$_4$/O$_2$ (= 38/2 sccm), RF power = 100 W, $P_{chamber}$ = 4 Pascal and $t_{etch}$ = 436 seconds. The CPL defines a channel width and length of the fabricated TFTs.

Next, the CPL etching is followed by the first passivation layer (1$^{st}$ PL) of Silicon oxynitride (SiO$_x$N$_y$). Silicon oxynitride is known as a good moisture barrier. [109] The thickness of 1$^{st}$ PL is 300 nm. The PECVD deposition is used with $T_S = 250$ °C, $P_{chamber} = 150$ Pascal, RF power = 360 W and $t_{dep} = 124$ sec. The gas mixture ratio
Figure 6.1: The vertical structure of (a) single and (b) double gate a-IGZO TFTs used for a stability study. The only difference between (a) and (b) is the existence of the top gate electrode. The calculated $C_{BG}$ and $C_{TG}$ are 17.7 and 7 nF/cm$^2$, respectively. The channel width and length are 60 and 10 µm, respectively.

is SiH$_4$:N$_2$O:N$_2$ = 24:30:570 sccm. Hence, the deposited film is Nitrogen-rich SiO$_x$N$_y$. The patterning of the passivation layer was done by dry etching. (CF$_4$/O$_2$ = 38/2 sccm, 100 W, 4 Pascal, 160 seconds) Next, the S/D contact vias and the top-gate electrode were sputtered over the 1$^{st}$ PL. (100-nm-thick Mo) The single gate TFTs, used for the comparison, do not have the top-gate patterns in this step. The patterning of S/D contact was done by wet etching with Mo enchant. (H$_3$PO$_4$:HNO$_3$:H$_2$O = 200:20:15, 20 seconds)

Additional passivation (2$^{nd}$ PL) is deposited by 300-nm-thick SiO$_x$N$_y$, same condition above, and patterned by wet etching (a low ammonium fluoride liquid (LAL 1000), for 90 seconds) to open contact area. The 2$^{nd}$ PL will allow an additional deposition of a transparent electrode (such as ITO), which can be used as a pixel electrode of AM-LCDs or AM-OLEDs. Finally, a thermal annealing was done using the rapid thermal annealing (RTA) in nitrogen atmosphere, 300 ºC for 30 minutes. The vertical structures of the single and double gate TFTs are shown in Figure 6.1. In this structure, the top gate insulator is the serialized capacitors of CPL (300-nm-SiO$_x$) and 1$^{st}$ PL (300-nm-SiO$_x$N$_y$). ($C_{TG} = 7$nF/cm$^2$)
6.2 Bias-Temperature Stress Study

6.2.1 Positive Bias-Temperature Stress (PBTS)

PBTS measurements are performed by using HP 4156A semiconductor parameter analyzer in the dark-shielding box with the ambient air. The device temperature was regulated by a heated chuck, which is controlled by Signatone temperature controller with a precision of 0.1 °C. Before the measurement, the TFTs are placed on the heated chuck which is set at the desired measurement temperature (T_{STR} = 80 °C) until the temperature controller displays the stable values. This is for ensuring the thermal equilibrium.

We selected a set of the single and double gate TFTs for the comparison. The single and double gate TFTs in the set are closely located within 500 µm. The four sets over the 4-inch glass substrate are measured to consider the process variation. For the single gate TFTs, the stress voltage of V_{STR} = +15 V are applied on the gate. Similarly, for the DG TFTs, the same V_{STR} are subjected both on top and bottom gate electrodes, thus two gates are synchronized. During PBTS, the drain voltage is set to ground (V_{DS} = 0 V). These stress conditions are illustrated in Figure 6.2.

The TFTs are stressed for a total stress time of 10,000 seconds (2.78 hours). At certain times (in log scale; 100, 300, 600, 1000, 3000, 6000 and 10000 seconds),
the stress are interrupted and the transfer characteristics are measured by sweeping the gate voltage \( V_{GS} \). To minimize a stress relaxation during these measurements, the measurement must be conducted as fast as possible. In this experiment, the measurement time of the transfer curves are below 10 seconds. This value is 10 times faster than the smallest stress interval, 100 sec. To minimized the measurement time, the measurement accuracy is set to lower value and the range of voltage sweep are reduced, \( V_{GS} \) from -5 to +10 V. We believe that the reduced range is still enough for observing the important TFT parameter, such as \( V_{TH} \). Furthermore, we confirmed that the measured results for the range of \( I_D > 10^{-11} \)A are not different with the data taken with a higher accuracy setup. (but slow, longer than 50 seconds) All measured TFTs have the channel width and length of 60 and 10 \( \mu m \), respectively.

Figure 6.3 shows the transfer characteristics of the TFTs, measured during the stress at 80 °C (\( V_{DS} = 0.1 \) V). For the TFTs set of (a) and (b), which are the worst results among four sets, the variation of the transfer curves are reduced on the DG TFT(b) in comparison to the single gate TFT(a). For (c)-(d) set, which is the best results among four sets, even though the magnitude of the variation is different with (a)-(b) set, DG TFT(d) also shows a smaller shift than the single TFT(c). Since similar results are repeated on the rest two sets, the observed results are confident and outside of the measurement error. We will use the TFTs set of (a)-(b) for the further discussion. The threshold voltages \( V_{TH} \) are extracted from the transfer curves in Figure 6.3, and the evolution of \( V_{TH} \), \( \Delta V_{TH} \), are summarized in Figure 6.5(a) with solid symbols. The best linear fitting method for 10 to 90 % of the maximum drain current is used for the \( V_{TH} \) extraction. The details about this extraction method can be found at § 3.1. From Figure 6.3, it is concluded that the DG a-IGZO TFTs have less changes on the transfer curve (\( \Delta V_{TH} = -0.3 \) V) than the single gate TFTs (\( \Delta V_{TH} = -1.2 \) V) under PBTS.

It is worth to note the transfer curves are shifting into the negative direction
Figure 6.3: The transfer characteristics of PBTS on single and double gate a-IGZO TFTs. The DG a-IGZO TFTs, (b) and (d), shows the smaller $\Delta V_{TH}$ than the single gate a-IGZO TFTs, (a) and (c). The compared single and double gate TFTs, (a)-(b) or (c)-(d), are closely located within 500 $\mu$m. However the distance between (a)-(b) and (c)-(d) sets are about 4 cm. ($T_{STR} = 80 ^\circ C$)
both for the single and double gate TFTs. The $\Delta V_{TH}$ is negative while changes on subthreshold swing and field effect mobility are negligible. The positive $\Delta V_{TH}$ shift is typically observed during PBTS [43, 98, 64], and this shift is often explained by the electron trapping into the gate dielectric and/or near the insulator/semiconductor interface. However, the observed negative $\Delta V_{TH}$ cannot be explained by this electron trapping mechanism. Moreover, Figure 6.5(a) shows that the $V_{TH}$ initially shifted first to positive direction before shifting to negative direction. We are speculating that the reason of the negative shift is originated from (i) the hole injection from the gate electrode into the gate dielectric or (ii) the positive ion, which is generated from the neutralization of the positively charged cations around Fermi level, trapping into the a-IGZO/insulator interface. However, this phenomena has to be carefully revisited in another study. Meanwhile we are focusing on understanding of the reduced amount of $\Delta V_{TH}$ in DG a-IGZO TFTs.

There are two possible scenarios to explain the improved electrical instability in the synchronized DG a-IGZO TFTs; (a) increased effective gate capacitance, $C_G$, during the measurement of the transfer curves and (b) the vertical electric-field compensation. First, we expect that any changes on $C_G$ is expected to affect TFT’s transfer characteristics. If we assume that the bias stress induces the trapped charges near the interface of gate insulator and semiconductor, the threshold voltage after the BTS ($V_{TH}$) and its shift ($\Delta V_{TH}$) can be described by the following equations,

$$V_{TH} = V_{TH}(0) - \frac{Q}{C_G} \quad \text{and}$$

$$\Delta V_{TH} = V_{TH} - V_{TH}(0) = -\frac{Q}{C_G}, \quad (6.1)$$

where $V_{TH}(0)$ is the threshold voltage of the fresh (unstressed) TFT. $Q$ and $C_G$ is the trapped charge amount near the interface and the gate capacitance of TFTs, respectively. From this equation, $\Delta V_{TH}$ is decreasing for the same $Q$ when $C_G$ has
an increased value.

We confirmed in Chapter V that the effective $C_G$ of DG a-IGZO TFTs with sync. bias ($V_{BG} = V_{TG}$) is equivalent to the sum of $C_{BG}$ and $C_{TG}$ (and $C_{DI} = C_{BG} + C_{TG} = 24.7 \text{ nF/cm}^2$). In contrast, the effective $C_G$ of single gate TFT is $C_{BG} = 17.7 \text{ nF/cm}^2$. Furthermore, the DG a-IGZO TFT measured with BG sweep ($V_{TG} = 0V$) or TG sweep ($V_{BG} = 0V$) has an effective $C_G$ equal to $C_{BG} = 17.7 \text{ nF/cm}^2$ or $C_{TG} = 7 \text{ nF/cm}^2$, respectively. According to Equation 6.1 and from discussion above, $\Delta V_{TH}$ will have the lowest value for DG TFT with the sync. bias measurement.

To verify the effective $C_G$ impact on TFT measurements, we measure $\Delta V_{TH}$ of DG TFTs under different measurement conditions. While $V_{STR}$ is applied to the both gate electrodes of DG TFT during the stress time (i.e. sync. stress), we measure DG TFT’s transfer curves under three different gate bias conditions (Figure 6.4): (a) sync. sweep, (b) BG sweep with $V_{TG} = 0V$ and (c) TG sweep with $V_{BG} = 0V$. The $\Delta V_{TH}$ extracted from Figure 6.4 are summarized in Figure 6.5(a). The DG TFT with sync. sweep has a smaller $\Delta V_{TH}$ than the single gate TFT. However, the DG TFT with the TG sweep shows a larger $\Delta V_{TH}$ than the single gate TFT. It is evident that $\Delta V_{TH}$ is differently measured for different sweep methods even for the identically stressed TFT.

From experimental data shown in Figure 6.5, we can observe that the magnitude of $\Delta V_{TH}$ is the largest for TG sweep and is the lowest for sync. sweep. The effective $C_G$ is the largest for sync. sweep and the lowest for TG sweep. This is in agreement with Equation 6.1. To avoid the $C_G$ impact during transfer curve measurements, the $\Delta V_{TH}$ are normalized by multiplying $C_G$ ($C_G \cdot \Delta V_{TH}$). This is shown in Figure 6.5(b). It is clear that all three $\Delta V_{TH}$ curves are merged in to the one curve after the normalization. Using the normalized $\Delta V_{TH}$, we are now able to clearly establish the difference between single and double gate TFTs. In conclusion, we strongly suggest that $C_G \cdot \Delta V_{TH}$ is better indicator than $\Delta V_{TH}$ when TFTs with different structures
Figure 6.4: The evolution of DG a-IGZO TFTs’ transfer characteristics under the synchronized PBTS. $V_{STR}$ of $+15$ V is applied on top and bottom gates; (a) synchronized sweep (b) bottom gate sweep and (c) top gate sweep. Although the same stress condition is used, the amounts of $\Delta V_{TH}$ are different with the readout (gate sweep) method.
Figure 6.5: The evolution of $\Delta V_{TH}$ under PBTS. (a) $\Delta V_{TH}$ vs. stress time (b) gate capacitance normalized $\Delta V_{TH}$, $C_G \cdot \Delta V_{TH}$. With the normalized $\Delta V_{TH}$, the difference of the single and double gate a-IGZO TFTs is clearly distinguished.
and under different measurement conditions are compared. Even after eliminating
the $C_G$ effects by the normalization, DG a-IGZO TFTs still shows smaller values
than the single gate TFTs, Figure 6.5(b).

Next we consider the vertical field compensation. The vertical field compensation
in DG TFTs refers that the vertical electric field induced by top and bottom gates
cancel out each other, resulting in the zero or very small field being present in a-IGZO
film. This would result a barely stressed a-IGZO film. However, in PBTS, the positive
voltages on the gate electrodes will induce the accumulated electron layer in the a-
IGZO channel. Furthermore, the electron accumulation layer is laterally connecting
source and drain, which is biased at 0 V. As a result, the mutual interaction between
top and bottom electric field is not allowed, and the vertical field compensation cannot
take place during PBTS. Therefore, we are expecting the enhanced PBTS instability
is due to a different origin.

6.2.2 Negative Bias-Temperature Stress (NBTS)

The similar experiment is conducted for NBTS. The measurement setups are same
as PBTS, but the stress voltage of $V_{STR} = -15$ V is used. The measured transfer
curves are shown in Figure 6.6 and the evolution of $V_{TH}$ during the stress time are
summarized in Figure 6.7. For the single gate TFT, $\Delta V_{TH}$ is around -0.2 V and $\Delta V_{TH}$
smaller than -0.1 V are observed for DG a-IGZO TFTs. The $\Delta V_{TH}$ in DG TFTs is
smaller than the measurement accuracy (0.1 V), so these data are not adequate for
the quantitative analysis and the normalization was not performed. However, it is
clearly shown that DG a-IGZO TFTs have the smaller $\Delta V_{TH}$ than the single gate
TFTs during NBTS. These observations are in a good agreement with the previously
reported results. [93]

In contrast to PBTS, the enhanced instability in DG a-IGZO TFTs could be
explained by the vertical field compensation. [93, 6] For a negative gate bias, the
Figure 6.6: The transfer characteristics during NBTS on single and double gate a-IGZO TFTs
hole accumulation layer is hardly formed in a-IGZO channel area. In other words, a-IGZO channel area is isolated from source and drain electrodes with high electrical resistance (lateral isolation). Consequently, a vertical interaction between the top and bottom gate electric field is allowed, resulting in the vertical field compensation in DG a-IGZO TFTs during NBTS. In other words, this will be equivalent to nearly zero stress across the a-IGZO channel region. Therefore, in agreement with experimental results, we observe very low $\Delta V_{TH}$ in DG TFTs during NBTS.

6.3 Application of DG a-IGZO TFTs to High Resolution AM-OLEDs

The a-IGZO TFT is emerging today as a strong candidate for a pixel circuit in AM-OLEDs, because of its remarkable merits, such as high mobility, low off current, high electrical stability and low temperature fabrication requirements. Aside from
these advantages, DG a-IGZO TFTs show even higher on-current capability, a sharper sub-threshold swing, excellent controllability of the threshold voltage, good electrical stability and excellent light stability. These characteristics make DG a-IGZO TFTs a very attractive candidate for the AM-OLED.

The simple pixel circuit in AM-OLED includes at least two TFTs with one storage capacitor ($C_{ST}$). [10] In a traditional two-TFT pixel circuit (Figure 6.8(a)), when the switching TFT ($T_{SW}$) is turned on during the programming stage, the data signal voltage is stored at $C_{ST}$ through $T_{SW}$ generating the node voltage ($V_{ST}$) on $C_{ST}$. Once the programming stage is completed, $T_{SW}$ is turned off during the retention stage. $V_{ST}$ at the gate of the driving TFT ($T_{DR}$) maintains a constant current, which flows through $T_{DR}$.

For the AM-OLED pixel circuit, two properties are important: the programing speed and the retention period. The programing speed of the pixel circuit is the time required to charge $C_{ST}$ to the desired $V_{ST}$. A lengthy required time may result in insufficient charging of $C_{ST}$, thereby causing an error in the display gray scale. [63] To maximize charging performance, it is necessary for $T_{SW}$ to have a high $I_{ON}$ and a fast switching capability between on and off states. Since DG a-IGZO TFT has a high on-current and a small $S$, it is expected that $T_{SW}$ will have an enhanced pixel charging performance.

Secondly, the retention period is also critical for AM-OLEDs. The retention period is the time that $C_{ST}$ retains the electrical charges, and these charges stored in $C_{ST}$ can leak out through a leakage current of $T_{SW}$ during this stage. The $C_{ST}$ charge loss causes display gray scale distortion. To prevent such distortion, TFTs having a low leakage current are desired. It is clear from this study that a-IGZO has a smaller leakage current than a-Si:H or poly-Si TFTs, which are currently the most widely used AM-OLED pixel circuits. Moreover, this study has demonstrated that the leakage current of the DG a-IGZO TFT is constant under different bias conditions.
Figure 6.8: (a) Traditional AM-OLED pixel driving circuit and (b) proposed AM-OLED pixel circuit based on DG a-IGZO TFTs to be used as switching and driving transistors.

and even under BTS or light illumination (when the top gate is present). Therefore, overall, we can expect an excellent electrical performance of the DG a-IGZO TFT pixel circuit. Figure 6.8(b) shows an example of the AM-OLED pixel circuit based on DG a-IGZO TFTs. Unlike the case in normal TFT structure, the TFT's top and bottom gates are connected together in the proposed pixel circuit. For dynamic control of the TFT threshold voltage, the top gate should be biased separately, which requires an additional control line.

6.4 Summary

In this chapter the bias-temperature stability of the coplanar homojunction DG a-IGZO TFTs are investigated. The stress temperature is set to 80 °C and the stress time is 10,000 seconds. In PBTS with $V_{STR} = +15$ V, the $\Delta V_{TH}$ is reduced by one third of the single gate TFTs. (the best location: 0.4 → 0.1 V, the worst location: 1.2 → 0.4 V) Similar experiments are performed for NBTS with $V_{STR} = -15$ V. As well as in PBTS, the $\Delta V_{TH}$ of DG a-IGZO TFTs shows reduced values from that of the single
gate. (0.2 → < 0.1 V) From the results, we conclude that synchronized DG a-IGZO TFTs are more stable than the single gate a-IGZO TFTs under bias-temperature stress and have great potential for the AM-OLED’s pixel circuit.
CHAPTER VII

Conclusion

7.1 Conclusions

In this dissertation, the requirements for the future AM-FPDs and AM-FPIs have been reviewed and the double gate (DG) coplanar homojunction a-IGZO TFT was investigated for its application. The higher field effect mobility ($\mu_{eff}$) around 10 - 20 cm$^2$/V·sec or even higher are desired for future high resolution displays, such as 8K $\times$ 4K and the refresh rate of 240 Hz. Furthermore, for the application in medical imaging, especially for tomosynthesis, APS (active pixel sensor) pixel circuit with 50 $\mu$m pixel-pitch and the dynamic range of 60 dB is required. The TFTs with $\mu_{eff} \geq 4.6$ cm$^2$/V·sec is desired for these requirements. According to previous intensive research studies on a-IGZO TFTs, it has been proved that a-IGZO TFTs with $\mu_{eff}$ over 10 cm$^2$/V·sec can be easily fabricated.

Besides the mobility requirement, TFT miniaturization is another important factor for high pixel density applications. Since an allowed pixel size decreases as the pixel density increases – the pixel size for 500 pixels per inch (PPI) is only 50.8 $\times$ 16.9 $\mu$m, for instance – the TFT needs to be scaled down along with the pixel size to be squeezed inside of the limited pixel area. Furthermore, it is known that the miniaturization of TFTs improves the display performance by reducing the parasitic capacitance.
Therefore, we have studied the scaling characteristics of coplanar homojunction a-IGZO TFTs in Chapter III. We confirm that the coplanar homojunction a-IGZO TFT has good ohmic contacts with a low contact resistance \( R_{SD} \cdot W, \ W = 60 \ \mu m \) of 16.8 \( \Omega \cdot cm \). Hence, we did not measured a significant degradation on \( \mu_{eff} \) with L down to 3 \( \mu m \). However, the current reduction is observed at low \( V_{GS} \) for long channel a-IGZO TFTs (L > 5 \( \mu m \)). In contrast, the current reduction occurs at high \( V_{GS} \) for short channel TFTs (L < 5 \( \mu m \)). The 5 \( \mu m \) is the optimal L for TFT structure studied in this work without suffering these two degradations. However, this optimal channel length could be different for different TFT structures, such as different dielectric material/thickness and metal contacts.

Furthermore, in the case of TFTs with L \( \leq \) 5 \( \mu m \), \( r_{out} \) and S degrade rapidly and negative \( V_{TH} \) is observed, and we speculated that is due to the weaken channel controllability of the gate for short channel TFTs. To achieve small L TFTs without any performance degradation, the thickness of gate dielectric should be scaled properly or a double-gate (DG) device structure must be introduced. In this regard, the DG coplanar homojunction a-IGZO TFT is fabricated and its electrical characteristics are investigated in Chapter IV. Under DG bias condition (i.e. synchronized condition), the top and bottom gate electrodes are connected together (synchronized), the top and bottom gate electrodes form two conduction channel layers at the top and bottom interfaces. A high \( I_{ON} \) and steep S are achieved without increasing \( I_{OFF} \). Moreover, the dynamic control of \( V_{TH} \) is demonstrated by applying various DC voltages on the top gate. We showed that the lack of the hole accumulation in the a-IGZO TFT is the basis for the linear dependence of the threshold voltage on top gate voltages. Additionally, the top gate is an excellent light shield, which ensures TFT stability under light illumination.

To provide better understanding of the electrical characteristics of DG a-IGZO TFTs, the analytic model of the TFTs are investigated in Chapter V. The simple
analytic models of DG a-IGZO TFTs with synchronized bias conditions are developed and compared with TG or BG only bias devices. From this work, we can conclude that the DG TFTs under the bias condition of $V_G = V_{BG} = V_{TG}$ can simply be considered as conventional TFTs with a gate capacitance of $C_{DI} = C_{BI} + C_{TI}$ and a threshold voltage of $V_{DTTH} = (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})/C_{DI}$.

Furthermore, it is clearly shown that the DG TFTs with the BG or TG bias have electrical performance comparable to the conventional single gate TFT in the linear operation regime. However, the DG TFTs with TG or BG bias conditions suffer from mobility degradations in the saturation regime and the decreased saturation voltage. Therefore, two gate electrodes need to be tied together to avoid such degradations. The congruence between the developed models and measurement results suggests that the developed models can successfully explain the electrical behaviors of the DG a-IGZO TFTs.

Finally, the electrical stability of DG a-IGZO TFT were investigated in Chapter VI. With positive bias-temperature stress, the threshold voltage shifts, $\Delta V_{TH}$, is reduced by one third of the value that is observed in single gate TFTs. (the best location: 0.4 → 0.1V, the worst location: 1.2 → 0.4V) Also in the negative bias-temperature stress, the $\Delta V_{TH}$ of DG a-IGZO TFTs shows the enhanced values. (0.2 → < 0.1 V)

Overall, the superior electrical properties and electrical/optical stability, observed in this dissertation, make the DG a-IGZO TFT a possible candidate for the pixel circuits of future high resolution AM-FPDs and AM-FPIs. We strongly believe that DG a-IGZO TFTs are a better choice that traditional single gate a-IGZO TFTs.

### 7.2 Recommendations for Future Work

Three subjects are recommended for completeness of the research related to DG a-IGZO TFTs.
• **Origin of the negative $V_{TH}$ shifts on the positive bias stress**: The transfer curves of a-IGZO TFTs typically show positive shifts under the positive bias stress condition. These shifts traditionally explained by the electron trapping near the semiconductor/insulator interface or into the gate insulator. However, both single and double gate TFTs in this dissertation shows the negative shifts on the positive stress. These negative shifts on the positive bias stress contravenes the electron trapping mechanism. Therefore, the further investigation on this subject is strongly recommended.

• **Parasitic capacitance extraction**: In this dissertation, the superior electrical properties and stability of DG a-IGZO TFTs are discussed. However, the major drawback of the double gate structure is its increased parasitic capacitance. The parasitic capacitance of TFTs is mainly due to the overlap between the gate and source/drain electrodes and affects on the dynamic performance (i.e. A.C. performance). Owing to the additional gate electrode in DG TFTs, the parasitic capacitance would increase. Since enhanced electrical properties of DG TFTs can make its size smaller (smaller channel width) for the same amount of drain current, a decrease in device $W$ can possibly cancel out a possible increase in parasitic capacitance. Nevertheless, the parasitic capacitance should be quantitatively analyzed/measured and considered at the stage of circuit design for the accurate circuit simulation.

• **Develop SPICE model for DG a-IGZO TFTs**: To fabricate an optimized (or complex) pixel circuits on AM-OLEDs or APS imagers for the industry applications, the accurate and reliable SPICE model is supposed to be developed. Although a few research has been reported on SPICE model of a-IGZO TFTs, there is still lack of the model for DG a-IGZO TFTs. The analytic models developed in Chapter V would be a good reference and a starting point of this work. The new SPICE model has to have a good consistence with the observed characteristics and also needs to include the above mentioned parasitic capacitance.
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