An Energy-efficient Adaptive CMOS Image Sensor

by

Jaehyuk Choi

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Doctroral Committee:

Professor Euisik Yoon, Chair
Professor Kensall D. Wise
Assistant Professor David D. Wentzloff
Assistant Professor James W. Cutler

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Finally, I want to give my thanks to my mother. Thank you for constant encouragement, support and love.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

In this thesis, an energy-efficient CMOS image sensor has been studied to adaptively provide low-power consumption, high dynamic range, and reduced spatial-temporal bandwidth for applications in distributed sensor networks and wireless biomedical imaging systems.

In wireless sensor nodes, image sensors typically have four main challenges to address: low power operation from limited energy sources such as batteries or energy harvesting units, high dynamic range imaging to cover a wide range of illumination, high spatial resolution for high-quality imaging, and high temporal resolution for video streaming output. However, it is difficult to optimize all of these as there are trade-offs among these four parameters and additionally the environmental conditions continuously change, requiring optimization of sensor operation on-the-fly.

One of the solutions to this trade-off is implementing an image sensor with situation-aware adaptability. In this work, three on-chip adaptive functions have been investigated including (1) energy-adaptive imaging for low-power operation, (2) illumination-adaptive imaging for high-dynamic range, and (3) object-adaptive imaging for temporal-spatial bandwidth suppression.

For proofs of concepts of this adaptive imaging, we designed two prototype chips. Both prototype sensors have been fabricated and fully characterized. In the first chip, we implemented the energy/illumination adaptation by reconfiguring the mode of operation.

Most of the time, the sensor operates in a monitoring mode at an extremely low power (less than 1.36 µW/frame) with the power supplied from energy harvesting units. It switches to either a high-sensitivity or a wide-dynamic range mode of operation depending on illumination conditions. This illumination adaptation provides reconfigurability for sensitivity and dynamic range. The sensor can provide a high sensitivity of 23.9 V/lx·s at low illumination, but it can be reconfigured to generate a high dynamic range of up to 99 dB in high illumination on-the-fly.

In the second chip, we implemented motion-triggered, object-adaptive imaging to suppress the redundancies in spatial and temporal bandwidths in image signals. The sensor will wake up when triggered by motion and extracts features from the captured image for the detection of objects-of-interest. Full image capture operation is performed only when the objects-of-interest are found, resulting in a significant reduction of total power consumption at the sensor node. Object detection has been performed using the classification algorithm and has achieved a 94.5 % success rate for human recognition from 200 test images.

Adaptability enables energy-efficient image sensing with continuously varying environmental conditions such as illumination, energy availability, and various objects changing in the focal plane. Using the three adaptation schemes, the implemented image sensors provide high dynamic range images (> 99 dB) at low power consumption (< 1.36 µW) while maintaining low bandwidth (< 3.5 %) for image signal transmission.

CHAPTER 1 INTRODUCTION AND BACKGROUND

1.1 Evolution of digital imaging systems

The evolution of digital imaging systems can be categorized as three generations according to their applications and technologies. In the 1st generation, the emergence of digital imaging systems enabled the development of a variety of devices such as digital still cameras, camcorders, webcams and so on. Industry also benefitted from the digital imaging solutions, for example, broadcasting systems, machine visions, and inspection systems. In the 1st generation of imaging systems, Charge Coupled Devices (CCD) had been widely used since developed in the 1970s. In the 2nd generation, imaging systems were integrated with handheld devices such as cell phones, laptops, and tablet PCs during the 1990s. This evolution was mainly enabled by the development of a low-cost CMOS process and also by improvements in communication technology. The main differences from the 1st generation imaging systems which were mainly used for consumer electronics and industry are that the 2nd generation imaging systems are operated by battery and are linked with the networks. As such the image sensor consumes less power, has a small form factor, and has a low cost for the application of portable devices. Due to these demands, CMOS image sensors replaced CCDs in most imaging products [1.1]. Currently, imaging systems are expected to be distributed in a wide area due to the emergence of sensor networks and ubiquitous computing. Moreover, wireless biomedical sensors also integrate image sensors for applications in endoscopy, microscopy and retinal implants. This 3rd generation of imaging systems are distributed, fully networked,

1

and operated with extremely low-power consumption from energy harvesting in order to monitor wide or unreachable areas. The networked distributed imaging systems have several advantages over conventional imaging system [1.2]:

1. Sensing visibility: multiple low-resolution imagers cover wider range than a single high-resolution imager

2. Pose diversity: multiple imagers are in different poses (position, orientation)

3. Statistical convergence: we can get the information based on the gross statistics of the environment

4. Multiple perspectives: we can get more information from the view-dependent properties of the object from different perspectives

Generation	1	2	3
Applications	Appliance, industry	Handheld devices	Distributed network
	Digital still camera, camcorder, Industrial automations	Cell phone, laptop, tablet	Surveillance networks, Micro vehicles, Wireless biomedical imaging
Technology	CCD	CMOS	CMOS SoC
Topology	Standalone	Linked	Fully networked
Power delivery	Wired or battery	Battery	Energy harvesting

Table 1.1 Main features of digital imaging systems

The main applications of distributed image sensor network are military surveillance, environmental monitoring, traffic management, surveillance over distributed crops, and healthcare / patient monitoring. The other main applications of 3rd generation imaging systems are biomedical sensors. One such commercialized sensor is the capsule endoscope [1.3] which integrates an image sensor, a controller, and a wireless transmitter. These image sensors can also be integrated with a wireless microscope [1.4] or with a

retinal stimulator [1.5, 1.6], and so on. The main features of each generation are summarized in table 1.1.

1.2 Solid-state imaging devices

A charge-coupled-device (CCD) is a device that transfers charges integrated in photo-sites serially by applying clock signals. Incident photons are converted to charge by a photo-detector. Generated charge is transferred vertically through vertical CCD, and transferred horizontally through horizontal CCD using the clock signal. In order to enhance the charge transfer efficiency, a high voltage clock signal is used. In the output stage, transferred charge is converted to voltage through the amplifier. The basic structure of a CCD image sensor is shown in figure 1.1
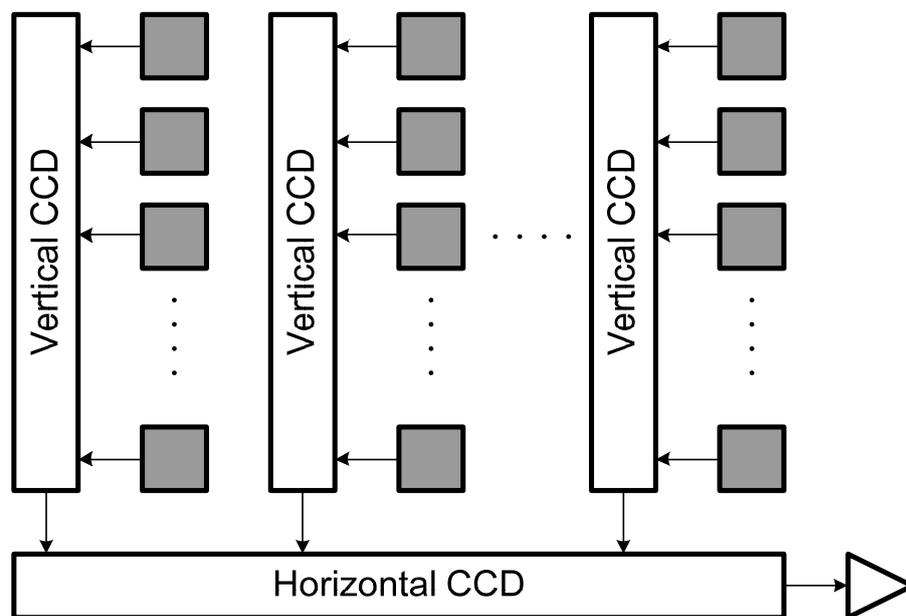
Figure 1.1 CCD image sensor.

CCDs have been used for high-end imaging systems due to low noise and high quantum efficiency. However, it consumes large power due to a charge transfer operation with high voltage. Power consumption is critical factor for mobile devices or any other

power-limited applications which require extremely low power consumption. Scalability is another important issue because it is difficult to scale the pixel array larger due to limited speed of charge transfer. Moreover, a CCD image sensor is difficult to integrate CMOS circuitry such as an image processor or an analog-to-digital converter, because a fabrication of CCD requires optimized fabrication process.

CMOS image sensors have not been widely used although it has longer history than a CCD image sensor. Since MOS image sensors have been developed in 1960's, low SNR of a CMOS image sensor made it behind from the market, and main focus of research in imaging devices has been concentrated on a CCD.

In 1980's, a MOS image sensor was resurfaced due to the development of CMOS fabrication technology. CMOS image sensor technology was rapidly developed due to the integration ability, scalability, low-cost, and low power consumption [1.7].

An imaging system with CMOS image sensor can be implemented with a single chip, or so called "Camera-on-a-chip", because both CMOS imagers and integrated circuits can be fabricated using standard CMOS technology with low cost. By integrating ADCs, periphery circuits, and image signal processors into one chip, the size of imaging system can be reduced. On the other hand, fabrication of CCD is specialized and optimized for effective photo-carrier generation and charge transfer. Imaging systems using CCD require off-chip components such as timing generators, analog-to-digital converters, and image processors. Accordingly, the cost for imaging systems with CCD imager is higher than one chip solution with CMOS image sensor.

CMOS image sensors can be categorized into two types: a passive pixel sensor or an active pixel sensor. A passive pixel sensor (PPS) consists of a photodiode and a selection

transistor as shown in figure 1.2 (a). The photocurrent which is generated from incident light is converted to voltage in the column-parallel charge amplifier [1.8]. A PPS has a high fill factor which is defined as the ratio of photodiode area over pixel area. In general, high fill factor provides higher sensitivity in a given form factor because a photodiode can collect more electrons. However, a PPS has low SNR for several reasons. First, small photo-current is difficult to read out due to large capacitance of column line. Second, considerable leakage current through the selection transistor corrupts the signal. Moreover, scalability of a pixel array is limited because the column-parallel charge amplifier has to drive larger capacitance.

Due to the low SNR of a PPS, most CMOS imagers have an active pixel sensor (APS) architecture. As shown in figure 1.2 (b), an active pixel has an in-pixel amplifier in order to drive the column line, which has large parasitic capacitance. Fill factor is decreased compared with passive pixel because of the area from in-pixel circuits. However, the isolation from the column line through an in-pixel buffer provides higher SNR compared with the PPS architecture.

CMOS image sensors output the voltage using an in-pixel amplifier, whereas the charge is transferred serially in CCD image sensors. Therefore, readout with high frame rate and random access is possible. Moreover, photo-detectors such as photo-gates and pinned photodiodes provide enhanced sensitivity and better noise immunity compared with conventional p-n junction photodiodes. The architecture and the operation principles of CMOS image sensor will be explained in chapter 2.

Column Output   Column Output

(a) Passive pixel   (b) Active pixel
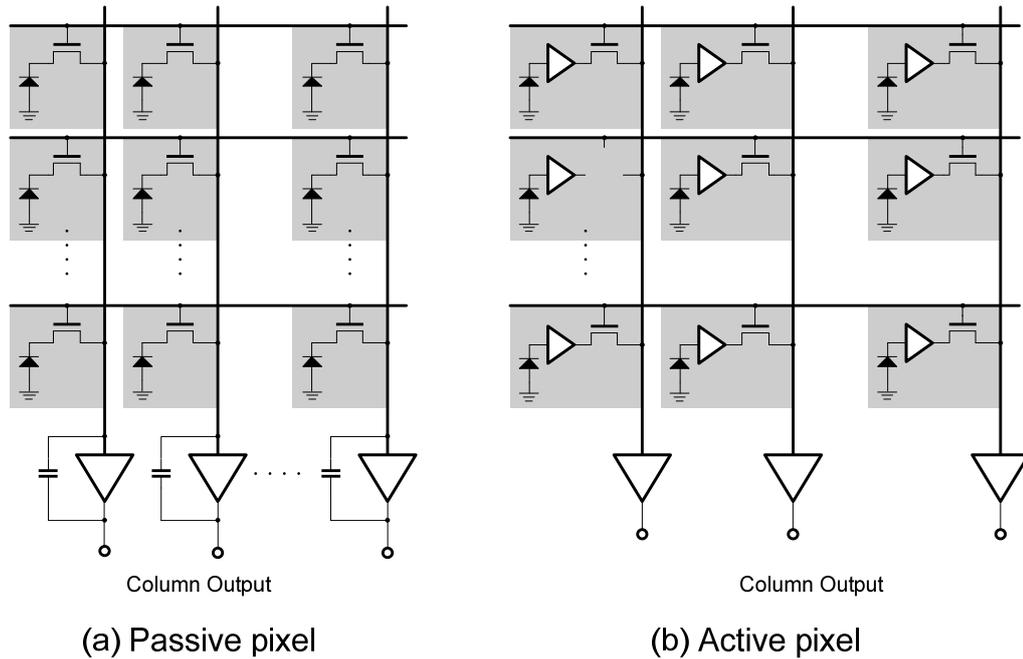
Figure 1.2 Passive pixel and active pixel sensor architecture.

1.3 Challenges in low-power image sensors

In applications for distributed image sensors and wireless biomedical sensors, we have four main challenges in image sensors as shown in figure 1.3. The first is power consumption because imaging systems use limited energy sources such as a battery or energy harvesting from the environment. State-of-art image sensors have large power consumption > 30 mW which is not applicable to be operated with energy harvesting. The power consumption of CMOS image sensors is difficult to be scaled down because the voltage scaling directly suppresses the SNR which brings loss of image quality. The second challenge is wide dynamic range. In outdoor applications, the illumination level varies from extremely dark to extremely bright. In biomedical sensors, illumination level is typically low, especially when monitoring inside the body or monitoring cells. Accordingly, the dynamic range and the sensitivity of image sensors should be high in order to guarantee reliable monitoring.

6
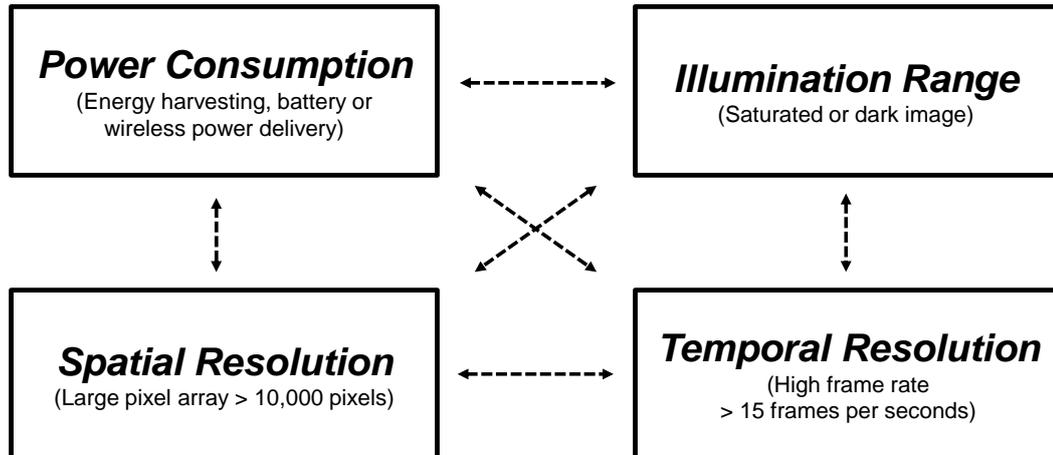
Figure 1.3 Four main challenges in image sensors.

Conventional CMOS imagers without integrated dynamic range enhancement schemes do not have enough dynamic range and sensitivity. The third challenge is large bandwidth (spatial) for large pixel arrays. The image signal has 8-bit (gray-scale) or > 10-bit (color) bit-depth. The number of pixels is typically larger than 10,000 (100×100 pixels). Therefore we need to transmit 80,000-bit for the transmission of one image frame, which is too large in bandwidth-limited applications. The image compression schemes such as JPEG and DPCM can reduce the bandwidth. However, the image compression entails the loss of information and requires power-consuming processing. The last challenge is high temporal resolution (or frame rate). Conventional image sensors have fixed frame rate from 15 to 60 frames per second (fps). Some high-speed sensors have high frame rate (> 1,000 fps) in order to suppress the motion-blur from moving objects [1.9-1.11]. As mentioned, transmitting 80k-bit with 15 fps requires huge bandwidth and power consumption. However, it is rare that the event we want to monitor occurs 15 times in a second. Therefore, imaging with constant frame rate is redundant. If sensors can monitor specific event and provide event-driven image transmission, temporal redundancy will be dramatically suppressed.

It is difficult to optimize for the four main challenges because these parameters have trade-off relationships each other. For example, the reduction of power consumption entails the reduction of dynamic range and bandwidth. Bandwidth reduction also entails the reduction of dynamic range or the increase of power consumption when we use complex image processing algorithms. Therefore, we need to find optimization points that consider these four parameters: power consumption, dynamic range & sensitivity, spatial bandwidth and temporal bandwidth. However, this optimization point varies according to the applications and time.

1.4 Research goals

The main goal of this work is implementing an energy-efficient image sensor that is applicable to the 3rd generation imaging system including distributed image sensor networks and biomedical sensors, i.e., implementing an image sensor with low-power consumption, wide dynamic range, and low spatial-temporal bandwidth. Considering four main parameters (power consumption, dynamic range & sensitivity, spatial bandwidth, and temporal bandwidth), an efficient way to implement an image sensor is providing the adaptability, because these four parameters always have trade-off. Figure 1.4 shows the proposed concept of an adaptive image sensing scheme. Three adaptation schemes suppress the redundancy of data and reduce the power consumption by adapting to the environment. In the adaptive imaging, the first procedure starts from motion sensing to reduce temporal bandwidth. The sensor is in sleep mode, while only the integrated motion sensor is turned on, and monitors with extremely low-power consumption. The sensor is woken up and is triggered to operation mode from the movement of the object. By motion-driven activation, we can eliminate constant imaging and constant image

8

transmission with fixed frame rate. Therefore, we can save both the power consumption and the bandwidth especially in a stationary environment. Then, the motion-triggered sensor monitors the object in the focal plane. As mentioned, not all of the objects in the scene are of interests. For example, a swaying tree in the background is not interesting.

Power consumption
Energy source adaptation
Adaptive power supply
from the energy harvesting &
illuminations conditions

Illumination range
Illumination adaptation
Adaptive dynamic range & sensitivity
from the illumination conditions

Spatial / temporal resolution
Object adaptation
Object-of-interest imaging
from the target-object detection
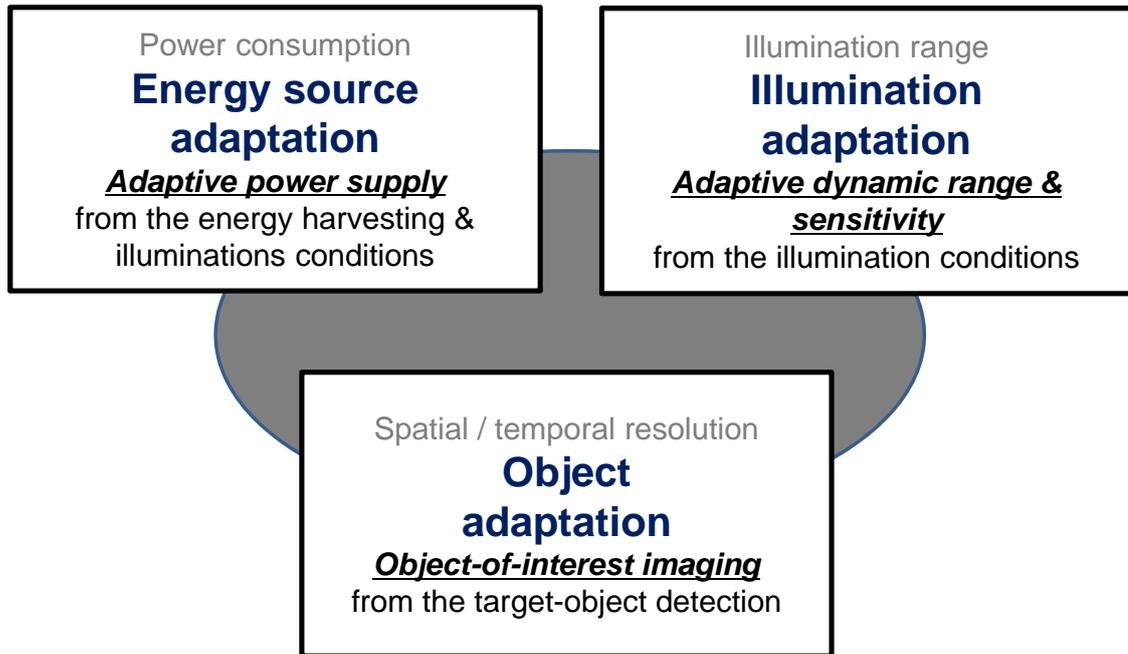
Figure 1.4 Concept of adaptive image sensing.

The sensor detects target objects in the 2nd procedure, i.e., it classifies whether the object in the focal plane is of our interest or not. In the 2nd procedure, instead of generating an image signal which has a large amount of data and redundancy, we generate a low-bandwidth feature for the object detection. The generated feature can be processed for the object detection in the host or in the local node. The processor classifies the object and feeds back the request signal to the sensor. If a target object is detected, imaging operation is initiated. This object-of-interest imaging for the object adaptation saves power consumption and bandwidth further.

9

After the object detection, the sensor starts the imaging operation with low power consumption. The main goal of the imaging is to provide a quality image signal in wide ranges of illumination with limited energy source. For low power consumption, the proposed sensor has an energy source adaptation using adaptive power supply voltage. For wide dynamic range, the sensor also has an illumination adaptation which has adaptive dynamic range and sensitivity for varying illumination conditions.
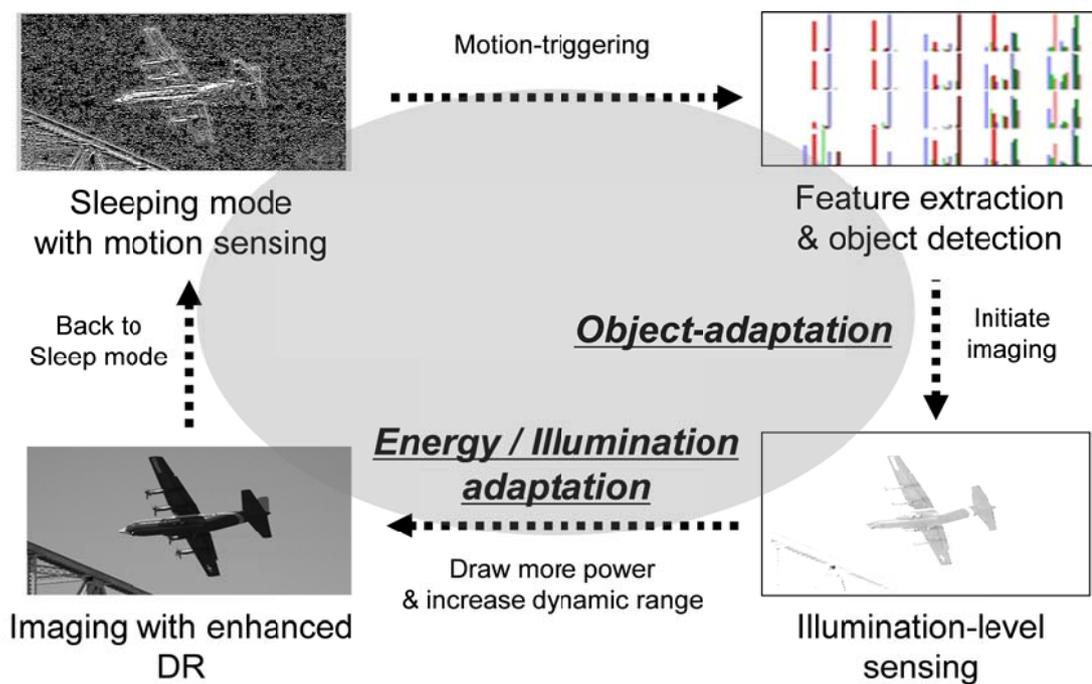
Figure 1.5 Operation of adaptive image sensing.

In order to implement the adaptive image sensor, we implemented two prototype chips as follows:

1. An adaptive CMOS image sensor with reconfigurable modes of operations: Demonstrates the operation of the energy-source adaptation and the illumination adaptation

2. A CMOS image sensor with embedded feature extraction for motion-triggered object-of-interest imaging: Demonstrates the operation of the motion adaptation and the object adaptation

1.5 Thesis organizations

Chapter 2 introduces a CMOS image sensor including basic operation principles. In chapter 3, the power consumption of CMOS image sensor is estimated first. From this estimation, the challenge and strategy of low-power CMOS imager will be discussed. Chapter 3 also illustrates previous works in three categories that are essential in the wireless image sensing systems: low-power CMOS image sensors, wide dynamic range & high-sensitivity image sensors, and image sensors with integrated image processing for the bandwidth suppression.

Chapter 4 describes an energy / illumination-adaptive image sensor. A proposed adaptive CMOS image sensor with reconfigurable modes of operations will be explained.

Chapter 5 illustrates an object-adaptive image sensor. A motion-triggered object-of-interest imaging based on the integrated feature extraction will be explained.

Chapter 6 summarizes this work and discuss about future works.

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CHAPTER 2 INTRODUCTION TO CMOS IMAGE SENSORS

2.1 Image signal chain and overall architecture

An image sensing is the process that measures the number of incident photons. The final output from image sensors is the digital image signal that quantizes the number of incident photons. An image signal chain is shown in figure 2.1. Incident photons generate electrons in photo-detectors. The photo-generated electrons are swept by electric field, which is from reverse-biased voltage applied to photo-detectors. In this way, the photocurrent (i_{ph}) flows in photo-detectors. The photocurrent is integrated in photo-detectors and is converted into the voltage V_{PD}. This voltage is read out though in-pixel amplifier circuits. Finally, output voltage V_{OUT} is converted to the digital signal.
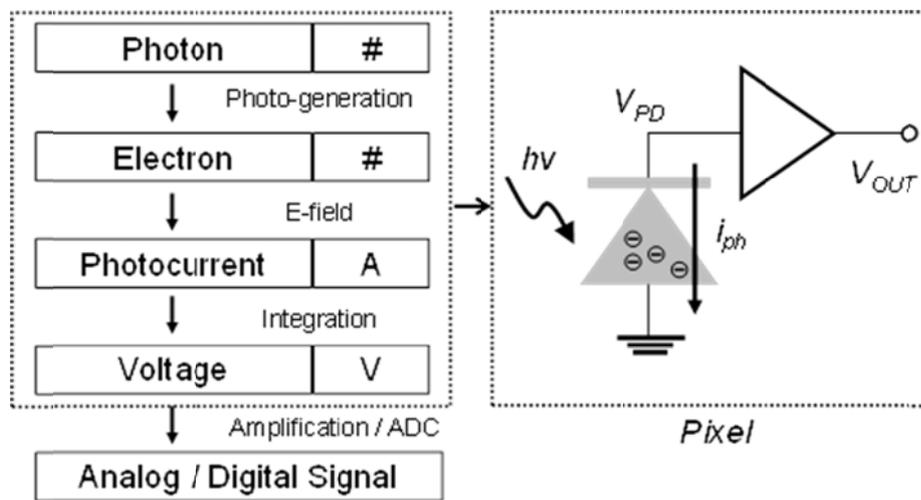
Figure 2.1 Image signal chain.

Figure 2.2 shows one example of the CMOS image sensor architectures. CMOS image sensors include pixel array, column-parallel correlated double sampling (CDS) circuits & ADCs, latches, row scanners and column scanners.
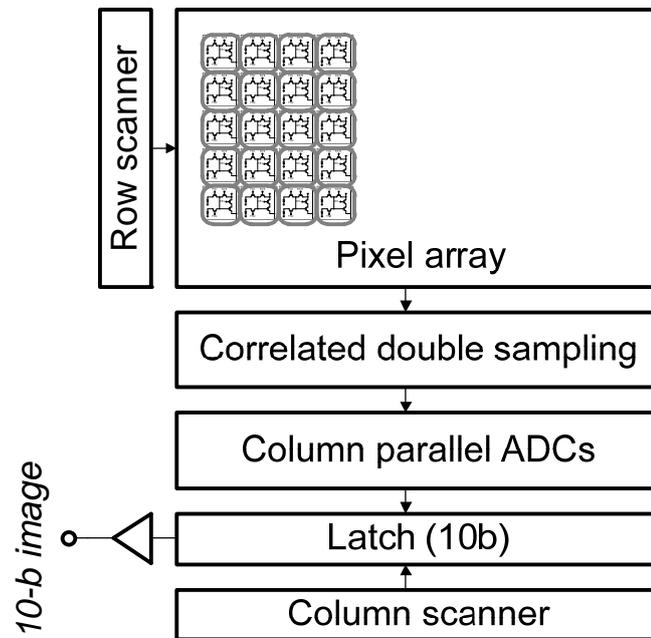
Figure 2.2 Overall architecture of CMOS image sensor.

The operation is as follows: (1) incident photons are converted into electrons, and electrons are accumulated in the photodiode in each pixel during the integration time (T_{INT}, also called exposure time) (2) in-pixel circuits convert integrated electrons into voltage. (3) The row scanner scans and selects one row out of pixel arrays. One row of pixels selected by the row scanner is read out through the column line. (4) CDS circuits cancel the fixed pattern noise that is inherent in pixel arrays. CDS circuits also amplify the signal and suppress the input-referred noise. (5) Noise-cancelled signals from CDS circuits are converted into the digital signals through ADCs. Converted digital signals are temporarily stored in latches before the readout. (6) Column scanners scan latches

column by column, read out digital signals. (7) The procedure repeats for entire rows, and one image frame is generated.

2.2 Photogeneration

A photon is the carrier of electromagnetic radiation of all wavelengths. It is massless and is traveling at the speed of light. The energy of photon can be expressed as Eq. 2.1.

$$E = h\nu = \frac{hc}{\lambda} \tag{2.1}$$

,where h is Planck's constant, c is speed of light λ is wavelength, and ν is frequency.

Silicon is the most widely used material for photo-detectors as well as for contemporary VLSI circuits. With incident photons, electron-hole pairs (e-h pairs) are generated. This process is called photogeneration. Separated e-h pairs can be combined and this process is called recombination. The photogeneration and recombination process is shown in figure 2.3. Silicon is in the equilibrium state without any incident photons. In the equilibrium state, the number of electrons in the conduction band (n_0) is equal to the number of holes in the valence band (p_0). Electron-hole (e-h) pairs are continuously generated from the thermal energy. However, generation rate (G) is equal to recombination rate (R) in the equilibrium.

When there are incident photons, the equilibrium is broken. When the photon energy (E=hν) is higher than the bandgap energy (E_g), photons collide with electrons in the lattice, and electrons absorb the energy of photons to become free electrons. Therefore, excess e-h pairs are generated as Eq.2.2:

$$n = n_0 + \Delta n, p = p_0 + \Delta p \tag{2.2}$$

15

,where n_0 is electron concentrations in the conduction band (@ equilibrium) and p_0: hole concentrations in the valence band (@ equilibrium). Generated e-h pairs are diffused and recombined within minority carrier lifetime (τ). Recombination rate (R) can be expressed as Eq. 2.3.

$$R = \frac{\Delta n}{\tau}$$ (2.3)

Incident photons into silicon surface travel in silicon. After traveling some distance, they are finally absorbed. Figure 2.4 shows the photonflux. The photon flux F can be expressed as Eq. 2.4.
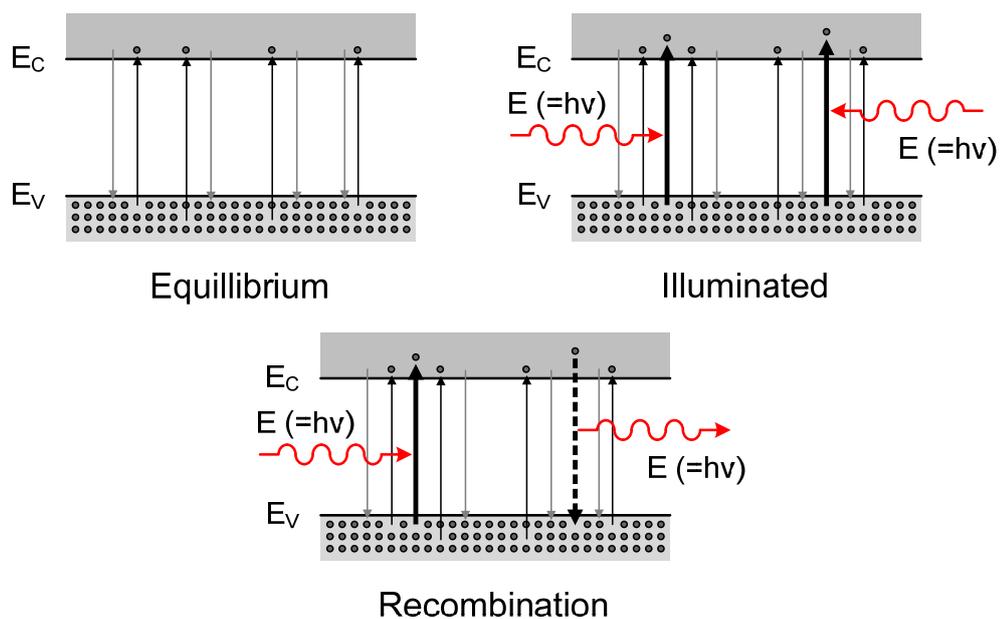
Figure 2.3 Image signal chain.

$$\frac{dF(x)}{dx} = -\alpha F(x) \;\rightarrow\; F(x) = F_0 e^{-\alpha x}$$ (2.4)

,where F_0 is the photon-flux of incident photons ($F(0)$), α is the absorption coefficient [cm^{-1}] that is material and wavelength dependent. The inverse of absorption coefficient α^{-1} is the penetration depth at which the photon-flux is reduced to e^{-1} (=0.37). Note that photons are absorbed after traveling the distance of α^{-1} (penetration depth). The penetration depth is dependent on both the material and the wavelength. As shown in figure 2.4, photons that have the wavelength of blue travel short distance, whereas photons that have the wavelength of red travel long distance because the penetration depth is proportional to the wavelength.
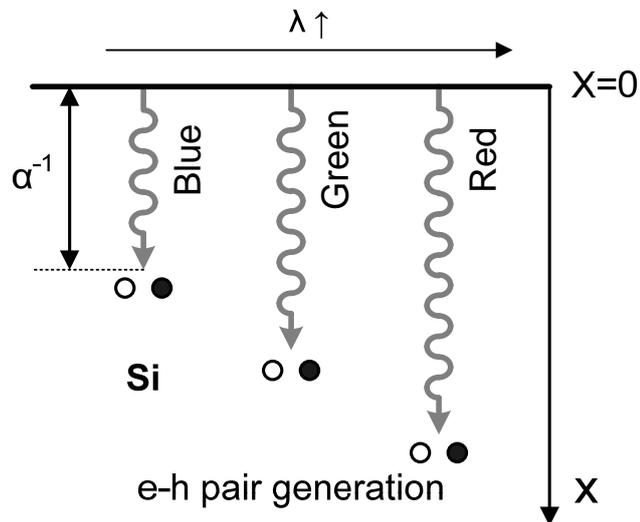
Figure 2.4 Absorption of the photon.

The generation rate of e-h pairs at the distance of x is proportional to the photon flux density dF(x)/dx as shown in Eq. 2.5.

$$G(x) = \frac{d(F_0 - F(x))}{dx} = \alpha F(x) = \alpha F_0 e^{-\alpha x} \qquad (2.5)$$

2.3 Photodetectors

Since photo-generated electrons are lost by the recombination, we have to collect electrons in order to measure the number of photons. In order to prevent the loss of electrons, we can just move electrons by electric field and collect in the collection sites as shown in figure 2.5. In order to reach a detectable signal level, electrons are accumulated in the capacitor during the integration time. The device that provides the electric field and also the storage capacitor is the photodiode, which is made of p-n junction.
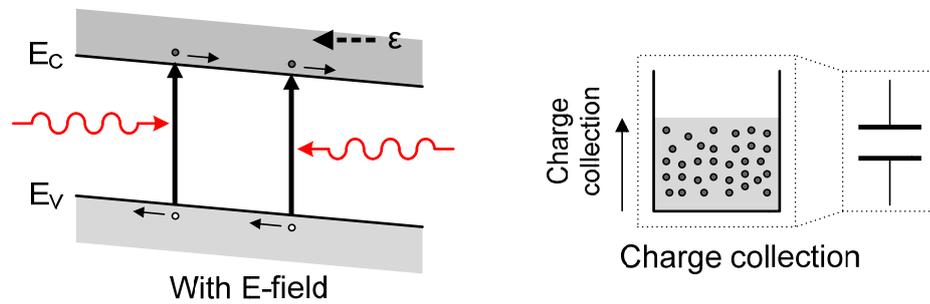
Figure 2.5 Charge collection.

2.3.1 P-N photodiode

A p-n junction photodiode is the photodetector that is available from the standard CMOS process. Figure 2.6 shows the p-n junction photodiode.
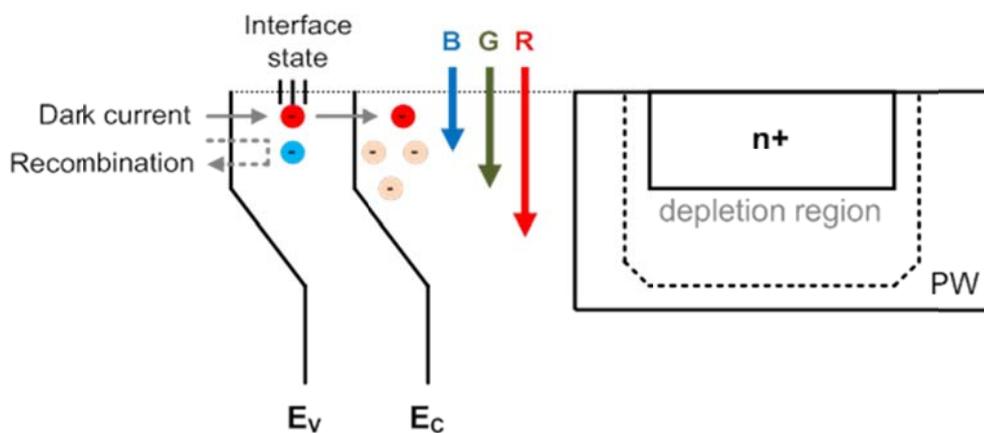
Figure 2.6 P-N photodiode.

18

The p-n junction is typically formed with n+/pwell or with nwell/p-sub. Photodiodes operate in the reverse biased condition. In the reverse biased condition, incident photons induce photocurrents in photodiodes.
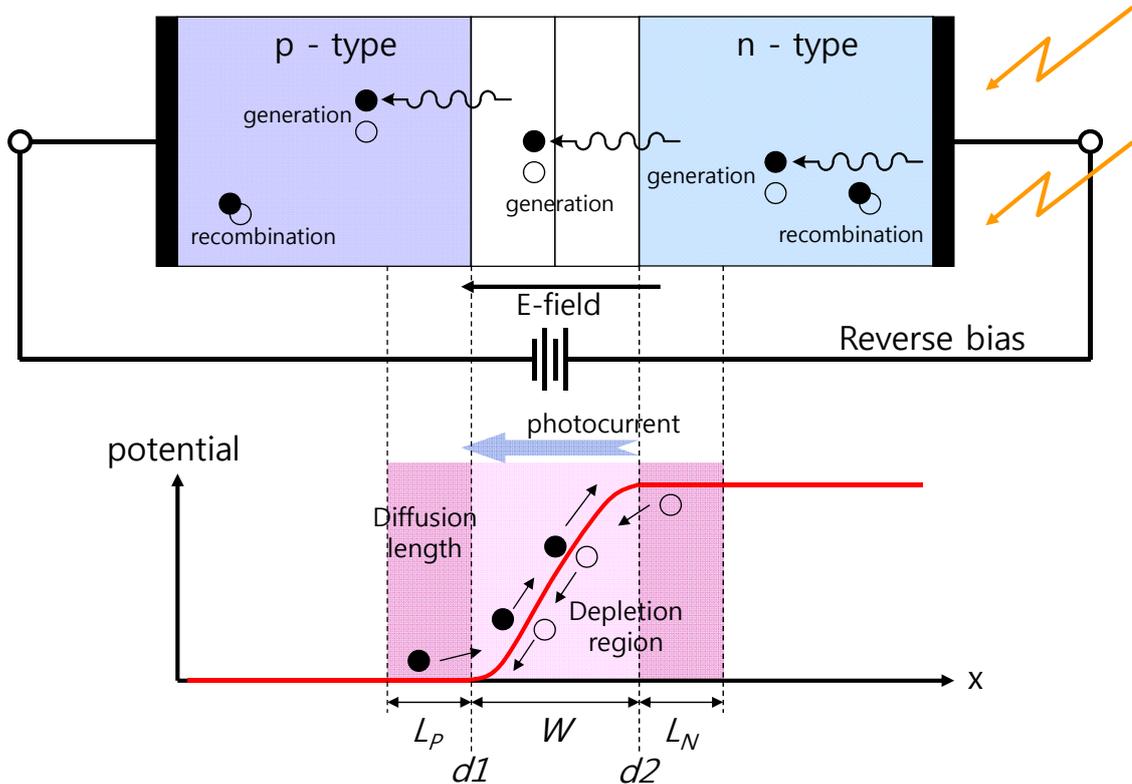
Figure 2.7 Photogeneration in P-N photodiode.

Photocurrent

As shown in figure 2.7, photo-generated electrons are swept by electric field in depletion regions. Note that photo-generated electrons in neutral regions are mostly recombined. In neutral regions, only a small portion of electrons that are generated within the diffusion length (L_p, L_n) from depletion regions diffuse into depletion regions and contributes to the photocurrent ($J_{ph(n)}$, $J_{ph(p)}$, diffusion currents). Electrons from depletion regions mostly contribute to the photo-current (J_{dep}).

Figure 2.8 shows the components of photocurrent. The total photocurrent density can be expressed as Eq. 2.6.

$$J_{ph} = J_{ph(n)} + J_{dep} + J_{ph(p)}$$

$$\approx J_{dep} = -q \int_{d1}^{d2} G(x)dx = qF_0\left(e^{-\alpha d_1} - e^{-\alpha d_2}\right)$$

(2.6)

,where d2-d1 is the depletion width W. In order to maximize the photocurrent, photodiodes should be optimized in order to have large depletion region. This can be achieved by (1) lowering the doping concentration of the bulk (2) shallow junction and (3) large reverse bias.
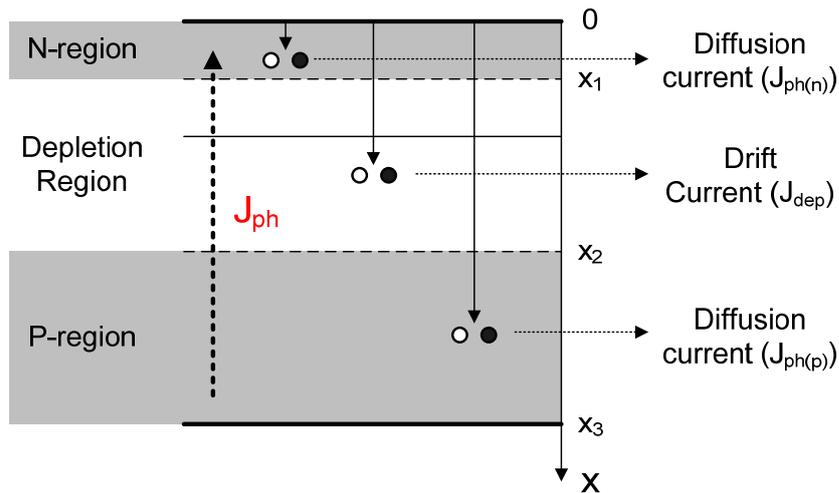
Figure 2.8 Photocurrent.

Dark current

Without any illumination, there is a leakage current in the photodiode. This is called "dark current". It is typically process dependent variable [2.1]. The dark current cause shot noise and fixed pattern noise, therefore, it decrease the SNR. The mechanism of the dark current can be categorized by two: one is the reverse-bias leakage current and the other is the surface generation current [2.2, 2.3]. Figure 2.9 shows the dark current

20

mechanism. The reverse bias leakage current mostly consists of two components: (1) generation current from the depletion current (thermal generation), (2) minority carrier diffusion current in neutral regions. The source of surface generation current is two: (1) the surface of n and (2) the interface with STI. Carriers are generated in the near vicinity of a surface via the interaction with interfacial taps due to the discontinuity of the lattice structure. The dark current equations can be expressed as follows:

$$\text{Generation current: } J_G = q\frac{n_i}{\tau_G}W \qquad (2.7)$$

$$\text{Diffusion current: } J_{DIFF} = q\sqrt{\frac{D_n}{\tau_n}\frac{n_i^2}{N_A}} \qquad (2.8)$$

$$\text{Surface generation current: } J_{SG} = \frac{qG_S}{2} \qquad (2.9)$$

$$\text{Total dark current: } J_{DARK} = J_G + J_{DIFF} + J_{SG} \qquad (2.10)$$

,where n_i is the intrinsic concentration of silicon, τ_G is the generation lifetime ($\tau_G = \tau_n + \tau_p$), W is the depletion width, G_S is the surface generation rate ($G_S = s_g n_i$), s_g is the surface generation velocity. The intrinsic concentration n_i is shown in Eq. 2.11 and the depletion width W is shown in Eq. 2.12.

$$n_i = \sqrt{N_C N_V e^{-E_g/2kT}} = A\left(\frac{T}{300}\right)^{3/2} e^{-E_g/2kT} \qquad (2.11)$$

$$W = \sqrt{\frac{2\epsilon(N_A + N_D)(V_{bi} - V)}{qN_A N_D}} \qquad (2.12)$$

,where N_C, N_V are carrier densities, E_g is the bandgap energy, N_A, N_D are doping concentrations, V_{bi} is the built-in potential of the p-n junction.
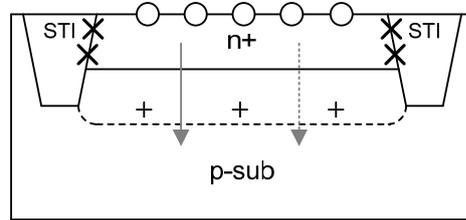
○ Surface defect

✕ STI interface defect

＋ Thermal generation

→ Minority carrier diffusion

Figure 2.9 Dark current mechanism.

According to Eq. 2.7 ~ 2.10, we can notice the factors affecting the dark current: (1) Temperature: if temperature increases, dark current also increases because of n_i term in the generation current and n_i^2 term in the diffusion current. (2) Doping concentration: if doping concentration increases (accordingly more defects), dark current increases due to the decrease of τ_G. (3) Reverse bias voltage: more reverse-biased voltage increases dark current due to increased W.

The dark current in p-n photodiodes decreases the SNR. This dark current is mostly from the surface generation, which is generated from the interface defects in the surface and in the STI region. Moreover, electrons that are generated near the surface can be easily trapped in the surface states and recombined, which do not contribute to the photocurrent. Therefore, p-n photodiodes have poor blue response.

By process variations, the surface can be isolated from the interface. Therefore, dark current can be suppressed. The photodiode which has isolated surface is called "pinned photodiode". The pinned photodiode will be explained in section 2.3.2.

Charge integration and detection

The photo-current (I_{ph}) is integrated in the junction capacitance of p-n junctions, and lowers the potential of cathode (in electron-potential, electrons are accumulated and the potential increases) as shown in figure 2.10. Note that the dark current (I_d) is also integrated. Operation procedures are as follows: (1) Before the integration of photocurrent, the cathode of photodiode is reset (V_R) (2) photocurrent discharges the junction capacitance (C_D) during the integration time (T_{INT}). Note that the parasitic capacitance (C_P) also contributes to the sense node voltage V_{PD}. (3) After T_{INT}, V_{PD} is read out using in-pixel buffers. (4) Reset again, next frame starts.
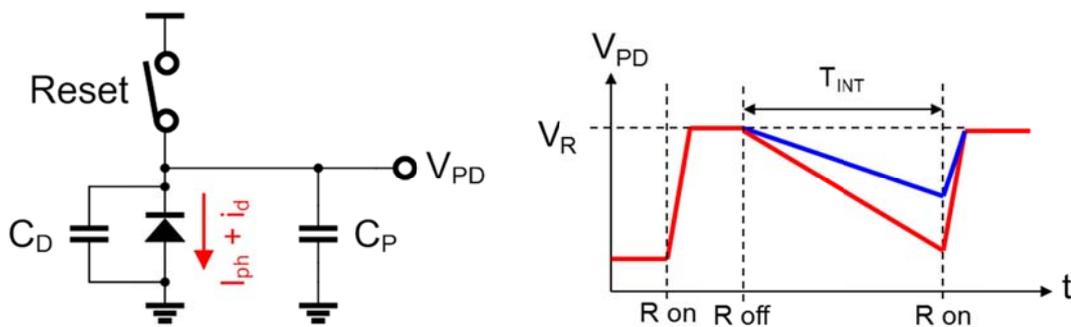
Figure 2.10 Charge integration.

Full well capacity

Like water is spilled out of bottle when we pour more than the maximum capacity of the bottle, same phenomena happens in photodiodes. When illumination is high and electrons are full of the capacitance, electrons are spilled over. The definition of full well capacity is the maximum capacity of charge storage of photodiodes. A full well capacity can be expressed as Eq. 2.13.

23

$$N_{SAT} = \frac{1}{q} \int_{V_{RESET}}^{V_{RESET} - V_{SWING}} C_{PD}(V) dV \quad [electrons] \qquad (2.13)$$

$$C_{PD}(V) \approx C_j = A_{PD} \left\{ \frac{q\epsilon N'_D N'_A}{2(N'_D + N'_A)(V_{bi} - V)} \right\}^{\frac{1}{2}} \qquad \text{for p-n junction}$$

$$\approx A_{PD} \left\{ \frac{q\epsilon N'_A}{2(V_{bi} - V)} \right\}^{1/2} \qquad \text{for p-n+ junction}$$

,where C_{PD} is the photodiode capacitance, C_j is the junction capacitance, V_{RESET} is the reset voltage and V_{SWING} is maximum voltage swing of the photodiode. Assuming C_{PD} is constant, full well capacity can be expressed as Eq. 2.14.

$$N_{SAT} = \frac{C_{PD} V_{SWING}}{q} \quad [electrons]$$
$$(2.14)$$
$$Q_{SAT} = C_{PD} V_{SWING} [C]$$

Conversion gain

The conversion gain is defined as the amount of voltage variation from one electron.

$$A_C = \frac{q}{\text{Capacitance of detection node}}$$
$$(2.15)$$
$$= \frac{q}{C_{PD}} \quad [\mu V/electron]$$

Higher conversion gain means that small amount of photons can induce high voltage swing. Therefore, higher conversion gain increases the sensitivity, which will be explained in the next subsection. In p-n photodiodes, the capacitance of detection node is C_{PD}. It means that higher the conversion gain, the full well capacity is lowered. If we can separate the detection node from photodiodes, we can achieve both high full well capacitance and high conversion gain. This will be revisited in the section 2.3.2.

Sensitivity

The sensitivity is defined as the ratio of output signal [V] to an incident illumination level [lx] in a second. The unit of sensitivity is [V/lx·s]. Note that high conversion gain increase the sensitivity, however, high sensitivity does not guarantee that the pixel has high conversion gain. The sensitivity can be increased from process optimization, microlens optimization, and so on.

Fill factor

Pixels consist of photodiodes and in-pixel readout circuits (typically source follower). The circuit area is shielded by metal layers in order to prevent from the photogeneration. Only the area of photodiode is exposed. Fill factor is defined as the portion of the pixel area that contributes to photo-sensitivity, i.e., the ratio of photodiode area to the pixel area. It is expressed as Eq. 2.16.

$$FF = \frac{A_{PD}}{A_{PIX}} \ [\%]$$ (2.16)

Larger fill factor increases the sensitivity because photodiodes collect more photons. One way to increase fill factor is shared pixel architecture. In shared pixel architecture, neighboring pixels share one readout circuit, and improves fill factor. Another way to achieve high fill factor is the backside illumination (BSI) technology. Using the BSI technology, photodiodes are exposed to the backside and the metal lines are located in the front side.

2.3.2 Pinned photodiode

The structure of a pinned photodiode is shown in figure 2.11. On top of the p-n junction, shallow p+ region is formed. This additional p+ implant isolates the n-region

from the surface and also from the STI region in order to suppress the dark current. Moreover, it offers better blue response compared with p-n photodiodes since the surface is isolated [2.2]. Note that n-region is fully depleted in order to collect more photons.
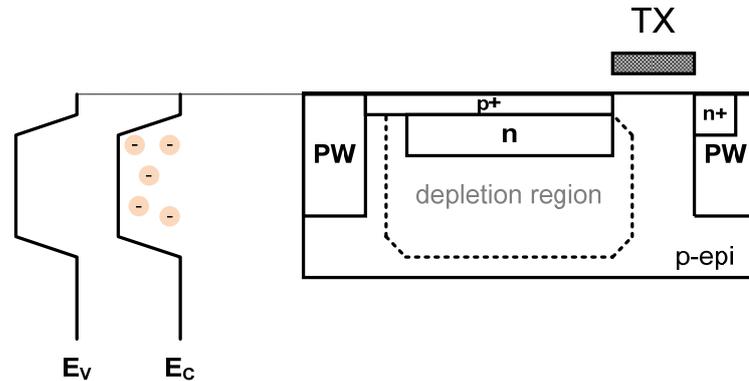
Figure 2.11 Pinned photodiode.

In this structure, the profile has a potential well due the p+-n-p structure. Therefore, photogenerated electrons can be collected in the potential well. The minimum potential of the well is called "pinning potential" which is generated from the profile of p+-n-p structure. Another advantage from pinned photodiodes is that we can completely transfer the collected electrons into the sense node without residual charges. Since the pinning potential is higher than the potential of sense node (which is reset to the power supply voltage), electrons in the well are completely transferred to the sense node with the aid of potential difference (electric field).

2.4 Pixel circuit

Pixel circuits consist of a photodiode and an in-pixel readout circuit. The photodiode has two types: p-n photodiodes and pinned photodiodes. In-pixel circuit drives the column line that has large parasitic capacitance. A source follower is typically used as an

in-pixel readout circuit. According to the number of transistors in pixel, the pixel is categorized as 3-T or 4-T pixel.

2.4.1 3-T Pixel with p-n photodiode

Figure 2.12 shows the 3-T pixel with p-n photodiode. Note that the bias current (not shown in the figure) is connected with column line (SIG) and is shared by all rows. The control signals (RST, SEL) is driven by the row scanner.

The operation procedure is described with electron potential diagrams in figure 2.13. The operation procedure is as follows: (1) Reset: the PD node is reset to $V_{DD} - V_{THR}$ due to the V_T drop in the reset transistor. In the reset operation, kTC reset noise (V_{kTC1}) that is thermal noise generated in the R-C circuit is added. (2) Integration: V_{PD} is decreased by integration of photocurrents. 'Q' is the integrated charge. (3) Signal readout: after integration time (T_{INT}), V_{PD} is read out through source followers. (4) Reset: reset PD node again for the next frame. (5) Reset level readout: this phase is for the correlated double sampling, which cancels the fixed-pattern-noise (FPN) in pixel.
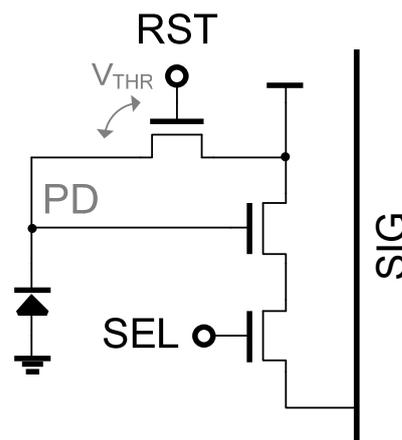
Figure 2.12 3-T pixel with p-n photodiode.

27
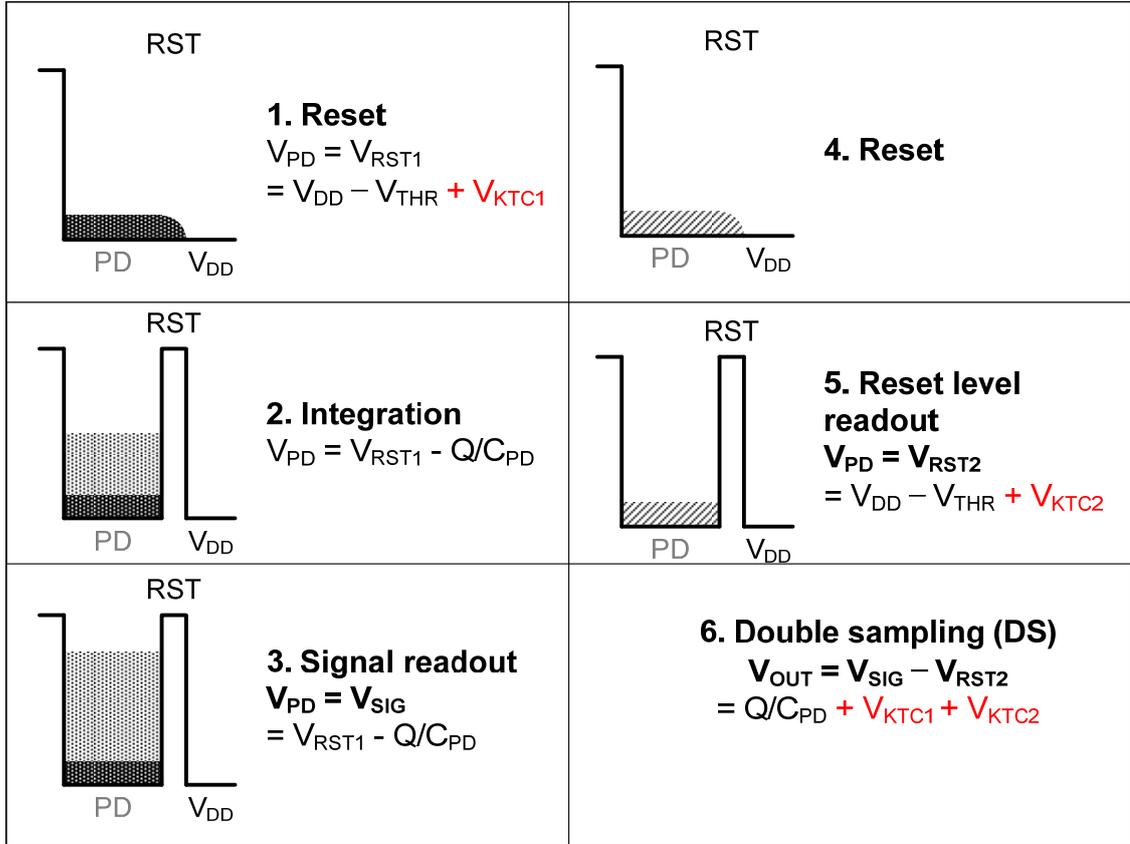
Figure 2.13 Operation of 3-T pixel.

The FPN is mainly from the V_T variation (in reset transistors and in source follower transistors) which is different from each pixel. By subtracting the reset level from the signal level, V_{THR} term is removed. In this phase, another kTC noise is added (V_{kTC2}). (6) Double sampling: V_{THR} term is removed. However, V_{kTC} is not cancelled from the double sampling because two kTC noise are not correlated each other, i.e., these two kTC noise are added in different timing. Since the kTC noise power can be expressed as kT/C, 3-T pixel has low SNR due to small capacitance of C_{PD}.

Moreover, as explained in the previous section, full well capacity and conversion gain are in trade-off relationships, i.e., larger well capacity induces lower conversion gain. Therefore, it is desirable to separate the detection node from photodiodes. The 4-T pixel

28

separates the detection node by using an additional transistor between the photodiode and the source follower.
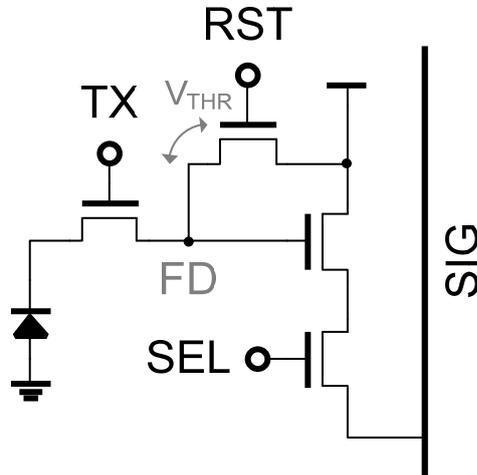
Figure 2.14 4-T pixel with pinned photodiode.

2.4.2 4-T Pixel with pinned photodiode

Figure 2.14 shows the 4-T pixel with pinned photodiode. As shown in the figure, the detection node which is called floating diffusion 'FD' is separated from photodiodes. The operation procedure is shown in figure 2.15. Assuming that FD node is reset before the integration, the operation is as follows: (1) Integration (2) Reset (FD): before the signal readout, reset FD node. The kTC noise is added (V_{kTC1}) (3) Reset level readout: read out the reset level for noise cancelling (4) Charge transfer: charges in photodiodes are transferred into the floating diffusion (TX is on). As explained before, pinning potential is higher than FD node, charges are fully transferred. (5) Signal readout: note that the signal has same kTC noise as in the reset phase (V_{kTC1}) since charges are dumped into the floating diffusion which already has kTC noise V_{kTC1}. (6) Correlated double sampling: the CDS operation cancels both the FPN and the kTC noise.

29
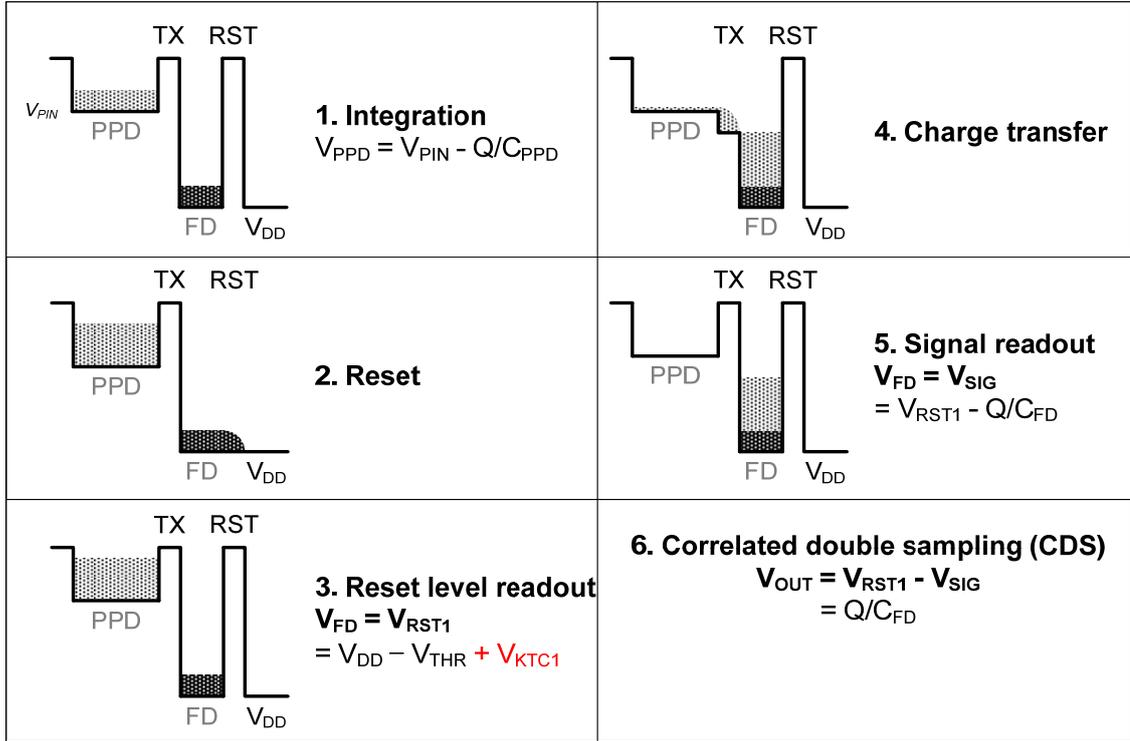
Figure 2.15 Operation of 4-T pixel.

Since kTC noise is cancelled in 4-T pixel, a 4-T pixel architecture offers better SNR compared with a 3-T pixel. Moreover, conversion gain of 4-T pixel ($A_{C(4T)} = q/C_{FD}$) is higher than 3-T pixel ($A_{C(3T)} = q/C_{PD}$). Note that the capacitance of FD (C_{FD}) consists of the gate capacitance of one transistor and the junction capacitance of two transistors. The capacitance of FD is small (typically < 5 fF) for the high conversion gain.

2.4.3 Shared-pixel architecture

The in-pixel circuits including the switch and the source follower takes some portion of the pixel area and decreases the sensitivity in a given pixel size. In order to increase the fill factor, neighboring pixels can share one readout circuit. This is called shared-pixel architecture [2.13-2.16]. Figure 2.16 shows 4-shared pixel circuit which has one readout circuit shared by four vertically neighboring pixels. In the shared pixel architecture, two

or four neighboring pixels share one floating diffusion (FD) node, one reset transistor and one source follower circuit.
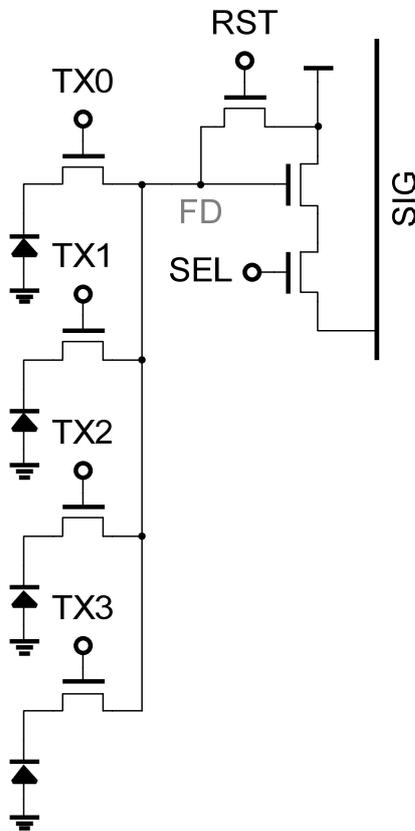
Figure 2.16 Shared pixel circuit.

In addition to small pixel size, we can easily perform the pixel merging in the shared pixel architecture. The pixel merging is the process to add signals from multiple pixels and provides better sensitivity and SNR (especially at low illumination) while reducing the spatial resolution. In the shared pixel architecture, integrated charges from photodiodes in a shared group are simultaneously transferred into a floating diffusion node and summed.

Contemporary CMOS imager typically uses two or four shared architecture. If more pixels are shared, we can achieve smaller pixel size with high fill factor. However, the

capacitance of FD node induces decreased conversion gain. Moreover, the leakage current from the other photodiodes in a shared group can corrupt the signal especially at high illumination. Asymmetry of the layout is another issue in the shared pixel architecture because only one readout path exists in multiple pixels. Due to the differences in adjacently located circuit components, photodiodes are no longer identical and the fixed pattern noise (FPN) can be induced [2.17].
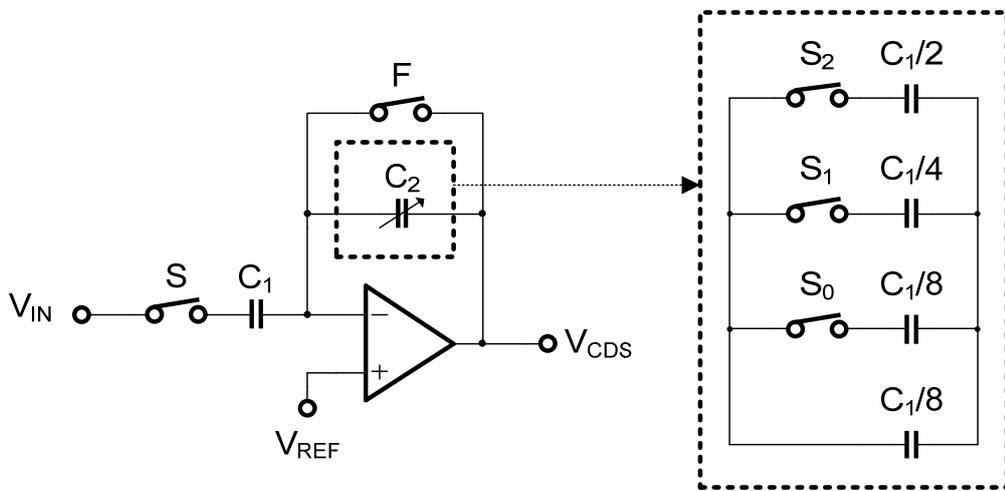
Figure 2.17 Correlated double sampling circuit.

2.5 Correlated double sampling (CDS)

A correlated double sampling (CDS) is an essential operation in order to suppress the fixed pattern noise (V_{FPN}) and the kTC noise (V_{kTC}). The fixed pattern noise is mainly from the variation of threshold voltage in in-pixel readout circuits. The kTC noise is the thermal noise in the RC circuit that is generated from the reset transistor and the sense node capacitance. In order to cancel the noise ($V_N = V_{FPN} + V_{kTC}$), CDS circuits sample reset voltage ($V_{RST} + V_N$) and signal voltage ($V_{SIG} + V_N$) successively, and subtract each other. One simple CDS circuit is shown in figure 2.17. The circuit consists of an operational amplifier, two capacitors (C_1 and C_2) and switches.

32

The operation is two-step procedure. The first step is the sampling phase. Unity feedback is formed by turning on the switch 'F'. While unity feedback is formed, the reset voltage ($V_{RST} + V_N$) is sampled on C_1. In this phase, charge in each capacitor can be expressed as follows:

$$Q_1 = C1\{V_{REF} - (V_{RST} + V_N)\}$$
$$Q_2 = 0$$

(2.17)

The second step is the amplification phase. Unity feedback is removed by turning off 'F'. After the unity feedback is removed, the signal voltage from the pixel is input to C_1. Since the '-' input of the operational amplifier tries to keep the voltage V_{REF} due to the feedback through C_2, the charge variation from the new input $V_{SIG} + V_N$ is totally delivered into C_2. Now the charge in each capacitor can be expressed as follows:

$$Q_1 = C_1\{V_{REF} - (V_{SIG} + V_N)\}$$
$$Q_2 = C_2(V_{OUT} - V_{REF})$$

(2.18)

The output of the CDS circuit can be expressed as follows:

$$V_{CDS} = V_{REF} + \frac{C_1}{C_2}(V_{RST} - V_{SIG})$$

(2.19)

CDS circuits generate noise cancelled signal (V_{RST} - V_{SIG}). CDS circuits can be implemented to amplify the signal by making the capacitance of C_2 programmable (PGA, programmable gain amplification) [2.3]. Using the amplification by the gain A, the input-referred noise will be suppressed as $\sqrt{V_{N2}/A}$ where V_{N2} is the noise in the signal chain after the CDS circuit (mostly from the ADC). The variable capacitance can be

implemented with configurable capacitance of C_2. For example, C_2 can be implemented with

$$C_2 = C_1/8 + S_0C_1/8 + S_1C_1/4 + S_2C_1/2$$

$$A = 1: C_2 = C_1 \ (S_2S_1S_0 = \text{"111"})$$

$$A = 2: C_2 = C_1/2 \ (S_2S_1S_0 = \text{"110"})$$

$$A = 4: C_2 = C_1/4 \ (S_2S_1S_0 = \text{"100"})$$

$$A = 8: C_2 = C_1/8 \ (S_2S_1S_0 = \text{"000"})$$

The gain A is controlled globally, i.e., same gain is applied to entire pixel array. The amplified signals are input to the ADC, and this amplification suppresses the input referred noise.

The CDS circuit shown in figure 2.17 induces another FPN. The operational amplifier has the offset voltage from the mismatch of differential pair, i.e., there is voltage difference (V_{OFFSET}) to make each current in the differential pair same. When unity feedback is formed, the '-' input voltage will be $V_{REF} + V_{OFFSET}$. Since the CDS circuit is typically implemented with column parallel, each column generates different V_{OFFSET} and the output image will have vertical stripe pattern. This FPN can be cancelled by 2nd CDS in the ADC, i.e., ADC samples both $V_{REF} + V_{OFFSET}$ (when CDS is in sampling phase) and $V_{REF} + V_{OFFSET} + V_{SIG}$ and cancels each other. The result of 2nd CDS is desired signal V_{SIG}.

2.6 Analog-to-digital converter (ADC)

CMOS image sensors have integrated ADCs for the digital signal output. As shown in figure 2.18, there are two schemes to implement ADCs: serial ADCs and column-parallel ADCs.

2.6.1 Serial ADC

Serial ADCs convert the signal of entire pixels serially. One row of signals is read out to the line buffer, which is implemented with sample and hold circuit. The signals stored in the line buffer are accessed serially by the column scanner. Therefore, high-speed ADCs such as pipeline ADCs are required [2.12]. As the pixel array is scaled to the large format, the speed bottleneck in the ADC is a critical factor.
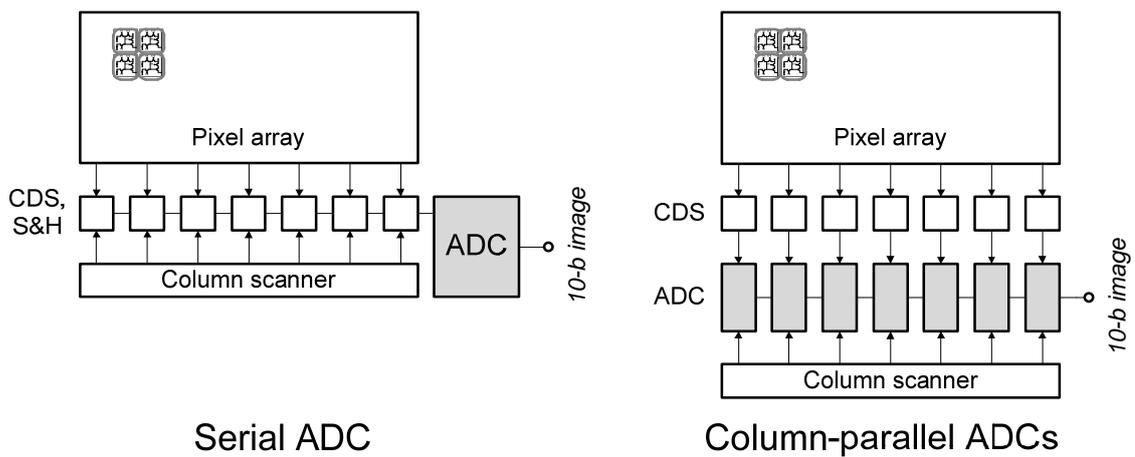
Figure 2.18 ADC schemes in CMOS image sensor.

2.6.2 Column-parallel ADC

Column-parallel ADCs convert the signal of one row in parallel. Cyclic ADCs, successive approximation (SAR) ADCs and single-slope (SS) ADCs are widely used for column-parallel ADCs [2.4]-[2.9]. Among them, SS ADCs are mostly widely used in CMOS image sensors.

35

Figure 2.19 shows the architecture and the operation principle of the SS ADC. Input voltage (V_{IN}) is compared with the ramp signal (RAMP). When ramp signal crosses the input voltage, the comparator output toggles and latches the counter value into the latch.

A single-slope ADC takes relatively small area because it requires only one comparator and latches. Moreover, it provides better linearity than cyclic or SAR ADC because the DAC output (ramp signal) is monotonously increased. The matching between columns is the most critical factor in column parallel ADCs. The SS ADC provides good matching because the ramp signal is globally applied to entire columns and the gain variation of the comparator is not so critical as long as the comparator has enough gain. The main drawback of SS ADCs is long A/D conversion time. For n-bit conversion, SS ADCs have 2^n clock cycles whereas SAR and cyclic ADC have n clock cycles.
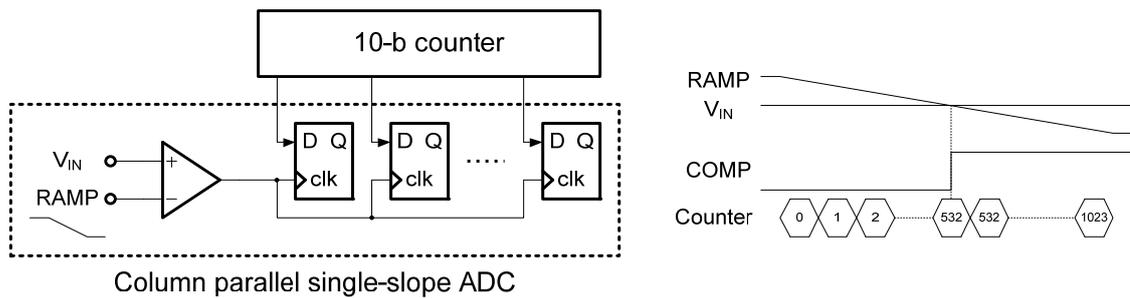
Figure 2.19 Single-slope ADC.

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CHAPTER 3 LOW POWER CMOS IMAGE SENSORS, DYNAMIC RANGE ENHANCEMENT AND EMBEDDED IMAGE SIGNAL PROCESSING

In this chapter, power consumption of CMOS image sensors will be estimated and power reduction strategy will be discussed. Then three categories of CMOS image sensors, which are essential for distributed imaging systems and biomedical sensors: (1) low-power CMOS image sensors, (2) wide-dynamic range & high-sensitivity CMOS image sensors and (3) CMOS image sensors with integrated image signal processing for bandwidth reduction. This chapter will introduce principles, challenges and previous works.

Since CMOS image sensors can be fabricated with CMOS process, power consumption can be scaled down compared with CCD image sensors. However, conventional CMOS image sensors still have large power consumption and they are difficult to be used with battery or with energy harvesting because applications of conventional image sensors are mostly 2nd generation imaging systems such as mobile devices. The SNR and the image quality have been a critical factors rather than power consumption. Moreover, voltage scaling has a limitation due to the signal range of the pixel.

In CMOS image sensors, a variety of circuits for image enhancement and processing can be integrated on a chip in order to implement camera-on-chip solutions. A dynamic range of conventional CMOS image sensors is around 60 dB, whereas the natural scene has more than 100 dB dynamic range. Therefore, high-sensitivity readout circuits and

dynamic range enhancement schemes should be integrated in order to provide a reliable monitoring.

A bandwidth is another critical factor because the image signal transmission with constant frame rate requires huge bandwidth. For bandwidth saving, lightweight image processing schemes such as the motion sensing or the region-of-interest (ROI) readout has been integrated in CMOS image sensors. These schemes process the signal from pixel arrays, and outputs events or features with low bandwidth.

3.1 Power consumption in CMOS image sensors

The block diagram of a CMOS imager for power estimation is shown in figure 3.1. In the typical approach, separate power supply between analog and digital block are used in order to achieve higher noise immunity.
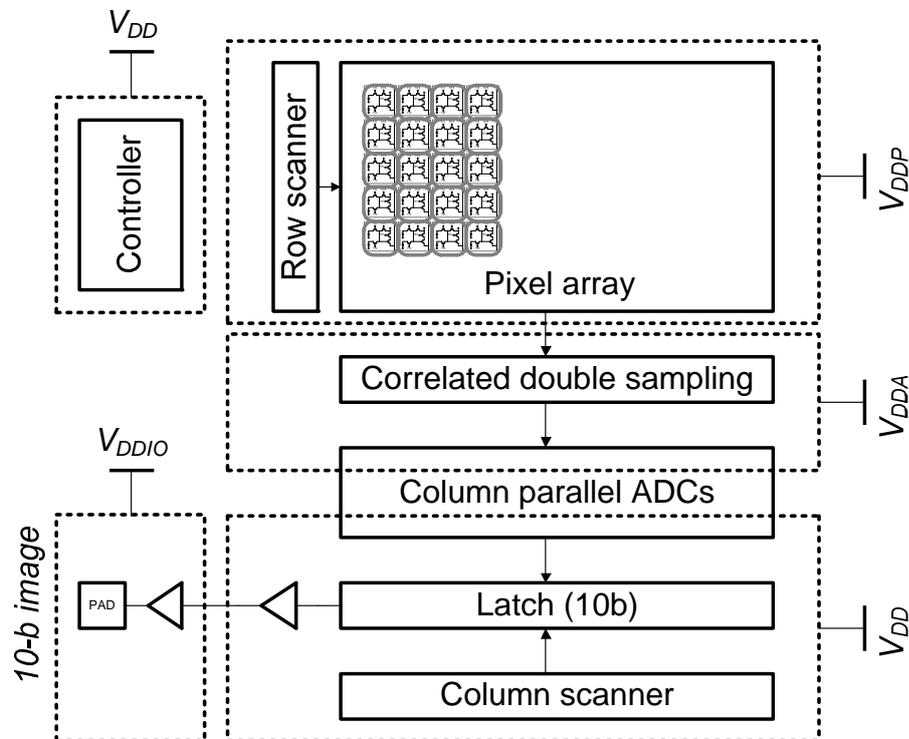
Figure 3.1 Block diagram of CMOS imager.

For the estimation, the analog power supply is further divided by two parts: pixel (V_{DDP}) and CDS/ADC circuit (V_{DDA}). The digital power supply can be further divided by two parts: the core including timing controllers and ADC digital circuits (V_{DD}) and I/O circuits (V_{DDIO}). In this section, power consumption in each block of CMOS imager will be estimated.

3.1.1 Power consumption: static, dynamic and leakage

The power consumption can be categorized into three: static, dynamic and the leakage power consumption [3.1].

Static power consumption

The static power consumption can be expressed as follows:

$$P_S = I_{AVG} \cdot V_{DD} \tag{3.1}$$

,where I_{AVG} is the average current and V_{DD} is the power supply voltage.

In imaging operation, most of static power consumption comes from the analog circuits including pixel arrays, CDS circuits, and also some part of ADCs (mostly from the comparators). These circuits repeat the operation row by row in rolling-shutter operation. The average current I_{AVG} can be calculated with the bias current and the duty cycle as follows:

$$I_{AVG} = I_{BIAS} \cdot \frac{\#_{ROW} \cdot T_{ON}}{T_{INT}} \cong I_{BIAS} \cdot \frac{T_{ON}}{T_{ROW}} \tag{3.2}$$

,where T_{ON} is the time that the circuit is activated. The row access time T_{ROW} can be defined as the time of one-row operation including the pixel readout, CDS (T_{CDS}), ADC (T_{ADC}), digital signal readout (T_{RD}) and blanking time before the next row operation. Assuming zero blanking time, the T_{ROW} can be expressed as:

$$T_{ROW} = T_{CDS} + T_{ADC} + T_{RD} \qquad (3.3)$$

Using Eq.3.3, the static power consumption of each circuit can be expressed as follows:

$$P_S = I_{BIAS}V_{DD}\frac{T_{ON}}{T_{ROW}} \qquad (3.4)$$

Dynamic Power Consumption

The dynamic power consumption in digital circuits consists of two components: one is from the load capacitor driving and the other is from the short circuit current during the transition. In a single gate, power consumption can be expressed as:

$$
\begin{aligned}
P_D &= C_L V_{DD}{}^2 f + t_{sc}V_{DD}I_{PEAK}f \\
&= C_L V_{DD}{}^2 f + C_{sc}V_{DD}^2 f \qquad (3.5) \\
&= (C_L + C_{SC})V_{DD}^2 f
\end{aligned}
$$

The first term shows the dynamic power from capacitor driving. C_L is the load capacitance of the gate and f is the frequency of transitions from '0' to '1'. The second term shows the dynamic power consumption from the short circuit current. t_{sc} represents the time of short circuit current generation, i.e., both pMOS and nMOS are turned on during the transition. I_{PEAK} is the peak short circuit current. In CMOS imagers, many digital circuits have to drive long metal line connected with each column circuits. In this case, total load capacitance (C_L) consists of load capacitance of each column circuit ($c_{l(col)}$) and also the parasitic capacitance of metal line (c_m) as follows:

$$\text{Eq. 3.6} \quad C_L = \#_{COL} c_{l(col)} + L c_m$$

$$\approx \#_{COL} \left\{ c_{l(col)} + W_{PIX} c_m \right\} \tag{3.6}$$

, where $\#_{COL}$ is the number of columns, L is the length of metal line, and c_m is the parasitic capacitance per unit length. The length L can be expressed as $\#_{COL} W_{PIX}$ where W_{PIX} is the pixel pitch. Some of digital circuits such as the counter in single slope ADCs and the clock generator operate with high frequency. Therefore, dynamic power consumption in CMOS imagers is dominated by the power consumption from the capacitor driving.

Leakage Power Consumption

When circuits are not operating, there is power consumption from the leakage current. The leakage current mainly comes from three components: sub-threshold (sub-V_T) current, junction leakage, and gate oxide tunneling [3.2]. In CMOS imagers, the leakage power consumption is more severe in digital circuits compared with analog circuits because digital circuits use thin-oxide transistor with low V_T for voltage scaling whereas analog circuits including pixels use thick-oxide transistor which allows higher voltage without breakdown in order to enhance the signal swing.

The sub-V_T current can be expressed as follows:

$$I = A e^{\left(\frac{1}{m V_T}\right)(V_{GS} - V_{T0} - \gamma' V_S + \eta V_{DS})} \left(1 - e^{-\frac{V_{DS}}{V_T}} \right) \tag{3.7}$$

, where η is the drain-induced-barrier-lowering (DIBL) coefficient and γ' is linearized body effect coefficient. As long as drain-source voltage (V_{DS}) is not zero, the sub-V_T current flows even when the gate-source voltage V_{GS} is zero. Note that low V_T

significantly increases the sub-V_T leakage in the exponential form. In short channel devices in digital circuits, the DIBL which lowers V_T increase the sub-V_T current.

The junction leakage is from the reverse-biased p-n junctions. The most significant factor of junction leakage is from the band-to-band tunneling (BTBT). Due to high electric field from revere biased p-n junctions, electrons tunnel from the valence band (p region) to the conduction band (n region).

The gate leakage current is from the gate oxide tunneling. High electric field across the SiO_2 makes electrons in the inverted silicon surface tunnel directly to the gate. This gate tunneling is more noticeable in the thin-oxide transistors.

Typically, leakage power consumption is much lower and is not comparable to static and dynamic power consumptions in conventional CMOS imagers. However, some of low-power imagers operate in the sub-V_T region with scaled V_{DD}. In this case, leakage power is an important factor in order to achieve minimum energy [3.3]. The low-power CMOS imagers using sub-V_T readout circuits will be introduced in section 3.2.

3.1.2 Power Consumption in the Image Signal Chains

In this section, power consumption in main blocks of image signal chains will be estimated. A signal chain of CMOS imagers is shown in figure 3.2. The operation timing diagram is shown in figure 3.3. The main parameters for power estimation are shown in table 3.1. In the estimation of dynamic power consumption, we consider the dynamic power consumption only from the capacitive driving ($C_L V_{DD}^2 f$) for simplicity. Moreover, the leakage power consumption will be ignored. This estimation causes error compared with actual dynamic power consumption. However, main purpose of power estimation in this section is to get power reduction strategy by inspecting the tendency of power

consumption according to critical parameters such as the number of pixel array, power supply voltage and pixel pitch. In this section, we will show only estimated equation without detailed derivation for digital circuit blocks. Detailed estimation of dynamic power consumption in digital circuit blocks will be shown in Appendix A.

Pixel Array

The circuit schematic of pixels in one column is shown in figure 3.4. The load capacitance of in-pixel source follower consists of junction capacitance of selection transistor, column line (SIG) parasitic capacitance and sample and hold capacitance (C_S). The sample and hold capacitor is a part of CDS circuits. The load capacitance of in-pixel source follower can be calculated as follows:

$$C_{SIG} = \#_{ROW}c_j + \#_{ROW}W_{PIX}c_m + C_S \tag{3.8}$$

The gain-bandwidth product (GB) of the amplifier is:

$$GB = f = \frac{g_m}{2\pi C_{SIG}} = \frac{\sqrt{2\beta I_{BIAS}}}{2\pi C_{SIG}} \tag{3.9}$$
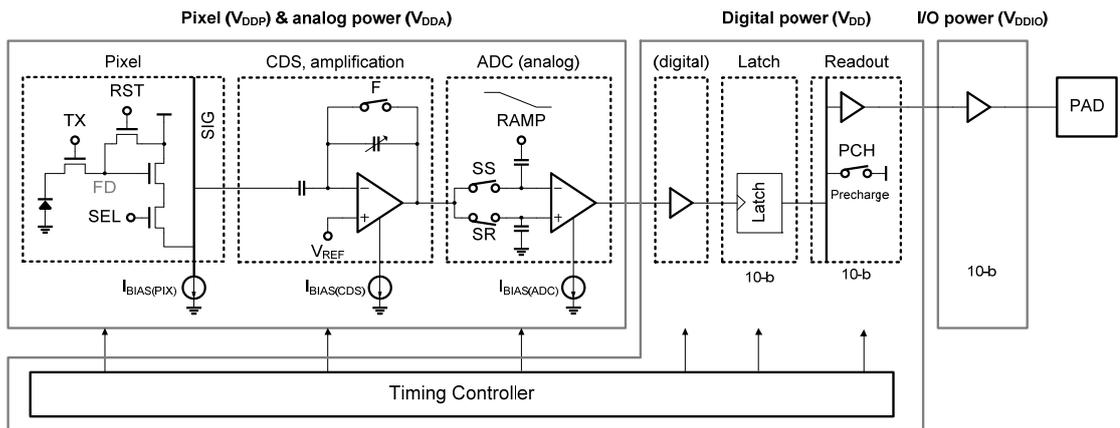
Figure 3.2 Signal chain of CMOS imager.
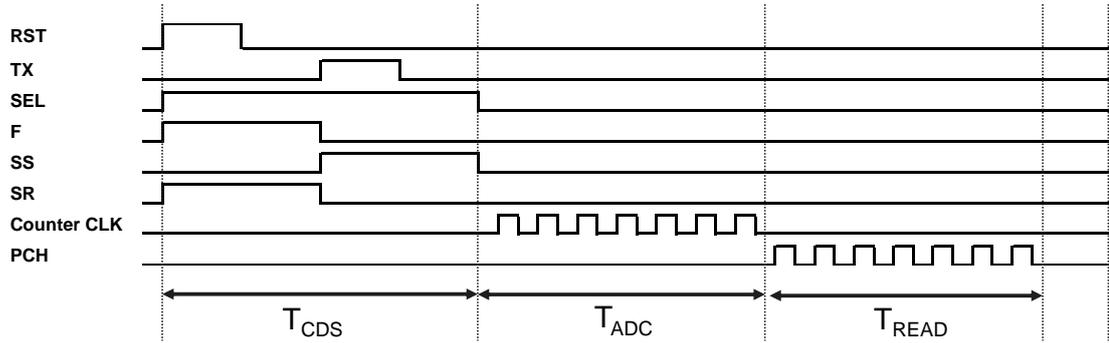
Figure 3.3 Signal chain of CMOS imager

Pixel array	$\#_{COL} \times \#_{ROW}$	320 × 240 (QVGA)
Pixel pitch	W_{PIX}	5 um
Frame rate	$FR = 1/T_{INT}$	30 fps
Integration time	T_{INT}	33.3 ms
Row access time	$T_{ROW} = 1/(FR \cdot \#_{ROW})$	139 μs
CDS time	T_{CDS}	8 μs
ADC time	$T_{ADC} = T_{CLK} \cdot 2^N$	99.7 μs
Digital signal readout time	$T_{READ} = T_{CLK} \cdot \#_{COL}$	31.2 μs
ADC resolution	N	10 bit
Pixel power supply	V_{DDP}	2.8 V
Analog power supply	V_{DDA}	2.8 V
Digital power supply	V_{DD}	1.8 V
I/O power supply	V_{DDIO}	1.8 V
Clock frequency (period)	f_{CLK} (T_{CLK})	10 MHz (100 ns)
Process transconductance parameter	K	50 uA/V^2
Capacitance of capacitors in CDS, ADC circuit	C_S, C_F	1 pF
Gate capacitance of transistor (minimum W/L)	c_g	0. 5 fF
Input capacitance of inverter (×1)	$3c_g$	1.5 fF
Parasitic capacitance of metal line (per unit length)	c_m	0.5 fF

Table 3.1 Parameters for the estimation of power consumption
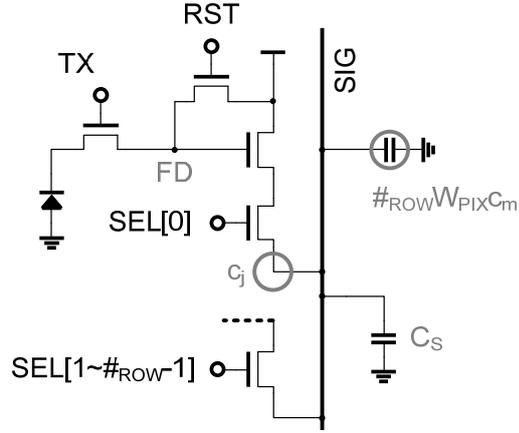
Figure 3.4 Pixel circuit with load capacitance of in-pixel source follower

For 1% settling, the 3-dB bandwidth should be 4.6 times larger than the pole frequency. Therefore, we assume that the time constant is 5 times smaller than the required time slot (T). Then the 3-dB bandwidth of in-pixel source follower can be shown as Eq.3.10.

$$f_{SF} = \frac{5}{0.5 \cdot T_{CDS}} = \frac{\sqrt{2\beta I_{PIX}}}{2\pi C_{SIG}} \tag{3.10}$$

In Eq. 3.10, the sampling time is set as $0.5T_{CDS}$ because two signals have to be sampled for the correlated double sampling. The source follower needs to be turned on during the CDS time. Considering the duty cycle (T_{CDS}/T_{ROW}), the power consumption of pixel arrays can be calculated as Eq.3.11.

$$\text{Eq. } 3.11 \quad P_{PIX} = \#_{COL} I_{PIX} V_{DDP} \frac{T_{CDS}}{T_{ROW}}$$

$$= \#_{COL} \left\{ \frac{(20\pi C_{SIG})^2}{2\beta \cdot T_{CDS}^2} \right\} V_{DDP} \frac{T_{CDS}}{T_{ROW}} \tag{3.11}$$

Column-parallel CDS Circuit

The CDS circuit consists of the programmable gain amplifier (PGA) with capacitive feedback as shown in figure 3.5. The PGA consists of one OTA, one input sampling capacitor (C_S) and programmable feedback capacitors (C_F). In figure 3.5, the gain of PGA (A_{PGA}) can be set up to 8 as an example. The 3-dB frequency of the CDS circuit can be described as:

$$f_{CDS} = \frac{5}{0.5 \cdot T_{CDS}} = \frac{1}{A_{PGA}} \cdot \frac{\sqrt{2\beta(0.5I_{CDS})}}{2\pi(2C_S)} \qquad (3.12)$$

The power consumption of the CDS circuit can be calculated as Eq.3.13.

$$P_{CDS} = \#_{COL}I_{CDS}V_{DDA}\frac{T_{CDS}}{T_{ROW}}$$

$$= \#_{COL}\left\{\frac{(40A_{PGA}\pi C_S)^2}{\beta \cdot T_{CDS}^2}\right\}V_{DDA}\frac{T_{CDS}}{T_{ROW}} \qquad (3.13)$$
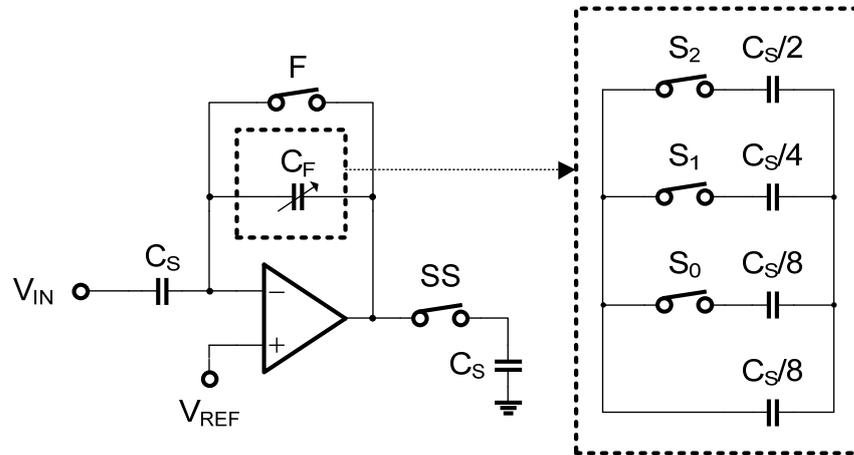
Figure 3.5 Correlated double sampling circuit with programmable gain amplification

Column-parallel Single-slope ADC

The single slope ADC consists of one comparator and latches. The latch can be implemented with SRAMs, D flip-flops or sometimes counter circuits. The power

48

consumption of the single-slope ADC is dependent on the topology of the comparator and the latch. In this estimation, one common topology that consists of a static preamplifier, a dynamic comparator and a 10-b D flip-flop will be analyzed as shown in figure 3.6. The clock frequency of counter in the single-slope ADC is determined by the number of pixels and also by the frame rate. The A/D conversion time (T_{ADC}) can be determined as Eq.3.14.

$$T_{ADC} = T_{ROW} - T_{CDS} - T_{READ} \qquad (3.14)$$

Note that there is an additional time budget for the digital signal readout (T_{READ}) because no additional line memories to store one row of image signals. With line memories, the ADC output will be stored in the line memory and the signal readout can be done while the next ADC cycle is performed.
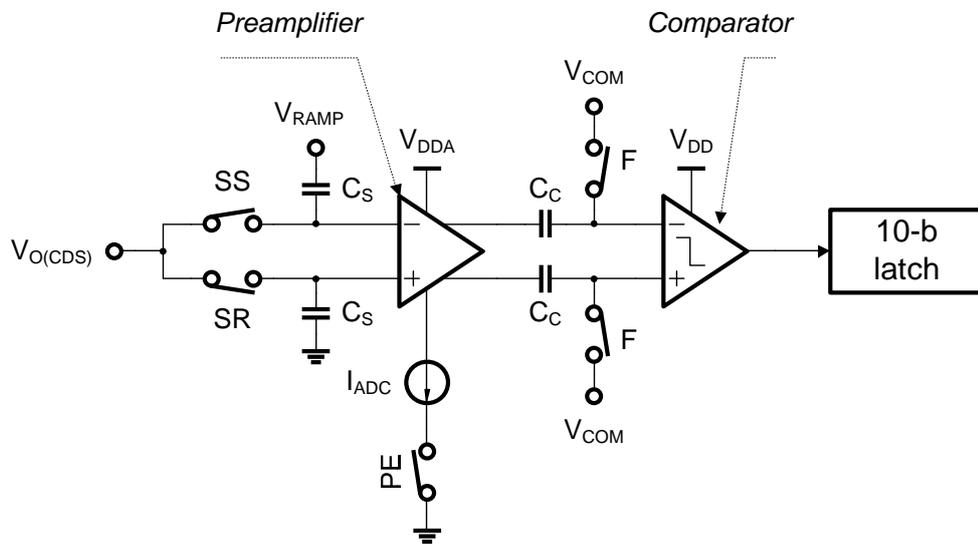
Figure 3.6 Column-parallel single-slope ADC

The A/D conversion time can be expressed with required clock period (T_{CLK}) and the frequency (f_{CLK}) as Eq.3.15.

$$f_{CLK} = \frac{1}{T_{CLK}} = \frac{2^N + \#_{COL}}{\frac{1}{FR \cdot \#_{ROW}} - T_{CDS}} \qquad (3.15)$$

A. Comparator: Preamplifier

The main role of a preamplifier is to suppress the offset voltage of dynamic comparators by providing a high gain. The offset voltage of the preamplifier can be suppressed by another CDS operation in the ADC. Therefore, the gain of the preamplifier is determined by the offset voltage of dynamic comparator. Assuming one LSB is 1 mV and the offset voltage of the dynamic comparator is 10 mV, the gain of the preamplifier (A_{PA}) over 10 guarantees the offset error under 1 LSB. In this estimation, the differential amplifier with diode-connected loads will be used as shown in figure 3.7.

The bandwidth of a preamplifier is determined by the clock frequency f_{CLK}. It is desirable to design the delay of a preamplifier under T_{CLK} in order to latch the counter signals within 1 LSB range, i.e., keep the bandwidth of the preamplifier over f_{CLK}. The 3-dB bandwidth of the preamplifier is:

$$f_{preamp} = f_{CLK} = \frac{1}{A_{PA}} \cdot \frac{g_m}{2\pi C_L}$$
$$= \frac{1}{A_{PA}} \cdot \frac{\sqrt{2\beta(0.5 I_{ADC})}}{2\pi C_L} \qquad (3.16)$$

The load capacitance (C_L) of the preamplifier includes the gate capacitance of load transistors and the gate capacitance of the dynamic comparator. Assuming total load capacitance (C_L) is $16c_g$, the power consumption of the preamplifier can be calculated as:

50

$$P_{PREAMP} = \#_{COL} \left\{ \frac{\left(32 A_{PA} \pi f_{CLK} c_g\right)^2}{\beta} \right\} V_{DDA} \frac{T_{CDS} + T_{ADC}}{T_{ROW}} \tag{3.17}$$
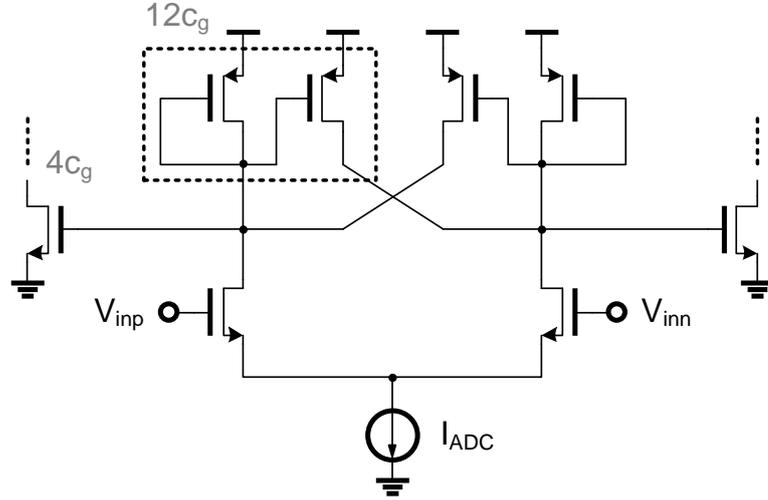
Figure 3.7 Preamplifier in the single-slope ADC

B. Comparator: Dynamic Comparator

The dynamic comparator performs the level decision from pre-amplified signals. It operates with two phases: the precharge and the comparison. Figure 3.8 shows the comparator circuit. The first stage that consists of a latch circuit, switches (pMOS for precharge), and inverters contributes to the power consumption in each clock cycle. The 2nd stage that consists of a RS latch and buffers has only one time switching during the ADC time. For simplicity, we consider only the gate capacitance for total load capacitances. The power consumption per one comparator (per column) can be expressed as Eq.3.18.

$$P_{COMP} = 6 c_{inv} V_{DD}^2 \frac{2^N}{T_{ROW}} + 12 c_{inv} V_{DD}^2 \frac{1}{T_{ROW}} \tag{3.18}$$
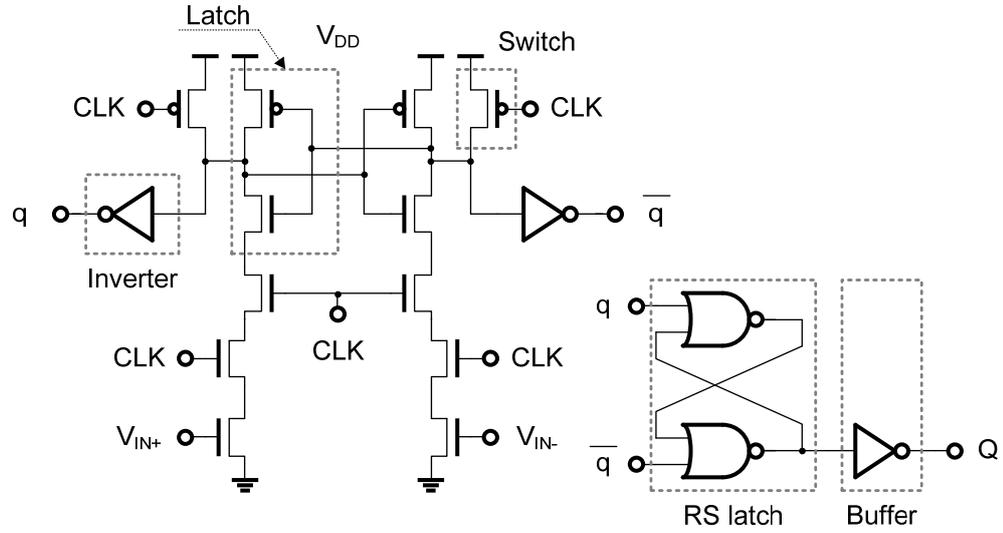
Figure 3.8 Dynamic comparator

C. Latches & counter

The latch for the N-bit single-slope ADC consists of N D flip-flops. The circuit schematic of the D flip-flop is shown in figure 3.9. Note that the clock signal (CK) is from the comparator output (Q) and the input signal (D) is from the counter. The comparator output has the frequency $1/T_{ROW}$ and the counter output has different frequency according to the bit position. The power consumption of one latch in the single-slope ADC can be represented as follows:

$$P_{D\_FF} = \left(13c_{inv} + c_g\right)V_{DD}^2 \frac{1}{T_{ROW}} + 5c_{inv}V_{DD}^2 \frac{f_{CNT(n)}}{T_{ROW}} \qquad (3.19)$$

,where $f_{CNT(n)}$ is the counter output frequency of n-th bit position. As shown in Eq.3.19, the power consumption of two inverters in the master stage of the latch is dependent on the input frequency, i.e., counter output frequency $f_{CNT(n)}$. In the single-slope ADC, when the clock signal is low, the master stage continuously changes its state from the counter signals. After the clock signal goes high and the counter signal is latched to the slave stage, no more switching occurs. The power consumption is dependent on the output

toggling from the comparator. Therefore, the power consumption is largely dependent on the signal level (i.e., light intensity) of single slope ADCs. In this estimation, we define the illumination level parameter 'I' which varies $1/2^N$ (dark) to 1 (bright). For The power consumption of the N-bit latch in single slope ADCs which uses a Gray counter can be expressed as follows:

$$P_{LATCH} = \#_{COL}\{N(13c_{inv} + c_g) + 5c_{inv}I(1 + 1 + 2$$
$$+ \cdots + 2^{N-2})\}V_{DD}^2 \frac{1}{T_{ROW}} \tag{3.20}$$

Note that the 2nd term includes the illumination level parameter 'I'. If the signal level is high from high illumination, the power consumption increases because the latch has more switching before the comparator output is toggled.
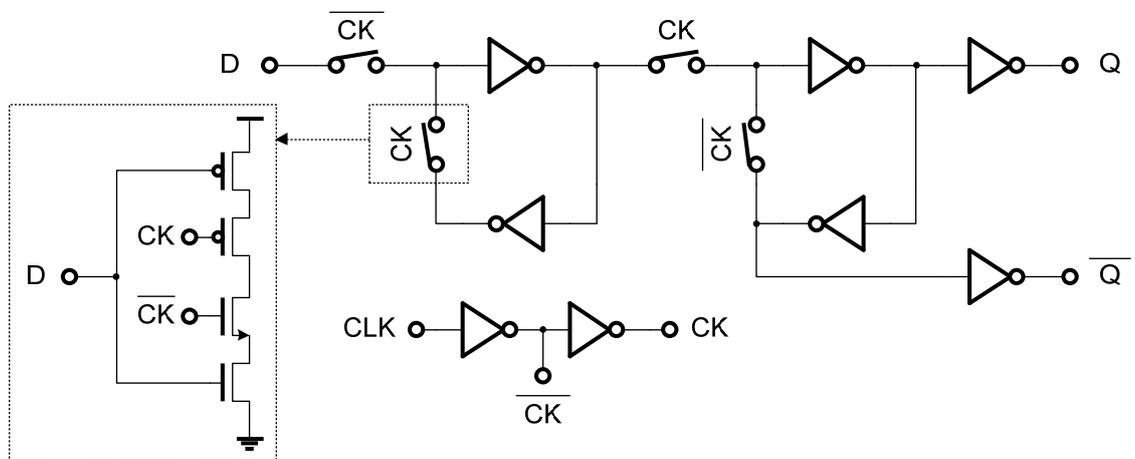
Figure 3.9 D flip-flop

Compared with a binary counter, a Gray counter provides better noise immunity because the output change occurs only in one bit position, i.e., timing jitter induces only 1 LSB error. Another advantage is low power consumption because total number of

53

switching is half of the binary counter. Detailed power estimation will be shown in appendix A. The overall power consumption from the counter can be expressed as:

$$P_{CNT} = (39c_{inv} + 0.5\#_{COL}W_{PIX}c_m)$$

$$\times V_{DD}^2 \frac{1 + 2 + \cdots + 2^{N-1}}{T_{ROW}} \qquad (3.21)$$

Digital signal readout

Figure 3.10 shows the digital signal readout circuit and the operation. The output of the 10-b latch drives the readout buffer. The readout buffer of all columns share one sense line (SL). The sense line is precharged with V_{DD} first. The column selection signal CS from the column scanner is enabled column by column. When stored digital signal is '1', the readout buffer draws the current from the precharged sense line and the voltage of the sense line is dropped. The sense amplifier senses the voltage drop of the sense line.
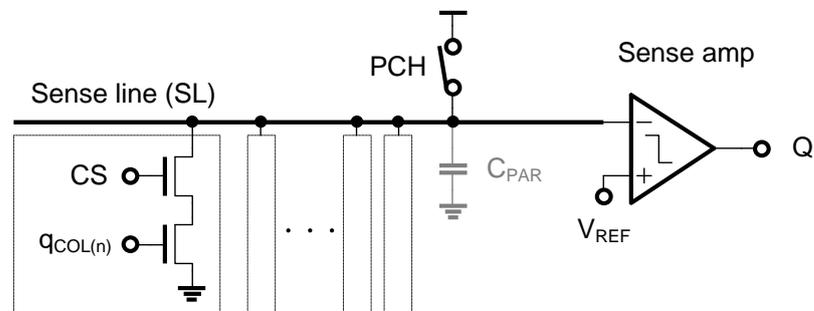
(a) Digital signal readout circuit
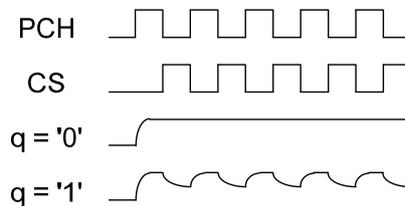
(b) Operation

Figure 3.10 Digital signal readout circuit and the operation

54

The power consumption occurs from two parts: precharge switches and sense amplifiers. The power consumption from the precharge switches is shown in Eq. 3.22.

$$P_{switch} = N\#_{COL}W_{PIX}c_mV_{DD}^2 \frac{\#_{COL}}{T_{ROW}} \tag{3.22}$$

In Eq. 3.22, we assumed V_{DD} swing of the sense line. We also assumed the worst case and all sense line voltage drops. Using the same dynamic comparator as in the single-slope ADC, the power consumption from sense amplifiers is:

$$P_{amp} = 18c_{inv}V_{DD}^2 \frac{\#_{COL}}{T_{ROW}} \tag{3.23}$$

The total power consumption from the digital signal readout is:

$$P_{READ} = \{N\#_{COL}W_{PIX}c_m + 18c_{inv}\}V_{DD}^2 \frac{\#_{COL}}{T_{ROW}} \tag{3.24}$$

Periphery circuits

A. Column scanner

In this estimation, a simple shift register instead of a decoder will be used for both the column and the row scanner. The column scanner requires $\#_{COL}$ shifting operation per one row time. The detailed power estimation will be shown in appendix A. The total power consumption from the column scanner is shown in Eq. 3.25:

$$P_{CS} = (12.5c_{inv} + 0.5Nc_g)V_{DD}^2 \frac{\#_{COL}^2}{T_{ROW}} \tag{3.25}$$

B. Row scanner

The row scanner consists of a shift register and drivers as shown in figure 3.11. The row scanner requires $\#_{ROW}$ shifting operation per one frame. In each row, the row scanner consists of one flip flop, three NAND gates, three level-up converters and three inverters. The NAND gate enables the pixel control signals (TX, R, S) according to the control signals (TXG, RG, SG). Since the pixel power supply is higher than digital power supply (V_{DD}), level-up converter is required to control the pixel circuit. The total power consumption of the $\#_{ROW}$-bit shift register is as follows:

$$P_{RS} = \{7c_{inv}\#^2_{ROW} + 20c_{inv}\}V^2_{DD}\frac{1}{T_{ROW}}$$

$$(3.26)$$

$$+\{6c_{inv} + \#_{COL}(W_{PIX}c_m + c_g)\}V^2_{DDH}\frac{1}{T_{ROW}}$$
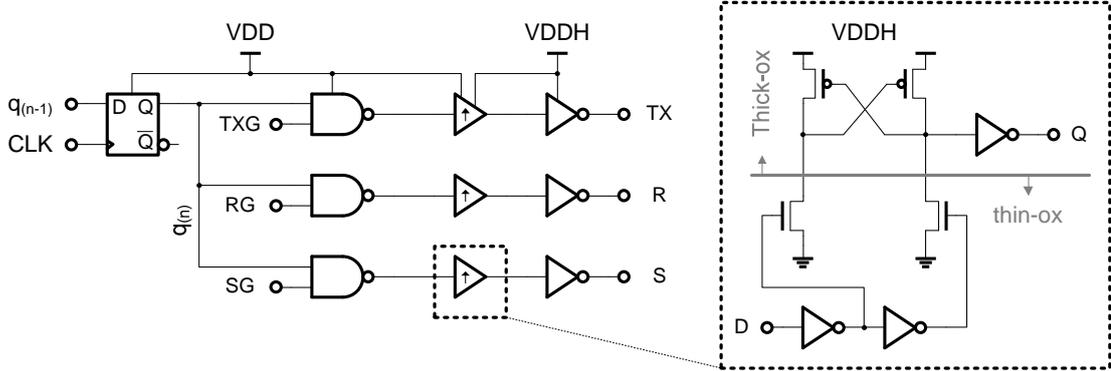
Figure 3.11 Row scanner

C. Timing generator

Simple timing generator consists of two counters: one is the horizontal counter (H-counter, assume N+1 bit counter) for column-wise operations and the other is the vertical counter (V-counter) for row-wise operations. Additional logic gates and registers are included for the signal generation. For simplicity, only the power consumption of two

counters will be estimated. The power consumption of binary ripple counter has shown in appendix A. The power consumption of two counters is as follows:

$$P_{H-counter} = 22c_{inv}(1 + 2 + \cdots + 2^N)\frac{1}{T_{ROW}}V_{DD}^2 \qquad (3.27)$$

$$P_{V-counter} = 22c_{inv}(1 + 2 + \cdots + 2^{X-1})\frac{1}{T_{INT}}V_{DD}^2 \qquad (3.28)$$

,where X is $\log_2[\#_{ROW}]$.

From Eq.3.27 and 3.28, the total power consumption from the timing generator is roughly estimated as shown in Eq. 3.29.

$$P_{TG} \approx 22c_{inv}(1 + 2 + \cdots + 2^N)\frac{1}{T_{ROW}}V_{DD}^2$$
$$\qquad (3.29)$$
$$+22c_{inv}(1 + 2 + \cdots + 2^{X-1})\frac{1}{T_{INT}}V_{DD}^2$$

I/O circuit

IO circuit includes the ESD protection circuit and drivers. Typically the strength of driving can be controlled according to the register values. Accordingly, the power consumption varies from the driving capability. In this estimation, the driver that has simple two-stage inverter chain will be estimate. The most power-consuming I/O pad is the clock signal pad, and the next is digital output pad. The power consumption from the clock signal and digital output pad are shown in Eq. 3.30 and Eq. 3.31 respectively.

$$P_{I/O(CLK)} = (16c_{inv} + C_{PAD})f_{CLK}V_{DD}^2 \qquad (3.30)$$

$$P_{I/O(DOUT)} = (16c_{inv} + C_{PAD})(1 + 2 + \cdots$$

$$+ 2^{N-1})\frac{1}{T_{ROW}}V_{DD}^2 \tag{3.31}$$

From Eq.3.30 and Eq.3.31, we roughly estimate the I/O power consumption as shown in Eq. 3.32.

$$P_{IO} \approx (16c_{inv} + C_{PAD})f_{CLK}V_{DD}^2$$

$$+(16c_{inv} + C_{PAD})(1 + 2 + \cdots + 2^{N-1})\frac{1}{T_{ROW}}V_{DD}^2 \tag{3.32}$$

3.1.3 Overall Power Consumption

Using the power consumption equations derived in the previous section, we can estimate the overall power consumption. Figure 3.12 shows the power consumption from each power supply voltage.
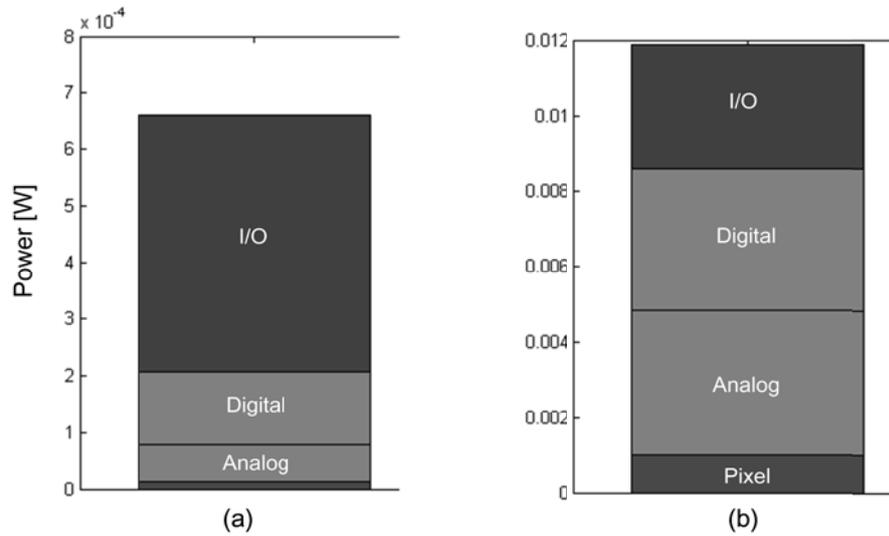
Figure 3.12 Overall power consumption in the signal chain according to the spatial resolution (a) 320×240 (b) 1280×960

The power consumption from the I/O circuits takes significant portion in the small number of pixel arrays (320 × 240) due to the large capacitance of I/O circuits. As the number of pixel increases, the parasitic capacitance of metal lines and the column-parallel circuits increase, therefore, relative portion of the I/O power consumption decreases. Figure 3.13 and 3.14 shows detailed power consumption from the analog power supply (V_{DDA}). In the analog power consumption, the portion of the ADC power increases in the large pixel arrays. This is because the CDS time (T_{CDS}) is fixed according to the charge transfer time in the pixel. Moreover, the load capacitance of CDS circuit is fixed with sampling capacitance. The only factor related with the number of pixels is the row time (T_{ROW}) as shown in Eq. 3.13. In the ADC power, the clock frequency f_{CLK} increases according to the number of pixels as shown in Eq.3.15.
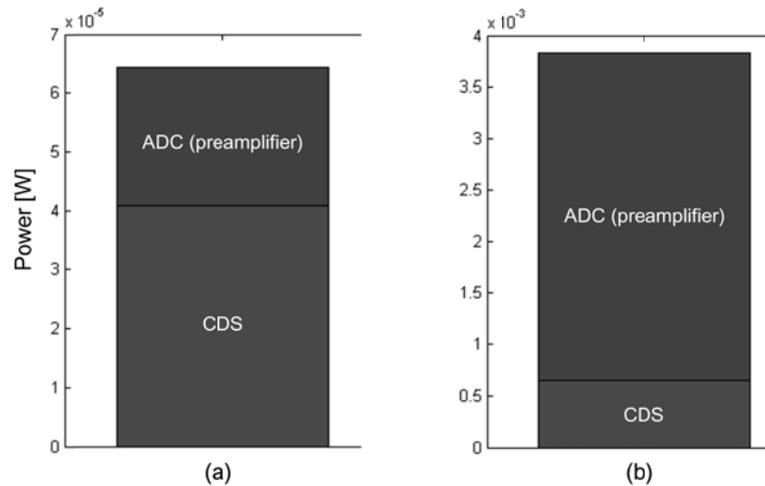
Figure 3.13 Analog power consumption in the signal chain according to the spatial resolution (a) 320 × 240 (b) 1280 × 960
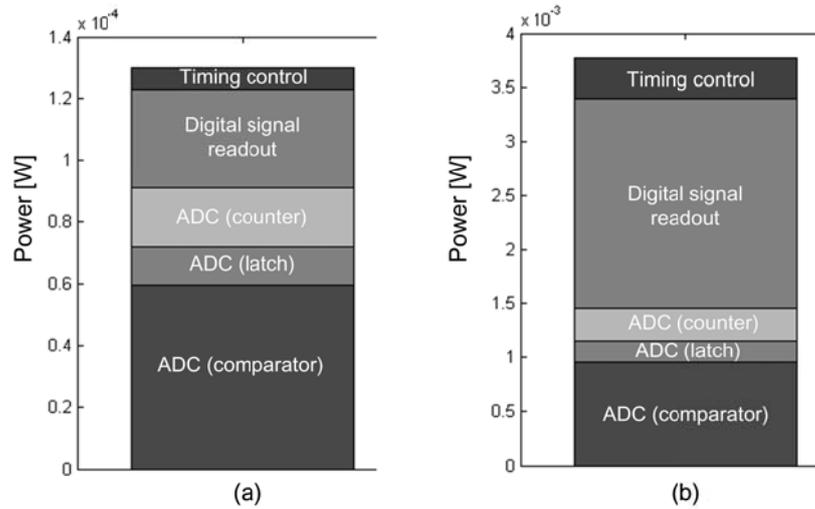
Figure 3.14 Digital power consumption in the signal chain according to the spatial resolution (a) 320 × 240 (b) 1280 × 960

Figure 3.14 shows detailed power consumption from the digital power supply (V_{DD}). As the number of pixel increases, the portion of power consumption from digital signal readout increases. This is because the power consumption from the digital signal readout has three factors that are increased according to the number of pixels: number of circuits (number of columns), load capacitance, and frequency.
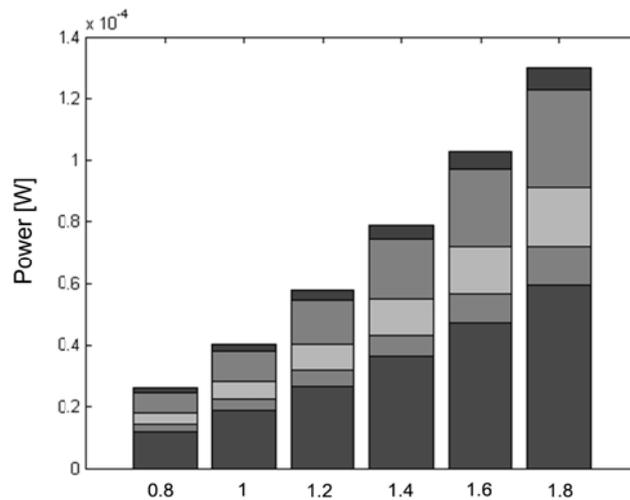
Figure 3.15 Digital power consumption according to the power supply voltage (320 × 240)
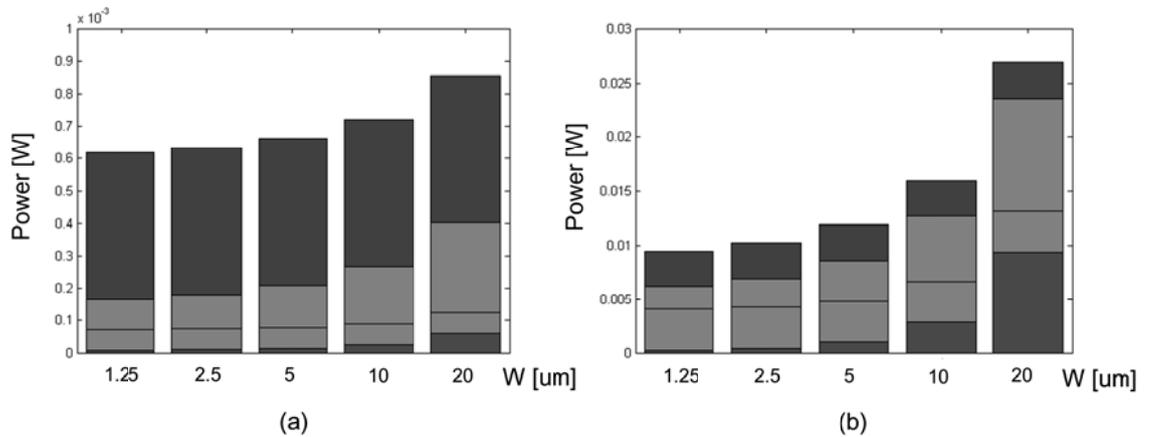
Figure 3.16 Overall power consumption according to the pixel pitch
(a) 320 × 240 (b) 1280 × 960

Figure 3.15 shows the effect of voltage scaling (V_{DD} = 0.8~1.8 V) in the digital power consumption. As expected, 1/2 scaling induces around 1/4 power reduction. Figure 3.16 shows the power consumption according to the pixel pitch. As pixel pitch increases, the pixel power consumption increases due to the increase of signal line parasitic capacitance.

3.1.4 Low-power design strategy

From the power estimation in previous sections, we can get several conclusions and power reduction strategies for low-power CMOS image sensors.

(1) Voltage scaling: obviously we have to use voltage scaling in both analog and digital blocks. In the case of digital circuits, the voltage scaling is effective because the power consumption is dependent on V_{DD}^2. Since the operation frequency is below 10 MHz in low resolution CMOS imager (< 320 × 240), which is applicable to the low-power wireless sensor node, we can easily achieve sub-1V power supply. However, the voltage scaling of the pixel and the analog power supply directly affects the SNR due to reduced signal ranges. Therefore, it is desirable to implement alternative pixel circuits and CDS circuits which are less vulnerable to the voltage scaling. In chapter 4, a low-power imager

61

employing the reconfigurable pixel architecture with reduced power supply will be discussed.

(2) Suppression of unnecessary switching: we can reduce the power consumption by reducing unnecessary switching activities. For example, the latch circuit in the single-slope ADC continuously changes the state before the comparator output is toggled. Another example is the precharging circuit. Whenever the digital signal has '0' value, the sense line voltage drops and dynamic current is drawn in the precharge operation. In chapter 4, we proposed several techniques in order to suppress redundant switching.

(3) Bandwidth reduction: The image sensor has high spatial-temporal resolutions and the I/O power takes more than 50% of total power consumption as shown in figure 3.12. In chapter 5, the bandwidth reduction scheme using embedded image processing algorithm will be explained.

(4) Small pixel size: As shown in figure 3.16, the power consumption increases according to the pixel size due to increased parasitic capacitance. In order to achieve low-power readout and an additional functionality, many low-power image sensors use additional in-pixel circuits, which increase the pixel size. In chapter 4 and chapter 5, a proposed low-power readout scheme with small pixel size will be explained.

3.1.5 Power consumption figure-of-merit (FOM)

Figure 3.17 shows the power consumption according to the spatial resolutions.

The power consumption is not increased linearly according to the resolution because of periphery circuits. However, the tendency is almost linear because the portion of power consumption from the periphery circuit is not so high. One of way to show the overall power consumption regardless of spatial-temporal resolution is the power FOM:

$$\text{FOM} = \frac{\text{Total power consumption}}{\# \text{ of pixels } \times \text{Frame rate}} \left[\frac{\text{pW}}{\text{pixels} \cdot \text{frame}} \right]$$
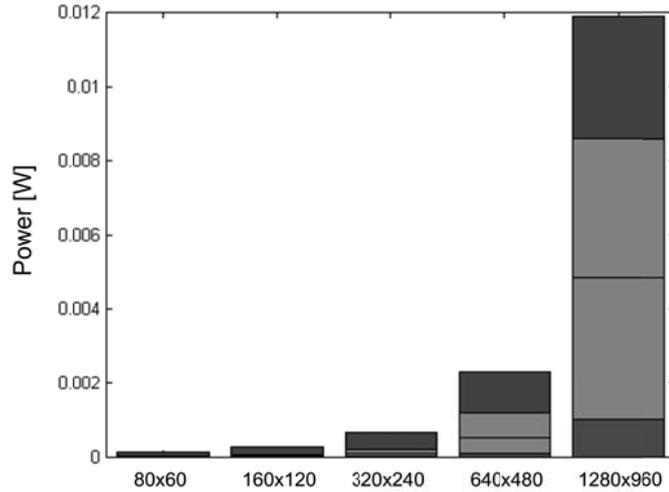
Figure 3.17 Overall power consumption according to the resolutions

In this thesis, we will utilize this power FOM for the power comparison. Since this power FOM does not reflect any SNR degradation, we will use additional FOM, which reflects SNR in chapter 4.

	Resolution	Frame rate	Supply Voltage	Power consumption	FOM
STMicroelectronics [3.4]	1280 x 1024	15 fps	2.8V (analog) 1.8V (digital)	75 mW (analog) 4.5 mW (digital)	4043
Cannon [3.5]	1944 x 1452	60 fps	Not shown	220 mW	1299
Aptina [3.6]	640 x 480	30 fps	Not shown	17 mW	1845
Samsung [3.7]	4400 x 3300	30 fps	2.8V (analog) 1.2V (digital)	512 mW	1175

Table 3.2 Power consumption of conventional CMOS image sensors

3.2 Low Power CMOS Image Sensors

Table 3.2 shows the power consumption and the power FOM of conventional CMOS image sensors. As shown in the table, the power consumption of conventional CMOS

imagers is over 30 mW in most cases. The applications of these sensors are mostly digital still cameras, cell phones, and automobiles. For the application of distributes sensors which are operated by batteries or energy harvestings, the power consumption of conventional sensors is too large to guarantee long lifetime of sensor nodes. Table 3.3 shows the power delivery from the energy harvesting. According to this table, in an overcast day (1,000 lx illumination), available power from the 3×3 mm^2 solar cell (150 pW/mm^2·lx) is only 1.35 µW. This power delivery requires 135 pW/pixel·frame FOM with 100×100 image sensor (@ 1 fps). This power budget is definitely small for conventional CMOS image sensors. Therefore, we need alternative approaches in order to implement a low power CMOS image sensor.

3.2.1 Limitation of Voltage Scaling

The most efficient way to scale the power consumption is the voltage scaling. However, the voltage scaling has limitations due to the SNR degradation. Figure 3.18 shows the signal ranges in the 4-T pixel architecture. The maximum and the minimum signal in the source follower output and in the FD can be expressed as follows:

$$(3.33)$$

(a) $V_{OUT(MAX)} = (V_{DD} - V_{THR}) - V_{TH}$: reset transistor's and source follower's V_T drop

(b) $V_{OUT(MIN)} = V_{DSsat}$: bias current transistor in saturation

(c) $V_{FD(MAX)} = V_{DD} - V_{THR}$: reset transistor's V_T drop

(d) $V_{FD(MIN)} = V_{DSsat} + V_{THR}$: source follower's V_T drop

From the equation 3.33(c) and 3.33(d), the maximum signal swing in the FD is

$$\Delta V_{FD} < (V_{DD} - V_{THR}) - (V_{DSsat} + V_{TH}) \qquad (3.34)$$

64

Vendor	Illuminance	Output Power	Size	Power / mm²·lx
Cymbet [3.8]	200 lx	80 uW	3000 mm² (estimated)	133.3 pW
	1000 lx	350 uW	3000 mm² (estimated)	116.7 pW
Cymbet [3.8]	Sunny	0.08 uW	0.07 mm²	5.7 nW
Clare [3.9]	6000 lx (direct sunlight)	200 uW	3.25 mm² (estimated)	10.3 nW
Enocean [3.10]	200 lx	13.5 uW	448 mm²	150.6 pW

Illumination condition	Full moon on a clear night	Dark overcast day	Overcast day	Full daylight
Illuminance [3.11]	1	100	1,000	10,000

Table 3.3 Solar energy harvesting example

Then, the minimum power supply can be calculated from Eq. 3.35.

$$\text{(a) } V_{DD} > \Delta V_{FD} + V_{THR} + V_{DSsat} + V_{TH}$$

$$\text{(3.35)}$$

$$\text{(b) } V_{DD} > \Delta V_{FD} + V_{DSsat} + 2V_T \ (V_T = V_{THR} = V_{TH})$$
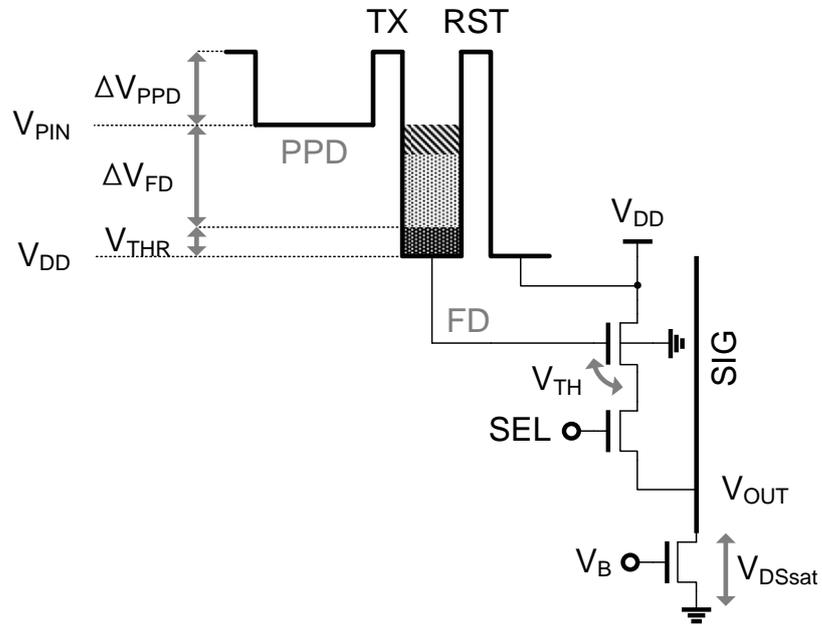
Figure 3.18 Signal range in the 4-T pixel

As shown in Eq. 3.35 (b), the minimum power supply voltage is "signal swing + V_{DSsat} + two V_T drop". This means that the voltage scaling reduces the signal swing, accordingly reduces the SNR. Assuming V_T = 0.8 V, V_{DSsat} = 0.2 V, and signal swing ΔV_{FD} is 1V (for 10-b resolution, 1 mV LSB), then minimum power supply voltage is 2.8 V. Note that contemporary CMOS image sensors use 2.8 V for the pixel & analog power supply voltage.

Another factor to limit the voltage scaling is the charge injection and the clock feed-through in the reset transistor as shown in figure 3.19. When the reset transistor is turned off, the voltage of FD is less than $V_{DD} - V_{THR}$ due to the charge injection and the clock feedthrough. The V_{FD} after the reset operation is V_{DD} - V_{THR} - ΔV_{CH}. Since the capacitance of FD is very small (< 5 fF), the resultant error ΔV_{CH} will be large (> 100 mV). Considering this error, Eq. 3.35 (b) can be modified as

$$V_{DD} > \Delta V_{FD} + V_{DSsat} + 2V_T + \Delta V_{CH} \qquad (3.36)$$
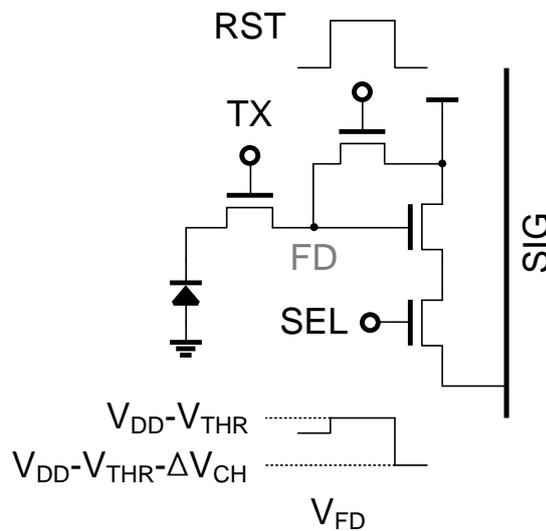
Figure 3.19 Charge injection and clock feedthrough in the reset transistor

Another side effect occurs in the source follower. Since the nMOS transistor in the pixel is not formed on the separate p-well, the body of nMOS transistor is connected with ground. This induces a body effect and the gain of the source follower becomes less than 1 as follows:

$$A_{V(SF)} = \frac{g_m}{g_m + g_{mb}} = \frac{1}{1 + \eta} < 1 \qquad (3.37)$$

Typically the source follower gain is around 0.8 ~ 0.9. Therefore, we can modify the Eq. 3.36 as follows:

$$V_{DD} > \frac{\Delta V_{FD}}{A_{V(SF)}} + V_{DSsat} + 2V_T + \Delta V_{CH} \qquad (3.38)$$

Moreover, the source follower has nonlinearity due to the channel length modulation of the bias transistor. The output voltage V_{OUT} and the current bias I_{BIAS} has nonlinear relationship as follows:

$$\text{(a) } V_{OUT} = V_{FD} - V_{GS}$$
$$\qquad (3.39)$$
$$\text{(b) } I_{BIAS} = K(W/2L)(V_{GS} - V_T)^2(1 + \lambda V_{OUT})$$

This non-linearity distorts the image signal, which is not desirable for the post image processing. If the power supply voltage is scaled down and enough signal swing is not guaranteed, the bias transistor falls into the linear region especially when the illumination is high (V_{OUT} is low).

3.2.2 Reset Signal Boosting

Hard reset

One V_T drop out of two V_T drop in the pixel circuit occurs in the reset transistor. In order to remove the V_T drop in the reset transistor, the signal 'RST' is boosted from V_{DD} to $V_{DD} + V_T$ using the charge pump circuit as shown in figure 3.20 [3.12]. This operation makes the reset transistor operates in the linear region, whereas the reset transistor operates in the sub-V_T region without reset signal boosting.

The reset operation with boosting is called hard reset and the reset operation without boosting is called soft reset. It is known that the hard reset doubles the kTC noise [3.13]. However, the kTC noise can be suppressed in the 4-T structure. By using the reset signal boosting, the minimum power supply voltage can be expressed as Eq.3.40.

$$V_{DD} > \frac{\Delta V_{FD}}{A_{V(SF)}} + V_{DSsat} + V_T + \Delta V_{CH} \tag{3.40}$$
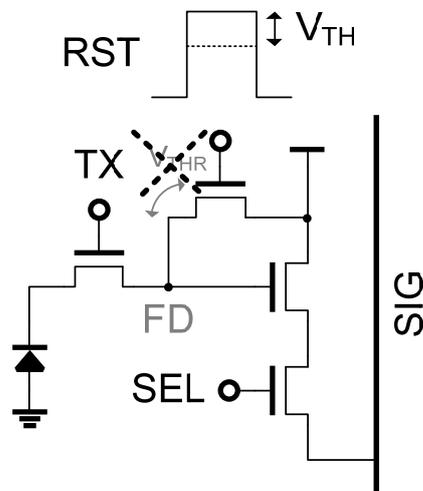
Figure 3.20 Hard reset: reset gate boosting

Capacitive coupling

Hard reset is an effective way to increase the signal swing with lower power supply voltage. However, additional boosting circuits that consist of charge pump are required. The charge pump circuits need large capacitors in order to boost the reset gate (RST) that

has large parasitic capacitance. This is not desirable in terms of the area and also the power consumption.
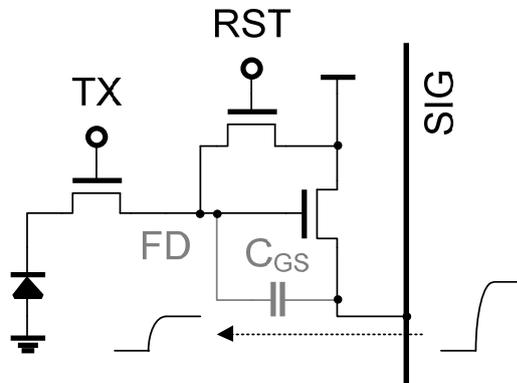
Figure 3.21 Reset level boosting with capacitive coupling (1)

Another method to increase the reset level is using a capacitive coupling [3.14]. Figure 3.21 shows the pixel circuit with the capacitive boosting. Note that the selection transistor is not used. For the row selection, the FD node is reset and the source follower is turned on. Using the soft reset, the FD node is reset with $V_{DD} - V_T$. The source follower output (SIG) increase slower than the FD node due to the large parasitic capacitance. Through the gate-source capacitance of the source follower, the increase of source follower output couples with the FD node, therefore, the reset level is boosted.
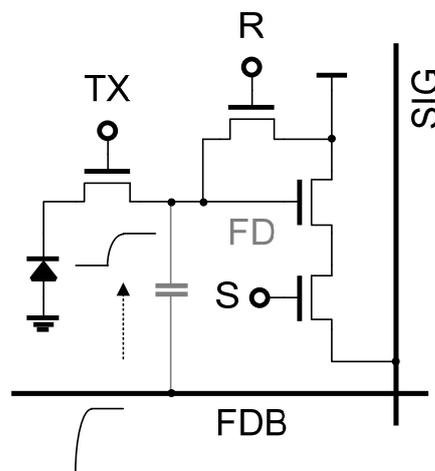
Figure 3.22 Reset level boosting with capacitive coupling (2)

Another scheme to boost reset level is shown in figure 3.22 [3.7]. In this scheme, additional metal line (FDB) has been placed. The parasitic capacitance between the FDB and the FD node operates as a coupling capacitor. When the FDB line is driven high, the FD node voltage increases.
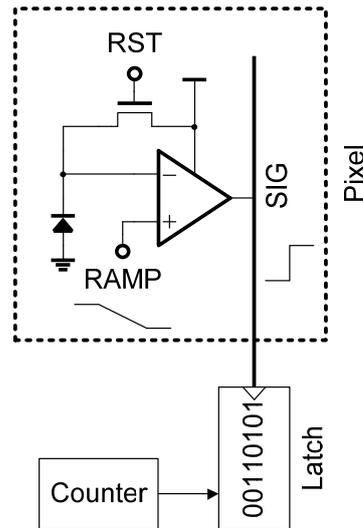
Figure 3.23 In-pixel pulse width modulation scheme

3.2.3 In-Pixel Pulse Width Modulation (PWM)

As explained in the previous section, conventional source follower readout has limitations of voltage scaling. Moreover, non-linearity and gain loss further limit the voltage scaling. Instead of using the source follower, an in-pixel comparator can be used for the readout by performing the single-slope ADC operation, which is one kind of pulse width modulation (PWM). Figure 3.23 shows the concept of in-pixel PWM. One input of the comparator is connected with the detection node. The other input is driven by the ramp signal. The comparator is toggled when the ramp signal crosses the voltage of detection node, then the counter value is latched. The advantage of the in-pixel PWM scheme is that there is no gain loss from the body effect. Moreover, it is less vulnerable from the current bias variation, which induces non-linearity. However, this scheme

70

generally requires larger pixel size due to the in-pixel comparator, which requires pMOS transistors. Another disadvantage is the input voltage variation during the ADC time because it requires 2^N cycles of operation for the N-bit conversion. In high illuminations, the detection node can be saturated during the ADC time.

In-pixel comparator without static bias current

Figure 3.24 shows one in-pixel PWM scheme [3.15]. In this work, nMOS-only comparator that has common source amplifier topology is used and no fill factor loss takes place. The operation is as follows: (1) Reset: the photodiode is reset by forming the unity feedback. (2) Integration (3) Precharge: before the readout, the column line is precharged (4) PWM: the ramp signal is applied to the source of the transistor. When the ramp signal crosses the voltage $V_{PD} - V_T$, the charged column line starts to be discharged. By regenerating the voltage variation of the column line, counter value is latched.

In this scheme, no static bias current is required except in the reset operation. Therefore, power consumption can be reduced. However, there is a limitation in the voltage scaling. The signal swing in the photodiode can be expressed as follows:

$$V_T < V_{PD} < V_{RAMP(RST)} + V_T$$

$$(V_{RAMP(RST)} = \Delta V_{PD(max)})$$

(3.41)

By adjusting the voltage of V_{RAMP}, the maximum signal swing can be controlled. Since the comparator has the common source topology, there is a current source connected with V_{DD}. In order to guarantee that current sources operate in the saturation region, the minimum power supply voltage can be calculated:

$$V_{DD} > \Delta V_{PD(max)} + V_T + V_{Dsat}$$

(3.42)

71

(a) Pixel architecture

(b) Operation
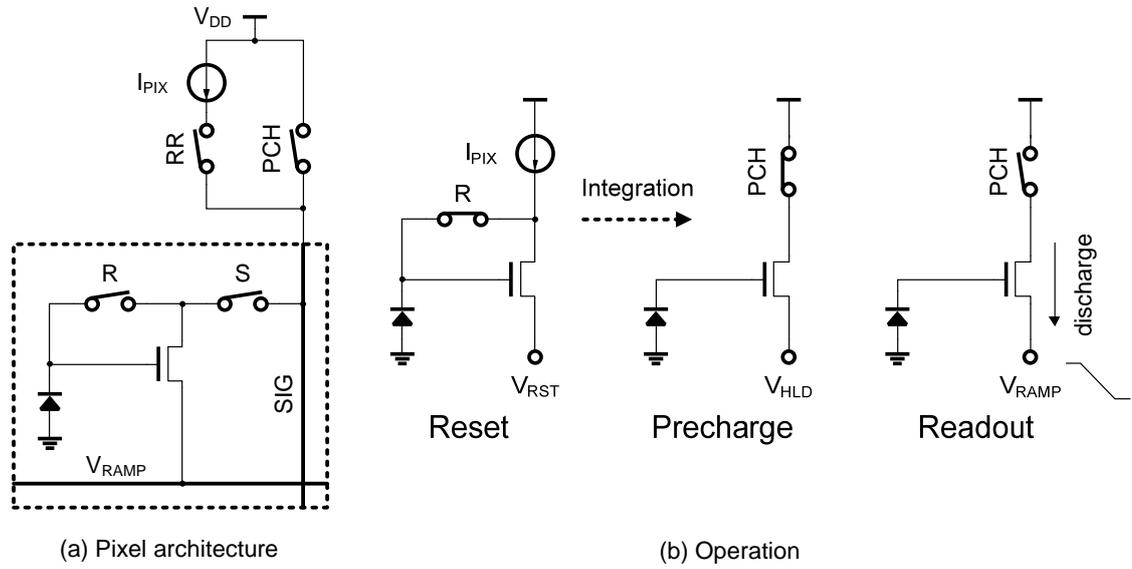
Figure 3.24 In-pixel comparator without static bias current

Therefore, it is difficult to achieve sub-1V power supply. In this scheme, ramp signal driving is another critical factor. Since the discharge current flows into the ramp signal line, it corrupts the ramp signal if it is not buffered. Driving the ramp signal will require more power consumption.

In-pixel Sub-V_T comparator

Figure 3.25 shows the in-pixel PWM scheme with a sub-V_T comparator [3.16]. By operating the comparator in sub-V_T region, voltage can be scaled down to < 0.5 V and the power consumption is 1.19 μW for 128 × 128 pixels. However, the comparator uses pMOS transistors that make the pixel size larger. The comparator requires 3 additional transistors compared with the 4-T pixel architecture. In order to guarantee the input range of the comparator, there is an additional diode-connected transistor in the reset path. This reduces the reset level and suppresses the SNR. Moreover, correlated double sampling is not applied in this scheme, therefore, FPN is large.

72
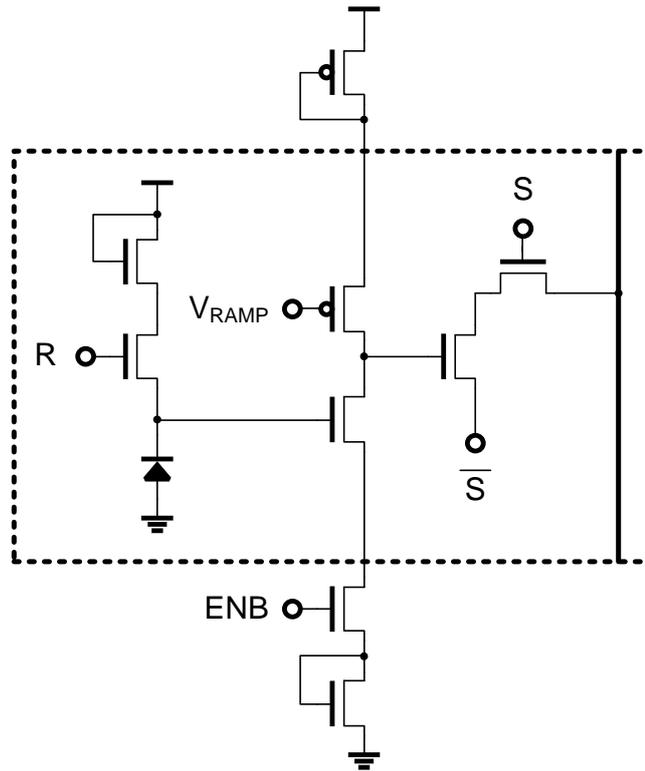
Figure 3.25 In-pixel PWM with sub-V_T comparator
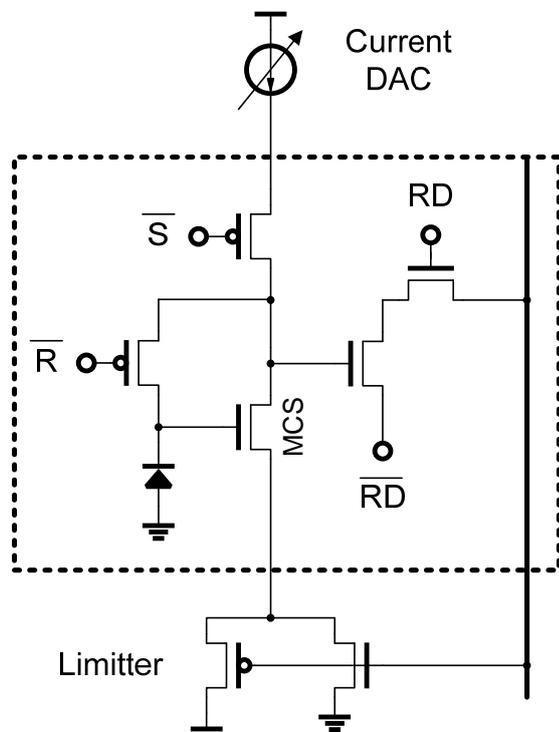
Figure 3.26 In-pixel sub-V_T comparator with current-controlled threshold

Figure 3.26 shows another in-pixel PWM scheme with sub-V_T comparator [3.17]. Instead of applying voltage ramp signal, this scheme uses current DAC and changes the threshold voltage of the transistor MCS for the PWM. The transistor MCS is biased by the current DAC and operates in sub-V_T region. The pixel includes only 5 transistors, however, it includes pMOS transistors that make the pixel size larger.

Scheme	Source follower with voltage scaling	In-pixel pulse-width-modulation (PWM)	
Pros	Small pixel	No gain loss, non-linearity	
Cons	Gain loss, non-linearity	Large pixel, input voltage change	
Reference	[3.12]	[3.16]	[3.15]
Readout circuit	Source follower	Sub-V_{TH} in-pixel comparator	nMOS-only comparator
Power supply	1.5 V	0.5 V	1.35 V
Power consumption	550 uW (total)	1.19 uW (total)	0.42 uW (pixel) 55.2 uW (total)
Power FOM [pW/pixel·frame]	723.4 pW	8.6 pW	468 pW
SNR	49.63 dB	23.1 dB	52.9 dB
Pixel array	176 x 144	128 x 128	128 x 96
Pixel size	5 x 5 um^2 (0.35 um CMOS)	5 x 5 um^2 (0.13 um CMOS)	3.2 x 3.2 um^2 (0.35 um CMOS)
Pros	Small pixel	V_{DD} scaling	Small pixel
Cons	Limited V_{DD}	Large pixel Low SNR	Limited V_{DD} Ramp generation

Table 3.4 Summary of low-power CMOS image sensors

Table 3.4 summarizes the previous low-power CMOS image sensors.

3.3 Wide Dynamic Range Image Sensors

A dynamic range (DR) is the parameter that determines the illumination range, which can be incorporated in one image. The DR of natural scenes is more than 100 dB, whereas the DR of conventional CMOS image sensors is only 60 ~ 70 dB. The definition of the DR in image sensors is as follows:

$$DR = 20 \cdot \log \frac{\text{Saturation level}}{\text{Minimum detectable level}} \ [\text{dB}] \qquad (3.43)$$

The minimum detectable signal is limited by noise floor. As shown in Eq. 3.43, in order to increase the dynamic range, we can increase the saturation level or reduce the noise floor. When we refer to "dynamic range extension", it typically means the dynamic range enhancement schemes, which increase the saturation level in order to prevent the saturation over wide ranges of illumination.

Reducing the noise floor is common issue for both conventional CMOS image sensors and WDR CMOS image sensors. In low illuminations, SNR is degraded due to low signal level. If CMOS image sensors have high sensitivity, i.e., generate higher signal level with less incident photons, SNR increases due to the increase of signal level. However, increasing only the sensitivity reduces the dynamic range because the signal will be saturated from smaller photons. Therefore, it is important to optimize both schemes according to the illumination. The sensitivity can be enhanced by several ways. One is the process optimization such as photodiodes, color filter arrays and microlens. The other is by the readout circuits. The CDS circuit and the programmable amplifier (PGA) is one example.

This section will explain about the sensitivity enhancement schemes. The integrated dynamic range enhancement schemes will be illustrated in the next section.

3.3.1 Sensitivity Enhancement

As explained in chapter 2, the sensitivity is defined as the ratio of the output signal [V] to the incident illumination level [lx] in a second. The unit of sensitivity is [V/lx·s]. Sensitivity can be increased by process optimization, microlens optimization, and so on.

One of way to increase the sensitivity is applying high gain in order to amplify the signal and suppress the noise. The programmable amplification in the CDS circuit is a good choice to increase the sensitivity. However, the PGA requires significant power consumption because it is configured with capacitive feedback. The capacitance is large enough to guarantee the matching between columns (typically > 1 pF). Moreover, column parallel PGAs only suppress the noise of ADCs, not the readout circuit noise from in-pixel source followers. Therefore, there are previous works that employ in-pixel amplification instead of column parallel amplification.
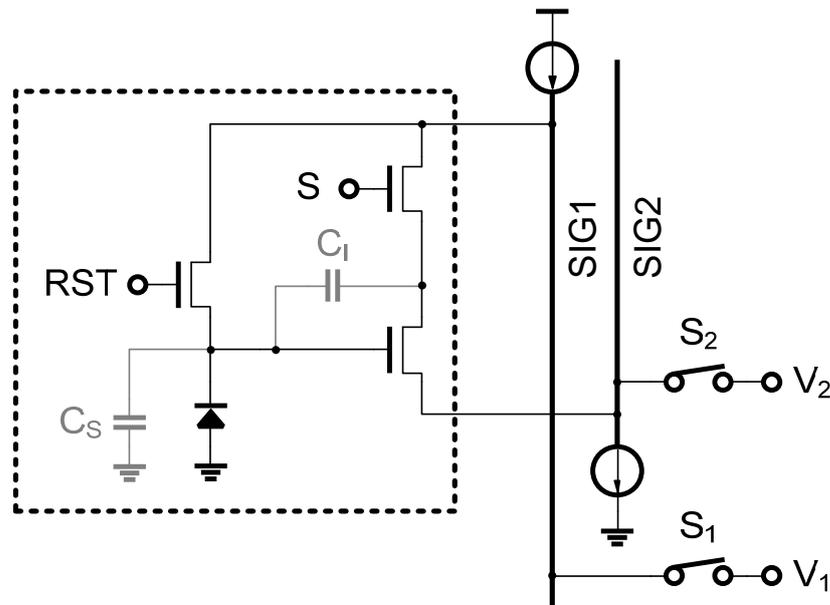
Figure 3.27 In-pixel nMOS common source amplifier with p-n photodiode

One previous work used the nMOS common source amplifier with p-n photodiode [3.18] as shown in figure 3.27. As mentioned, in the 3-T pixel structure, kTC reset noise is not cancelled. In order to suppress the kTC noise in the 3-T structure, this work used unity feedback using in-pixel commons amplifiers. In simple one pole amplifiers, the gain increment by A_V induces the bandwidth reduction by A_V. Therefore, the noise power

from kTC noise is decreased by A_V. Assuming the amplifier gain is infinite, the gain of the amplifier can be defined as follows:

$$A_V = \frac{C_S}{C_I} \qquad (3.44)$$
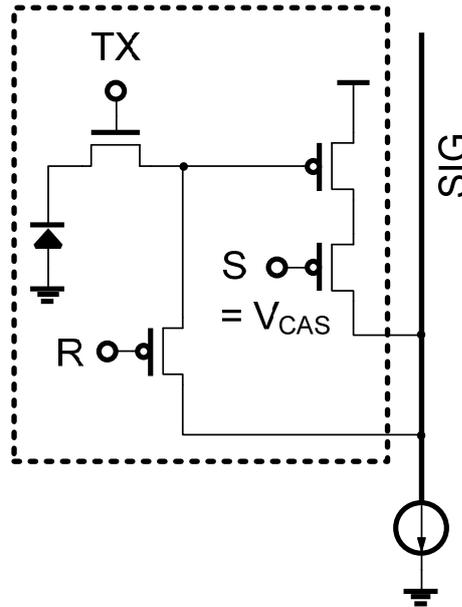
Figure 3.28 In-pixel pMOS common source amplifier with pinned photodiode

In Eq.3.43, C_S is the capacitance of the detection node and C_I is the gate-drain capacitance of the transistor M2. Since C_S has the capacitance over 10 fF, and C_I is less than 0.5 fF, high gain > 20 is achievable. However, the gain of common source amplifiers cannot be an infinite and it is typically around 10, which brings out the reduction of the gain compared with Eq. 3.44.

Another previous work used pMOS common source amplifiers with pinned photodiode [3.19]. This work uses similar topology as a conventional 4-T pixel structure except that they used pMOS common source amplifiers as shown in figure 3.28. In pinned photodiodes, the reset level should be high enough in the floating diffusion in order to guarantee complete charge transfer. In order to increase the reset level that is set

77

by the unity feedback, a pMOS amplifier is chosen. In the selection transistor, the voltage bias V_{CASC} is applied for the cascade configuration. It suppresses the Miller effect and higher gain is achievable. The input referred noise is suppressed by the gain of amplifier ($g_m R_i$) as follows:

$$v_i = \sqrt{\gamma \frac{kT}{C_S} \cdot \frac{1}{g_m R_i}} \qquad (3.45)$$

,where C_S is the sampling capacitor in the column (not shown in the figure) This work achieved 0.86 e⁻ readout noise whereas the conventional CMOS imagers have > 2 e⁻ readout noise. However, pMOS transistors increase the pixel size (11×11 μm² in this work).

In summary, it is desirable to implement the in-pixel amplification for two reasons: (1) Avoid using power-consuming column-parallel PGAs while increasing the sensitivity (2) The in-pixel amplification suppresses the noise from pixel readout circuits.

3.3.2 Dynamic Range Enhancement Schemes

The integrated DR enhancement scheme can be categorized as two: non-linear scheme and linear scheme.

The basic principle of nonlinear scheme is to compress the pixel output response and cover wider ranges of illumination before the pixel output is saturated. Figure 3.29 (a) shows basic concept of nonlinear scheme.

The linear scheme can be categorized as two: sensitivity adjustment and multiple exposure schemes. In the sensitivity adjustment, the sensitivity is intentionally decreased by reducing the conversion gain. As explained before, the conversion gain is q/C_D where C_D is the capacitance of the detection node. By connecting additional capacitance C_{OV}

with the C_D, the conversion gain will be reduced to $q/(C_D + C_{OV})$. The additional capacitance lowers the sensitivity. However, it increases the illumination range that is able to be sensed. Figure 3.29 (b) shows the basic concept of sensitivity adjustment scheme.
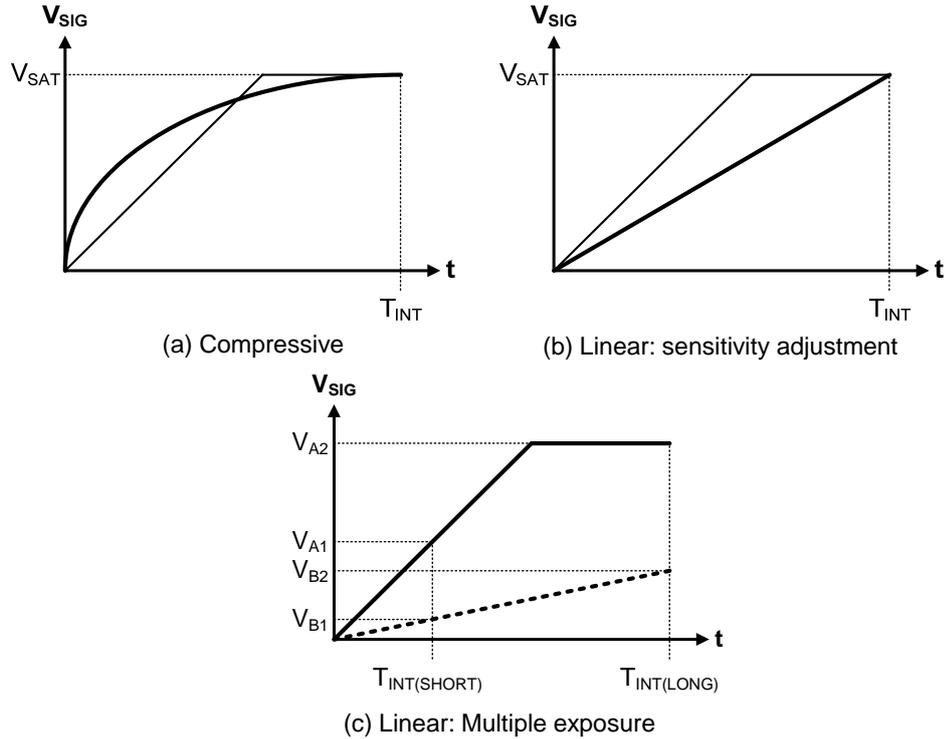
Figure 3.29 Dynamic range enhancement schemes

In the multiple exposure scheme, multiple signals from multiple integration time (from short to long) are synthesized. Figure 3.29 (c) shows the example of dual exposure. In the figure, two cases of pixel output response are shown: one is in high illumination (output is saturated) and the other is in low illumination. By applying the dual exposure, V_{A1} and V_{A2} will be synthesized. Although V_{A2} is saturated signal in high illumination, we can get the information from V_{A1}. Likewise, V_{B1} and V_{B2} will be synthesized in low illumination case. In this case, V_{B1} can be low and therefore has low SNR. However, V_{B2} has enough signal level from long integration time.

In the next three subsections, each scheme will be explained with previous works.

3.3.2.1 Nonlinear Scheme: Logarithmic Pixel

For a nonlinear response, a logarithmic response can be used because it is easy to implement by the transistor which operates in the sub-V_T region. The logarithmic pixel is shown in figure 3.30. Since the current is exponentially proportional to the gate-source voltage V_{GS}, V_{GS} is logarithmically dependent on the current. However, since the transistor operates in the sub-V_T region, it suffers high FPN due to the variation. In order to achieve both high SNR from the dark to moderate illumination and high DR in high illumination, linear-logarithmic pixel can be implemented
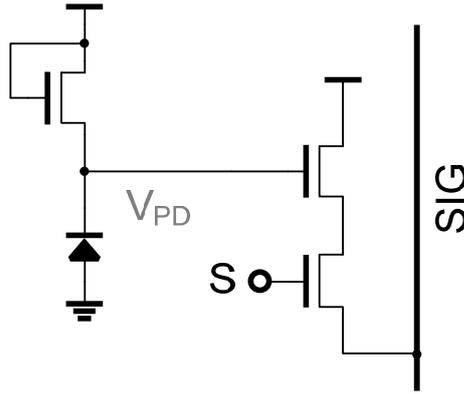
Figure 3.30 Logarithmic pixel

Figure 3.31 shows the linear-logarithmic pixel [3.20]. If the detection node voltage V_{PD} is smaller than $V_{LOG}-2V_T$, V_{PD} can be derived as follows:

$$(a)\ i_{ph} = i_{DS3} = i_0 e^{\frac{qV_{GS}}{kT}} = i_0 e^{q(V_{LOG}-V_X)/kT}$$

$$= i_{DS2} = i_0 e^{q(V_X-V_{PD})/kT} \tag{3.46}$$

$$(b)\ V_X = \frac{V_{LOG} + V_{PD}}{2}$$

80

$$\text{(c) } V_{PD} = V_{LOG} - 2\frac{kT}{q}\ln\left(\frac{i_{ph}}{i_o}\right)$$

By series connection of two diode-connected transistors M2 and M3, the logarithmic response term in Eq. 3.46 (c) has doubled gain. When V_{PD} is larger than V_{LOG}-2V_T, the transistor M2 and M3 is turned off and the pixel operates in the linear region as conventional 3-T pixel. In this structure, by adjusting V_{LOG}, the trip point between the linear region and the logarithmic region can be controlled.
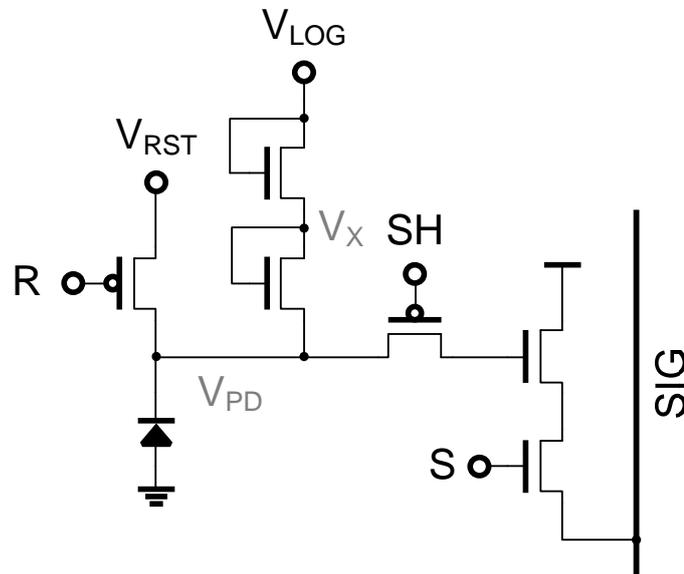
Figure 3.31 Linear-logarithmic pixel

The advantage of the logarithmic pixel is that it does not have much fill factor loss and the operation simple, i.e., no additional timing control is required. However, the logarithmic response from the sub V_T region has higher FPN that is cannot be cancelled from the CDS operation. The previous work shows 112 dB DR, 9.4 μm pixel pitch, 30 % FF using 0.35 μm CMOS process. It shows 0.83 % FPN in the linear region and 1.37 % FPN in the logarithmic region.

3.3.2.2 Linear Scheme: Sensitivity Adjustment

The sensitivity is dependent on the conversion gain q/C_{FD}. With large C_{FD}, we can transfer and store more charge in the FD node. However, the sensitivity is decreased due to larger capacitance. As shown in figure 3.32, the sensitivity can be controlled using an additional capacitor C_S and a selection switch S2. In this scheme, the pixel keeps high sensitivity in low illumination (S2 off). The pixel decreases the sensitivity in high illumination in order to prevent the saturation from high illumination (S2 on). However, the dynamic range extension is limited according to the capacitance of C_S. Larger C_S induces lower sensitivity due to reduced fill factor in low illumination.
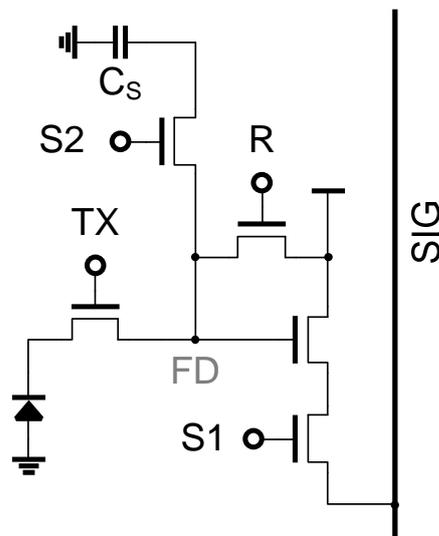
Figure 3.32 Sensitivity adjustment using in-pixel capacitor

Another scheme using the sensitivity adjustment is shown in figure 3.33. When illumination is high and the accumulation of photogenerated electrons exceeds the well capacity, a photodiode is saturated and electrons are spilled over. If we collect these spilled electrons in the additional capacitor with larger capacitance, we can read out signals with reduced sensitivity. This lateral overflow scheme [3.21] is shown in figure

82

3.33. In figure 3.33 (a), the pixel circuit is shown. An additional overflow capacitor C_{OV} and the floating diffusion (FD) is connected through the transistor S2.
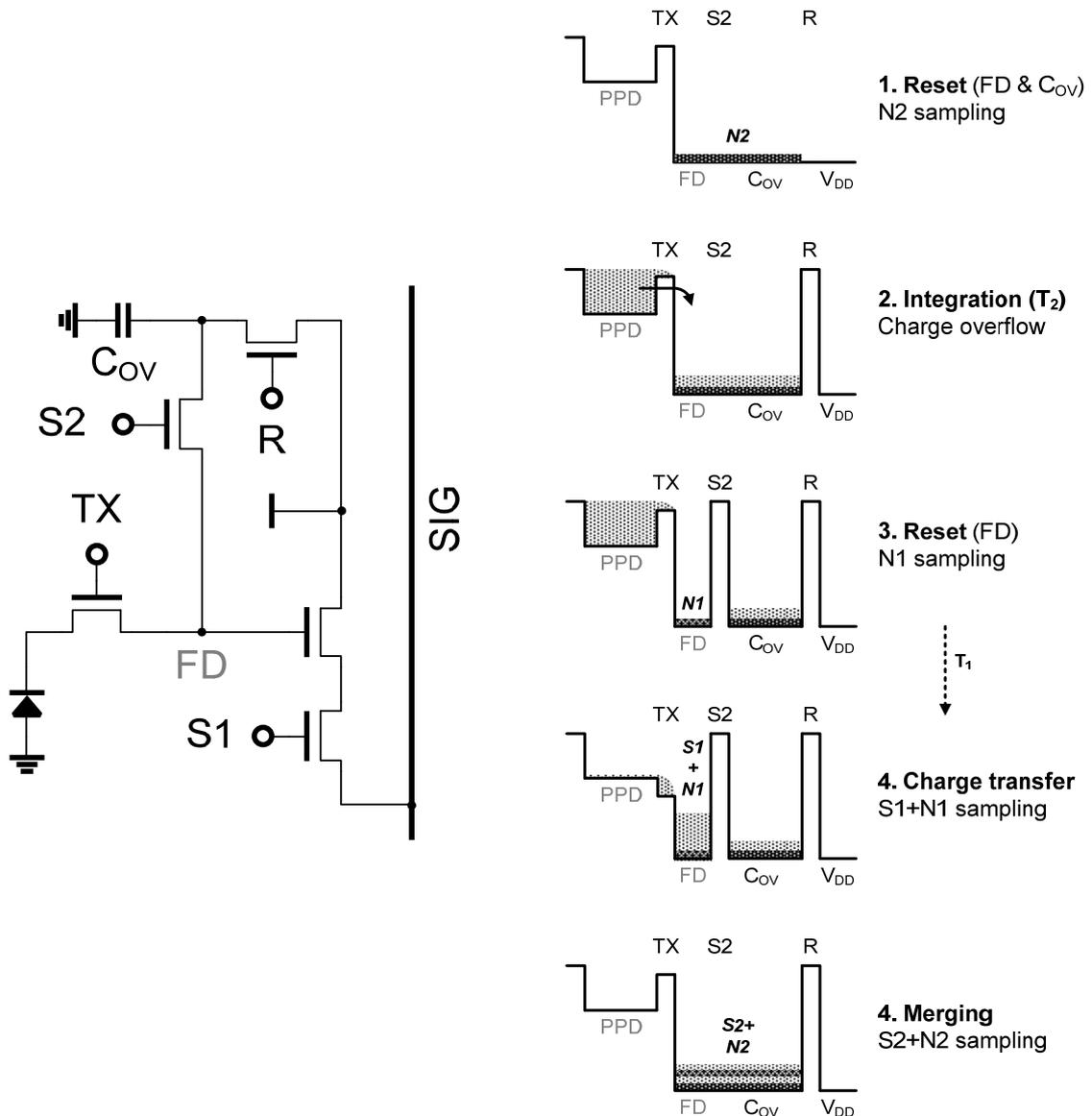
Figure 3.33 Lateral overflow scheme (a) Pixel circuit (b) Operation procedure

The operation procedure is described in figure 3.33 (b) with electron potential diagrams. The operation procedure is as follows: (1) Reset FD and C_{OV} (S: on) (2) Integration, if charges are spilled over, they are collected both in the FD and C_{OV}. (3) Reset FD: S is turned off, and FD is reset. (4) 1st signal readout: transfer charges into FD

83

and then readout signal (5) 2nd signal readout: S is turned on again and charge stored in C_{OV} is read out together with charges in the FD. Two signals from (4) and (5) are synthesized in external circuits.

The advantage of this scheme is that it has linear response. Linear response is preferable in a post image processing. It also has better SNR than nonlinear methods. However, due to the additional capacitor and transistor, fill factor will be decreased. In this work, the poly capacitor is implemented for C_{OV} and it is placed below the metal line. Therefore, fill factor loss is decreased. The previous work achieved 93 dB DR, 5.6 μm pixel pitch, 45 % fill factor using 0.18 μm CIS process. The limitation is that shared pixel structure cannot be applicable with this scheme. Therefore, it is difficult to scale down the pixel size.

3.3.2.3 Linear Scheme: Multiple Exposures

Another linear scheme for the dynamic range enhancement is a multiple exposure scheme. Image signals with multiple integration time are synthesized. Figure 3.34 shows the architecture using triple exposure [3.22]. In the case of triple exposure, three image signals with three different integration times from short to long have to be synthesized. In order to synthesize three image signals, two image signals should be temporarily stored in line memories before final image signals are read out and are synthesized together. Therefore, multiple exposure scheme requires additional memories.

Assuming three integration times are defined as follows:

T_{ROW}: one row access time, $T_1 = L \cdot T_{ROW}$, $T_2 = M \cdot T_{ROW}$, $T3 = N \cdot T_{ROW}$ ($L > M > N$)

The image signal from T_1 is temporarily stored during $(M+N) \cdot T_{ROW}$. After $M \cdot T_{ROW}$, the image signal from T_2 is temporarily stored during $N \cdot T_{ROW}$. After $N \cdot T_{ROW}$, the final

image signal from T_3 is read out and three image signals are synthesized into one image signal with wide dynamic range. Therefore, total M+2N rows of line memories are required. This takes significant portion of total die area. In the previous work, memory occupies 12 % of total area.

Moreover, this scheme requires multiple readouts, which require additional power consumption.
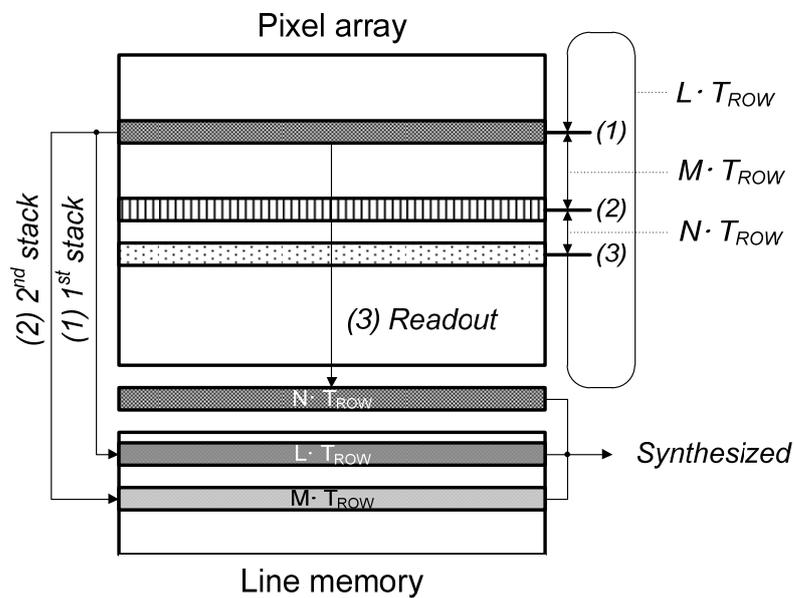
Figure 3.34 Triple exposure scheme

3.3.2.4 Summary of Integrated Dynamic Range Enhancement Schemes

Table 3.5 shows the summary of integrated dynamic range enhancement schemes. As mentioned in chapter 1, the image sensor has to generate a high dynamic range image (around 100 dB) at low-power consumption. Non-linear scheme using the logarithmic pixel has no fill-factor loss and simple operations. However, it has low SNR and temperature variation, which does not satisfy the requirement of reliability. Therefore, the linear scheme is better choice in applications for distributes sensors. The sensitivity adjustment scheme is one good solution. However, it is not applicable to the shared pixel

architecture, which is critical to achieve small form factor and low cost The multiple-exposure scheme also has larger form factor due to the additional line memory. Moreover, it has higher power consumption than other two schemes.

In the proposed adaptive image sensor, we proposed the low-power dual exposure scheme that does not require additional circuits or memories. It will be discussed in chapter 4.

Dynamic Range Enhancement	Non-linear	Linear	
		Sensitivity adjustment	Multiple exposure
Principle	Compress the pixel output response	Store overflown charge to the large capacitor (reduce the sensitivity)	Multiple signals from multiple integration time (short to long) are synthesized
Pros	No fill-factor loss Simple operation	Linear response Better SNR than non-linear	Linear response Better SNR than non-linear Small pixel size
Cons	Low SNR (logarithmic response from Sub-V_T transistor)	Larger pixel size (additional in-pixel capacitor)	Large power consumption, Line memory

Table 3.5 Summary of integrated dynamic range enhancement schemes

3.4 CMOS Image Sensors with Integrated Image Signal Processing for Bandwidth Reduction

If an image sensor generates M × N resolution 8-bit images with 30 frames per second (fps), total bandwidth is 240·M·N, which requires huge bandwidth and power consumption for an image signal transmission. However, the imaging with constant frame rate and the maximum resolution has redundancy in terms of both the spatial and temporal domain.

An image compression is one way to reduce the bandwidth [3.23, 3.24]. Many image compression techniques such as differential pulse code modulation (DPCM) or JPEG

format for still images or MPEG for videos are applied to the commercial digital imaging systems.

Even though the image compression offers the bandwidth savings, it still requires large bandwidth if imaging systems operate with fixed resolution and fixed frame rate. Moreover, typically these image compression algorithms require complex processing. Therefore, it is not adequate for distributed imaging systems especially for applications of surveillance systems that continuously monitor specific target objects or specific events.

Instead of generating images with maximum frame rate and resolution, several CMOS imagers generate only low-bandwidth features from motion events [3.25-3.29] or low resolution images that contains only target objects in order to save bandwidth [3.31, 3.32]. Another scheme generates variable resolution images for the bandwidth reduction [3.33-3.35]. In the next three subsections, previous works with integrated image processing for the bandwidth saving will be introduced.

3.4.1 Feature extraction

The motivation of a feature extraction is suppressing the bandwidth by generating low bandwidth features from specific events. Instead of transmitting full resolution images, the sensor delivers features only when specific events have been monitored.

One of simple feature is the temporal change from the motion sensing. The basic operation of the motion sensing in CMOS image sensors is frame difference that has simple operation. The difference between current frame signals and stored previous frame signals are subtracted. For the motion detection, storage elements are required to store the signals of previous frame. These storage elements can be placed in pixels as depicted in figure 3.35 [3.29]. There are two sample and hold circuits and two signal readout paths

for direct frame difference output. However, fill factor is decreased and pixel size becomes large due to in-pixel capacitors and additional readout paths. Pixel size is 32.2μm × 32.2μm in 0.5μm technology, and fill factor is 33%.
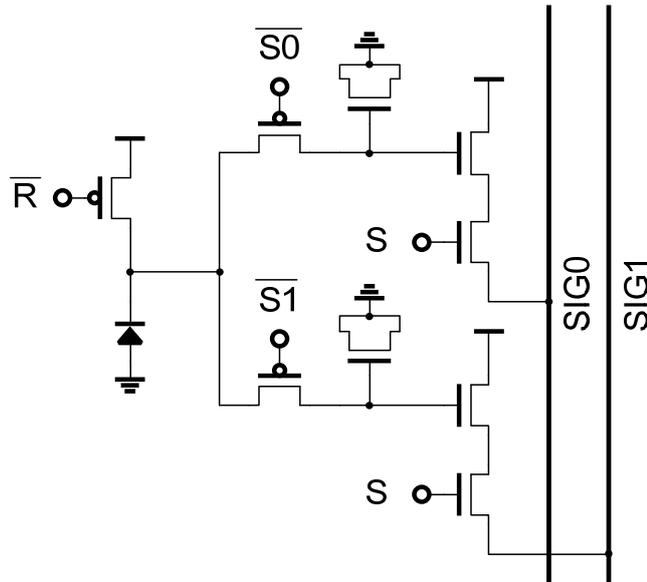
Figure 3.35 Pixel with direct frame difference output
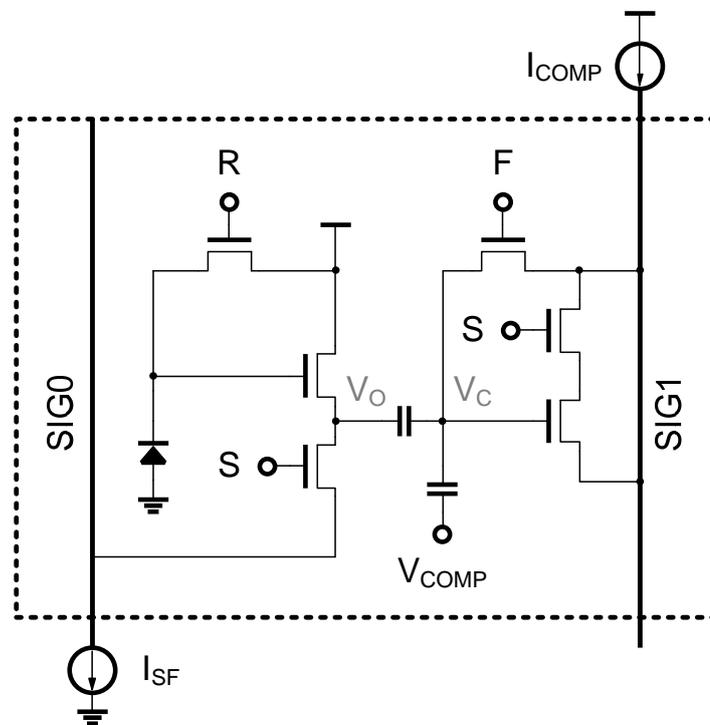
Figure 3.36 In-pixel comparator for the frame difference

88

Another previous work for the motion event generation contains two capacitors and a comparator in pixel as shown in figure 3.36 [3.25]. It generates normal image through the source follower as conventional 3T-pixel sensors. In addition, the comparator for the motion detection is integrated and generates motion images (frame difference). The analog output of frame difference is quantized into 2-bit digital signal in order to encode three events: no-motion, darker and brighter changes. This pixel contains 6 transistors and two capacitors. Fill factor is 17% and pixel size is $25.2 \times 25.2 \ \mu m^2$ with 0.5 μm technology.

Another example of simple feature extraction is the address event representation (AER). Instead of frame-based imaging, the sensor generates the output asynchronously based on the events [3.30]. The pixel responds to relative changes of light intensity and asynchronously generates 1-b signals. The sensor outputs the address of pixels that generated 1-b signals, i.e., have enough contrast change. Since the pixel has to monitor the temporal contrast change, it has additional capacitors and circuits, which increase the pixel size (8.1% fill factor, $40 \times 40 \ \mu m^2$ pixel size using 0.35μm technology).

By transmitting the output only when the temporal change is detected, data redundancy can be suppressed. However, the data rate of AER increases according to the number of pixels. Moreover, it responds to environmental conditions such as changes of illuminations or movements of background in addition to movements of actual target objects.

3.4.2 Region-of-Interest (ROI) readout

The region-of-Interest (ROI) image means the partial image containing an interested object out of entire image. The ROI readout scheme also suppresses the redundancy

because the background image is redundant. We don't need to generate entire image including redundant backgrounds. By generating only some parts of an entire image, required bandwidth and power consumption are saved. Accordingly, fast and simple post image processing is applicable.

The ROI can be simply determined by external logics [3.32]. A pixel array is divided with fixed-sized block, and several blocks for the ROI are selected by external logics. Basic block size is 32 × 32 pixels. The ROI size can be variable by the external control. However, this work does not include integrated ROI decision that detects target objects. This work just selects a group of blocks and outputs ROI images.
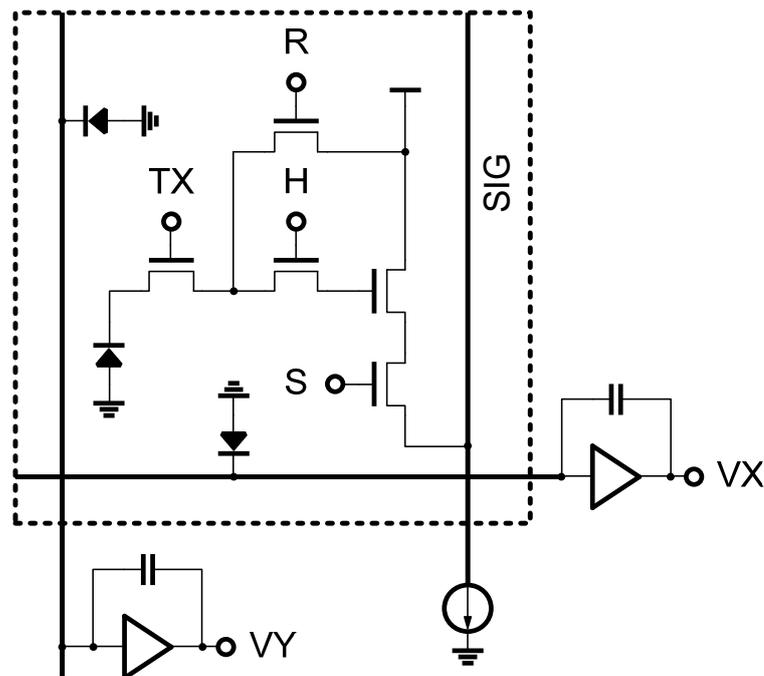
Figure 3.37 Pixel structure with two additional photodiodes

More advanced ROI readout capability has been published [3.31]. In this work, the sensor generates the ROI image containing brighter objects compared with the background image. This approach is targeted to the application for the car plate (that is bright from the headlights) monitoring at night. The pixel circuit is shown in figure 3.37.

In the pixel, two additional photodiodes are integrated. Each additional photodiode detects brightness using column / row parallel charge amplifiers. Each output of charge amplifiers generates profiles in X-Y directions. Using these profiles, ROI is decided by external circuit. The size of additional photodiode is small and fill factor is not severely reduced. However, this scheme is focused on the limited application and cannot detect dark object.

3.4.3 Variable-resolution image Readout

Variable-resolution readout means that the image sensor generates images with variable-resolutions from the maximum to the reduced resolutions. In order to reduce the resolution, a subsampling is a simple method to be implemented. However, the subsampling induces the aliasing effect. Therefore, a low resolution image is generally obtained by averaging or summing the image signals rather than skipping.

Low resolution images can be generated in various ways. By integrating passive capacitive networks, averaged value can be calculated [3.33, 3.34]. However, additional capacitors take large area.

Another method is charge-binning technique. The charge binning is originated from CCD image sensors, and is applied to CMOS image sensors by using the shared pixel architecture [3.36, 3.37]. In this scheme, charges integrated in several photodiodes are transferred into a floating diffusion with small capacitance, and sensitivity is enhanced.

The image signal can also be merged in digital domain [3.35]. After the analog-to-digital conversion, signals are averaged using digital circuits. However, it has worse SNR compared with charge domain merging because the readout noise and quantization noise are added..

3.5 Motion-adaptive multi-resolution image sensor

Constant frame-rate images with maximum spatial resolution entail high bandwidth and also large power consumption [3.38, 3.39]. This may limit its application for portable devices or wireless sensor networks in which both bandwidth and power consumptions are limited. Reducing the spatial resolution is one way to reduce the amount of image data. However, details in the image may be lost from the reduced resolution.

One efficient approach to reduce the bandwidth is to provide multiple temporal resolutions in one focal-plane: i.e., to provide a high frame rate only in the region-of-interest (ROI) where the moving objects are located and allow a low frame rate for the rest of stationery backgrounds. The images of the stationary objects are typically redundant at a high frame rate and it only degrades the SNR while wasting the large bandwidth.

120 fps

240 fps

Normal image with motion blur and
64 x 64 ROI image

Multi-resolution image
(full, 15 fps / ¼, 240 fps)
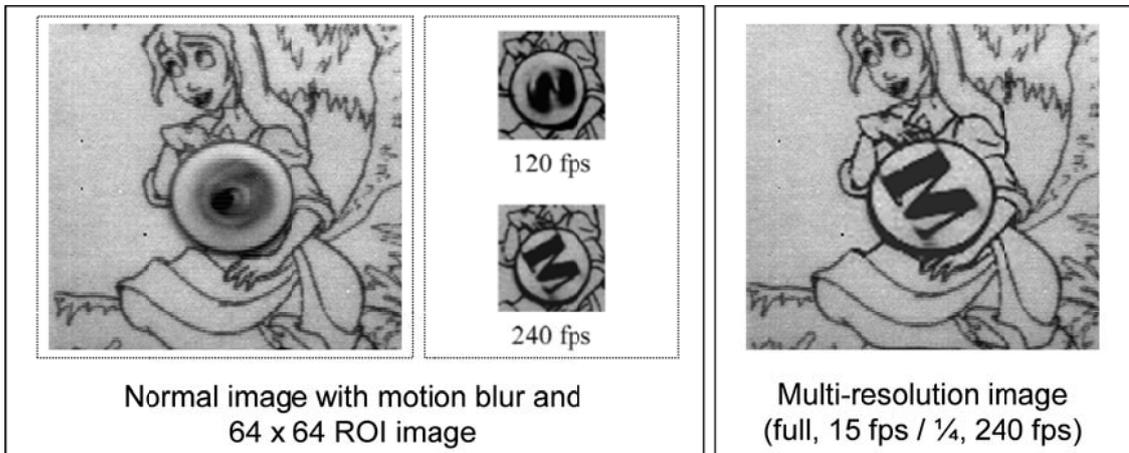
Figure 3.38 Images from motion-adaptive multi-resolution image sensor

Moreover, the spatial resolution in the ROI can be further optimized to reduce the amount of data. Combining the multiple temporal and spatial resolutions, we can acquire the image with details for stationery objects and with negligible motion-blur for the moving objects at low-power consumption and low-bandwidth.

92

In order to suppress the redundancy of bandwidth, a motion-adaptive multi-resolution CMOS imager that is able to provide an adaptive spatial-temporal multi-resolution for the specific region of interest which is autonomously determined from motion detection has been proposed [3.40]. Figure 3.38 shows output images from the multi-resolution image sensor.
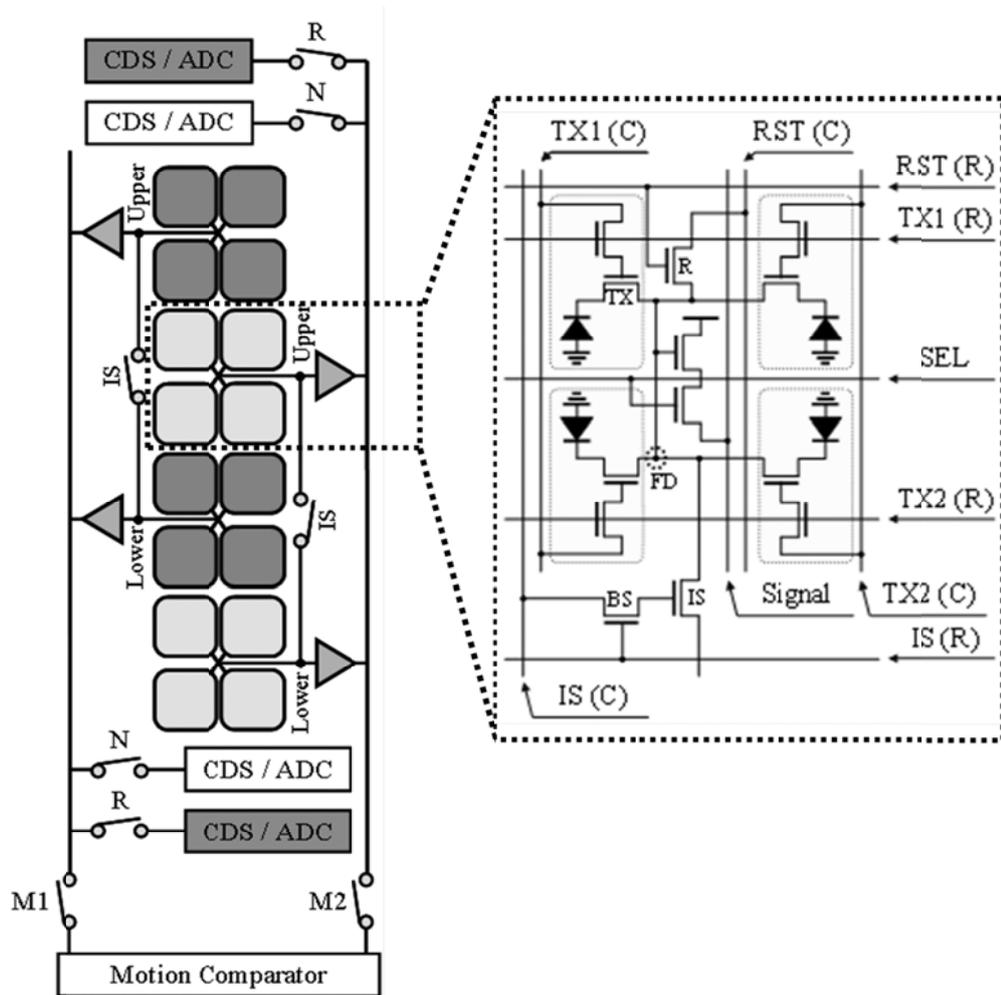
Figure 3.39 Pixel and column architecture of the multi-resolution image sensor

The sensor can simultaneously generate spatial-temporal multi-resolution readouts from the two channels: one at low frame rate with the maximum spatial resolution for the stationery backgrounds delivering the details of scenery; and the other at high frame rate

with the reduced spatial resolution for the moving objects in the ROI suppressing the motion blur. Since the high frame readout is performed only in the ROI, bandwidth and power consumption can be significantly reduced. In the ROI, the spatial resolution is reduced by four times. The charges from four shared pixels are summed in a floating diffusion node in order to enhance the SNR during the short integration time.
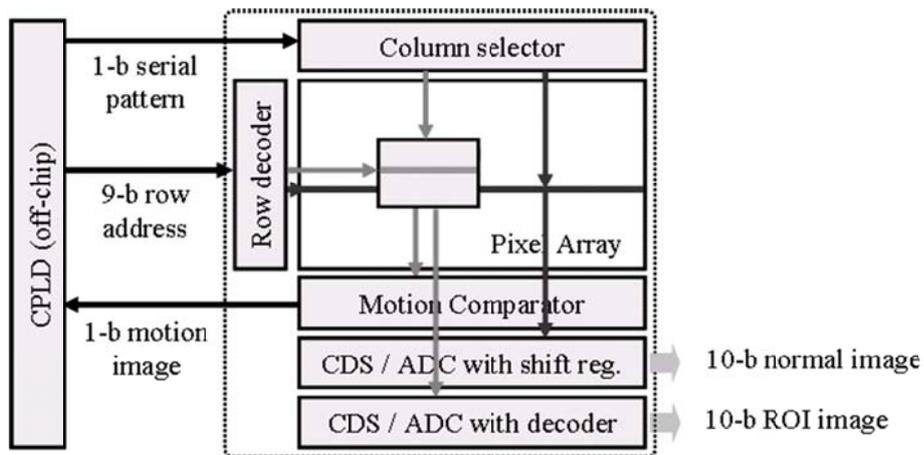
(a) Block diagram
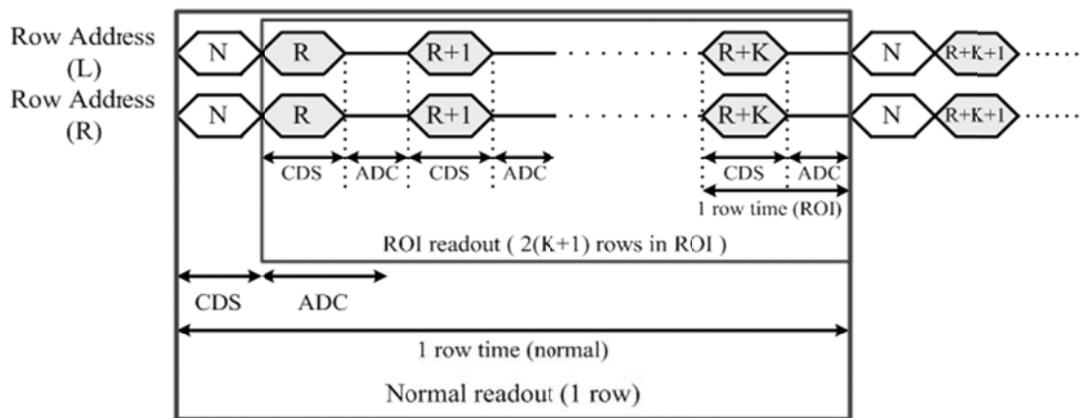
(a) Timing diagram

Figure 3.40 Multi-resolution readout: (a) Block diagram (b) Timing diagram

The ROI is determined in real-time by the integrated on-chip motion detection circuit. This circuit has been implemented in a small area by sequential inter-pixel switch

operations and does not require any additional in-pixel memory. Figure 3.39 shows the pixel and column architecture of the multi-resolution sensor. The pixel has 4-shared pixel architecture. The floating diffusions (FD) of two 4-shared groups are connected with inter-pixel switch (IS).

Instead of using additional in-pixel capacitor or frame memory, a floating diffusion node in the pixel has been used as an analog memory. The signal from the lower FD is transferred to upper FD through IS and the half of previous frame signal is stored in upper FD (because the capacitance of two FDs are same). After the half of integration time, the half of current frame signal is generated in the lower FD. The frame difference can be generated by comparing two FDs.

Figure 3.40 shows the block diagram of multi-resolution sensor. In the multi-resolution readout, the row decoder and the column selector provide independent pixel controls for the ROI as well as the background region. The dual channel CDS/ADC blocks will generate the normal and ROI image signals respectively. The motion detection is performed only within the ROI. From continuous motion detection, the ROI will be redefined and updated from the FPGA. The ROI signals are accessed at a high frame rate during the blanking time in the one row time that is assigned for normal readout.

3.6 Summary

In this chapter, we estimated and analyzed power consumption in CMOS image sensor. From this estimation, we can draw power reduction strategies: voltage scaling with modified architecture, suppression of redundant switching, reduction of output bandwidth, and small pixel size.

This chapter introduced three categories of previous works about low-power CMOS image sensors, integrated dynamic range enhancement / high-sensitivity readout, and the integrated image processing for the bandwidth savings. As mentioned in chapter 1, for applications of distributed sensors, four requirements (low-power consumption, reliability, spatial and temporal bandwidth) should be satisfied together. However, these four requirements are generally in trade-off and this trade-off is clearly shown from the previous works.

For the low-power consumption, a voltage scaling is limited due to the SNR degradation. The in-pixel PWM is an alternative method to achieve low-power consumption. However, it also has SNR degradation and the limitation of voltage scaling. Moreover, the input voltage of in-pixel comparator is corrupted from the illumination change due to the long conversion time.

In order to achieve reliable sensing in wide range of illumination, we have to increase the dynamic range. Two methods for wide dynamic range are integrated dynamic range enhancement scheme and high-sensitivity readout. Three dynamic range enhancement schemes are introduced in this chapter. Non-linear scheme using the logarithmic pixel offers no fill-factor loss and simple operation. However, it has low SNR and temperature variations, which do not satisfy the requirement of reliability. The sensitivity adjustment scheme is not applicable to the shared pixel architecture and increases the form factor. The multiple-exposure scheme also makes large form factor due to the additional line memory. Moreover, it requires higher power consumption than other two schemes.

For the spatial and temporal bandwidth savings, integrated lightweight image processing is essential. The motion sensing and the ROI image readout suppress both the spatial and temporal redundancy because they generate low bandwidth output only when events or interested objects are detected. The variable-resolution readout also provides a spatial bandwidth saving by merging neighboring pixels. However, these schemes have limitations for applications of wireless imaging systems due to large pixel size and high sensitivity for environmental conditions (motion from the background, illumination).

Since it is difficult to satisfy four requirements at the same time, it is desirable to implement an image sensor adaptable, i.e., the image sensor changes its operation adaptively according to environmental conditions and applications. It is also important to implement with small pixel size and small form factor in order to reduce both power consumption and cost. In this chapter, a motion-adaptive imager that is able to provide an adaptive spatial-temporal multi-resolution for the specific region of interest that is autonomously determined from the motion detection has been introduced. The next two chapters will explain about the three adaptive imaging methods: energy, illumination, and objective adaptive imaging.

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CHAPTER 4 ENERGY/ILLUMINATION-ADAPTIVE IMAGE SENSOR WITH RECONFIGURABLE MODES OF OPERATION

For outdoor surveillance or biomedical applications, sensitivity and dynamic range are important to deliver reliable information over widely changing illumination. However, constant monitoring with maximum awareness requires large power consumption and is not feasible for energy-limited applications such as battery-operated and/or energy-scavenging wireless sensor nodes. One of ways to reduce the power is voltage scaling [4.1, 4.2]. However, it significantly reduces the SNR and results in poor image quality [4.2]. The signal can be easily corrupted from the noise in dark conditions or be saturated in bright conditions. Dual power supply has been applied but still the conventional source follower readout scheme limited the signal range [4.3]. Most imagers with high-sensitivity and wide dynamic range reported [4.4, 4.5] consume large power > 50 mW, unsuitable for wireless imager node applications. Therefore, it is imperative to implement an imager adaptable to an environment, i.e., the sensor keeps monitoring at an extremely low power, turns into the high sensitivity or wide dynamic range imaging when illumination varies, or when detailed image transmission is requested from the network. The sensor changes its operation back to monitoring mode when the energy harvesting is poor or it is needed to save more charges in the battery. In this chapter, we report an adaptive CMOS image sensor which employs four different imaging modes: monitoring, normal, high-sensitivity and wide-dynamic-range (WDR) modes. This adaptable feature

enables the reliable monitoring while significantly enhancing the battery lifetime of wireless image sensor nodes.

4.1 Adaptive imaging operation and overall architecture

Figure 4.1 shows the operation of the adaptive imaging and figure 4.2 shows the block diagram of the proposed sensor chip. In the monitoring mode, the sensor operates at 0.8V supply. In-pixel comparators and 8-b successive approximation (SAR) ADCs enable power saving. For an in-pixel ADC, a SAR ADC is chosen because its short conversion time (8 cycles) saves power. Other three modes operate at 1.8V supply with 10-b single-slope (SS) ADCs. In high-sensitivity mode, each pixel generates an amplified signal from in-pixel differential common-source amplifiers, which suppresses the input referred noise in dark conditions. In normal mode, the signal is read out though a source follower as in conventional sensors.
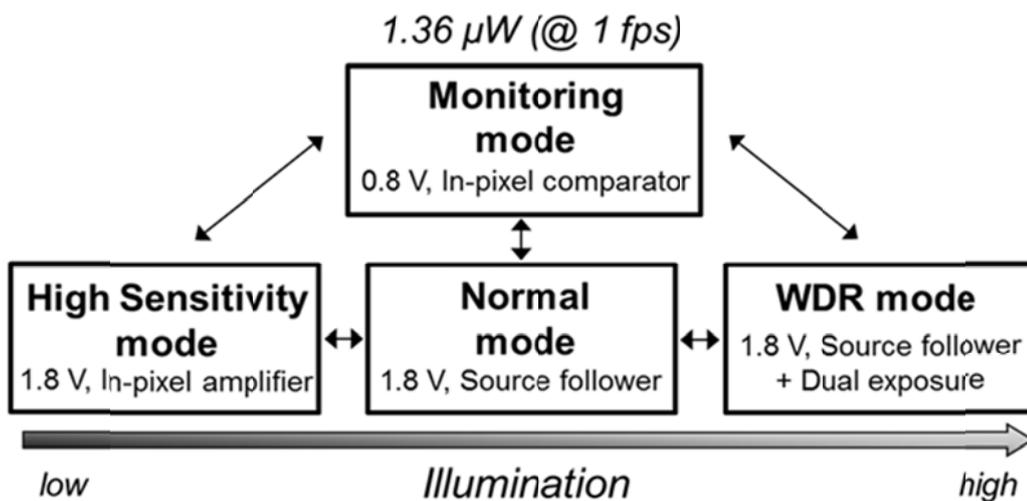
Figure 4.1 Operation of adaptive imaging
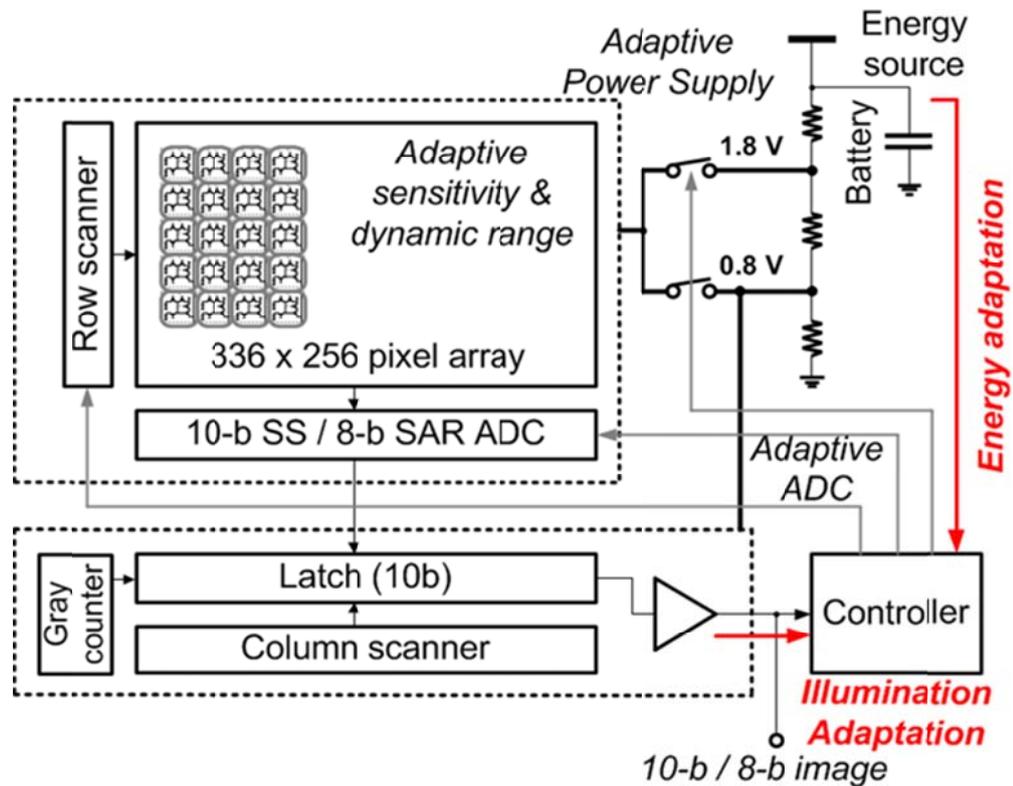
Figure 4.2 Operation and block diagram of the adaptive image sensor with reconfigurable modes

In WDR mode, dual exposure prevents the signal from saturation by providing two integration times, short and long, in the same frame. The sensor has column parallel ADCs and 10-b latches. The ADC is designed to be reconfigured to operate as either 8-b SAR or 10-b SS ADCs according to the modes. The column scanner accesses the latch and image signals are read out through sense amplifiers.

4.2 Pixel and column circuits for reconfigurable modes

Figure 4.3 shows the pixel architecture and figure 4.4 shows equivalent circuits in each mode. Two pixels are vertically shared and form one group. Two groups can form a differential pair for in-pixel differential amplifiers. This differential configuration eliminates a gain loss from the body effect in the source follower. In order to reduce the

V_{GS} drop and increase the signal swing, low-V_{TH} transistors are used for 'T_{AMP}.' The control signals for transmission gates, 'TX0' and 'TX1,' are boosted by bootstrap circuits outside the pixel. For differential readout, each group uses separate signal lines 'SIG0' and 'SIG1.' 'COM' line, which is common to two groups, is connected to either pixel power supply (for source follower operation) or current bias (for differential amplifier operation). 'RSTC' is connected to the capacitive DAC for in-pixel SAR ADC in the monitoring mode or is connected to pixel power supply for the reset operation. Figure 4.5 shows the timing diagram of the pixel control in each mode.
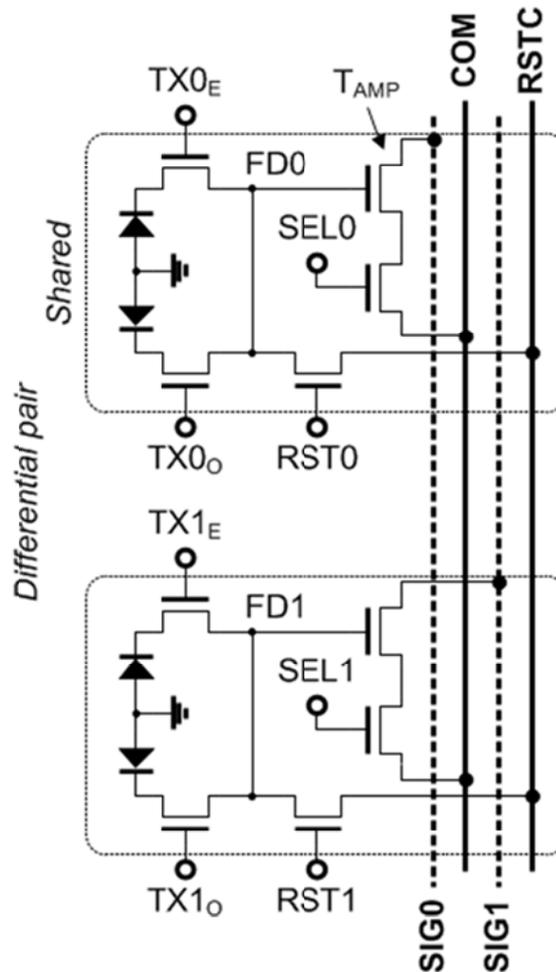
Figure 4.3 Pixel circuit of reconfigurable pixel
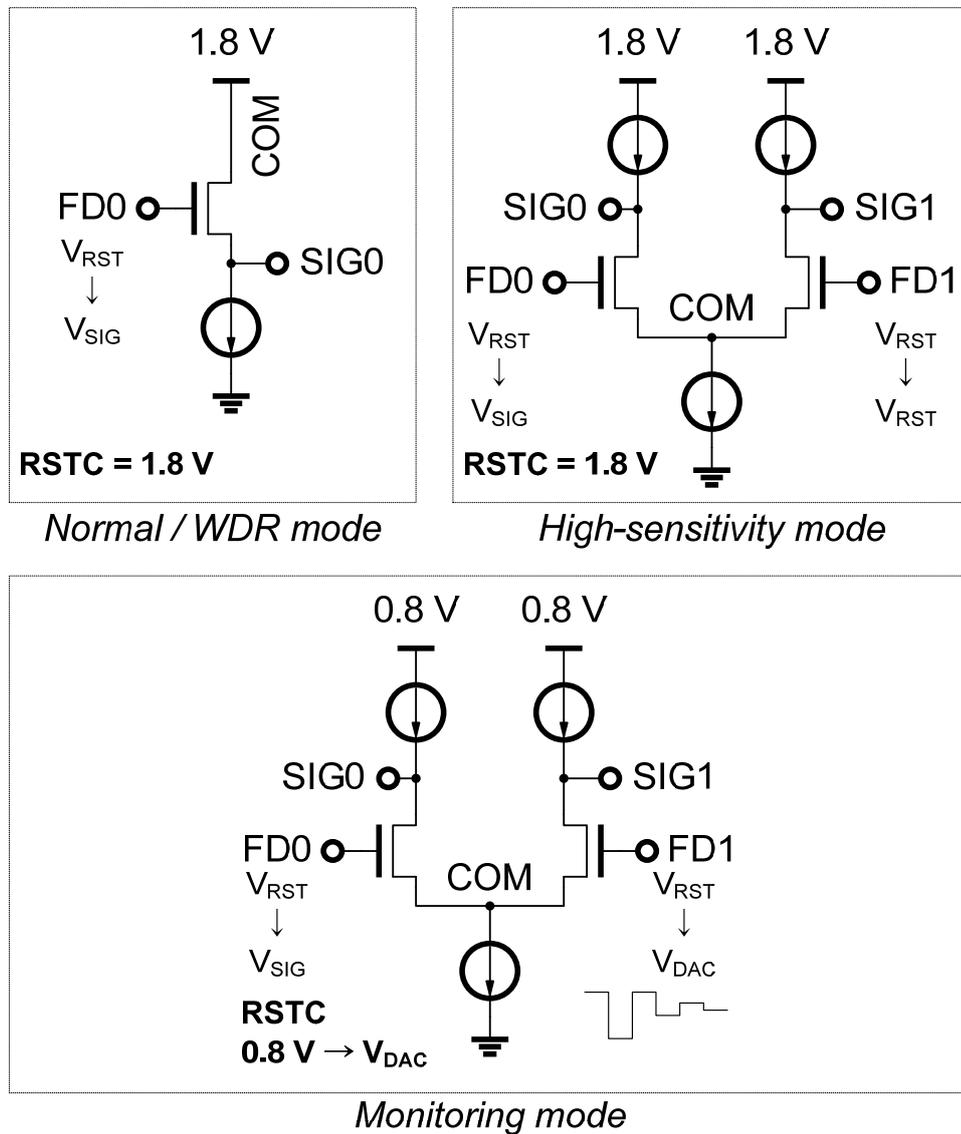
Figure 4.4 Pixel architecture and equivalent circuits in each mode

In monitoring mode, the pixel circuit operates as a preamplifier of SAR ADC at 0.8V as shown in figure 4.6. The signal from the capacitive DAC, which is located in the column circuits, is provided through 'RSTC' and the in-pixel preamplifier generates the amplified comparison signal in each conversion cycle. The pixel power supply (0.8 V) is used for the reference voltage of SAR ADC.

106
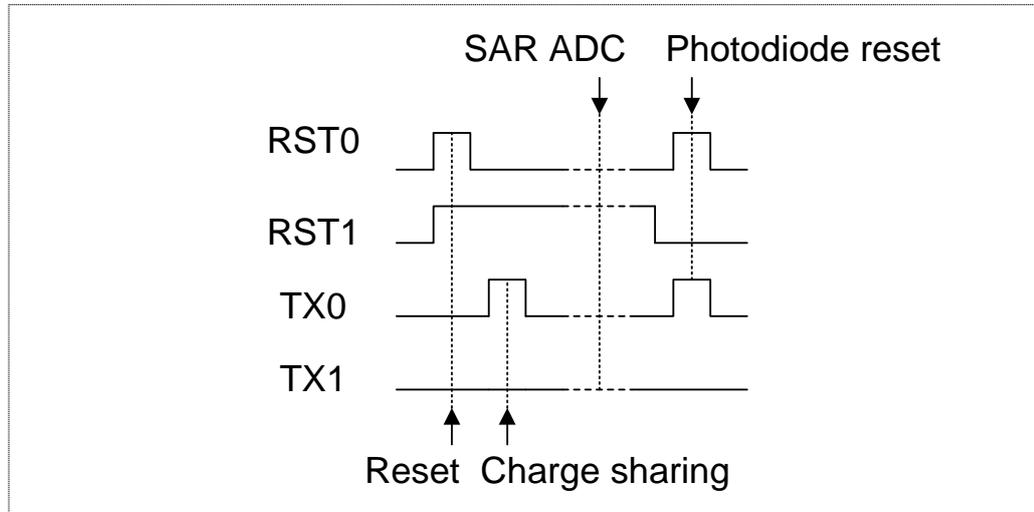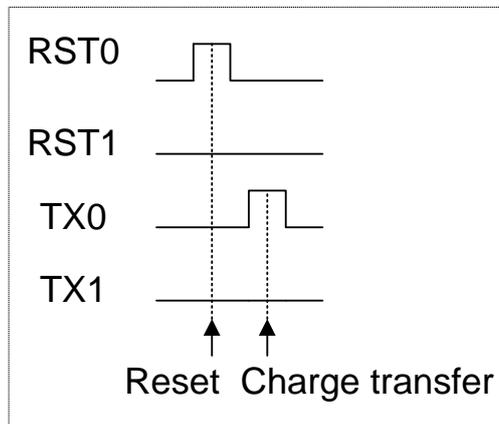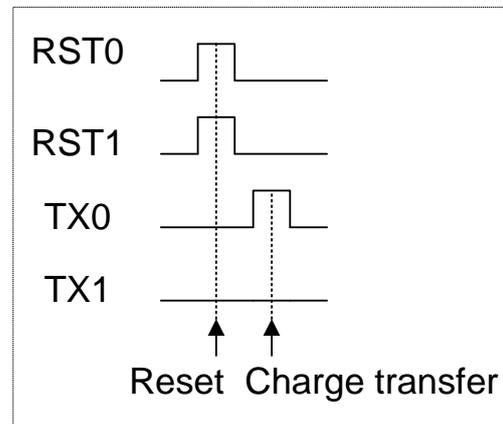
Figure 4.5 Timing diagram of the pixel control in each mode

Figure 4.7 shows the capacitive DAC for the SAR ADC. Since most power consumption comes from the driving of capacitances, we used a modified DAC with reduced capacitance [4.6]. Conventional DAC has total 2^8C capacitances for 8-bit conversion. In addition to large power consumption, placing capacitors in the small column pitch is also a problem. However, the modified DAC has only 47C total capacitances.

107

In order to adjust the signal swing, we used parasitic capacitance of 'RSTC' instead of employing additional reference capacitors or voltage generators.
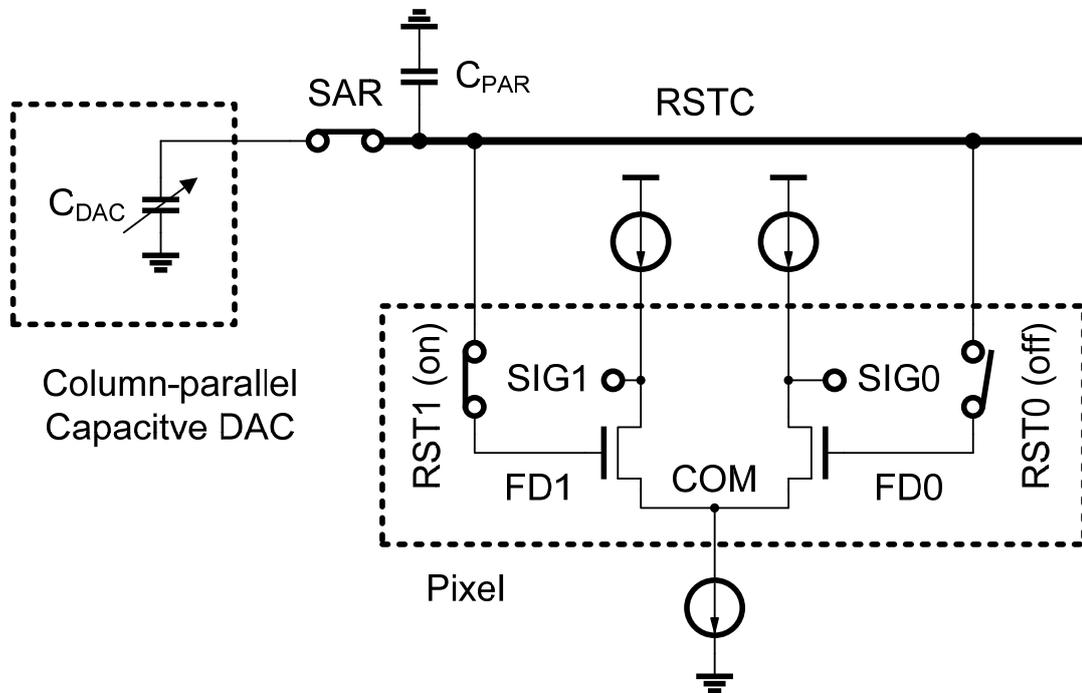
Figure 4.6 In-pixel SAR ADC in monitoring mode
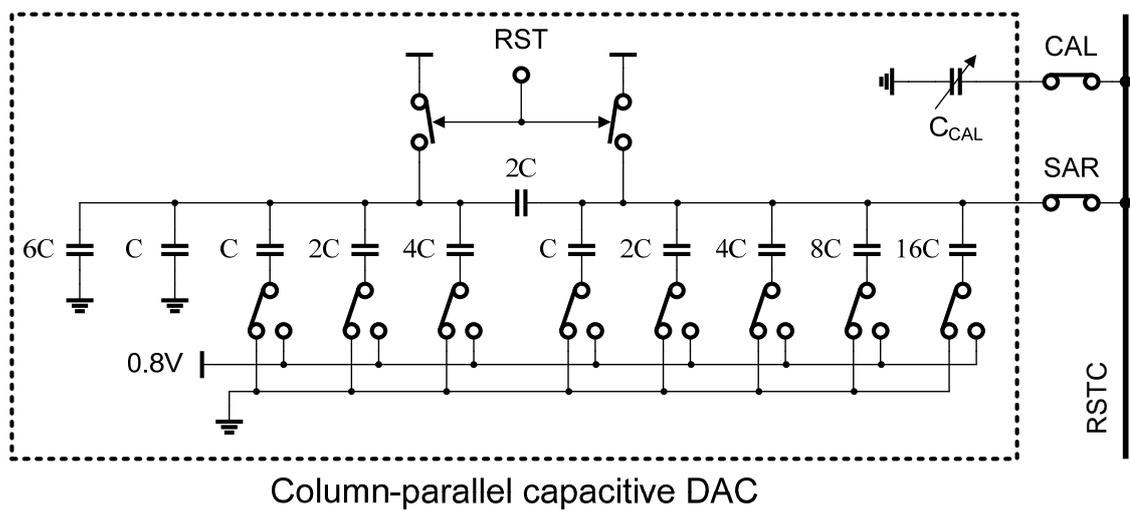
Figure 4.7 Capacitive DAC with reduced capacitance

The reference voltage of SAR ADCs in the monitoring mode is as follows:

$$V_{REF} = \frac{C_{DAC}}{C_{DAC} + C_{PAR}} V_{DD} \qquad\qquad (4.1)$$

, where C_{DAC} is DAC capacitance, C_{PAR} is the parasitic capacitance of RSTC line. In order to suppress the FPN from the parasitic capacitance variation, we added calibration capacitors C_{CAL} which are configured by 4-b digital signals. However, we did not have to use the calibration capacitors in the testing because we did not see any noticeable FPN from signal swing variation. The measured signal swing is 0.41 V out of 0.8 V power supply. Since the pixel operates at 0.8V, it is difficult to achieve a complete charge transfer from pinned photodiodes due to low reset level in the floating diffusion. Therefore, we chose to apply charge sharing. After integration, the floating diffusion node is reset and then the integrated charge is shared with the floating diffusion by opening the transfer gate. This operation disables true CDS like a 3-T pixel; however, we can achieve significant power savings.
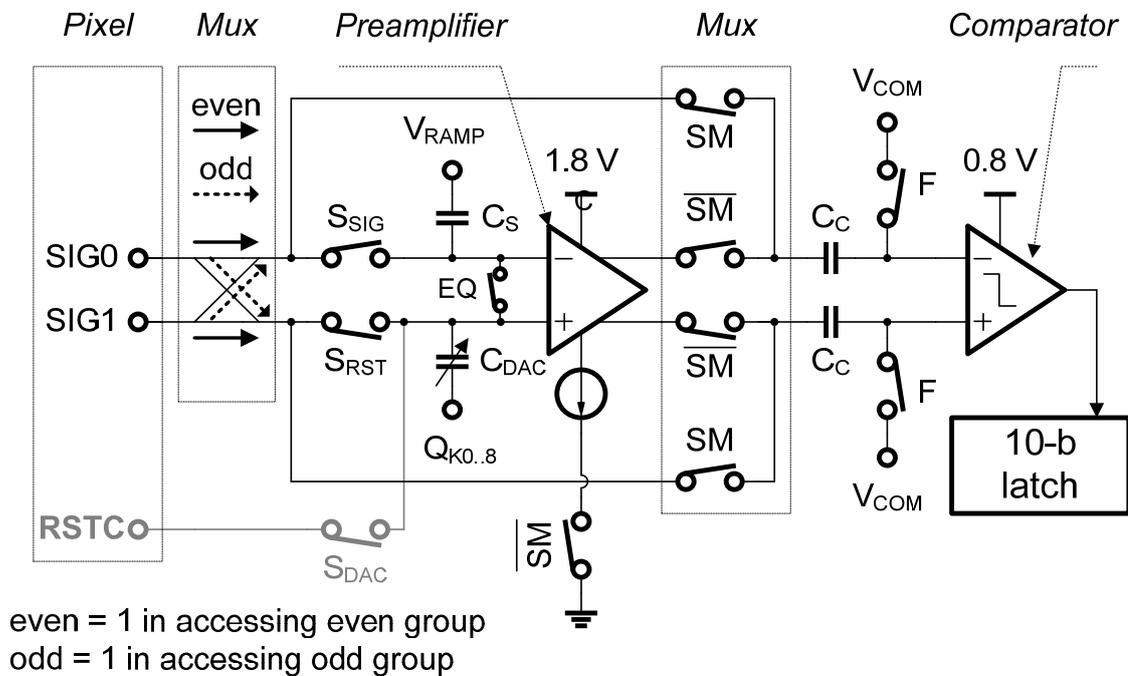
Figure 4.8 Column-parallel ADC for the reconfigurable modes

109

In normal mode, the pixel circuit is configured as a source follower that is exactly same as in conventional 4-T pixels. In high-sensitivity mode, the pixel operates as a differential common-source amplifier and achieves a higher gain (> 6). The differential common source amplifier generates the output signal from the two floating diffusion nodes: one gives a signal voltage and the other gives the reset voltage. In WDR mode, the same circuit is used as in the normal mode. In order to enhance the dynamic range, pixel merging with dual exposure is applied to the pixel. This will be explained in the next subsection.
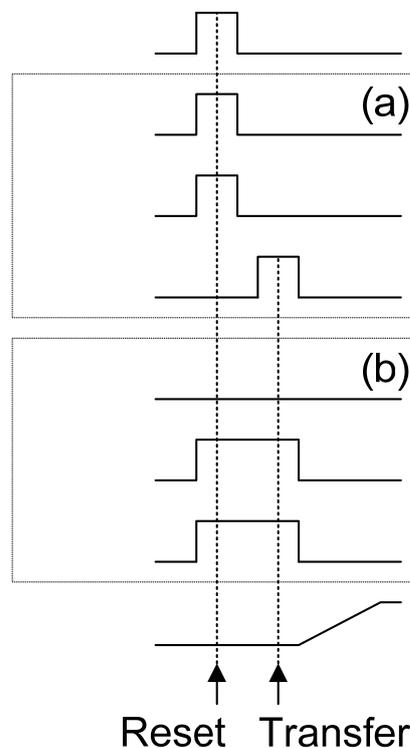
Figure 4.9 Timing diagram of column-parallel ADC (a) Single ended input (normal, WDR mode), (b) Differential input (high-sensitivity mode)

Figure 4.8 shows the column parallel ADC and figure 4.9 shows its operation. The column parallel ADC consists of a preamplifier operating at 1.8 V, a dynamic comparator at 0.8V, and switches for mode configuration. In monitoring mode, only 0.8 V supply is

110

used and column-level preamplifiers are turned off for power saving. The amplified signal from the pixel ('SIG0', 'SIG1') is directly delivered to the dynamic comparator through 'SM' for SAR ADC. In the other three modes, the column parallel ADC operates as a single-slope ADC. The coupling capacitor 'C_C' stores the offset of the preamplifier and suppresses the column FPN. In the normal and WDR modes, reset voltage is sampled in C_{DAC}, signal voltage is sampled in C_S, and then V_{RAMP} is swept. In case of high-sensitivity mode, the operation is fully differential, i.e., the differential signals from the pixel is sampled in C_S and C_{DAC} simultaneously.
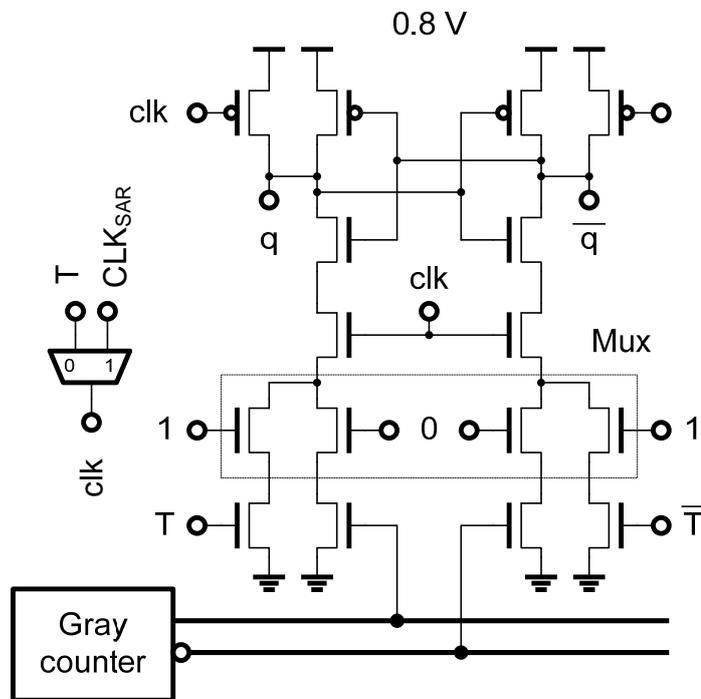
T: comparator output

Figure 4.10 Hybrid latch circuit

111
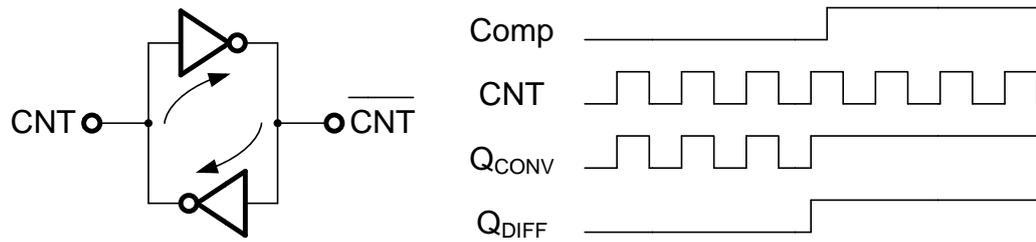
Figure 4.11 Comparison with conventional latch in single-slope ADC

Figure 4.10 shows the hybrid latch circuit. The latch operates for both SAR and SS ADC by multiplexing. Differential latching reduces switching power because it only switches once during the whole SS ADC cycles, while the SRAM or transfer-gate based flip-flop always changes its state whenever the counter signal changes. The switching characteristics of differential and conventional latches are shown in figure 4.11.

4.3 In-equality readout

Figure 4.12 shows conventional digital signal readout scheme.
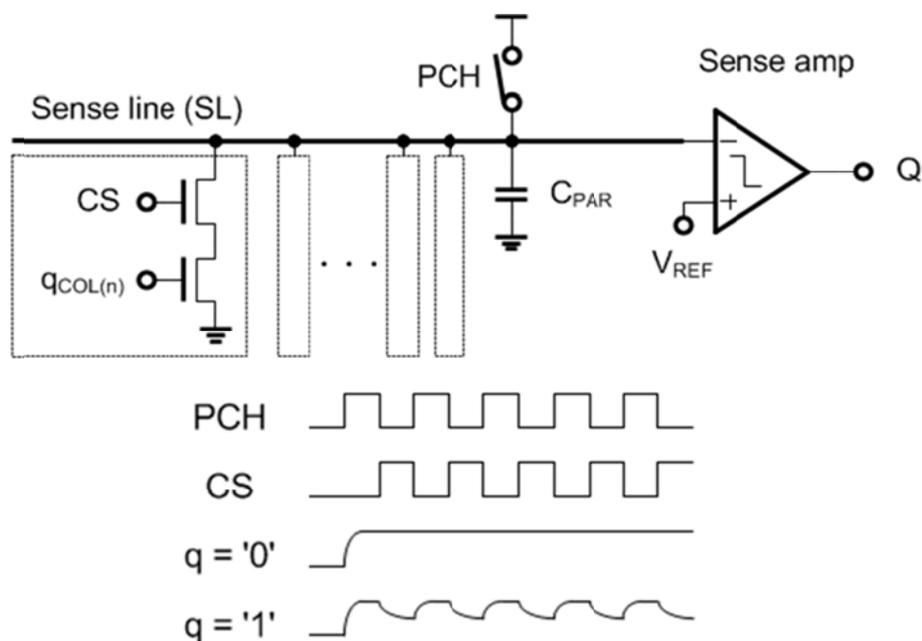
Figure 4.12 Conventional digital image signal readout circuit and operation

112

The precharged sense line (SL, sense amplifier input) is discharged through the readout cell according to the stored value in the latch.

Figure 4.13 Image locality

When the digital signals from the column latch are accessed, the precharged line may be frequently discharged by the readout cell according to the stored value in the latch. When the stored signal is '1', the precharged line is discharged and the line should be charged again for the next column readout. Precharging the sense line that has large capacitance entails huge dynamic power consumption.

Fortunately, the image signal has strong locality as shown in figure 4.13. It has high probability that neighboring pixels have similar values. In order to reduce the power consumption in the precharge node, we implement a scheme to read an inequality between neighboring columns since most image signals typically have locally similar values (low spatial bandwidth).

Figure 4.14 shows the digital signal readout circuit. We put XOR gates in the readout cell for upper 4 MSBs. One of the two XOR gate inputs comes from the left column. The

line keeps the pre-charged voltage if the two columns have the same value. In this case, there is negligible dynamic current. We tested with 100 images from the image database [4.7]. The probability of equality in each bit position is shown in Figure 4.15. The probability of equality is defined as Eq. 4.2. This plot is from the averaged result of 100 images. Figure 4.15 (a) shows the probability that 1-b digital signals in specific bit position are same in the neighboring columns. Figure 4.15 (b) shows the probability that 1-b digital signal in specific bit position is '1'. The probability of '1' is defined as Eq. 4.3.

$$P_{EQ} = \frac{\text{\# of pixels with equality}}{\text{Total \# of pixels}} \qquad (4.2)$$

$$P_1 = \frac{\text{\# of pixels with '1'}}{\text{Total \# of pixels}} \qquad (4.3)$$
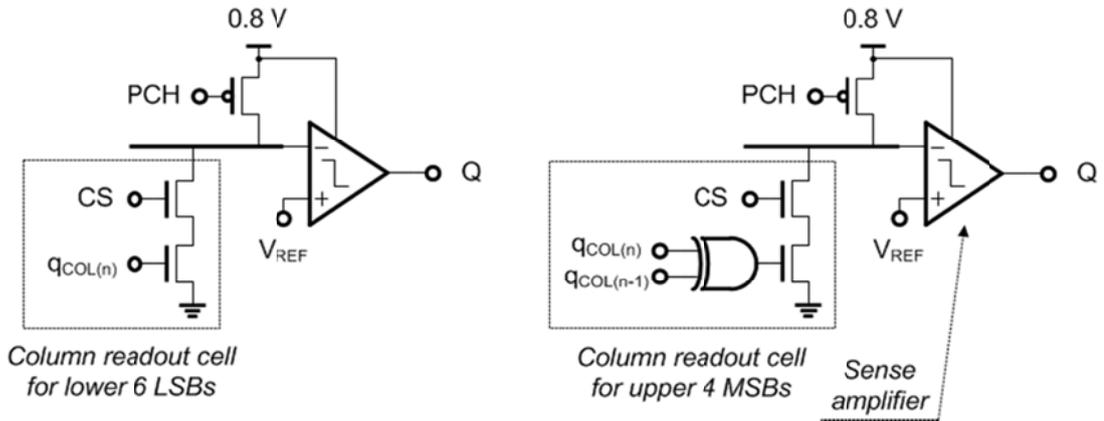
Figure 4.14 Digital image signal readout circuit with in-equality readout

The probability of equality means the probability of negligible dynamic current. As shown in the figure, the probability of equality is 0.73 (@ 4th bit) and 0.94 (@ MSB), whereas the probability of '1' is around 0.5. The power consumption overhead from the transmission gate based XOR is negligible. According to this analysis, we can achieve a power reduction of 68% (only from the pre-charge) and 5% from the total chip power in

the monitoring mode. The area overhead from XOR gates is only 0.36 % from the core size.
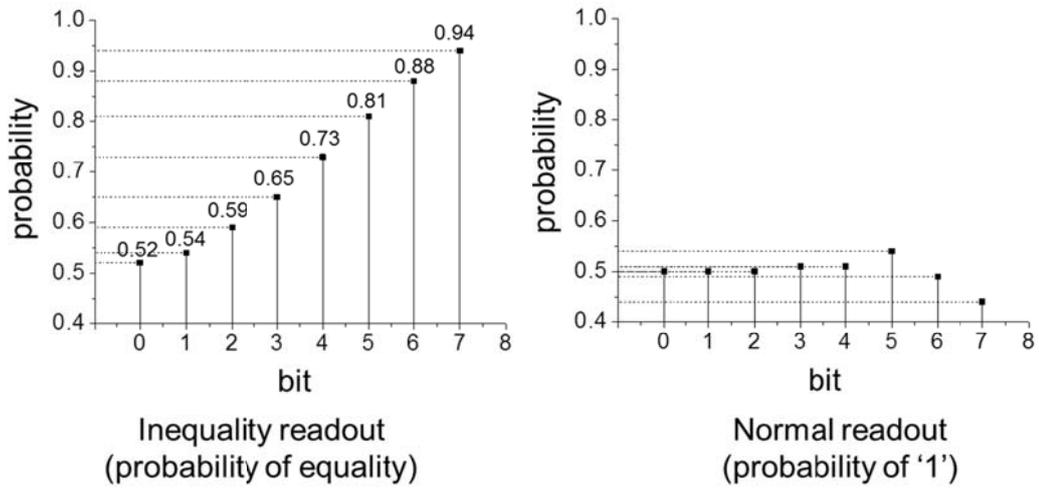
Figure 4.15 Averaged probability of equality

$$T_{INT2} = K \cdot T_{ROW} = T_{INT}/(M/K)$$
$$T_{INT} = M \cdot T_{ROW} = T_{INT1} + T_{INT2}$$
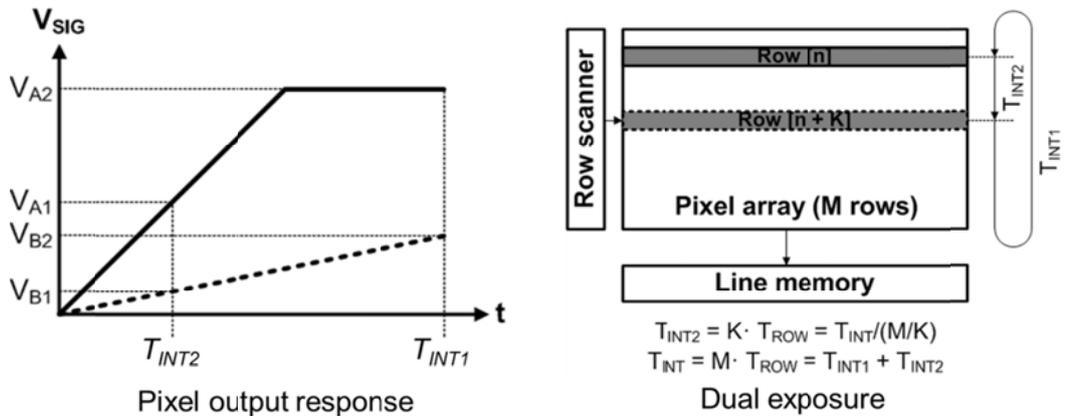
Dual exposure

Figure 4.16 Dual exposure scheme: pixel output response and conventional implementation

4.4 Dual exposure with pixel merging

As mentioned in chapter 3, dynamic range extension using the linear scheme such as the sensitivity adjustment and the multiple exposure schemes provide better SNR than nonlinear schemes. In the linear scheme, multiple exposure is better choice because the sensitivity adjustment requires in-pixel capacitors and this scheme is not applicable to the

shared pixel architecture. However, multiple exposure scheme requires additional line memories. It also entails large power consumption due to the multiple readouts.

In this work, we implemented a dual exposure scheme with pixel merging. The operation principle is shown in figure 4.16. The signal from short integration time (T_{INT2}) and the signal from long integration time (T_{INT}) are synthesized. As shown in the pixel output response, we can get the signal without saturation from the short integration time (T_{INT2}) in high illumination. In conventional dual exposure scheme, line memories are required for the synthesis as shown in figure 4.16. Moreover, two times readout doubles the power consumption from the readout.
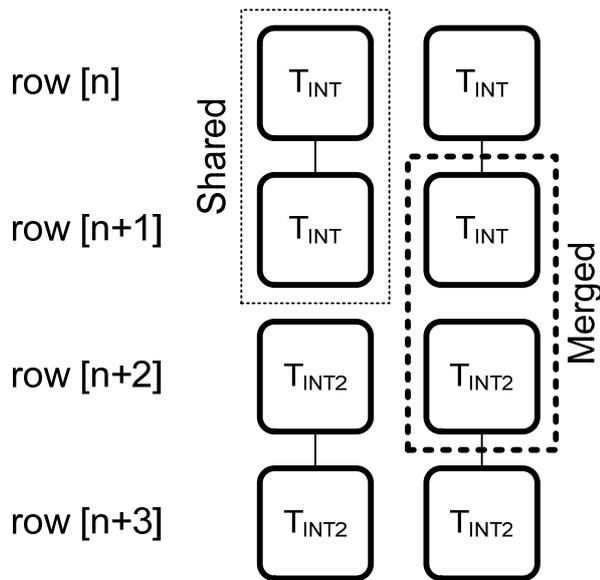
Figure 4.17 Dual exposure with pixel merging

In order to avoid additional line memory and additional power consumption, we proposed a dual exposure scheme based on the pixel merging. As shown in figure 4.17, the even group has a regular integration time (T_{INT}) and the odd group has a short integration time (T_{INT2}). In the readout, one row from the even group and one row from the odd group are merged, and generate a signal with enhanced dynamic range. This

116

scheme sacrifices the spatial resolution by half; however, it is adequate for low-power applications because no additional in-pixel element or image reconstruction is required and the operation is simple. Since we need only one time readout, no additional power consumption is required as the conventional multiple exposure schemes.
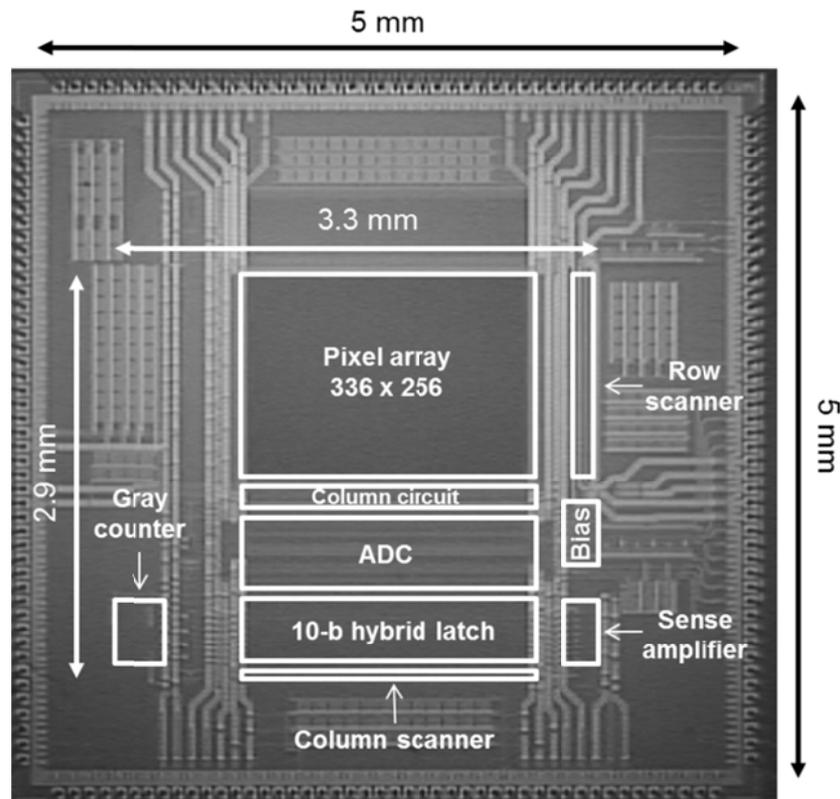
Figure 4.18 Chip microphotograph

4.5 Implementation and experimental results

A prototype chip has been fabricated using 0.18μm CIS process. A chip micrograph is shown in figure 4.18. The performance of the sensor is summarized in table 4.1.

Figure 4.19 shows the captured images from the fabricated device. Figure 4.19 (a) shows the image from the monitoring mode (@ 9 lx) and figure 4.19 (b) shows the image from the high-sensitivity mode in a dark condition (@ 0.4 lx).

Process	0.18 μm 2P4M CIS		
Core size	3.32 x 2.96 mm²		
Pixel size	5.6 x 5.6 μm²		
Pixel array	336 x 256		
Fill factor	45.5 %		
Dynamic range	57.1 dB (normal) / 99.2 dB (WDR)		
Mode	Normal	High sensitivity	Monitoring
Sensitivity [V/lx·sec]	4.02	23.9	0.65
FPN [%]	0.29	0.75	1.35
Power (Pixel array, @ 15 fps)	32.3 μW	69.6 μW	14.2 μW
Power (ADC analog, 1.8 V, @ 15 fps)	680 μW	736.3 μW	0.03 μW
Power (Digital, 0.8 V, @ 15 fps)	55.8 μW	61.4 μW	5.62 μW
Total Power (@ 15 fps)	768.1 μW	867.3 μW	19.9 μW (@ 15 fps)
			1.36 μW (@ 1 fps)
Power FOM [pW/pixel·frame]	595.32	672.2	15.4

Table 4.1 Chip characteristics
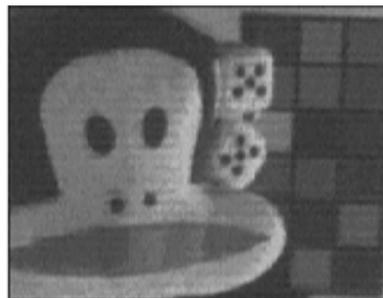
(a) Image from monitoring mode
(0.8V, 15 fps, 9 lx)

(b) Image from high-sensitivity mode
(1.8V, 15 fps, 0.4 lx)
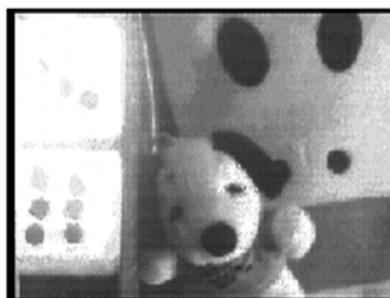
(c) Saturated image
(1.8V, 15 fps)

(d) Image from WDR mode
(merged with different integration time:
$T_{INT2} = T_{INT1}/16$, 1.8V, 15 fps)

Figure 4.19 Sample images

118

Figure 4.19 (c) shows the image from the normal mode when illumination high. The saturation from high illumination is eliminated in WDR mode as shown in figure 4.19 (d).

The power figure of merit (Power-FOM) can be defined as the power normalized to frame rate and the number of pixels, given by power/frame·pixel. This does not exactly reflect a good indication for the performance of image sensors because the power consumption of certain circuit blocks does not linearly increase as the pixel array size becomes large. More importantly, signal-to-noise ratio (SNR) can be significantly compromised with power consumption to the level that the acquired images are extremely poor. Another figure of merit, SNR-power FOM, can be defined considering both SNR and power consumption in its figures:

$$\text{SNR-Power FOM} = \frac{\text{SNR}}{\text{PowerFOM}} \times 10^{-12} [\text{dB}] \qquad (4.4)$$

We compared the SNR-Power FOM of our work with previous low-power CMOS imagers in table 4.2. When we calculate the FOMs of previous works, we used the whole chip power consumption and the reported SNR.

Ref	Pixel array	Pixel array	Power supply	Power FOM [pW/pixel·frame]	SNR [dB]	SNR-power FOM [dB]
[4.2]	In-pixel PWM	128 × 128	0.5	8.6	23.1	13.73
[4.8]	In-pixel PWM	128 × 96	1.35	468	52.9	24.67
[4.1]	Source follower	176 × 144	1.5	723.4	49.63	21.03
This work	In-pixel SAR	336 × 256	0.8	15.4	39.9	25.22

Table 4.2 FOM Comparison with Previous Works

We also plot the FOM in two axes: one is SNR and the other is Power FOM. We indicate a diagonal line that shows an equivalent SNR/Power-FOM line where the

projection of achievable SNR is estimated when additional power consumption is allowed.
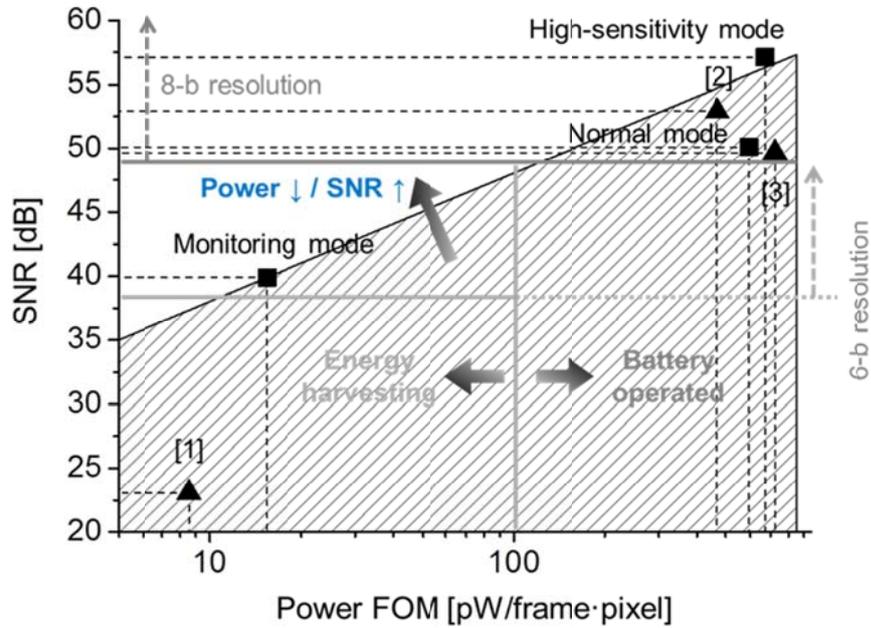
Figure 4.20 SNR vs. Power-FOM Plot

In the monitoring mode, the sensor should be able to operate solely depending on harvested energy. Then, the power FOM should be less than 100 [pW/frame/pixel] to be suitable for the operation of 1 μW @ 100×100 pixels, 1 fps. At the same time, in order to monitor the environment without severe performance degradation, the effective resolution of images should be over 6 bits (SNR = 36.1 dB). Further image processing in the sensor node or in the base station can enhance the SNR and provide reliable monitoring. Our sensor working in the monitoring mode satisfies this condition, while the other previous sensors cannot.

In order to get more accurate environmental data (high-sensitivity) or in extreme illumination conditions (wide-dynamic range), the sensor will adaptively change its mode of operation and the power source can be switched from energy harvester to a battery. For

these accurate image capturing modes, at least 8-b resolution (SNR = 48.2 dB) is required. As shown in figure 4.20, our sensor can provide adequate SNR in other modes of operation at the minimum power consumption. The sensor, however, will be mostly working in monitoring mode by default unless the special needs happen. During the monitoring mode, the extra energy harvested will recharge the battery. Considering both SNR and power FOM, this work shows the best performance as shown in the figure.

4.6 Summary

In this chapter, we explained the energy/illumination adaptive imaging. As a prototype, an adaptively reconfigurable CMOS imager has been designed and characterized. It operates at 1.36 µW in the monitoring mode from harvested energy and reconfigures to capture high-sensitive (24V/lx·sec) and wide dynamic range images (100dB) at 867 µW in battery operation upon request. The chip achieved power FOM of 15 pW/pixel·frame in 0.18 µm technology.

Chapter 4 References

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CHAPTER 5 OBJECT-ADAPTIVE IMAGE SENSOR WITH EMBEDDED FEATURE EXTRACTION FOR MOTION-TRIGGERED OBJECT-OF-INTEREST IMAGING

5.1 Introduction

The image signal transmission requires large bandwidth to transmit the 8-b M × N signals with 15 fps. The wireless transmission with high bandwidth requires high power consumption > 10 mW which is not feasible in wireless sensor nodes. Using the low-power transmission such as UWB still requires > 1 mW power consumption [5.1]. Therefore, it is important to reduce the bandwidth as well as reduce the power consumption of the image sensor. One way to reduce the bandwidth is to generate signals only when event happens by monitoring temporal changes [5.2-5.4]. However, this event-based imaging has extraneous redundancy because the sensor may also respond to environmental conditions, such as change of illumination or background movement in addition to actual target objects.

In this chapter, a motion-triggered object-of-interest (OOI) imaging to suppress the redundancy in imaging as well as transmission of signals will be explained. Figure 5.1 shows the operation procedure of the motion-triggered OOI imaging. In most of time the sensor is in sleeping mode until it is triggered by motion. Then it wakes up, it generates and transmits 8-b features for object detection. The signal processing unit which resides either in the host or in the sensor node, performs detection of objects and feeds back 1-b

request signal to initiate further imaging operation if the target object-of-interest is identified.

The feature extraction is the process that provides transformed representation sets with less bandwidth. There is a variety of image processing for the feature extraction: from simple low-level feature extraction that does not need shape information (for example: edge detection, curvature detection, optical flow estimation) to the complex high-level feature extraction that finds the shapes in the images (for example: Hough transform, template matching).

The object detection is the task of finding presence and position of the object. The object detection requires descriptors, which is a set of feature data describing the properties of image. By comparing and matching the descriptors with the descriptors of known objects, we can detect the object. The descriptor should be congruent, compact and invariant (for example, invariant to the orientation of the object or invariant to the illumination) [5.5]. A variety of algorithms for generating descriptor has been researched such as Haar wavlet, sacale-invariant feature transform (SIFT), shape context and so on. Among many feature extraction algorithms, we incorporated the histogram-of-oriented-gradients (HOG) because it gives a high detection rate of objects with simple operation [5.6]. The HOG feature is used in the human detection for applications of pedestrian detectors. Humans have been proven to be difficult object to detect due to the variability of appearance, cloth and articulation. While HOG feature provides powerful performance (i.e., low miss rate of detection) compared with other features including wavelets [5.7, 5.8], it has simple operation to be implemented in wireless sensor nodes. In this work, we implemented the HOG feature extraction algorithm using mixed-signal circuitry in order

to save both power and area. The HOG feature output requires only 3.5% of bandwidth when compared with conventional 8-b image capturing.
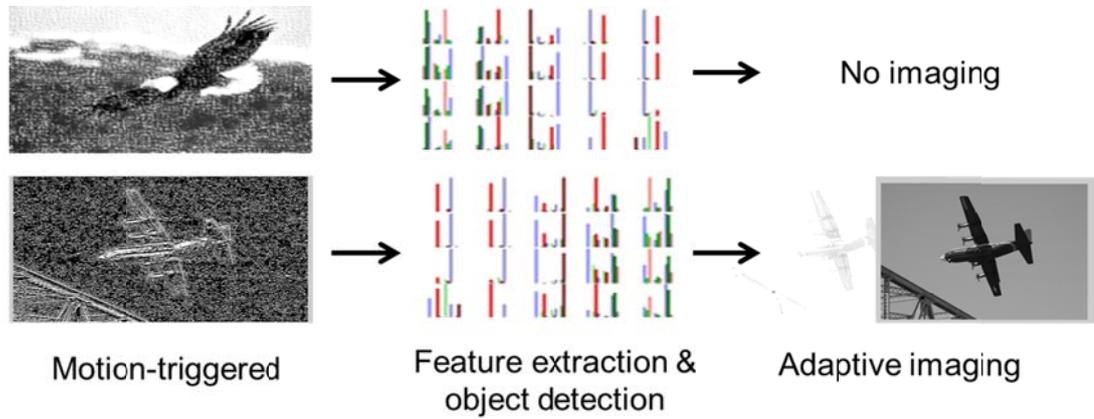
Figure 5.1 Motion-triggered object-triggered object-of-interest (OOI) imaging

For the object adaptive imaging, we implemented a prototype CMOS image sensor with an integrated histogram of oriented gradient feature extractor. The prototype chip has 256×256 pixel arrays and generates $L \times K \times 9$ 8-bit features (@ $256/L \times 256/K$ cell size) where the number of blocks $L \times K$ is controllable. In the case of 32×32 blocks, we can achieve $\times 113$ bandwidth saving compared with generating image signals. In the next section, the operation principles of the HOG feature will be explained. Then, the proposed CMOS image sensor with OOI imaging will be described.

5.2 Histogram of Oriented Gradients (HOG) feature

The HOG feature extraction procedure is shown in figure 5.2. The HOG feature extraction chain is as follows:

(1) **Spatial gradient** generation: apply two 1-D masks GX and GY for the x and y direction respectively. The masks are GX = [-1 0 1] and GY = [-1 0 1]^T. The result generates two $M \times N$ gradient images from the $M \times N$ image for x and y direction respectively.

125

(2) **Magnitude** and **angle** calculation: from two gradient images, calculate the magnitude |H| and angle θ as follows:

$$|H| = \sqrt{GX^2 + GY^2} \tag{5.1}$$

$$\theta = \tan^{-1}\frac{GY}{GX} \tag{5.2}$$

(3) **Voting**: each pixel is voted to 9 bin numbers (0 ~ 8), which decode the angle from 0° to 180° as shown in figure 5.2. For example, if the angle θ is 50°, then the bin number is 2.

(4) **Histogram** generation: M × N image is divided by L × K blocks. Each block has M/L × N/K pixels. Typically the block size M/L × N/K is over 8 × 8. Each block generates one histogram. Each histogram has 9 bin numbers as an index. According to the voting, the magnitude |H| is accumulated in each bin number. The accumulated magnitude in a cell will be finally normalized.

The histogram of oriented gradients shows the magnitude distributions in each angle. For example, if there is a horizontal pillar in the scene, the histogram will have the biggest magnitude accumulation in the bin number 4 (80° ~ 100°).

The block size (M/L × N/K) induces different detection result. Large cell size can generate the information over wide area instead of losing the details. Small cell size can generate detailed information but requires more processing. Some of object detectors have the classification algorithms that use multiple cell sizes in one detection procedure [5.9]. For example, the histogram from four different cell sizes 8 × 8, 16 × 16, 32 × 32 and 64 × 64 are concatenated as a feature set and the concatenated feature set is used for the classification.

As an integrated feature extractor in CMOS image sensors, it is desirable to implement the cell size programmable in order to be applicable to the different situations such as the object or the classification algorithm. Moreover, after the sensor generates the histogram with $M/L \times N/K$ cell size, histograms with multiple cell size can be generated by the post image processing, which can be applicable to the algorithm mentioned above.
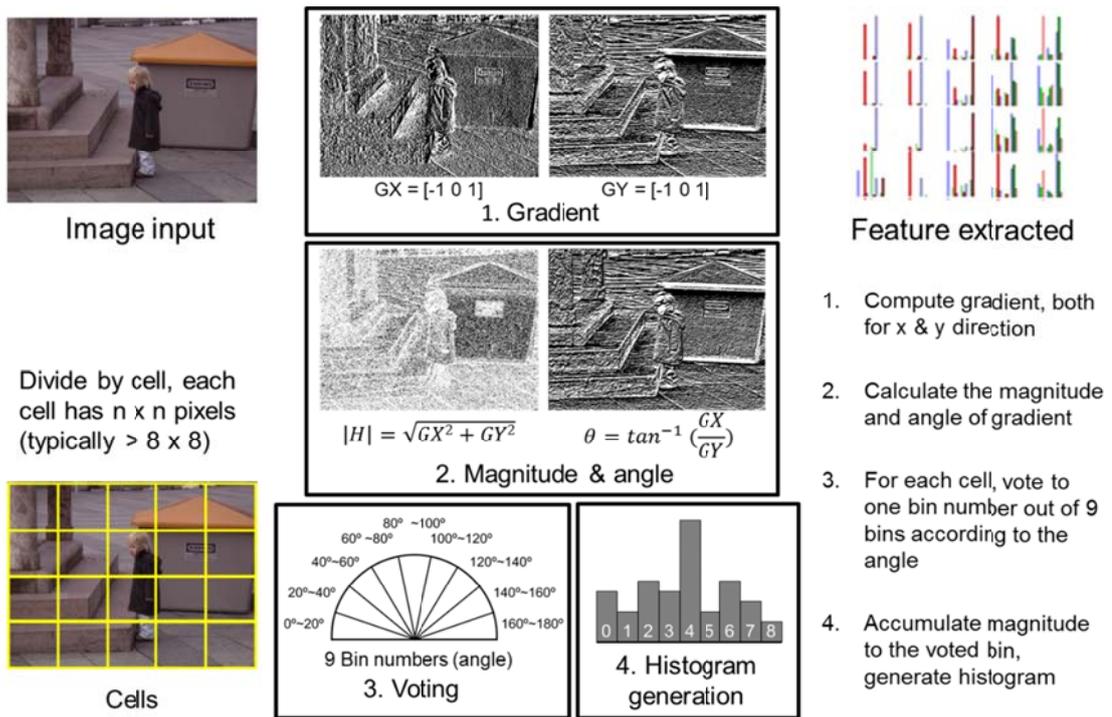
Figure 5.2 HOG feature extraction procedure

5.3 CMOS imager with motion-triggered object-of-interest imaging

5.3.1 Object-of-interest imaging

Figure 5.3 shows the simplified block diagram of three different modes of operation in the proposed sensor chip. In motion sensing mode, the sensor generates 128×128 1-b motion map for motion triggering. The column-parallel ADCs operate as a 1-b motion comparator. Once the motion is detected, the sensor wakes up and turns into the feature extraction mode. In this mode, the sensor generates and transmits 8-b feature signals that

are extracted from full 8-b 256 × 256 images. We have SRAM blocks, which temporarily store intermediate signals during HOG feature calculation. One part of SRAM blocks are allocated for line buffers to store 3 rows of images and the rest are allocated for feature signal accumulation. In imaging & storing mode, the sensor generates and transmits 8-b images upon the request from the host. The SRAM operates as a frame memory, which can store region-of-interest images containing the object-of-interest.
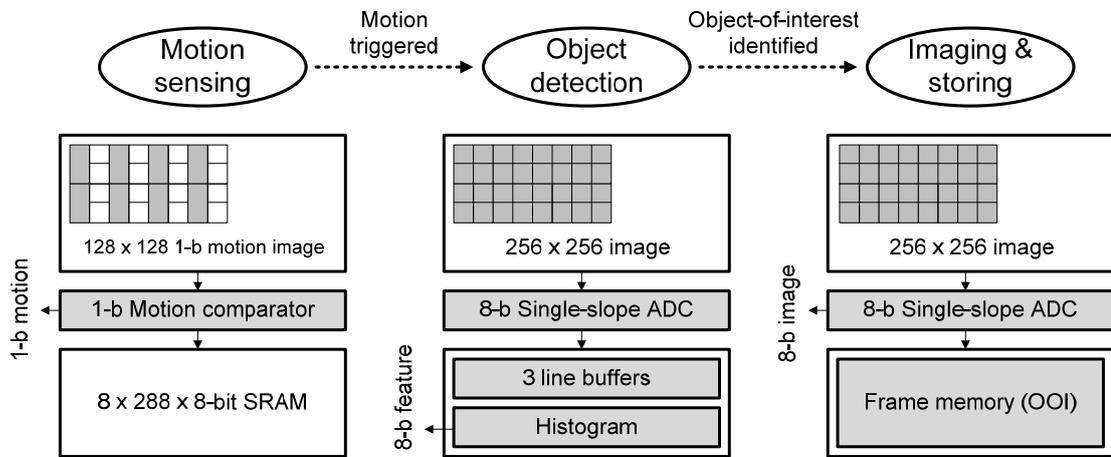
Figure 5.3 Operation of the motion-triggered object-of-interest imaging

5.3.2 Overall architecture

The overall architecture of the sensor is shown in figure 5.4. The column-parallel 8-b single slope ADCs operate as a 1-b motion comparator in the motion sensing mode and generates a 1-b motion map with frame-difference signals from the pixel. For HOG feature extraction, we need to calculate the magnitude and angle of spatial gradients. The pixel array is divided into m × m sub-blocks where the size of sub-blocks is fully programmable. A set of histogram that maps the magnitude of spatial gradients in each angle is generated for each block. The processing of feature signal extraction is as follows: (1) Three rows of images are read out and are temporarily stored in SRAMs; (2) Spatial gradients (GX and GY) are calculated with masking [-1 0 1] and [-1 0 1]^{T},

128

respectively; (3) Gradient-to-angle converter (GAC) generates 9 bin numbers, which map 9 different angles from 0° to 180°; and (4) Histogram generator accumulates the magnitude of gradients (|GX+GY|) corresponding to its angle (θ = tan-1(GY/GX)) calculated from GAC, and store them back to SRAMs. The accumulated magnitudes are normalized by K in order to deliver full-scale 8-b feature signals.
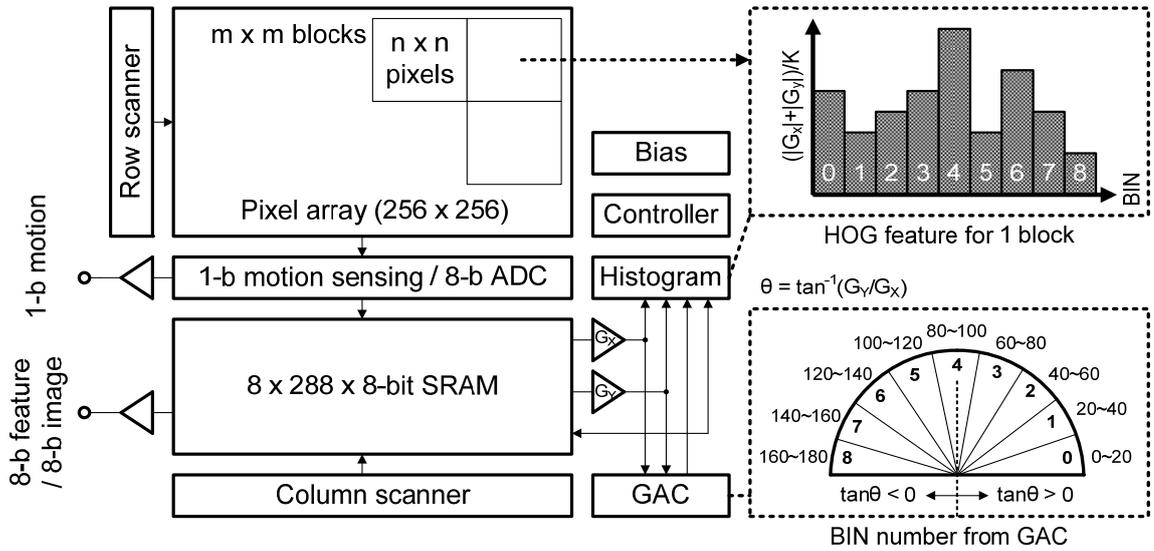
Figure 5.4 Overall architecture

5.3.3 Pixel circuit

Figure 5.5 shows the pixel architecture. The pixel employs a reconfigurable differential topology, which enables both source follower readout and differential common source amplification without any additional transistors, as reported in our previous work [5.10]. Two vertical neighboring pixels share the COM line and connect signals through SIG0 and SIG1. In this sensor, we used an additional in-pixel capacitor $C_{E/O}$ as frame buffer memory for motion sensing as well as for low-power imaging. The in-pixel capacitor is implemented using an MIM capacitor and it is placed on top of pixel

129

circuits. Therefore, the capacitor does not induce any fill-factor loss. Two vertically neighboring pixels are connected with a merging switch (M) for pixel merging.
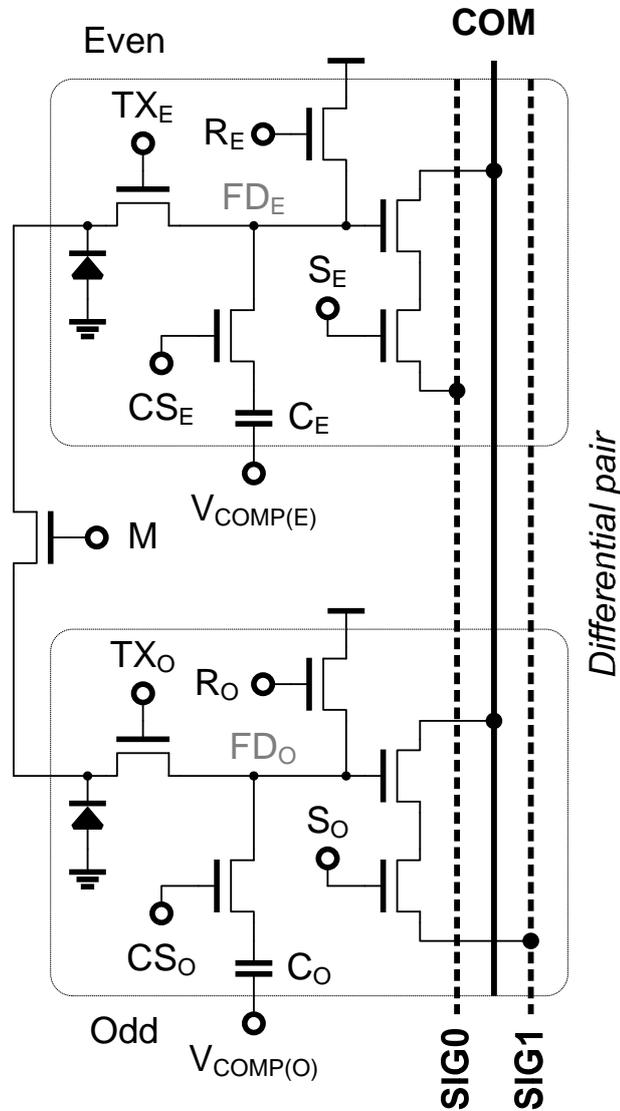
Figure 5.5 Pixel circuit

The equivalent circuit of the pixel is shown in figure 5.6. In the motion sensing mode, operation sequence is as follows: (1) Two pixels are merged and one in-pixel capacitor samples the previous frame signal (V_1); (2) The other in-pixel capacitor samples the current frame signal (V_2); (3) A short pulse is applied to $V_{COMP(E)}$ in the even pixel and

130

V_1 is compared with V_2; (4) Likewise, another pulse is applied to $V_{COMP(O)}$ in the odd pixel and two voltages are compared again. When the frame difference $|V_1 - V_2|$ is higher than the amplitude of V_{COMP} pulse swing, 1-b motion output is generated.

Motion sensing

Low-power imaging

Figure 5.6 Equivalent pixel circuit for motion sensing and low-power imaging

For low-power imaging in the feature extraction mode, the pixel circuit operates as a pre-amplifier for an 8-b single slope ADC. The integrated charges in a photodiode are transferred to an in-pixel capacitor in the even pixel whereas the odd pixel keeps the reset voltage. A ramp signal is applied to $V_{COMP(E)}$ and the potential is dropped at SIG0 node

131

due to charge transfer. The latching occurs around the reset voltage. In this scheme, V_{GS} drop in the amplification transistors does not induce the loss of signal swing as in the conventional source follower readout; i.e., the power supply can be scaled down by more than 0.5 V (nominal voltage drop in V_{GS}). In this sensor, we used 1.3V for pixel power supply which significantly saves power consumption in the pixel circuits.

5.3.4 Column circuit

Figure 5.7 shows the column circuit. The column circuit consists of the column-parallel 8-b ADC and SRAMs.
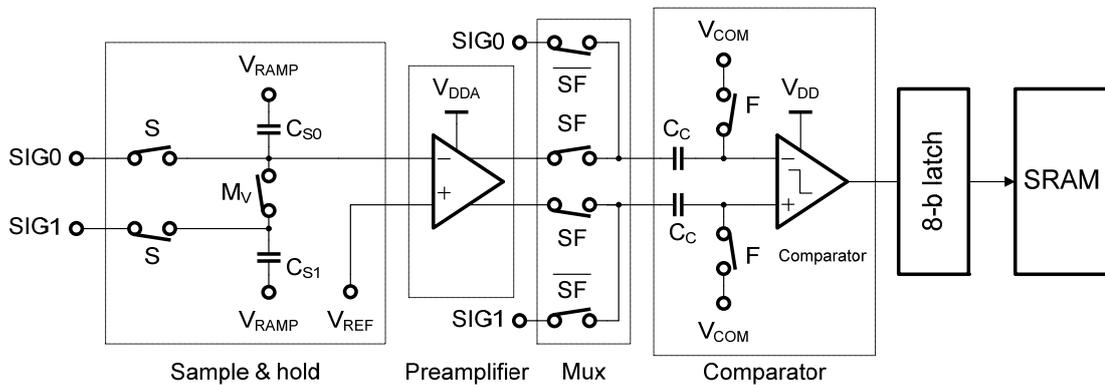
Figure 5.7 Column circuit

The ADC consists of sample & hold circuit, preamplifier, multiplexer, comparator and 8-b latch. Note that the sample & hold circuit and the preamplifier are used for the readout from the in-pixel source follower only for the testing purpose. The preamplifier is turned off in actual operation. In actual operation, the differential signal line SIG0,1 are directly connected with comparator inputs through the multiplexer. The offset voltage of the in-pixel differential comparator is stored in the capacitor C_C in order to suppress the FPN from the offset voltage. When F is enabled, the output from the reset voltage is sampled on C_C. After F is disabled, integrated charges are transferred and ramp signal is

132

swept for the AD conversion. The power supply voltage of the column circuit (V_{DD}) is 0.8 V.

5.3.5 Gradient-to-Angle Converter (GAC)

Figure 5.8 shows the voting process. Since the angle θ can be expressed as $\tan^{-1}$(GY/GX), we can decode the angle into 9 bin numbers using the following equation:

$$\tan\theta = \frac{GY}{GX} \qquad\qquad (5.3)$$
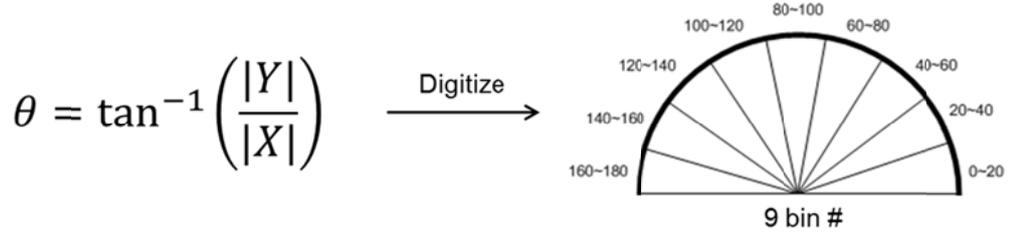
Figure 5.8 Voting process

In order to decode with 9 bin numbers using the above equation, tanθ should be compared with the result from a divider. This operation requires a divider, also a look-up table for the trigonometric function. Instead of using the complex operation, we proposed a simple mixed-signal approach in order to avoid digital implementation, which consumes huge area/power. The gradient-to-angle converter (GAC) circuit based on the mixed-signal approach is shown in figure 5.9. The timing diagram of GAC is shown in figure 5.10. The GAC generates 9 angle information from 0° to 180° in 4-b bin numbers. The 8-b gradient signals (GX and GY) are converted to analog signals using two binary capacitive DACs. When the switch S1 is off, the binary DAC output is divided by two. One capacitor (C0,1) operates as the part of DAC, which generates trigonometric function, while the other (C0s,1s) operates as a hold capacitor, which contains the gradient.
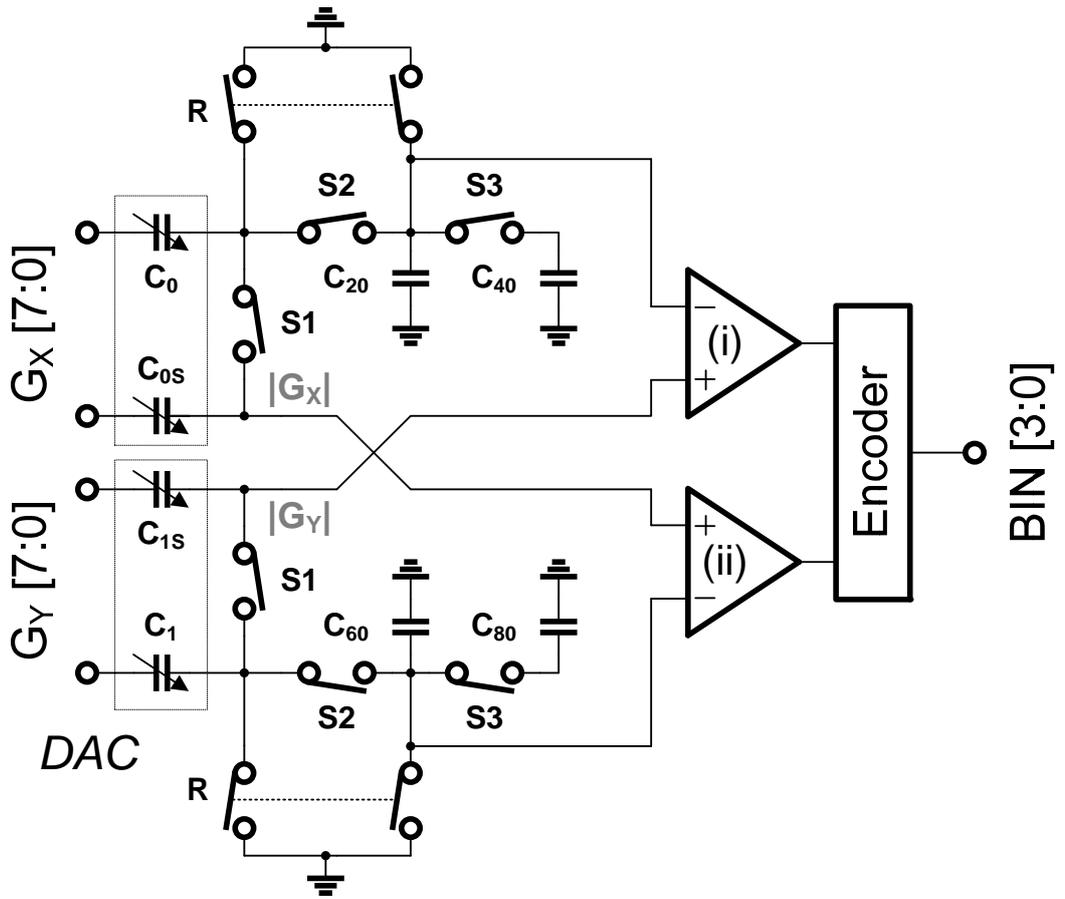
Figure 5.9 Gradient-to-angle converter (GAC)
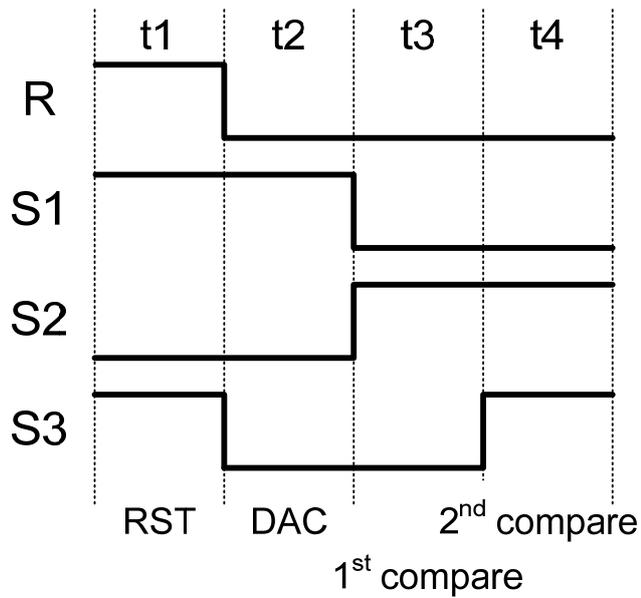
Figure 5.10 Timing diagram of gradient-to-angle converter (GAC)

The gradient is multiplied by tanθ and 1/tanθ in each channel, respectively, according to capacitance values of C20, C40, C60, and C80.

	(i) $|GX| \cdot \tan\theta = |GY|$ (tanθ<1)	(ii) $|GX| = \frac{|GY|}{\tan\theta}$ (tanθ>1)
t3	$\dfrac{C_0}{C_0 + C_{20}} = \tan 40°$	$\dfrac{C_1}{C_1 + C_{60}} = \dfrac{1}{\tan 60°}$
t4	$\dfrac{C_0 + C_{20}}{C_0 + C_{20} + C_{40}} = \tan 20°$	$\dfrac{C_1 + C_{60}}{C_1 + C_{60} + C_{80}} = \dfrac{1}{\tan 80°}$

Table 5.1 Capacitance ratio in the GAC

The proposed GAC performs two comparisons in parallel using two comparators. The comparison is as follows:

$$|GX| \cdot \tan\theta = |GY| \ (\tan\theta < 1) \tag{5.4}$$

$$|GX| = \frac{|GY|}{\tan\theta} \ (\tan\theta > 1) \tag{5.5}$$

Angle	Sign of Y/X	GAC result (80/60/40/20)	Decoded BIN
0° ~ 20°	+	0000	0000
20° ~ 40°	+	0001	0001
40° ~ 60°	+	0011	0010
60° ~ 80°	+	0111	0011
80° ~ 90°	+	1111	1111
90° ~ 100°	-	1111	1111
100° ~ 120°	-	0111	0111
120° ~ 140°	-	0011	0110
140° ~ 160°	-	0001	0101
160° ~ 180°	-	0000	0100

Table 5.2 Encoding of 9 bin numbers

In the first comparison, |GY| is compared with |GX| · tanθ. In the second comparison, |GX| is compared with $\frac{|GY|}{\tan\theta}$. In each comparison, two-step comparisons are performed. In the first comparison, θ is 40° in the first step and is 20° in the second step. This two-step comparison divides the range of the angle as follows: θ > 40° or 20° < θ < 40° or θ < 20°. Likewise, in the second comparison, θ is 60° in the first step and is 80° in the second step. This two-step comparison divides the range of the angle as follows: θ < 60° or 60° < θ < 80° or θ > 80°. Each step generates 1-bit comparison result. Therefore, total 4-bit output is generated from two two-step comparison. Since tanθ = - tan(180° − θ), we don't need to do the operation for the angle higher than 90°. In other words, the comparison only cares about the magnitude of tanθ and detects the angle range from 0° to 90°. The sign bit (which we already have generated from the gradient calculation) shows whether the decoded angle is in 0° < θ < 90° or in 90° < θ < 180°. After two-step comparisons during t3 and t4, the 4-bit output from the comparison is encoded according to the sign bit (S) in order to generate a final bin number. Table 5.2 shows the encoding table. The sign bit determines whether the encoded angle is in 0° < θ < 90° or in 90° < θ < 180°.

5.4 Chip characteristics and object detection simulation

The prototype chip has been fabricated using 0.18 μm 1P4M CMOS process. Figure 5.11 shows the chip microphotograph. The core size is 2.35 × 3.18 mm². Figure 5.12 shows the captured images from the fabricated device including a 128 × 128 1-b motion map and a 256×256 8-b image from the in-pixel single-slope ADC. A 256 × 256 angle map shows the angle calculated from the GAC. A 8-b feature from 8 × 8 blocks are

shown with the vector. In this figure, only two angles that have the biggest magnitude are shown for simplicity.
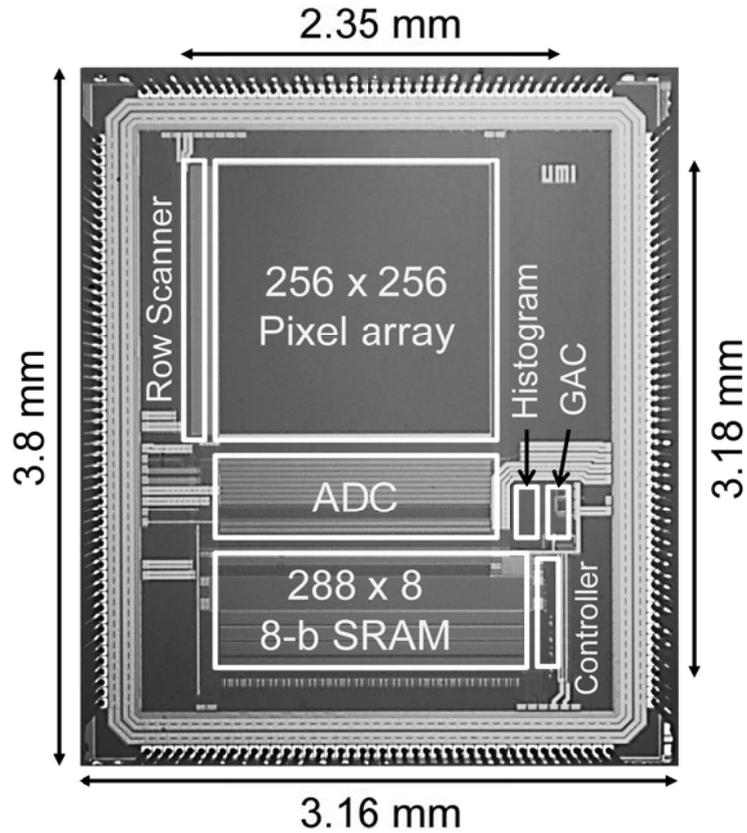
Figure 5.11 Chip micrograph

The performance of the sensor is summarized in table 5.3. We achieved a normalized power of 13.46 pW/frame•pixel in motion sensing and 51.94 pW/frame•pixel in feature extraction. In order to verify the performance of the integrated feature extraction unit, we tested the object detection from the extracted features using 200 pedestrian images from DaimlerChrysler dataset [6.10]. For testing, we input test images serially into the 8-b latch in the column parallel ADC and generated feature. The test result shows 94.5 % detection rate. The detailed procedure of the object detection will be described in section 5.4.1.

(a) 256 x 256 8-b image from low-power imaging
(b) 128 x 128 1-b motion map

(c) 256 x 256 4-b angle map from the GAC

8x8x9 8-b histogram

From the scene   From the test pattern
(d) 8 x 8 8-b features
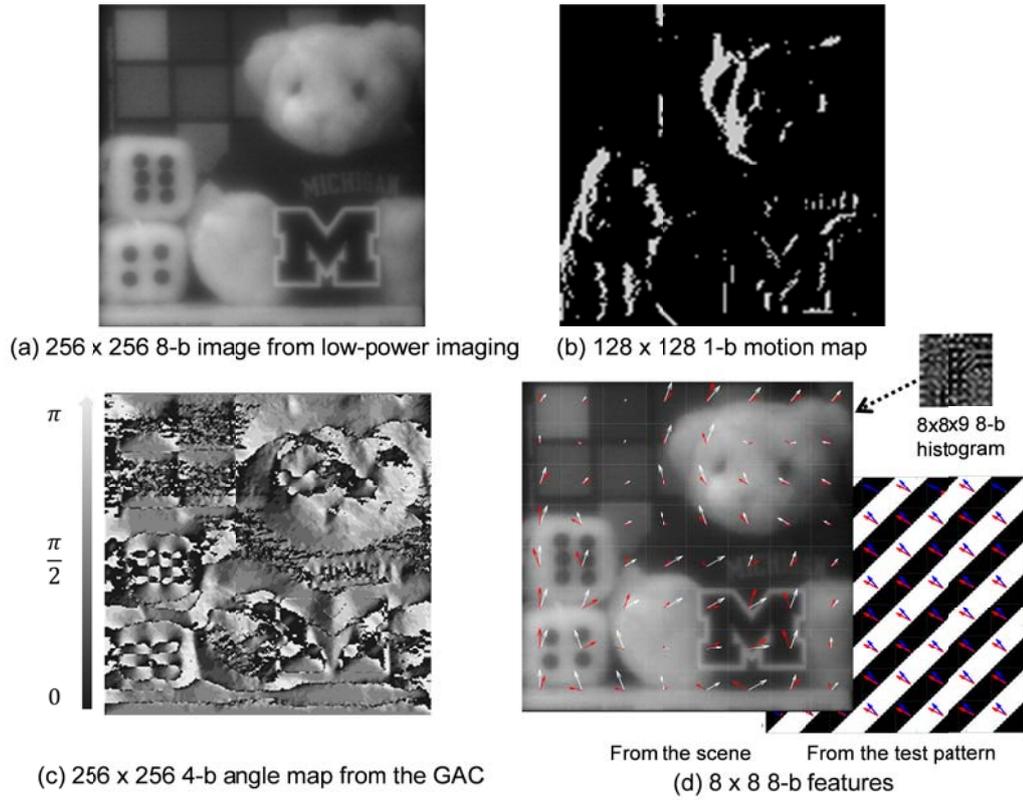
Figure 5.12 Sample images

Process	0.18 µm 1P4M CMOS			
Core size	2.35 x 3.18 mm²			
Pixel size	5.9 x 5.9 µm²			
Pixel array	256 x 256			
Fill factor	30 %			
FPN	0.05 %			
Dynamic range	54.8 dB			
Power supply	Pixel		1.3 V	
	Digital		0.8 V	
Power consumption & Power FOM	Mode	Power (@ 15 fps)	Power / frame	FOM (power/pixel•frame)
	Motion sensing	3.31 µW	0.22 µW	13.46 pW
	Imaging with feature extraction	51.06 µW	3.4 µW	51.94 pW
Detection rate of object detection	94.5 %			

Table 5.3 Chip characteristics

138

5.4.1 Testing of the object detection

Figure 5.13 shows the object detection procedure. The object detection requires classifier with embedded classification algorithm. The classifier identifies the object-of-interest and generates 1-b output of the detection result. In order to classify the object, pre-trained model has to be loaded on the classifier. The training requires another algorithm such as support vector machine (SVM), which is supervised learning model with associated learning algorithms that analyze the data and recognize the patterns.
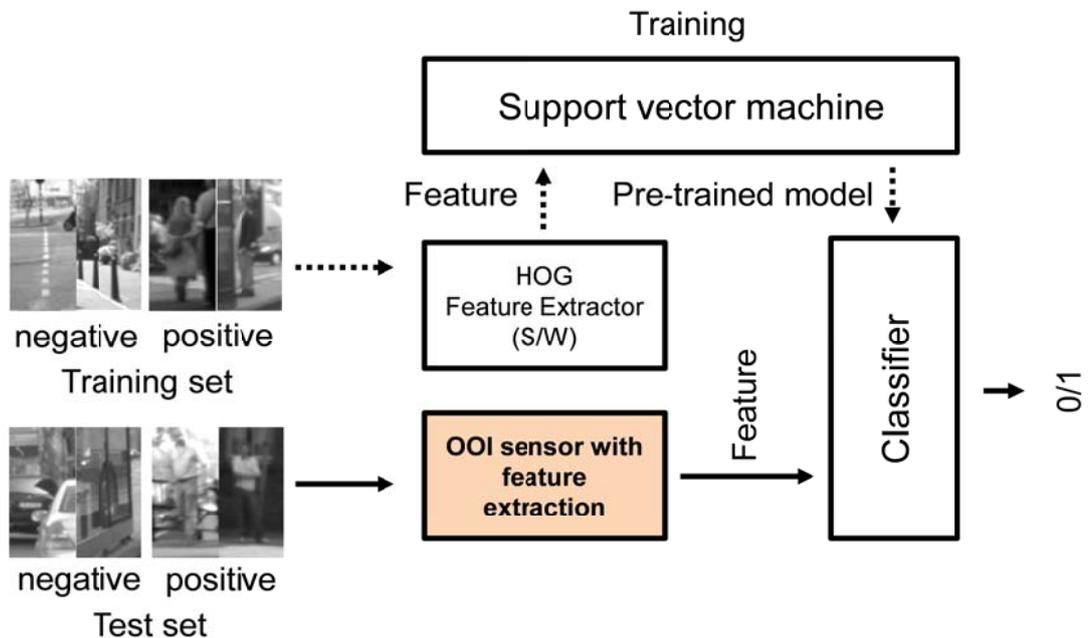
Figure 5.13 Object detection procedure

For the training, usually lots of images (training image set) more than 1,000 are used. This training set includes both the positive images (with the target object) and the negative images (without target object). For the object detection testing, a different set of images (test image set) are used. The feature is input to the trained classifier and the detection rate can be measured. In this work, we used simple SVM for the training and SVM classifier without any advanced algorithms in the MATLAB. We used 1,000

training images (500 positive, 500 negative) for the training [6]. In order to measure the detection rate, we used 200 test image sets (100 positive, 100 negative) [6.10]. The test images are serially input to the latch in the single-slope ADC and generated HOG feature from the fabricated chip are input to the classifier. According to the measurement, it shows 95% detection rate for the positive image set and 94% detection rate for the negative image set. The overall detection rate is 94.5 %. We expect improved detection rate by using advanced training and classification algorithms [6.9].

5.4.2 Power figure of merit (FOM) comparison with previous low-power imagers

The proposed CMOS imager with object-of-interest imaging consumes low power applicable to wireless sensor network applications. In low-power sensors, a small pixel pitch is an important factor because the parasitic capacitance of metal line (C_m) is linearly increased according to the pixel pitch (W_{PIXEL}) as shown in Eq.5.6

$$C_m = N_{PIXEL} \cdot W_{PIXEL} \cdot c_m \qquad (5.6)$$

In Eq.5.6, N_{PIXEL} is the number of pixels and c_m is the parasitic capacitance per μm. Since the power consumption is proportional to the capacitance, low-power sensors should have small pixel pitch. However, small pixel pitch decreases the sensitivity of the pixel due to reduced fill factor. Therefore, it is important to keep high fill factor while reducing the pixel pitch. Many low-power sensors use additional in-pixel circuits [6.1-6.3] or pMOS transistors [6.4] for the in-pixel event generation or in-pixel ADC.

In this work, we use the differential pixel topology by grouping two vertically neighboring pixels in order to achieve in-pixel ADC without additional transistors. The additional in-pixel memory is implemented with MIM capacitor and it is located on the top of pixel circuits in order to keep small pixel pitch. In this way, we achieved 5.9 μm

pixel pitch with 30% fill factor. For the comparison of power consumption, the power figure of merit (FOM) is typically used. The power FOM is defined as the power normalized to frame rate and the number of pixels, given by power/frame·pixel. Table 5.4 shows the power FOM comparison. The proposed sensor has 13.46 pW power FOM in the motion sensing, 51.94 pW in the feature extraction including the imaging power, and it shows the lowest power consumption as shown in the table.

Ref.	[6.4]	[6.5]	[6.3]	[6.2]	[6.1]	This work
Process	0.5 μm CMOS	0.35 μm CMOS	0.5 μm CMOS	0.18 μm CMOS	0.18μm CIS	0.18μm CMOS
Pixel array	90 x 90	128 x 64	64 x 64	64 x 40	320 x 240	256 x 256
Pixel pitch	25.2 μm	26 μm	33 μm	10 μm	5.6 μm	5.9 μm
Fill factor	17 %	20 %	11.5 %	25.4 %	45.5 %	30 %
Integrated feature extraction	Temporal change	Contrast change	Temporal change	-	-	Temporal change + HOG
Power FOM	17,700 pW	244 pW	1373 pW	163 pW	15.4 pW (monitor)	13.46 pW (motion)
					595.3 pW (normal)	51.94 pW (feature)

Table 5.4 Comparison with previous low-power sensors

5.5 Summary

In this chapter, the object-adaptive image sensor with embedded feature extraction for motion-triggered object-of-interest imaging has been described. The sensor wakes up triggered by motion sensing and extracts features from the captured image for the detection of object-of-interest. Full image capturing operation is performed only when the interested objects are found, which significantly reduces power consumption at the sensor node. The chip operates at 0.22 μW/frame in motion sensing mode and operates at 3.4 μW/frame for feature extraction, respectively.

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pp. 114-116, Feb. 2012

[5.12] Daimler Pedestrian Benchmark Datasets

(http://www.gavrila.net/Research/Pedestrian_Detection/)

CHAPTER 6 CONCLUSION AND FUTURE WORK

This thesis presents an environment-adaptive CMOS image sensor for energy-efficient operation. This chapter summarizes the main contributions and future directions of adaptive sensors.

6.1 Conclusion and summary of contributions

Main contributions of the completed work are summarized as follows:

(1) Implementation of adaptive imaging at low-power consumption ($< 1.36 \, \mu W$) with high dynamic range (99 dB) and low data rate ($< 3.5 \, \%$);

(2) Low power imaging at the best SNR-power FOM of 25.22 dB among the work reported up to date; and

(3) Low power imaging with feature extraction at the best power FOM (51.94 pW) among the work reported up to date.

We proposed an adaptive image sensor that is applicable to wireless distributed image sensor networks and wireless biomedical imaging systems. The adaptive imaging includes: (1) the energy-adaptive imaging for the low-power consumption, (2) the illumination-adaptive imaging for high dynamic range, and (3) the object-adaptive imaging for spatial-temporal bandwidth savings. In order to prove the feasibility of the proposed adaptive imaging schemes, we designed two prototype chips: one for the energy/illumination adaptation, and the other for the object adaptation. Both prototype sensors have been fabricated and fully characterized.

144

For the energy adaptation, we implemented the low-power monitoring operation in the adaptive image sensor. The sensor keeps monitoring at an extremely low power < 1.36 µW/frame, and only turns into high sensitivity or wide dynamic range imaging operation when the power delivery is enough from energy harvesting units. In-pixel SAR ADCs enable the voltage scaling down to < 0.8 V without any significant loss of signal swing and non-linearity. The differential latches in the single slope ADC further reduce the switching power. The in-equality readout scheme is also introduced to reduce the number of switching at the output.

The illumination adaptation extends the dynamic range for reliable imaging in wide range of illumination. At low illumination, the pixel circuit is reconfigured to become a high-gain amplifier, and provides high sensitivity of 23.9 V/lx·s. At high illumination, in-pixel dynamic range extension is performed using pixel merging and dual exposure readout. This scheme significantly saves the chip size compared with conventional schemes, and consumes less power compared with the multiple exposure schemes. The sensor provides high dynamic range over 99 dB.

The object adaptation has been implemented by identifying the object-of-interest (OOI) from the features extracted from image signals. The sensor wakes up triggered by motion sensing and extracts features from the captured image for detection of the object-of-interest. Full image capturing operation is performed only when interesting objects are found, which significantly reduces bandwidth and power consumption of the sensor node. The fabricated chip operates at 0.22 µW/frame in the motion sensing and operates at 3.4 µW/frame in the imaging with feature extraction.

In summary, the adaptability enables an energy-efficient image sensing in continuously varying environmental conditions such as illumination, energy harvesting, and a variety of objects captured in the focal plane. By accommodating the three adaptation schemes, the fabricated image sensor could provide high dynamic range images at low power consumption, while maintaining low bandwidth in image signal transmission.

6.2 Future adaptive image sensor

For the complete system, the adaptive image sensor should incorporate other processing units including power management units and control blocks for self-decision making, and also has to be mounted on a platform suitable for the deployment in a distributed image sensor networks and for portable biomedical imaging systems.

6.2.1 Adaptive imaging system-on-a-chip

In the previous works, the energy/illumination adaptation and the object adaptation capability have been implemented separately in the two prototype chips. In the future sensor platform, all adaptive imaging capabilities should be integrated in a single chip in order to achieve low-cost and small form-factor as well as low power consumption. In the two prototype chips that we designed, some parts of control signals has been generated from the off-chip FPGA that is mounted on the testing board for flexibility in characterization. In the future design, all control blocks as well as other essential circuit blocks have to be integrated on a chip, especially power management units (PMU) and wireless transmitters. The power management unit (PMU) selects the energy source either from energy harvesting units or from batteries, and it generates multiple power supply voltages for the entire sensor unit.

146

The controller is essential in order to manage the adaptive operation. The controller should include: energy source monitoring, illumination-level analysis from previous frame signals, motion triggering from the motion sensor output, and object detection algorithm. The overall architecture of the adaptive imaging SoC is illustrated in figure 6.1.
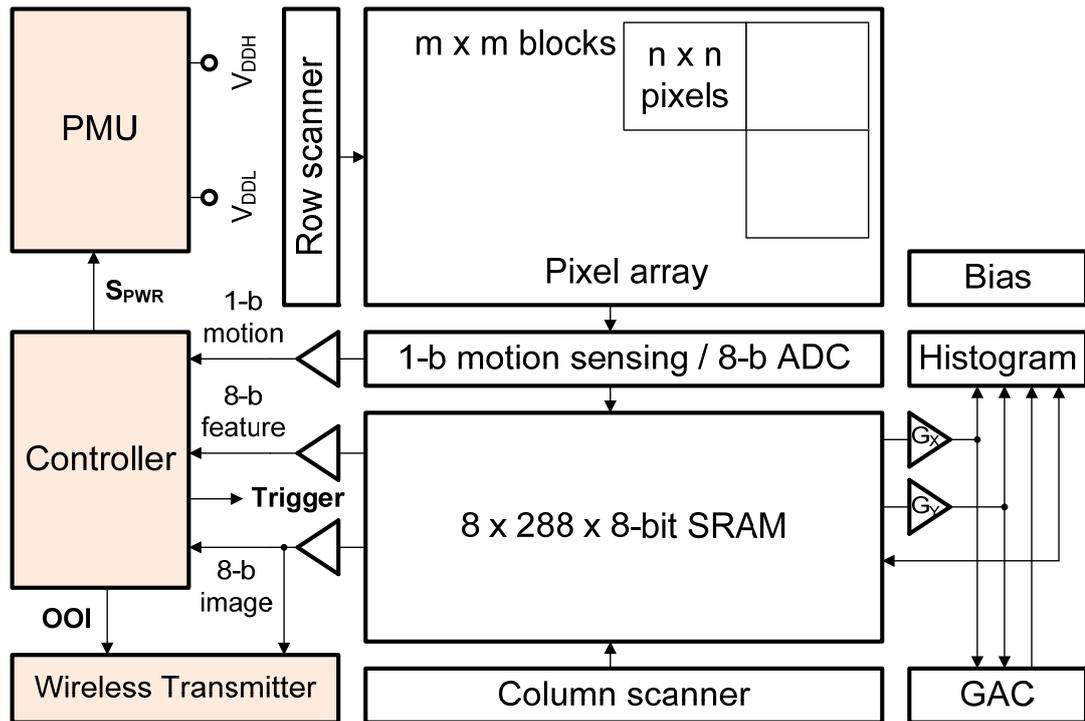

Figure 6.1 Overall architecture of adaptive imaging SoC

6.2.2 Integration in a sensor platform

After the design and the characterization of the adaptive imaging SoC, the final step would be the integration of the sensor platform including lens, solar cells and batteries. One of implementation is a three-dimensional cubic module that enhances the range of monitoring. Figure 6.3 shows one possible implementation of imaging-cubic (iCube) sensor platforms. The cubic sensor includes four adaptive imaging SoCs, two solar cell panels, and batteries in each plane. The lens is mounted on top of each imager. The foldable architecture using a flexible PCB enables 360° field of view. Therefore, we can

147

achieve high sensing visibility in multiple perspectives for effective surveillance. Moreover, the sensor platform can be implemented in small size less than $5 \times 5 \times 5$ mm^3 at low cost. The low-cost manufacturing enables multiple placements of sensors in a given area. From the imaging cube systems, we are able to collect more accurate data based on gross statistics for environmental monitoring, surveillance, and security applications.
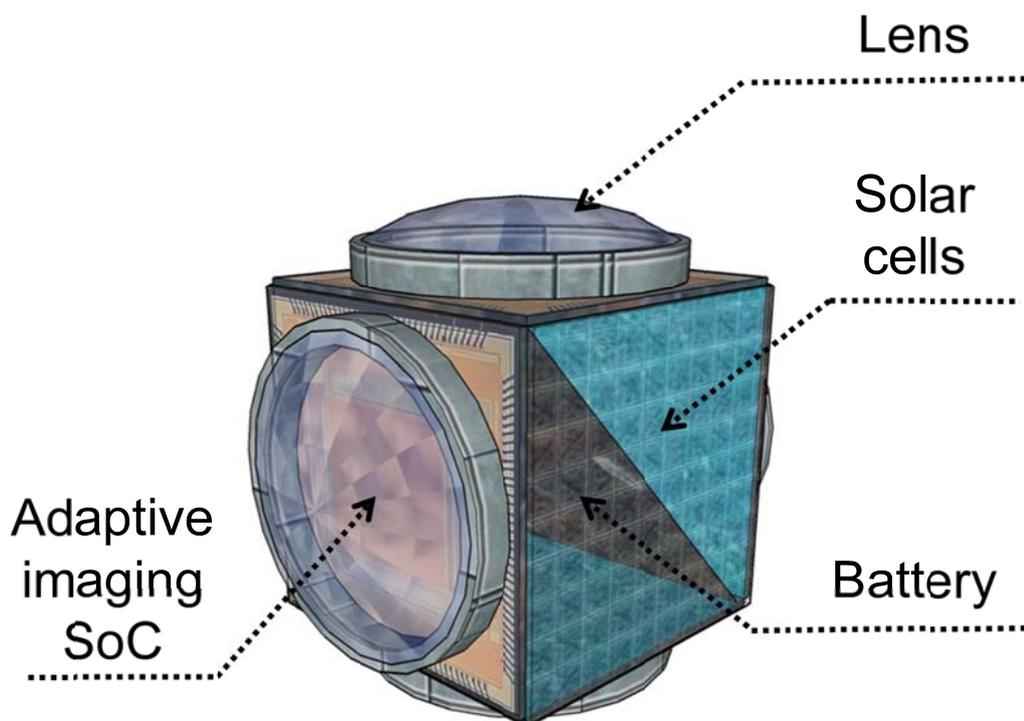
Figure 6.2 Illustration of imaging Cubic (iCube) sensor platform.

APPENDIX

Appendix A

Estimation of Power Consumption in CMOS Image Sensor

In this section, we describe detailed estimation of dynamic power consumption in digital circuit blocks. As mentioned in chapter 3, we consider the dynamic power consumption only from the capacitive driving ($C_L V_{DD}^2 f$) for simplicity. Moreover, the leakage power consumption will be ignored. This estimation cause error compared with actual dynamic power consumption. However, basic purpose of power estimation in this section is to get power reduction strategy by inspecting the tendency of power consumption according to important parameters such as the number of pixel array, power supply voltage and pixel pitch.

Column-parallel Single-slope ADC

A. Comparator: Dynamic Comparator

The dynamic comparator performs the level decision from the pre-amplified signals. It operates with two phases: the precharge and the comparison. Figure A.1 shows the comparator circuit.
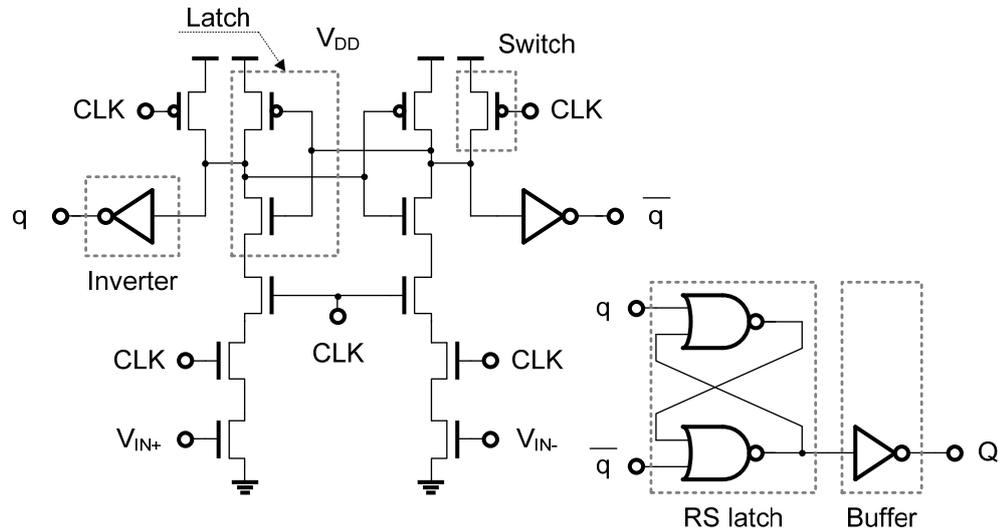

Figure A.1 Dynamic comparator

The first stage which consists of latch, switch (pMOS for precharge) and inverter induces the power consumption in each clock cycle. The frequency is $2^N/T_{ROW}$. The 2nd stage which consists of RS latch and buffer has only one time switching during the ADC. Therefore the frequency is $1/T_{ROW}$.

The power consumption per one comparator (per column) can be expressed as:

$$P_{COMP} = (P_{SW} + P_{LATCH} + P_{INV}) + (P_{SR} + P_{BUFFER})$$

$$== \frac{2^N}{T_{ROW}}\{2c_{inv}V_{DD}^2 + 2c_{inv}V_{DD}^2 + 2c_{inv}V_{DD}^2\} +$$

$$\frac{1}{T_{ROW}}\{2c_{inv}V_{DD}^2 + 10c_{inv}V_{DD}^2\} \tag{A.1}$$

$$= \frac{2^N}{T_{ROW}}(6c_{inv})V_{DD}^2 + \frac{1}{T_{ROW}}(12c_{inv})V_{DD}^2$$

,where P_{SW} is the power consumption from the precharge switches, P_{LATCH} is from the latch, P_{INV} is from the inverter, P_{SR} is from the RS latch, and P_{BUFFER} is from the buffer..

B. Latches

The latch for N-bit single-slope ADC consists of N D flip-flops. The circuit schematic of D flip-flop is shown in figure A.2. The output Q is connected with read buffer (one nMOS transistor, not shown in the figure) for the digital signal readout.

The power consumption of one latch in the single-slope ADC can be represented as follows:

$$\tag{A.2}$$

$$P_{D\_FF} = 2c_{inv}V_{DD}^2f_D + 3c_{inv}V_{DD}^2f_D \text{ : from 2 transmission gates \& 2 inverters, master}$$
$$+2c_{inv}V_{DD}^2f_{ck} + 4c_{inv}V_{DD}^2f_{ck} \text{ : from 2 transmission gates \& 2 inverters, slave}$$
$$+7c_{inv}V_{DD}^2f_{ck} + c_gV_{DD}^2f_{ck} \text{ : from clock buffer and output buffers}$$

152

$$= \left(13c_{inv} + c_g\right)V_{DD}^2 f_{ck} + 5c_{inv}V_{DD}^2 f_D$$

$$= \left(13c_{inv} + c_g\right)V_{DD}^2 \frac{1}{T_{ROW}} + 5c_{inv}V_{DD}^2 \frac{f_{CNT(n)}}{T_{ROW}}$$

$f_D = 1/T_{ROW}$, input (D) frequency, the input signal is the counter output.

$f_{ck} = f_{CNT(n)}/T_{ROW}$, clock (clk) frequency, the clock signal is the comparator output.

$f_{CNT(n)}$: counter output frequency of n-th bit position
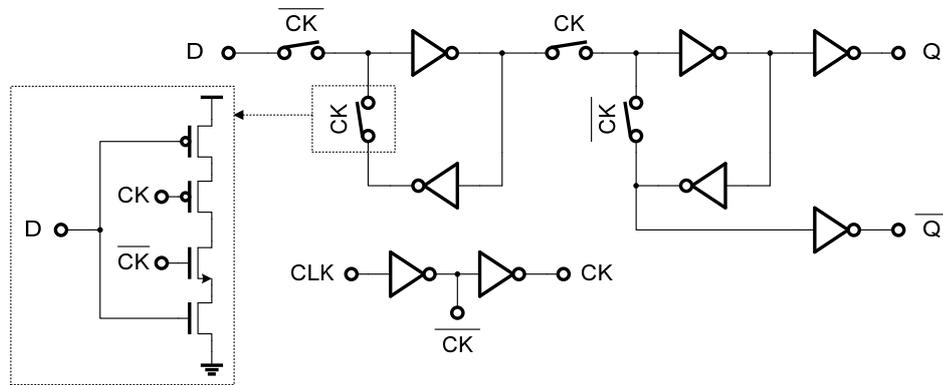
Figure A.2 D flip-flop

The total number of switching of N-b Gray code is $(1+1+2+\dots 2^{N-2})$. Therefore, the counter output frequency $f_{CNT(n)}$ is $(1+1+2+\dots 2^{N-2})/T_{ROW}$.

As shown in the equations, the power consumption of two inverters in the master stage is dependent on the input frequency. In the single-slope ADC, when clock signal is low, the master stage continuously changes its state from the counter signals. After clock goes high and the counter signal is latched to the slave stage, no more switching occurs. Therefore, the power consumption is largely dependent on the signal level (i.e., light intensity) of single slope ADC. In this estimation, we define the illumination level parameter 'I' which varies $1/2^N$ (dark) to 1 (bright). For the power consumption of N-bit latch in the single slope ADC which uses Gray counter can be expressed as follows:

153

$$P_{LATCH} = N\left\{(13c_{inv} + c_g)V_{DD}^2 \frac{1}{T_{ROW}}\right\}$$

$$+5c_{inv}V_{DD}^2 \frac{1}{T_{ROW}}I(1 + 1 + 2 + \cdots + 2^{N-2})$$

(A.3)

Note that the 2nd term includes the illumination level parameter 'I'. If the signal level is high from high illumination, the power consumption increases because the latch has more switching before the comparator output is toggled.

C. Counter

Figure A.3 shows the Gray-code counter circuit. The 1st stage is the ripple counter which generates the binary code. The Gray code from the XOR gates are buffered in the 2nd stage flip-flops in order to suppress the glitches.
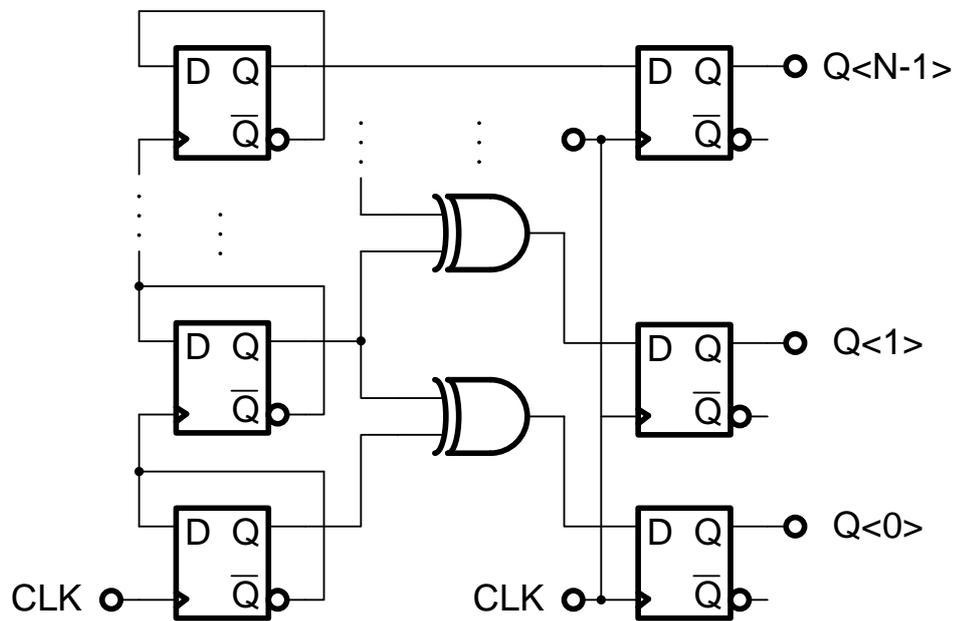

Figure A.3 Gray-code counter

The power consumption of the N-bit ripple counter can be expressed as:

(A.4)

$$P_1 = 2c_{inv}V_{DD}^2F + 3c_{inv}V_{DD}^2F \qquad \text{: from 2 transmission gates \& 2 inverters, master}$$
$$+2c_{inv}V_{DD}^2F + 4c_{inv}V_{DD}^2F \qquad \text{: from transmission gates \& 2 inverters, slave}$$
$$+7c_{inv}V_{DD}^2F + 4c_{inv}V_{DD}^2F \qquad \text{: from clock buffer and output buffers}$$
$$= 22c_{inv}V_{DD}^2F$$

$$F = \frac{1 + 2 + \cdots + 2^{N-1}}{T_{ROW}}$$

The exclusive-or (XOR) gate for the Gray code conversion consists of 3 gates. The power consumption of XOR gate is:

$$P_2 = 2c_{inv}V_{DD}^2F + c_{inv}V_{DD}^2F_{GRAY} \qquad (A.5)$$

The 2nd stage flip-flops for the glitch suppression has the power consumption as follows:

$$(A.6)$$

$$P_3 = 2c_{inv}V_{DD}^2F_{GRAY} + 3c_{inv}V_{DD}^2F_{GRAY} \text{ : from 2 transmission gates \& 2 inverters, master}$$
$$+2c_{inv}V_{DD}^2F_{GRAY} + 4c_{inv}V_{DD}^2F_{GRAY} \text{ : from transmission gates \& 2 inverters, slave}$$
$$+7c_{inv}V_{DD}^2F + 4c_{inv}V_{DD}^2F_{GRAY} \text{ : from clock buffer and output buffers}$$
$$= 15c_{inv}V_{DD}^2F_{GRAY} + 7c_{inv}V_{DD}^2F$$

$$F_{GRAY} = \frac{1 + 1 + \cdots + 2^{N-2}}{T_{ROW}} \approx \frac{F}{2}$$

The inverters drive the metal lines with high capacitance. The power consumption from the driver is as follows:

$$P_4 = \#_{COL}W_{PIX}c_mV_{DD}^2F_{GRAY} \qquad (A.7)$$

The overall power consumption from the counter can be expressed as:

$$P_{CNT} = P_1 + P_2 + P_3 + P_4$$

$$(A.8)$$

$$= (39c_{inv} + 0.5\#_{COL}W_{PIX}c_m) \times V_{DD}^2 \frac{1 + 2 + \cdots + 2^{N-1}}{T_{ROW}}$$

Periphery circuits

155

A. Column scanner

In this estimation, a simple shift register instead of decoder will be used. In each stage of shift register, the output buffer drives N nMOS transistor (for N-b digital signal readout, the column selection) in one column. The clock frequency f_{ck} is $\#_{COL}/T_{ROW}$, and the input frequency f_D is half of the clock frequency. The power consumption of one flip flop is shown as:

(A.9)

$$P_{D\_FF} = 2c_{inv}V_{DD}^2 f_D + 3c_{inv}V_{DD}^2 f_D \quad \text{: from 2 transmission gates \& 2 inverters, master}$$

$$+2c_l V_{DD}^2 f_D + 4c_{inv}V_{DD}^2 f_D \qquad \text{: from 2 transmission gates \& 2 inverters, slave}$$

$$+7c_{inv}V_{DD}^2 f_{ck} + Nc_g V_{DD}^2 f_D \qquad \text{: from clock buffer and output buffers}$$

$$= 7c_{inv}V_{DD}^2 f_{ck} + \left(11c_{inv} + Nc_g\right)V_{DD}^2 f_D$$

$$= 7c_{inv}V_{DD}^2 f_{ck} + \left(11c_{inv} + Nc_g\right)V_{DD}^2 \frac{f_{ck}}{2}$$

$$= \left(12.5c_{inv} + 0.5Nc_g\right)V_{DD}^2 \frac{\#_{COL}}{T_{ROW}}$$

The total power consumption from the column scanner is:

$$P_{CS} = \left(12.5c_{inv} + 0.5Nc_g\right)V_{DD}^2 \frac{\#_{COL}^2}{T_{ROW}} \qquad (A.10)$$

B. Row scanner

The row scanner consists of a shift register and drivers as shown in figure A.4. In each row, the row scanner consists of one flip flop, three NAND gates, three level-up converters and three inverters. In the shift register, the input frequency f_D is $1/T_{ROW}$ and the clock frequency fck is $\#_{ROW}/T_{ROW}$. The power consumption of one D flip-flop in the shift register can be expressed:

(A.11)

$$P_{D\_FF} = 2c_{inv}V_{DD}^2 f_D + 3c_{inv}V_{DD}^2 f_D \quad \text{: from 2 transmission gates \& 2 inverters, master}$$

$$+2c_{inv}V_{DD}^2 f_D + 4c_{inv}V_{DD}^2 f_D \quad \text{: from 2 transmission gates \& 2 inverters, slave}$$

156

$$+7c_{inv}V_{DD}^2 f_{clk} + 4c_{inv}V_{DD}^2 f_D \quad : \text{from clock buffer and output buffers}$$

$$= 7c_{inv}V_{DD}^2 \frac{\#_{ROW}}{T_{ROW}} + 15c_{inv}V_{DD}^2 \frac{1}{T_{ROW}}$$
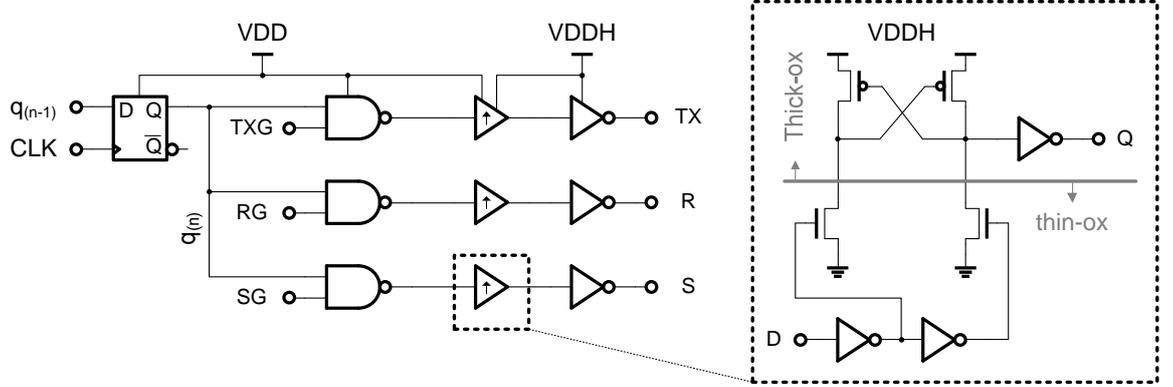
Figure A.4 Row scanner

The total power consumption of the $\#_{ROW}$-bit shift register is as follows:

$$P_{SHR} = 7c_{inv}V_{DD}^2 \frac{\#_{ROW}^2}{T_{ROW}} + 15c_{inv}V_{DD}^2 \frac{1}{T_{ROW}} \tag{A.12}$$

The NAND gate enables the pixel control signals (TX, R, S) according to the external control signals (TXG, RG, SG). The power consumption of three NAND gates in each row is as follows:

$$P_{NAND} = 3c_{inv}V_{DD}^2 \frac{1}{T_{ROW}} \tag{A.13}$$

Since the pixel power supply is higher than digital power supply (V_{DD}), level-up converter is required to control the pixel circuit. In one level-up converter,

$$\tag{A.14}$$

$$P_1 = 2c_{inv}V_{DD}^2 \frac{1}{T_{ROW}} \quad (1^{st} \text{ stage})$$

$$P_2 = 2c_{inv}V_{DDH}^2 \frac{1}{T_{ROW}} \quad (2^{nd} \text{ stage})$$

$$P_3 = 4c_{inv}V_{DDH}^2 \frac{1}{T_{ROW}} + \#_{COL}(W_{PIX}c_m + c_g)V_{DDH}^2 \frac{1}{T_{ROW}} \qquad \text{(driver)}$$

$$P_{conv} = P_1 + P_2 + P_3$$

The power consumption from level-up converters from all rows can be expressed:

$$P_{LU} = 3P_{conv} = 2c_{inv}V_{DD}^2 \frac{1}{T_{ROW}}$$

$$+\{6c_{inv} + \#_{COL}(W_{PIX}c_m + c_g)\}V_{DDH}^2 \frac{1}{T_{ROW}} \qquad \text{(A.15)}$$

The total power consumption from the row scanner is:

$$P_{RS} = P_{SHR} + P_{NAND} + P_{LU}$$

$$= \{7c_{inv}\#_{ROW}^2 + 20c_{inv}\}V_{DD}^2 \frac{1}{T_{ROW}} \qquad \text{(A.16)}$$

$$+\{6c_{inv} + \#_{COL}(W_{PIX}c_m + c_g)\}V_{DDH}^2 \frac{1}{T_{ROW}}$$