Graphene Nanoelectronics - From Synthesis to Device Applications

by

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To my loved ones

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ABSTRACT

Nanotechnology is the pinnacle of the scientific effort to breach the dimensional limit in matter. Every now and then, this technology offers us a rare glimpse into the true potential of a common material. Graphite, a material found in pencils, has been used by humans since the 4th millennium BC. When atomic particles in graphite are confined in the two-dimensional nanoscale limit, these quasiparticles enter an exclusive domain of relativistic electron theory of the Dirac equation. This single atomic sheet of carbon atoms that provides the confinement is called *graphene*. In this thesis, we present research efforts to harness the extraordinary attributes of graphene and explore new possibilities in the field of nanoelectronics.

First, the importance of bilayer graphene and its tunable bandgap is discussed. For the first time, a rational route to synthesize wafer scale bilayer graphene is investigated using a low-pressure chemical vapor deposition (LPCVD) method. Subsequently, the existence of tunable bandgap devices are confirmed with cryogenic carrier transport measurements from dual-gate bilayer graphene transistors. We further explore the feasibility of a bilayer graphene-based, flexible, transparent conductor, and confirm the efficiency and the exceptional mechanical robustness of the material. The sheet resistance change of the graphene film at 2.14% strain is less than 15%, a 20-fold improvement over commercial indium oxide films.

Next, we report flexible and transparent all-graphene circuits for binary and quaternary digital modulations for the first time. Importantly, the entire modulator circuits are fabricated with graphene only, and this monolithic structure allows unprecedented mechanical flexibility and near-complete transparency. By exploiting the ambipolarity and the nonlinearity in graphene transistors, we achieved quadrature phase shift keying (QPSK) using just two graphene transistors, representing a drastic reduction in circuit complexity when compared with conventional silicon-based modulators.

Lastly, we address the shortcomings of small gain in conventional graphene transistors by designing the very first graphene heterostructure bipolar junction transistor. The exploitation of graphene's low density of states and tunable Fermi level leads to graphene-semiconductor junctions with higher emitter injection efficiency compared to that of a conventional Schottky junction. This property is utilized for the invention of a graphene-based bipolar junction transistor with high on/off ratio($>10^5$) and current gain (>33).

Chapter I

Introduction

1.1 Foreword

Carbon is one of the most distinctive elements in the periodic table. Carbon bonds allow an almost infinite number of carbon derivatives with other elements, forming the basis of all known organic materials. Furthermore, carbon atoms can also form very stable bonds with themselves. Carbon-carbon single bonds, double bonds, and triple bonds allow the formation of 3-D, 2-D, 1-D, and even 0-D structures. The versatility and the potential of this element has led to many theoretical and experimental studies on carbon-based nanomaterials such as zero-dimensional fullerenes and one-dimensional carbon nanotubes. The existence of a two-dimensional carbon nanosystem was not considered possible because of its inherent thermodynamic instability; as the lateral size of a two-dimensional system grows, the phonon density integrated over the 3D space available for thermal vibration diverges rapidly [1, 5]. However, in 2004, when a monolayer of graphite was exfoliated from bulk graphite, scientists were able to observe a stand-alone two-dimensional carbon nanosystem [1, 6, 7]. This was possible by removing the bulk graphite at a sufficiently low temperature such that the thermal fluctuations were unable to break the atomic bonds [5]. This single sheet of carbon that has been exfoliated from bulk graphite was named "graphene." It is an atomic thick layer

of carbon atoms tightly packed into a honeycomb crystal lattice as shown in Figure 1.1. The carbon atoms (black dots) are all sp^2 hybridized (i.e. one 2s orbital hybridizes with 2px and 2py orbitals to generate three sp^2 orbitals). There is one electron per carbon atom left in the 2pz orbital, and the 2pz orbitals form π-bonds with the neighboring 2pz orbitals. The two-dimensional graphene formed by these bonds is actually the building block of all other carbon-based nanomaterials as shown in Figure 1.2.

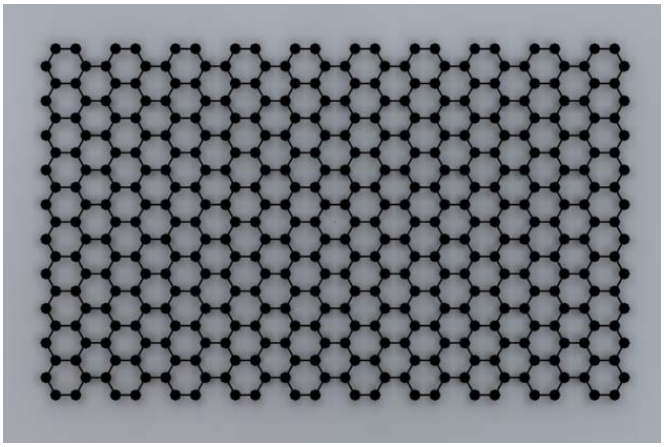

Figure 1.1 The graphene crystal lattice.

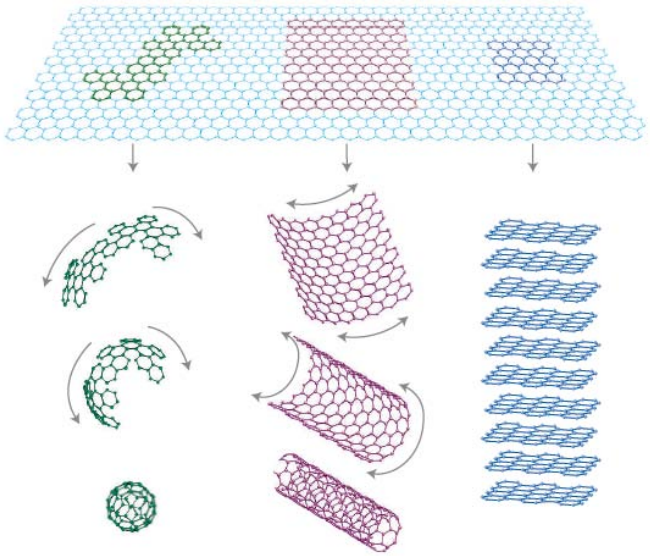

Figure 1.2 Graphene is the two dimensional building block for carbon based nanomaterials of all other dimensionalities. It can be wrapped up into 0-D fullerenes, rolled into 1-D carbon nanotubes or stacked into 3-D graphite. (adopted from [1])

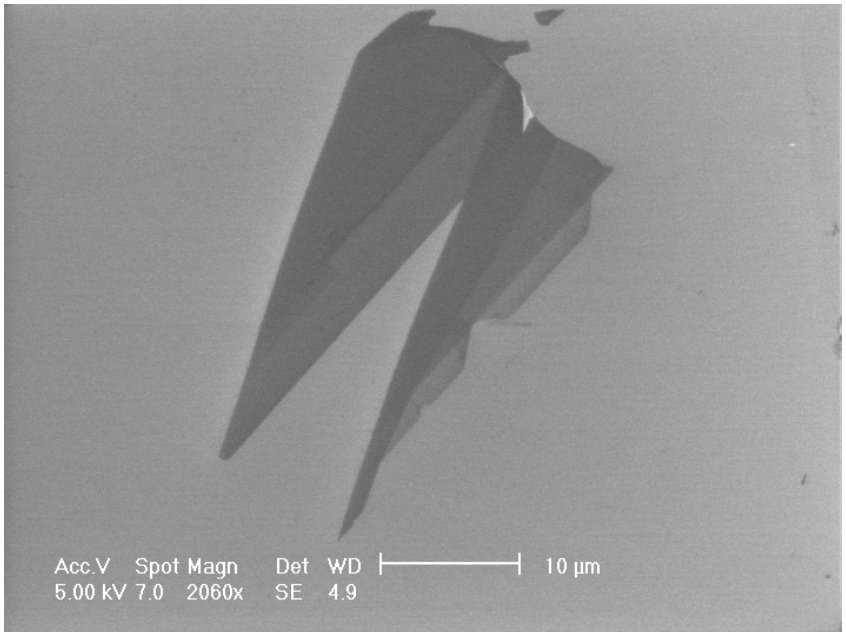

Figure 1.3 A scanning electron microscopy image of mechanically exfoliated graphene and graphite. Graphene is shown as the region with the lightest color at the right edge of the sample. The rest of the darker colored areas of the sample are either few layer graphenes or thicker graphite.

This two-dimensional allotrope of carbon has emerged as a promising material for novel applications in electronics due to its remarkable physical and electronic properties. It is the thinnest known material but also the strongest ever measured in terms of mechanical stiffness[5]. The charge carriers exhibit extremely high carrier mobility with zero effective mass[6]. It can also sustain current density six orders of magnitude higher than that of copper and shows record thermal conductivity[5]. These astonishing properties can only be understood by studying the unique band structure and morphology of graphene, which will be explained in this chapter.

1.2 The electronic properties of graphene

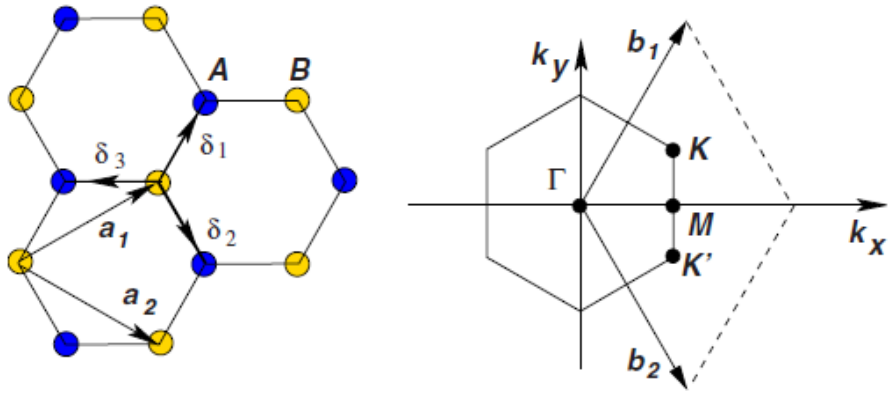

Figure 1.4 Hexagonal crystal lattice of graphene (left) and its Brillouin zone (right). $\mathbf{a_1}$ and $\mathbf{a_2}$ are the lattice unit vectors, and δ_i, i=1,2,3 are the nearest-neighbor vectors. In its corresponding Brillouin zone, the Dirac cones are located at the K and K′ points. (adopted from [6])

Graphene atoms are arranged in a hexagonal crystal lattice as shown in Figure 1.4 (left). The structure can be understood as a triangular lattice with a basis of two atoms per unit cell (depicted as blue and yellow in Figure 1.4). The interatomic distance of two carbon atoms is ~1.42 Å [6].

The band structure of graphene follows simple nearest neighbor tight binding approximation [8]. Since graphene has two atoms per unit cell, the points of particular importance are K and K' points at the corners of the graphene Brillouin zone also known as the Dirac points (Figure 1.4 right). Near these points, the energy bands derived from the tight binding Hamiltonian shows linearly dependence of electron energy to the wave vector[9] as shown in the zoom-in of the Figure 1.5. The crystal structure of graphene with two sublattices allows quantum mechanical hopping between the sublattices leading to the formation of two energy bands[10], and their intersection near the edge of the

Brillouine zone results in conical energy dispersions. The bandgap of a graphene is exactly zero, with conduction band and valence band meeting at the K and K' points also known a Dirac point or a charge neutrality point.

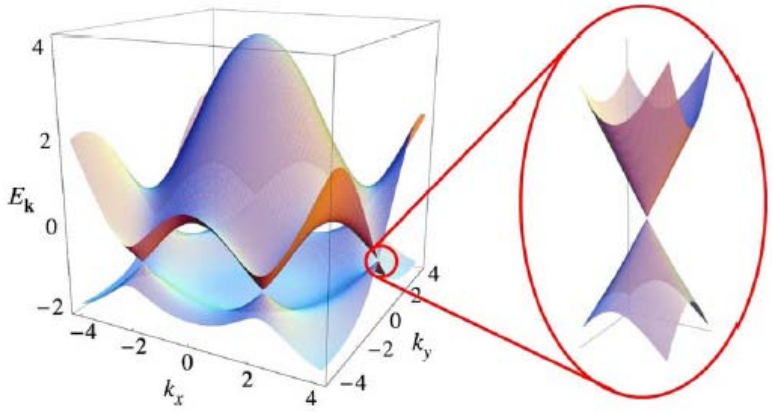

Figure 1.5 The energy dispersions of graphene crystal lattice. The conductance band touches the valence band at the K and the K' points (i.e. the Dirac points). (adopted from [6])

The most interesting aspect of graphene energy spectrum is that its charge carriers can be described by a Dirac spectrum for massless fermions[11, 12] rather than the usual Schrödinger equation for nonrelativistic particles.[1, 5, 6, 10, 13]. The Dirac spectrum is governed by the Dirac equation, which describes relativistic quantum particles with spin 1/2, such as the electrons. The important feature of the Dirac equation is the existence of antiparticles such as positrons[14]. Positrons are antiparticle counterpart of electrons with electric charge of +1e, spin of 1/2, and the same mass as the electrons. The fundamental property of the Dirac equations is often referred to as the charge-conjugation symmetry[14]. This term is used to describe how states at the negative energy (electrons) and the positive energy (positrons) are conjugated, being described by different components of the same spinor wave function[14].

For Dirac particles with a mass m, there is a gap between the minimum electron energy, $E_o=mc^2$ and the maximum positron energy $-E_o$. In this case, the energy is linearly dependent on the k wave vector only when the energy value is much larger than E_o. However, for massless Dirac fermions, the gap is zero and the energy is linearly dependent on k at any energy. The particles in graphene are neither massless nor relativistic. However, as explained earlier from the tight binding approximation, the quasiparticles in the graphene structure exhibit a linear dispersion relations following the equation $E=\hbar k v_F$, as if they were massless relativistic particles (such as photons) governed by the Dirac equation[1, 5, 6, 10, 15]. (Here, the role of the speed of light c is replaced by fermi velocity $v_F \approx c/300$.) This means that electrons in graphene all move at a constant speed ($\sim v_F$) regardless of their momentum. Because of this linear dispersion, the quasiparticles in graphene behave very differently from other semiconductor or metal with energy spectrum approximated by parabolic (i.e. free electron like) dispersion relations.

For example, although the bandgap is zero, the gate voltage can still modulate the density of states in graphene[15] and switch from low conductivity states near the Dirac point to high conductivity states elsewhere. However, because there is no bandgap, there is still a finite amount of current even at the low conductivity state near the Dirac point[6, 15] leading to high switch-off current in graphene based transistors. The minimum conductivity is also affected by defect, impurities and the substrate[15, 16].

The graphene crystal also shows exceptional electronic quality such that charge carriers can travel ballistically over submicron distance [1, 7, 17, 18]. Mobility values that are extremely high (~20,000 cm^2/Vs) were reported for single-layer graphene in

several literatures. [16, 17, 19]. The mobility in these samples is limited by scattering on charged impurities [20, 21] or microscopic ripples [22, 23][3,7]. However, both source of scattering can be reduced significantly by careful sample preparation and they are not the ultimate limiting factors of carrier mobility in graphene structure[17]. It is the intrinsic scatterers such as phonons that cannot be removed at room temperature that sets the fundamental limit of mobility in graphene [16, 17, 19]. This electron-phonon scattering in graphene was found to be a very weak contribution factor to its overall resistivity [24]. For example, Chen et. al.[24] have experimentally proven that the electron-acoustic phonon scattering contributes very little (~30Ω) to graphene's room temperature resistivity. At technologically relevant carrier density of 1×10^{12} cm^{-2}, they have experimentally shown that a mean free path of >2μm and an intrinsic mobility value of 200,000 cm^2/Vs can be reached[24].

Graphene's carrier transfer characteristics also stands out as it shows perfect ambipolar electric field effect so that its charge carrier can be tuned continuously as shown in Figure 1.6 [1]. Its low-energy spectrum is shown as insets in Figure 1.6 indicating the changes in the position of the Fermi energy E_F with respect to the changing gate voltage V_g. Positive gate voltage induce electrons while negative voltage induce holes. The concentration of electrons and holes can be as high as $10^{13}cm^{-2}$ [1].

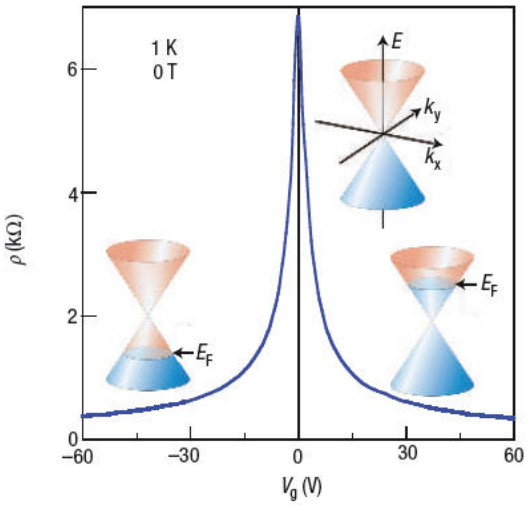

Figure 1.6 Ambipolar electric field effect in single-layer graphene. The insets show its low-energy spectrum, indicating changes in the position of the Fermi energy E_F with varying gate voltage V_g. (adapted from [1])

1.3 Graphene applications in electronics

During the last century, silicon-based electronics have contributed immensely to changing our world. New technologies such as portable handheld devices, biomedical apparatus, next-generation displays, and ubiquitous sensor systems were introduced as the technology matured. The industry has maintained the pace of silicon technology by following Moore's law which states that the number of transistors on a chip will double approximately every two years. However as the transistors made of silicon are scaled down, the material's limitations are becoming more apparent. International Technology Roadmap for Semiconductors (ITRS) now considers graphene to be among the candidate materials for post-silicon electronics. In this context, graphene has been proposed as an emerging material to replace silicon in high speed electronics. For example, a graphene transistor with a cutoff frequency as high as 300 GHz has been demonstrated [25]. This

achievement, which exceeds that of silicon transistor, is quite remarkable considering the fact that graphene was found only a few years ago. However, in the field of digital electronics, there is a general consensus that graphene-based transistors will not be able to replace silicon transistors in the near future[5, 26]. There are several reasons for this predicament. First, the fabrication of the integrated circuits is highly complicated, and the semiconductor fabrication plants are extremely expensive to modify. Second, scaling and other design modifications, such as three-dimensional gate structure, have provided the needed performance improvements in the past, and there has been little motivation for the manufacturers to introduce devices based on any material other than silicon. Third, and most importantly, the lack of a bandgap and a complementary structure such as CMOS in graphene transistor technology prevents sufficient turning off of the logic circuit, resulting in significant leakage current and static power dissipation. On the other hand, CMOS logic gates consist of both n- and p-type metal–oxide–semiconductor field-effect transistors (MOSFETs) that can switch between the on-state and the off-state. In the steady state, certain MOSFETs are always switched off so that no current (except a small leakage current) flows through the power source and the ground. The ability of silicon MOSFETs to switch off enables extremely low static power dissipation in CMOS logic. In a conventional FET, this requires semiconducting channels with a sizeable bandgap of at least 0.4eV [26]. It is very challenging to achieve a bandgap this large in graphene transistors, and the resulting on/off ratio of a typical graphene transistor is very low (~100) [27]. Despite graphene transistors' low on/off ratio, which limits their usage in the digital/logic applications, they are in many ways attractive in the analog/radio frequency applications. In analog circuit applications, switching off is not the major limiting

factor[26]. In a small-signal amplifier, for example, the transistor is operated in the on-state and a small AC signal that needs to be amplified is superimposed onto a DC gate source bias. Also, the scaling theory predicts that field-effect transistors with a thin gate oxide and a vertically thin gate-controlled region will be robust against short-channel effects even when the gate length is very short [26]. The possibility of having channel that is just a single atomic layer thick is one of the most attractive features of graphene transistors as its extremely thin structure allows shorter scaling of channel length without the adverse short-channel effects [26]. In addition, the ambipolar carrier transport behavior of graphene transistors can be utilized to simplify circuits[28] that otherwise use a complementary structure (e.g. CMOS) having both NFETs and PFETs in a circuit. This is possible because ambipolar graphene transistor exhibits both the property of an NFET and a PFET depending on its gate bias. Adding to the fact that graphene exhibits a naturally high mobility, several pioneering works on graphene analog electronics led to the demonstration of graphene-based frequency doublers[29, 30], amplifiers[28, 31, 32], mixers[33, 34], and modulators[28, 35, 36]. Graphene analog electronics is an active field of research and further development is expected in the future[26].

Another area of interest for graphene application is flexible electronics. Although graphene is the strongest and the stiffest material yet discovered in terms of tensile strength and elastic modulus respectively, it is also extremely flexible [37]. The strength and flexibility results from its covalent sp^2 bonds[37]. Because of its mechanical strength combined with its unique electrical properties, graphene can be used as both the channel and electrode material for flexible electronic devices[38-41]. New applications in the

areas of flexible displays[42], wearable electronics[43] and biomedical skin-like devices[44, 45] are some examples of how graphene can be utilized.

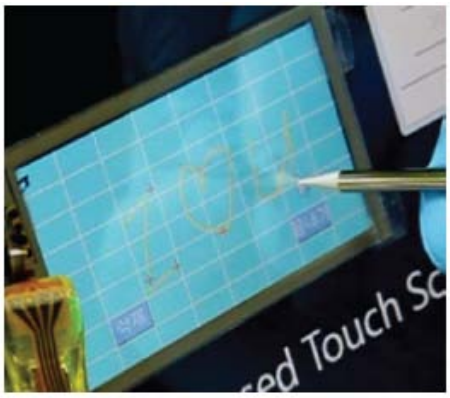

Figure 1.7 A graphene based touch screen demonstrated in ref [4].

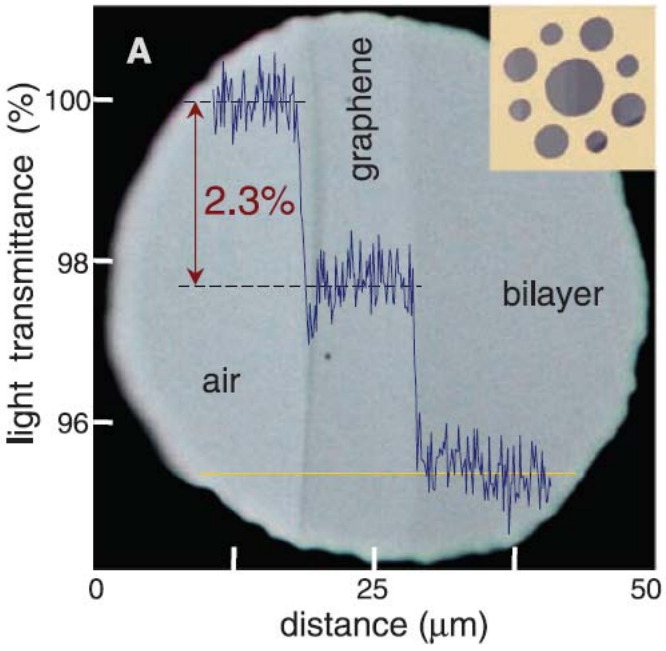

Figure 1.8 Photograph of a 50 μm aperture partially covered by graphene and its bilayer. The line scan profile shows the intensity of transmitted white light along the yellow line. The inset is the support structure with 20, 30, and 50 μm in diameter with graphene placed over them. (adopted from [3])

Graphene also shows interesting optical properties. For example, it can be optically visualized, despite being only a single atom thick. As shown in Figure 1.8, graphene absorbs significant amount of light per layer (2.3% per layer at wavelength of 550nm, [3]) but because it is only one atomic layer thick, the transmittance is about 97.7% and it is highly transparent. Graphene is not only transparent but also quite conductive due to its semi-metallic property. The sheet resistance of a pristine layer is about 2 kΩ to 6 kΩ[46] and the value can be as low as 125Ω depending on the chemical doping method[4]. The sheet resistance value can lowered even more by either stacking several graphene layers[4, 47-49] or fabricating a hybrid nanowire/nanomesh structure[50] with graphene. Several research groups have demonstrated graphene layers as transparent conductive material that can compete with some of the oxide based transparent conductive material (e.g. indium tin oxide or ITO) that dominates the current market. The main advantage of graphene based transparent conductor compared to oxide based material is its mechanical flexibility. Oxide materials, in general, are very brittle and therefore are not suitable for flexible electronics application[51-53]. The usage of graphene transparent conductor will opened up some new possibilities and applications such as flexible solar cells[54], transparent & flexible displays and electronics[4], bendable touch screens[4] and some biomedical applications that requires stretchability and transparency[44].

1.4 Graphene synthesis

Graphene was first introduced by micromechanical exfoliation of graphite[7]. This method involves peeling off a piece of graphite by using an adhesive tape. Although

this process can be optimized to produce high quality sample up to few hundred micrometers in size, it is impractical for large-scale applications. Hence, a large-scale synthesis method is in need of development. Several approaches have been explored to provide graphene in a more practical manner for industry applications. These methods include segregation of carbon containing substrates by heat treatment[55, 56], reduction of graphene oxide [38], liquid phase exfoliation[57, 58], longitudinal splitting of carbon nanotubes[59], and chemical vapor deposition (CVD)[4, 48, 60, 61].

Carbon segregation method was demonstrated using silicon carbide (SiC)[55] after high-temperature annealing as shown in Figure 1.9. High quality graphene layers can now be produced on SiC in an argon atmosphere [55]. However, the silicon carbide substrate is very expensive and there is a limitation on how much this method can be compatible with other substrates such as silicon wafer.

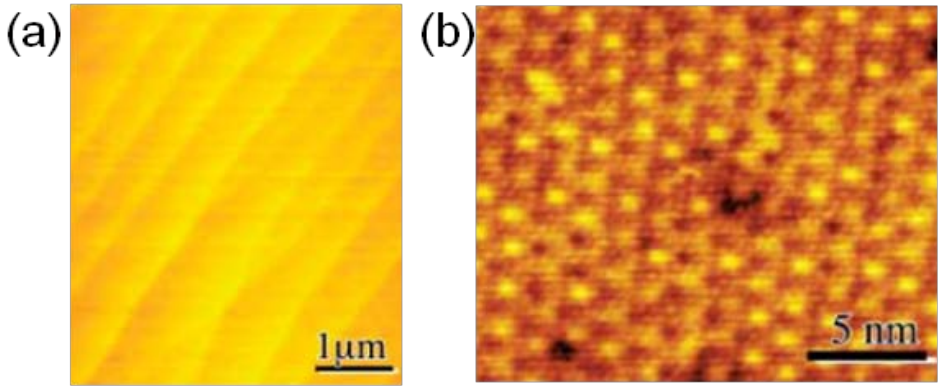

Figure 1.9 Epitaxial graphene grown on SiC wafer. (a) AFM image of graphitized SiC. Graphite is continuous over the steps. (b) STM image of one monolayer of epitaxial graphene on SiC. (adopted from [55]

It is also possible to use graphene oxide aqueous suspension to obtain a graphene sheet using vacuum filtration method [38]. After filtration, the graphene oxide flakes on the filter membrane (Figure 1.10 (a)) is transferred by placing the membrane with the film side down onto a substrate and dissolving the membrane with acetone. The reduction

of the graphene oxide films is achieved through a combination of hydrazine vapor exposure and low-temperature annealing treatment [38]. The microscopic image of reduced graphene oxide is shown in Figure 1.10 (b).

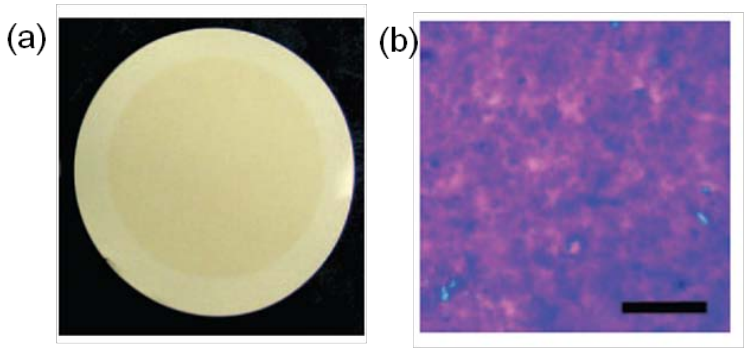

Figure 1.10 Thin films of solution-processed graphene oxide. (a) Photographs of graphene oxide thin films on filtration membrane. (b) Films showing the different densities of the overlapped regions (darker colors) between the graphene sheets. Scale bar is 20 μm. (adopted from [38])

Another solution based method to obtain a graphene sheet is liquid-phase exfoliation[57, 58]. This method consists of chemical wet dispersion of graphite followed by ultrasonication in aqueous solvents. Up to 70% single layer graphene sheet can be achieved by sonication followed by sedimentation based ultracentrifugation [57]. Figure 1.11 (b) shows the scanning electron microscopy (SEM) image of the dispersion of graphene after ultrasonication. Figure 1.11 (c) is the transmission electron microscopy (TEM) images of a folded graphene sheet on a TEM grid. Exfoliation of graphite-intercalated compounds[62] and expandable graphite[63] is also possible.

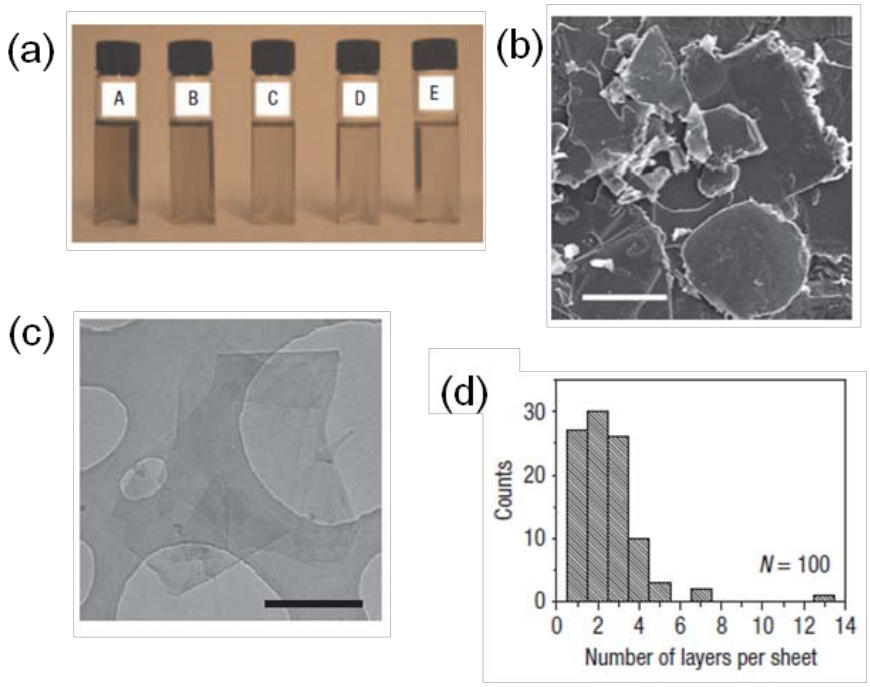

Figure 1.11 Optical characterization and Electron microscopy of graphite dispersions. (a) Dispersions of graphite flakes in N-methylpyrrolidone (NMP), at a range of concentrations ranging from 6 μg/ml to 4 μg/ml. (b) SEM image of sediment after centrifugation. Scale bar is 25 μm. (c) Bright-field TEM images of a folded graphene sheet and multilayer graphene, both deposited from NMP. Scale bar is 500 nm. (d) Histogram of the number of flakes as a function of the number of monolayers per sheet**.** (adopted from [57])

However, all the solution based methods introduced previously suffer from defects and interflake junctions, and generally have much lower carrier mobility and sheet conductance compared to mechanically exfoliated sample or CVD grown samples [52]. The interflake junctions can be observed from Figure 1.10 (b) and Figure 1.11 (b). The non-uniformity of graphene flakes for liquid phase exfoliation is also shown as a histogram in Figure 1.11 (d).

One way to make a high quality graphene nanoribbon was demonstrated by using carbon nanotubes [59]. Since carbon nanotubes are actually rolled up graphene (i.e. graphene in a tube shape), a high quality graphene can be derived from pristine carbon

nanotubes. This was possible by longitudinal unzipping or splitting of the wall of carbon nanotubes by means of solution based oxidative process (Figure 1.12 (a), (b))[59]. Unlike previously introduced solution based methods, this method yielded high quality individual graphene nanoribbons with bandgap suitable for high performance devices[59]. These ribbons were particularly noteworthy for their smooth side edge profile which may eliminate some of the edge effect that causes adverse effect on graphene nanoribbon devices[64]. However, this method is also prone to the difficulties that many researchers face with carbon nanotubes: it is difficult to control the location of these nanoribbons for scalable electronics[59].

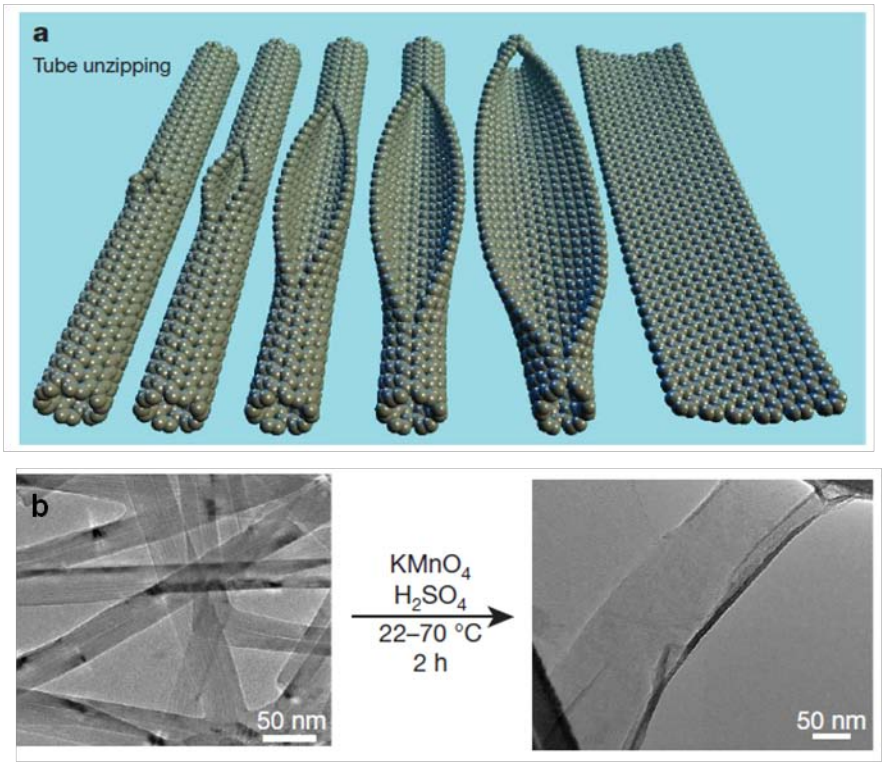

Figure 1.12 Nanoribbon formation and imaging (a) Representation of the gradual unzipping of one wall of a carbon nanotube to form a nanoribbon. (b) TEM images depicting the transformation of multi-walled carbon nanotubes (left) into oxidized nanoribbons (right). The right-hand side of the ribbon is partly folded onto itself. The dark structures are part of the carbon imaging grid. (adopted from [59])

One of the most promising and inexpensive way to synthesize reasonably high quality graphene is chemical vapor deposition method on transition metals such as Ni[65, 66] or Cu.[2, 4]. The formation of graphene is the consequence of diffusion and segregation of carbon impurities from the bulk to the surface during the annealing and cooling stages.

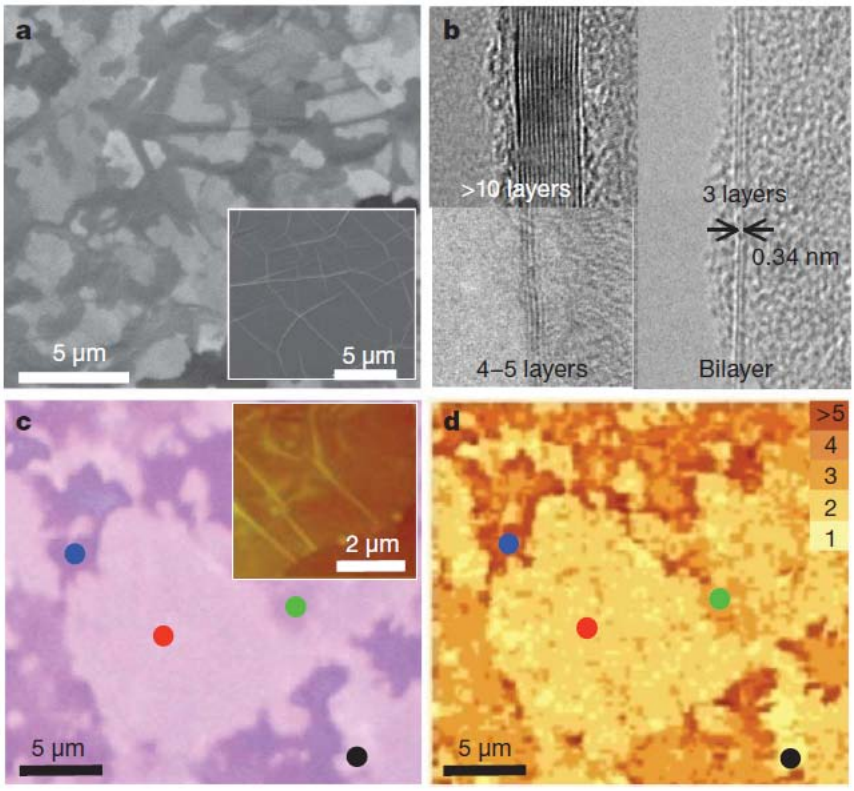

Figure 1.13 Various spectroscopic analyses of the large-scale graphene films grown on nickel foils by CVD. (a) SEM images of as-grown graphene films on thin (300 nm) nickel layers and thick (1 mm) Ni foils (inset). (b) TEM images of graphene films of different thicknesses. (c) An optical microscope image of the graphene film transferred to a 300 nm thick silicon dioxide layer. The inset AFM image shows typical rippled structures. (d) A confocal scanning Raman image corresponding to image in (c). The number of layers is differentiated by the color contrast. (adopted from [66])

Nickel has a relatively higher adsorption rate of carbon compared copper and this resulted in multilayer graphene film as shown in Figure 1.13. On the other hand, uniform single layer graphene was grown on copper foils over large area due to copper's lower adsorption rate of carbon. The introduction of copper foil (Figure 1.14) as the graphene growth substrate allowed access to high quality material that has a mobility up to 7000 $cm^2V^{-1}s^{-1}$.[2]. Also graphene area as large as 30 inch in diameter [4] was achieved as shown in Figure 1.15.

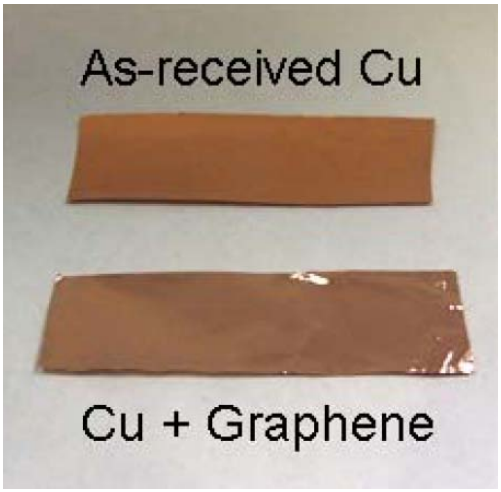

Figure 1.14 Photos of as-received Cu foil without graphene and Cu foil covered with graphene. (adopted from [2])

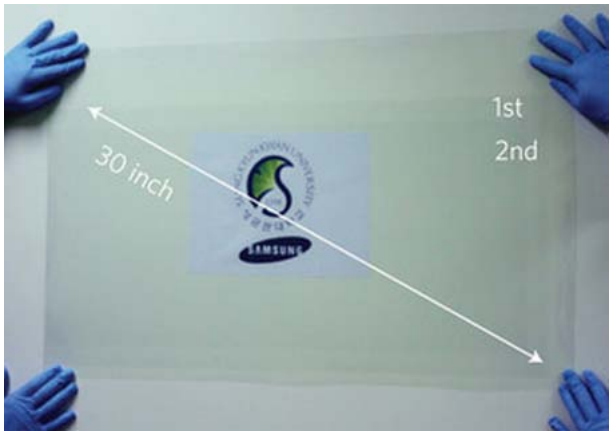

Figure 1.15 A transparent ultralarge-area graphene film transferred on a 35-inch PET sheet. (adopted from [4])

This method involves thermal decomposition of hydrocarbons (in a form of methane gas) on the surface of transition metal and then carbon was segregated from the surface upon cool down. The temperature for thermal decomposition would reach 1000 °C. After cool down, a polymer such as Poly(methyl methacrylate) (PMMA) or Polydimethylsiloxane (PDMS) would be coated on top of the graphene coated copper foil. After coating, the other side of copper would be exposed to oxygen plasma to remove the backside graphene. The copper underneath would then be etched away in aqueous solution such as ferric nitrate or ammonium persulfate that is used as a copper etchant. This etching process would typically take 4 to 24 hours depending on the copper thickness. After the copper is etched away, the remaining pmma-graphene structure can be transferred to an arbitrary substrate. After some drying period, the pmma will be removed by acetone to expose the graphene for further process. An illustration of the graphene transfer process is shown in Figure 1.16. The capability to transfer high quality graphene to an arbitrary substrate is a strong advantages of the CVD based graphene synthesis method. Large area graphene in wafer scale can be readily obtained and the size is only limited by the synthesis apparatus.

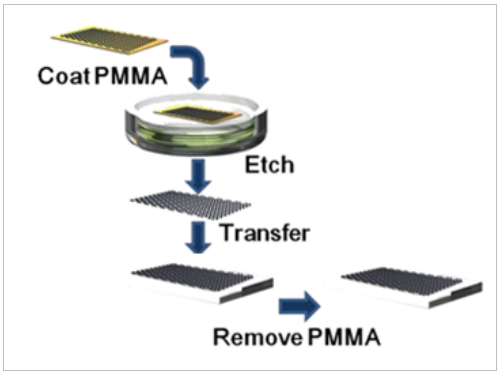

Figure 1.16 An illustration of graphene transfer process. Graphene on top of the copper foil is coated with PMMA and the backside copper is etched using wet etchant. The

graphene is transferred to an arbitrary substrate and the top PMMA is removed with acetone.

All of the graphene material used in this work was synthesized by CVD method using a copper foil (25 μm thick) as the substrate. The details of the CVD process will be discussed in the next chapter. A commercial CVD furnace with the capability to flow required gases (e.g. methane, hydrogen, and argon) at controlled temperature and vacuum level was used in this work (Figure 1.17).

Figure 1.17 The CVD furnace model used in this work. The quartz tube inside the furnace is 3 inches in diameter.

1.5 Verification of graphene layer number

It is important to verify the number of graphene layer in a sample because graphene and graphite (or multilayer graphene) exhibits very different electronic behavior [6]. There are several techniques to verify the number of graphene layers. Raman spectroscopy and transmission electron microscopy are two well known optical characterization methods to confirm the number of graphene layers. It may be more difficult to verify the number of layers with atomic force microscopy or optical microscopy, mainly due to graphene's extremely thin structure and high transmittance.

Raman spectroscopy is a spectroscopy method to study the vibrational, rotational low frequency mode of a system. It relies on Raman (inelastic) scattering of laser light to observe how light interacts with molecular vibrations and phonons. It is important to understand the phonon dispersion of graphene to interpret the Raman spectra of graphene. Since the unit cell of monolayer graphene contains two carbon atoms, A and B, there are six phonon dispersion bands as shown in Figure 1.18. Out of three acoustic (A) and three optical (O) phonons, the atomic vibrations are perpendicular to the graphene plane for one acoustic branch and one optic phonon branch, corresponding to the out-of-plane (o) phonon modes. For other two acoustic and two optic phonons, the vibrations are in-plane (i). The longitudinal (L) or transverse (T) direction is defined according to vibrations parallel with or perpendicular to the A–B carbon–carbon directions, respectively. The in-plane iTO and LO optic modes are degenerate near the zone center (Γ point) [67, 68].

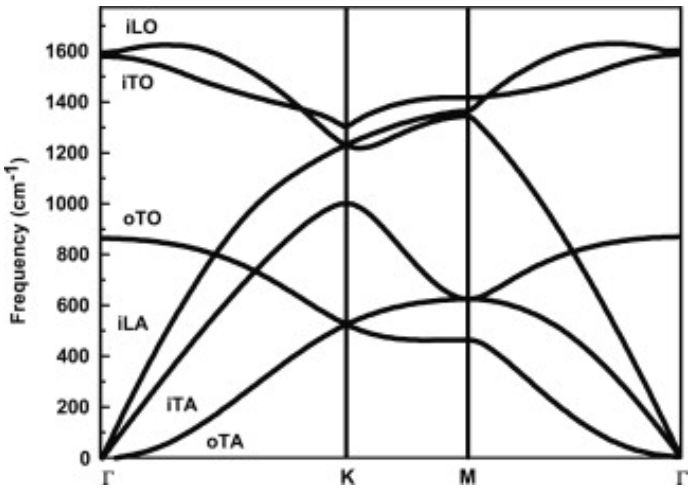

Figure 1.18 Calculated phonon dispersion relation of graphene showing the iLO, iTO, oTO, iLA, iTA and oTA phonon branches. (Adapted from [69])

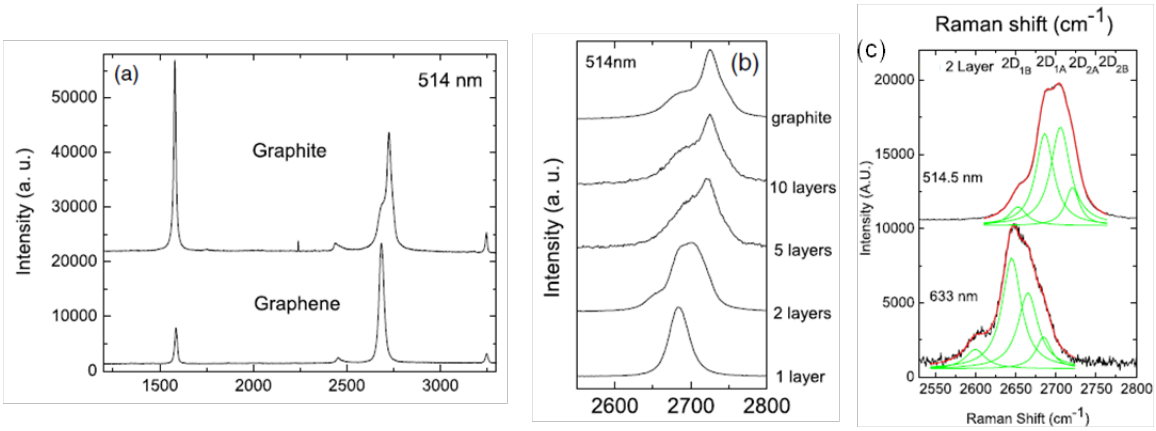

Figure 1.19 Raman spectra of graphene with different thickness (a) Comparison of Raman spectra at 514 nm for bulk graphite and graphene. They are scaled to have similar height of the 2D peak at ~2700 cm^{-1}. (b) Evolution of the 2D band at 514 nm with the number of layers. (c) The four components of the 2D band in bilayer (two layer) graphene at 514 and 633 nm. (adapted from [68])

Figure 1.19 (a) is the Raman spectra of graphite and graphene, respectively. The two most notable features are the G peak at 1580 cm^{-1} and 2D (also known as G') peak at 2700 cm^{-1}. There is also another small peak near 1350cm^{-1} known as the D peak. (This peak is not so apparent in Figure 1.19). The G peak originates from the doubly

degenerate (iTO and LO) phonon mode at the Brillouin zone center[67]. On the other hand, the 2D and D peaks are due to second-order processes, involving two iTO phonons near the K point for the 2D peak or one iTO phonon and one defect in the case of the D peak[67]. Thus higher D peak intensity corresponds to higher level of defects. Note that the G peak intensity of graphene and graphite is comparable. [Figure 1.19 (a) is rescaled to show similar 2D band intensity.]

As the graphene layer become thicker, a significant change of the 2D peak in both the shape and the intensity is observed as shown in Figure 1.19 (b). One very important observation is that for single layer graphene, 2D peak has a single symmetric peak but for double layer graphene, the 2D peak can be fitted with 4 different peaks as shown in Figure 1.19 (c). The four components of 2D peak are due to the splitting of electronic bands. In bilayer graphene, the interaction of the graphene planes causes the electronic band to divide into four bands, with a different splitting for electrons and holes[68]. The incident Raman laser light induces electron-hole pairs and the electron-phonon scattering occurs. Then the iTO phonons (Figure 1.18) near the K point couples to all four bands resulting in phonons with four different momenta. These wave vectors correspond to phonons with different frequencies and result in four different peaks in the 2D band Raman spectra. Hence, it is possible to distinguish single layer and bilayer graphene from Raman spectra by observing the 2D peak shape and intensity. Notably, four components in the 2D band peak of bilayer graphene increase the full width at half maximum (FWHM) of the 2D band and also the ratio of 2D band to G band is smaller for bilayer graphene. It is worth noting that up to three layers of graphene, these methods are reliable enough but as the layers get thicker, it is more difficult to distinguish the signals from those of a bulk graphite.

Transmission electron microscopy can also be used to distinguish single layer and bilayer graphene. Figure 1.20 is the TEM diffraction pattern of a bilayer graphene layer at

normal incidence. Innermost diffraction spot s are from the (100) planes, while second innermost ones are from the (110) planes.

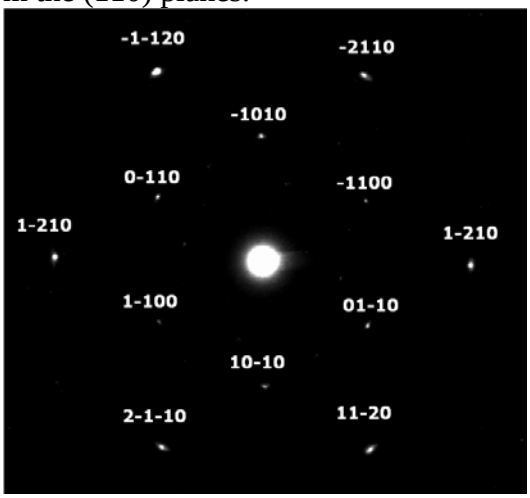

Figure 1.20 Diffraction pattern of a bilayer graphene layer from transmission electron microscopy and its Bravais-Miller indices. Six fold symmetry is clearly observable.

One definitive indication of single layer graphene is that its reciprocal space (Figure 1.20) has only the zero-order Laue zone and, therefore, no dimming of the diffraction peaks should occur at any angle [70]. In contrast, the diffraction peaks will dim for crystal lattices in three dimension. Hence, for bilayer graphene, the peaks would be suppressed strongly at some angle. Another indication is the peak intensity ratio of (100) plane and (110) plane. From kinematic calculation, it has been derived that the intensity ratio of these two planes would be ~1.1 for single layer graphene and ~0.28 for bilayer graphene[71]. In other words, for bilayer graphene, the outer (110) plane intensity would be stronger than the inner plane (100) intensity while the opposite is true for single layer graphene.

It is also possible to verify the number of layers by using electrical characterization methods by applying a perpendicular electric field and observing its carrier transport properties. The hamiltonian that describes the electronic properties of bilayer graphene near the Fermi level is shown in equation 2.1 [72].

$$H = \begin{bmatrix} \Delta & -\frac{h}{8\pi^2 m} v_F (k_x - ik_y)^2 \\ -\frac{h}{8\pi^2 m} v_F (k_x + ik_y)^2 & -\Delta \end{bmatrix} \quad \text{.....Equation 2.1}$$

where k is the momentum, v_F is the Fermi velocity, h is the Plank constant, and Δ is the onsite energy difference between the two sublattices in the graphene crystal. Normally the Δ is zero and the hamiltonian results in a quadratic dispersion relations with zero bandgap. To open up a bandgap in bilayer graphene, the inversion symmetry in the graphene plane must be broken by making Δ a non-zero value. This can be achieved by applying a perpendicular electrical field to the bilayer graphene plane[72-75]. Recently, this opening of a bandgap was observed experimentally[72, 73]. Figure 1.21(a) shows a dual gate graphene FET structure that was used to observe the top gate response curve respective to discrete back gate voltages as shown in Figure 1.21 (b). The resistance peak in each curve corresponds to the Dirac point (or charge neutrality points) for a given back gate voltage V_b. The peak resistance differs at different Dirac points because the field-induced bandgap differs[72, 73]. Lower peak resistance comes from a smaller bandgap and higher peak resistance is from a larger bandgap [73].

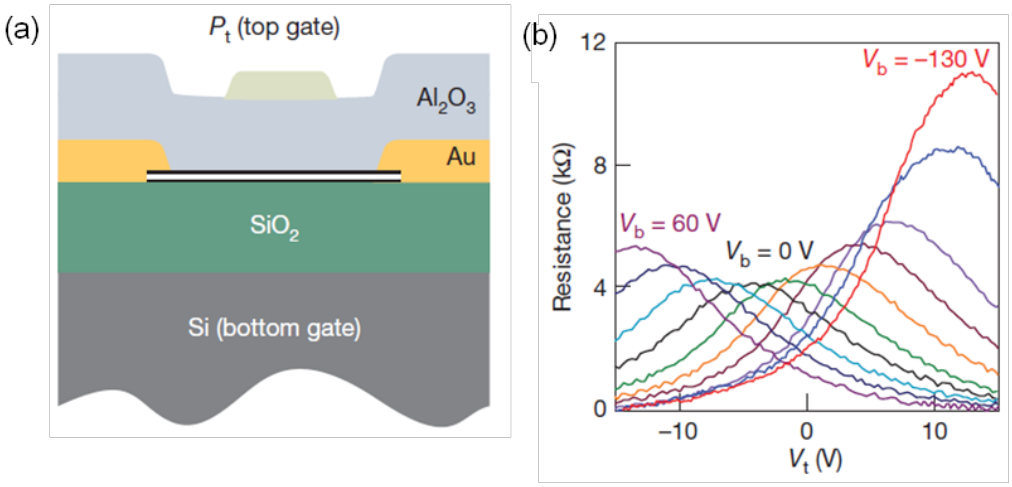

Figure 1.21 Gate response curve of double gate graphene transistor. (a) Illustration of a cross-sectional side view of the gated device. (b) Graphene electrical resistance as a

function of top gate voltage V_t at different fixed bottom gate voltages V_b. (adopted from [73])

1.6 Motivation and Goals

Graphene's most unique property is its two-dimensional structure, and the true potential of graphene may also lie in this morphology. Although other zero-dimensional and one-dimensional carbon nanostructures were studied for a longer period of time, the difficulty in controlling the exact position and the concentration of these individual nanomaterials was a major obstacle in commercialization for integrated electronics[26]. Furthermore, the chirality (directionality of graphitic hexagonal lattice) and the thickness of one-dimensional carbon nanotubes were very important as they determined the bandgap and the electronic behavior of the individual nanotubes[6]. Controlling these parameters of carbon nanotubes in a reliable way is still a challenge even after two decades of study since its discovery[26]. On the other hand, graphene's two-dimensional property allows the facile integration of bottom-up nanomaterial synthesis with top-down lithographic fabrication. After graphene is transferred onto a substrate, a conventional semiconductor fabrication process can be used to manufacture various devices. This property also allows seamless integration of current state-of-the-art technology with graphene. Since graphene can also be transferred to an arbitrary substrate, the possibility of utilizing exotic substrates such as plastics opens up doors for novel applications in both electronics and photonics.

The purpose of this work is to understand the fundamental properties of graphene to explore new possibilities in the field of nanoelectronics. Therefore, a thorough

characterization of the synthesis method, the film quality, the doping method, and the device fabrication is an essential component of this work. After understanding these basic qualities, the next step is to investigate new types of applications that may have been difficult or even impossible with conventional electronic components. Some of these new applications we would like to explore in this work are tunable bandgap transistors, transparent but flexible conductors, modulator circuits for radio frequency application, completely transparent flexible circuits all based on graphene material, and bipolar junction transistors based on graphene-silicon heterostructure.

1.7 Thesis Organization

In chapter 2, a novel CVD synthesis method to produce a sufficiently large area of bilayer graphene will be introduced. Until now, most bilayer graphene samples have been fabricated using mechanical exfoliation of graphite[27, 72, 73, 76]. These samples have limited sizes of μm^2 and are certainly not scalable. Bilayer graphene has an electric-field-induced bandgap up to 250 meV,[27, 72-76], as explained earlier, and this property eliminates the need for extreme scaling or costly substrates. Furthermore, exciton binding energies in bilayer graphene are also found to be tunable with an electric field.[77] The motivation of chapter 2 is to develop a reliable and rational method to produce a large-area bilayer graphene to harness the unique ability to control the bandgap.

Highly homogenous growth of bilayer graphene will be confirmed experimentally by using optical and electrical characterization methods. The optical characterization methods introduced in chapter 2 include Raman spectroscopy (both the single-shot method and the two-dimensional raster scanning method) and transmission

electron microscopy (TEM) diffraction-pattern analysis. Atomic force microscopy (AFM) and scanning electron microscopy (SEM) were also used to probe the characteristics of the graphene layer. The electrical characterization will include the fabrication of dual-gate bilayer graphene transistor structure, carrier transport measurement, and yield analysis.

Upon successful demonstration of wafer-scale bilayer graphene synthesis, the possibility of using graphene as a transparent conductor is explored in chapter 3. As explained earlier, its relatively high electrical conductivity and optical transparency make it an excellent candidate for transparent conducting material. Potential applications for graphene-based transparent conductors would be touchscreens, liquid crystal displays, organic photovoltaic cells, and organic light-emitting diodes. One of the key challenges for making graphene transparent conductors is achieving low enough sheet resistance with a transmittance value comparable to those of conventional transparent conductive materials. The second challenge is achieving uniform sheet resistance across the area. In order to satisfy both of these criteria, stacking of single-layer graphene has been the method of choice in the recent studies[48, 49, 52]. In chapter 3, a more efficient method of achieving uniform, high quality transparent conductors with homogeneous bilayer graphene films is introduced. The sheet resistance value is lowered even more by introducing a room temperature chemical doping method. The quality of the material is fully characterized by measuring the sheet resistance value as a function of the transmittance value in comparison with other published works. In the final section of chapter 3, a comprehensive comparison with the conventional indium oxide-based

transparent conductor, in terms of its mechanical flexibility, reveals the robustness of bilayer graphene-based conductors.

The study on graphene transparent conductors leads to an interesting conclusion: graphene material can be used as a low resistance material for interconnects as well as a channel material for transistors. This is analogous to silicon as it is also possible to modify the property of silicon by introducing chemical dopants, albeit at high temperature. Adding to the fact that graphene is highly flexible and that low temperature processing is possible after the graphene transfer process, an all-graphene circuit is demonstrated in chapter 4. Graphene was used to make the channels, the interconnects, the resistors, and the source/drain/gate electrodes of this circuit without using any metal.

This is the first demonstration of an all-graphene circuit, and due to its monolithic structure, the circuit is fully flexible (up to 2.7% strain) and transparent (~95% transmittance). This opens up new opportunities in flexible electronics mainly because of graphene's unique property as a flexible electronics material. Most materials that are used in flexible electronics are either amorphous[78, 79] or organic[80]. It is known that mobilities of these materials are quite limited, usually lower than 10 $cm^2V^{-1}s^{-1}$. This mobility value is not the limiting factor for low-speed applications such as flexible batteries[81, 82] and flexible tactile sensors[44, 45]. However, nearly all flexible electronic devices require a data communication module, which requires high frequency components and transistors. Without harnessing the communication module inside the flexible apparatus, the lack of portability will severely limit the functionality of various flexible applications.

Graphene, on the other hand, is a material with a mobility value several orders of magnitude higher than those of conventional amorphous or organic material[17, 19]. This opens up new possibilities in the field of flexible high-speed electronics. Several recent works in graphene analog electronics have led to the development of high-speed transistors[83, 84] and analog circuits such as frequency doublers[29, 30], mixers[33, 34], and modulators[28] signifying the feasibility of graphene analog circuits that are also flexible. In the same context, the all-graphene circuits were designed to function as modulator circuits to encode digital information to a higher frequency carrier wave. The ambipolarity of the graphene transistors was fully exploited to perform quaternary digital modulations with just one or two transistors. Furthermore, the whole circuit was fabricated with graphene only, making it not only fully flexible but also completely transparent with its monolithic structure. This feature is an additional benefit for other applications that require transparency, such as touch screens or electronics-embedded smart glasses.

Although graphene is known for its extraordinary characteristics, the lack of an energy bandgap and the low on/off ratio is a persistent problem. In addition, the weak saturation behavior due to its ambipolar transfer characteristics limits the transistor's intrinsic gain and cut-off frequency. In Chapter 5, the first bipolar transistor based on graphene/silicon heterojunction will be introduced. The graphene/silicon junction has several unique properties, such as bias dependent work function and variable Schottky barrier. Exploiting these unusual traits, high on/off ratio and high gain will be demonstrated. A comparison with a metal-based surface barrier transistor will also

confirm the higher emitter injection efficiency of the graphene/silicon junction compared to a normal Schottky junction.

Conclusions and summary are outlined in Chapter 6.

Chapter II

Wafer Scale Homogeneous Bilayer Graphene Films by Chemical Vapor Deposition

2.1 Introduction

The discovery of electric field induced bandgap opening in bilayer graphene opens new door for making semiconducting graphene without aggressive size scaling or using expensive substrates. However, producing bilayer graphene was previously achieved mostly by mechanical exfoliation, and synthesis of wafer scale bilayer graphene posted tremendous challenge. In this chapter, we report homogeneous bilayer graphene films over at least 2 inch × 2 inch area, synthesized by chemical vapor deposition on copper foil and subsequently transferred to arbitrary substrates. The bilayer nature of graphene film is verified by Raman spectroscopy, atomic force microscopy (AFM), and transmission electron microscopy (TEM). Importantly, spatially resolved Raman spectroscopy confirms a bilayer coverage of over 99%. The homogeneity of the film is further supported by electrical transport measurements on dual-gate bilayer graphene transistors, in which bandgap opening is observed in 98% of the devices.

2.2 Synthesis of Bilayer Graphene Films

2.2.1 Chemical Vapor Deposition Process

Recent developments in CVD method have allowed successful production of large scale single-layer graphene on metal substrate. However, the synthesis of uniform bilayer graphene film remains extremely challenging. Here we report the first synthesis of wafer scale bilayer graphene film limited only by our synthesis apparatus. Our method is based on CVD growth of bilayer graphene on copper surface, and is characterized by the depletion of hydrogen, high vacuum, and slower cooling rate compared to previous single-layer graphene synthesis.[2, 66, 85]

First, 25μm thick copper foil (99.8%, Alfa Aesar) was loaded into an inner quartz tube inside a 3 inch horizontal tube furnace of a commercial CVD system (First Nano EasyTube 3000). The system was purged with argon gas and evacuated to a vacuum of 0.1 Torr. The sample was then heated to 1000°C in H_2 (100 sccm) environment with vacuum level of 0.35 Torr. When 1000°C is reached, 70 sccm of CH_4 is flowed for 15 minutes at vacuum level of 0.45 Torr. The sample is then cooled slowly to room temperature with a feedback loop to control the cooling rate. The vacuum level is maintained at 0.5 Torr with 100 sccm of argon flowing. The time plot of the entire growth process is shown in Figure 2.1.

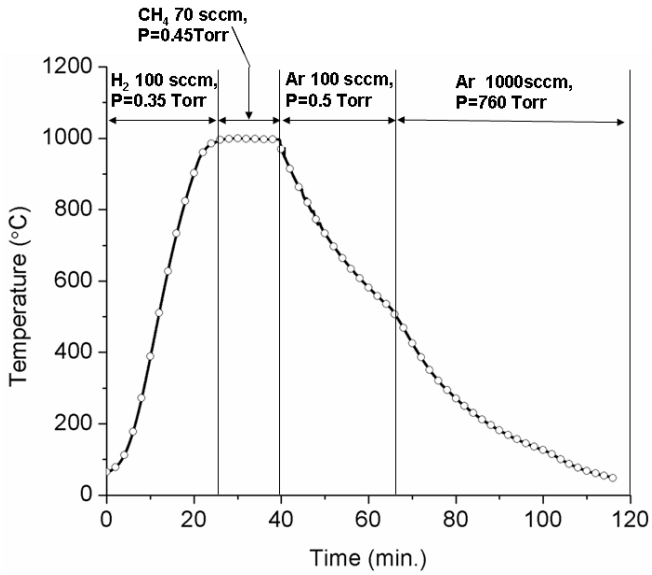

Figure 2.1 Temperature vs. time plot of bilayer graphene growth condition. Pressure value is denoted as "P".

2.2.2 Transfer Process

Two different methods were used to transfer bilayer graphene from copper foil to SiO_2 substrates. The first method utilize thermal release tape (Nitto Denko) to transfer bilayer graphene from the copper foil.1 The tape was attached to the copper surface and a force of 6.25 N/cm^2 was applied to the copper/bilayer graphene/tape stack for 10 minutes with EVG EV520IS wafer bonder. The other side of the copper is exposed to O_2 plasma for 30 seconds to remove the graphene on that side. The copper was etched away using iron (III) nitrate (Sigma Aldrich) solution (0.05g/ml) for 12 hours. A 4 inch silicon wafer with thermally grown SiO_2 was precleaned with nP12 nanoPREP using plasma power of 500W for 40 seconds to modify the surface energy and produce a hydrophilic surface. The tape and bilayer graphene stack was transferred to the precleaned SiO2 wafer and a force of 12.5N/cm^2 was applied for 10 minutes. The substrate was then

heated to 120 °C to eliminate the adhesion strength of the thermal release tape. The tape was then peeled off and the adhesive residue was removed with warm acetone.

Polymethyl methacrylate (PMMA) can also be used instead of thermal release tape to transfer bilayer graphene. This method is easier as it does not require a bonding tool but the edge part of the graphene is usually rough due to uneven thickness of spin coated PMMA at the edge. In this method, one side of the sample is coated with 950PMMA A6 (Microchem) resist and cured at 180°C for 5 minutes. The other side of the sample is exposed to O_2 plasma for 30 seconds to remove the graphene on that side. The sample is then left in iron (III) nitrate (Sigma Aldrich) solution (0.05g/ml) for at least 12 hours to completely dissolve away the copper layer. The sample is transferred on to a silicon substrate with thermal oxide. The PMMA coating is removed with acetone and the substrate is rinsed several times.

2.3 Optical characterization of bilayer graphene films

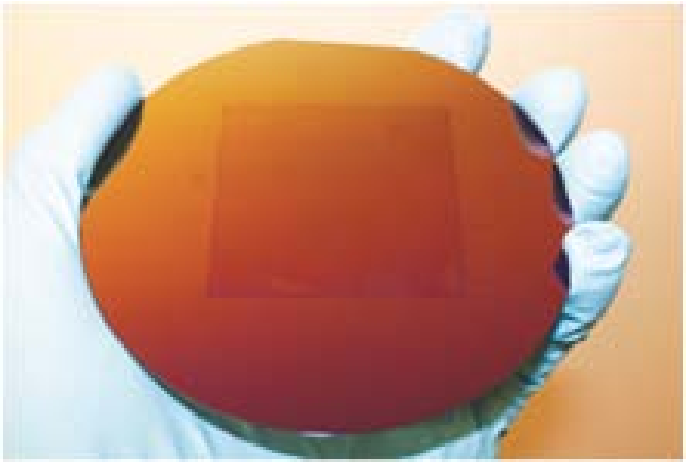

Figure 2.2 Wafer scale homogeneous bilayer graphene film grown by CVD. Photograph of a 2 inch by 2 inch bilayer graphene film transferred onto a 4 inch Si substrate with 280nm thermal oxide.

Figure 2.3 Optical microscopy image showing the edge of bilayer graphene film. Scale bar is 100 μm.

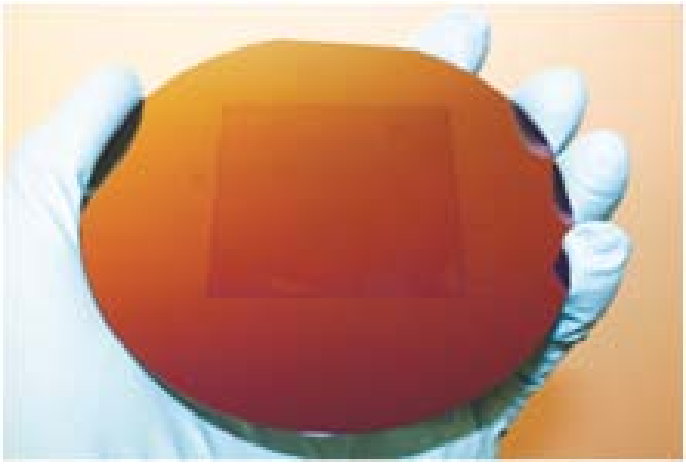

Figure 2.2 shows photographic image of a wafer scale (2 inch × 2 inch) bilayer graphene film transferred onto a 4 inch silicon wafer with 280 nm thick SiO_2. A typical optical microscope image (Figure 2.3) of the transferred bilayer graphene film shows almost no color variation except for the region where the film is torn and folded (lower right of Figure 2.3). To identify the number of layers for our graphene sample, the film thickness is first measured using AFM (Figure 2.4). Height profiles across patterned graphene edges show that thickness of our graphene samples range from 0.9 nm to 1.3 nm, suggesting number of graphene layers below 3.

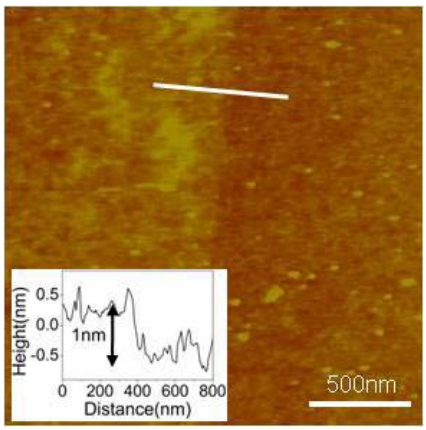

Figure 2.4 AFM image of bilayer graphene transferred onto SiO_2/Si. (Inset) Height profile obtained by taking cross section along the white line on the image. The heights of our bilayer graphene were consistently found to be between 0.89nm and 1.2nm.

2.3.1 Raman spectroscopy

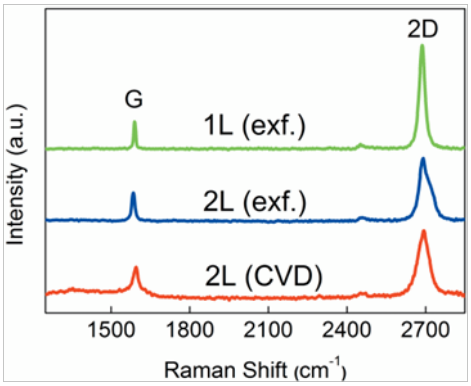

Figure 2.5 Raman spectra taken from CVD grown bilayer graphene (red solid line), exfoliated single-layer (green solid line) and bilayer graphene (blue solid line) samples. Laser excitation wavelength is 514 nm.

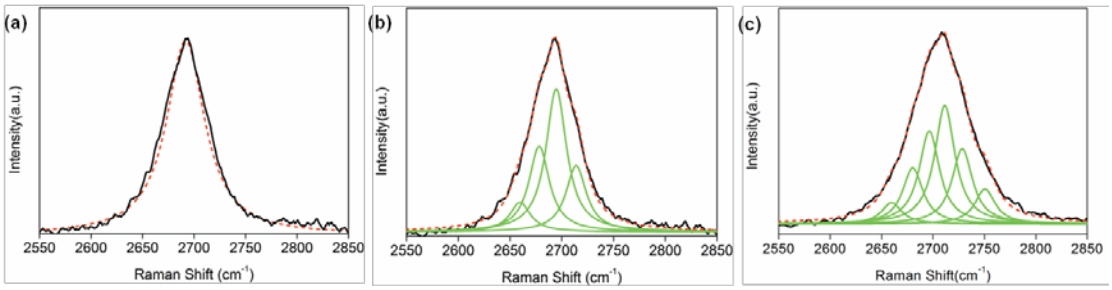

Figure 2.6 The measured 2D Raman band of a bilayer with the FWHM of 45cm^{-1}. (1) Single Lorentzian fit (red dash line) of the peak of Figure 2.6a clearly shows deviation from the measured 2D band. (b)The peak can be well-fitted with the sum of four single Lorentzian (green solid line) of 24cm^{-1} FWHM. (c), The measured 2D Raman band of a trilayer with the FWHM of 62cm^{-1}. 2D peak of trilayer are fitted with six single Lorentzian (green solid line)

We further performed Raman spectroscopy measurements (Renishaw spectrometer at 514nm) on ten randomly chosen spots across the film, and compared them with reference samples prepared by mechanically exfoliating Kish graphite [67, 76, 86]. The red curve in Figure 2.5 represents a typical Raman spectrum from our sample. Two peaks are clearly visible between Raman shift of 1250 cm^{-1} – 2850 cm^{-1}, corresponding to the G band (~1595 cm^{-1}) and 2D band (~2691 cm^{-1}), respectively. Importantly, the spectrum exhibits several distinctive features. First, 2D band shows higher peak intensity than G band with the 2D-to-G intensity ratio I_{2D}/I_G ~2.31, suggesting the number of graphene layers less than 3.[2, 68, 87] Second, the full width at half maximum (FWHM) of 2D band peak is measured to be ~45 cm^{-1}, exceeding the cut-off of ~30 cm^{-1} for single-layer graphene.[67, 86, 88]

Third, the 2D band peak cannot be fitted with single Lorentzian [Figure 2.6 (a)], but fitting from four Lorentzian peaks with a FWHM of 24 cm^{-1} yields excellent agreement [Figure 2.6 (b)]. Raman spectra taken from the other 9 spots show similar features with

the 2D band FWHM of 43~53 cm^{-1}. These observations are strong reminiscent of characteristic bilayer graphene Raman spectrum. In addition, reference Raman spectra taken under identical conditions from exfoliated single-layer (green curve) and bilayer (blue curve) graphene are also presented in Figure 2.5. Exfoliated single-layer graphene shows a 2D band FWHM of 24 $cm^{-1}$and I_{2D}/I_G of 3.79, while exfoliated bilayer graphene shows a FWHM of 46 cm^{-1} and I_{2D}/I_G of 2.25. Together, the AFM height measurements, the Raman spectra, and the direct comparison with the exfoliated samples clearly support the bilayer nature of our CVD synthesized graphene film. We also measured the D band to G band intensity ratio, I_D/I_G, of our bilayer graphene sample to be around 0.11~0.3, indicating a relatively low defect density.

2.3.2 Transmission electron microscopy

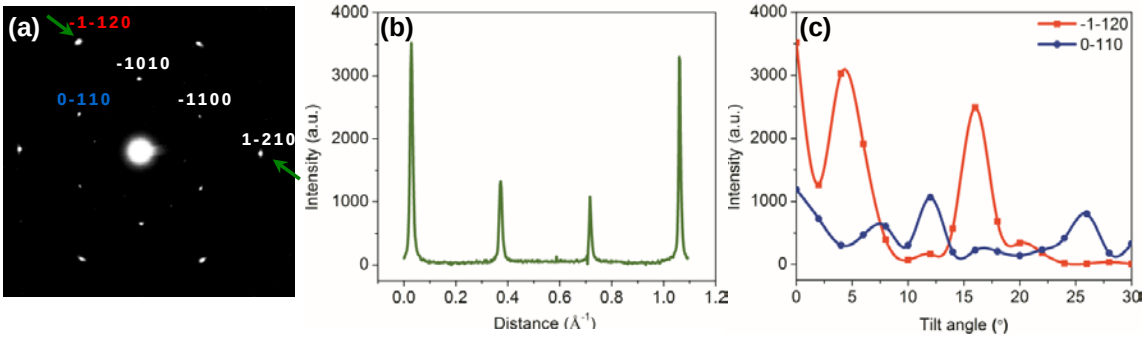

Figure 2.7 Selected area electron diffraction pattern of bilayer graphene. (a) Normal incident diffraction pattern of bilayer graphene sample. The bilayer graphene film was transferred onto copper grid with holy carbon supporting film. The diffraction image was taken by JEOL 2010F Analytical Electron Microscope with acceleration voltage of 200 kV. (b) Profile plot of diffraction peak intensities across a line cut indicated by the green arrows shown in (a). (c) Diffraction peak intensities as a function of tilt angle for (0-110) (in red) and (-1-120) (in blue).

TEM selected area electron diffraction pattern was measured to further characterize the graphene film [Figure 2.7 (a)]. The six-fold symmetry is clearly visible

and Bravais-Miller (hkil) indices are used to label the diffraction peaks. Importantly, the diffraction intensities of inner peaks from equivalent planes [1100] are always higher than outer peaks from [2100]. The intensity ratios of I_{-1010}/I_{-1-120} and I_{-1100}/I_{1-210} are close to 0.28 [Figure 2.7 (b)], indicating that the film is not a single layer and it retains AB stacking structure [70, 71, 89]. We further studied the tilt angle-dependent diffraction peak intensity for both inner and outer peaks. As shown in Figure 2.7 (c), both (0-110) and (-1-120) peaks show strong intensity modulation with tilt angle, and both peaks can be suppressed completely at certain angle. It is known that monolayer graphene has only zero order Laue zone and weak intensity modulation is expected at any angle.[70, 89] Our TEM results again agree with AFM and Raman measurements for the bilayer nature of the graphene film. We also notice additional diffraction spots, which are caused by the residues on the film due to insufficient sample cleaning.

2.3.3 Two dimensional Raman raster scan

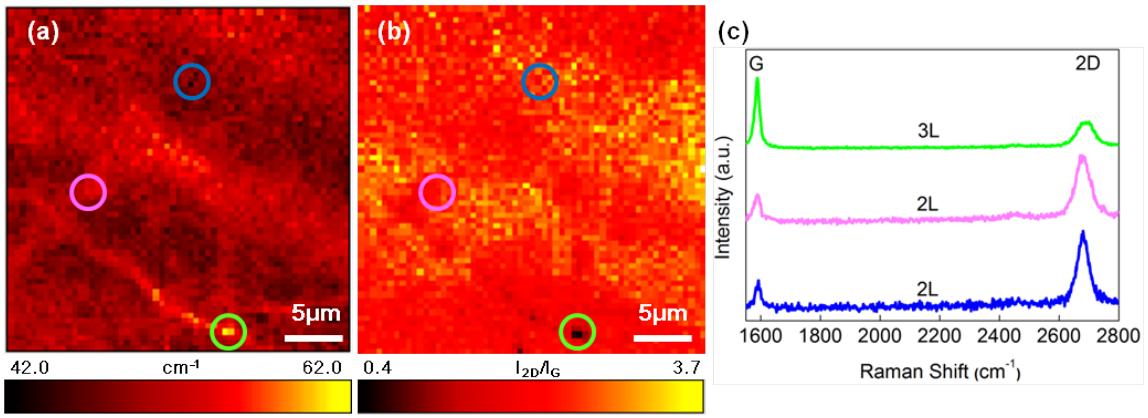

Figure 2.8 Spatially resolved Raman spectroscopy of CVD bilayer graphene. (a) and (b), Two-dimensional color mapping of the FWHMs of Raman 2D band and I_{2D}/I_G ratios over 30 μm × 30 μm area, respectively. (c) Raman spectra from the marked spots corresponding colored circles showing bilayer and trilayer graphene.

To further evaluate the uniformity of CVD grown bilayer graphene film, we performed spatially resolved Raman spectroscopy. Here, identifications of the number of graphene layers rely on combination of the FWHM of 2D band[2, 67, 68, 88, 90] and peak intensity ratio $I_{2D}/I_{G.}$[2, 60, 68, 87] Figure 2.8 (a) shows a color map of the 2D band peak width over 30 μm by 30 μm area, with FWHM values ranging from 42 cm^{-1} (dark color) to 63cm^{-1} (bright yellow). The data show uniformly distributed red color with only a few localized yellow spots. The peak intensity ratios I_{2D}/I_G are also mapped in color [Figure 2.8 (b)] over the same area, with values ranging from 0.37 (dark color) to 3.77 (bright yellow). Comparisons between Figure 2.8 (a) and Figure 2.8 (b) reveal that larger peak widths are consistent with smaller I_{2D}/I_G ratios. Furthermore, Figure 2.8 (c) compares the Raman spectra taken from three representative spots indicated using green, pink, and blue circles. Raman spectrum taken at green-circled spot has the largest FWHM (62.9 cm^{-1}) and smallest I_{2D}/I_G (0.37), indicating trilayer graphene [Figure 2.6 (c)]; pink-circled (blue-circled) spot shows FWHM = 55 cm^{-1} and I_{2D}/I_G = 2.2 (FWHM = 43.8 cm^{-1} and I_{2D}/I_G = 2.91), indicating bilayer graphene. These results confirm that the CVD bilayer graphene film is highly homogeneous, with only very small fraction corresponding to possibly 3 layers.

We then quantified the bilayer graphene coverage by studying the statistics of 2D band peak width and I_{2D}/I_G ratio. Figure 2.9 (a) illustrates the histogram of the FWHMs of 2D band taken from the Raman mapping. The average peak width is determined to be 51 ± 2 cm^{-1}. Furthermore, cumulative counts plotted in Figure 2.9 (b) indicate that more than 99% of the FWHM values are below 60 cm^{-1} (pink spheres). In addition, the histogram of I_{2D}/I_G ratios (Figure 2.9 (a), inset) shows an average value of 2.4 ± 0.4, and

the corresponding cumulative count plot (Figure 2.9 (b), inset) shows that more than 99% of I_{2D}/I_G ratios are larger than 1. Using FWHM = 60 cm^{-1} together with I_{2D}/I_G = 1 as the crossover values between bilayer and trilayer graphene, our data give an estimate of at least 99% coverage of bilayer graphene with less than 1% of trilayer over the entire area.

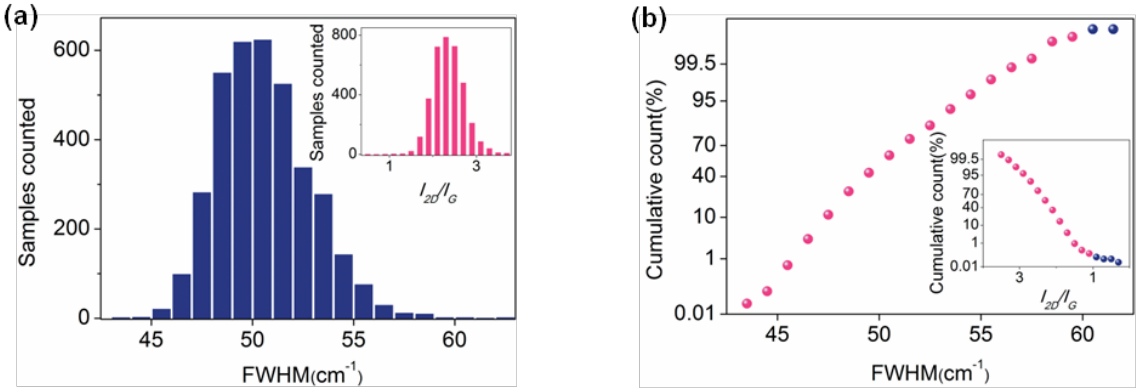

Figure 2.9 . (a) Histogram of the FWHMs of Raman 2D band corresponding to area shown in Figure 2.8 (a). (Top right Inset) Histogram of I_{2D}/I_G ratios for the same area. (b) Cumulative count plot of FWHMs of 2D band. Pink (blue) spheres represent the FWHM less (more) than 60 cm-1. (Inset) Cumulative count plot of I_{2D}/I_G ratios. Pink (blue) spheres indicate the ratio larger (smaller) than 1. (For Raman mapping, λ_{laser}=514 nm, 500nm step size, 100x objector).

2.4 Electrical characterization of bilayer graphene films

2.4.1 Fabrication

A direct verification of the bilayer nature of our CVD graphene film comes from electrical transport measurements. For this purpose, dual-gate bilayer graphene transistors were fabricated with three different dimensions, channel length and channel width of 1 μm×1μm, 1 μm×2μm, and 2 μm×2μm, respectively. A scanning electron microscope (SEM) image and an illustration of the fabricated device are shown in Figure 2.10. All devices have a local top gate and a universal silicon bottom gate with Al_2O_3 (40nm) and

SiO_2 (310 nm) as the respective gate dielectrics. This dual-gate structure allows simultaneous manipulation of bilayer graphene bandgap and the carrier density by independently inducing electric fields in both directions.[72, 73]

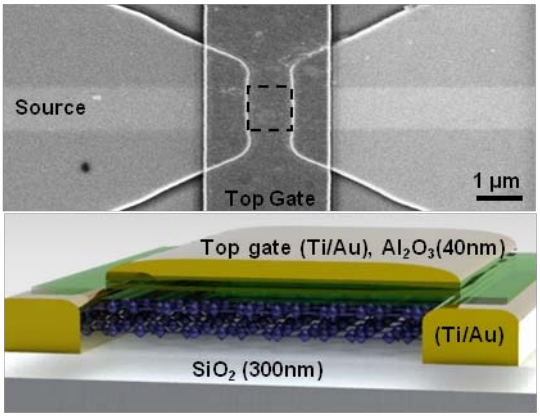

Figure 2.10 Electrical transport studies on dual-gate bilayer graphene devices. Scanning electron microscopy image (top) and illustration (bottom) of a dual-gate bilayer device. The dashed square in the SEM image indicates the 1μm × 1μm bilayer graphene piece underneath the top gate.

2.4.2 Electrical measurement of band gap

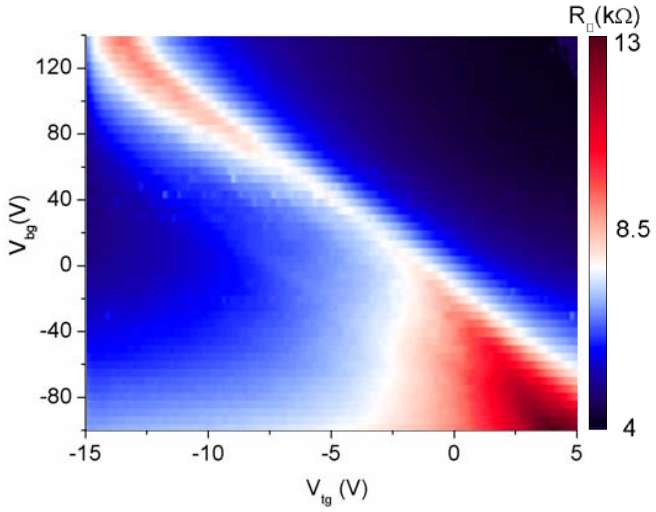

Figure 2.11 Two dimensional color plot of square resistance $R_{\square}$ vs. top gate voltage V_{tg} and back gate voltage V_{bg} at temperature of 6.5K.

Figure 2.11 shows a two dimensional color plot of square resistance $R_{\square}$ vs. both top gate voltage (V_{tg}) and bottom gate voltage (V_{bg}), obtained from a typical 1×1 μm device at 6.5 K. The red and blue colors represent high and low square resistance, respectively. The data clearly show that $R_{\square}$ reach peak values along the diagonal (red color region), indicating a series of charge neutral points (Dirac points) when the top displacement fields cancel out the bottom displacement fields.[72, 73] More importantly, the peak square resistance, $R_{\square,\ Dirac}$, reaches maximum at the upper left and lower right corner of the graph, where the average displacement fields from top and bottom gates are largest.

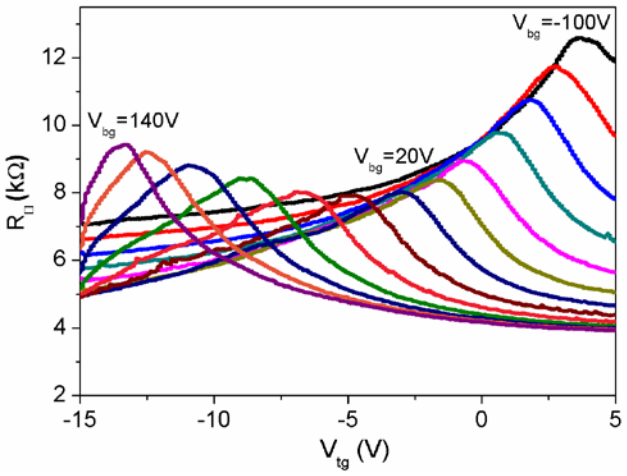

Figure 2.12 $R_{\square}$ vs. V_{tg} at different value of fixed V_{bg}. The series of curves are taken from Vbg of -100V to 140V, with 20V increment.

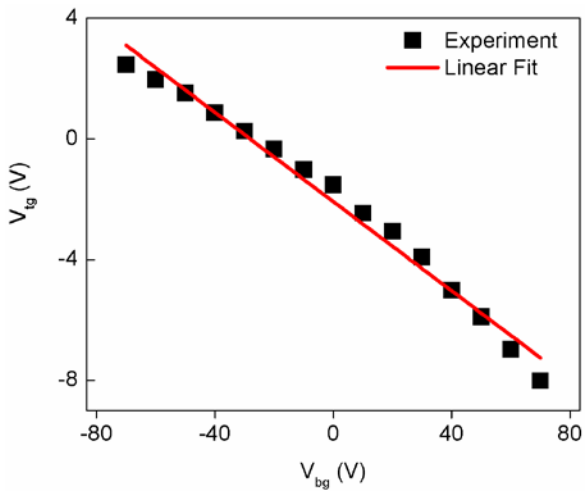

Figure 2.13 The charge neutral points indicated as set of (V_{tg}, V_{bg}) values at the peak square resistance $R_{\square,dirac}$. The red line is the linear fit. The electrical measurements were carried out in a closed cycle cryogenic probe station (LakeShore, CRX-4K), using lock-in technique at 1kHz with AC excitation voltage of 100μV.

Horizontal section views of the color plot in Figure 2.11 are also shown in Figure 2.12, with $R_{\square}$ plotted against V_{tg} at fixed V_{bg} from -100 to 140 V. Once again, for each $R_{\square}$ vs. V_{tg} curve square resistances exhibit a peak value, and $R_{\square,\ Dirac}$ increases with increasing V_{bg} in both positive and negative direction. The charge neutral points are further identified in Figure 2.13 in terms of the (V_{tg}, V_{bg}) values at $R_{\square,\ Dirac}$. Linear relation between V_{tg} and V_{bg} is observed with a slope of -0.073, which agrees with the expected value of $-\varepsilon_{bg}d_{tg}/\varepsilon_{tg}d_{bg}$ = -0.067, where ε and d correspond to the dielectric constant and thickness of the top gate (Al_2O_3: d_{tg} = 40nm, ε_{tg}=7.5) and bottom gate (SiO_2: d_{bg} = 310nm, ε_{bg}=3.9) oxide.[72, 73] We also notice the deviation from linear relation at high field; the origin of which is not understood currently and requires further study.

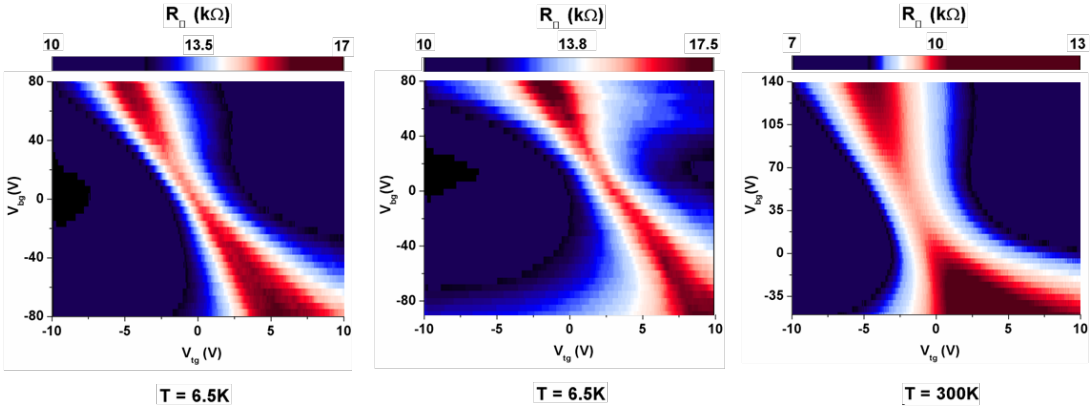

Figure 2.14 Three dual-gate graphene devices showing bilayer transport behavior.

Similar results from three other devices are shown in Figure 2.14, and more than 46 measured devices show qualitative agreement. These electrical characterizations yield direct evidence for the successful synthesis of bilayer graphene. The observation of increasing $R_{\square,\,Dirac}$ values at higher fields is an unmistakable sign of bandgap opening in bilayer graphene.[72, 73] In comparisons, the peak resistance at the charge neutral point should remain roughly constant for single-layer graphene,[72] while $R_{\square,\,Dirac}$ decreases at higher field for trilayer graphene.[91] In addition, we also compared the temperature dependence of $R_{\square,\,Dirac}$ at V_{bg} ~ 0V and V_{bg} ~ -100 V (Figure 2.15).

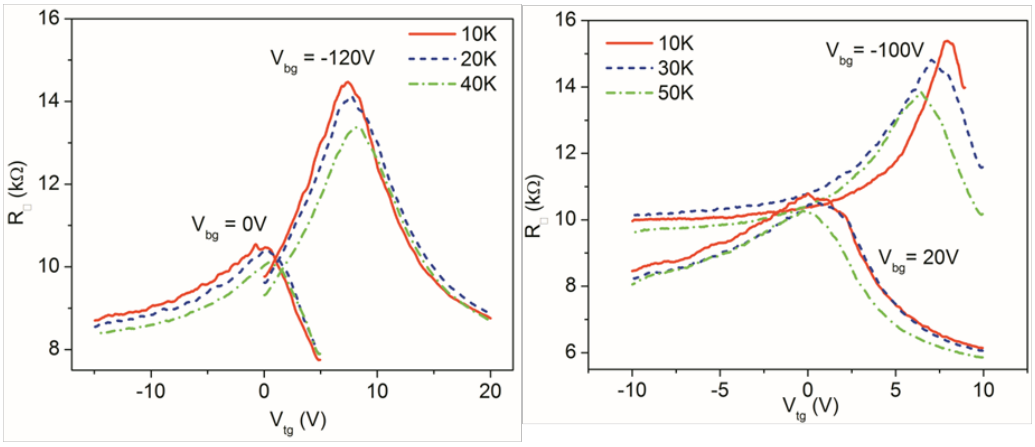

Figure 2.15 Two dual-gate graphene devices showing temperature dependent resistance versus top gate voltage sweep at two different back gate voltages.

Larger variation of $R_{\square,\ Dirac}$ vs. temperature is observed under higher electric field, which again agrees with field-induced bandgap opening in bilayer graphene.[72, 73] We note that the observed resistance modulation due to electric field and temperature are smaller compared to devices made by mechanical exfoliation,[72, 73] which can be attributed to the polycrystalline nature of CVD graphene film. We also note that our devices show large fluctuations of the offset voltage (from impurity and surface doping), with some cases exceeding 140 V for the bottom gate. This could be caused by the ion residues from the etching process, and further investigations are needed.

2.4.3 Yield and distribution

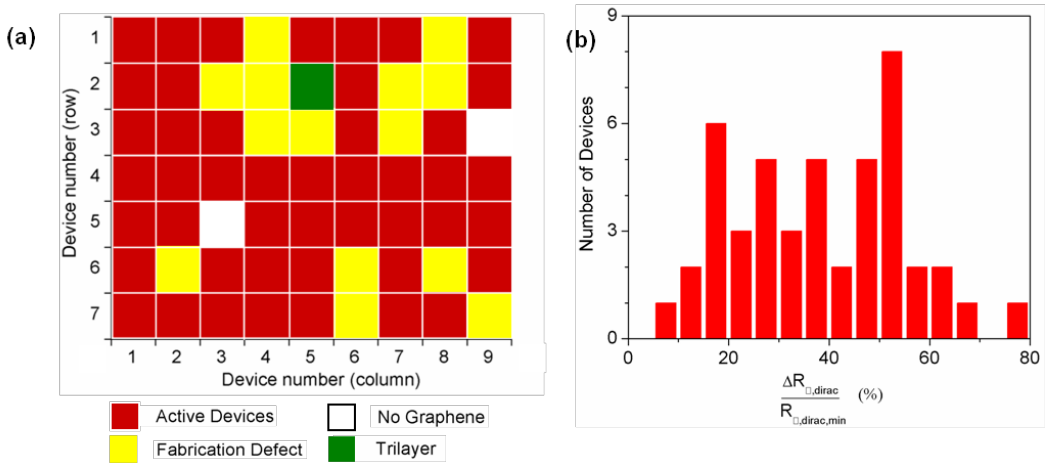

Figure 2.16 Bilayer statistics from electrical transport measurement on dual-gate graphene devices. (a) A color-coded map of 63 devices (7 rows x 9 columns) fabricated across the same graphene film. The red squares indicate bilayer graphene confirmed by transport measurement; the yellow squares indicate devices which have fabrication defects; the white squares mark the region with no graphene; and the green square represents device with trilayer response from the transport measurement. (b) Histogram of $\Delta R_{\square,dirac}$ / $R_{\square,dirac,min}$ values in percentage for 46 active devices.$\Delta R_{\square,dirac}$ corresponds to the maximum difference in $R_{\square,dirac}$ within V_{tg} of ±10V and V_{bg} of ±120V. $R_{\square,dirac,min}$ is the minimum peak resistance.

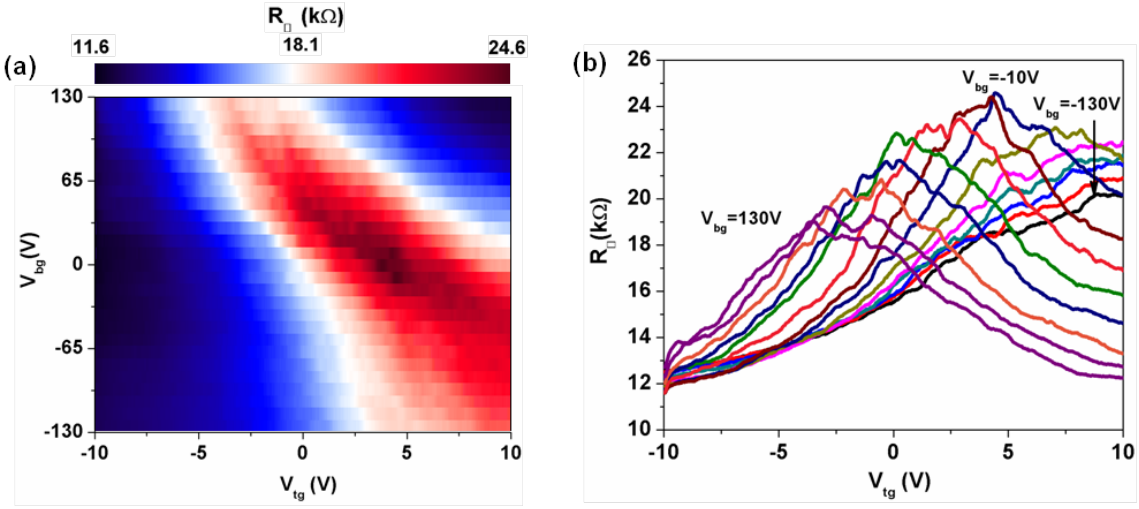

Figure 2.17 (a) A device showing trilayer transport behaviour. The observed peak square resistance decreases as increasing field. This is distinctively different from bilayer response. (b) Horizontal section views with R□ plotted against V_{tg} at fixed V_{bg} from -130 to 130 V with 20V increment.

We also studied the statistics of bilayer graphene occurrence for 63 (7 row x 9 columns) dual-gate devices fabricated across the same film [Figure 2.16 (a)]. 46 out of 63 devices show bilayer graphene behaviors, characterized by increasing $R_{\square,Dirac}$ at larger fields. Of the remaining devices, 2 devices contain no graphene pieces, and 14 devices have fabrication defects.[34] Interestingly, one device shows trilayer characteristics[91] with decreasing $R_{\square,Dirac}$ under both more positive and more negative fields (Figure 2.17). Hence, 46 out of 47 (98%) working devices show bilayer characteristics. For the bilayer graphene devices, we also calculated the maximum percentage changes of peak square resistance, $\Delta R_{\square,Dirac} / R_{\square,Dirac,min}$, in which $\Delta R_{\square,Dirac}$ denotes the maximum difference in $R_{\square,Dirac}$ within V_{tg} of ±10V and V_{bg} of ±120V, and $R_{\square,dirac,min}$ is the minimum peak square resistance. The histogram of the percentile changes is shown in Figure 2.16 (b), with an average peak resistance change of 38% and maximum value of 77%. In addition, the average room temperature carrier mobilities were measured to be ~580 $cm^2V^{-1}s^{-1}$, which are the lower-bond values without excluding the device contact resistance. The smaller-

than-expected $R_{\square,Dirac}$ modulation is believed to be caused by defects and unintended impurity doping[73]. High quality gate dielectrics have been shown to improve the bilayer graphene device performance dramatically[27]. The electrical measurement results echo the finding from Raman measurements: our CVD grown bilayer graphene film is highly homogeneous.

2.5 Discussion and conclusion

Lastly, we would like to comment on the key growth parameters for our CVD bilayer graphene films. It has been suggested that graphene growth on copper surface is self-limited to single layer[2], but both of our Raman and electrical characterizations clearly prove otherwise. We systematically varied the key growth conditions, and the resulting film quality was evaluated using Raman spectroscopy (Table 2-1).

Sample Number	Growth Pressure (Torr)	Growth Temperature (°C)	Growth Time (min)	Ar Flow rate (sccm)	CH_4 Flow rate (sccm)	H_2 Flow rate (sccm)	2D Band FWHM (cm^{-1})	I_{2D}/I_G	I_D/I_G	Cooling rate (°C/min)
1	0.5	1000	15	0	70	0	46.6	2.628	0.258	18
2	0.5	1000	15	0	140	0	47	2.12	0.57	18
3	Ambient	1000	15	1000	50	0	59.12	1.402	0.36	18
4	1.5	1000	15	0	40	600	60	0.64	1.11	18

Table 2-1 Comparison of graphene samples synthesized under different conditions**.**

From Table 2-1, increasing CH_4 flow rate by 2 times has no noticeable effect on 2D band width and I_{2D}/I_G values, except for a larger I_D/I_G ratio corresponding to more disorders. However, increasing growth pressure to ambient condition leads to larger 2D band width and smaller I_{2D}/I_G ratio, indicating the increasing portion of trilayer graphene. This result is consistent with recent literature, that higher pressure favors multilayer

graphene growth on copper surface.[92] Based on our results, we speculate that the key parameter for the bilayer graphene film growth is the slow cooling process (~18°C/min). Cooling rate has been found to be the critical factor for forming uniform single or bilayer graphene on Nickel [65, 66, 93].

Although the mechanism of bilayer graphene growth is an important topic, not many studies have been conducted on this area partly because the discovery was so recent. A compelling study has been recently reported on the growth of bilayer on copper substrate by isotopic labeling of methane precursors [94]. In this study, the isotope labeled graphene films were investigated by Raman mapping and ion mass spectrometry. The result shows that during the growth at high temperature, the second layer of graphene forms beneath the top graphene layer. Additionally, the second layers share the same nucleation center and the same edge termination as the first layer. This outcome is highly counter-intuitive but it explains important growth mechanism of bilayer graphene on copper substrate. This suggest that bilayer growth is promoted by catalytic decomposition of methane trapped in a nanoscale chamber between the first layer and the copper substrate[94].

The size of the homogeneous bilayer graphene films is limited only by the synthesis apparatus, which can be further scaled up. The integration with existing top-down lithography techniques should bring significant advancement for high performance, light-weight, and transparent graphene electronics and photonics. Furthermore, because the CVD grown bilayer graphene film can be transferred to arbitrary substrates, adopting

high-k dielectrics for both top and bottom gates should drastically improve the device performance.

Chapter III

Homogeneous Bilayer Graphene Film based Flexible Transparent Conductor

3.1 Introduction

Single and few-layer graphene have emerged as promising materials for novel applications in electronics due to their remarkable optical and electrical properties.[6, 7, 13, 53, 95] Their semi-metallic nature with high carrier mobility and low opacity also make them ideal candidates as transparent conductors (TC) for photovoltaic devices, touch panels, and displays.[3, 13, 48, 51]

Indium tin oxide (ITO) is commonly used as a transparent conductor for many applications, but ITO suffers from high cost, material deterioration from ion diffusion, and brittleness making it incompatible with flexible substrates.[49, 51] Graphene, on the other hand, shows great promise as a transparent conductor due to its high chemical resistivity, low manufacturing cost, and atomically thin, flexible structure.[1, 6, 49, 51, 53]

Several methods have been pursued to synthesize graphene based transparent conductor including reduction of graphene oxide[38, 96-99], liquid exfoliation using organic solvents[46, 100], and chemical vapor deposition(CVD).[2, 4, 49, 60, 61, 66, 92, 101, 102] The CVD method in particular, has drawn great attention as this method yields high quality graphene film. Homogeneous single layer graphene (SLG) can be

synthesized on a transition metal substrates with low carbon solubility (e.g. copper) using low pressure CVD (LPCVD).[2, 4] However, the sheet resistance of a pristine (undoped) SLG is still too large (2000-6000 Ω)[2, 46, 49] for it to be used as a transparent conductor. Hence, several groups have reported the SLG stacking method with layer-by-layer doping to achieve lower sheet resistance.[2, 4, 49] The drawback with this approach is that it requires a multitude of transfer processes, which increases the processing time and cost. Alternatively, multi-layer graphene (MLG) with lower sheet resistance can be directly synthesized using LPCVD method on transition metals with relatively high carbon solubility (e.g. nickel),[47, 60, 66, 101, 103, 104] or on copper substrate using atmospheric pressure CVD (APCVD) method.[92, 105] However it suffers from several drawbacks such as poor thickness uniformity[47, 60, 66, 92, 103-105] compared to LPCVD grown SLG. Fluctuation of graphene thickness will cause the sheet resistance and the transmittance to vary among different areas of the sample. There was also a report on higher level of defect on APCVD grown MLG compared to LPCVD SLG because of particulate deposition resulting from atmospheric process condition.[92] Furthermore, the MLG method eliminates the possibility of layer-by-layer doping used in a stacked SLG layer, which has been proven to lower the total sheet resistance dramatically.[4]

3.2 Preparation of bilayer graphene based transparent conductor

To this end, the use of homogeneous bilayer graphene (BLG) films for a flexible transparent conductor introduced in this chapter. The BLG films are synthesized using LPCVD on a copper substrate.[61] In contrast to CVD grown MLG,

the BLG film shows high uniformity and very low defect level.[61] By producing uniform, defect free stacks, we demonstrate a BLG based transparent conductor with 180$\Omega_{\square}$ sheet resistance at 83% transmittance. The use of homogeneous BLG films drastically reduces the processing cost and time compared to SLG based transparent conductors while maintaining high uniformity and quality.

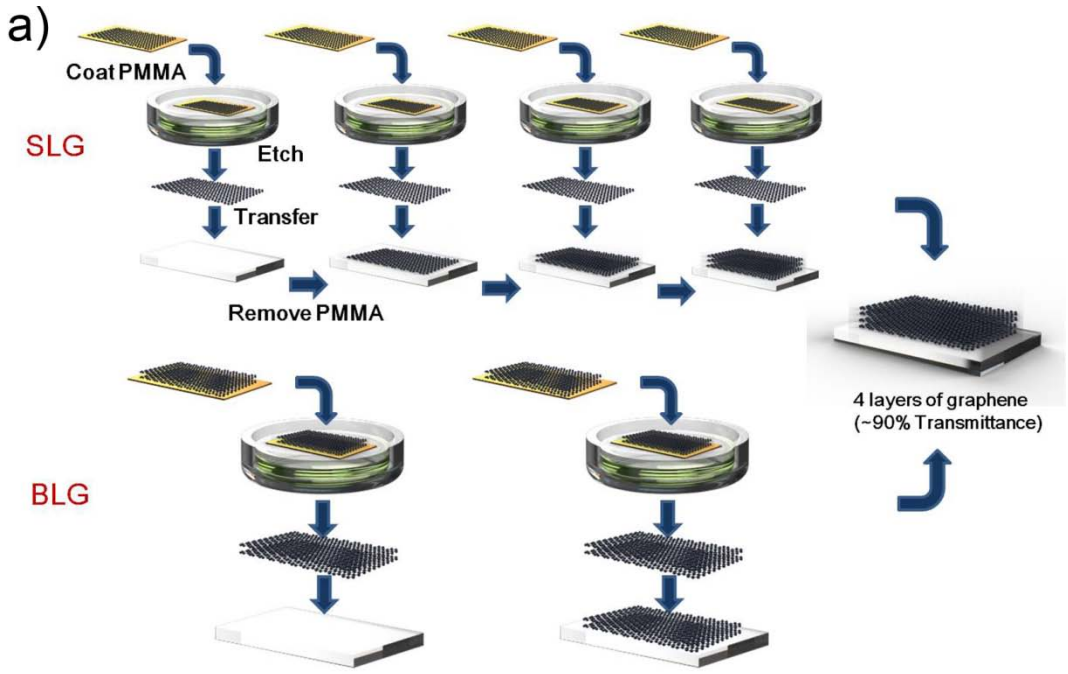

Figure 3.1 Schematic comparison of SLG method and BLG method to synthesize 4 layers of graphene stack to achieve lower sheet resistance.

Figure 3.1 is an illustration showing a stack of four uniform graphene layers prepared by two different methods using either SLG or BLG. Each transfer process consists of multiple steps that include CVD synthesis, coating of graphene with poly methyl methacrylate (PMMA), copper etching, transfer, drying, and removing of the polymer layer. In order to form a stack of four graphene layers, four repeated transfers are needed when using SLG, while only two transfers are required for BLG. It is clear that the BLG method significantly reduces the amount of raw materials and

time required by reducing the number of transfer processes by half.

3.3 Comparison of SLG and BLG stacks

3.3.1 Raman spectroscopy and optical verification

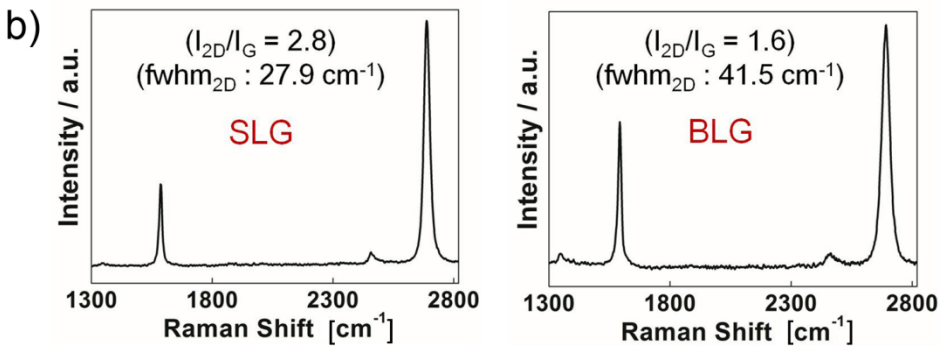

Figure 3.2 Raman spectra taken from CVD grown SLG (left) and BLG (right) samples. The average values of I_{2D}/I_G and $fwhm_{2D}$ from 10 random areas are shown in the plot.

Raman spectra were taken at 10 random spots on the CVD graphene films to verify the number of graphene layers for both SLG and BLG (Figure 3.2). The two most important parameters in determining SLG and BLG from the Raman spectra are the ratio of 2D band (~2691 cm^{-1}) intensity to G band (~1595 cm^{-1}) intensity (I_{2D}/I_G) and the full width at half maximum ($fwhm_{2D}$) value of the 2D band.[67, 68] The mean value of the I_{2D}/I_G ratio is 2.8 for SLG and 1.6 for BLG, while the mean value of the 2D band $fwhm_{2D}$ is 27.9 cm^{-1} for SLG and 41.5 cm^{-1} for BLG. These Raman spectra values are definitive indications of SLG and BLG, respectively.

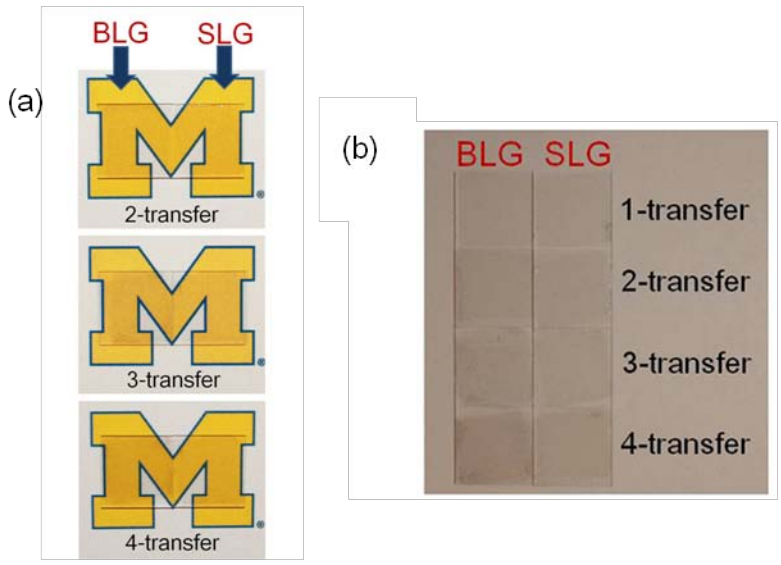

Figure 3.3 Optical comparison of SLG and BLG graphene stacks on glass substrate for 1,2,3,4 transfers with (a) and without(b) background color.

The differences in the opacity of SLG versus BLG stacks become more obvious as the number of transfers increases [Figure 3.3 (a)]. This is because the difference in the number of graphene layers increases from two to four layers as the number of transfers increases from two to four. Figure 3.3 (b) shows the direct optical comparison of both SLG stacks and BLG stacks without the background color.

3.3.2 Transmittance measurement

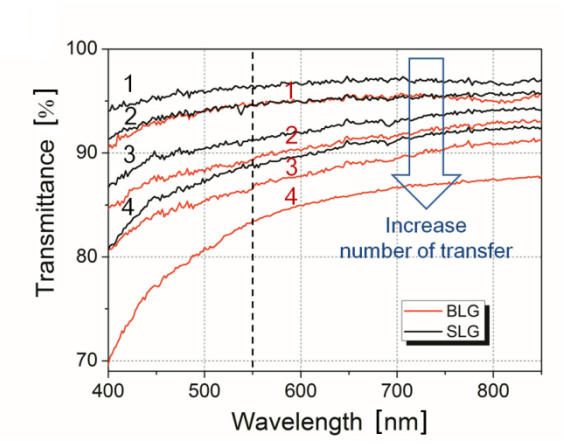

Figure 3.4 Transmittance curve as a function of wavelength for both SLG and BLG stack after 1,2,3,4 transfers respectively. The number near each measurement line indicates the number of transfers.

Furthermore, we measured the transmittance (T) of both SLG stacks and BLG stacks on glass substrates for comparison (Figure 3.4). It is clear that the transmittance of both SLG and BLG stacks drops as the number of transfers increases. For quantitative comparison, the transmittance values of SLG 1-, 2-, 3-, and 4-transfer stacks at 550nm wavelength[4, 48, 49, 101] are measured to be 96.5%, 94.6%, 91.3%, and 89.0%, respectively. The transmittance values of BLG 1-, 2-, 3-, and 4-transfer stacks at 550nm wavelength are 94.7%, 89.3%, 86.6%, and 83.0%, respectively. This result indicates that as expected, BLG's opacity is twice the value of SLG. The transmittance spectrum decreases as it nears the ultraviolet region due to exciton-shifted Van Hove singularity in the graphene density of states.[53] It is also interesting to note that the downward shift in transmittance near the high energy region is more significant as the number of stacked layers increases. This was observed in many other works[4, 48, 49, 66] and it may be due to residue trapped between layers.

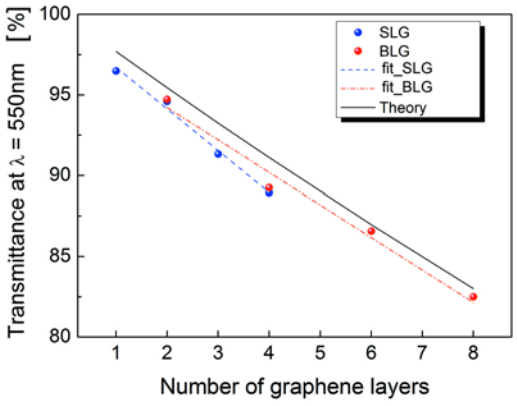

Figure 3.5 Transmittance value at λ=550nm as a function of graphene layers for SLG and BLG stacks and its fits.

Figure 3.5 shows the transmittance values at 550 nm as a function of the total graphene layer numbers, and compares them with the theory. Nair et al have shown that transmittance of graphene is defined by the fine structure constant ≈ 0.0073 and the transmittance of single graphene layer can be expressed as $T \approx -\pi\alpha \approx 97.7\pm0.1\%$.[3] Hence, the transmittance of multiple layers can be expressed as $T^n=(1-\pi\alpha)^n$,where n is the number of layers.[106] The plots confirm that the increases in opacity of both BLG stacks and SLG stacks are close to the theoretical value. The offset of 1%-2% from the theory can be observed and we believe the deviation is likely due to a small amount of polymer residue (e.g. PMMA) that may have been trapped between the sandwiched layers.

3.3.3 Sheet resistance measurement

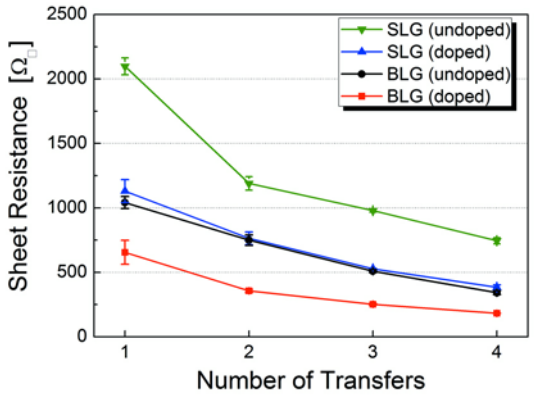

Figure 3.6 Sheet resistance of both undoped and doped SLG,BLG stacks with different number of transfers.

We also characterized the sheet resistance ($R_{\square}$) values for both undoped and nitric acid doped SLG and BLG stacks using four probe method (Figure 3.6). Each data point is taken from 10 different regions on each sample and standard deviation values are expressed with error bars. As the number of transfers increases, the sheet

resistance decreases for both doped and undoped samples. The sheet resistance also drops roughly by a factor of two after layer-by-layer nitric acid doping.

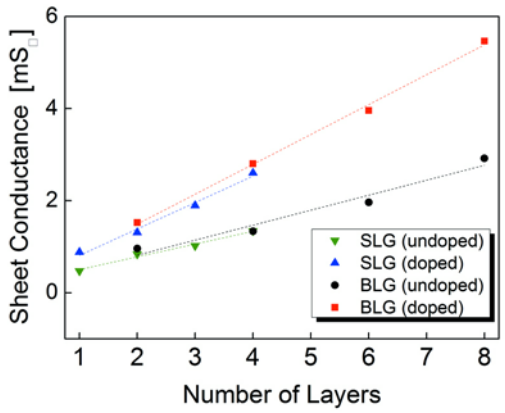

Figure 3.7 Sheet conductance of both undoped and doped SLG,BLG stacks as a function of graphene layer number.

The total resistance of multiple layers of graphene is composed of both in-plane sheet resistance of individual layers and inter-layer resistance between layers.[49] High inter-layer resistance implies resistive interface that will cause most of the current to flow only at the top most layer.[49] To investigate the effect of inter-layer resistance in multi-layer graphene stacks, we plot sheet conductance $G_{\square}$ versus the number of graphene layers in Figure 3.7. Linear fits for undoped samples yield 0.278 $mS_{\square}$/layer for SLG stacks and 0.325 $mS_{\square}$/layer for BLG stacks, which shows a 17% increase for BLG stacks. Linear fit for doped samples yielded a 0.574 $mS_{\square}$/layer for SLG stacks, and 0.649 $mS_{\square}$/layer for BLG stacks which shows a 13% increase for BLG stacks. It is interesting to note that sheet conductance per layer for BLG was found to be slightly higher than that of SLG. The result is unexpected because SLG based conductors have been doped twice as many times compared BLG based

conductors. It is known that a randomly stacked graphene structure will have large interlayer distances that would strongly reduce the electronic dispersion perpendicular to the basal plane compared to a Bernal-like or an ordered stack structure.[107, 108] Since a SLG stack consists of only randomly stacked layers while a BLG stack will retain its ordered layers between each transferred layer, it is possible that BLG was advantageous in maintaining stronger coupling between adjacent layers. In addition, the number of interfaces created from the transfer processes is lower for BLG compared to that of SLG. For example, a four graphene layer stack consists of three transfer interfaces for a SLG stack while only one transfer interface exists in a BLG stack. This may have also helped in lowering the total inter-layer resistance.

3.4 Comparison with other methods

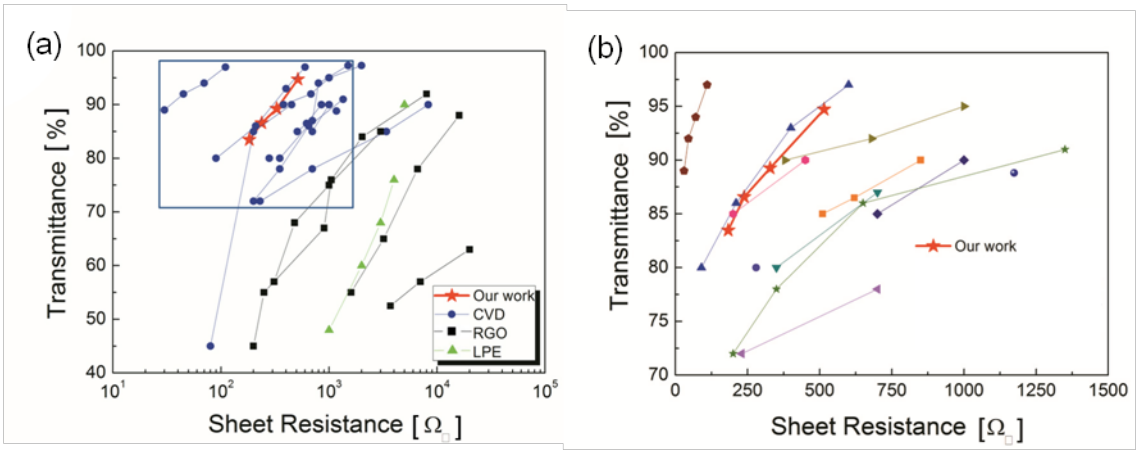

Figure 3.8 (a),(b) Transmittance versus sheet resistance for graphene based transparent conductors grouped according to production methods in log scale (a) and only with CVD method in linear scale (b). Blue rectangle in (a) represents the range of x,y axis for (b).

Recent progress in graphene transparent conductor, in terms of transmittance and sheet resistance, is summarized in Figure 3.8 (a) and Figure 3.8 (b). In Figure 3.8 (a), the reports are categorized according to different production strategies. The

quality of transparent conductor is superior as the characteristics line leans toward the upper left region of the graph, indicating a higher transmittance with lower sheet resistance.[51, 53] In most cases, CVD grown graphene[2, 4, 47, 49, 60, 66, 101-104, 109] has been proven to be superior compared to liquid based synthesis method such as reduction of graphene oxide (RGO)[96-99] and liquid phase exfoliation (LPE)[46, 100] due to its inherent lack of structural defect.[51, 53] Figure 3.8(b) focuses only on CVD methods with nitric acid as the dopant and the sheet resistance is shown with the x-axis as the linear increment. Our results using BLG are comparable or better than other CVD methods using SLG stacks or MLG.

3.5 Sheet resistance change with strain

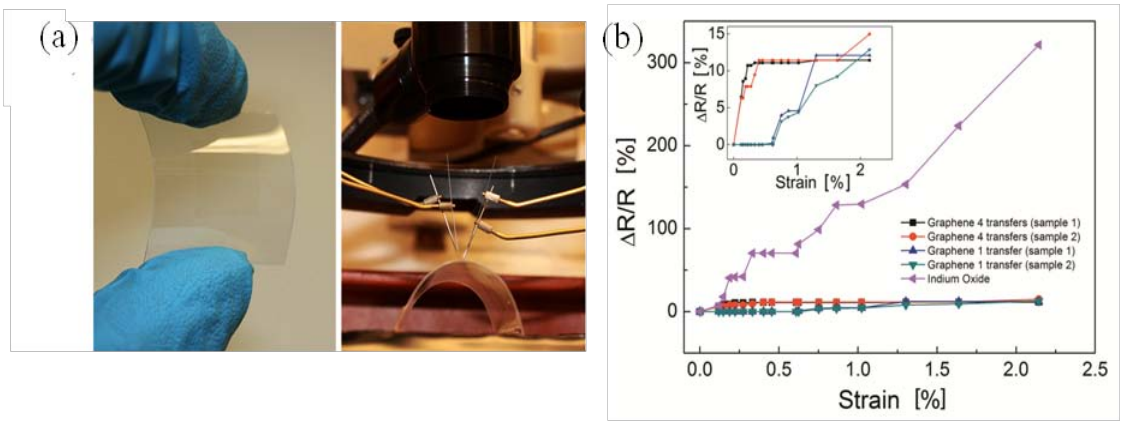

Figure 3.9 (a) Photographs of graphene film on flexed PET substrate(left) and measurement setup of strained substrates (right). (b) Variation in resistance of stacked BLG films and indium oxide films on 200μm thick PET substrate as a function of strain values.

One of the most significant advantages of a graphene based transparent

conductor is its electromechanical stability and mechanical flexibility.[4, 48, 51, 66, 98, 102] To test the sheet resistance of BLG stacks under a mechanical deformation, we transferred BLG films onto 200μm thick polyethylene terephthalate (PET) flexible substrates and patterned them with gold electrodes for four-probe measurement [Figure 3.9(a)]. Two samples of both BLG 1-transfer and BLG 4-transfer were tested in comparison with a commercial Indium oxide on a PET substrate under bending condition. Figure 3.9(b) shows relative change in sheet resistance versus strain due to bending. The radius of curvature is converted to the unit of strain from the equation $\varepsilon=d/2r$, where ε is surface strain, d is substrate thickness, and r is radius of curvature.[110] At 2.14% strain, the sheet resistance of the indium oxide sample increased by 321% while the graphene samples only increased by 10 to 15%. The indium oxide sample shows a drastic change in sheet resistance due to its brittle nature while graphene samples are much more robust against bending. The inset of Figure 3.9(b) shows a more detailed comparison between BLG 1-transfer and BLG 4-transfer samples. It is interesting to note that BLG 4-transfer samples show slight increase in sheet resistance (~10%) at a lower strain than BLG 1-transfer samples. This was not reported in any previous literature. The shear stress that acts between the stacked layers[111] may have disrupted the interface state between graphene layers, and bending the substrate may increase the inter-layer resistance leading to earlier increase in the sheet resistance. Detailed understanding will require further study.

3.6 Uniformity of BLG stack

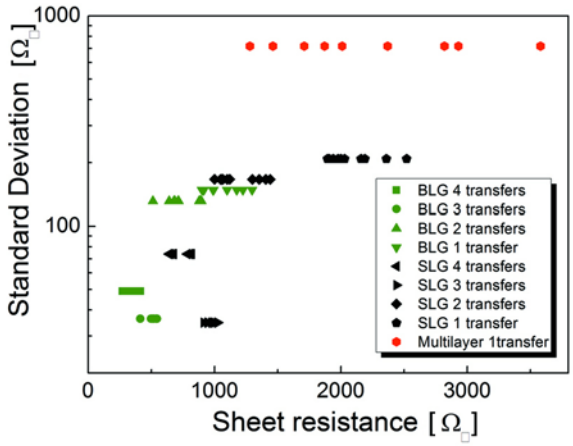

Figure 3.10 Distribution of sheet resistance and its standard deviation values for SLG,BLG stacks and a cvd grown multilayer (MLG) sample. 10 measurements were taken on different areas of each sample.

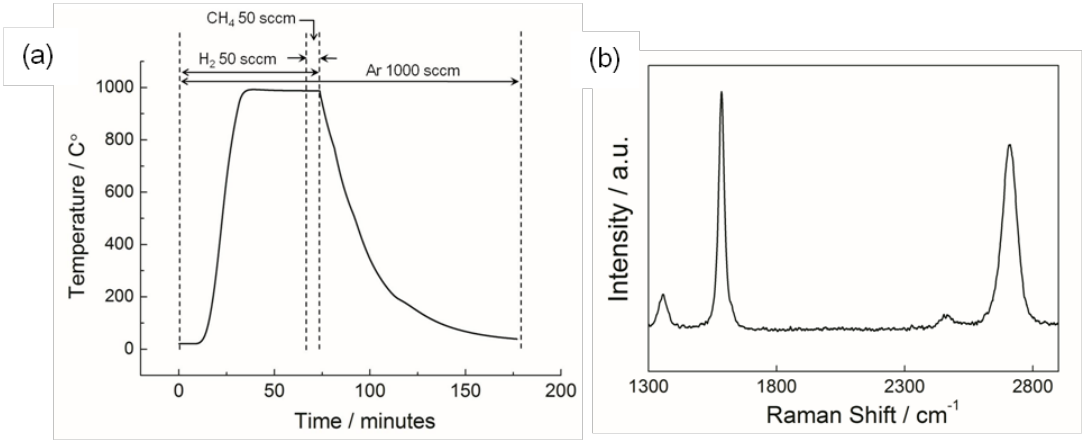

Figure 3.11 (a) Temperature vs. time plot of multilayer graphene growth condition. Pressure is maintained to atmospheric pressure at all time except the initial purge stage. (b) Raman spectroscopy result showing typical multilayer signal.

Last, we evaluate the uniformity of graphene film stacks by taking ten measurement points from different areas of each sample. In Figure 3.10, the sheet resistance values of SLG, BLG stacks, and MLG are plotted with standard deviation

as the vertical axis. The actual values of sheet resistance are plotted for facile observation of the distribution. The MLG sample was grown with the APCVD method (See Appendix A for details) on copper substrate. The time plot of the MLG growth process is shown in Figure 3.11(a). After the transfer process to silicon substrate with thermal oxide, Raman spectroscopy was used to verify the existence of multilayer graphene. For this typical raman spectra shown in Figure 3.11(b), I_{2D}/I_G ratio is 0.78 and the $fwhm_{2D}$ is 63. However for 10 different measurements on random areas, the value of I_{2D}/I_G varied from 0.51 to 1.11 and $fwhm_{2D}$ varied from 47.78 to 68.27. This indicate the non-uniformity of MLG. Going back to Figure 3.10, BLG and SLG samples show similar distribution of sheet resistance and standard deviation for films with the same number of transfers. On the other hand, the MLG sample shows high standard deviation indicating a higher level of non-uniformity in sheet resistance across the sample area. The result agrees with several publications reporting non-uniformity in thickness for MLG.[47, 60, 66, 92, 101, 105] We also acknowledge that the sheet resistance of MLG has strong correlation with surface roughness[105] and there is an effort to produce a smoother (more uniform) multilayer graphene. Nonetheless, BLG stacks stand out with both better uniformity than MLG and drastically reduced fabrication complexity compared to SLG stacks. It is also interesting to note that the standard deviation value becomes lower as the number of stacks increases. This may be attributed to the increased number of graphene layers that can act as channels to negate certain high resistivity areas (e.g. wrinkles or defects) that may reside on one of the layers in the stack.

3.7 Discussion and conclusion

SLG stacks have been proven to be a high quality transparent conductor in many reports.[4, 48, 49] However, most researches overlook the fact that SLG stacks require multiple graphene transfers that results in considerable amount of material waste due to metal wet etching. Furthermore, transferring a large area of graphene is a delicate process that may jeopardize the overall quality of graphene and it is best to minimize the number of transfers. Our BLG method can significantly simplify the process to save cost, time, and reduce waste. Furthermore, the quality and uniformity of BLG stack based transparent conductors have been confirmed to be very high. Although our method of nitric acid doping lowered the sheet resistance by a factor of two, using different dopants and doping methods can lead to further reduction of sheet resistance by a factor of three to five.[49, 106] Utilization of a graphene hybrid structure[50] with BLG can also open up new possibilities for an ultra-low sheet resistance transparent conductor.

Chapter IV

Flexible and Transparent All-Graphene Circuits for Quaternary Digital Modulations

4.1 Introduction

Physically compliant electronics with the capability to conform to a non-planar surface is a field of rapidly growing interest due to the numerous possibilities it offers. Applications ranging from flexible solar cells [54], displays [42], e-papers [112], wearable electronics [43], and biomedical skin-like devices [44, 45] open up new opportunities in the field of electronics. However, nearly all flexible electronic devices require an external power supply and data communication modules, and the lack of portability can severely limit the functionality of various applications. To drive the field forward, three key challenges need to be addressed: a means to generate or store power (e.g., flexible batteries or power generators), a data collecting scheme (e.g., flexible sensors), and a system to transmit and receive the collected data (e.g., flexible wireless communication scheme). Recent advances in the field have led to notable progress in the two areas of flexible power [81, 82] and flexible sensors [44, 45]. However, designing and manufacturing a flexible wireless communication system is still a challenge due to material constraints. Conventional organic polymers [80], amorphous silicon [78], or

oxide-based thin film transistors [113] show only modest performance in this area owing to their limited carrier mobilities.

In this regard, graphene is the ideal material for flexible high speed communication systems due to its unique electronic and physical properties, including high carrier mobility [16], ambipolarity [1, 6], transparency [3], and mechanical flexibility [37]. From its high carrier mobility, a unity gain cut-off frequencies of up to 300 GHz have been achieved with graphene transistors fabricated with exfoliated sample and 155 GHz for transistor fabricate with CVD graphene (Figure 4.1). [25, 84]. Graphene was also used as the channel and the gate material for flexible transistors owing to its mechanical flexibility[39, 41].

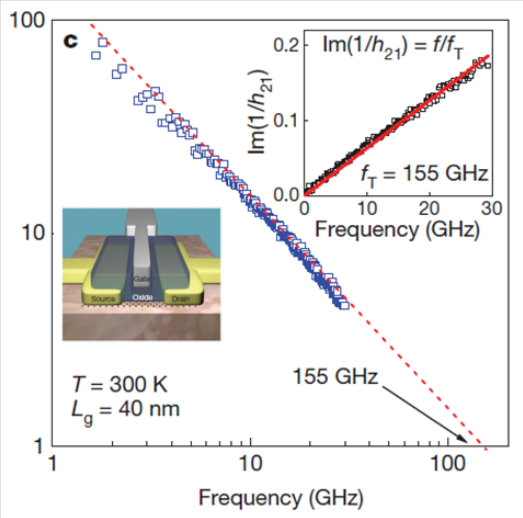

Figure 4.1 Graphene transistor made CVD graphene with a cutoff frequency of 155 GHz. Inset is an illustration of the graphene transistor structure. (adopted from [84])

Several pioneering works on graphene analog electronics led to the demonstration of graphene-based frequency doublers (Figure 4.2) [28-30], mixers [33, 34], and

modulators [28, 35, 36] on rigid substrates. Graphene mixers (Figure 4.3) were shown to effectively suppress odd-order intermodulations by exploiting the symmetric character of graphene transistors [33]. A high-performance mixer fabricated by integration of graphene transistors and passive components on a single silicon carbide wafer was also demonstrated (Figure 4.4) [34]. Several groups demonstrated binary digital modulation schemes [binary phase shift keying(BPSK) and binary frequency shift keying(BFSK)] with graphene transistors on rigid substrates [28, 35, 36]. The finding of graphene based mixers, modulators and high speed transistors all paves the way for an integrated graphene based radio frequency (RF) electronics.

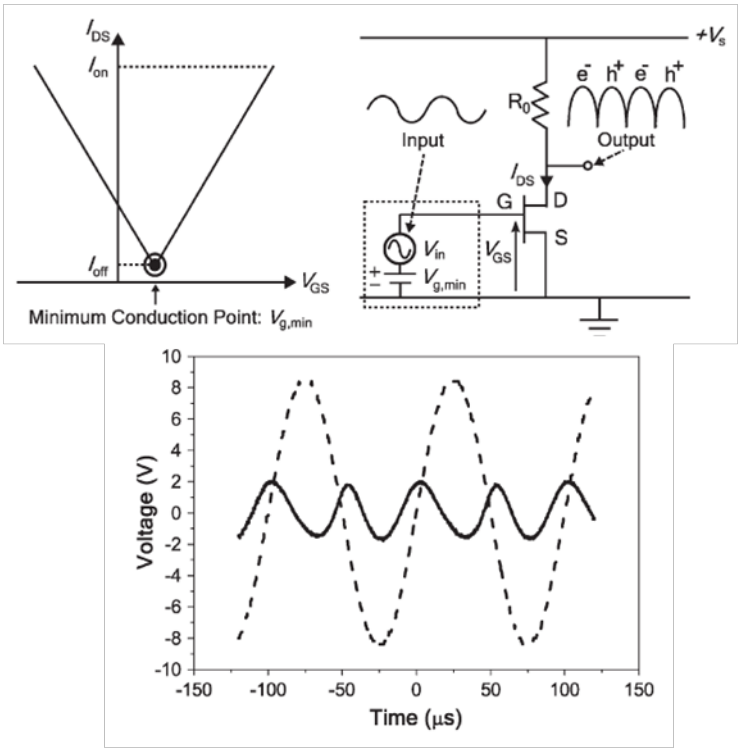

Figure 4.2 Graphene frequency multiplier was demonstrated with just one transistor in reference [30]. This is possible by superimposing an AC signal to a DC voltage which is biased at the charge neutrality point. (adopted from [30])

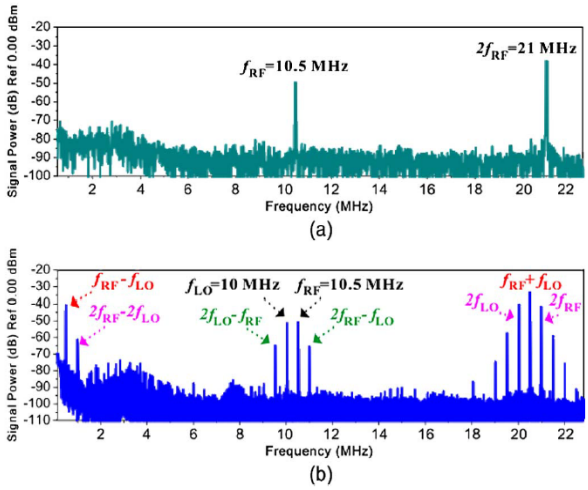

Figure 4.3 Spectrum analysis of a graphene transistor based doubler and a mixer from reference [33]. (a) Output spectrum with single RF input f_{RF} = 10.5 MHz without LO signal. The frequency doubling is observed. The signal power at $2f_{RF}$ = 21 MHz is about 10 dB higher than the signal power at fRF = 10.5 MHz without filtering. (b) Output spectrum with RF input f_{RF} = 10.5 MHz and LO f_{LO} = 10 MHz at equal power. The presence of strong signal power at $f_{RF} - f_{LO}$ = 500 kHz and $f_{RF} + f_{LO}$ = 21.5 MHz demonstrates mixing operations. (adopted from [33])

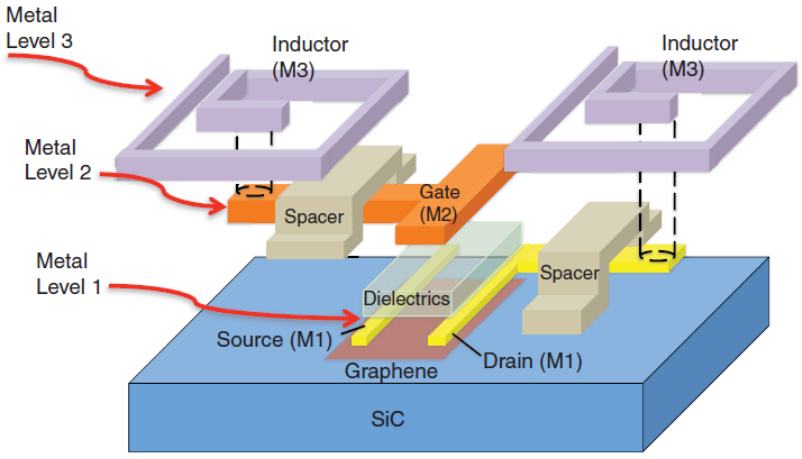

Figure 4.4 Illustration of a graphene mixer circuit integrated with silicon carbide wafer and other passive components. (adopted from [34]). The top-gated graphene transistor and two inductors are connected to the gate and the drain of the Graphene FET. Three metals layers of the graphene IC are represented by M1, M2, and M3. A layer of 120-nm-

thick SiO2 is used as the isolation spacer to electrically separate the inductors (M3) from the underlying interconnects (M1 and M2).

Despite the remarkable progress, all the previous analog circuits have been demonstrated on rigid silicon substrates. Also, the usage of graphene was limited to the transistor itself and was not extended to the whole circuit. In addition, all the previous modulators were demonstrated as binary modulators in which only single bit of data was encoded per symbol. To this end, we demonstrate, an all-graphene flexible and transparent circuit for quaternary digital modulation that can encode two bits of information per symbol in this chapter. The entire circuits are both flexible and transparent with every part of the circuit—including the transistor channels, the interconnects between transistors, the load resistance, and the source/drain/gate electrodes—fabricated with graphene only. The monolithic structure allows unprecedented mechanical flexibility and complete transparency to the circuit which is not possible with either silicon or metal. This is possible due to graphene's unique property of being a zero-bandgap material retaining the property of both metal and semiconductor. Importantly, the ambipolarity of graphene transistors drastically reduces the circuit complexity when compared with silicon-based modulators. No more than a couple of transistors are required for the two quaternary modulation schemes demonstrated, whereas a multitude of transistors are required for conventional modulator circuits [114, 115].

4.2 Constellation diagram of different modulation method

The basic modulation techniques map the information by varying up to three different parameters (amplitude, frequency, and phase) of the carrier wave to represent the data. The most fundamental binary digital modulation techniques that correspond to each of these three parameters are binary amplitude-shift keying (BASK), binary frequency-shift keying (BFSK), and binary phase-shift keying (BPSK). Until now, only two of these binary modulation scheme (BPSK, BFSK) were demonstrated[28, 35, 36]. By adding the BASK scheme, the three basic binary schemes have been completed. Furthermore, by combining two or more binary modulation schemes, it is possible to extend this technique into quaternary digital modulation schemes such as 4-ary amplitude-shift keying (4-ASK) and quadrature phase-shift keying (QPSK) [116]. Specifically, QPSK explores all four quadrants of the constellation, and it is the key building unit for highly efficient modulation techniques that are widely used in today's telecommunication standards such as Code division multiple access (CDMA) and Long term evolution (LTE). The above-mentioned binary and quaternary digital modulation schemes are plotted in a polar constellation with the radial coordinate as the amplitude and the angular coordinate as the phase (Figure 4.5). Importantly, all of them can be realized by using all-graphene circuits on the flexible and transparent platform.

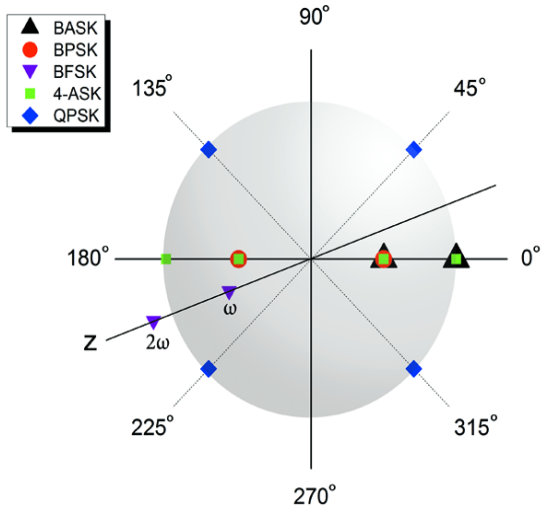

Figure 4.5 A constellation diagram depicting five different digital modulation techniques demonstrated in this work. The z-axis, representing the frequency, is included to show the frequency modulated signals.

4.3 Device fabrication and transmittance

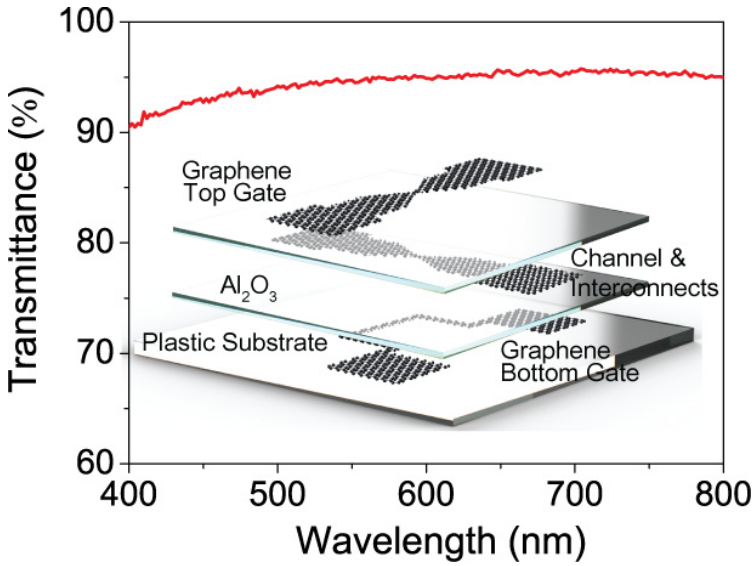

Figure 4.6 A plot of the transmittance as a function of the wavelength and an illustration of the all-graphene transistor structure (inset).

Figure 4.6 shows the transmittance value of the graphene circuit on top of a plastic substrate (polyethylene naphthalate) as a function of the light wavelength (see Appendix B for details of transmittance measurement). Figure 4.6 (inset) shows the structure of the device fabricated on a bendable plastic substrate. The top, middle, and bottom graphene layers form the top gate layer, the channel/interconnect layer, and the bottom gate layer, respectively. Graphene films used in this work are synthesized using chemcal vapor deposition (CVD) method on copper foil [41, 61]. After the CVD synthesis, one side of the copper sample with graphene was coated with 950PMMA A2 (Microchem) resist and cured at 180°C for 1 minutes. The other side of the sample was exposed to O_2 plasma for 30 seconds to remove the graphene on that side. The sample was then left in Ammonium persulfate (Sigma Aldrich, 248614-500G) solution (0.025g/ml) for at least 6 hours to completely dissolve away the copper layer. Then the graphene was transferred to a 100um thick polyethylene naphthalate (PEN) substrate. The PMMA coating is removed with acetone and the substrate is rinsed with deionised water several times. The graphene layer was then patterned with a conventional stepper tool (GCA AS200 AutoStepper) using SPR220 3.0 (Microchem) resist. The process temperature was kept under the glass transition temperature of the plastic substrate (120°C) at all times. After graphene was patterned, 2nm of Al_2O_3 was deposited as a buffer layer using e-beam evaporation. Then 65nm of Al_2O_3 was deposited as the dielectric using atomic layer deposition at 80°C. Another graphene layer was transferred on top of the Al_2O_3 layer to form the channel layer and then it was patterned with lithography again. E-beam evaporation and atomic layer deposition of Al_2O_3 with the same thickness as the bottom dielectric was repeated on top of the channel layer. Final graphene layer was transferred again on top of the

dielectric and patterned with lithography to be used as the top gate. The final device is highly transparent as shown in Figure 4.6 (~95% transmittance at 550nm wavelength) and fully bendable as shown in Figure 4.7. Although three layers of graphene were transferred, the overall transmittance is higher than the expected value of 93% [3] because the majority of the area is covered with only one layer of graphene after patterning and two layers of Al_2O_3. Only the channel area which occupies little space would have all three graphene layers (the bottom gate, the channel, and the top gate) overlapping each other. Under the optical microscope, the graphene devices can be identified by the contrast difference among the top gate, channel, and bottom gate region of the all-graphene transistor (Figure 4.7 inset).

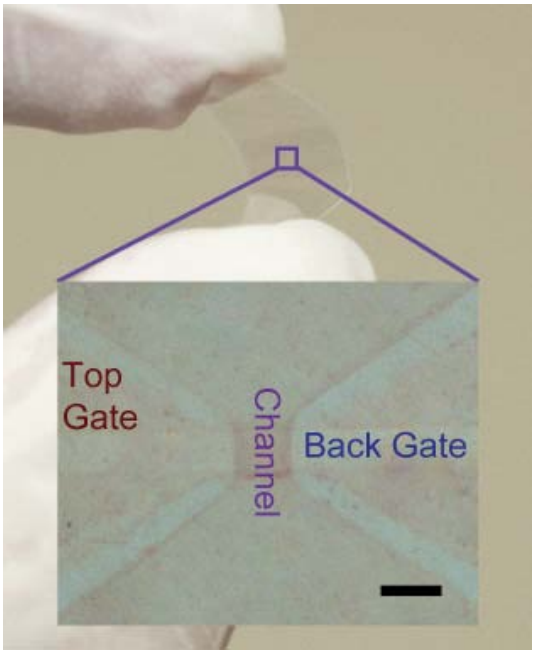

Figure 4.7 a photograph of graphene circuit on a transparent and bendable plastic substrate, and a microscopic image of an all-graphene transistor (inset). The scale bar is 10μm.

The gate response curve was measured for each all-graphene transistors, and the yield was over 98% with 64 out of 65 transistors being fully functional.

4.4 Modulation mechanism and transistor characteristics

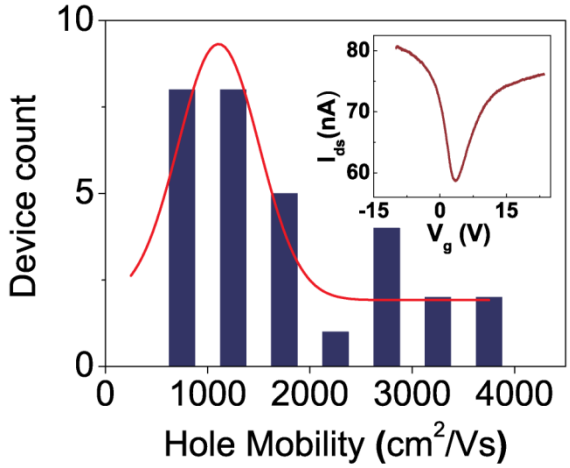

Figure 4.8 A histogram of the hole mobility extracted from 30 transistors and its Gaussian fit (red line). The inset is a plot of the ambipolar current as a function of gate voltage for a typical all-graphene transistor. Voltage across the drain and the source is 10mV.

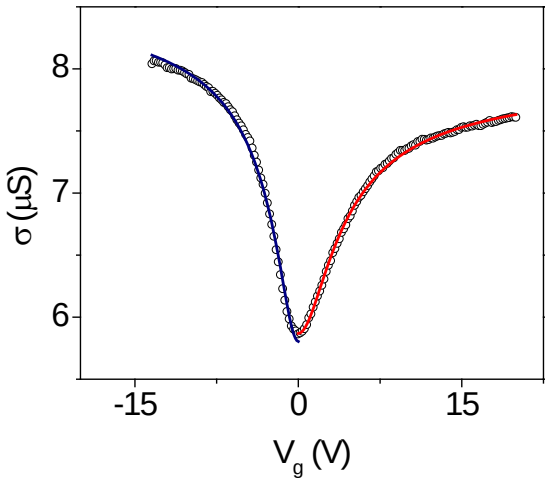

Figure 4.9 Conductance as a function of gate voltage (round symbols) and its fittings (solid line) for a typical device. The blue and the red solid lines correspond to the fittings

for hole and electron mobility respectively. See Appendix C for details on the fitting method.

Figure 4.8 (inset) shows a typical gate response curve from the fabricated all-graphene transistors. Slight shift in the charge neutrality point is observed due to environmental doping. The carrier mobility value can be extracted by fitting the experimental value of source-to-drain conductance over varying gate voltages [117]. The device presented in Figure 4.8 (inset) has a hole carrier mobility value of 3342±26 cm^2/Vs and electron carrier mobility of 2813±11 cm^2/Vs (Figure 4.9). Figure 4.8 is a histogram for hole mobility values extracted from 30 different samples. The average hole mobility is 1771 cm^2/Vs with a standard deviation of 982.6 cm^2/Vs. These mobility values are several orders of magnitude higher than those of alternative materials such as organic polymer [80] and amorphous materials [78] as expected. More importantly, the unique ambipolar gate response of graphene transistors allows simple implementation of previously mentioned binary modulation schemes as illustrated in Figure 4.10. The amplitude, frequency, or phase of the output voltage will be determined by the operating gate bias point of the graphene transistor. For example, amplitude modulation (AM) can be achieved by utilizing the transconductance change over the gate voltage difference. Frequency modulation (FM) is achieved by interchanging the bias point from a region dominated by electron (or hole) carriers to the charge neutrality point. Similarly, phase modulation (PM) is realized by changing the bias point from an electron (or hole) carrier dominated region to the hole (or electron) carrier dominated region.

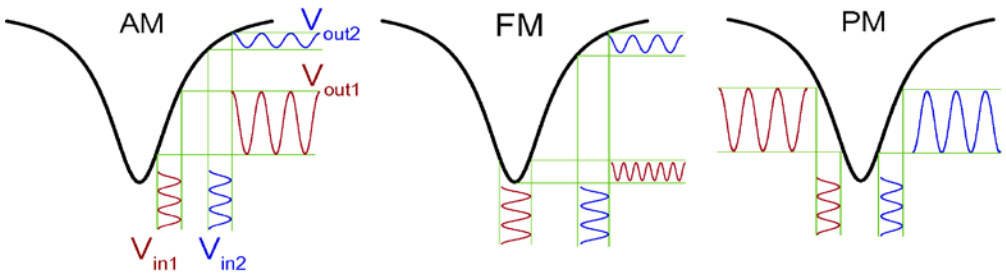

Figure 4.10 Illustrations of amplitude, frequency, and phase modulation of a sinusoidal wave achieved by operating a single ambipolar graphene transistor at different gate biases.

4.5 Binary and quaternary modulation with a single transistor

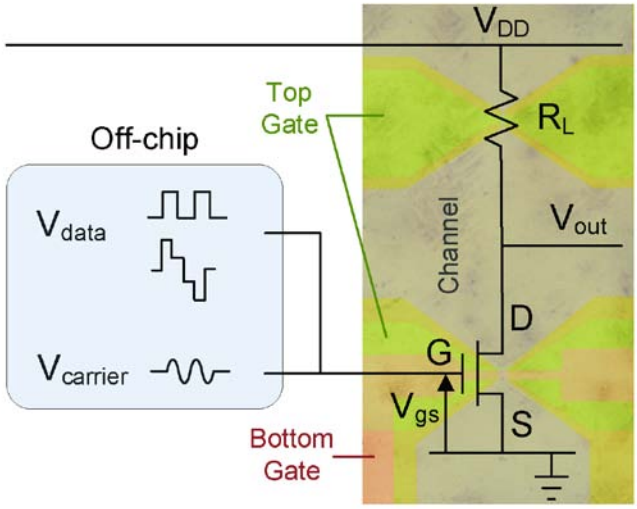

Figure 4.11 A circuit diagram with a false-color image of graphene transistors connected in a common-source configuration. The V_{data} signal is the digital data that is encoded onto the carrier signal $V_{carrier}$. The V_{data} signal is a square wave for all three binary digital modulation schemes and a four level step-like wave for the quaternary amplitude-shift keying modulation scheme.

We next demonstrated the three binary modulation schemes by using the all-graphene circuit. Figure 4.11 shows the circuit diagram overlaid on a false colour image of the device. Green, grey, and red are the respective colours for the top, middle, and bottom graphene layers. A graphene transistor was used for the modulation and another unbiased graphene transistor was used as the load resistor (R_L) for output (V_{out}). The middle graphene layer (grey) serves as the transistor channel, the interconnect between the transistor, the load resistor, and the source/drain electrodes. To achieve digital modulation, the carrier wave ($V_{carrier}$), the data bitstream (V_{data}), and the DC gate bias (V_{gs}) are added together and applied to the top gate (green) of the modulating transistor. Both V_{gs} and V_{data} determine the operating bias point of the transistor and modulate the carrier signal accordingly. The bottom gate (red) delivers additional flexibility to the measurement, and it can also be used to adjust the charge neutrality point (V_{Dirac}) if there is environmental doping.

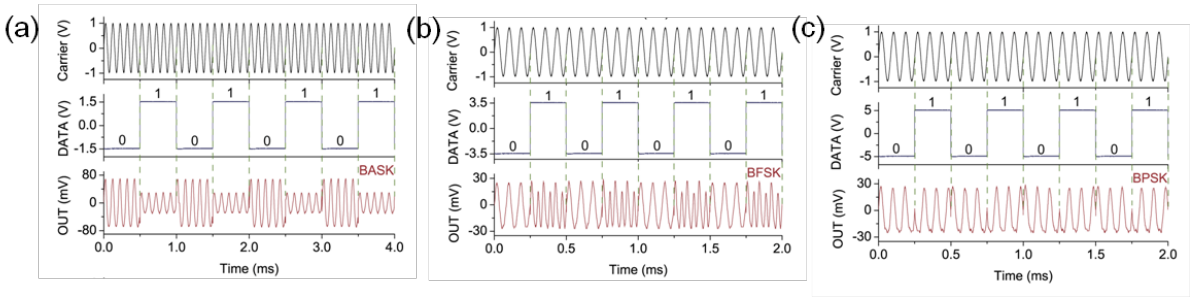

Figure 4.12 (a) Time domain plot of the binary amplitude-shift keying. V_{DD} of 1V was the power supply voltage. (b) Time domain plot of the binary frequency-shift keying at V_{DD} of 1V. (c) Time domain plot of the binary phase-shift keying at V_{DD} of 1V.

Figure 4.12 (a),(b),(c) shows plots of three basic binary modulation schemes demonstrated with the all-graphene circuit. For BASK, the sum of V_{data} and $V_{carrier}$ is superimposed on V_{gs} so that the different transconductances on different bias points will allow $V_{carrier}$ to change in amplitude at the output . Binary information of 0 and 1 is successfully represented by the low and high amplitude of carrier signal, respectively [BASK, Figure 4.12 (a)]. Similarly, we control V_{gs} and V_{data} to adjust the bias point for both BFSK and BPSK. 0 and 1 are successfully differentiated by the doubling in frequencies [BFSK, Figure 4.12 (b)], or by the 180° phase change [BPSK, Figure 4.12 (c)]. To the best of our knowledge, this is the first demonstration of BASK using graphene circuit, while previous works have only shown BPSK and BFSK[28, 35]. By adding the BASK scheme, the three basic binary schemes have been completed using flexible graphene circuits. We note that the output voltage has a DC component for 0 and 1 because the transistor is operating at different bias points on the gate response curve. The DC component can be filtered out using a high pass filter and it has been removed for clarity in this work.

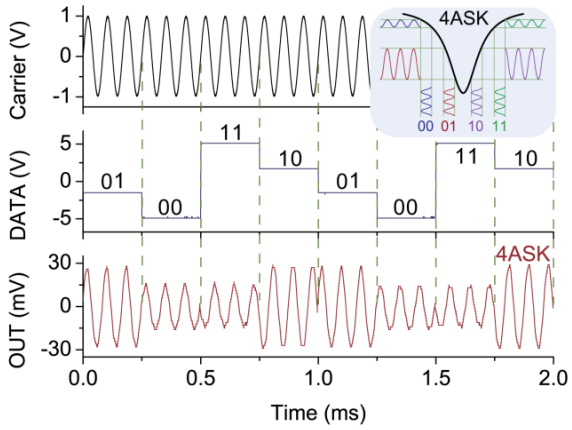

Figure 4.13 A time domain plot of the quaternary amplitude-shift keying modulation of carrier signal. The inset is an illustration describing the four operating gate bias points used in 4-ASK. V_{DD} is 1V.

Furthermore, by combining BASK and BPSK, a 4-ary amplitude shift keying (4-ASK) was demonstrated as shown in Figure 4.13. The inset of Figure 4.13 illustrates the four bias points used in the 4-ASK scheme that correspond to 00, 01, 10, and 11. Both the phase and the amplitude information are used to distinguish the quaternary signal that is encoded in the carrier wave. Output of 00, 01, 10, and 11 are represented by “low amplitude, 270° phase”, “high amplitude, 270° phase”, “high amplitude, 90° phase”, and “low amplitude, 90° phase” in the carrier wave, respectively. 4-ASK is a quaternary digital modulation scheme that uses four points in the constellation diagram (Figure 4.5) and doubles the data transfer rate compared to a binary scheme. Importantly, this is the first demonstration of quaternary modulation with just one transistor (excluding the transistor that is used as a resistor), which is not possible in conventional silicon based modulators.

4.6 Quadrature phase-shift keying with two graphene transistors

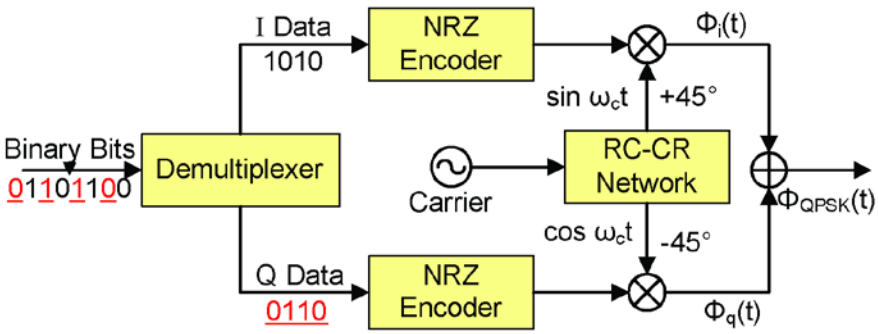

Figure 4.14 A conceptual diagram of a conventional quadrature phase-shift keying transmitter structure. NRZ encoder is a non-return-to-zero encoder where 1 is represented by a positive voltage state and 0 is represented by a negative voltage state. RC-CR network is the resistance-capacitance–capacitance-resistance phase shift network which generates two orthogonal wave functions with 90° phase difference.

A more fundamental quaternary modulation scheme is QPSK, which explores all four quadrants of the constellation. Figure 4.14 shows a typical QPSK transmitter structure used in modern digital communication. A binary data stream is demultiplexed into the in-phase component (I) and the quadrature-phase component (Q). I and Q components are encoded onto two orthogonal basis functions, such as a sine wave and a cosine wave, respectively, before they are summed to generate a QPSK modulated signal.

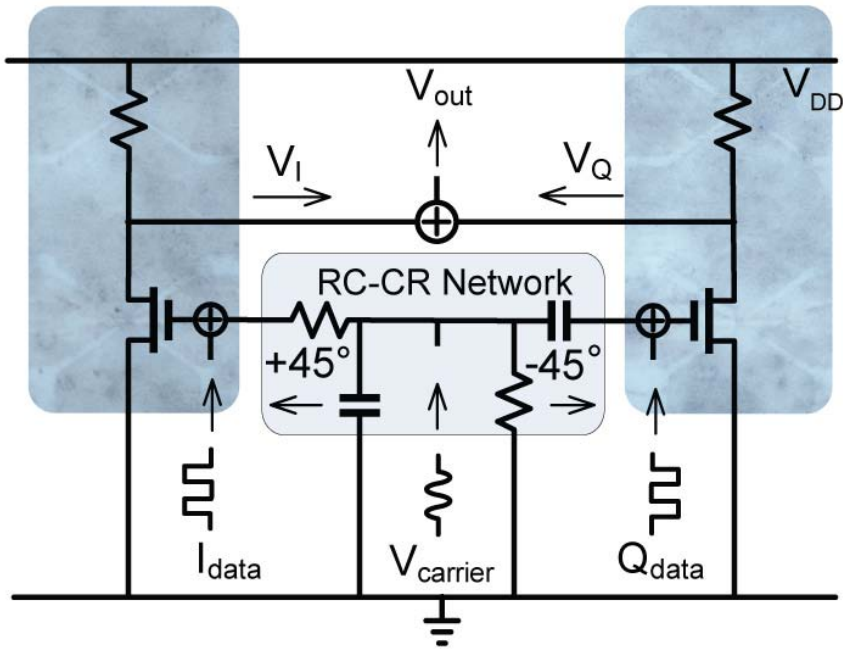

Figure 4.15 , An all-graphene circuit diagram of the quadrature phase-shift keying system using two transistors. The actual microscopic image of the all-graphene circuit under a blue filter is shown. The transistor dimension is 10μm × 10μm.

Here, we used just two transistors with similar gate response in the all-graphene circuit to demonstrate the QPSK modulation (Figure 4.15). Actual microscope images under a blue filter is shown in the figure. A sinusoidal wave from the function generator was connected to a simple off-chip resistance-capacitance – capacitance-resistance (RC-CR) phase shift network to generate two orthogonal wave functions with 90° phase difference. The sinusoidal input is shifted by +45° in the CR branch and by -45° in the RC branch [118]. Then each of these signals is summed internally by the function generators with two square waves (I_{data} and Q_{data}) and fed to the gates of each transistor (A detailed measurement setup is shown in Figure 4.16).

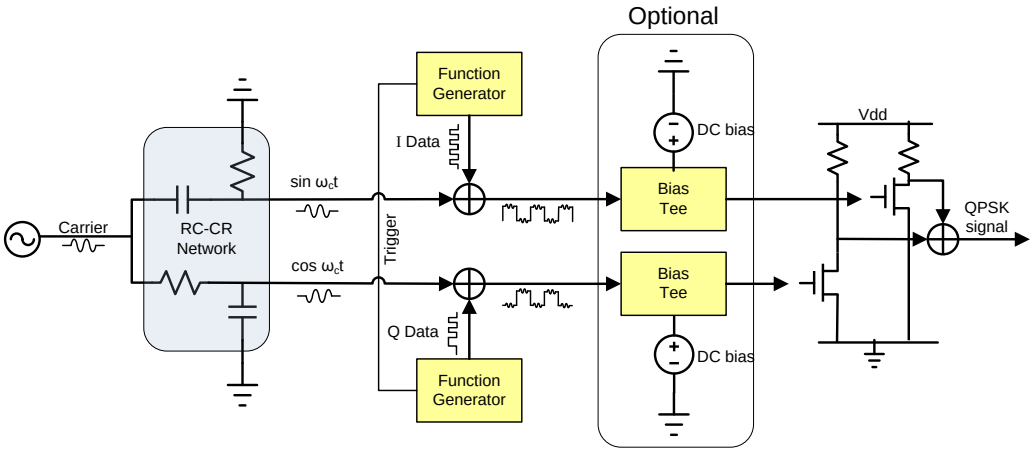

Figure 4.16 Detailed measurement setup for quadrature phase shift-keying signal generation. A sinusoidal carrier signal is generated from a signal generator and fed to an RC-CR phase shift network. The phase of the sinusoidal signal is shifted by +45 and -45 when it passes through RC and CR structure respectively. The resulting two orthogonal functions (sin $\omega_c t$ and cos $\omega_c t$) with a phase difference of 90° are summed internally in two different function generators with its respective digital data signal shown as the square wave. The two function generators are phase matched using the trigger function. If the charge neutrality point (V_{Dirac}) is not centered at zero voltage due to environmental doping, the signal can be connected with a bias tee with a DC bias and then fed to the gate of each transistor. When the DC bias is approximately equal to V_{Dirac}, the phase modulation of each transistors will be symmetric. If the Dirac point at 0 voltage, the signals can be directly inserted to the gates of each transistors without a bias tee The two generated signals which are the final quadrature phase-shift keying signals were added internally and measured with an oscilloscope.

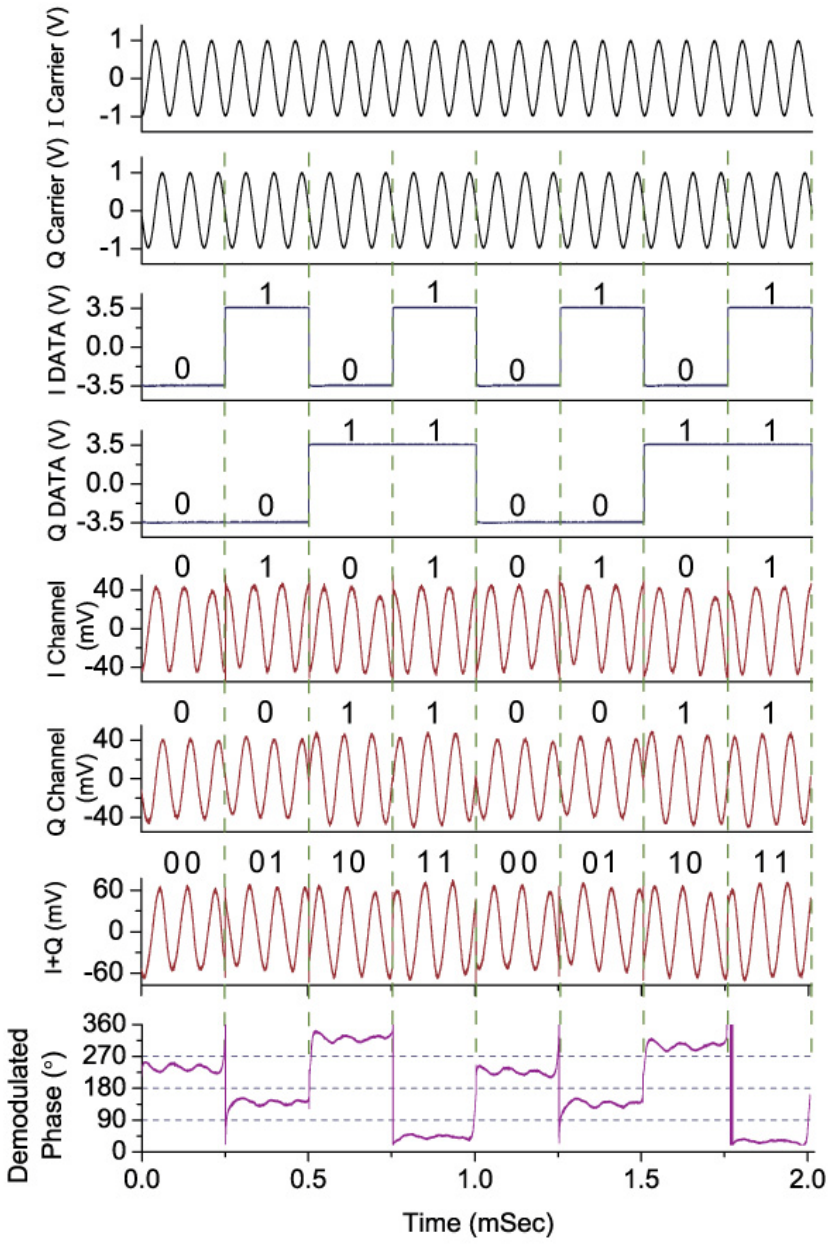

Figure 4.17 Time domain plots of the input and output signals demonstrating quadrature phase-shift keying modulation scheme. V_{DD} of 7V was the power supply voltage.

The outputs (V_I and V_Q) are then summed to generate the final QPSK modulated signals. These signal components are plotted in Figure 4.17. The $I_{carrier}$ and the $Q_{carrier}$ are

the orthogonal carrier signals. The data bitstream with 00, 01, 10, 11 is represented by the in-phase component I_{data} and the quadrature-phase component Q_{data} as shown in the plot. Modulating $I_{carrier}$ with I_{data} results in phase changes in $I_{channel}$ and the same applies to $Q_{carrier}$, Q_{data}, and $Q_{channel}$. Data bit 0 and 1 in I_{data} corresponds to phase of 180° and 0 ° in $I_{channel}$. Similarly, Data bit 0 and 1 of Q_{data} corresponds to phase of 90° and 270 ° in $Q_{channel}$. The sum of $I_{channel}$ and $Q_{channel}$ is the final output signal ($I+Q$) which has distinct phase shifts of 225°, 135°, 315°, and 45°, each corresponding to binary data of 00, 01, 10, and 11.

To validate the result, the instantaneous phase information was extracted from the final output signal ($I+Q$) and plotted as demodulated phase (Figure 4.17, bottom panel). This mathematical form of demodulation was achieved by extracting the phase information from the Hilbert transform of the output signal ($I+Q$). The plot of the demodulated phase indicates a clear distinction of phase shift between different QPSK signals. The carrier to noise ratio (C/N) which is the ratio of signal power to the white-noise power was found to be 21.1 dB from the frequency spectrum using a conventional signal analysis program (see Appendix D for details). The corresponding bit error rate (BER) assuming additive white Gaussian noise (AWGN) channel is much lower than the performance threshold BER of 10^{-4}, above which the radio link is considered to be in outage[119]. This confirms the robustness and accuracy of the graphene based QPSK modulator. From the output signal (($I+Q$) and the input carrier signals, the gain of the QPSK modulator is calculated to be around 0.06, one of largest ever measured with graphene modulators. The gains of our all-graphene binary and quaternary modulators are comparable or larger than all the previous modulator works as shown in Table 4-1 .

Although these gain values are less than 1, in a modern transmitter structure, the amplification of the signal is primarily accomplished by an audio amplifier or a power amplifier, and a gain is not an essential component of the modulator.

Publication	Gain	Modulation	Comments
Wang et.al.[29]	0.005	10 kHz	Frequency doubling
Yang et. al. [28]	~0.01	4-10 kHz	BPSK, BFSK
Hsu et. al.[36]	0.005	500 Hz	BPSK
Harada et.al [35]	~0.05	30 kHz	BPSK
Sordan et.al. [120]	<0.025	100 Hz	Boolean logic
This work : binary modulation	**0.03~0.07.**	**10 kHz**	**BPSK, BFSK, BASK. The first demonstration of BASK.**
This work : quaternary modulation	**4ASK : 0.03** **QPSK : 0.06**	**10 kHz**	**4-ASK, QPSK. The first demonstration of quaternary modulations.**

Table 4-1 Signal gain comparison of past works and this work.

4.7 All-graphene modulator circuits under mechanical strain

Last, we examine the performance of all-graphene circuit under mechanical strain (Figure 4.18). Frequency modulation (i.e., frequency doubling, Figure 4.19) was first evaluated at different bending radii. To quantify the comparison, fast Fourier transform (FFT) was applied to the doubled output voltage, yielding peaks at ω and 2ω corresponding to the original frequency and the doubled frequency (Figure 4.20). The ratios of these two peaks, which indicate the spectral purity of the frequency doubling,

are plotted as a function of the bending radii in Figure 4.18 (a). Very little change is observed under different bending radii, indicating the robustness in circuit performance under mechanical strain. In addition, various binary digital modulation schemes are also successfully demonstrated at maximum strain level of 2.7% (bending radius of 5.5mm) under the test set-up Figure 4.18 (b). The results further confirm the transparent all-graphene modulators are fully functional under highly strained conditions.

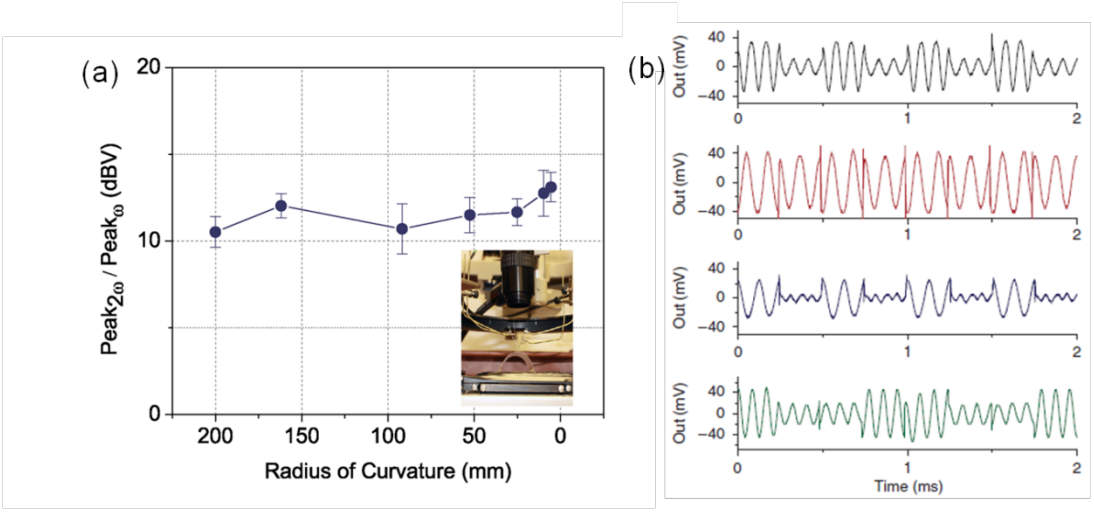

Figure 4.18 Flexible and transparent all-graphene digital modulator circuits under mechanical strain. (a) The plot of the signal amplitude ratio of the original and the doubled frequency as a function of the curvature radius for a graphene frequency doubler. The inset is a photograph of the measurement setup. (b) Time domain plots of binary amplitude-shift keying (black), binary phase-shift keying (red), binary frequency-shift keying (blue), and quaternary amplitude-shift keying (green) schemes achieved with mechanically strained all-graphene circuits at 5.5mm radius of curvature (2.7% strain).

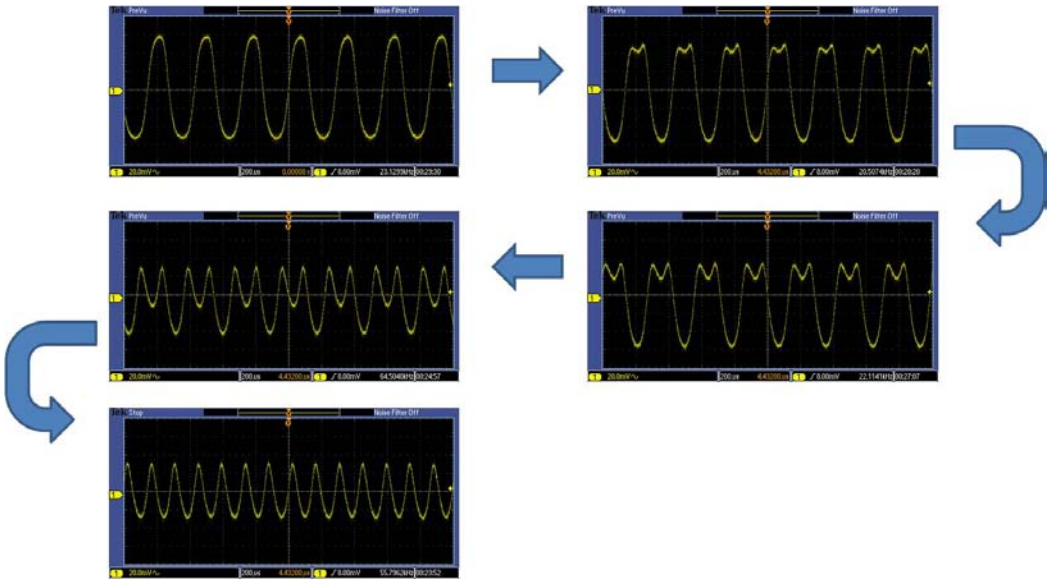

Figure 4.19 Oscillscope images of the frequency doubling as a result of gradual gate bias shift. As the gate DC bias point shifts from the negative side (hole carrier dominated) to the Dirac point, frequency doubling due to ambipolar characteristics of graphene transistor can be observed. If the DC bias point is not exactly at the Dirac point, the output signal will show asymmetry.

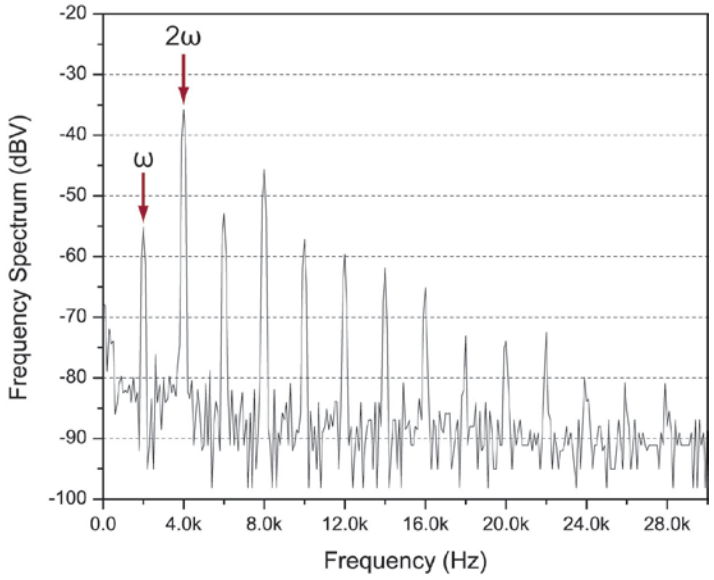

Figure 4.20 Fast Fourier Transform (FFT) of a typical frequency doubled signal. A typical Fast Fourier Transform (FFT) of the doubled signal from a mechanically strained graphene transistor is shown. The radius of curvature was 5.5mm for this plot. The doubled frequency (2ω) term and the original frequency (ω) term has a signal amplitude

difference of 20 dBV. The higher order terms also shows significantly weaker signal strength compared to the doubled frequency. The higher order terms can be filtered out if necessary.

4.8 Discussion and conclusion

The operating principle and technique of flexible and transparent all-graphene modulators described here can be applied to widely used network technologies in today's multimedia and communication devices by either introducing pulse shaping with signal delays or coupling aforementioned modulation schemes [116]. Several recent works also demonstrated voltage gain in graphene transistors showing possibility of graphene based amplifiers and RF front-ends in radiofrequency communication system [31, 32, 121]. The combination of an efficient modulation method with a reliable RF front-end will be the key factor in determining the practicality of mobile and flexible apparatus. In conjunction with conventional thin film technology and high resolution lithography, all-graphene modulator circuit will play a pivotal role in realizing a high speed, mechanically compliant, and transparent electronic system in the near future.

Chapter V

Bipolar Junction Transistor Based on Graphene Heterostructure

5.1 Introduction

The development of graphene-based electronics led to significant progress in several fields, particularly in the area of high-frequency transistors[83, 84], analog electronics[28, 29, 31-34], and mechanically compliant device technologies[39-41, 122]. However, with all its remarkable traits, the absence of an energy gap in graphene inhibits any realistic integration of graphene with current platforms of electronic circuits. The large leakage current near the charge neutrality point precludes any application of graphene transistors in the field of digital electronics. Other solutions of opening up a bandgap in graphene by utilizing nanoribbons[59, 64, 123], bilayer graphene[61, 72, 73, 76], or chemical functionalization[124] either degrades the electronic performance of graphene or does not contribute to a large enough bandgap.

The ambipolarity of graphene is also known to hamper current saturation in the transistor output characteristics[26]. The weak current saturation behavior has an adverse effect on its intrinsic gain and in order to achieve a noticeable gain in graphene amplifiers[26], special structures, such as a complementary structure[31, 35] or an

embedded gate structure[32], are required. Even with these unconventional designs, the highest low frequency gain achieved was only A_v=3.7 (11.4 dB)[31].

Hence, this need has stimulated research on graphene transistors with strong on/off switching capabilities and high gain. One promising route to achieve this is by forming a graphene heterostructure with a second material, either an insulator or a semiconductor. Britnell et al.[125] demonstrated a field-effect transistor based on quantum tunnelling from a graphene electrode through atomically thin dichalcogenides (such as boron nitride or molybdenum disulfide) to another graphene electrode. Figure 5.1 illustrates the band structure of the graphene field-effect tunneling transistor and its working mechanism.

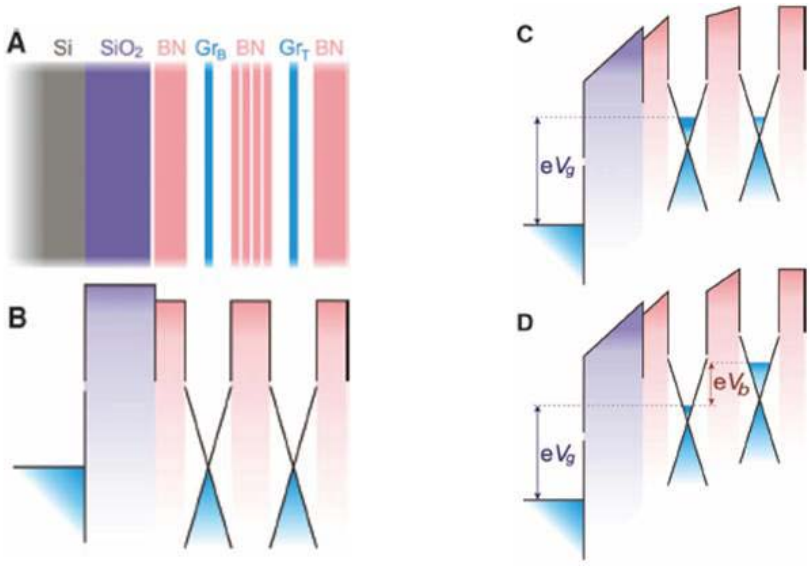

Figure 5.1 Graphene field-effect tunneling transistor based on atomically thin dichalcogenides between two graphene electrodes. (a) Schematic structure. BN is boron nitride and Gr is graphene. (b) The corresponding band structure with no gate voltage applied. The cones illustrate graphene's Dirac-like spectrum and, the boron nitride between two graphene electrodes act as the tunnel barrier for electrons. (c) The same band structure for a finite gate voltage V_g and zero bias V_b. (d) Both V_g and V_b are finite. (adopted from [125])

When a gate voltage Vg is applied between the Si substrate and the bottom graphene layer (GrB), the carrier concentrations n_B and n_T in both the bottom and the top electrodes increases because of the weak screening by monolayer graphene[6], as shown schematically in Figure 5.1(c). The increase of the Fermi energy E_F in the graphene layers can lead to a reduction in barrier height for electrons tunneling because the electric field penetrating through GrB alters the shape of the barrier[126]. Moreover, the increase in the tunneling density of state (DOS) as E_F moves away from the charge neutrality point[6] leads to an increase in the tunnel current I. The use of graphene in this device architecture is critical because this exploits graphene's low DOS, which for a given change in Vg leads to a much greater increase in E_F as compared with a conventional semiconductor with parabolic dispersion[127, 128]. This difference translates into much greater changes of both the barrier height and the tunneling DOS. This work demonstrated an on/off ratio of $\approx$ 50 for a boron nitride device and $\approx 10^4$ for a molybdenum disulfide device[125].

Yang et al.[129] also demonstrated an on/off ratio as high as 10^5 with a vertical graphene/silicon structure. In this work, instead of controlling the tunnelling probability, the height of the Schottky barrier formed between the graphene and the bulk silicon was varied by modulating the work function of graphene to adjust the carrier flow.

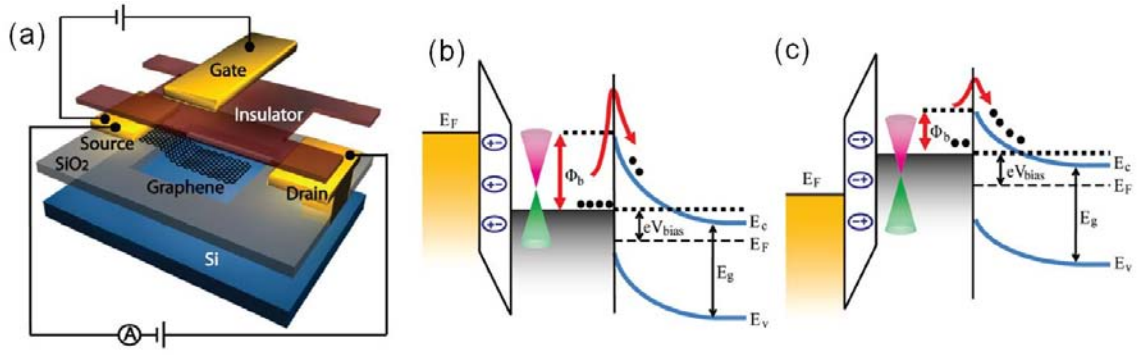

Figure 5.2 Tunable graphene-silicon junction device (a) a schematic diagram of the device (b) Schematic band diagrams of graphene-silicon Schottky barrier with the electric field effect generated by the gate on the top of graphene. Applying negative voltage on the gate induces holes in graphene, increasing its work function and increasing the Schottky barrier height. As a result, the reverse current across the Schottky barrier decreases. (c) Positive gate voltage decreases the Schottky barrier height and increases reversed current. (adopted from [129])

As shown in Figure 5.2, the gate electrical field will electrostatically modulate the graphene's work function through the top gate dielectric above the graphene, which results in a variation on the Schottky barrier height ϕ_B. Because the injection of the majority carriers from graphene to silicon is determined by the Schottky barrier height, the top gate then directly controls the magnitude of the current across the source and the drain.

Changing the work function of a material with an electrical field is a unique feature of graphene[125, 130-133], and it is usually not observed in any bulk material, whether it is a semiconductor or a metal. This is possible because graphene is an atomically thin two-dimensional material with low DOS whose carrier concentration can be modulated with an electrical field. Yu et al. [131], demonstrated that by applying scanning Kelvin probe microscope techniques to back-gated graphene devices, the work function can be

controlled by electrical-field-induced modulation of carrier concentration. The scanning Kelvin probe microscopy was used to map the surface potential variation of a sample surface. The change of work function is due to the Fermi level shift resulting from the electrical field induced carrier doping[129].

Thus far, all the demonstrated devices[125, 129, 132] utilizing variable work function were field-effect transistors (FETs) with electrical fields applied across a dielectric layer. However, the variable work function of graphene can also be exploited in other types of transistors.

Looking back on the history of transistors, FETs were not the first to be invented. The early transistors were based on the junction characteristics[134], not on the gate-induced electrical field. In fact, the very first transistor used a metal-semiconductor (gold-germanium) junction to achieve gain in a transistor. This transistor is called a "point contact transistor" (Figure 5.3 (a)). A few years later, the transistor structure was improved and was later called a "surface barrier transistor"[135].

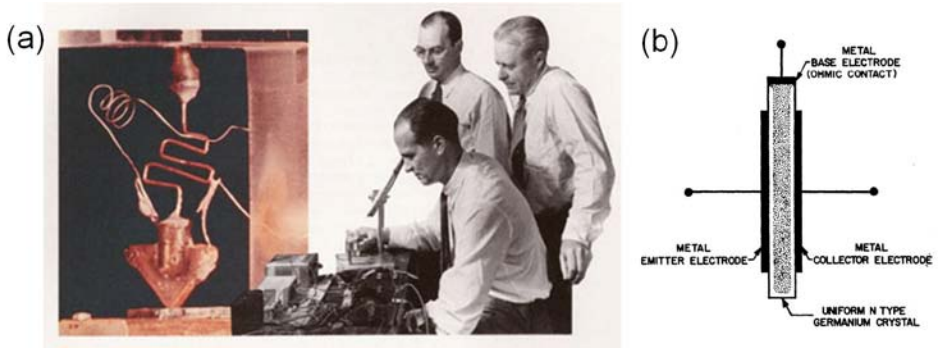

Figure 5.3 (a) The very first transistor ("point contact transistor") invented by William Shockley, John Bardeen, and Walter Brattain in 1947. (b) The structure of the surface barrier transistor (adopted from [135])

The name "surface barrier transistor" is derived from the fact that the interfaces of the transistor, which perform the functions of emission and collection of the carriers, are

located at the surface of the semiconductor crystal[135]. Just like a bipolar transistor, the forward current of the surface barrier transistor is made up of both the minority and the majority carrier in the semiconductor[135]. For transistor purpose, it is desirable to increase the minority carrier current to increase gain. However, it is known that the dominant carriers across a typical Schottky junction during the forward bias condition are majority carriers. This is because when a Schottky junction is forward biased, the potential barrier seen by the majority carrier is very low, and the majority carrier injection from the semiconductor to the metal leads to a large forward bias current before the recombination and the diffusion (minority carrier injection from the metal side) becomes important[136]. This may be the reason the early point contact transistors and the surface barrier transistor suffered from low gain (~ 2 to 3 at most [136]). The early surface barrier transistor also suffered from high reverse current, low temperature tolerance, poor manufacturability, and rapid performance deterioration upon exposure to the environment. This is mostly due to the innate instability of metal (e.g. ion migration, thermal instability, punch through, low reverse bias tolerance) and the difficulty in manufacturing such a thin semiconductor to make a heterostructure[134]. Eventually these metal-semiconductors became obsolete as the diffusion-based doping and the surface passivation of silicon for encapsulation and insulation became common practices. The improvement of diffusion and oxidation technology eventually led to the birth of the modern bipolar junction transistors (BJT). The bipolar junction transistor is analogous to the surface barrier transistor (SBT) in the way that both utilize the minority carrier flow. The difference is that SBT consists of metal-based Schottky junctions while BJT is composed of p-n junctions.

5.2 Motivation for graphene based bipolar transistor

It is important to note that the Schottky junction-based SBTs did not become obsolete because of their speed or energy efficiency. In fact, a very rapid transient response is a distinctive characteristic of a Schottky diode. In pn junction devices the excess minority carriers stored in the quasineutral regions of the semiconductor must be removed before the device can be switched from the forward bias on state to the reverse bias off state[136]. In a Schottky diode, there is very little minority carrier injection and storage within the semiconductor because the diffusion component of the current is typically negligible. The reverse recovery time of a commercial Schottky diode can be only a few nanoseconds. This is the reason Schottky diodes are used in Schottky diode clamped BJT to improve BJT turn-off transient response[136]. Furthermore, Schottky diodes have lower forward voltage drop compared to p-n diodes, offering higher switching speed with better power efficiency[137]. Because of these characteristics, Schottky junctions are integral components of many of today's high-frequency, high-power devices such as metal semiconductor field-effect transistors (MESFETs) and high electron mobility transistors (HEMTs)[137].

In this work, we will demonstrate the first bipolar transistor based on graphene-semiconductor heterojunction. We term it a bipolar transistor because both the majority carriers and the minority carriers are responsible for the current flow. This is a new type of graphene transistor utilizing the mechanism of both the bipolar junction transistor and the surface barrier transistor. This is possible because graphene is a zero-bandgap semiconductor that has the properties of both metal and semiconductor. The junction

formed by graphene and the semiconductor cannot be described by the traditional Schottky junction model with an invariant Fermi level of metal. On the contrary, the graphene-semiconductor junction is fundamentally different from a traditional Schottky junction in two ways: First, the Fermi level of graphene can be shifted by either an external electrical field[125, 129, 132] or charge carrier transport[133, 138], and this capability subsequently affects the barrier height. Second, when the Fermi level is aligned to the Dirac point of a neutral single-layer graphene, the DOS vanishes at this point and the DOS is very low in the vicinity[7]. Because of graphene's low DOS, the E_F change due to given external E-fields is much greater than that of a conventional semiconductor with parabolic band structure[125]. This behavior is also quite different from that of conventional metal in which charge transport or E-field can barely vary the Fermi level because of the high density of states at the Fermi energy in metal.

Exploiting this characteristic of graphene, it is possible to design bipolar junction devices instead of previously demonstrated field-effect devices. Compared to MOSFETs, BJTs are known to have higher base leakage current and lower input impedance. MOSFETs are also generally less expensive compared to BJTs in terms of their used area on a chip. However, BJTs in general have superior frequency response because they are not limited by the large input capacitance of FETs [136]. It is possible to fabricate extremely fast transistors (e.g. Heterojunction Bipolar Transistors, HBT) utilizing heterostructures. Moreover, bipolar junction devices have exponential transfer characteristics compared to the quadratic characteristics of FETs. As a result, BJTs inherently have higher transconductance (g_m) compared to those of FETs with similar bias current because the small signal g_m of an FET is inversely proportional to gate

overdrive (V_{gs}-V_t) while for a BJT, it is inversely proportional to the thermal voltage (V_T). Reducing the gate overdrive excessively to increase the g_m of a MOSFET will inevitably cause the MOSFET to enter subthreshold regime, reducing its performance[137]. Moreover, some bipolar devices (e.g. IGBT) can sustain higher voltage and current compared to silicon MOSFETs and hence are better for high power applications. Although MOSFETs dominate today's electronic industry, bipolar devices are still a vital component in many specialized areas of analog and power electronics. In this regard, exploring graphene-semiconductor junction-based bipolar devices may offer unique opportunities and advantages compared to graphene junction-based FETs.

5.3 Bipolar transistor based on graphene heterostructure

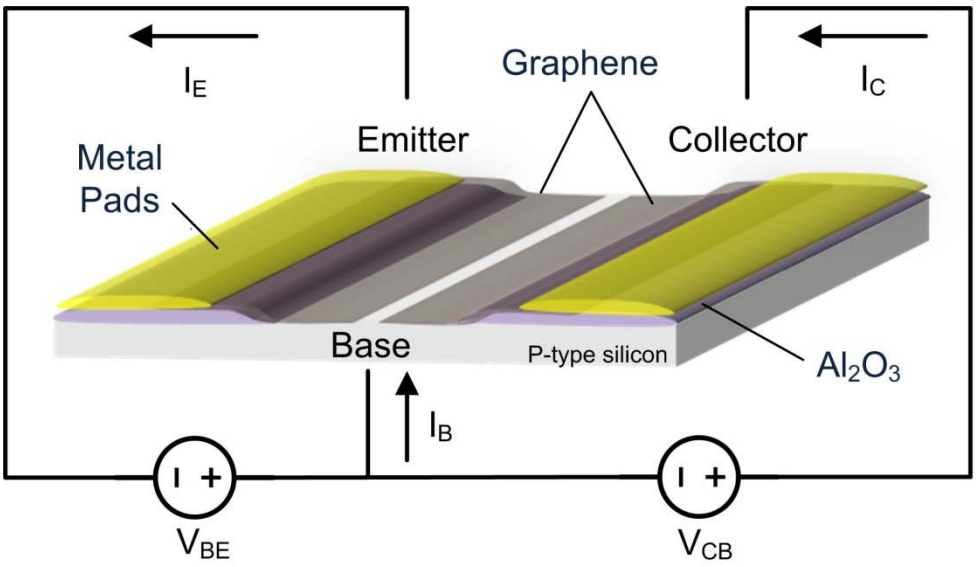

Figure 5.4 Schematic of bipolar transistor made of graphene-silicon heterostructure.

Figure 5.4 is a schematic of the bipolar transistor made of graphene-semiconductor heterostructure. In this structure, the most conventional semiconductor material that is readily available (silicon) was used as the base material between an emitter and a

collector, both made of single-layer graphene. A lateral structure was designed instead of a vertical structure for several reasons. First of all, this is the first demonstration of a graphene-based bipolar transistor, and a high quality single crystalline silicon was desirable to exclude any kind of failure mechanism that may come from a low quality semiconductor. Graphene itself is also highly inert and it is extremely difficult to epitaxially grow high quality material on top of a graphene sheet to form a vertical structure. Additionally, having a lateral structure greatly simplified the fabrication procedure by reducing the process steps.

A p-type silicon (10-20 ohm-cm, $n \approx 10^{15}$ cm^{-3}) wafer was used for this device. After the deposition of 100nm thick Al_2O_3 using an ALD process, the silicon surface was exposed using buffered HF etch. Immediately after etching, a graphene layer was transferred. Graphene layers are known to be impermeable to gases[139], and immediate transfer of graphene minimized the formation of oxide on silicon. Palladium was chosen as the metal because it is known to have low contact resistance with graphene and to have a similar work function [130]. After metallization (palladium, 80nm) to form the probe pads, photolithography was used to pattern the graphene. The length of the graphene-graphene gap is 1.5 μm and the width is 360 μm. Such a high ratio was chosen to minimize any effect of series resistance coming from the graphene layer. After patterning, another Al_2O_3 layer (used as a passivation layer, not shown in Figure 5.4) was deposited to protect the device from any environmental effect. The final passivation layer serves two purposes. It prevents environmental doping of graphene and also acts as an additional protection layer against silicon oxidation. After a simple transport measurement, the

Dirac point of the transferred graphene was found to be near 0V gate voltage, which means there was very little doping from the environment.

This form of graphene-based transistor offers several unique advantages. First of all, the interfaces of the transistor, which perform the function of emission and collection, are all located at the surface. With no gate dielectric, this transistor has the potential to become the world's thinnest bipolar junction transistor with active region thickness of only a few nm. Another advantage is that there are no high temperature diffusion processes to form the emitter or collector. Absolutely no furnace process was used to form this transistor, and other than the initial oxide formation, every process was done at room temperature. This greatly reduces cost and offers new opportunities for electronics based on a polymer platform that requires a low temperature process. Furthermore, unlike metal, which was used in the surface barrier transistor, graphene is extremely stable and tolerant against high temperature. Graphene is known to be stable up to 2800°C in vacuum and 750°C in air[140]. This greatly mitigates the disadvantages of metal-based Schottky junction devices in high voltage or high power applications where the junction may heat up. With graphene, there are no metal ion migrations at high temperature that will either short the device or degrade the performance. Moreover, graphene is known to be a great diffusion barrier that will prevent any metal ion diffusion[141].

5.4 Graphene - silicon junction interface

Before looking into the output characteristics of the graphene heterojunction BJT, it is first necessary to investigate its junction properties.

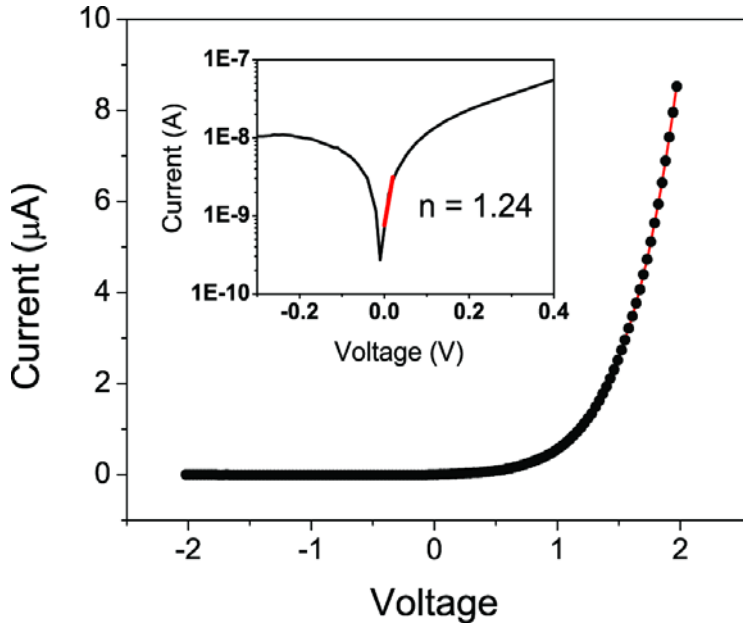

Figure 5.5 Current versus bias voltage characteristics of diode formed by graphene on p-type silicon. The inset figure shows the current on a log scale.

Figure 5.5 displays diode characteristics of graphene-silicon junction in both linear and log (inset) scale. From the diode equation,

$$I = I_o \left[\exp\left(\frac{qV_{bias}}{nk_BT}\right) - 1\right] \text{.....Equation 5.1}$$

and the forward characteristics at low bias, we can extract a diode ideality factor n ≈ 1.24. The ideality factor obtained in our diode is better than those reported with exfoliated graphene samples on silicon [142, 143]. This confirms the high interfacial quality of our graphene-silicon junction.

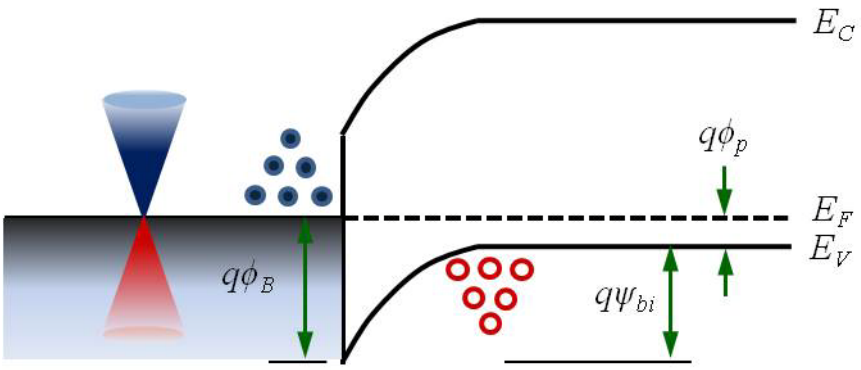

Figure 5.6 Energy band-diagram of graphene on p-type silicon under thermal equilibrium

Figure 5.6 illustrates the energy band diagram for graphene on a p-type silicon under thermal equilibrium. Under zero bias condition, the junction is similar to a typical Schottky junction. Several experimental results in the past have confirmed the barrier height ϕ_B of graphene on p-type silicon to be around 0.45 eV[129, 142].

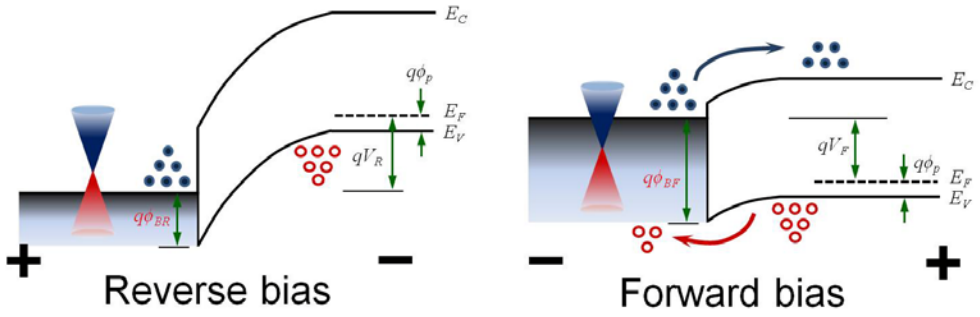

Figure 5.7 Energy band-diagram of graphene on p-type silicon under reverse and forward bias.

Figure 5.7 illustrates the energy band diagram for the forward and the reverse bias condition. It is important to note that the barrier height ϕ_B changes with different bias conditions. This is unusual because there is no gate structure in this case. Several

experimental results have confirmed this phenomenon in the past. Tongay et al.[138] found that the graphene's Fermi level and the work function are subject to variation during charge transfer across the graphene-semiconductor interface as measured by *in-situ* Raman spectroscopy. Zhong et al.[133] also confirmed that the Fermi level and the work function in graphene can be shifted by the charge carrier transport using conductive atomic force microscopy. Under the reverse bias condition, this changes little in terms of charge transport. Barriers for both holes and electrons are high and neither charge carrier can readily pass through the barriers. However, under the forward bias condition, the result is dramatically different from that of a traditional Schottky junction. A rise in the barrier height from ϕ_B (Figure 5.6) to ϕ_{BF} (Figure 5.7) will increase the barrier height for holes from the graphene side to the p-silicon side. However, it also decreases the barrier for electrons from the graphene side to the silicon side. These electrons are minority carriers for the p-type silicon, which indicates that minority carrier injection is facilitated by using graphene instead of metal. This is a very important characteristic of graphene semiconductor junction, which is the fundamental working mechanism of the bipolar junction transistor based on graphene heterojunction. The differences between the graphene- and the metal-based transistor are explained in the next chapters.

As for the hole carriers (majority carriers) from silicon to graphene, the potential barrier height is similar to that of a metal Schottky junction. However, graphene's low DOS for holes due to the bias will hamper the hole transport from the silicon layer to graphene and this may also promote the gain characteristics of the BJT.

5.5 Output characteristics

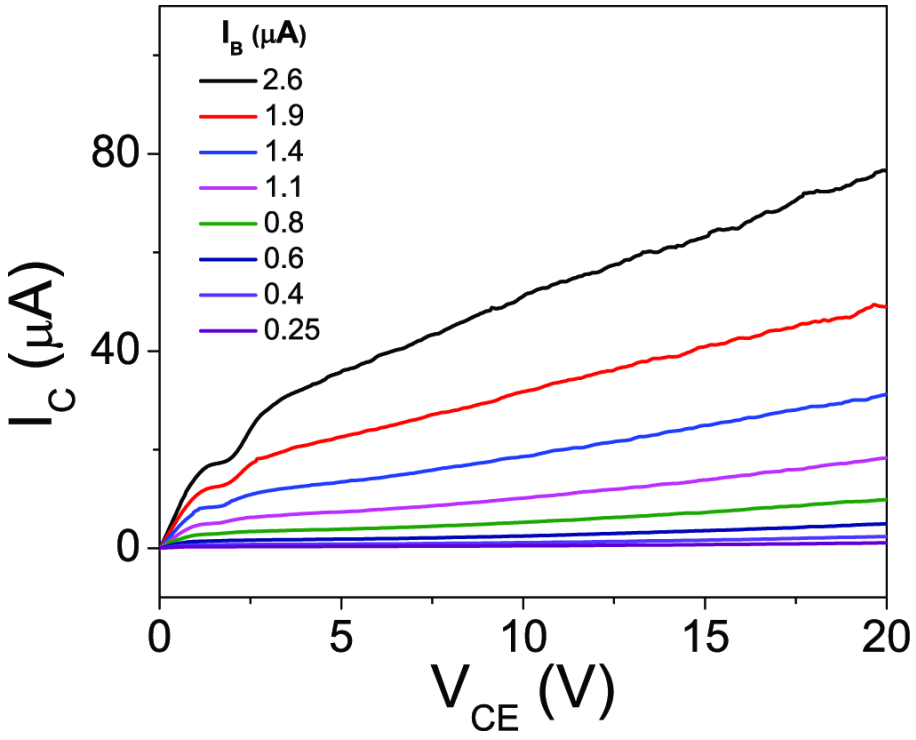

Figure 5.8 Output characteristics of graphene bipolar transistor.

Figure 5.8 shows the output characteristics of the graphene bipolar transistor. Depending on the V_{CE} and the I_B bias, on/off ratio exceeding 10^5 is readily achievable. One distinctive feature that is not observed in most standard data is the quasi-saturation of I_C near the region of lower V_{CE} and higher I_B value. Physically, this is caused by conductivity modulation in the collector when the injected electron density is higher than the collector doping.[137] This leads to high electron concentration at the collector side of the base edge leading to a reduced current in quasi-saturation region compared to that of normal saturation region. This phenomenon is not new in conventional bipolar junction transistors with silicon junctions. Since the graphene near the collector region is nearly neutral or slightly p-doped, this quasi-saturation is expected. As V_{CE} increases, the neutral base width decreases and this prevents current from saturation[137]. This is

known as the Early effect, which was observed in the output characteristics. The Early voltage V_A extrapolated from the output curve was -22V.

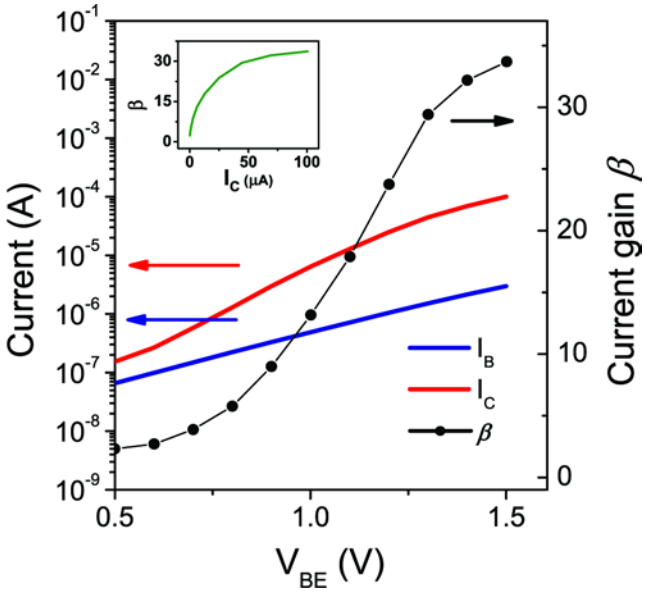

Figure 5.9 The Gummel plot and the current gain β as a function of base-emitter voltage V_{BE}. The inset is the current gain β as a function of the collector current.

Figure 5.9 is a Gummel plot (red and blue lines) with both the collector current I_C and the base current I_B on a logarithmic scale as a function of the forward bias voltage V_{BE} applied to the emitter and the base terminal. The current gain $\beta = I_C/I_B$ is also shown as a function of V_{BE} and as a function of I_C (inset). As typically found in most bipolar transistors, the current gain is approximately constant (≈33.7 at I_C≈100μA) for the voltage range where both the base and the collector currents are approximately ideal [144]. However, at lower current, the large base current prevents the current gain from reaching the maximum value and the gain is typically lower[144].

5.6 Comparison with metal based surface barrier transistor

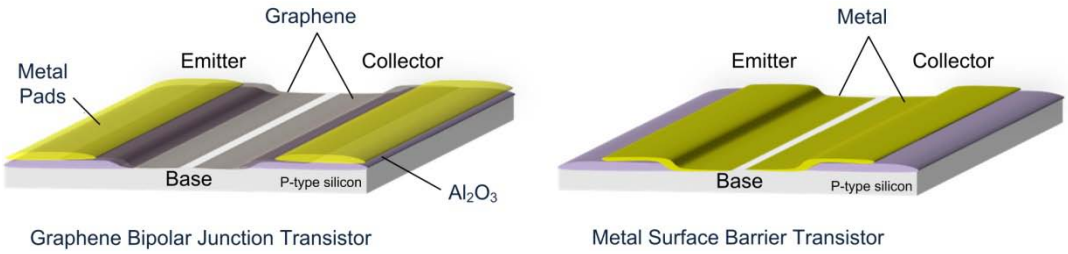

Figure 5.10 Structural comparison between a graphene based bipolar transistor and a metal based surface barrier transistor.

In order to observe the graphene's effect on the barrier, a comparison with its metal counterpart is essential. To have a fair comparison, a metal-based surface barrier transistor (SBT) was fabricated with exactly the same dimension, contact metal type (Pd), and contact metal thickness (80nm). Palladium was chosen as the metal because its Schottky barrier height with p-type silicon (~0.4 eV)[145] is known to be similar to that of graphene/p-silicon (~0.45 eV)[129, 142]. In addition, as stated earlier, palladium forms a low resistance contact with graphene[130]. The metallization method (e-beam evaporation) for the metal SBT was exactly the same as the method for the graphene BJT.

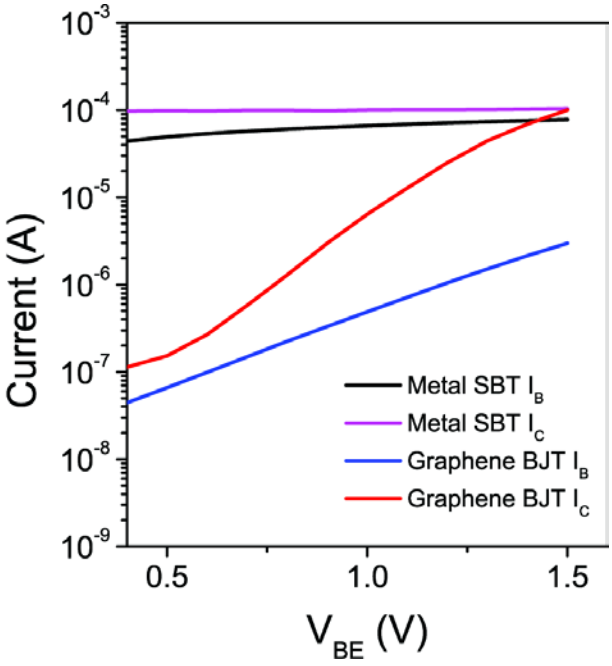

Figure 5.11 The Gummel plot of graphene bipolar junction transistor (red, blue) and metal surface barrier transistor (magenta, black).

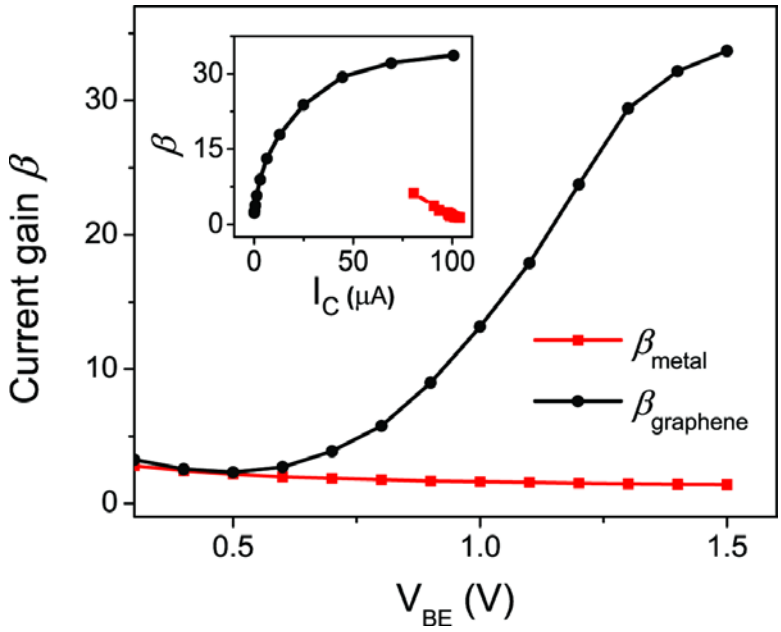

Figure 5.12 The current gain comparison of graphene bipolar junction transistor (black) and metal surface barrier transistor (red) as a function of V_{BE} and I_C(inset).

The output characteristic of a metal SBT showed a stark contrast to that of a graphene BJT. Figure 5.11 is a comparison of the Gummel plot for the metal SBT and the graphene BJT. First of all, the magnitude of I_B and I_C of metal SBT were several orders of magnitude higher than those of graphene BJT. This is comprehensible because the metal thickness of metal SBT (80nm) is ~80 times thicker than that of graphene (<1nm). However, what is more interesting is that the rate of increase for I_C,I_B and the ratio of I_C to I_B was much smaller for the metal SBT. Figure 5.12 is the current gain β comparison of these two types of transistors. The most distinctive characteristic of this plot is the opposite trend of the current gain increase for both transistors. For a graphene BJT, the current gain β increases with base-emitter voltage V_{BE} and collector current I_C just like a conventional BJT. However, for a metal SBT, the current gain decreases with increasing V_{BE} and I_C. In addition, the gain value for metal SBT was significantly lower with a maximum value around 3. Just like the first surface barrier transistor, the metal SBT suffered from low gain. In order to understand what is causing this, it is necessary to investigate the energy band diagram for both of these transistors.

5.7 Operating Principle

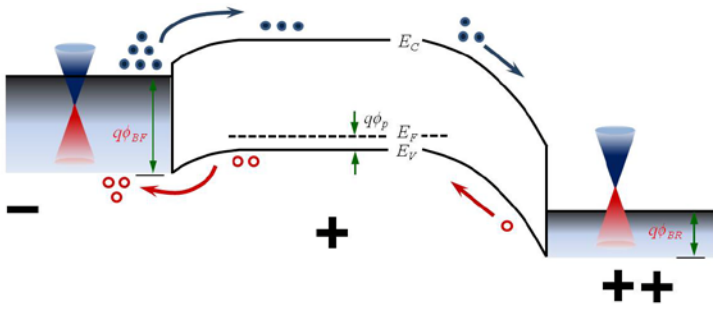

Figure 5.13 The energy band diagram of a graphene BJT on p-type silicon biased in the normal operating condition. The junction at the left is the base-emitter junction and the junction at the right is the base-collector junction.

Figure 5.13 is the energy band diagram of the graphene BJT biased in the normal operating condition. Analogous to an n-p-n BJT, minority carriers (electrons) are injected from the graphene emitter to the p-silicon base and diffused to the graphene collector. The base, being a p-type, does not collect electrons. The hole diffusion component that originates from the base acts as the base current. If the ratio of the electron to hole diffusion components of the base emitter junction is larger than 1, a current gain I_C/I_B is realized[137].

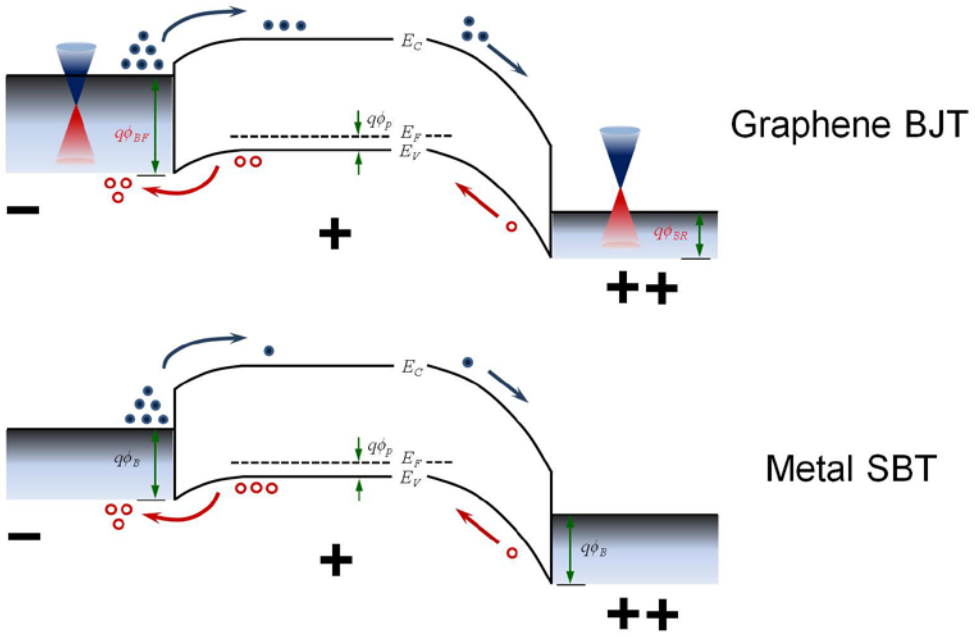

Figure 5.14 Comparison of the energy band diagram for graphene BJT and metal SBT under normal operating bias condition

Figure 5.14 is an illustration comparing the energy band diagram of the graphene BJT and the metal SBT. The main difference is that for a graphene BJT, the Fermi level of the graphene is shifted because of its low DOS. This in turn results in different barrier heights for both the base-emitter (BE) junction and the base-collector (BC) junction. However, for the metal SBT, the Fermi level remains the same because of metal's high

DOS near the Fermi energy. In the metal SBT, as higher V_{BE} or V_{CE} is applied to the BE junction, the increase in the majority carriers (hole) is much larger than the increase in the minority carriers (electrons). This is a typical Schottky junction behavior where the majority carrier dominates the current flow across the BE junction. This explains the current gain reduction in metal SBT (Figure 5.12) as V_{BE} or I_C increases.

As for the graphene BJT, as V_{BE} is increased across the BE junction, the flow of the minority carrier (electrons) from the graphene emitter to the p-silicon base is facilitated by the change in the barrier height ϕ_{BF}. As higher V_{BE} bias is applied, the barrier lowers even more and this increases minority carrier injection. Although the increase in V_{BE} will also decrease the barrier for the majority carriers (holes), the low DOS of graphene will limit the maximum amount of majority carrier current component. Consequently, as higher V_{BE} is applied, the ratio of the minority carrier injection to the majority carrier diffusion (i.e. the current gain β) will increase. This explains the current gain increase in Figure 5.12 as V_{BE} increases. Regardless of the barrier height at both junctions, the ultimate limiting factor for the carrier flow would be the low DOS of graphene. This may also be the limiting factor for higher current gain and explains the current gain saturation shown in Figure 5.12. In addition, just like most BJTs, as higher I_C flows, the current gain reaches a saturation point because the injected minority carrier in the base approaches the majority carrier density at the base (also known as high-level injection condition), effectively decreasing the emitter efficiency[137].

5.8 Common-emitter configured amplifier response

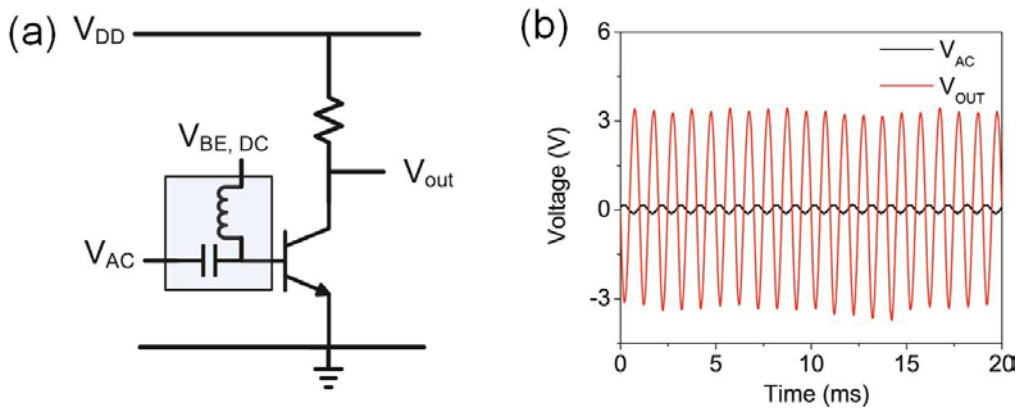

Figure 5.15 (a) Common emitter amplifier configuration with a graphene BJT. (b) Transient response of the amplifier input and output. The voltage gain is 24.9.

The graphene BJT was configured as a common-emitter amplifier (Figure 5.15 (a)) and the transient response is shown in Figure 5.15 (b). A voltage gain of 24.9 was observed with I_E of 16μA. This is one of the highest gains achieved with a graphene transistor-based amplifier circuit. The input V_{AC} was 0.28 V_{pp} and the output V_{out} was 6.96 V_{pp}. Gate bias V_{BE} was 1.5 V and the load resistance value was 10 kΩ.

5.9 Discussion and conclusion

Decades of research have been conducted to optimize the structure of conventional bipolar junction transistors and their variants. The graphene-based bipolar junction transistor investigated in this work is unlikely to replace the conventional bipolar transistors. However, fully understanding the extraordinary behavior of the graphene-semiconductor junction will lead to various electron devices with diverse functionalities.

This work has resulted in building the first graphene-based bipolar junction transistor. As stated earlier, this type of transistor exploits a Schottky-like junction but

has higher minority carrier injection efficiency analogous to a semiconductor p-n junction used in bipolar transistors. Along with graphene BJT's extremely thin active area, a low temperature process that eliminates expensive furnace steps, and extremely high temperature tolerance, this new type of graphene transistor offers opportunities for novel applications in specialized areas such as flexible thin film electronics or high temperature, high power electronics. In addition, because it is possible to form this Schottky-like junction without using metal, several problems that stem from the use of metal (e.g. metal ion migration, thermal instability, punch through, and low reverse bias tolerance) can be completely disregarded. It is even possible to completely eliminate the use of metal by using a thicker graphene layer that is doped. Moreover, since there is no dielectric layer in the graphene BJT, the drawbacks of a dielectric layer (e.g. dielectric breakdown due to electrostatic discharge (ESD), higher RC constant due to parasitic capacitance) are also mitigated.

Finally, as explained in the previous section, the work function tunability of graphene is a phenomenon that is unique to the graphene semiconductor junction. Many new possibilities for novel device structures exist, and these graphene junction-based solid-state devices will provide additional functionalities to the field of electron devices.

Chapter VI

Summary and Conclusions

6.1 Summary of completed work

The purpose of this study was to understand and exploit the extraordinary properties of graphene to develop novel applications in the area of nanoelectronics. A comprehensive understanding of its energy band structure, junction characteristics, and carrier transport behavior is an essential component of this work. After a thorough characterization of the synthesis method, the film quality, and the doping method, several novel applications for graphene were investigated. A rational method to grow wafer-scale, bilayer graphene film was developed and utilized to produce high quality transparent and flexible conductive material. Based on the accumulated knowledge of the synthesis and the fabrication methodology, a fully bendable and transparent all-graphene circuit capable of encoding quaternary digital information was developed and tested. In the previous chapter, the first graphene-based bipolar transistor, developed by utilizing graphene's variable work function, was introduced. This device fully exploits the low DOS and the Fermi level tunability of graphene, and it opens up new possibilities for unconventional applications such as flexible thin film electronics, high temperature electronics, and high-speed, high power devices.

6.1.1 Wafer scale homogeneous bilayer graphene films by chemical vapor deposition

Single- and few-layer graphene are promising materials for post-silicon electronics because of their potential for integrating bottom-up nanomaterial synthesis with top-down lithographic fabrication at wafer scale. However, single-layer graphene is intrinsically semimetal; introducing an energy bandgap requires patterning nanometer-width graphene ribbons or utilizing special substrates. Bilayer graphene, instead, has an electric-field-induced bandgap up to 250 meV, thus eliminating the need for extreme scaling or costly substrates. A synthesis method to produce a wafer-scale, bilayer graphene film was developed to allow scaling of tunable bandgap, bilayer graphene transistors. The very high uniformity of bilayer graphene film was confirmed with various optical and electrical measurements.

6.1.2 Homogeneous bilayer graphene film based flexible transparent conductor

Graphene is considered a promising candidate to replace conventional transparent conductors because of its low opacity, high carrier mobility and flexible structure. Multi-layer graphene or stacked single-layer graphenes have been investigated in the past but both have their drawbacks. The uniformity of multi-layer graphene is still questionable, and single-layer graphene stacks require many transfer processes to achieve sufficiently low sheet resistance. In this work, bilayer graphene film grown with low-pressure chemical vapor deposition was used as a transparent conductor for the first time. The technique was demonstrated to be highly efficient in fabricating a conductive and uniform transparent conductor compared to multi-layer or single- layer graphene. Four transfers of bilayer graphene yielded a transparent conducting film with a sheet resistance of 180 $\Omega_{\square}$ at a transmittance of 83%. In addition, bilayer graphene films transferred onto plastic substrates showed remarkable robustness against bending, with sheet resistance

change less than 15% at 2.14% strain, a 20-fold improvement over commercial indium oxide films.

6.1.3 An all-graphene flexible and transparent circuit for quaternary digital modulation

In modern communication systems, modulation is a key function that embeds the baseband signal (information) into a carrier wave so that it can be successfully broadcast through a medium such as air or cables. A flexible signal modulation scheme is hence essential to a wide range of applications based on flexible electronics. Here, a fully bendable all-graphene modulator circuit with the capability to encode a carrier signal with quaternary digital information is reported for the first time. By exploiting the ambipolarity and the nonlinearity in a graphene transistor, two types of quaternary modulation schemes have been demonstrated: 4-ary amplitude-shift keying (4-ASK) and quadrature phase-shift keying (QPSK) with just 1 and 2 all-graphene transistors. This represents a drastic reduction in circuit complexity when compared with conventional modulators based on silicon transistors. In addition, the circuit is not only flexible but also highly transparent (~95% transmittance) owing to the all-graphene design with every component (channel, interconnects between transistors, load resistor, and source/drain/gate electrodes) fabricated from graphene films. The transistors exhibit a mean hole mobility value of 1770 cm^2/Vs which is several orders of magnitude higher than those of conventional flexible electronics materials, such as organic and amorphous materials. Taken together, these results represent a significant step toward achieving a high-speed communication system that can be monolithically integrated on a flexible and transparent platform.

6.1.4 Bipolar junction transistor based on graphene heterostructure

In this project, the first bipolar junction transistor based on graphene-silicon heterostructure was designed and investigated. Single-layer graphene was used to form the emitter and the collector, and a p-type silicon was used as the base. This BJT fully utilized the Fermi level tunability of graphene to increase minority carrier injection efficiency of the base-emitter junction; it was compared with a metal-based transistor to verify the result. A higher current gain was observed in the graphene-based BJT and an opposite trend in gain increase was observed in the metal transistor. This confirmed the unique property of the graphene-semiconductor junction that is distinctively different from that of a typical Schottky junction. The graphene-based BJT offers several unique advantages, such as an extremely thin active area, low cost, a low temperature fabrication process, and high-temperature tolerance. A BJT current gain of 33.7 and a common-emitter amplifier voltage gain of 24.9 were achieved. Both values are among the highest values achieved with graphene-based transistors.

6.2 Future outlook and challenges

It has been eight years since graphene was discovered by the two Nobel laureates. Since the discovery, the research on graphene material has evolved from the exclusive field of quantum physicist to the domain of various application engineers from interdisciplinary branches of science. In this chapter, I would like to outline the future and the challenges of graphene based applications in the field of nanoelectronics.

6.2.1 Transparent conductors

One graphene application that is close to commercialization is graphene based transparent, flexible conductors. When compared with conventional oxide based inorganic transparent conductors, graphene films have several appealing properties such as mechanical robustness, uniformity, and atomically thin structure. Graphene synthesis methods based on CVD currently seems to be the best method for this application [41, 52]. Although a direct graphene growth on an insulating substrate to eliminate the transfer process would be ideal, it is still highly challenging to form a continuous, defectless graphene on dielectric substrates [146].

Some future improvement can be sought with a more reliable transfer process that minimize any mechanical defects[4] and methods to lower the sheet resistance without compromising the transparency by either incorporating metal nanostructures[50] or high quality doping[49, 106]. Both academic and industry works already show great improvements and we may see commercial products based on graphene conductors in the near future.

6.2.2 Analog electronics

The application of graphene transistors in the analog electronics platform is another area with great potential. Graphene is unlikely to replace traditional semiconductor materials (e.g. Si, Ge, III-V) completely due to its lack of bandgap and poor on/off ratio. However, it could be used to improve upon traditional semiconductor based devices, particularly in the field of high-speed electronics and optical modulators

[147]. It is relatively simple to incorporate graphene on a traditional semiconductor based system due to its uniform 2-dimensional nature and room temperature transfer process [147]. Regardless of the simple integration process, graphene analog electronics face a number of challenges. Several analog components such as mixers [33, 34], frequency multipliers [29, 30], modulators [28, 122] and amplifiers [31, 32] have been already demonstrated. However, none of these components was methodically connected to form a complete system. This can be challenging and many chip designers may not be motivated to utilize a new material unless it is necessary. In most systems that utilize bulk semiconductors, graphene is just one choice out of many materials such as III-V semiconductors.

Currently, it is difficult to predict whether the benefit of adding graphene material to a traditional platform such as silicon outweighs the additional complexity and the cost. Although this is something not clear at the moment, it is highly expected that graphene will play a role in high-speed electronics on a non-traditional, flexible platform such as plastic, fabric, or rubber. This is simply because there are not many high mobility (>1000 cm^2/Vs) materials out there that is mechanically flexible and robust. The transparency of graphene is another advantageous feature that may also be used in "see-through" electronics including smart glasses with the capability to display complex information on a transparent platform when necessary.

In general, there are several challenges that graphene researchers have to overcome before graphene can be accepted as an established electronic material. The main challenge that most graphene researchers face in the application for electronics is its poor on/off ratio and weak saturation behavior. It is cautiously predicted that this problem

will not be easily resolved without using an additional material to form a heterostructure with graphene[26, 125]. The first BJT based on graphene that the author presented is an example how graphene can be utilized with the conventional materials to form a suitable transistor for application area other than analog electronics. The higher on/off ratio and the strong saturation behavior of this hybrid device shows promise in high transconductance, high gain electronics in both the digital and the analog domain.

The next one is the environmental effect, particularly environmental doping. Environmental doping will shift the Dirac points subsequently causing so called "process variations". It is crucial to control the impurity level during metal etching and subsequent process to minimize the shift of Dirac point in order to realize wafer-scale graphene electronics.

Another issue of importance is the parasitic components (e.g. contact resistance, series resistance) from the use of graphene material. Although it is presumed graphene and metal forms an ohmic contact, some researchers have brought up the issue of contact resistance between graphene and metal[148], which can be particularly important in high-speed RF applications. The control of interface quality between graphene and metal is important to reduce any contact asymmetry or parasitic components. The finite sheet resistance of graphene is another component that need to be addressed if graphene is to be used as an interconnect or a conductive material to replace metal. This is particularly related to the previous subject of transparent conductor and there are many on-going research efforts to improve the sheet conductivity.

The final issue that requires attention is the substrate. Due to SiO_2 induced scattering associated with trap charges and low energy surface phonons, special substrate

such as diamond-carbon, boron nitride, or SiC are advantageous for high speed electronics[83, 84, 149]. Incorporating these substrates, recent state-of-art graphene process has resulted in wafer-scale circuits consisting of graphene transistors with cut-off frequencies of 300 GHz[149] without the aid of any special fabrication process.

Throughout the history of semiconductor industry, the process of introducing a new material has never been simple. Even III-V materials, which have been studied for a long time, still face many challenges [150]. As interest in graphene material continues to expand, the technical issues related to graphene process will also be resolved. When the key challenge of graphene-semiconductor integration and processing is addressed, graphene material will be a vital part of the on-going electronics evolution.

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APPENDICES

Appendix A

Multilayer graphene (MLG) characterization and growth

25μm thick copper foil (99.8%, Alfa Aesar) was loaded into an inner quartz tube inside a 3 inch horizontal tube furnace of a commercial CVD system (First Nano EasyTube 3000). The system was purged with argon gas and evacuated to a vacuum of 0.1 Torr. The sample was then heated to 1000°C with argon (1000sccm) and hydrogen (50 sccm) flow at atmospheric pressure for annealing. When 1000°C is reached, the annealing process is maintained for 30 minute, and then 50 sccm of CH_4 is flowed for 5 minutes at atmospheric pressure. The sample is then cooled to room temperature without CH_4 gas flow. The hydrogen is cut off but the argon flow is maintained during the cooling process.

Appendix B

Transmittance measurement

The transmittance measurement setup consists of a monochromator (Acton SP2300 triple grating monochromator/spectrograph, Princeton Instruments) coupled with a 250Wtungsten halogen lamp (Hamatsu), a collimator, and a photodetector. An iris was used to prevent the photodetector from absorbing the scattered light from the substrate. Optical power measurements were carried out using a 1928-C power meter (Newport) coupled to a UV enhanced 918UV Si photodetector (Newport). A blank PEN substrate was used as a reference for subtraction.

Appendix C

Carrier Mobility Extraction

The contact resistance and the mobility can be extracted by fitting the experimental value of resistance across the source and drain of the graphene transistors with the following equation[148],

$$\boldsymbol{R_{total}} = \frac{\boldsymbol{V_{ds}}}{\boldsymbol{I_{ds}}} = \boldsymbol{R_{contact}} + \frac{\boldsymbol{L}}{\boldsymbol{q\mu W}\sqrt{\boldsymbol{n_o}^2 + (\boldsymbol{C_{ox}}\frac{(\boldsymbol{V_g} - \boldsymbol{V_{Dirac}})}{\boldsymbol{q}})^2}} \quad \text{.....Equ. A1}$$

where the variables are defined as drain/source voltage V_{ds}, drain/source current I_{ds}, contact resistance $R_{contact}$, gate capacitance C_{ox}, residual carrier concentration n_o, the gate voltage V_g, the charge neutrality point V_{Dirac}, drain/source width W and length L. Device in Figure 4.9 indicated a hole mobility of 3342±26 cm^2/Vs and electron mobility of 2813±11 cm^2/Vs with residual concentration of $n_o = (2.47\pm0.01)\times10^{11}$ cm^{-2}, and $R_{contact}$ = 116.4±0.1 kΩ. For all the cases, the residual concentration matched well with the reported values 2×10^{11} cm^{-2} .[117] Notably, the high contact resistance is resulted from series resistance of long graphene strips which have been used as the interconnects between the drain/source electrodes and the contacts. Although the large series resistance currently limits the frequency performance of the devices, this problem can be resolved by partial doping of graphene interconnects in the future. Several works have shown it is

possible to lower the graphene sheet resistance significantly by room temperature doping[41, 49].

Appendix D

Extraction of carrier to noise ratio (C/N)

Signal to noise ratio is defined as,

$$10\log_{10}\frac{V_{signal}^2}{V_{Noise}^2}\ [\mathrm{dB}] \quad \textbf{.....Equ. A2}$$

This figure characterizes the ratio of the fundamental signal to the noise spectrum. The noise spectrum includes all non-fundamental spectral components such as spurs and the noise floor in the Nyquist frequency range (sampling frequency / 2) without the DC component, the fundamental itself and the harmonics. Six harmonics were considered in our calculation. Carrier to noise ratio (C/N) [i.e. signal to noise ratio of a modulated signal] of 21.1 dB was extracted from the fast Fourier transform plot using a conventional program, SBench 6.1 (Spectrum GmbH). The bit error rate (BER) from this C/N value is significantly better than the performance threshold of a QPSK system as indicated in the reference [119].

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