

**Nano-Watt Modular Integrated Circuits for  
Wireless Neural Interface**

**by**

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**A dissertation submitted in partial fulfillment  
of the requirements for the degree of  
Doctor of Philosophy  
(Electrical Engineering)  
in the University of Michigan  
2013**

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## **DEDICATION**

To my beloved family for all their support and patience during my years of study

## ACKNOWLEDGMENTS

I would like to express my greatest gratitude and appreciation to my research advisor, Prof. Euisik Yoon, for all his support, and guidance during my Ph.D. study at University of Michigan, Ann Arbor, MI. This work would not have been possible, and I would not be what I am now, without his endless guidance to extreme level of quality work since 2003. I would also like to thank my doctoral committee members, Prof. Ken Wise, Khalil Najafi, Michael Flynn, and Parag Patil, for their participation, invaluable advice, and thoughtful comments and suggestions for increasing the quality of this research work. I would like to thank Dr. Dan Moran and Tim Denison for the supports and advices.

I would also like to thank my former and current colleagues in my research group: Khaled, Seok-Jun, Ji-Hyun, Sung-Yun, Kyoungwan, Kyuseok, Xia, Fan, Patrick, Yu-Chih, Mike, Roberto, Adam, Yu-Ju, Yu-Heng, Jaehoon, Maesoon, Il-Joo, Hyung-Kyew, Gwang-Hyun, Sang-wook, Sewhan, Seong-Jin, Kyoung-Hyun, Young-Ji, and Prof. Songjun Lee for their helpful suggestions, useful discussions, technical and emotional support.

Finally, my deepest gratitude and indebtedness go to my parents, for all the sacrifices they made to make my life better and more successful. I would also like to express my sincere gratitude to my beloved my family, Ho-Jung La and Nathan (Hochae) for all their love and understating and support throughout the years



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## **ABSTRACT**

### **Nano-Watt Modular Integrated Circuits for Wireless Neural Interface**

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In this work, a nano-watt modular neural interface circuit is proposed for ECoG neuroprosthetics. The main purposes of this work are threefold: (1) optimizing the power-performance of the neural interface circuits based on ECoG signal characteristics, (2) equipping a stimulation capability, and (3) providing a modular system solution to expand functionalities.

To achieve these aims, the proposed system introduces the following contributions/innovations as follows: (1) power-noise optimization based on the ECoG signal driven analysis, (2) extreme low-power analog front-ends, (3) Manchester clock-edge modulation clock data recovery, (4) power-efficient data compression, (5) integrated stimulator with fully programmable waveform, (6) wireless signal transmission through skin, and (7) modular expandable design. Towards these challenges and contributions,

three different ECoG neural interface systems, ENI-1, ENI-16, and ENI-32, have been designed, fabricated, and tested.

The first ENI system, ENI-1, is a one-channel analog front-end and fabricated in a  $0.25\ \mu\text{m}$  CMOS process with chopper stabilized pseudo open-loop preamplifier and area-efficient SAR ADC. The measured channel power, noise and area are  $1.68\ \mu\text{W}$  at  $2.5\text{V}$  power supply,  $1.69\ \mu\text{V}_{\text{RMS}}$  (NEF=2.43), and  $0.0694\text{mm}^2$ , respectively. The fabricated IC is packaged with customized miniaturized package. *In-vivo* human EEG is successfully measured with the fabricated ENI-1 IC.

To demonstrate a system expandability and wireless link, ENI-16 IC is fabricated in  $0.25\ \mu\text{m}$  CMOS process and has sixteen channels with a push-pull preamplifier, asynchronous SAR ADC, and intra-skin communication (ISCOM) which is a new way of transmitting the signal through skin. The measured channel power, noise and area are  $780\text{nW}$ ,  $4.26\ \mu\text{V}_{\text{RMS}}$  (NEF=5.2), and  $2.88\text{mm}^2$ , respectively. With the fabricated ENI-16 IC, *in-vivo* epidural ECoG from monkey is successfully measured.

As a closed-loop system, ENI-32 focuses on optimizing the power performance based on a bio-signal property and integrating stimulator. ENI-32 is fabricated in  $0.18\ \mu\text{m}$  CMOS process and has thirty-two recording channels and four stimulation channels with a cyclic preamplifier, data compression, asymmetric wireless transceiver (Tx/Rx). The measured channel power, noise and area are  $140\text{nW}$  ( $680\text{nW}$  including ISCOM),  $3.26\ \mu\text{V}_{\text{RMS}}$  (NEF=1.6), and  $5.76\text{mm}^2$ , respectively. The ENI-32 achieves an order of magnitude power reduction while maintaining the system performance. The proposed nano-watt ENI-32 can be the first practical wireless closed-loop solution with a practically miniaturized implantable device.

# **CHAPTER 1**

## **INTRODUCTION**

A number of the organs of the human body have their own specific roles to maintain human homeostasis such as heart beat rate, blood pressure, temperature, motion and so forth. Among these organs, the brain plays an essential role in organizing and regulating the organism in the most harmonious way. The brain is the most complex organ which not only controls other organs, but can also think, feel, and express emotion.

Unfortunately, over 5% of the US population is suffering from neurological diseases such as epilepsy, Parkinson's disease, and Alzheimer's disease. Furthermore, around 2% of the US population has experiences amputation due to car accidents, work injuries, or battle wounds. These kinds of disabilities can easily put the patient into a dangerous situation, but also affect them and their family's life quality. In order to treat these people and provide them with renewed way of mobility, we need to better understand the function of the brain.

A neural interface could help us understand neural activities by monitoring neurons (single or multiple or a group of neurons) and extracting certain features of their activities. The extracted information from a neural interface system can be utilized to treat people as well as to control neural prosthetics such as a wheel chair or artificial limb so that they can play an active role in the society again.

In this chapter, we will introduce the basic brain physiology in order to understand the origin of the neural signals. Also, advances in the various neural interface systems

will be reviewed and compared. After discussing the challenges of developing the neural interface system, the research objectives and the contributions of this work will be explained.

## **1.1 Brain Physiology**

With a weight of about 1.5 kg and a size of around 1130 cm<sup>3</sup> in women and 1260 cm<sup>3</sup> in men, the brain consists of very soft white and grey matter, similar to gelatin, and is composed primarily of two types of cells: neurons and glial cells. Contrary to any other cells, neurons can transmit signals to specific target cells over long distances. Glial cells support the brain structure, metabolism, and insulation between the neurons. Neurons, however, are usually considered the most important cells in the brain.

A neuron consists of a soma, dendrites and an axon, as shown in Figure 1-1 (a). A neuron transmits the signal from the soma to the axon in the form of electrochemical pulses called action potentials, which have a bandwidth of up to 10 kHz with duration of 10 to 100 ms, and can travel through the axon at speeds of 1 to 100 m/s. The typical connection of a single axon can be up to several thousand synaptic connections with other neurons. At the end of the axon, the axon terminal and the dendrite of another neuron form a synapse where the transmitted action potential is converted into a chemical neurotransmitter, transmitted, and received by other neurons as shown in Figure 1-1 (b). Once the concentration (or potential) of neurotransmitter received by the next neuron exceeds a certain threshold level, the following neuron transmits the signal to the next neuron.

Figure 1-2 shows the transient response of the action potential. Action potentials are generated by special types of voltage-gated ion channels such as sodium and potassium



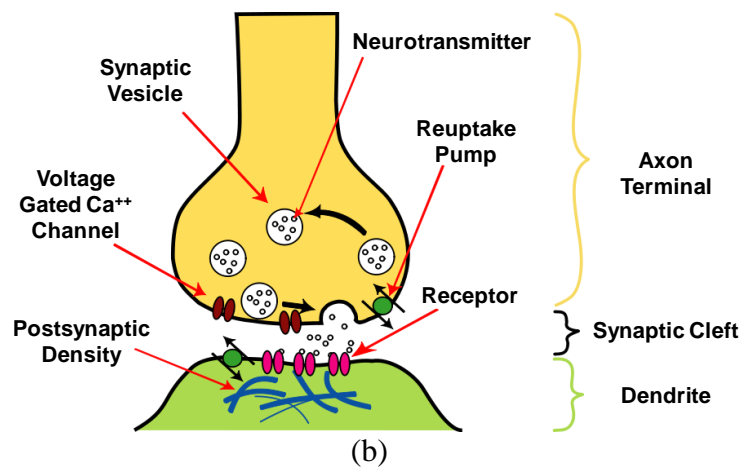
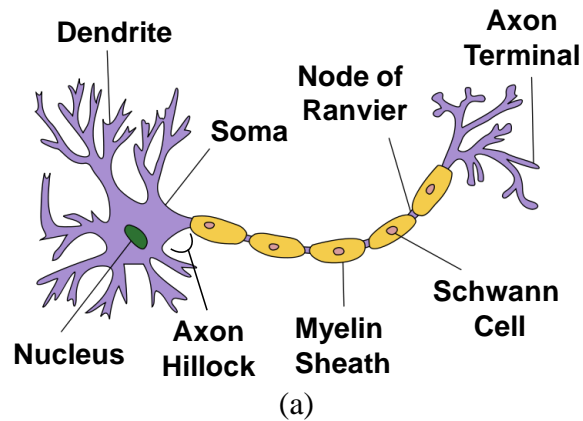


Figure 1-1: Neuron Structure and Synapse (Image Source: Wikipedia)

channels in plasma membrane. The sodium channels are open if the membrane potential increases above a threshold. When the channels open, sodium ions flow into the membrane and change the electrochemical potential gradient across the membrane. Once the polarity of the plasma membrane is reversed, the sodium channels close. Then, potassium channels are activated to allow potassium to flow from inside to outside the neuron and reverse the electrochemical potential gradient. The potassium ion flow creates a negative shift on the potential that can prevent an action potential moving backward. An action potential can travel from neuron to neuron by generating an electrical current flow. This electrical current flow from multiple neurons can also produce a group current

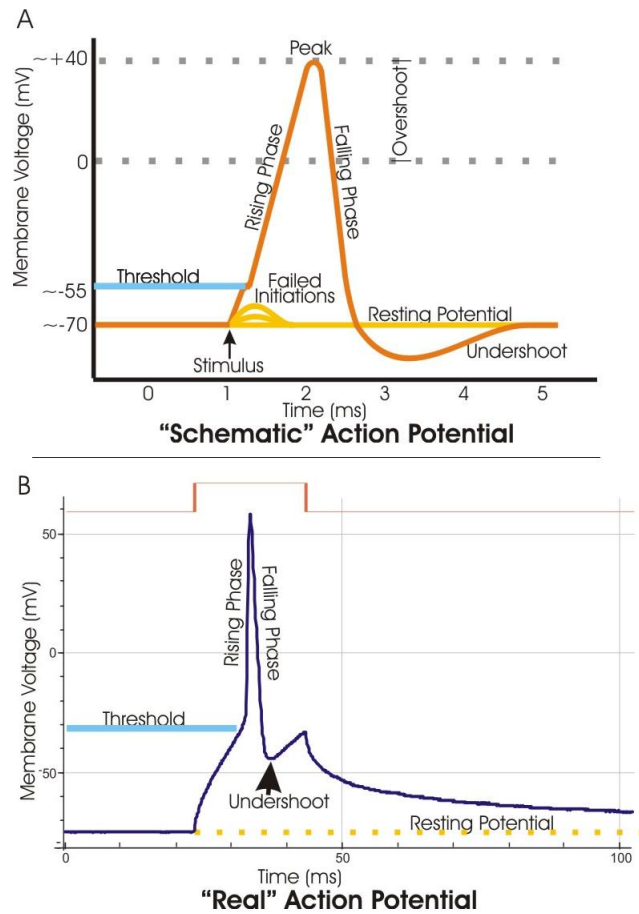


Figure 1-2: Action Potential (Image Source: Wikipedia)

flow, generating potential (or voltage) within a certain area. The group potential can travel up to the surface of the human brain scalp.

The action potentials generated from the body sensory organs, representing vision, sound, smell, and other sensations, can travel up to the brain. Then, the brain determines the related actions to regulate human homeostasis and the appropriate reaction. However, if sensory organs, action potential signal paths, and/or brain neurons are damaged, the human might not function properly. For example, epilepsy is caused by the unwanted sudden action potentials generated throughout a wide area. In order to treat these people and restore normal functionality, we need to develop a neural interface system to

understand the neuron activities and to provide efficient therapy methods. The following section introduces the neural interface system.

## **1.2 Neural Interface System Overviews**

As mentioned in the previous section, the neural interface system enables us to understand neural activities. In order to interact with the neurons, several sensing methodologies exist such as EEG, ECoG, and Spike detection. Each methodology requires different needs and applications. In this section, we will discuss the various application and recording methodologies with advanced neural interface system.

### **1.2.1 Closed-Loop Epilepsy Treatment System**

The neural interface systems enable us to build a direct communication pathway between the human brain and external devices. By having a direct pathway to brain, we can study the neural activity and build neuroprosthetics and brain computer interface. Also, this technique can be used for the entertainment. Particularly, the brain disorder treatment is one of the most interesting applications because it can totally change the quality of the life who suffers from the brain disorder. For this reason, in this work, we will focus more on the brain disorder.

Although there are many brain disorders such as Parkinson's disease and brain tremor, particularly, in this work we will focus on epilepsy. Epilepsy is ranked as third neurological disorder with 2.5 million populations only in the USA and 50 million worldwide. Among these patients, about one third of epilepsy patients are intractable and not responsive to medication treatment. More importantly, the incidence of medically intractable epilepsy has been reported to be 17,000 new patients per year only in the USA.

The epileptic seizure is spontaneous and chronically occurs and this disease makes not only the patient difficult but also families and friends to have normal life. More difficult thing is that the epileptic seizure can vary person to person based on the symptom and the site location in the brain. And, each individual requires a personalized treatment.

The most common method to treat is the medication. It is safe and easy to take as needed. However, as mentioned, the drug doesn't work for some patients and the efficacy is not satisfactory for all the patients. For these intractable patients, surgical resection can be another option to treat seizure. In the surgical resection, neural surgeon localizes and removes the location where the epilepsy occurs from the brain. Due to its direct treatment to the brain, this method is very effective. However, this method has a high risk and very expensive due to the high technical complexity. Also, the clinical and technical resources are significantly limited for current medical conditions. So, all of these factors make it difficult for the patients to get the benefit from this surgical resection. To help those who cannot take any benefits from these two methods, it is very important to develop another new treatment method with high efficiency and easy accessibility.

As an alternative treatment method, recently, electrical brain stimulation has been introduced. This method is still in the research phase but, some research shows very promising result such that the electrical stimulation on cortical surface can stop the seizures effectively and electrical stimulation cause less side effects than the medication. There are two ways of electrical brain stimulation methods: open-loop stimulation and closed-loop stimulation. The key difference is whether the stimulation is based on the neural activity or not. In open-loop stimulation, the device stimulates brain continuously with given frequency and predefined setting value. This method does not rely on the




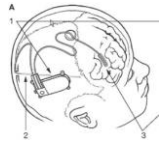
	<b>Medtronics</b>	<b>Cyberonics</b>	<b>NeuroVista</b>	<b>NeuroPace</b>
<b>Application</b>	DBS for Epilepsy	VNS for Epilepsy	Intractable Epilepsy	Intractable Epilepsy
<b>Electrode Type</b>	Passive, DBS	Passive, VNS	Passive, Intracranial	Active, Intracranial
<b>Modality</b>	Rec / Stim	Stim	Rec	Rec / Stim
<b>Wireless Data</b>	Inductive (Short Time)	N/A	Wireless (Data/Visual/Audio)	Inductive (Short Time)
<b>Power</b>	Battery (Replaceable)	Battery (Replaceable)	Battery (Replaceable)	Battery (Replaceable)
<b>FDA</b>	Not Fully Approved	Approved	N/A	Not Fully Approved
<b>Algorithm</b>	Simple	N/A	Warning	Simple
<b>Device Picture</b>				

Figure 1-3: Existing Epilepsy Treatment System

neural activity and inefficient and can cause brain damage due to the continuous stimulation. On the other hand, the closed-loop system, the device monitors the neural activity and once the seizure is detected, it stimulates the brain and stop the seizure. Because of this closed-loop property, this method is more efficient and safer than the open-loop stimulation.

The first approach for this brain stimulation was done by Medtronics and Cyberonics using pre-existing techniques such as deep brain stimulation and vagus nerve stimulation. However, efficiency of these approaches is not still satisfactory. Another company Neurovista also presents the system to treat the epilepsy. However this system only monitors the brain signal and warns the patients that the epilepsy will occur. As a new approach, Neuropace presents the closed-loop system and shows a promising result. However, this system is built up with off-the-shelf component and, system volume is too

big to be implant inside the brain. More critical drawback of these systems is that all these methods have a very simple and inefficient algorithm to detect the epilepsy in advance and impossible to upgrade or reprogram once implanted inside the body for the personal algorithm, which is an essential functionality for effective and practical closed-loop system.

### **1.2.2 Challenges on Epilepsy Treatment System**

To develop the successful and practical epilepsy treatment system, we must overcome some challenges such as subject safety and system performance and functionality and long-term reliability. To avoid any transcutaneous connection from brain to external device, the system must be fully implantable. And, once implanted, it must operate inside brain as long as possible. Also, from the system, we want to have a very clean brain signal over the large area to increase the detection efficiency of the epilepsy more precisely with the personalized algorithm. The stimulation is also essential to treat the patient using an integrated stimulator. Once the device is implanted, the recording quality of the system must maintain. For this reliable operation, we need a hermetic shielded package with chronic long-term electrodes. To successfully overcome these obstacles, the implantable neural interface system must have low-power low-noise closed loop capability with wireless data power transmitter, algorithm, package, and electrode.

To monitor a brain signal to detect the epilepsy efficiently, in the next section, we will discuss the neural recording methodologies in detail.

### **1.2.3 Various Neural Recording Methods**

The neural potential generated by single or multiple neurons can be categorized by four primary different signals: single unit action potential (SUAP), local field potentials

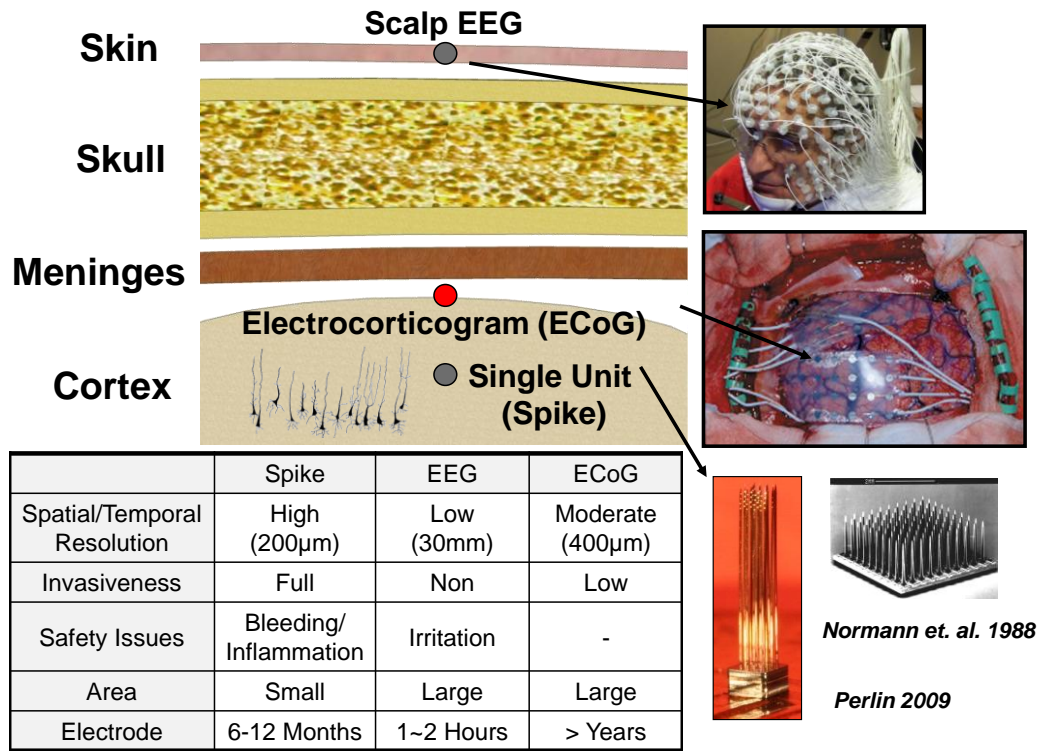


Figure 1-4: Various Neural Interface Systems and its comparison

(LFP), electrocorticogram (ECoG) and scalp electroencephalogram (EEG) according to its sensing location [1]. All of these methods attempt to record  $\mu$ V-level extracellular potentials generated in the cerebral cortical layers. However, each method varies in its relative invasiveness as well as its spatial and spectral frequency. Generally, there is a trade-off between these parameters; the more invasive the recording technique, the higher the spatial and spectral frequency content of the recorded signal. As the spatial/spectral frequency content increases, so does the amount of information gathered from the brain recordings.

Single unit action potential gives us the most accurate neural activity information [1]. The signal is recorded from a single neuron under the cortex, and could provide the 0.2 mm spatial resolution with up to 10 kHz in bandwidth, and 1 mV in amplitude. However, in order to reach a single neuron using micro-machined electrodes [2], [3], the system

must be severely invasive and can lead to an infection of neural tissue. A scalp EEG potential can be obtained on the surface of the scalp. Even though the scalp EEG system is the safest system due to non-penetration of the cranium, a so-called non-invasive system, the bio-information provided by a EEG system is very limited in time and space because the scalp EEG system can only detect the ensemble activities of neuron groups. Furthermore, in the EEG system, the chronic monitoring with free movement is limited by many external cables and devices [4]. In the last few years, ECoG has gained popularity among researchers as the most pragmatic method for long-term chronic brain monitoring. ECoG system records the brain activities on the surface of the cortex penetrating the meninges which is the brain protection membranes under the cranium: the dura mater, the arachnoid mater, and the pia mater. The ECoG system is less invasive than the action potential system, and the recorded signal can provide more accurate bio-information than a surface EEG signal, with 5mm in spatial resolution, 500  $\mu$ V in amplitude, and up to 250 Hz in bandwidth. However, in spite of these advantages, this system still has some limitations such as large system volume and safety issue because currently a passive electrode array is implanted by opening a 2cm hole in skull by craniotomy and tethered with a bundle of wires for data transmission [5], [6].

#### **1.2.4 Advances in Neural Interface Systems**

The ability to continuously record neural signals from active animals and humans has been one of the most important goals in neuroscience and neurophysiology. The neural interface system has been advanced based on the sensing electrodes technology. In this section, the advances in neural interface system will be introduced.



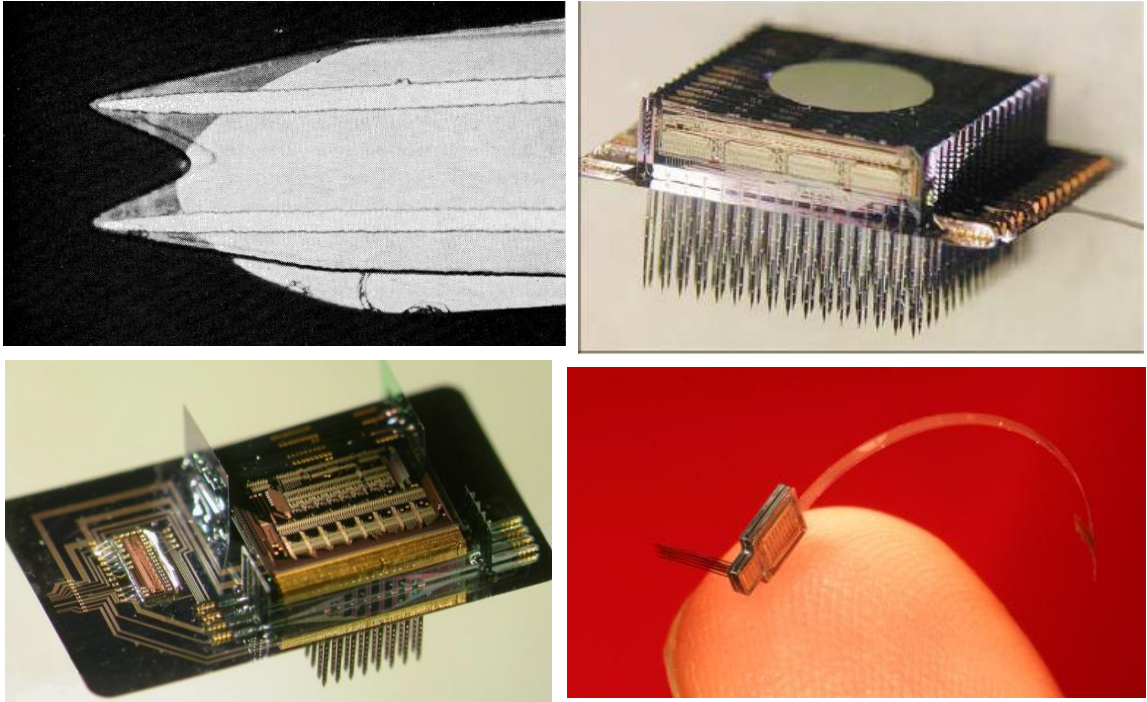


Figure 1-5: 2-D and 3-D Microelectrode Arrays developed by University of Michigan probes.

#### 1.2.4.1 Action Potential / Local Field Potential Recording

Over the past 40 years, University of Michigan has developed and optimized MEMS and micro-fabrication technologies which contributed a major part in developing biocompatible, fully-implantable neural interface systems with a micro-electrode array that penetrates the cortex. This approach has been investigated and has shown remarkable achievements.

Figure 1-5 shows the Michigan probes developed for action potential / local field potential recording. The developed electrode array from two dimensional probe [2], [7] to three dimensional probes [8–11] provide the new era of the interfacing the neurons.

Another research group from University of Utah [12] also developed the three-dimensional micro electrode array as shown in Figure 1-7. The Utah electrode array was developed for interfacing with the shallow cortical structures of the brain where the relatively short electrodes are suitable. However, its shank length is limited by the

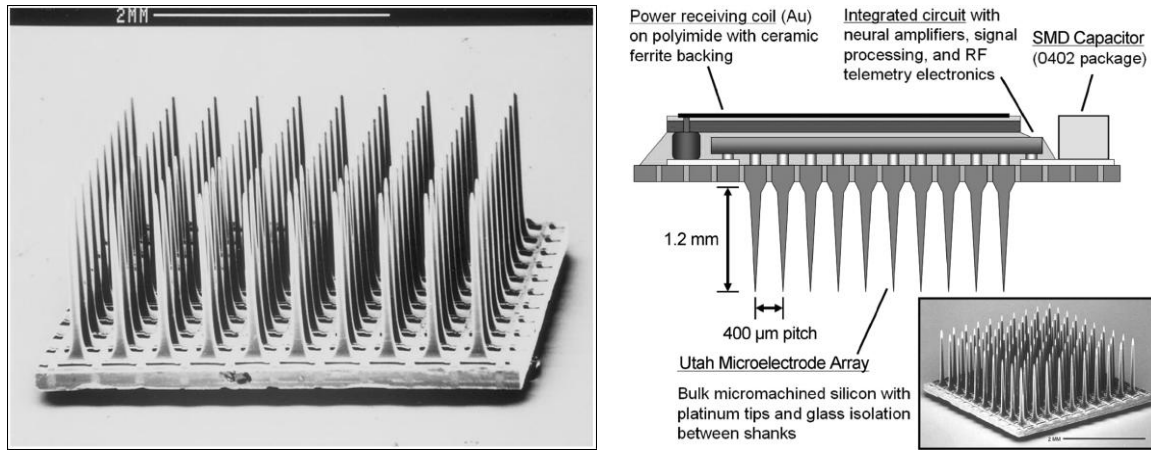


Figure 1-7: 3-D Utah Microelectrode Arrays and its signal processing unit

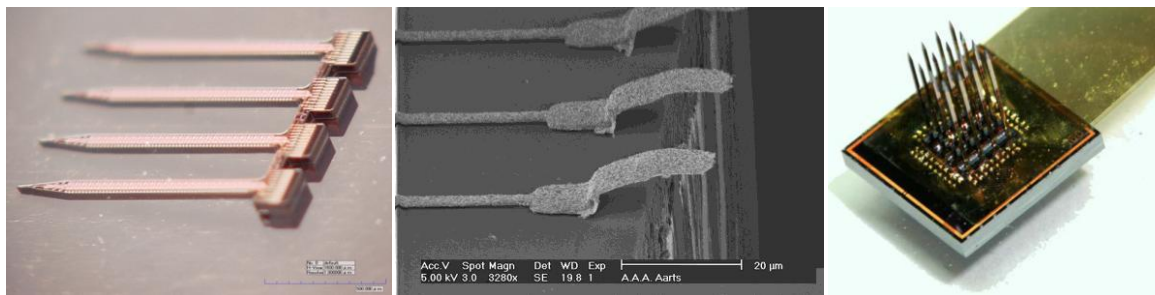


Figure 1-6: 3-D NeuroProbe Project Probe

available wafer thickness. Harrison [13] has developed the interface circuit for the Utah microelectrode array as shown in Figure 1-7.

NeuroProbe Project from Europe [14] developed the 2-D electrode array separately. Using the gold beam lead as shown in the middle in the Figure 1-6, the 2-D electrode array is inserted and bonded on the platform where the analog front-ends is located to process the signal.

However, the cortex penetration of a micro-electrode array results in safety and stability issues due to infection and foreign-body response, which hinders these neural interface systems from being utilized in practical and chronic applications.



Figure 1-8: Electroencephalogram (EEG) System

#### **1.2.4.2 Electroencephalogram (EEG) Recording [15–19]**

As an alternative approach, electroencephalogram (EEG) systems have been widely used for brain-computer interfaces as shown in Figure 1-8. However, the quality of the measured signals by EEG does not satisfy the current neuroscience requirements for successful diagnosis and treatment of central nervous system (CNS) disorders and neural-based prosthetics. A practical compromise between signal fidelity and safety is highly needed in the mentioned areas of research.

#### **1.2.4.3 Electrocorticogram (ECoG) Recording**

Electrocorticography (ECoG) or intracranial EEG (iEEG) is one of the promising techniques for using electrodes on the surface of the cortex or epidural layer to record electrical activity from the cerebral cortex. This method requires a craniotomy to implant the electrode; it is an invasive procedure. ECoG was introduced to treat epilepsy by

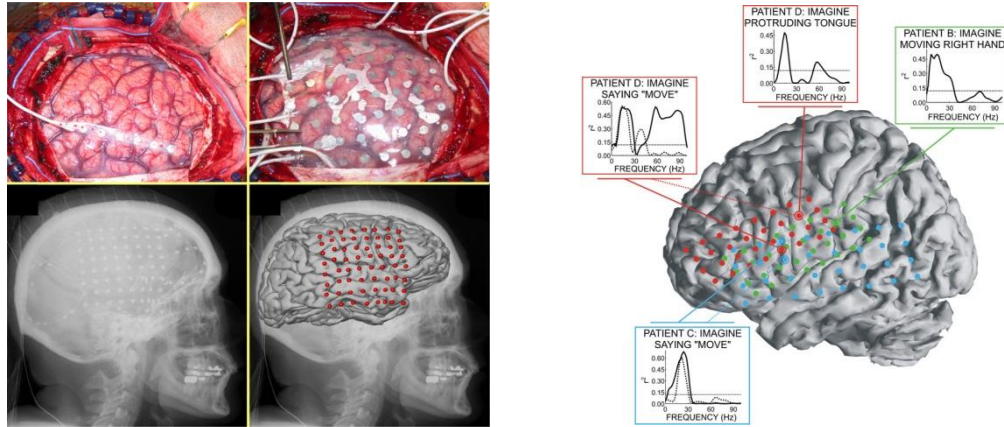


Figure 1-9: Electrocorticogram (ECoG) Recording System from Washington University

neurosurgeons, Penfield and Jasper, in the early 1950s. Recently, ECoG has gained attention as a recording technique by its promising results in brain-computer interfaces (BCI) [20],[21],[22],[23], which are direct neural interfaces that record and extract subjects intention in the form of a neural signal to provide controllability to prosthetic, electronic, or communication devices. In 2004, Daniel Moran from Washington University, St Louis developed a ECoG system and measured the ECoG signal from the human brain for developing a reliable bran-computer interface system as shown in Figure 1-9 [5], [6], [24].

Compared to the previously mentioned penetrating electrode for spike detection and scalp electrode for EEG, ECoG is a promising recording technique using an electrode array or strip placed on the surface of epidural or subdural regions. This method does not penetrate the blood-brain barrier, so it is less invasive than penetrating electrodes. ECoG electrodes are located closer to neurons than EEG electrodes; they can provide more accurate temporal and spatial information.

In order to realize a successful and practical ECoG neural interface system, multiple components need to be realized such as hermetic sealed package, flexible and long-term reliable electrode array, biocompatible and implantable battery or robust wireless

rechargeable system, wireless data transceiver, low-power low-noise analog front-ends, feature extraction algorithm, external device driver, and direct or indirect feedback blocks. Among these components, this work will focus on implementing a neural interface integrated circuit including an analog front-end, a wireless data transceiver, and a stimulator as a direct feedback method for ECoG applications including BCI and epilepsy treatment system.

### **1.3 Design Challenges of ECoG Neural Interface Circuit**

The ECoG brain signals typically have low amplitude ( $< \pm 50 \mu\text{V}$ ) and a relatively low bandwidth ( $< 500\text{Hz}$ ). For the following signal processing, these signals need to be amplified with low-noise amplifier ( $5 \mu\text{V}_{\text{rms}}$ ). Figure 1-10 shows ECoG signal power spectral density from human subject [25]. From the observation, the power spectral density is a function of frequency,  $P(f) \approx f^{-2}$  for  $< 70\text{Hz}$  and  $P(f) \approx f^{-4}$  for  $70\text{Hz} < f < 500\text{Hz}$ . This means that ECoG signals power spectral density decrease as the frequency increases. This feature will be discussed in more detail in Chapter 4. In order to increase an accuracy with high temporal and spatial resolution of this vulnerable brain signals, multiple locations up to 252 electrodes over the large area [26] of the brain need to be monitored simultaneously. To address this issue, a neural interface devices need to have the capability of dealing multi-channel configuration or expanding the number of devices modularly.

From the system point of view, as mentioned earlier, ECoG is an invasive method and needs a craniotomy to place electrodes array and implantable interface system inside the skull. For this reason, once it is implanted, it is desirable for implanted systems to operate



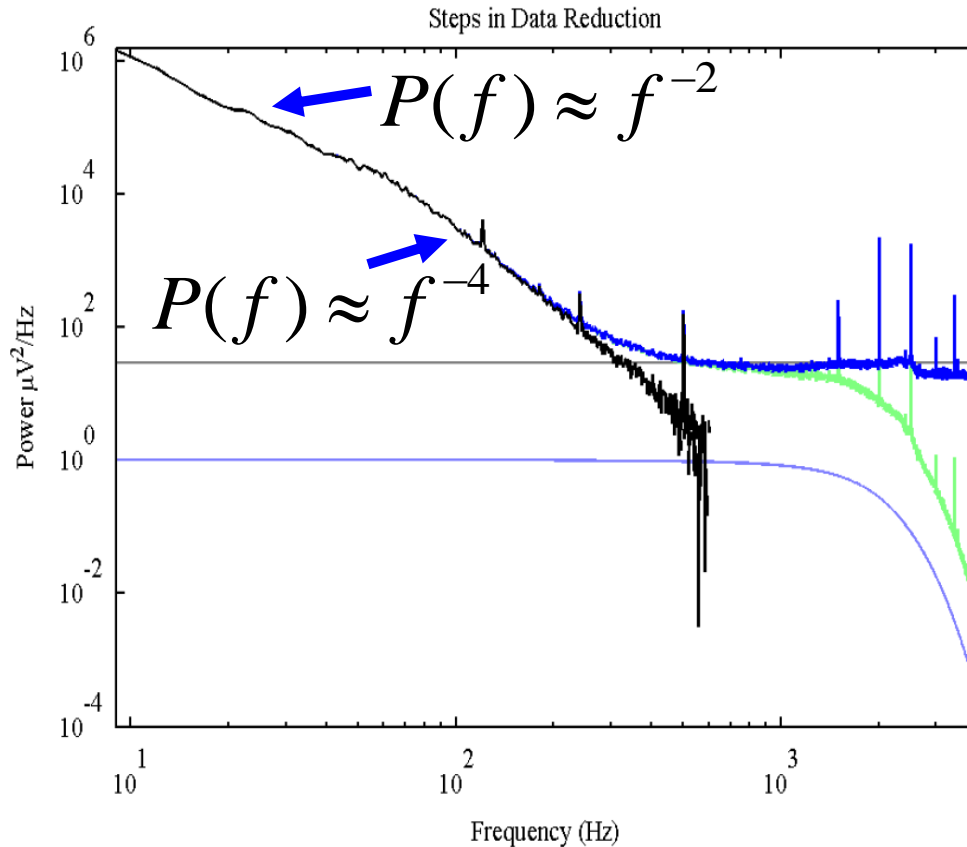


Figure 1-10: ECoG Power Law Scaling Characteristics [25]

for weeks or even for years. To meet this requirement and elongate the lifetime of the system, neural interfaces must consume below  $1\mu\text{W}$  per Channel.

From safety point of view, there should be no transcutaneous connections between implanted devices to external systems in order to prevent any possible infection after implantation. Low-power wireless data transmission and reception is also essential. Also, volume of the implanted system should be miniaturized so that the devices do not cause any harm to the brain tissue or any other organ.

ECoG is a relatively recent research area, and so far, only few groups are working on ECoG interface circuits. In terms of signal similarity, interfacing circuit of EEG [27–31] and local field potential (LFP) from the spike detection system [13], [32–39] can be

utilized to record ECoG signals. However, because EEG is not an implantable system, the power and safety requirements of ECoG differ from those of EEG. Spike detection neural interfaces can be a good solution for ECoG interface circuits, due to the similar power and safety requirements. However, these spike detection neural interface circuits require much high bandwidth ( $< 10\text{kHz}$ ), and corresponding circuits such as analog to digital converter, wireless data transfer speed are optimized for the spike signal characteristics, not for local field potentials, thus ECoG signals characteristics.

Recently, some groups have published implantable interface circuits for ECoG recording with on-chip spectral analysis functionality [40], [41] to provide separate information for different applications such as motion, epilepsy, and depression detection. However, these approaches consume a high power ( $5\mu\text{W/Ch}$ ) which limits possible number of channels and increases the system volume size.

However, implementing a neural interface circuit combining low-power analog front-ends, wireless data transceiver, modular expandability, and stimulation on the same silicon substrate for developing fully functional ECoG-based neural interfaces still presents numerous technical challenges that are yet to be addressed.

#### **1.4 Proposed Research**

As one way of solving the challenges and huddles presented in the previous sections, we proposed a neural interface system: BioBolt minimally invasive ECoG system to treat epilepsy. In this system, instead of high-risk craniotomy, a burr hole can be open and through the hole, we can insert flexible electrode array and the bolt-shaped implanted device, named as BioBolt, is located inside hole. Then, BioBolt will be covered by skin eventually. Due to this bolt-shape, it can be easily implanted and removed. This simple

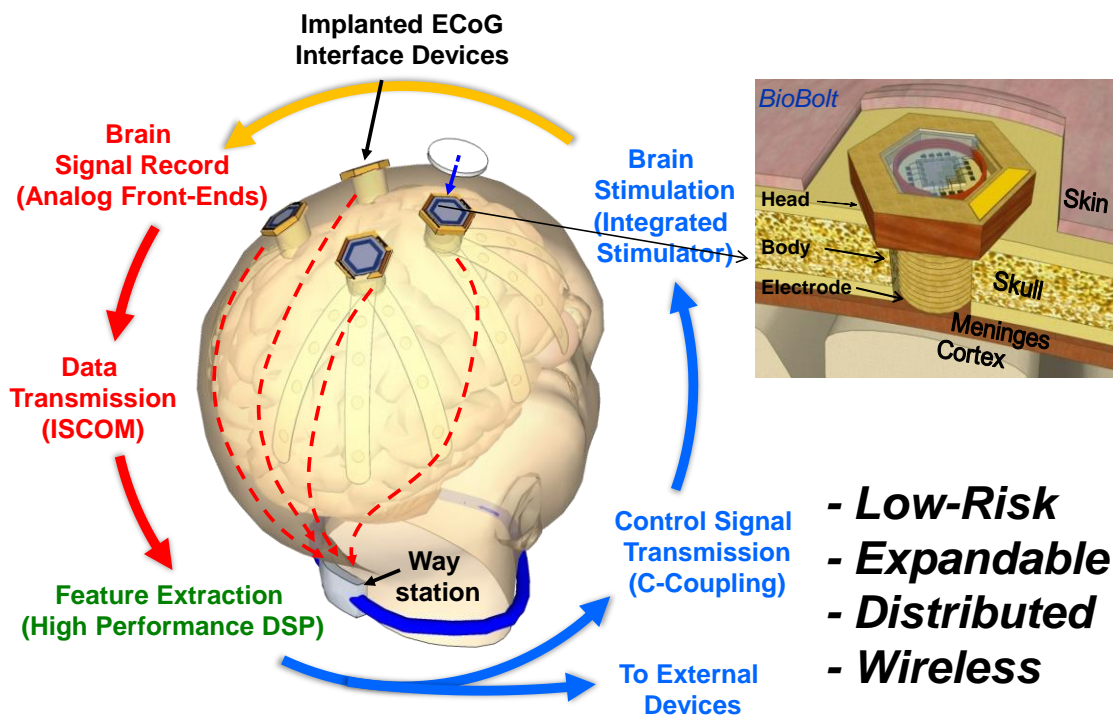


Figure 1-11: Conceptual wireless modular EDSP-assisted closed-loop neural interface system

procedure will be able to reduce the operation time and risk dramatically in the near future. This implanted BioBolt records the brain signal. Then, the signal is transmitted through the skin using a new concept, intra-skin communication. Especially, sending data using ISCOM can reduce the power and form factor significantly by avoiding RF antenna or inductors. Detailed operation of ISCOM will be explained in Chapter 3 and 4. As mentioned, the algorithm is not efficient yet. So, by having an external DSP unit, we can save the power and form factor of BioBolt and the algorithm can be easily upgradable and find the best personalized solution effectively. The extracted command will be back to BioBolt and treat the epilepsy effectively with integrated stimulator.

This conceptual BioBolt has a multiple components inside as shown in Figure 1-12. It has a low-power closed-loop integrated circuit, wireless power source, data link. At the



bottom, it is connected to flexible ECoG electrodes and all the components are hermetically sealed inside the enclosure. Among these components a low-power closed-loop IC and ISCOM are the most critical components, because it determines performance as well as power consumption. Especially, in the implantable system, low-power consumption is more critical because of limited power source and system volume. During my Ph.D. work, I mostly focused on the low-power closed-loop IC and ISCOM to make a great improvement in terms of power.

- *Power and system volume consideration:* For implantable system, power and system volume must be considered simultaneously, because the battery or wireless power transfer unit determines the overall system volume. With SR416SW coin battery (dimension: 4.8x1.6 mm<sup>2</sup>, capacity: 8 mAh), for more than two weeks operation, which is typical monitoring period for an intractable patient in the hospital, the total power consumption must be below 20 μW, or channel power consumption must be below 1 μW.

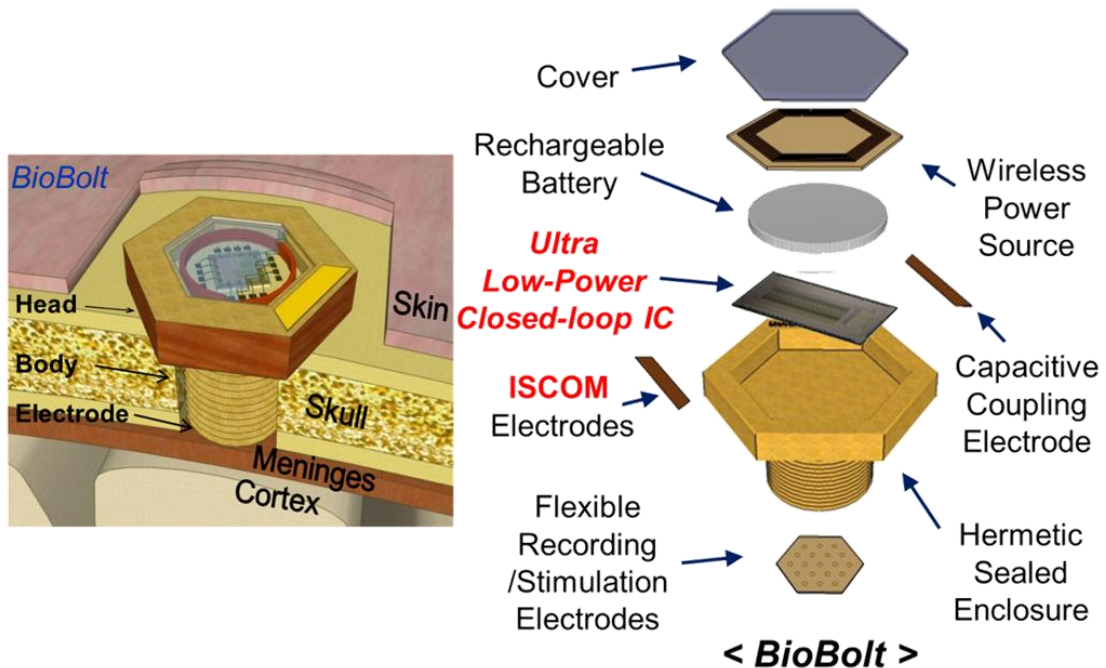


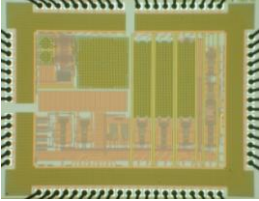
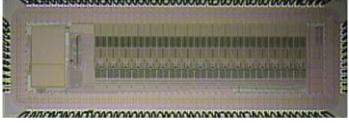
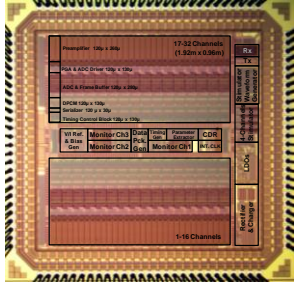
Figure 1-12: Conceptual BioBolt Architecture

Table 1-1: Target Performance Characteristics of the proposed system

<b>Target Performance Characteristics</b>	
<b>Number of Recording Channels</b>	<b>32</b>
<b>Modularity of BioBolt</b>	<b>up to 8</b>
<b>Power Consumption / Channel (Excluding Stimulation Block)</b>	<b>&lt; 1<math>\mu</math>W (1V Analog / 0.5V Digital)</b>
<b>Overall Amplification Factor</b>	<b>40 / 46 / 54 / 60 dB</b>
<b>Preamplifier Bandwidth</b>	<b>0.1Hz ~ 500Hz</b>
<b>System Input Referred Noise</b>	<b>&lt; 5 <math>\mu</math>Vrms (0.01~1kHz)</b>
<b>Input Voltage Range</b>	<b>&lt; <math>\pm</math> 1mV</b>
<b>CMRR / PSRR / Channel Isolation</b>	<b>&gt; 60 dB</b>
<b>ADC Sampling Frequency</b>	<b>&gt; 1kS/s</b>
<b>ENOB (for Av=500, 5<math>\mu</math>Vrms noise)</b>	<b>&gt; 6 bits</b>
<b>Wireless Data Bandwidth</b>	<b>&lt; 400kb/s</b>
<b>Bit Error Rate</b>	<b>&lt; 10<sup>-8</sup></b>
<b>Number of Stimulation Channels</b>	<b>4</b>
<b>Programmable Stimulation Current Output</b>	<b>&gt; 100 <math>\mu</math>A (up to 10mA )</b>

To realize this conceptual system, there are many components to implement and steps to complete. As a first step, an implantable neural interface circuit including low-power analog front-ends, wireless Tx/Rx, and integrated stimulator are implemented. Based on ECoG characteristics and constraints, target performance characteristics have been summarized in Table 1-1. To meet all the requirements, three different ECoG neural interface (ENI) generations are designed, fabricated, and characterized. Key features of each fabricated chips are summarized in the Table 1-2. First approach proposed in 2008 has a single channel preamplifier and analog to digital converter. The recorded data has been successfully transmitted wireless using FM telemetry implemented with off-the-

Table 1-2: Fabricated neural interface integrated chips for this research project

ENI-1	ENI-16	ENI-32
		
<ul style="list-style-type: none"> <li>- 1-Ch Analog Front-End</li> <li>- 1.68<math>\mu</math>W/Ch @2.5V(AFE)</li> <li>- 1.69<math>\mu</math>V<sub>RMS</sub> (0.5~300Hz)</li> <li>- NEF: 2.43</li> <li>- Tx: FM Telemetry using external IC (1.87mW)</li> </ul>	<ul style="list-style-type: none"> <li>- 16-Ch Analog Front-End</li> <li>- 0.63<math>\mu</math>W/Ch @1V(A)/0.5V(D)</li> <li>- 4.26 <math>\mu</math>V<sub>RMS</sub>(1~500Hz)</li> <li>- NEF: 5.2</li> <li>- Tx: ISCOM with FSK (160<math>\mu</math>W)</li> <li>- Modularity: up to 4</li> </ul>	<ul style="list-style-type: none"> <li>- 32-Ch Analog Front-End</li> <li>- 0.12<math>\mu</math>W/Ch @1V(A)/0.5V(D)</li> <li>- 3.26 <math>\mu</math>V<sub>RMS</sub>(0.1~1000Hz)</li> <li>- NEF: 1.05 (inc. ADC noise)</li> <li>- Data Compression (DPCM)</li> <li>- Rx: C-Coupling (BPSK-CEM)</li> <li>- Tx: ISCOM with BPSK (4.6<math>\mu</math>W)</li> <li>- Integrated Stimulator (&gt;100<math>\mu</math>A)</li> <li>- Modularity: up to 8</li> </ul>

shelf components. This version of IC has been assembled with customized and miniaturized package and characterized.

The second expanded version implemented in 2010 is a one-way monitoring neural interface system. It has the capability to record brain signals from 16 channels simultaneously, digitize the signals, modulate it using FSK and BPSK (Manchester code) and transmit the digitized signal wirelessly using intra-skin communication which is a similar approach to Galvanic coupling in the research area of intra-body communication. In this second version, all the peripheral circuits such as clock generator, reference generator, and LDOs are implemented for a fully stand-alone operation without external components.

As the last and complete version, the third interface IC includes thirty-two channels analog front-ends, data compression, low-power transceiver (Tx/Rs), integrated

stimulator for a closed-loop functionality, and modularity. Throughout the thesis, the main features and contributions will be presented in more detail.

## 1.5 Thesis Contributions

The proposed neural interface system has introduced the following contributions/innovations as follows:

- *To optimize neural interface circuit for epidural and subdural Electroencephalogram (ECoGs):* ECoGs could be an alternative signal solution to provide optimized signal integrity and system safety because the microelectrode is close enough to the brain to accurately record brain activity, and the epidural recording method does not penetrate blood-brain barrier, the risk of infection during surgery and experimentation could be reduced substantially.
- *To design and characterize an extreme low-power analog front-end:* a low-noise preamplifier and analog-to-digital converter has been proposed to increase system lifetime.
- *To design and characterize a low-power data compression:* To reduce the data bandwidth for wireless data transfer, this work presents a lossy data compression technique, differential pulse code modulation (DPCM) which is an effective compression method for ECoG signal.
- *To design and characterize a low-power clock and data Recovery circuit:* To realize a low-power clock data recovery circuit, this work utilizes clock-edge modulation for Manchester-encoded signal.

- *To develop and verify a wireless intra-skin communication (WISCOM) system:* WISCOM can transfer data wirelessly through the skin. Using the skin as a conductive media has technical benefits: (i) low-power consumption, (ii) low noise and interference, and (iii) no antennas or coils required for RF wireless communication.
- *To implement a fully programmable stimulator:* the stimulator can provide the most effective stimulation waveform for individual subjects based on the extracted features
- *To integrate implantable peripheral circuits:* To minimize the system volume, all the peripheral circuits such as reference/bias generator, clock generator, and LDOs have been implemented on the same silicon substrate.
- *To design and verify the modular expandable sensor system:* The cluster-based BioBolt system can be expanded to cover a wide spread area of the brain and also is capable of sensing various biopotentials such as temperature and pressure using multiple BioBolts.
- *To verify the system with in-vivo and in-vitro measurement:* Developed recording circuits will be verified by either measuring in-vivo animal ECoG signals or in-vitro head-stages tester unit.

### **1.5.1 Thesis Organization**

The following chapters of this thesis present a detailed design analysis and performance characterization of the proposed wireless nano-watt modular neural interface circuit. They are organized as follows:

- Chapter II presents a single-channel wireless analog front-end with FM telemetry.
- Chapter III presents a sixteen channels wireless modular analog front-end using intra-skin communication (ISCOM)
- Chapter IV presents a thirty-two channel nano-watt modular integrated circuit for closed-loop neural interfaces
- *Chapter V* summarizes final conclusions and highlights contributions of this work, and suggests possible and meaningful further works in this research area.

## **CHAPTER 2**

### **WIRELESS SINGLE CHANNEL NEURAL INTERFACE WITH FM TELEMETRY**

To evaluate and verify the feasibility of neural interface integrated circuit, we designed and implemented the first prototype which consists of a single-channel analog front-end, optimized for low-power and low-noise operation, and utilizes a wireless FM telemetry link. Battery-powered implantable miniaturized neural interface device is also implemented and packaged with the customized enclosure. In this chapter, we will discuss this first generation system in further detail.

#### **2.1 Overall System Architecture**

Figure 2-1 shows overall system architecture of the proposed neural interface IC. The proposed system consists of electrodes, preamplifier, ADC, output driver, FM transmitter, power source, and bias circuit. The blue-colored shape indicates the implantable neural interface enclosure, which is made of Pt and coated with Perlyene for the insulation of the metallic enclosure from the body. The transducer-like electrode that converts ion-based charge variation due to neuron activity into electron-based electrical signals is fabricated using Pt. The amplitude of a typical neural signal is from few  $\mu\text{V}$  to mV. These weak signals are amplified up to a 1 volt range by a low-noise preamplifier and supplied to a voltage controlled oscillator (VCO) for wireless data transmission. All components inside the blue-colored shape are powered by the integrated battery inside the enclosure. In

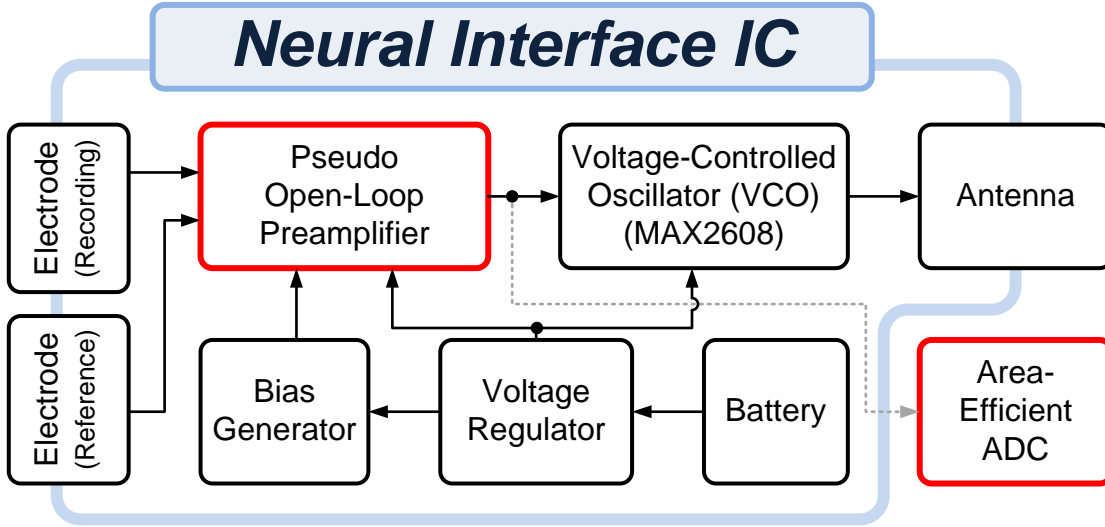


Figure 2-1: Overall Architecture of the Proposed Neural Interface IC

In addition to the above blocks, a low-power SAR analog-to-digital (ADC) was also designed, fabricated, and fully characterized. In this prototype system, this ADC is not included for the prompt prototype implementation. However, the design and characterization of this fabricated SAR ADC will help to optimize the SAR ADC for the next generation neural interface.

The pseudo open-loop amplifier and area-efficient SAR ADC (red-colored blocks in the Figure 2-1) are custom-designed circuit blocks for an optimized system performance and the rest of the blocks are implemented using commercially available components including electrode, VCO, regulator, and antenna. In the following sections, 2.2 and 2.3, the proposed pseudo open-loop preamplifier and area-efficient SAR ADC will be discussed. Sections 2.4 and 2.5 will discuss the wireless FM telemetry and electrode. The implementation and characterization of the prototype system with the fabricated preamplifier and other components will be explained in section 2.6.



## 2.2 Low-Power Low-Noise Pseudo-Open-Loop Preamplifier

Brain activities can be interpreted from the electrical potentials that stem from extracellular neural activities. These potentials can be categorized into four different primary signals according to their sensing locations: single unit action potential (SUAP) from a neuron, local field potentials (LFP) from groups of neurons under the cortex, electrocorticogram (ECoG) on the surface of the cortex, and electroencephalogram (EEG) on the surface of the scalp [42]. SUAP is recorded with signals from 100Hz up to 10 kHz in bandwidth and  $\pm 500$   $\mu\text{V}$  in amplitude, while LFPs have amplitudes of  $\pm 500$   $\mu\text{V}$  and frequency up to 200 Hz. The ECoG and EEG potentials exhibit amplitudes ranging from 1  $\mu\text{V}$  to 100  $\mu\text{V}$  and bandwidth up to 200 Hz. In this range, the thermal and 1/f noise as well as interferences from the cell-electrode interface can severely interfere with neural potentials. Because these neural potentials are vulnerable to external interferences such as drift/offset from the cell-electrode interface and power line noise, analog signal processing functions such as amplification and signal filtering is critical for a reliable interface.

Many analog front-end preamplifier circuit techniques have been investigated to achieve low-power low-noise performance. The design strategy of the operational transconductance ( $g_m$ ) amplifiers (OTAs) in the majority of previous works [18], [34], [43–53] is to maximize  $g_m$  of the input transistors for noise-power efficiency, and to minimize  $g_m$  of the rest of the transistors in the OTA to lower their noise contribution. Based on this strategy, the input transistors are operating in the weak inversion region where their efficiency ( $g_m/I_D$ ) is maximized. To minimize  $g_m$  of the rest of the transistors, [43] operates the transistor in the strong inversion region, and [34], [44] utilize the source

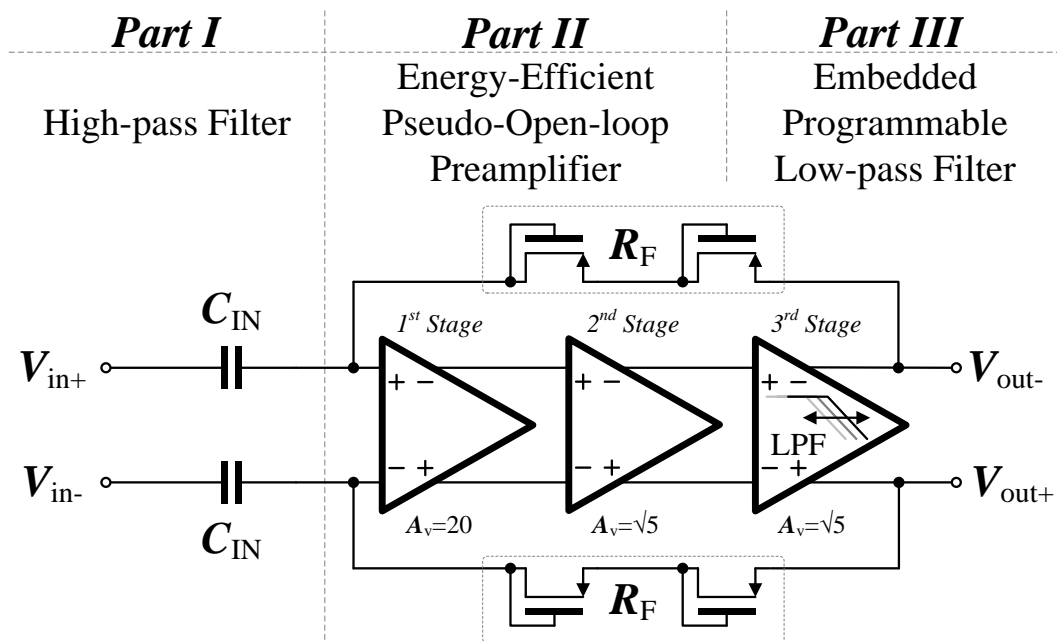


Figure 2-2: Overall system schematic of the pseudo-open-loop preamplifier for the neural applications.

degeneration technique to reduce  $g_m$  of the rest of transistors further. In addition, the class AB topology [47], [48] is also proposed to increase the effective  $g_m$  of the input transistors. With these optimized OTAs, most preamplifiers described in previous research are configured by using capacitive feedback to achieve precise gain.

To achieve a better power-noise performance than the closed-loop topology, [54] has proposed a DC-coupled fully-differential open-loop preamplifier with four-stage topology for the temperature-frequency converter. However, this open-loop preamplifier requires a common-mode feedback (*CMFB*) circuit and large external components, and is not optimized for neural application. For neural applications, [55] has also proposed an open-loop preamplifier for better power-noise performance. Even though it shows better noise-power performance for a given power budget, this amplifier, however, still suffers

from low linearity, imprecise gain, and low PSRR due to the lack of a differential signal path.

In this work, we propose a low-power low-noise fully-differential pseudo-open-loop preamplifier with programmable bandwidth. By using pseudo-open-loop topology, the proposed preamplifier can achieve high power-noise efficiency as well as high linearity and precise gain control. The proposed fully-differential preamplifier can balance the common-mode of the differential outputs without a *CMFB* circuit, and bias the AC-coupled input transistors without an external reference. By using a current-ratio gain design technique, this proposed preamplifier achieves a stable gain over process and bias variations. We have also implemented a programmable embedded  $g_m$ -*C* low-pass filter (*LPF*) whose cut-off frequency can be tuned by the transconductance in the output stage so that the proposed preamplifier can be configured to be used in recording single neuron spikes or field potentials (*EEG*, *ECoG*).

This section is organized as follows. Section 2.2.1 describes the overall system architecture. In section 2.2.2, the low-power low-noise design principles with noise analysis of the proposed amplifier is presented. Results of test-bench chip characterization and in-vivo measurement are presented in Section 2.2.3, and Section 2.2.4 concludes the section.

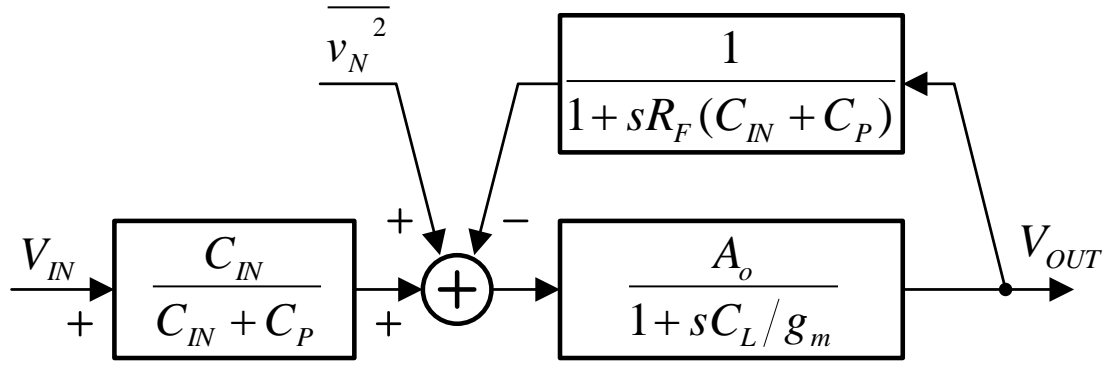
### **2.2.1 Overall System Architecture**

Overall architecture of the proposed preamplifier is shown in Figure 2-2. This proposed pseudo open-loop preamplifier consists of three parts.

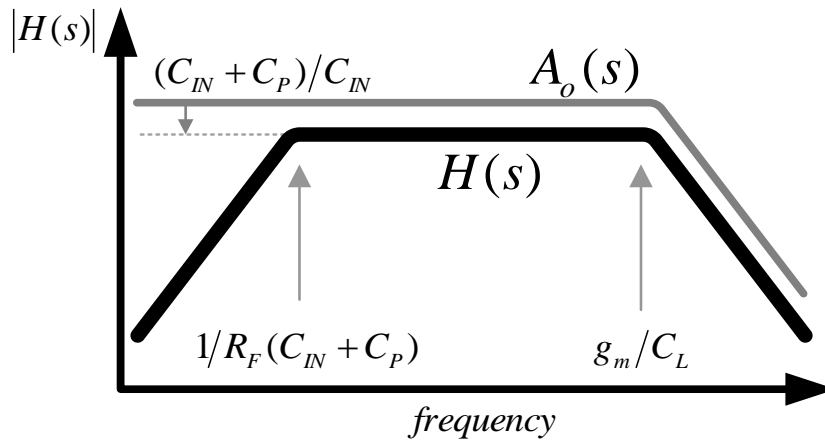
In Figure 2-2, part I, a high-pass filter, formed by  $C_{IN}$  and MOS-bipolar transistor ( $R_F$ ) [56], is implemented prior to the OTA. This rejects the interference from the cell-

electrode interface that could easily saturate the preamplifier due to its amplitude up to hundreds of mV [44]. By utilizing a MOS-bipolar transistor the low-frequency high-pass cutoff corner is set to be below 0.5 Hz. In part II, we develop a low-power low-noise fully-differential pseudo-open-loop preamplifier. One of the main concerns in designing open-loop amplifiers is setting the gain reliably and accurately. To achieve accurate gain control, a diode-connected load is used at each stage. This diode-connected load can provide two additional features in addition to gain control: eliminating a CMFB circuit in the fully-differential structure, and biasing the input transistor in the AC-coupled structure. Because the diode-connected load at output nodes will generate stable voltage set by the bias current, the common-mode voltage from the differential output nodes can be self-balanced without help from a complex CMFM circuit. The self-generated voltage from the output node can be connected to the input transistor through the feedback path using a MOS-bipolar transistor to supply bias voltage as shown in Figure 2-2. This feedback path through the  $R_F$  acts as a unit-gain feedback to provide the bias voltage in only the very low frequency region, because it forms a low-pass filter with  $C_{IN}$  and  $C_p$ , and  $R_F$ , where the feedback factor,  $\beta$ , can be given as  $1/(1+sR_F(C_{IN}+C_p))$ .

For low-power and low-noise performance, the transistors in the first stage are operating in the weak-inversion region, while transistors in the following stages are in the strong inversion region. Here we need to mention that if we design the following stages (2<sup>nd</sup> and 3<sup>rd</sup>) with only one stage, it would be simple to implement and consume less power. However, this strategy will increase the required chip area exponentially as the gain increases. To compromise this area-gain constraint, we split the following stage into two stages.



(a) Block diagram of signal flows



(b) Ideal transfer function

Figure 2-3: Block diagram and ideal transfer function of the pseudo-open-loop preamplifier

In part III, in order to eliminate any undesirable noises above the cut-off corner as well as unwanted power consumption, we implemented a bandwidth-programmable *LPF* using output impedance ( $1/g_m$ ) of the third stage and output load capacitor ( $C_L$ ) as an embedded  $g_m$ - $C$  *LPF*. By adjusting the bias current, thus the transconductance, the preamplifier can be configured to have flexible bandwidths for various applications.

The overall transfer function of the proposed preamplifier can be derived using the signal flow shown in Figure 2-3 (a). From the block diagram, we can easily derive the transfer function:

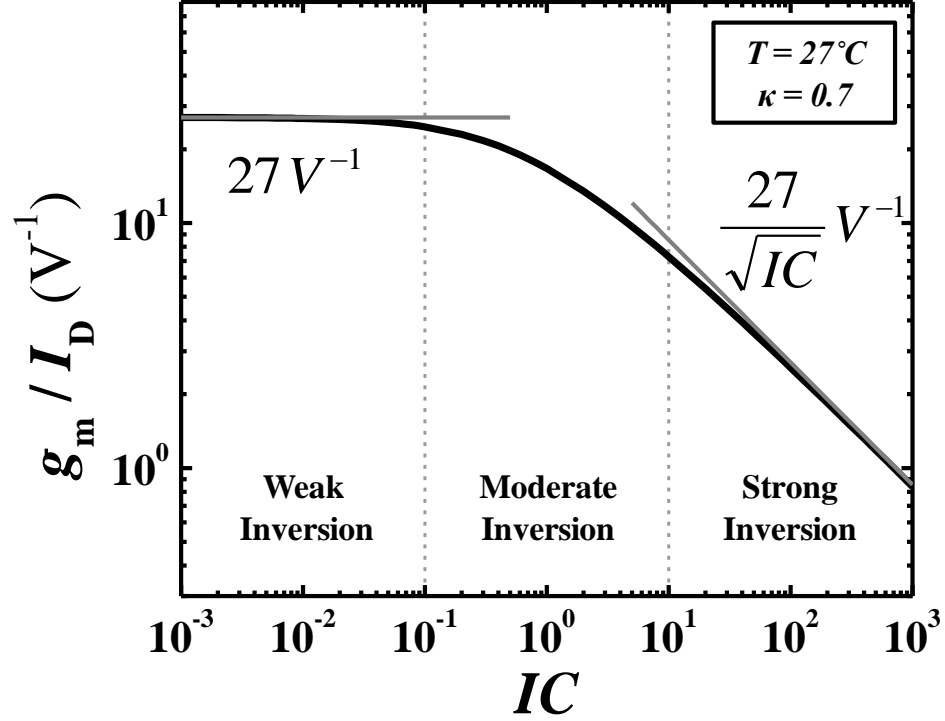


Figure 2-4: Transistor efficiency according to the operating regions

$$|H(s)| = \underbrace{\left( \frac{C_{IN}}{C_{IN} + C_P} \right)}_{\text{Attenuation}} \cdot \underbrace{\left( \frac{sR_F(C_{IN} + C_P)/A_o}{1 + sR_F(C_{IN} + C_P)/A_o} \right)}_{\text{High Pass Corner}} \cdot \underbrace{\left( \frac{1}{1 + sC_L/g_m} \right)}_{\text{Low Pass Corner}} \cdot A_o \quad \text{Eq. 2-1}$$

where  $A_O$  is the open-loop gain of the proposed OTA discussed in the following section. As shown in equation Eq. 2-1, the proposed preamplifier operates as a band-pass amplifier whose mid-band gain is attenuated from  $A_O$  by  $(C_{IN}+C_P)/C_{IN}$  because of the capacitive voltage divider effect. The corner frequencies,  $\omega_{HP}$  and  $\omega_{LP}$ , are set by  $1/R_F(C_{IN}+C_P)$  and  $g_m/C_L$ , respectively. From this analysis, we can notice the proposed preamplifier operates as an open-loop amplifier above  $\omega=1/R_F(C_{IN}+C_P)$ . The ideal transfer function is illustrated in Figure 2-3 (b).

Using the block diagram, we can also estimate the input-referred noise power of the system as

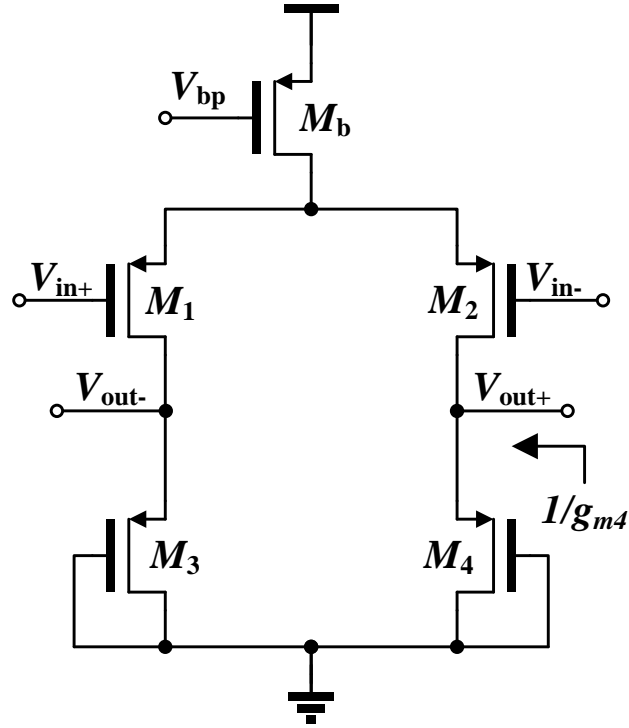


Figure 2-5: Conventional Diode-Connected Load Topology with PMOS input stage

$$\overline{v_{n,preamp}^2} = \left( \frac{C_{IN} + C_P}{C_{IN}} \right)^2 \cdot \overline{v_{n,OTA}^2} \quad \text{Eq. 2-2}$$

In this equation, in order to minimize the noise power of the preamplifier, we need to increase  $C_{IN}$  or decrease the input-referred noise power of the OTA. In this design we will focus on optimizing the noise power in OTA rather than increasing  $C_{IN}$  to minimize chip area.

### 2.2.2 Low-Power Low-Noise OTA Design

To optimize the noise and power performance of the proposed OTA, it is important to consider transconductance and efficiency. In this section, we will derive transconductance ( $g_m$ ) and discuss its energy efficiency ( $g_m/I_D$ ) using the EKV model [57]; then, the optimization of the OTA will be discussed.

### 2.2.2.1 Transconductance ( $g_m$ ) in All Regions

Transconductance in OTA is the most important parameter in determining the overall performances such as gain, noise, and bandwidth. However, because of the nonlinearity of transistors,  $g_m$  changes for the weak, moderate, and strong inversion regions. To determine the operating region of the transistor, we can compare the drain current ( $I_D$ ) with the moderate inversion characteristic current ( $I_S$ ) [58] which is given by

$$I_S = \frac{2\mu C_{ox} U_T^2}{\kappa} \cdot \frac{W}{L}, \quad \text{Eq. 2-3}$$

where  $U_T$  is the thermal voltage, and  $\kappa$  is the subthreshold gate capacitive coupling coefficient ( $\approx 0.7$ ). The ratio of  $I_D$  to  $I_S$ , the inversion coefficient  $IC$  [57], can be expressed as

$$IC = I_D / I_S = \frac{\kappa}{2\mu C_{ox} U_T^2} \cdot \frac{I_D}{W/L}. \quad \text{Eq. 2-4}$$

Based on this inversion coefficient, the operating regions of the transistor can be determined in three different inversions regions [59]: (1) weak inversion for  $IC < 0.1$ , (2) moderate inversion for  $0.1 < IC < 10$ , and (3) strong inversion for  $10 < IC$ . In the viewpoint of the circuit designer, we can choose the drain current level and/or the aspect ratio of the transistor to set the transistor operating region. Using the EKV model, we can derive the transconductance, which is valid in all operating regions, as follows:

$$g_m \approx \frac{\kappa I_D}{U_T} \frac{2}{1 + \sqrt{1 + 4 \cdot IC}}. \quad \text{Eq. 2-5}$$

We can also estimate the efficiency of the transistor [43] by normalizing the transconductance with the drain current,  $g_m/I_D$ . As shown in Figure 2-4, we can easily notice that the efficiency increases as the inversion coefficient decreases. With  $\kappa=0.7$  and  $T=27^\circ\text{C}$ , we can simplify the  $g_m/I_D$  for the three different inversion regions as follows:



$$\frac{g_m}{I_D} \approx \begin{cases} 27 & \text{for weak inversion} \\ 54 / (1 + \sqrt{1 + 4 \cdot IC}) & \text{for moderate inversion} \\ 27 / \sqrt{IC} & \text{for strong inversion} \end{cases} \quad \text{Eq. 2-6}$$

In the weak inversion region, the transistors are most efficient with saturated efficiency ( $\approx 27V^{-1}$ ), while in the strong inversion region, the transistors are least efficient with decreasing efficiency by a factor of  $27/\sqrt{IC}$ .

### 2.2.2.2 Low-Noise Low-Power OTA for Accurate Open-Loop Gain

1) *Gain with Diode-connected Load:* As mentioned earlier, gain accuracy is one of the main concerns in designing an open-loop amplifier. To achieve accurate open-loop gain, the diode-connected load is used in each stage as shown in Figure 2-5. The gain of the conventional topology (in Figure 2-5) can be expressed as

$$A_o = \frac{g_{m1}}{g_{m3}} = \frac{\kappa_1 I_{D1} / U_T}{\kappa_3 I_{D3} / U_T} \cdot \frac{1 + \sqrt{1 + 4 \cdot IC_3}}{1 + \sqrt{1 + 4 \cdot IC_1}} \quad \text{Eq. 2-7}$$

To minimize any possible process variation of  $\kappa$ , we can use the same type transistor for both input ( $M_{1,2}$ ) and load ( $M_{3,4}$ ) transistors. In our design, we use PMOS transistors, because PMOS transistors have less  $1/f$  noise than NMOS transistors. Then, we can rewrite Eq. 2-7 depending on the operation regions as follows:

$$A_o = \begin{cases} \frac{I_{D1}}{I_{D3}} & \text{for weak inversion} \\ \frac{I_{D1}}{I_{D3}} \cdot \frac{\sqrt{IC_3}}{\sqrt{IC_1}} = \frac{I_{D1}}{I_{D3}} \cdot \frac{\sqrt{(W/L)_3}}{\sqrt{(W/L)_1}} & \text{for strong inversion} \end{cases} \quad \text{Eq. 2-8}$$

From this equation, we can conclude that the gain of the diode-connected load topology is set by the current ratio for the weak inversion region, and by the aspect and current ratio for the strong inversion region.

2) *First Gain Stage in Weak Inversion:* the schematic of the proposed diode-connected load is shown in Figure 2-6. From the noise analysis in section 2.2.2.3, the

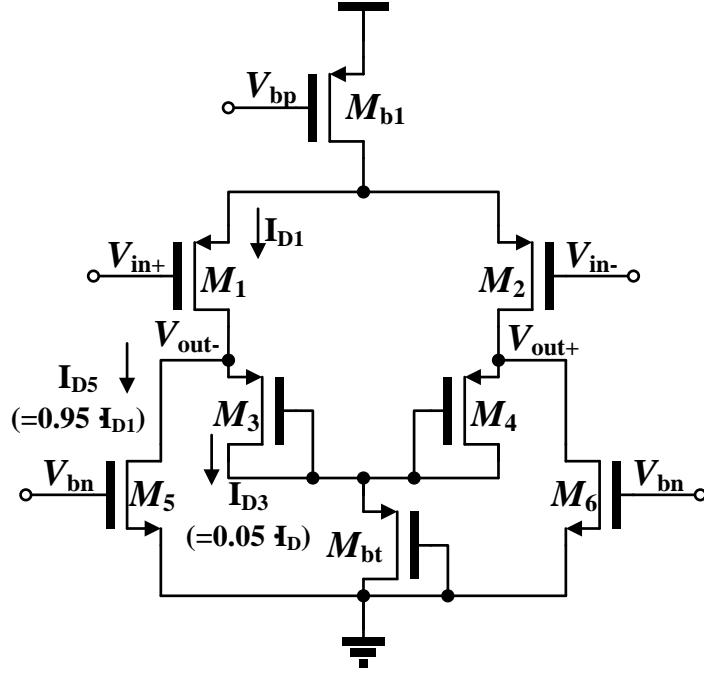


Figure 2-6: Proposed Diode-Connected Load Topology

transistors in the first stage are operating in weak inversion for energy efficiency. To achieve high power-noise performance, most of the power is allocated for the first stage as  $I_{1st}:I_{2nd}:I_{3rd}=10:1:1$ . The gain of the first stage is set to be 20 by the current ratio that is controlled by the current steering transistors ( $M_{5,6}$ ) based on the analysis in section 2.2.2.3, and it can be expressed as

$$A_{o1} = \frac{g_{m1}}{g_{m3}} = \frac{I_{D1}}{I_{D3}} = 20 \quad \text{Eq. 2-9}$$

One concern in this topology is that the output common-mode voltage level ( $V_{GS_{3,4}}$ ) is below the threshold voltage and is too low for proper biasing of the following stages, because the  $M_{3,4}$  are operating in the subthreshold region with low drain current. To ensure proper operation, we use a bootstrapping transistor ( $M_{bt}$ ) to boost the common-mode output voltage of the first stage.

3) *Second and Third Gain Stage in Strong Inversion:* in the following stage, we use the conventional diode-connected load operating in strong inversion to minimize its noise

contribution, as shown in Figure 2-5. In designing the following stage, we might be able to achieve the required gain of 5 with only one stage. However, this strategy will increase the required chip area exponentially as the gain increases. To compromise this area-gain constraint, we might use the current steering technique to alleviate the area burden as the first stage. However, this approach requires an accurate current source which might be difficult to implement at the current level of a few nano amperes. Because of this constraint, we split the following stage into two. And, this splitting strategy saves the area by a factor of 2.5 for a gain of 5 ( $\sqrt{5}$  for each stage) with negligible bias current increment of about 30nA.

4) *Embedded Programmable Low-Pass Filter*: as shown in Figure 2-5, the output impedance of each stage equals  $I/g_m$  due to the diode-connected load, and can be easily controlled by changing the bias current. Especially at the third stage, we can realize an embedded programmable low-pass  $g_m$ - $C$  filter using the output impedance ( $I/g_m$ ) and load capacitance ( $C_L$ ). We need to mention that the change of the bias current in the third stage shifts only the bandwidth while keeping the gain intact, because the gain of the third stage is set by the aspect ratio rather than the current, as shown in Eq. 2-8.

### **2.2.2.3 Noise Analysis**

The neural potentials have typical signal amplitudes below the mV range. To properly process these weak signals, the front-end preamplifier should lower its own generated noise to achieve a high signal-to-noise ratio (SNR). In this section, we will analyze the noise performance of the proposed OTA and derive the design criteria for a low-power design. For simplicity, we will consider only thermal noise sources, while the flicker noise, which is another significant noise source, will be discussed in the following section.

Table 2-1: Operating Point of Transistors for the Proposed Preamplifier

Devices	Type	W/L	IC	Inversion Region	$g_m$	$g_m/I_D$
$M_1, M_2$	p	200/1	0.02	Weak	4.43	26.86
$M_3, M_4$	p	12/2	0.03	Weak	0.22	26.55
$M_5, M_6$	n	1/100	67.84	Strong	0.49	3.12
$M_7, M_8, M_{11}, M_{12}$	p	1/20	7.34	Strong	0.14	8.40
$M_9, M_{10}, M_{13}, M_{14}$	p	1/100	36.72	Strong	0.07	4.16
$M_{bt}$	p	4/2	0.18	Weak	0.39	23.60
$M_{b1}$	p	20/20	7.34	Strong	2.77	8.40
$M_{b2}, M_{b3}$	p	2/20	7.34	Strong	0.28	8.40

Furthermore, the noise sources from the first stage only will be analyzed, because the effect of the other noise sources from the following stages is negligible due to the high gain of the first stage.

To analyze the effect of the thermal noise sources, we can model the thermal current noise of the MOSFET as

$$\overline{i_{no,thermal}^2} = 4\gamma kTg_m, \quad \text{Eq. 2-10}$$

where  $\gamma = 2/3$  for the strong inversion region and  $\gamma = 1/(2\kappa)$  for the weak inversion region, respectively. Then, from this thermal current noise model, we can derive the total input-referred thermal noise generated by the proposed OTA and can rewrite it by assuming  $IC_1 \ll 1$  and  $IC_5 \gg 1$ , which can be expressed as

$$\begin{aligned} \overline{v_{ni,total}^2} &= \frac{4kT}{\kappa_p \cdot g_{m1}} \left( 1 + \frac{g_{m3}}{g_{m1}} + \frac{4\kappa_p}{3} \cdot \frac{g_{m5}}{g_{m1}} \right) \\ &\approx \frac{4kT}{\kappa_p \cdot g_{m1}} \left( 1 + \frac{1}{A_{o1}} + \frac{4\kappa_n}{3} \cdot \frac{1}{\sqrt{IC_5}} \right), \end{aligned} \quad \text{Eq. 2-11}$$

where  $\kappa_p$  and  $\kappa_n$  are the subthreshold gate capacitive coupling coefficients for PMOS and NMOS transistors, respectively.

As shown in Eq. 2-11, in order to minimize the noise effect at the input of the OTA, we should increase three design parameters: (1) the transconductance of the input transistor ( $g_{m1}$ ), (2) the gain of the first stage ( $A_{o1}$ ), and (3) the inversion coefficient of the current steering transistor,  $M_5$  ( $IC_5$ ). First, we can maximize  $g_{m1}$  by using the transistor in the weak inversion region where the transistor is most energy-efficient for a given power budget. On the other hand, the rest of the transistors can be operated in the strong inversion region to minimize their noise contribution. Second, we can increase  $A_{o1}$  by raising the steering current up to  $I_{D1}$ . However, implementing an accurate current mirror in the level of the nano amperes is challengeable, and the excessively high gain of the first stage may saturate the following stages. Last, we can increase  $IC_5$  by decreasing the aspect ratio of the  $M_5$  ( $W/L_5$ ) as shown in (4). The excessively small  $W/L_5$ , however, will need  $V_{GS5}$  above the supply voltage to provide the current to maintain the required gain. From these noise analyses of the proposed OTA, we set the gain of the first stage to be 20 and the aspect ratio of the current steering transistor to be 1/100. The simulation results show that the input-referred noise of the proposed preamplifier is  $78.4\text{nV}/\sqrt{\text{Hz}}$  with  $I_{TOTAL}=400\text{nA}$ .

The operating point and dimensions of the transistors for the proposed pseudo-open-loop preamplifier are summarized in Table 2-1.

#### **2.2.2.4 Noise Efficiency Factor**

To evaluate the noise-power efficiency, we can estimate the noise efficiency factor (NEF) which is introduced in [60] and given by

$$NEF = V_{ni,rms} \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}}, \quad \text{Eq. 2-12}$$

where  $BW$  is the frequency bandwidth,  $I_{tot}$  is the total current drain in the system, and  $V_{ni,rms}$  is the total input-referred noise. This NEF compares the total input-referred noises of the proposed neural amplifier with that of an ideal bipolar transistor which is given by

$$\overline{v_{ni,bipolar}^2} = \frac{4kT \cdot U_T}{I_{tot}} \quad \text{Eq. 2-13}$$

Assuming a typical value of  $\kappa=0.7$ , we can rewrite Eq. 2-12 using Eq. 2-11 and Eq. 2-13 as follows:

$$NEF = \sqrt{\frac{\overline{v_{ni,total}^2}}{\overline{v_{ni,bipolar}^2}}} \approx 2 \cdot \sqrt{\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m5}}{g_{m1}}\right)} \quad \text{Eq. 2-14}$$

Using Eq. 2-14, we can estimate the theoretical NEF of the proposed preamplifier to be 2.16.

In addition, to simplify designing a neural amplifier, we may generalize Eq. 2-14 as

$$NEF_{simple} = F_{topology} \cdot \sqrt{\left(1 + \frac{\alpha_1}{g_{m1}} + \frac{\alpha_2}{g_{m1}} + \dots\right)}, \quad \text{Eq. 2-15}$$

where  $F_{topology}$  is a factor depending on the topologies: 1 for single input and 2 for differential input, and  $\alpha_n$  is a n-th device parameter:  $g_m$  for transistors and  $I_4/R$  for resistors. This simplified approach provides an estimate of NEF in initial phases of the design or characterization.

### 2.2.2.5 Current Steering Circuit and its Mismatch

As shown in Figure 2-7, we implemented a current steering circuit to set the gain of the first stage by generating the current ratio between the input and load transistors. In order to achieve an accurate gain, the current mismatches in the current steering transistors,  $\Delta I_1$  from  $M_{b1}$ - $M_{st1}$  and  $\Delta I_2$  from  $M_{st2}$ - $M_5$ , need to be minimized. For low-noise

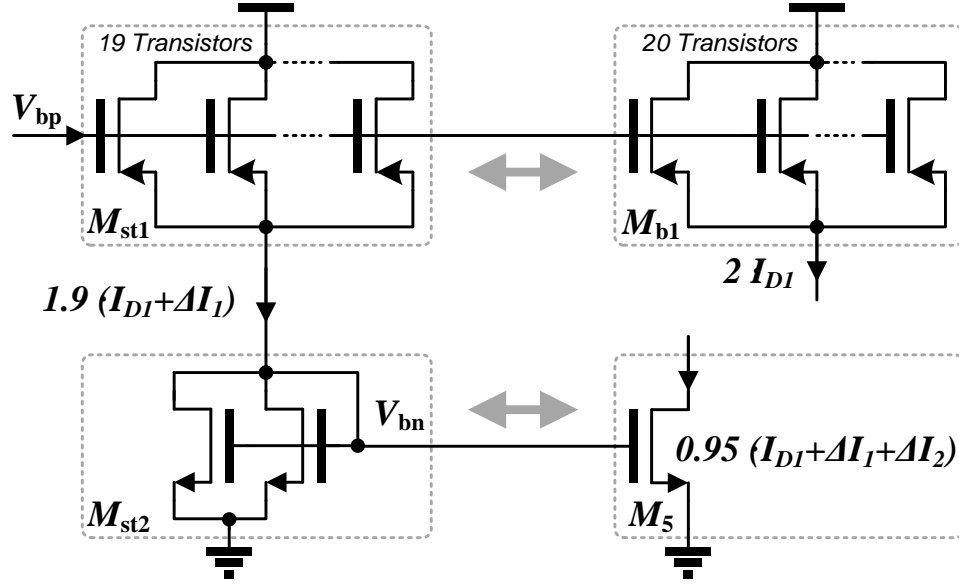


Figure 2-7: Current-steering circuit and its bias circuit for mismatch analysis

operation as mentioned in Section 2.2.2.3, all transistors in the current steering circuit are operating in the strong inversion region. For the following analysis, we can express the drain current as

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \quad \text{Eq. 2-16}$$

where  $\lambda$  is the channel modulation coefficient. The current mismatch between transistors can be determined by three parameters: (1) the gate dimension mismatch  $\Delta(W/L)$ , (2) the threshold voltage mismatch  $\Delta V_{TH}$ , (3) and the channel length modulation ( $V_{DS}$  and  $\lambda$ ), and can be expressed as follows:

$$\Delta I = \frac{\partial I_D}{\partial (W/L)} \Delta \left( \frac{W}{L} \right) + \frac{\partial I_D}{\partial (V_{TH})} \Delta V_{TH} + \frac{\partial I_D}{\partial (V_{DS})} \Delta V_{DS} \quad \text{Eq. 2-17}$$

As for the  $\Delta I_1$ , the current mismatch from the several unit transistors of  $M_{b1}$  and  $M_{st1}$  is averaged out and will be negligible. In this analysis, we consider only the dominant current mismatch,  $\Delta I_2$ , between  $M_{st2}$  and  $M_5$ . Because  $\Delta(W/L)$  is inversely proportional to the area of the transistor, we can assume  $\Delta(W/L)$  is negligible due to its large area

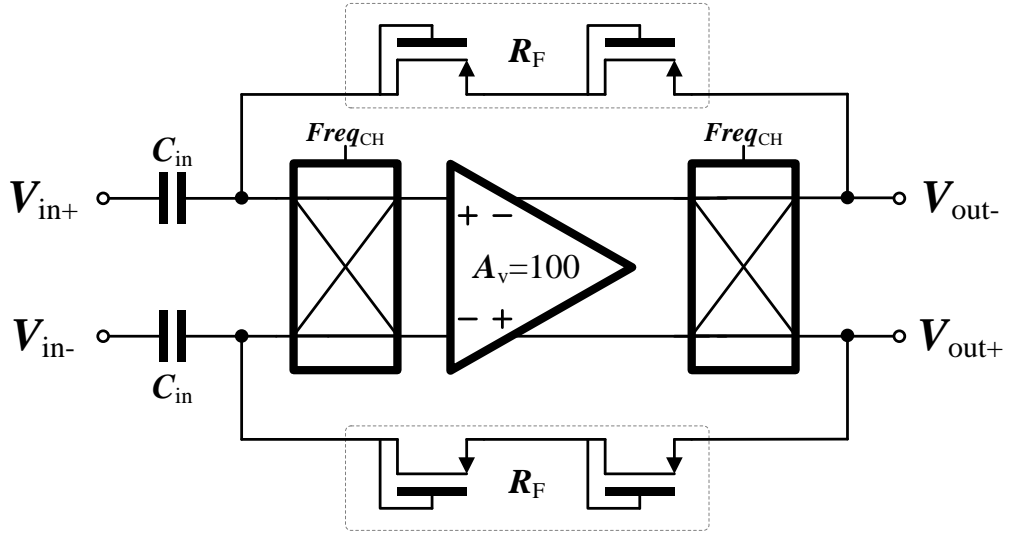


Figure 2-8: Chopper stabilized preamplifier

( $\approx 100\mu\text{m}^2$ ). To derive design criteria, we can normalize the current mismatch using Eq. 2-16 and Eq. 2-17 as

$$\frac{\Delta I_2}{I_D} = -\frac{2 \cdot \Delta V_{TH}}{V_{GS} - V_{TH}} + \frac{L - L'}{L} \cdot \Delta V_{DS}, \quad \text{Eq. 2-18}$$

where  $L'$  is the effective channel length due to the channel length modulation. In Eq. 2-18, the current mismatch can be minimized by increasing the length of the transistor and the overdrive voltage ( $V_{GS} - V_{TH}$ ). Because the  $V_{DS}$  output of the first stage changes by hundreds of mV, the effect of  $V_{DS}$  must be minimized by increasing the transistor length. For this reason, the transistor size is designed to be  $W/L = 1\mu\text{m}/100\mu\text{m}$  and the overdrive voltage to be over 700mV.

#### 2.2.2.6 1/f Noise Reduction by Chopper Stabilization

In addition to thermal noise, 1/f (or flicker) noise severely interferes with the low-frequency neural signals in EEG and ECoG applications. To reduce the flicker noise, we used large PMOS transistors ( $W/L = 200\mu\text{m}/1\mu\text{m}$ ) in the first stage. However, we still



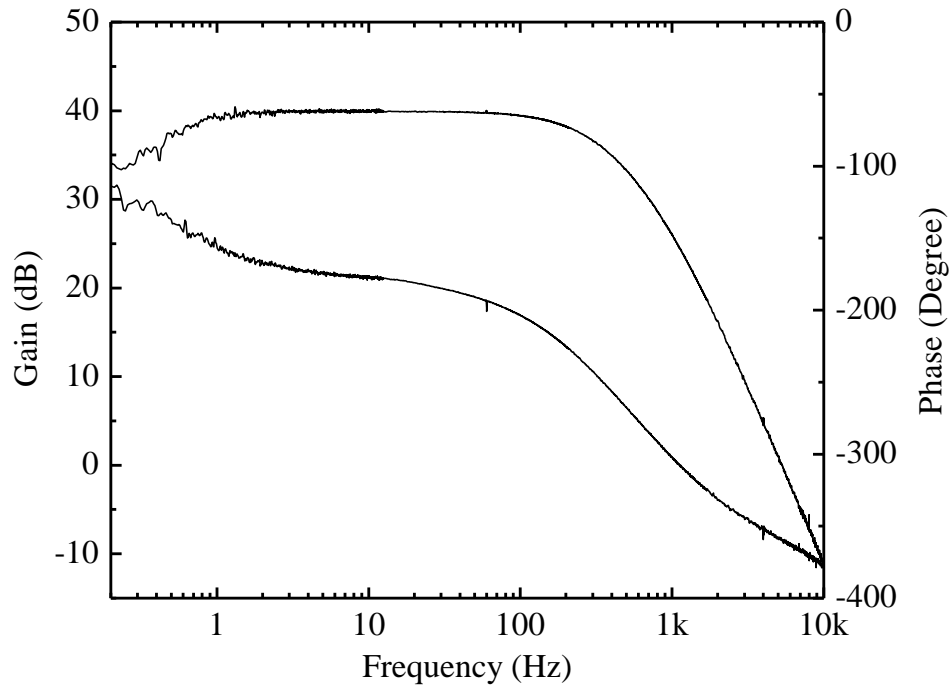


Figure 2-9: Measured transfer function of the preamplifier configured to consume 400nA and 2.5V

have relatively large  $1/f$  noise. To suppress it even further, we utilize a chopper stabilization technique as shown in Figure 2-8.

### 2.2.3 Measurement Results

The fabricated preamplifier using  $0.25\mu\text{m}$  1P5M CMOS process is measured in this section. Test-bench and *in-vivo* measurement of the chip have been performed for the characterization and the verification, respectively.

#### 2.2.3.1 Test-Bench Chip Characteristics

Figure 2-9 shows the measured gain and phase frequency response of the fabricated pseudo-open-loop preamplifier from 0.2 Hz to 1 kHz when the preamplifier is configured to consume 400nA at 2.5 V supply. At this configuration, the measured gain and phase at

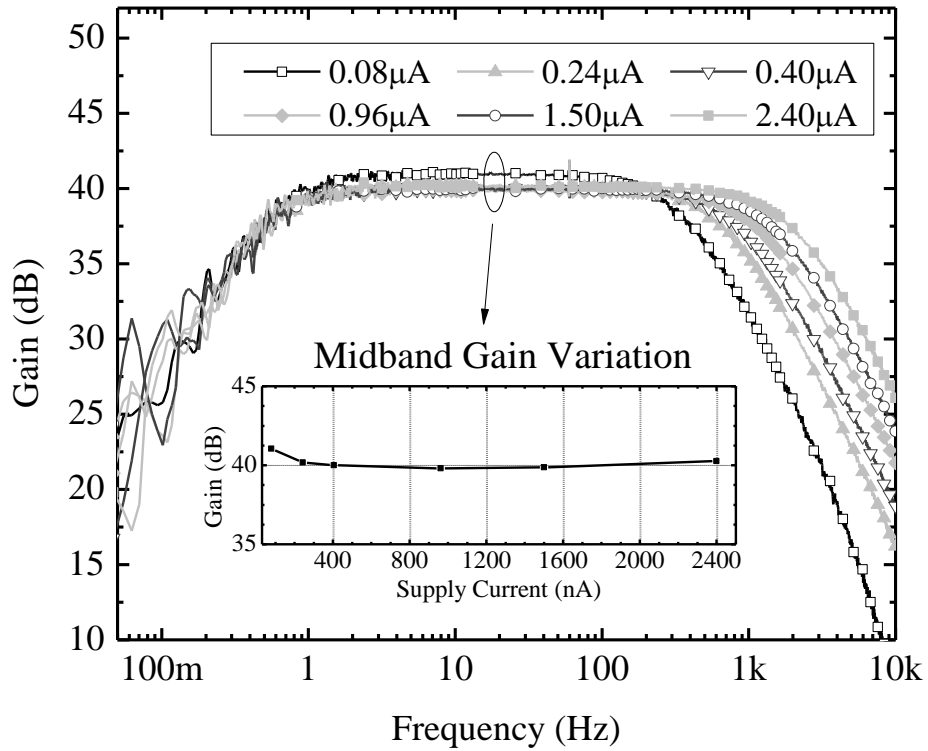


Figure 2-10: Transfer function and mid-band comparison under various bias conditions

the mid-band are 39.95dB and -180 degrees due to the three-stage structure, respectively. And, at the high frequency range above 2 kHz, the phase of the transfer function approaches -360 degrees; the inverted output signal could cause the instability. However, the inverted output signal cannot be fed back into the input because of the low-frequency signal path formed by the large MOS-bipolar resistor ( $R_F$ ) and input capacitance ( $C_{IN}$ ). This low-frequency signal path ensures the preamplifier stays stable over the operating frequency range.

To verify the gain variation, which is one of the main concerns in designing an open-loop preamplifier, the mid-band gain has been measured under various bias conditions, and on multiple chips. To check the gain variation due to bias variation, the transfer functions of the preamplifier with different bias currents from 80nA to 2.4μA have been

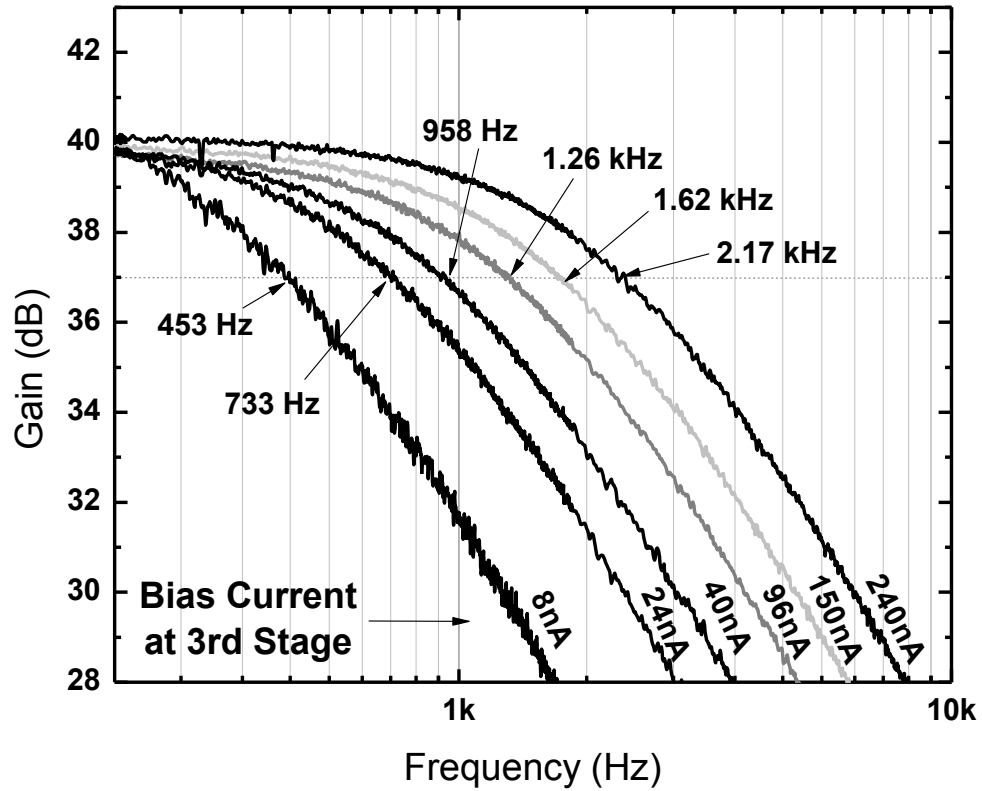


Figure 2-11: Frequency response of the embedded  $g_m$ - $C$  filter

measured, as shown in Figure 2-10. The measured mid-band gains at 20 Hz are shown in the inner plot. With bias current from 240n to 2.4 $\mu$ A, the mid-band gains show a stable gain of  $40.01 \pm 0.2$ dB. Below 240nA, however, the mid-band gain is diverted from its designed value because of the current-ratio mismatch of the current steering circuit at the first stage. To verify the process variation, the preamplifiers from twenty different chips were characterized; the measured mid-band gains show a stable gain of  $39.95 \pm 0.53$ dB.

The frequency response of the programmable  $g_m$ - $C$  filter that is formed by the output load capacitance and  $g_m$  of the load transistor at the third stage is shown in Figure 2-11. In this configuration, the load capacitance is 2 pF, including parasitic capacitances from the PAD and ESD circuits. By altering the bias current of the third stage from 8 nA to 240nA, the cut-off frequency varies from 453 to 2.17kHz.

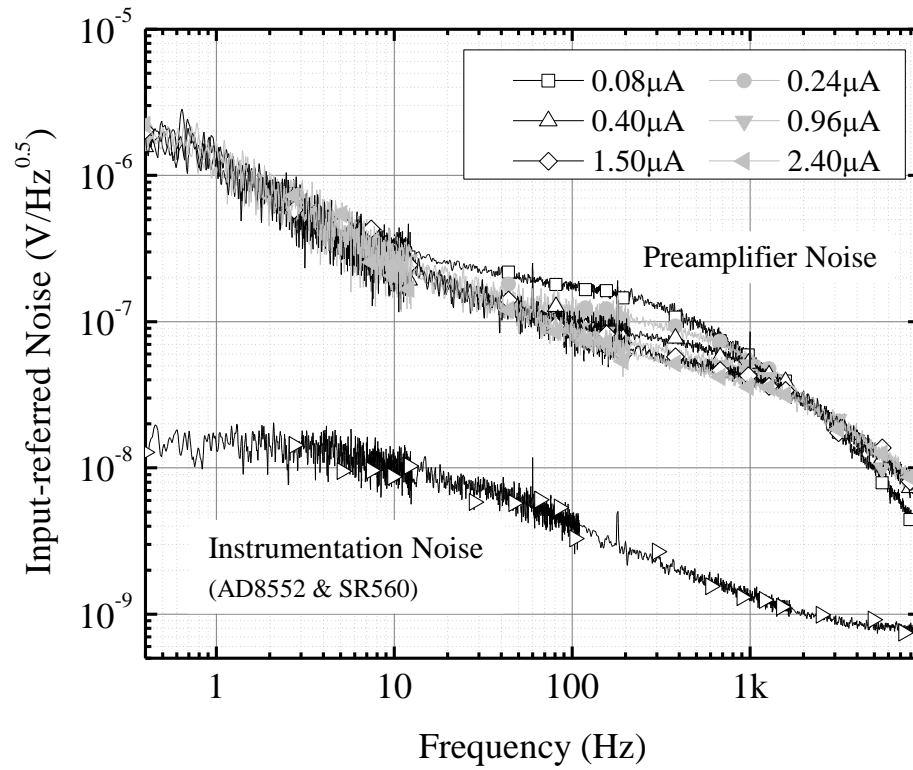


Figure 2-12: Measured noise spectrums under various bias conditions

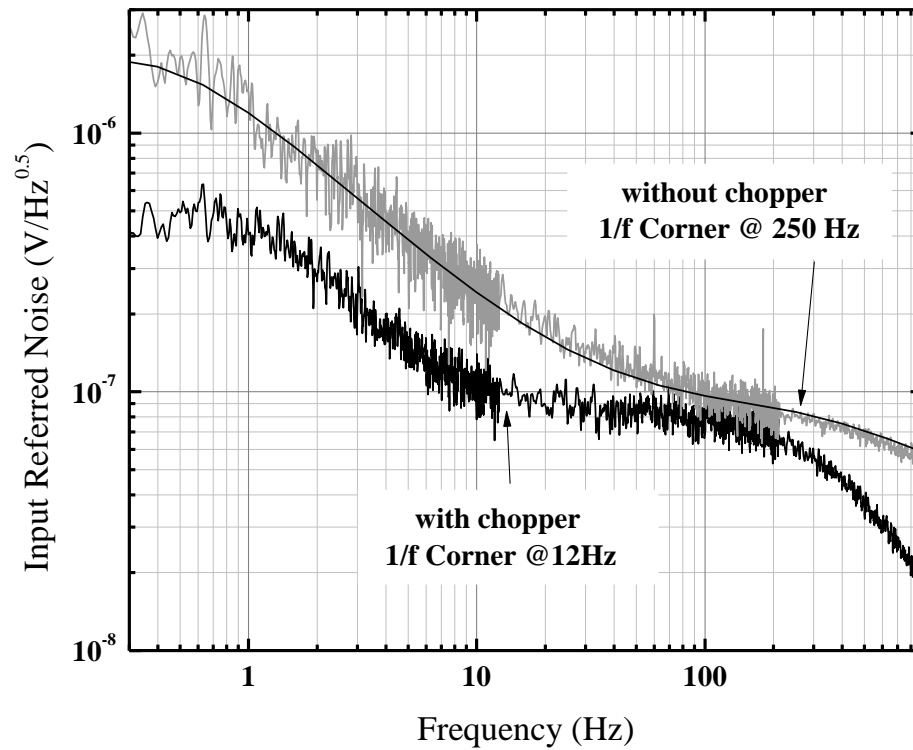


Figure 2-13: Measured input-referred noise spectrums with and without chopper operation compared with the simulated input-referred noise spectrum

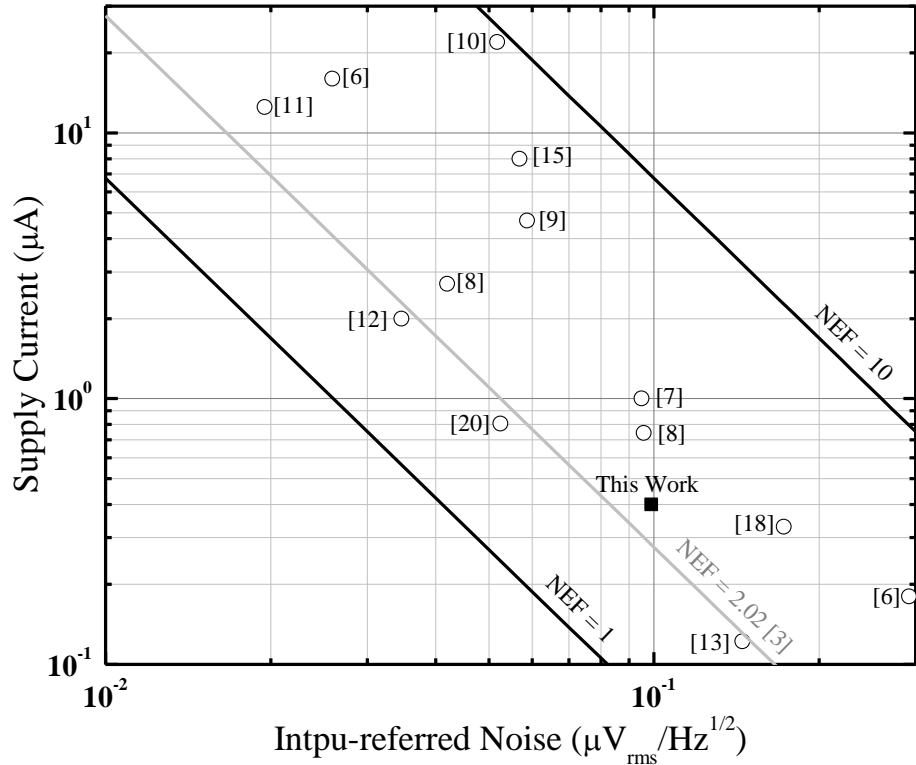


Figure 2-14: Noise efficiency factor (NEF) comparison graph with previous approaches reported in the literatures

The input-referred noise spectrum of the proposed amplifier, which is calculated by dividing the output noise spectrum by the mid-band gain, has been measured and compared with instrumentation noise under various bias current conditions. As shown in Figure 2-12, the thermal noise floor of the preamplifier decreases, as the bias current increases. Especially, in the low-frequency range below 200 Hz, the flicker noise is dominant, and could severely interfere with weak neural potentials. To record low-frequency weak neural potentials such as EEG and ECoG properly, a chopper stabilization technique has been utilized, as shown in Figure 2-13. The gray plot shows the measured input-referred noise spectrum with the total bias current of 400nA without the chopper operation, and the black solid line shows the simulated input-referred noise spectrum. The measured and simulated input-referred noise spectrums show a good agreement with  $K_{fn} = 3.5e-25$ ,  $A_{fn} = 0.9$ ,  $K_{fp} = 5.2e-25$ ,  $A_{fp} = 1.5$ . By enabling the chopper

at 1 kHz, the flicker noise corner frequency is reduced by a factor of 20 from 250 Hz to 12 Hz. This chopper modulator can be operated with additional power consumption of below 10nA. The power consumption of the timing generator is excluded from this power consideration because it can be shared with multiple preamplifiers in a multi-channel system. And, eventually, the up-modulated flicker noise is filtered out using an external low-pass filter with 300 Hz corner frequency. The measured thermal noise level is  $85\text{nV}/\sqrt{\text{Hz}}$  and the input-referred noise is  $1.69\mu\text{V}_{\text{rms}}$  from 0.3Hz to 1 kHz. The noise performance of the proposed preamplifier with enabled chopper is compared with previous literature in Figure 2-14. Single-ended input and output topology [55] shows the smallest NEF of 1.8 among the literature. However, this topology is impractical in the neural interface system because of its low PSRR and linearity. To our knowledge, the fabricated pseudo-open-loop preamplifier had achieved the best NEF value of 2.43 among the differential topologies.

The fabricated preamplifier occupies an area of  $0.189\text{mm}^2$ , and the input-series capacitors occupy over 75% area of the preamplifier, as shown in Figure 2-15. The total harmonic distortion (THD) was measured to be below 1% when an input signal of  $2.25\text{mV}$  @ 100 Hz is applied; the measured dynamic range is 53.5 dB. The measured CMRR and PSRR are 79 dB and 82 dB, respectively, as shown in Figure 2-16. The chip characteristics are summarized in Table 2-2.

### **2.2.3.2 In-vivo EEG Measurement**

To verify the performance of the fabricated preamplifier, we in-vivo EEG signals of a human subject have been measured, as shown in Figure 2-17 instead of monkey ECoG due to the target monkey's safety issue. The EEG electrodes are

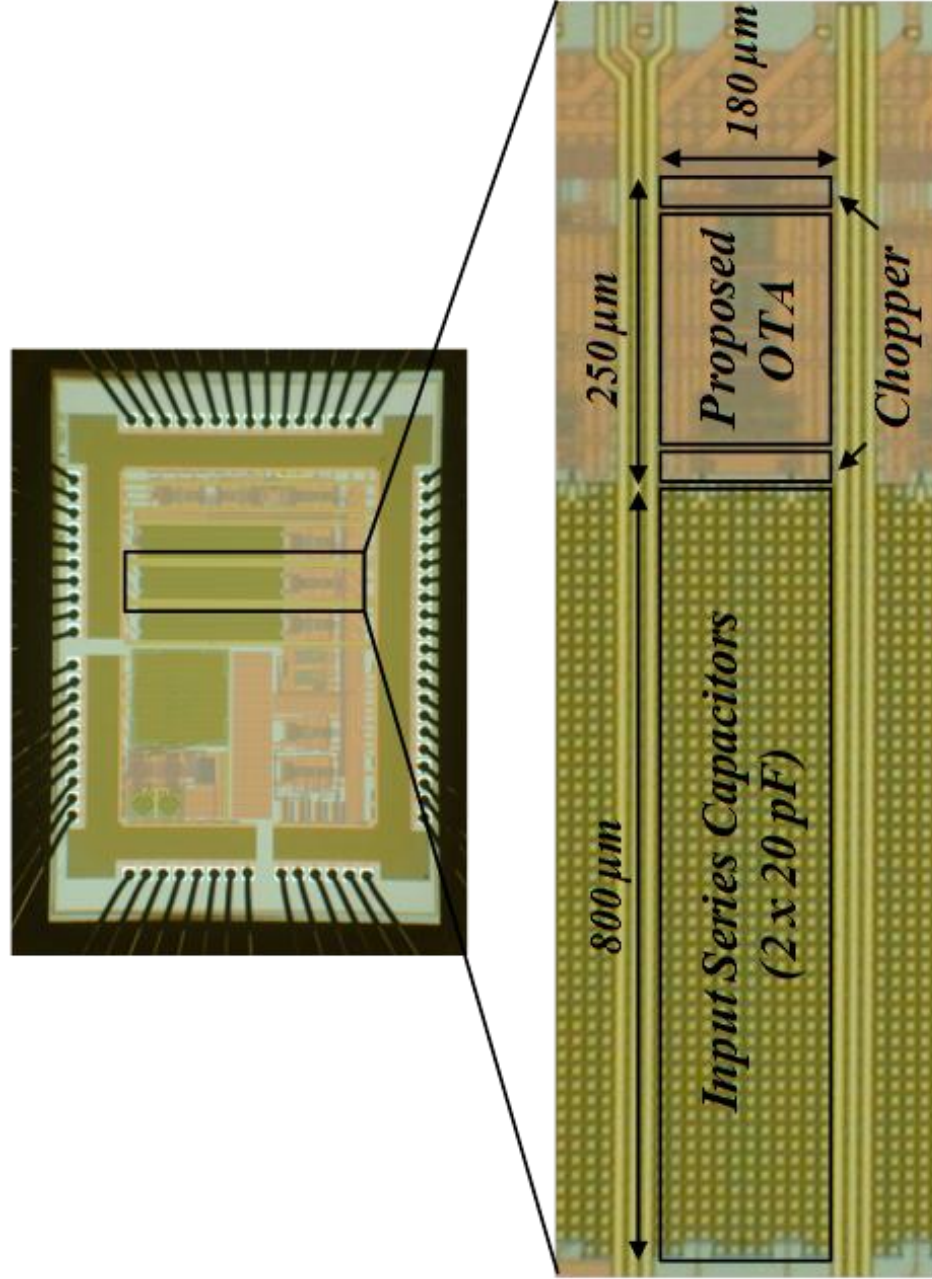
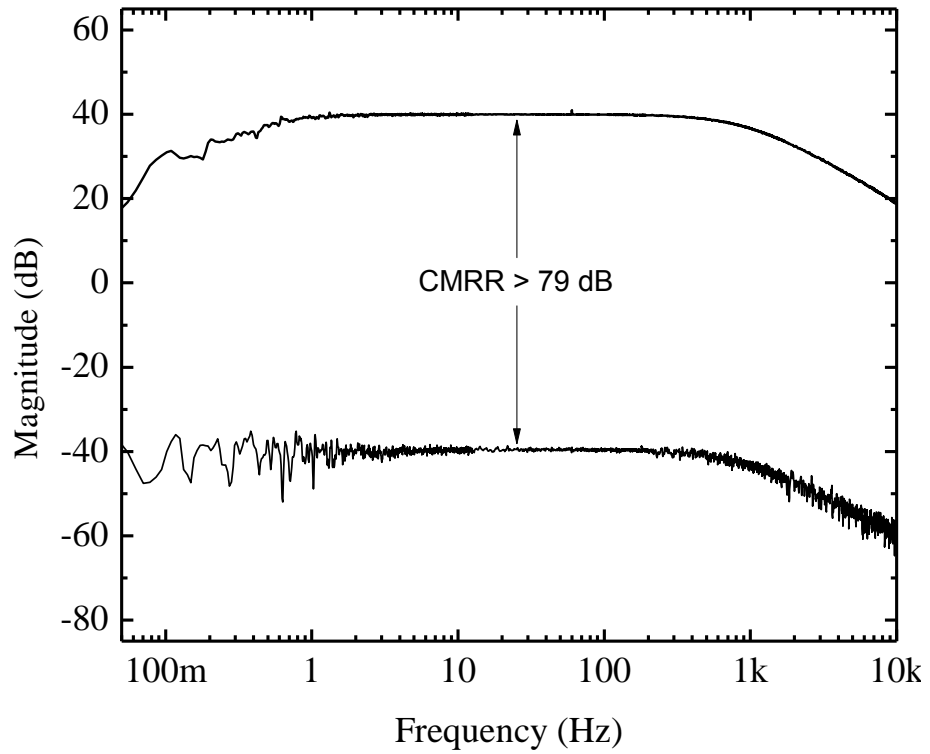
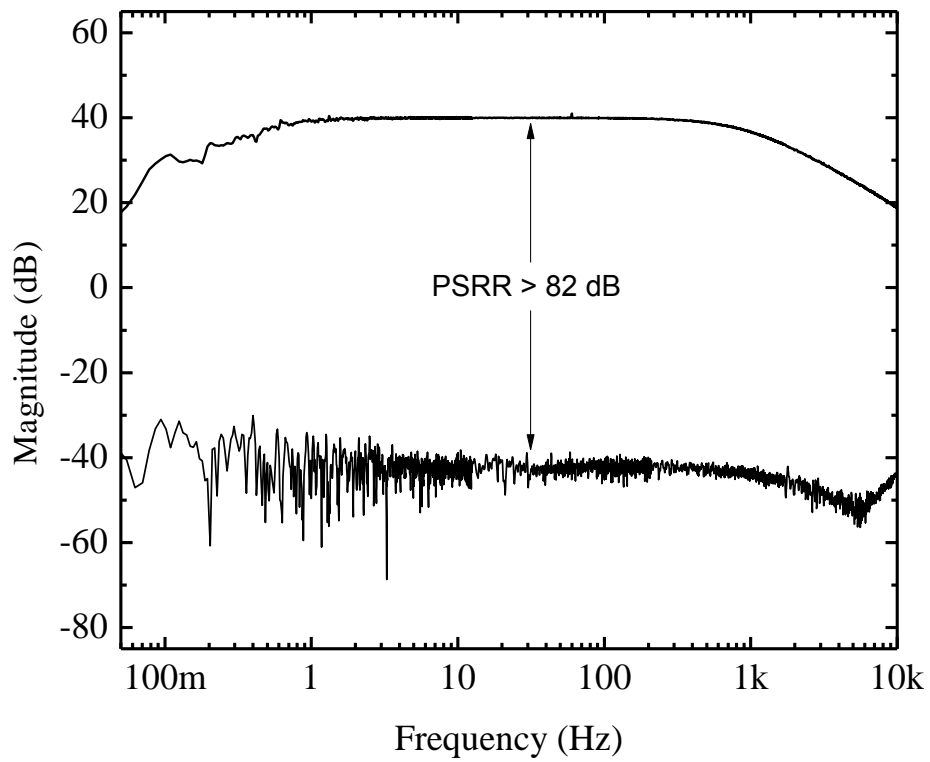


Figure 2-15: Microphotograph of the fabricated preamplifier in a test chip.



(a) CMRR



(b) PSRR

Figure 2-16: Measured CMRR and PSRR of the neural amplifier

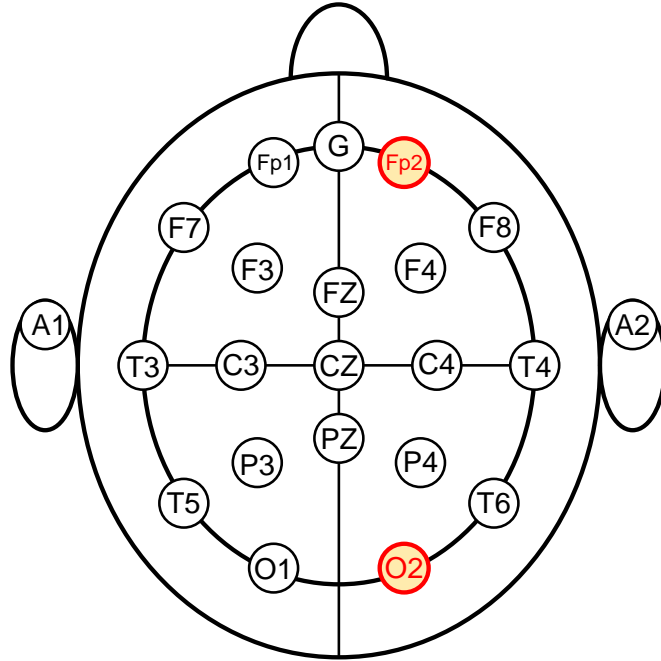


Parameter	Measured Results
Technology	0.25 $\mu$ m 1P5M CMOS
Supply Voltage	2.5 V
Total Current	0.4 $\mu$ A
Gain (Average $\pm \sigma$ , 20 chips)	39.95 $\pm$ 0.53 dB
Bandwidth	0.51 ~ 292 Hz
Input-referred Noise	1.69 $\mu$ V <sub>rms</sub>
Noise Efficiency Factor	2.43
THD	< 1 % (2.25mV <sub>pp</sub> @ 100 Hz)
Dynamic Range	53.5 dB
CMRR	79 dB
PSRR	82 dB
Area	0.189 mm <sup>2</sup>

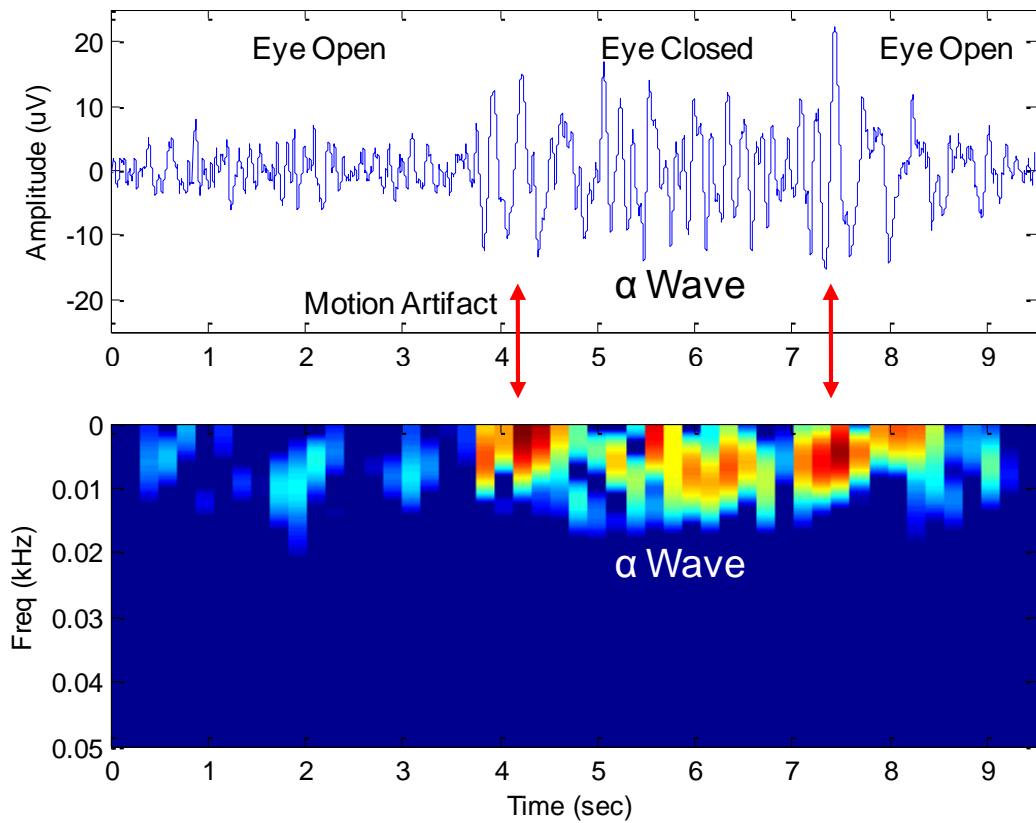
Table 2-2: Performance Summary of the Proposed Pseudo Open-Loop Preamplifier located in Fp2 and O2, and measured as differential inputs, as shown in Figure 2-17 (a). Figure 2-17 (b) shows the recorded waveform and its spectrogram while the subject blinks its eyes. During eye-shut periods, we observed  $\alpha$ -waves in 8–12 Hz bandwidth which is a typical brain activity in the absence of visual stimulus [61]. Eye lid motion artifact can be distinctly shown during the recording session indicated by the arrows.

### 2.2.4 Summary

We have proposed, designed, fabricated, and characterized a low-noise low-power pseudo-open-loop preamplifier with a programmable band-pass filter for neural interface systems. The proposed amplifier is configured to consume 400nA at 2.5V power supply and the total chip area is 0.189mm<sup>2</sup>. The measured thermal noise is 85nV/ $\sqrt$ Hz and input-referred noise is 1.69 $\mu$ V<sub>rms</sub> from 0.3Hz to 1 kHz when using a chopper stabilization technique to suppress flicker noise. The fabricated preamplifier shows the noise efficiency factor of 2.43. We have implemented a programmable  $g_m$ -C filter at the output stage. The bandwidth of the preamplifier can be



(a) EEG 10-20 Electrode Location



(b) Waveform and its spectrogram

Figure 2-17: *In-vivo* EEG measurement

adaptively programmed from 453 Hz to 2.2 kHz, applicable for various neural interface systems.

### **2.3 A Low-Power Area-Efficient 8 bit SAR ADC Using Dual Capacitor Arrays**

Recently, multichannel neural interface systems have been implemented to monitor neural activities. For the comprehensive analysis of neural activities, it is essential to develop simultaneous real-time monitoring of multiple sites. Typically, neural activities such as spike/LFP, ECoG and EEG contain most of information in the bandwidth below 10 kHz with maximum amplitude of  $\pm 500 \mu\text{V}$ . In these implantable neural interface microsystems, the sub-mV range neural signals should be amplified up to the minimum level they can be digitized at appropriate resolution. The intrinsic noise immunity of the digital signal can enhance the stable data transmission using wired/wireless communication links between the implanted system and the external world.

In order to digitize the amplified analog signal in the above signal transmission chain, various analog-to-digital converters are available to be utilized such as single/dual slope ADCs, sigma-delta modulator ADCs, pipe-line ADCs. Among these a successive approximation register (SAR) ADC is one of the most suitable approaches for neural interface applications due to its simplicity, low power consumption, and reasonable resolution.

#### **2.3.1 Low-Power Area-Efficient Design Considerations for Various Resolution**

Due to the various constraints for the implantable neural interface system such as limited power and multichannel capability, various design aspects such as power, area will be considered in this section.

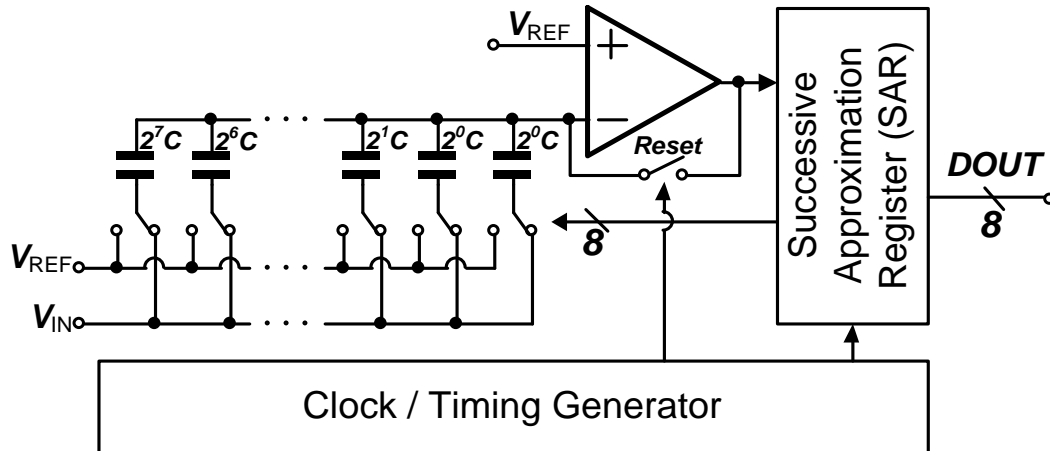


Figure 2-18: Overall Architecture of a Conventional 8-bit SAR ADC

### 2.3.1.1 Power Consumption Analysis

Figure 2-18 shows overall architecture of a conventional SAR ADC. It consists of a comparator, a binary-weighted charge-redistributed DAC, successive-approximation registers, and a clock/timing generator. To design and achieve the low-power operation of the ADC, we need to estimate the power consumption of each component, particularly, based on the resolution requirements, because the conversion speed requirement is relaxed by the slow sampling frequency which is below 10kS/s.

1) *Latched Comparator*: Typically, the comparator consists of the preamplifier to prevent the kick-back effect and the regenerative stage to increase the gain as shown Figure 2-19. To obtain higher resolution and to minimize the effects of the kickback during the reset phase from the regenerative gain stage, a preamplifier is utilized with a gain of 10. The pre-amplified signal, then, is amplified using the cross coupled back-to-back inverter configuration. Here, the preamplifier consumes a static power during the whole ADC operation, while the regenerative gain stage consumes a dynamic power during the latch phase. By assuming each stage bandwidth is wide enough to handle the

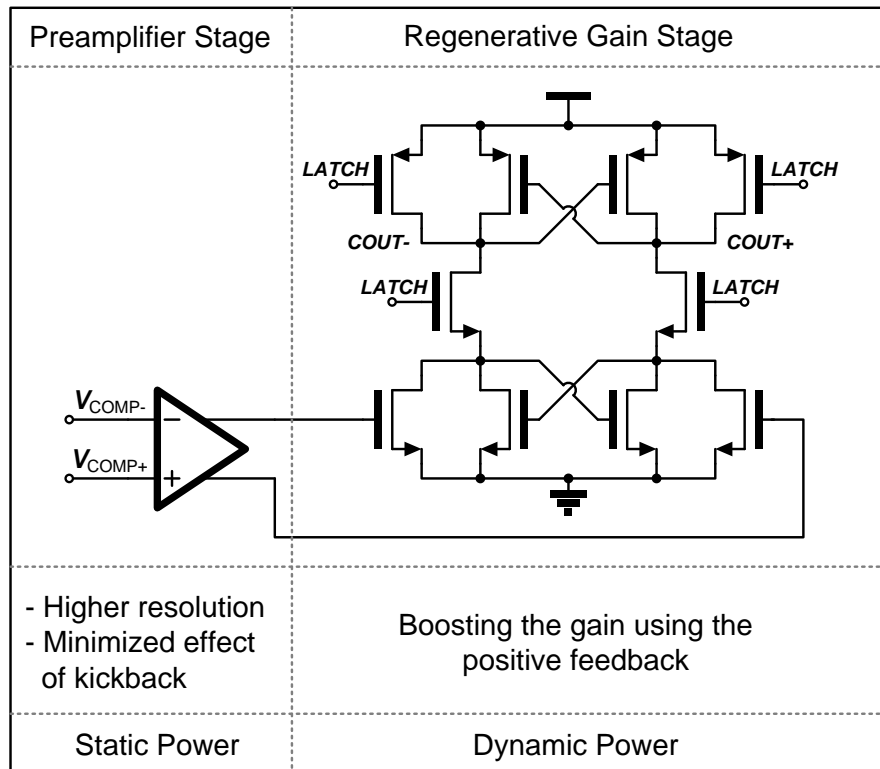


Figure 2-19: A Typical Architecture for a Latched Comparator

required conversion steps or number of bit, we can simply estimate that, as the ADC resolution increases, the power consumption in the regenerative gain stage will increase linearly, while that of the preamplifier stage will remain unchanged. From this simple estimation, in order to save power consumption, we can utilize only the regenerative gain stage by eliminating the preamplifier stage with a careful design taking care of the kickback effect and metastability of the regenerative comparator.

2) *Digital Blocks: SA Register and Clock/Timing Generator:* Likewise the regenerative stage of the comparator, the digital block which consists of logic gates and flip-flops consumes dynamic power. The power consumption from digital blocks also increases linearly as the ADC resolution increase.

3) *Capacitive DAC:* As you can see in Figure 2-18, typically binary-weighted capacitive DAC is utilized due to its simple operation as well as the possible low-power

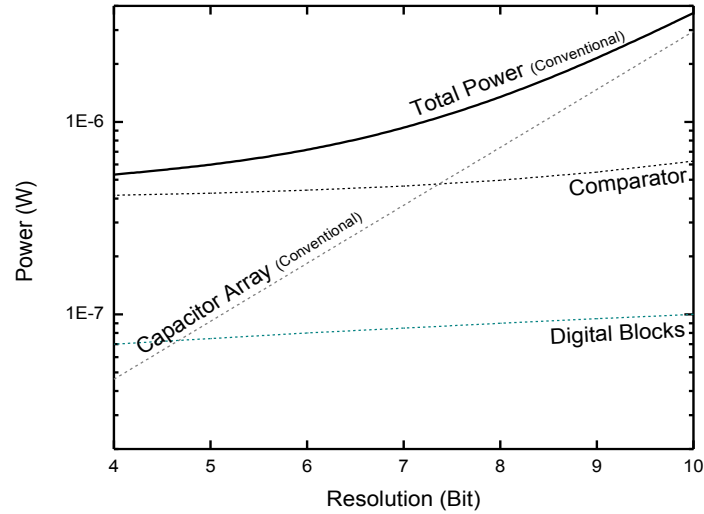


Figure 2-20: Power Consumption Estimation

operation. However, the power consumption for charging and discharging the binary-weighted capacitor bank increases exponentially as the ADC resolution increase.

Based on the previous analysis, Figure 2-20 shows the power consumption of each component with various resolution bits. From Figure 2-20, above 6bit resolution, the power consumption of the capacitance will be dominant among the all blocks.

### 2.3.2 Area Efficient SAR ADC Architecture

With a gain of 60 dB prior to the ADC, the quantization noise is required to be less than  $5 \text{ mV}_{\text{rms}}$ , which can be achieved by 8 bit or higher resolution capability of ADC. Figure 2-21 shows a conventional 8-bit SAR ADC structure, which typically consists of three parts: capacitor array (for sample and hold and DAC), comparator, and successive approximation register (SAR). For relatively lower resolution ADCs (<6b), the comparator and SAR consume most power [62]. However, as we already discussed in the previous section, when the resolution of ADCs increases, the power consumption required for charging and discharging the capacitor array becomes significant. Also, the total capacitance required for DAC increases exponentially proportional to the number of

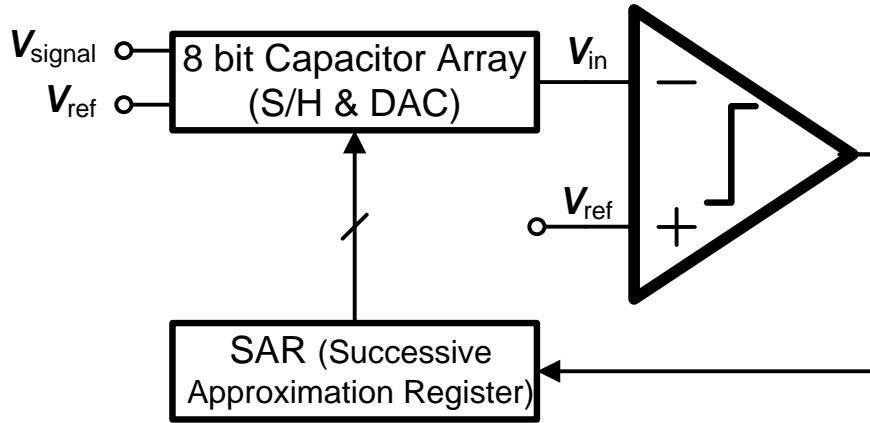


Figure 2-21: The overall structure of conventional SAR ADC

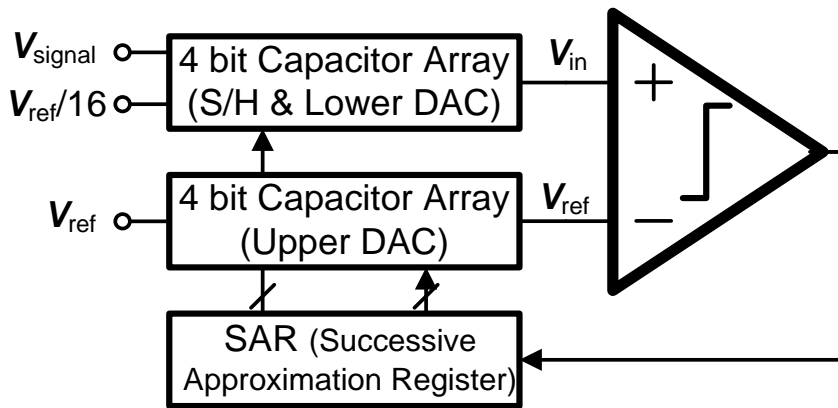


Figure 2-22: The overall structure of the proposed area-efficient SAR ADC

bits. In the high resolution ADCs, the capacitor array takes most of the area and power consumption. It becomes more important to reduce the total capacitance and area as the number of bits required in ADC increases and multiple implementations of ADCs is needed.

In this section, we propose an area-efficient 8 bit SAR ADC using dual capacitor arrays. Using the dual capacitor array banks, we can reduce the required capacitor array area by a factor of  $2^{N/2-1}$  compared to the conventional approaches. This feature can not only reduce the area but also the power consumption by eliminating the power required for charging/discharging the capacitor array.

### 2.3.2.1 Dual Capacitor Arrays

The key idea of the proposed SAR ADC is to perform the successive approximation on both sides of comparator inputs using dual capacitor arrays rather than only in one side. As shown in Figure 2-22, the 8-bit DAC can be split into two identical 4-bit capacitor arrays. The upper DAC is used to quantize upper 4 bits, while the lower DAC does lower 4 bits. The main advantage of the dual capacitor arrays is the reduction of the total capacitance and area for DAC capacitors by a factor of

$$\text{Reduction Factor} = 2^{\frac{N}{2}-1}, \quad \text{Eq. 2-19}$$

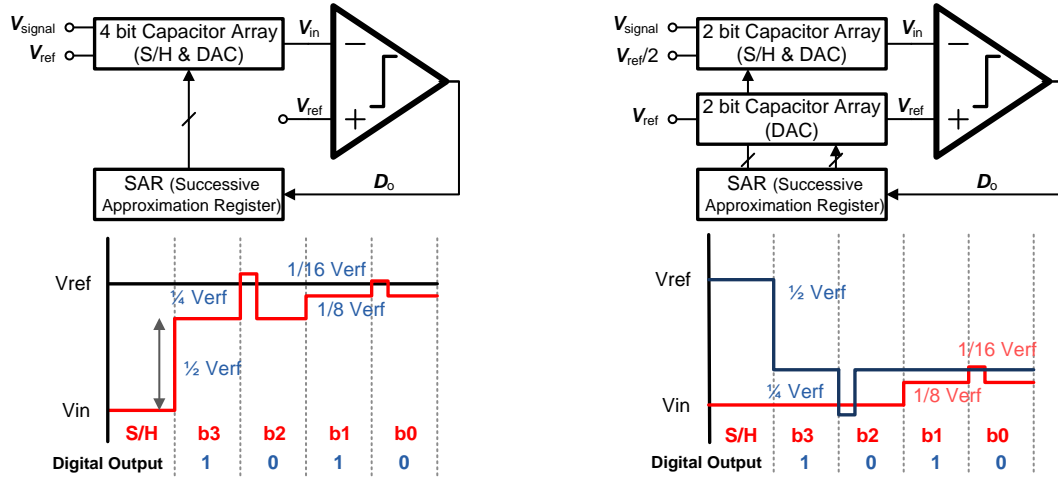
where N is the number of bit. For example, the reduction factors become 8 and 16, respectively for 8 and 10 bit resolutions. And the power consumed by the capacitor array would be reduced by the same reduction factor. This advantage is more effective for higher resolution ADCs. By applying this technique, we can effectively implement the ADCs within the given area and power budget. This feature easily equips the neural interface system with a simultaneous real-time monitor capability of the multiple neural activities. The dual capacitor array operation will be explained in detail in the following sections.

### 2.3.2.2 SAR ADC Operation

Fig. 3 shows an example of 4-bit conversion in conventional SAR ADC and the proposed ADC structure. Basic operations of a 4-bit SAR ADC can be divided into two steps: sample/hold and a sequence of successive approximations. During each approximation step,  $V_{in}$  can be expressed as:

$$V_{in}[n] = V_{in}[n-1] + \frac{V_{ref}}{2^{n+1}} (1 - (-1)^{D_o[n]}), \quad \text{Eq. 2-20}$$





(a) Conventional SAR ADC

(b) Area Efficient SAR ADC

Figure 2-23: 4 bit SAR ADC operation examples: (a) Conventional SAR ADC, (b) Proposed area-efficient SAR ADC

If the  $V_{in}[n]$  is smaller than  $V_{ref}$ , the comparator output is 1, and the SAR sets the output  $b_n = 1$  and generates the control signal to make  $V_{in}[n]$  be  $V_{in}[n-1] + V_{ref} / 2^n$ . If  $V_{in}$  is greater than  $V_{ref}$ , the output is  $b_n = 0$ , and the  $V_{in}$  stays from previous step. The red line shows  $V_{in}$  from each steps. By repeating this step four times, the signal can be quantized at a 4-bit resolution.

As shown in Figure 2-23(a), the conventional ADC is performing the approximation in the one input node of the comparator while the other input side is fixed to reference. On the other hand, the proposed ADC uses both sides (signal side: 2 bit and reference side: 2 bit) to perform the approximation. During the first two steps, the upper DAC is operated to approximate  $V_{ref}$  to  $V_{in}$  as shown by blue line in Fig. 3 (b). During the following two steps,  $V_{in}$  is approximated to  $V_{ref}$  using the lower DAC. After 4 steps, the signal is digitized as 1010. For the same resolution, the proposed ADC requires only half ( $= 1/\text{reduction factor} = 1/2^{N/2-1}$ ) the area for the capacitor array and consumes half the power compared to the conventional ADC. Here, it should be noted that, in the proposed scheme, we need an additional reference,  $V_{ref} / 2^{N/2}$  which can be provided externally.

### 2.3.3 SAR ADC Circuit Blocks

#### 2.3.3.1 Comparator

Figure 2-24 shows the circuit schematic of the comparator. Due to smaller capacitance in the dual capacitor arrays, the regenerative comparator may cause kickback effect during the regenerative phase. This coupling effect between the input and output may severely deteriorate the performance of ADC. To suppress this phenomenon, a buffer stage with a gain of 10 is introduced prior to the regenerative comparator. The difference between the two inputs ( $V_{in}$  and  $V_{ref}$ ) is sampled and amplified through the buffer stage and then forwarded to the regenerative stage during reset phase. As the regenerative phase starts, on the rising edge of  $V_{Latch}$  the difference is amplified and eventually the polarity of the difference is determined. In the proposed ADC, two identical capacitor arrays are located at both input nodes of the comparator. This configuration helps to suppress the comparator offset which may come from the charge

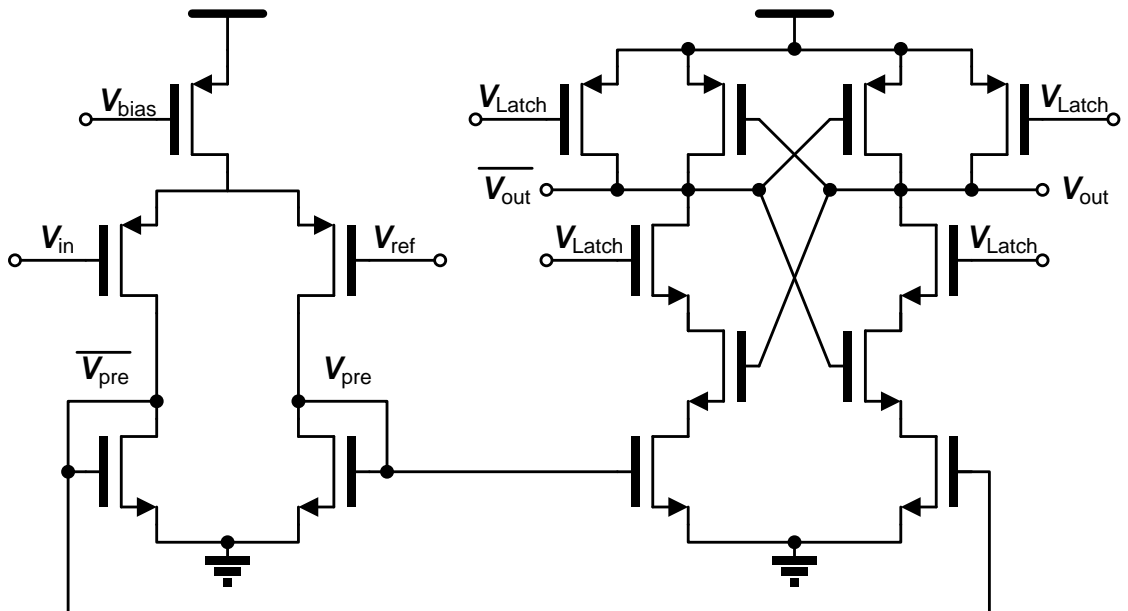


Figure 2-24: Schematics of the comparator

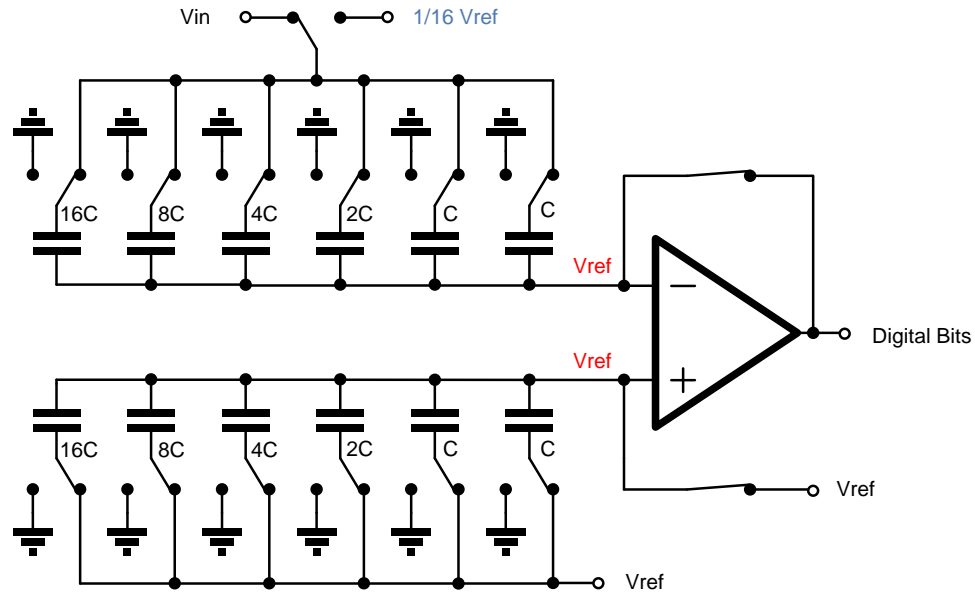


Figure 2-25: Dual capacitor array (during reset phase)

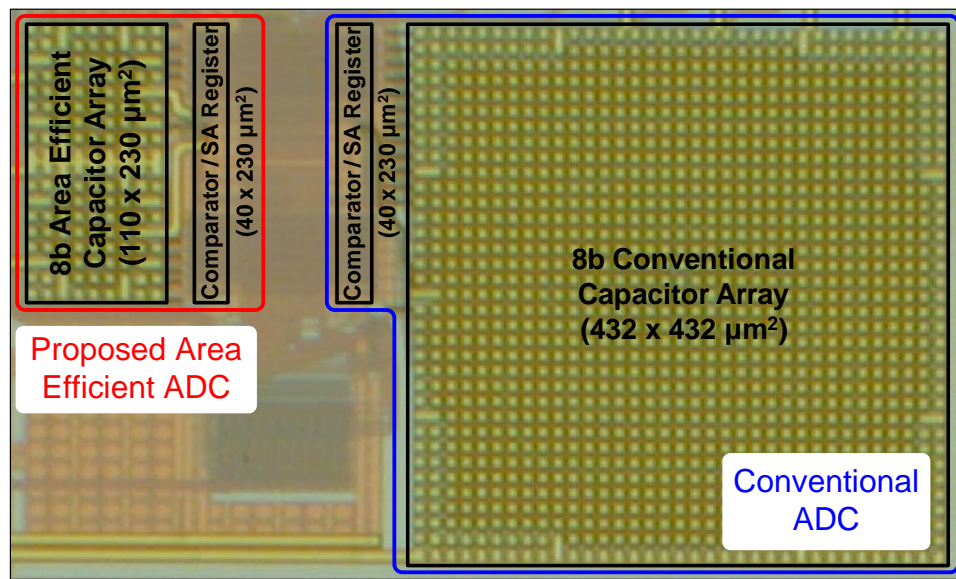


Figure 2-26: Microphotograph of the fabricated preamplifier in a test chip

injection from the reset switches or any unexpected possible leakage path.

### 2.3.3.2 Dual Capacitor Arrays

As shown in Figure 2-25, to implement both upper and lower DACs, two identical capacitor arrays have been implemented using MIM capacitors, where a unit capacitance is given as 100fF. Total capacitance for the SAR 8 bit ADC is  $2 \times 2^4 C_{\text{unit}} = 32 C_{\text{unit}}$ . The

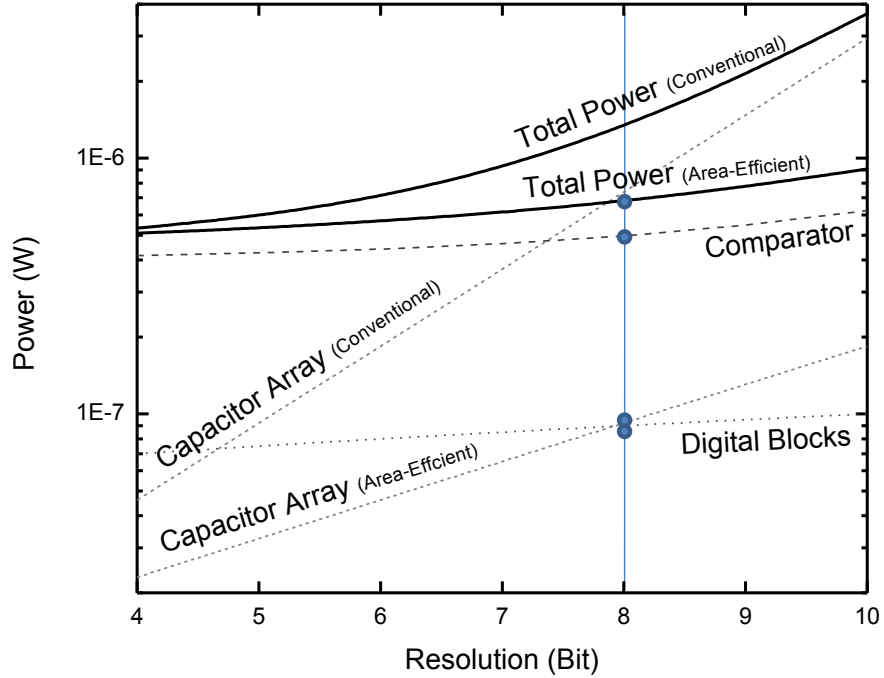


Figure 2-27: Power consumption comparison with respect to the resolution

two 4 bit capacitor arrays are identical except that the lower DAC has an additional switch to sample and hold the signal during the comparison.

### 2.3.4 Measurement Results

Figure 2-26 shows the fabricated ADC using 0.25 $\mu$ m 1P5M CMOS process. To evaluate the proposed ADC, a conventional ADC is also fabricated, measured, and characterized. The total active area of the proposed ADC is 0.035 mm<sup>2</sup>, while the conventional ADC occupies 0.196 mm<sup>2</sup>. ADC performance is summarized in Table 2-3. The fabricated ADCs have a resolution of 8 bit with a sampling frequency of 20kS/s. The total power consumption of the proposed ADC is 680nW at 1.8V (Analog) and 2.5 V (digital) supply by utilizing the dual capacitor array. The comparator consumes most of the power (~498 nW), and the proposed capacitor array consumes 92nW at 1.2V input range, while the conventional capacitor array consumes ~737 nW, which is eight times higher and even higher than the comparator.

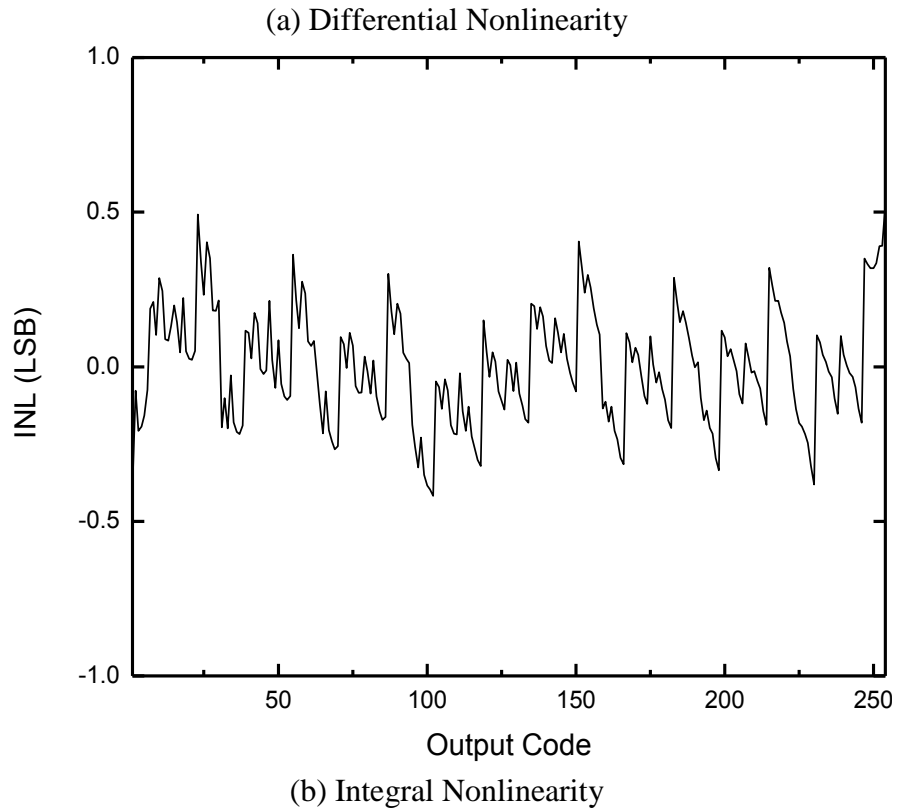
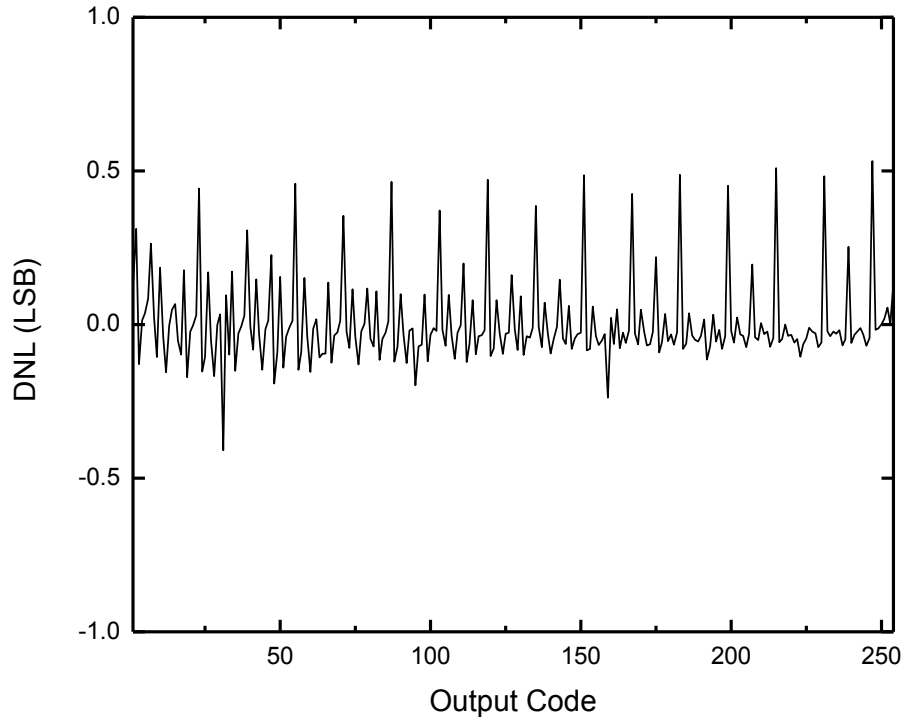


Figure 2-28: The measured (a) DNL and (b) INL of the proposed ADC

We also estimate the power consumption as a function of resolutions in ADC as shown in Figure 2-27. The total power consumption increases with resolution. The power

consumption by the conventional capacitor array itself becomes significantly high when the resolution is above 7 bit, as it increases exponentially with resolution by a factor of  $2^N$ . On the other hand, the power consumption of the proposed capacitor array slowly increases by a factor of  $2^{N/2}$ , and consumes much less power. Even in 10 bit resolution, the power consumption of the proposed capacitor array stays below that of the comparator.

#### **2.3.4.1 Static Characteristics**

Figure 2-28 shows the measurement results of differential nonlinearity (DNL) and integral nonlinearity (INL). The measured INL and DNL are both below  $\pm 0.5$  LSB.

#### **2.3.4.2 Dynamic Characteristics**

The measured 8 bits digital output codes are analyzed using a FFT from the input signal of 8046.875 Hz at 256 samples shown in Figure 2-28. The measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are  $42.82 \pm 0.47$  dB and  $57.90 \pm 2.82$  dB, respectively. Total harmonic distortion (THD) and effective number of bit (ENOB) are  $-53.58 \pm 2.15$  dB and  $6.65 \pm 0.07$  bits, respectively.

We also measured the dynamic response of the ADC at different sampling frequencies to verify the leakage characteristic. Leakage can be especially significant in small capacitor arrays at low sampling frequency ( $<1$  kS/s) such as EEG or ECoG applications. The results are shown in Figure 2-30. The performance of the proposed ADC remains constant in the range of the various sampling frequencies (625 Hz ~ 20 kHz) indicating that the leakage is not a serious issue even though we use the small capacitance array bank.

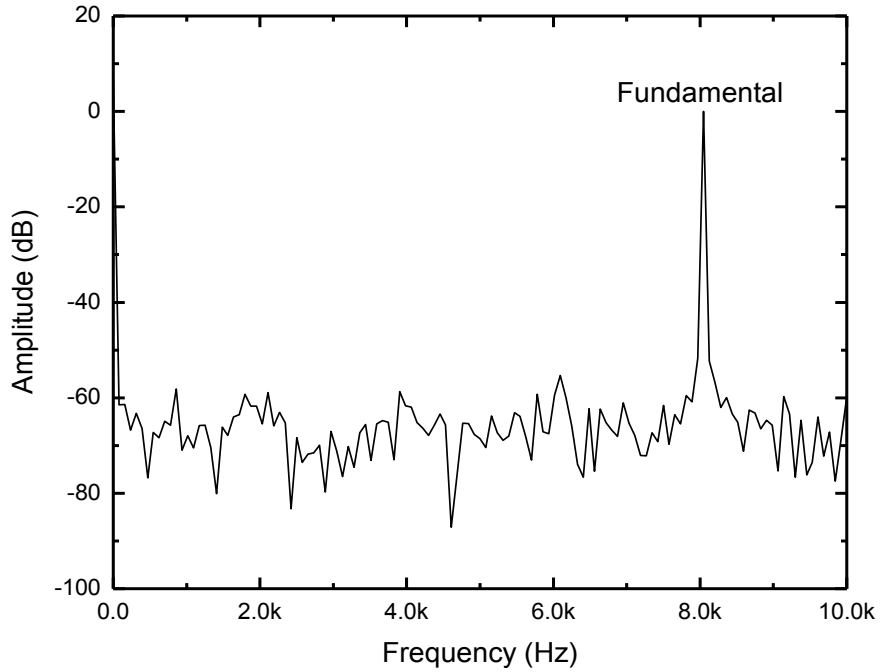


Figure 2-29: FFT plot of the measured digital output codes for an input frequency of 8046.875 Hz

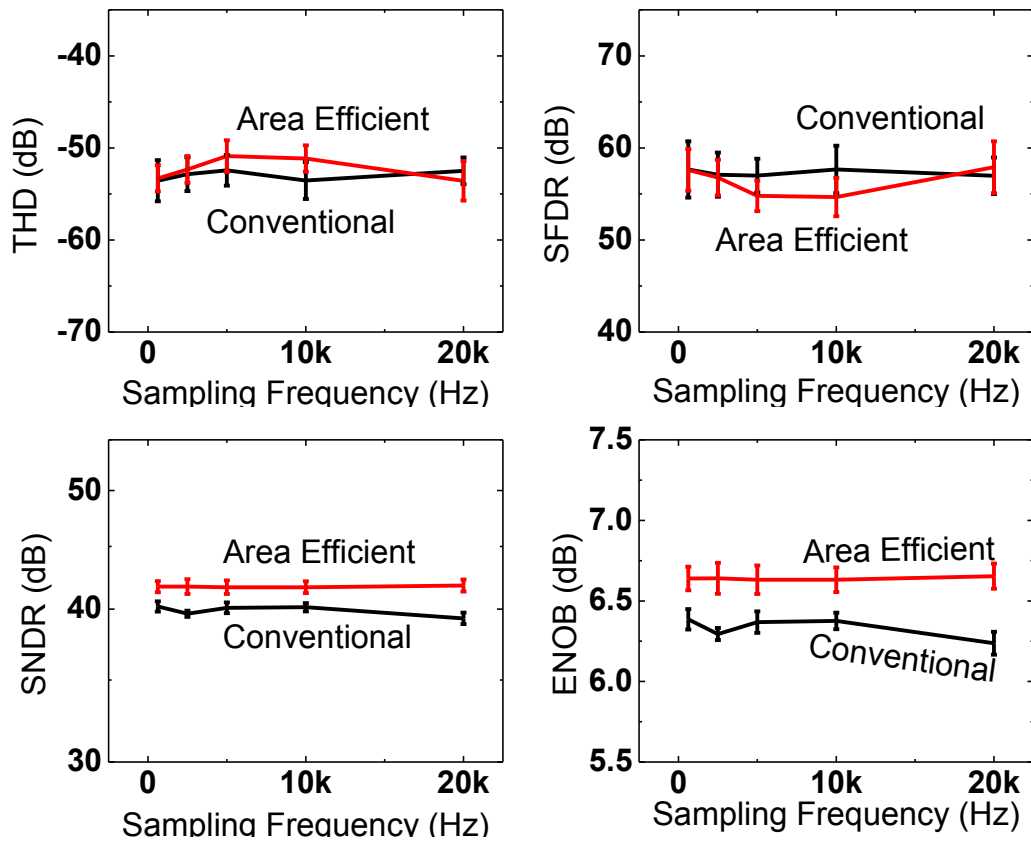


Figure 2-30: Measured dynamic characteristics with different sampling frequency: Area efficient and Conventional ADCs

<b>Parameter</b>	<b>Measured</b>
<b>Technology</b>	<b>0.25<math>\mu</math>m 1P5M CMOS</b>
<b>Supply Voltage</b>	<b>1.8V (Analog) / 2.5 V (Digital)</b>
<b>Sampling Frequency</b>	<b>20 kS/s</b>
<b>Power Consumption</b>	<b>680 nW</b>
<b>INL</b>	<b>&lt; <math>\pm 0.5</math> LSB</b>
<b>DNL</b>	<b>&lt; <math>\pm 0.5</math> LSB</b>
<b>SNDR</b>	<b>42.82 <math>\pm</math> 0.47 dB</b>
<b>SFDR</b>	<b>57.90 <math>\pm</math> 2.82 dB</b>
<b>THD</b>	<b>-53.58 <math>\pm</math> 2.15 dB</b>
<b>Resolution/ ENOB</b>	<b>8 bits / 6.65 <math>\pm</math> 0.07 bits</b>
<b>Figure of Merit</b>	<b>0.34 pJ/conversion</b>
<b>Area</b>	<b>0.035 mm<sup>2</sup></b>

Table 2-3: Performance Summary Table of Area Efficient SAR ADC

### 2.3.5 Conclusion

We have proposed, designed, fabricated and fully characterized an area-efficient SAR ADC using dual capacitor arrays for neural microsystems. The proposed ADC consumes 680nW and the total chip area is 0.035 mm<sup>2</sup>. The measured SNDR, SFDR, THD, and ENOB are 42.82  $\pm$  0.47 dB, 57.90  $\pm$  2.82dB, -53.58  $\pm$  2.15 dB, and 6.65  $\pm$  0.07 bits, respectively. Compared to the conventional ADC, the proposed ADC consumes less power by a factor of  $2^{N/2-1}$  (8 in this paper) and occupies less area. This reduction factor increases exponentially with the increase of resolution. This implies that the proposed scheme will benefit more at higher resolution ADCs in EEG or ECoG applications. With the proposed ADC, we can effectively implement the neural interface system with multiple ADCs within a given area and power budget.



## 2.4 Wireless Data Transmission using FM and USRP

In order to implement a fully implanted neural interface system, a wireless data communication block is essential. To verify feasibility of the wireless data link, we have designed and tested the wireless data link between implanted devices and external device. As shown in Figure 2-31, the amplified neural signals are modulated by FM transmitter and transmitted through the antenna. These transmitted signals are, then, retrieved by FM receiver and computer. This wireless link has been built using three components: MAX260X [63] as FM transmitter, USRP [64] as RF receiver, and GNU-Radio [65] as control software. MAX260X family is a miniaturized IF VCO which can up-convert the analog input signal to an RF signal centered at 260 MHz in this project. The power consumption of MAX2607 is 5.25mW. For antenna, we used a unipolar antenna with  $1/20\lambda$  ( $=57.5$  mm) in length for small form factor. Even though 260MHz frequency band is used in this report, eventually, 402~405MHz MICS band [66] will be used from next implanted devices. This MICS band is a frequency band allocated by FCC for medical

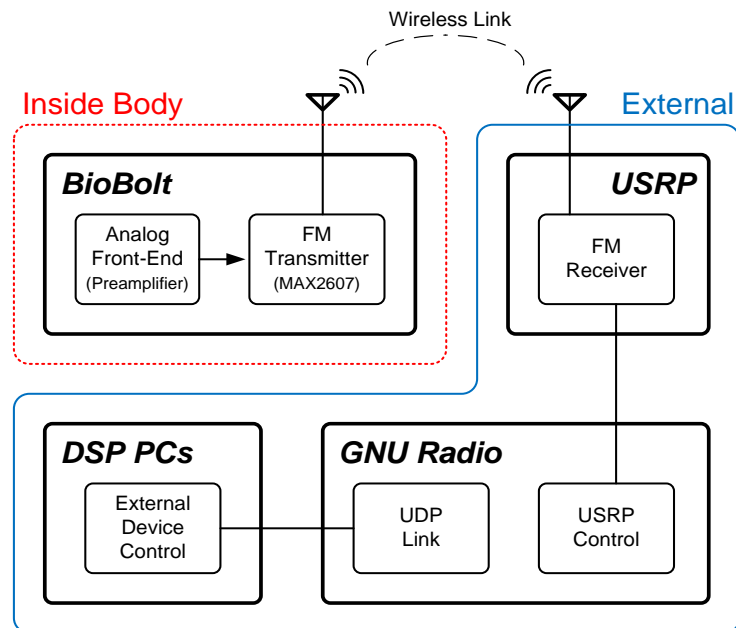


Figure 2-31: Wireless Data Link Architecture

implant device for reasonable signal propagation characteristics in the human body. For the receiver, we utilized the Universal Software Radio Peripheral (USRP) from Ettus Research LLC. This receiver is configured to receive 50 to 860 MHz signal with daughter board (TVRX). This software radio system is controlled by a GNU Radio which is an open-source software defined radio (SDR) platform. It provides a complete development environment to create our own radios, and to handle all of the hardware interfacing, multithreading, and portability issues.

For the realization of a full brain computer interface system, a real-time signal processing is required to control external devices such as artificial limb or a cursor on the screen. To provide this capability, a UDP link is also implemented to broadcast the retrieved signal to multiple signal processing computers in real-time. Even though the current wireless link is set to FM communication to verify the concept, it can be easily adopted to other modulation techniques such as FSK, PSK which are digital modulation techniques, and known to have better power and noise efficiency than FM modulation. Figure 2-32 shows the result of the designed wireless data link. To test the wireless data

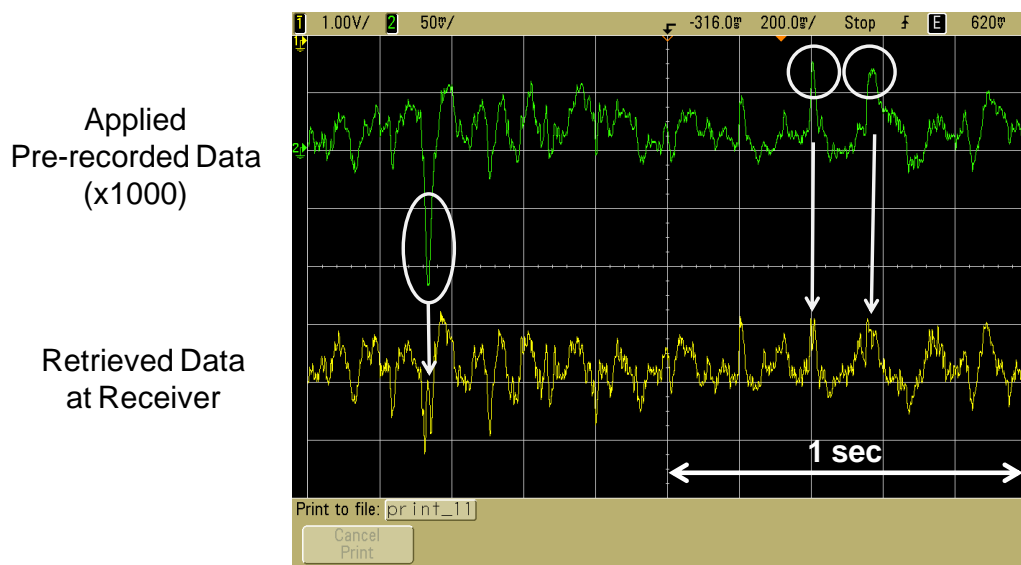


Figure 2-32: Wireless Data Link Test

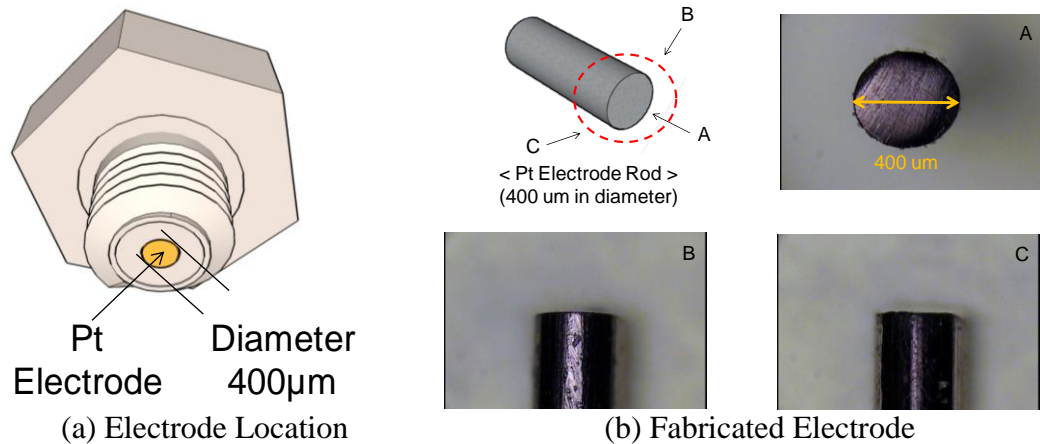


Figure 2-33: Electrode Fabrication and Dimension

link, the pre-recorded neural data (Green Trace) is applied to the preamplifier. The amplified signal is transmitted using MAX2607 and retrieved by USRP and GNU Radio (Yellow Trace). Due to BPF characteristic of the pseudo-open-loop preamplifier (0.5Hz ~ 2kHz), the low-frequency signal ( $< 0.5\text{Hz}$ ) is suppressed. Even though large amplitude signal is distorted due to the limited bandwidth (up to 5 MHz) of FM receiver (USRP) as shown in Figure 2-32, it can be easily addressed by integrating programmable gain amplifier (PGA) to control the gain of the system or using digital modulation techniques such as FSK in next version of implanted devices.

## 2.5 Electrode Fabrication and Characteristic

To convert from ion-based neuron activity into electron-based electrical signal, we designed and fabricated Pt electrode which is located at the bottom of the implanted devices body as shown in Figure 2-33(a). In this prototype, we used only one electrode. The next version of prototype will include sixteen channels per one bolt. The cross section of the Pt wire with 400 µm in diameter is used as electrode. For uniform surface, the cross section of the wire is grinded with fine sand paper as shown in Figure 2-33 (b).

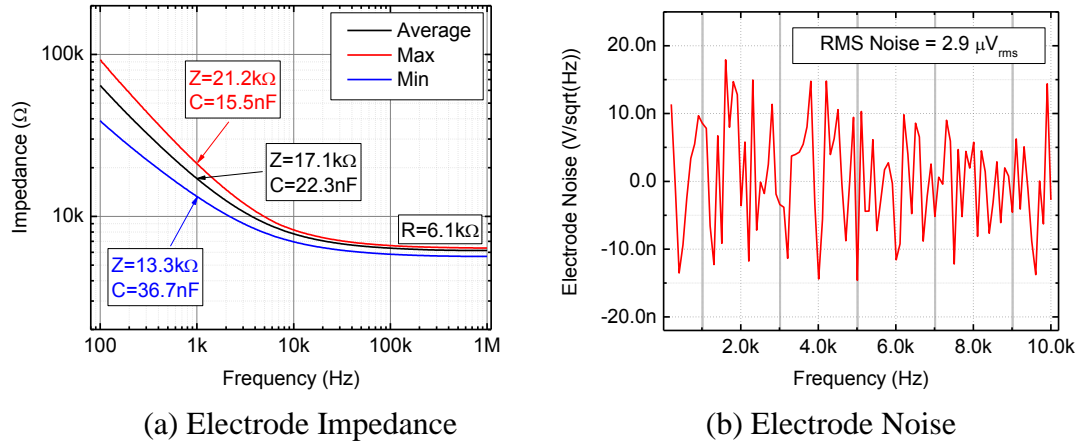


Figure 2-34: Electrode Characteristics (a) Impedance and (b) Noise

The impedance and noise of the fabricated electrode were measured in the saline solution as shown in Figure 2-34. The average impedance is  $17.1\ \text{k}\Omega$  at  $1\text{kHz}$  with series capacitance of  $22.3\text{nF}$ . The noise is measured to be below  $\pm 20\text{nV}/\sqrt{\text{Hz}}$  and  $2.9\ \mu\text{V}_{\text{rms}}$  between  $100\text{Hz}$  and  $10\text{kHz}$ .

## 2.6 Prototype-0 Implementation

The implantable device is assembled as shown in Figure 2-37. Titanium (Ti) is used as a frame material for safety and bio-compatibility of the system. This Ti frame can provide not only a rigid structure but also the floating ground and reference for a fully differential preamplifier packaged inside the implanted device and waystation to suppress any possible DC interferences. To insulate the Ti frame from the rest, the whole system is coated with a bio-compatible insulator, Parylene. Electrode is connected to the PCB located inside the cavity of the implantable device using jumper wire. A coin-type battery is placed underneath the PCB inside the enclosure. On the PCB, the fabricated analog front-end, output driver, and FM transmitter with bias circuit are placed. The cavity inside the implantable device is completely filled with medical grade elastomer from

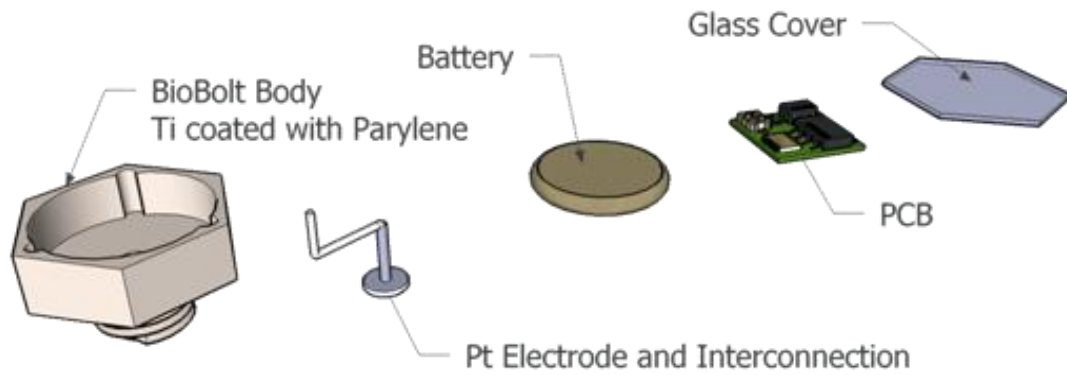
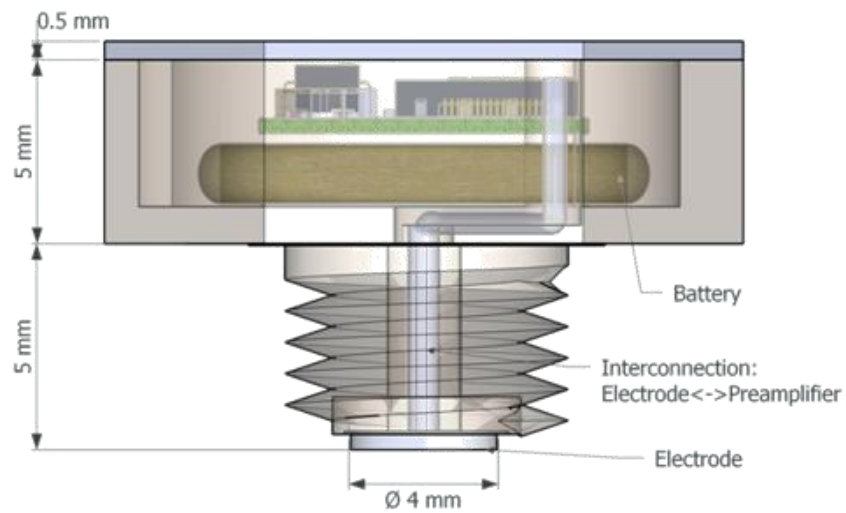
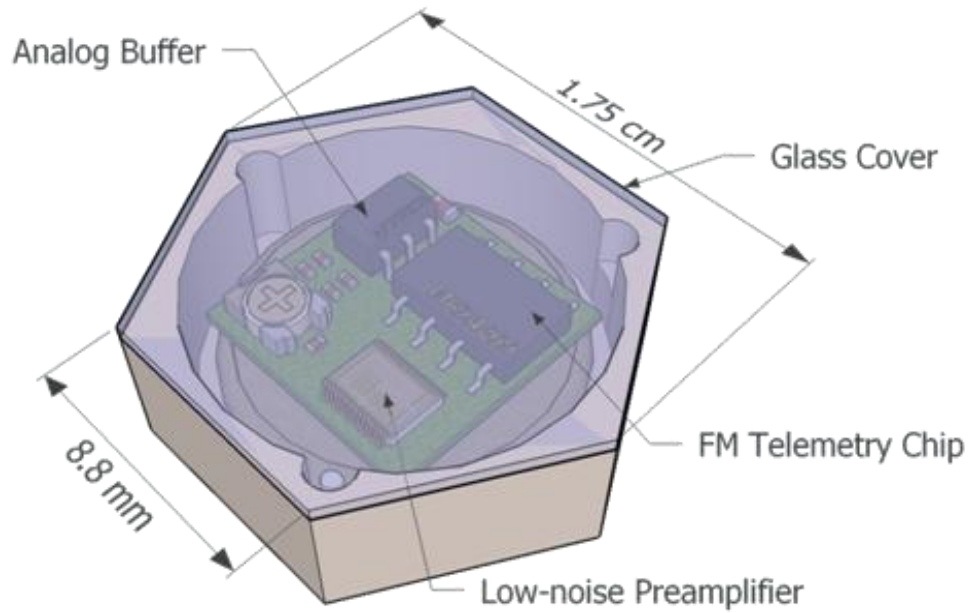


Figure 2-35: All dimensions of Implemented Implantable Device

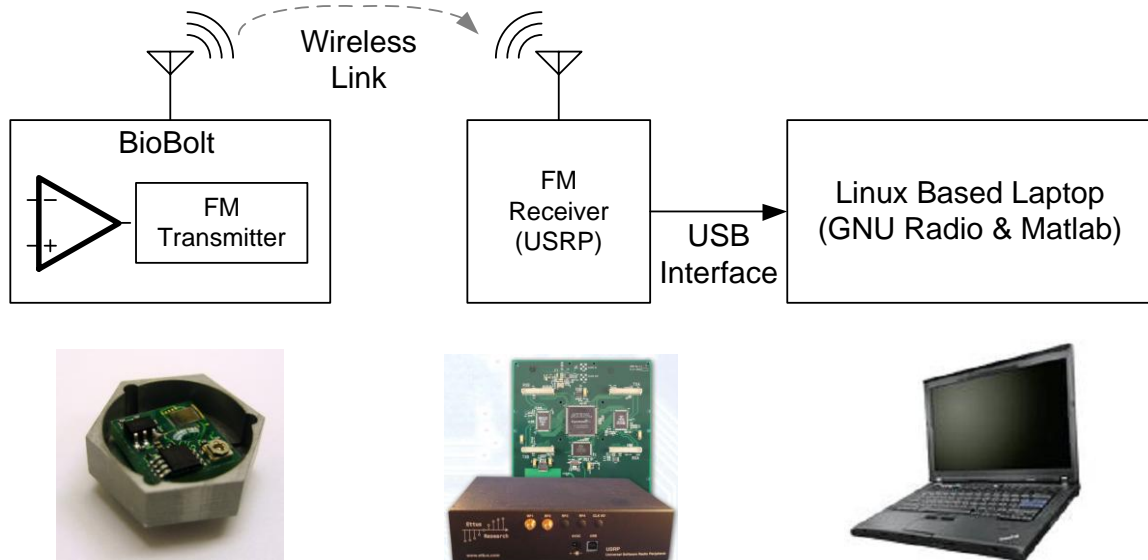


Figure 2-36: Overall System Architecture of Implantable Device Prototype 0

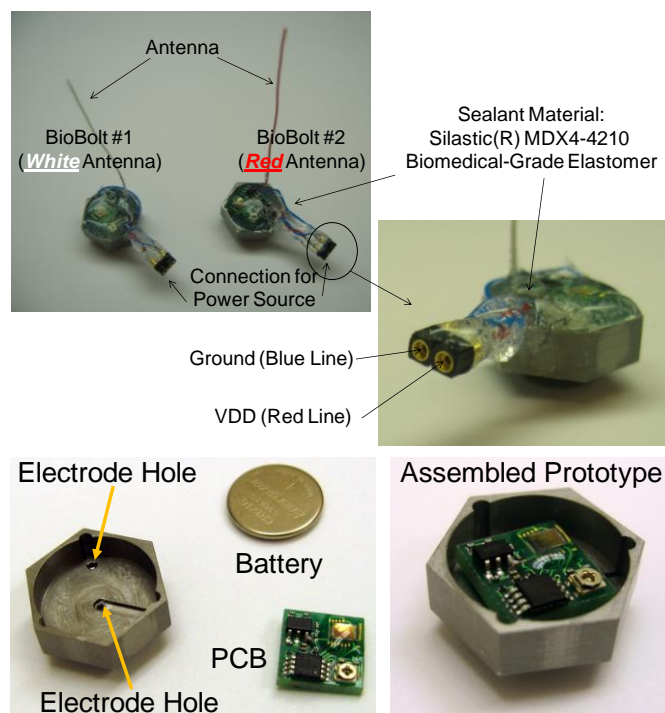


Figure 2-37: Assembled Implantable Device

Dow Corning [67] for the insulation between the integrated components, and the environmental tissues. All dimensions of the implantable device are shown in Figure 2-35. The assembled implantable device is shown in Figure 2-37. Two implantable devices are assembled and the operation was proved by test-bench measurement. To characterize the

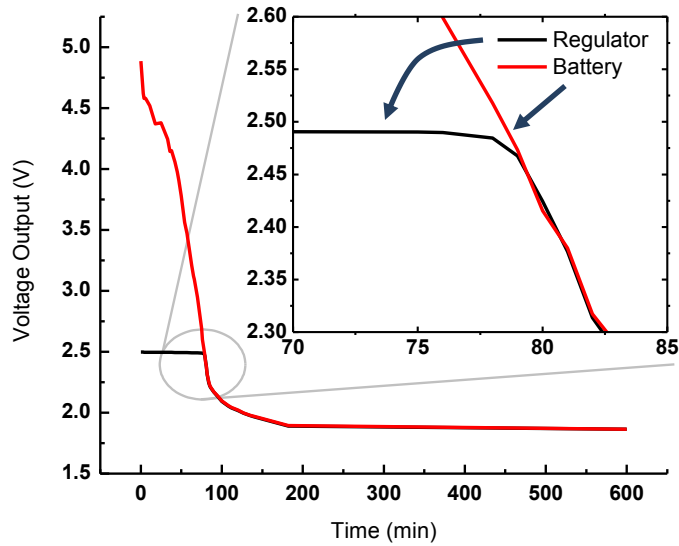


Figure 2-38: Battery Life Time

overall power requirement, the battery life time has been tested. The power for whole implantable device system is supplied by two-series batteries (Lithium Battery, 1216) and regulated by bias circuit. Using two-series batteries, the whole implantable device system can operate over 70 min before the regulator's output drops as shown in Figure 2-38.

## 2.7 Conclusion

To minimize the power and area, in this ENI-1, we have proposed single channel analog front with energy efficient pseudo open-loop amplifier and area and power efficient SAR ADC. The total power consumption for this system is  $1.7 \mu\text{W}$  at 2.5 power supply without a wireless FM telemetry.

The main goal of the proposed pseudo open-loop preamplifier is a power and area reduction. To save the area, we utilized the electrode capacitance and switched capacitor to realize the high pass filter and we could reduce the area by more than 50%. And, to achieve the power goal, here we proposed open-loop preamplifier with chopper stabilization and the power reduction was more than 30%.

In SAR ADC, typically, a reference voltage is fixed, and the sampled signal is modulated to find the final value using a binary weighted capacitor array. However, this capacitive array occupies the most area and consumes significant power to charge and discharge. To address this, we modulate not only the signal and but also reference together as shown here. This approach helps us to divide the capacitor array into two split array and effectively, reduce the area and power by a factor of 8 which is about more than 80% reduction.

The fabricated IC is assembled and packaged with customized miniaturized package as shown in the previous section. And, the recorded neural signal is transmitted with the FM telemetry wireless link by consuming 12mW. With CR1216 lithium coin battery, the developed wireless neural interface system can operate up to 70 min. The main factor to limit the lifetime of the system is the wireless communication using off-the-shelf components. In this next chapter, we will discuss a new concept of wireless communication using the skin, intra-skin communication (ISCOM), to mitigate the power requirement of the wireless communication block.



## CHAPTER 3

### WIRELESS SIXTEEN CHANNEL NEURAL INTERFACE CIRCUIT USING INTRA-SKIN COMMUNICATION FOR MODULAR EXPANDABILITY

In the previous Chapter, we developed and characterized the first prototype of the neural interface integrated circuit which has one channel analog front-end with FM telemetry. Based on the analysis and results of the system characterization, we have developed the sixteen channel analog front-ends with wireless intra-skin communication. In this chapter, we will discuss the low-power low-noise analog front-ends and the wireless intra-skin communication.

#### 3.1 Overall System Architecture

An overall block diagram of the proposed neural interface integrated circuit is shown in Figure 3-1. Whole electrical components are enclosed in a bolt-shaped Titanium fixture coated with Parylene and filled with Silastic for electrical insulation. This bolt-shape structure allows for simple implantation and removal. The whole system is placed in a hole in the skull, and is completely covered by skin to prevent any possible infection. The neural activities recorded from the sixteen flexible epidural electrodes are simultaneously amplified and digitized by an analog front-end block. The digitized outputs are serialized, encoded (Manchester Code), and transmitted wirelessly through the skin using ISCOM. For system-level power optimization, all blocks use either 0.5V or 1V supply voltages generated by internal regulators. Digital blocks are controlled by an

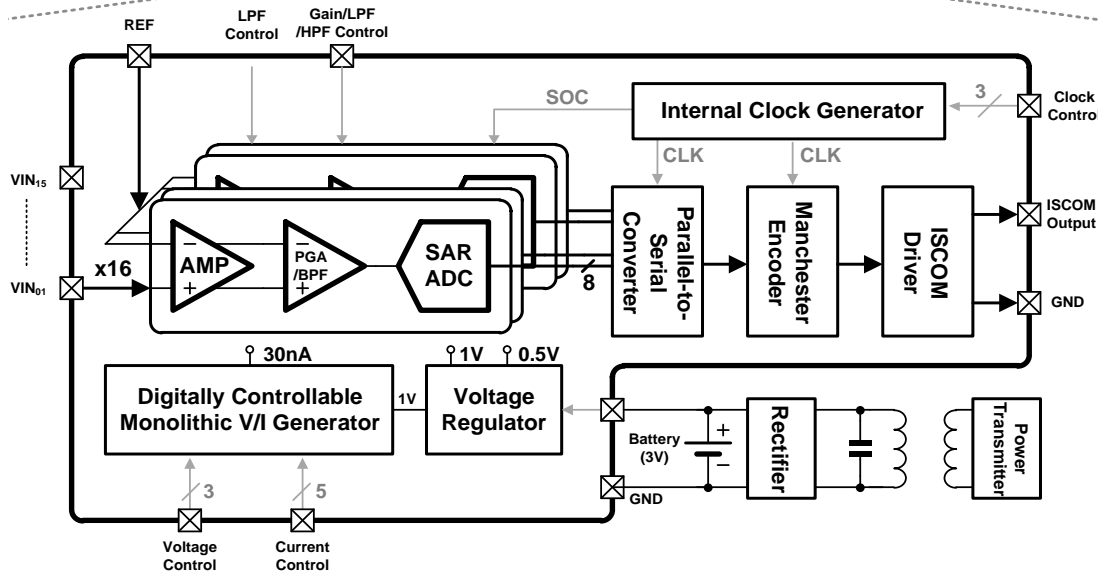
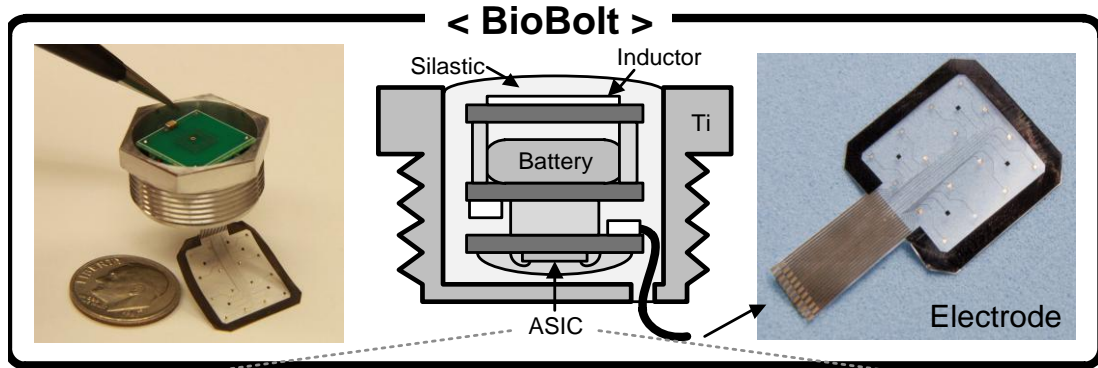


Figure 3-1: Overall architecture of the proposed system and block diagram of the ASIC

on-chip clock generator. All blocks inside of the ASIC are digitally controllable to accommodate various neural activities such as single neuron spike signal, local field potential, electrocorticogram, and electroencephalogram. This programmability can enable the system to be tolerable to any possible process variation.

The proposed system can be categorized into two blocks: (a) signal processing block including electrode, preamplifier, ADC, and intra-skin communication, and (b) supporting block including a voltage/current generator, voltage regulator, and clock generator. The following sections of this chapter will explain the function and requirements of each component.

### 3.2 Low-Noise and Low-Power Preamplifier with Quasi-Floating Body Transistors

The last decade has seen increasing demands for monitoring brain activity in freely behaving animals and humans for clinical diagnoses and neuroscientific research. In these fields, developing chronic and real-time monitoring interfaces has been one of the most important goals. To establish these reliable interfaces, a low-power low-noise implantable analog front-end preamplifier is essential for allowing chronic monitoring and recording of brain activities. Many analog front-end preamplifier circuit techniques have been investigated to achieve low-power low-noise performance. The design strategy of the operational transconductance ( $g_m$ ) amplifiers (OTAs) in the majority of previous works [34], [44], [55], [68–70] is to maximize  $g_m$  of the input transistors to gain noise-power efficiency by operating them in subthreshold (or weak inversion) region, and to minimize  $g_m$  of the rest of the transistors in the OTA to lower their noise contribution in the strong inversion region. There is still room to optimize the noise-power efficiency more.

In this section, we propose a low-power low-noise pseudo-double-gated push-pull preamplifier using quasi-floating body transistor to maximize the energy efficiency as an analog front-end for implantable neural interface system.

#### 3.2.1 Noise Analysis – General Preamplifier

As analyzed in section 2.2.2.3, the input-referred thermal noise of a differential preamplifier can be expressed as

$$\begin{aligned} \overline{v_{ni,total}^2} &= \frac{4kT}{\kappa_p \cdot g_{m1}} \left( 1 + \frac{g_{m3}}{g_{m1}} + \frac{4\kappa_p}{3} \cdot \frac{g_{m5}}{g_{m1}} \right) \\ &\approx \frac{4kT}{\kappa_p \cdot g_{m1}} \left( 1 + \frac{1}{A_{o1}} + \frac{4\kappa_n}{3} \cdot \frac{1}{\sqrt{IC_5}} \right). \end{aligned} \tag{Eq. 3-1}$$

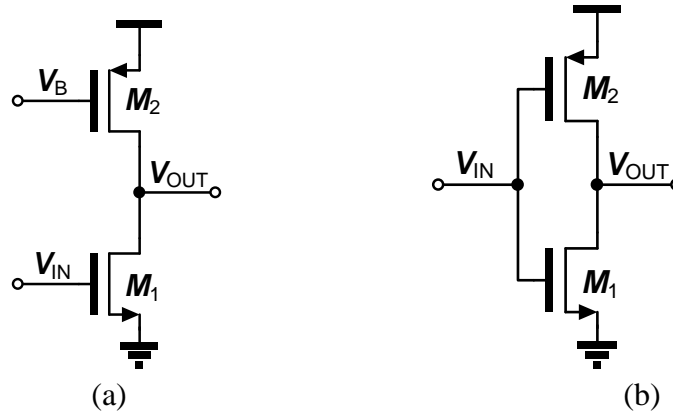


Figure 3-2: Single Common Source Topology with (a) Active Load and (b) Push-Pull Topology

From the Eq. 3-1, we can notice that to reduce the noise, we need to increase the input transistor's transconductance and minimize the transconductance of the other transistors. Based on the analysis from the previous section, we can maximize the input transistor's transconductance by operating the transistor in the weak inversion region where the MOSFET acts as a bipolar device. However, for a given current budget, the available transconductance is limited by the given process. To achieve better noise-power performance, it is desired to minimize the transconductance of the other transistors and it will be the best if we can eliminate that of the rest transistors. One method has been proposed in the previous section 3.2 using pseudo-open-loop topology [70] And, a source degenerated transistor was utilized [34]. In addition to this, many research groups have been working to eliminate the transconductance effectively [55], [71], [72]. We will discuss a push-pull topology in the following section.

### 3.2.2 Push-Pull Preamplifier Approaches

#### 3.2.2.1 Noise Analysis - Push-Pull Topology

The open-loop gain of a single common source amplifier with active load (Figure 3-2 (a)) can be expressed as shown in Eq. 3-2, while the corresponding input-referred noise

can be calculated by Eq. 3-3. If we assume that the transistor  $M_2$  does not introduce any noise, the theoretical minimum input referred noise can be expressed as shown in Eq. 3-4.

$$A_V = -g_{m1} \times (r_{o1} // r_{o2}) \quad \text{Eq. 3-2}$$

$$\overline{v_{n,in}^2} = \left[ \frac{8kT}{3} \cdot \frac{1}{g_{m1}} \left( 1 + \frac{g_{m2}}{g_{m1}} \right) \right] \cdot \Delta f \quad \text{Eq. 3-3}$$

$$\textit{Theoretical Minimum Input-referred Noise: } \overline{v_{n,in}^2} = \left[ \frac{8kT}{3} \cdot \frac{1}{g_{m1}} \right] \cdot \Delta f \quad \text{Eq. 3-4}$$

On the other hand, the open-loop gain of the single common source amplifier with push-pull topology (Figure 3-2 (b)) increases by a factor of two, as compared to the active load approach as shown in Eq. 3-5. If we design  $M_1$  and  $M_2$  to have a same transconductance,  $g_{m1} = g_{m2}$ , Eq. 3-6 can be rewritten as Eq. 3-7. The theoretical minimum input-referred noise power can be effectively reduced by a factor of two. With the push-pull topology, we can achieve twice the open-loop gain and half the noise power of the active load approach while maintaining the same amount of power consumption.

$$A_V = -(g_{m1} + g_{m2}) \times (r_{o1} // r_{o2}) \quad \text{Eq. 3-5}$$

$$\overline{v_{n,in}^2} = \left[ \frac{8kT}{3} \cdot \frac{1}{g_{m1} + g_{m2}} \right] \cdot \Delta f \quad \text{Eq. 3-6}$$

$$\textit{Theoretical Minimum Input-referred Noise: } \overline{v_{n,in}^2} = \frac{1}{2} \cdot \left[ \frac{8kT}{3} \cdot \frac{1}{g_{m1}} \right] \cdot \Delta f \quad \text{Eq. 3-7}$$

### 3.2.2.2 Frequency-Dependent R-C Switch (Quasi-Floating Gate Transistor)

However, it is difficult to find a meta-stable point to bias this push-pull topology. To address this problem, we can utilize a frequency-dependent RC switch shown in Figure 3-3. By connecting a large capacitive and resistive path to the gate terminal of the transistor, we can form a frequency-dependent RC switch as shown in Figure 3-3 (a,b).

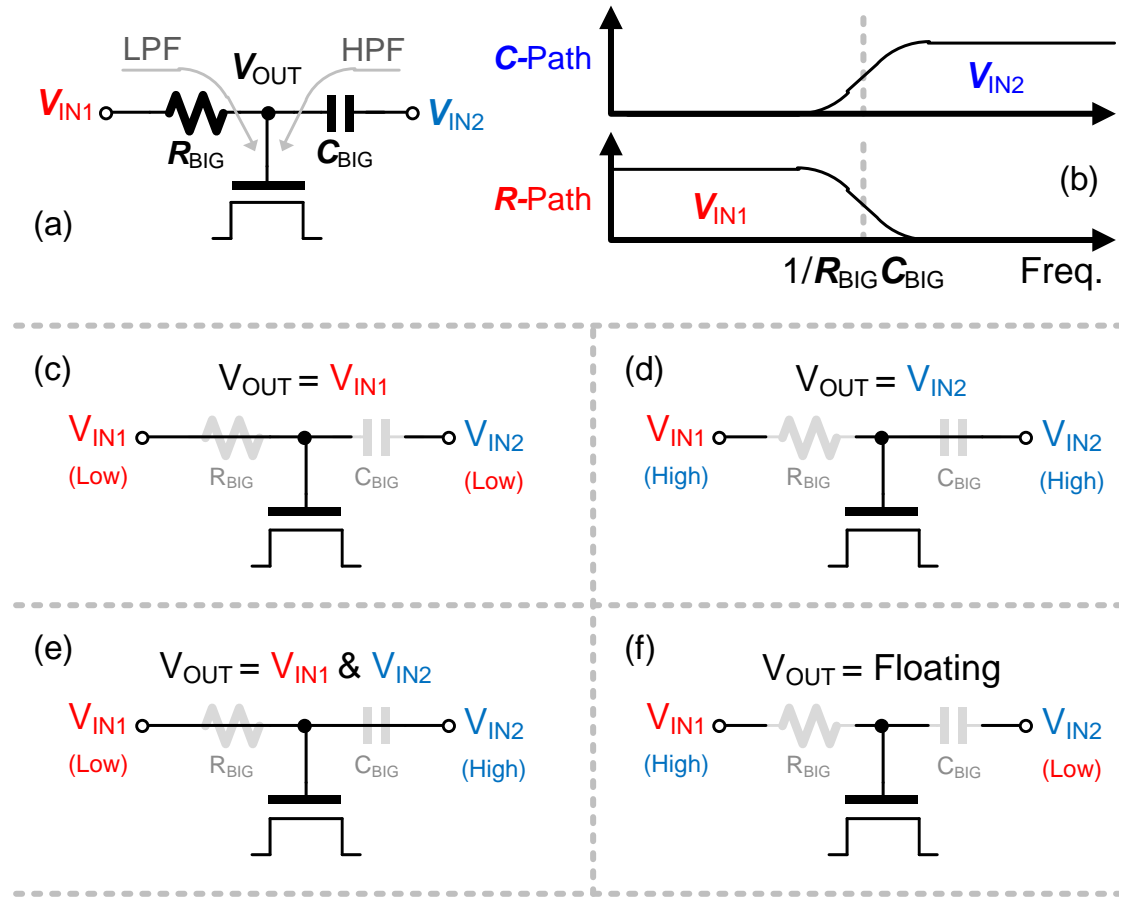


Figure 3-3: Frequency-Dependent R-C Switch

This RC switch can be operated in four different ways of (c~f) in Figure 3-3. According to the frequency of the signals, the gate voltage can be  $V_{IN1}$ (c),  $V_{IN2}$ (d),  $V_{IN1}&V_{IN2}$ (e), and floating (f). For our application, we will use case (e) to provide a bias through the resistive path and apply signal through the capacitive path.

### 3.2.2.3 Self-Biased Push-Pull Preamplifier

Using frequency-dependent R-C switch, we can configure the push-pull topology as shown in Figure 3-4 (a). Let us assume  $C_1$  and  $R_F$  form a corner at 0.1Hz. In this case, at the low-frequency region ( $<0.1\text{Hz}$ ), the resistive path is closed while capacitive path is open so that through the  $R_F$  path,  $M_1$  and  $M_2$  can form the diode-connected transistors and

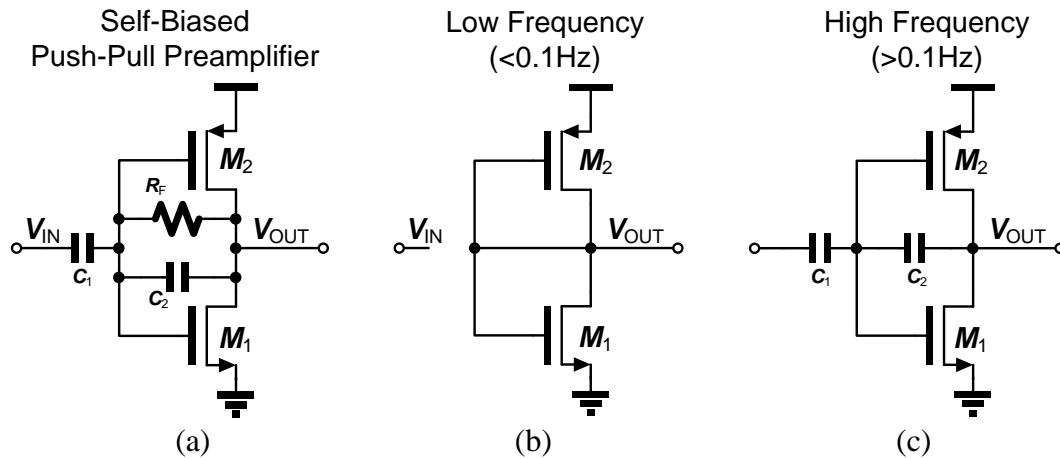


Figure 3-4: Self-Biased Push-Pull Pre-amplifier

bias themselves. On the other hand, at the high-frequency region ( $>0.1\text{Hz}$ ), the neural signal can be amplified with a gain of  $A_{CL}=|C_1/C_2|$ .

### 3.2.3 Double-Gated Push-Pull Pre-amplifier using Quasi-Floating Transistor

As shown in the previous section, the push-pull topology performs better than a pre-amplifier with active load in terms of noise-power efficiency, because the input transistors act as a load transistor as well. In addition to this push-pull topology, to further enhance transconductance, the body is also utilized as a second gate. The quasi floating is named because the body bias is biased by the leakage current through the source and body interface. In this section, the quasi floating body transistor is proposed and utilized to improve the efficiency furthermore.

#### 3.2.3.1 Quasi-Floating Body Transistor

The quasi-floating body transistor is shown in Figure 3-5. Contrary to the conventional connection, in the quasi floating body transistor, the body is not connected directly to any terminals. Instead, the floating body is biased through the junction diode

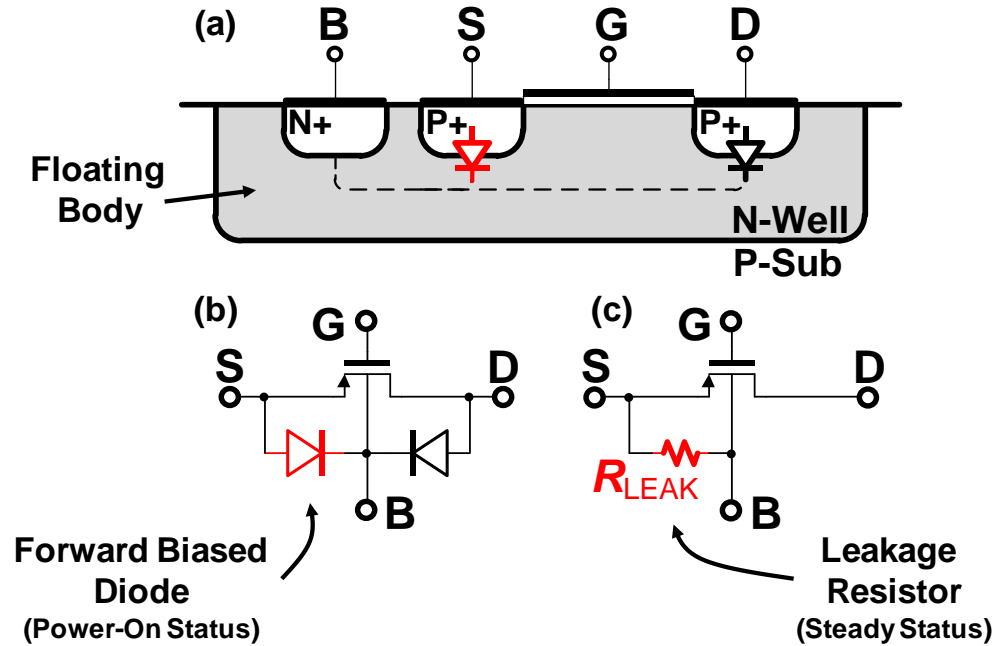


Figure 3-5: Quasi-Floating Body Transistor

between source and body. The operation can be explained as follows: At the moment when device turns on, the source terminal sets to  $V_{DD}$ , while the other terminal is still ground. This connection puts the S-B diode in forward bias and this forward biased S-B diode can bias the potential of the body. As the potential of the body approaches that of the source, this junction diode will work as a big leakage resistor. And, eventually, the floating body is biased up to the potential of the source terminal. In other words, without any direct connection to bias the body, the floating body is connected to the source through the junction diode. The configured transistor is named as quasi-floating body transistor.

### 3.2.3.2 Pseudo-Double-Gated Transistor

As for the noise-power efficiency, we need to maximize the  $g_m$  of the transistor. To achieve this goal, typically, MOSFET's BJT-like behavior in the subthreshold region is utilized. On the top of this, in this work, we introduce the pseudo-double-gated transistor



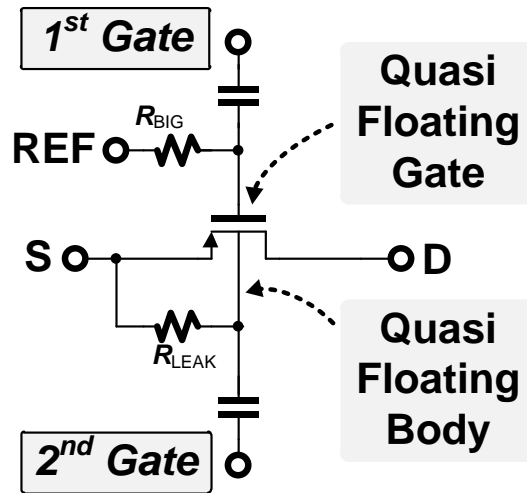


Figure 3-6: Pseudo Double Gate Transistor using Quasi Floating Body

to maximize the noise-power efficiency furthermore by using the body as a secondary gate to increase the effective  $g_m$ . This pseudo-double-gated transistor is using the frequency-dependent R-C switch discussed in the section 3.2.2.2 as shown in Figure 3-8. The R-C switch at the gate terminal forms the quasi-floating gate as first gate, and the R-C switch at the body terminal forms the quasi-floating body as second gate. By applying the signal into the capacitive path connected to gate and body, we can expect the effective transconductance will increase by a factor of 1.2 as shown in Eq. 3-8, where  $\eta$  is a body-effect transconductance ratio,  $g_{mb}/g_m$ , and the typical value of  $\eta$  is about 0.2~0.3. From this equation, we can expect the estimated input-referred noise can be reduced by 20% with the same power consumption.

$$g_m'' = g_{m1} + g_{mb1} = g_{m1} (1 + \eta) \approx 1.2 \times g_{m1} \quad \text{Eq. 3-8}$$

### 3.2.3.3 Design Consideration

There are several issues when designing the proposed pseudo-double gated push-pull preamplifier. In this section, we will discuss the possible issues such as (1) limited output

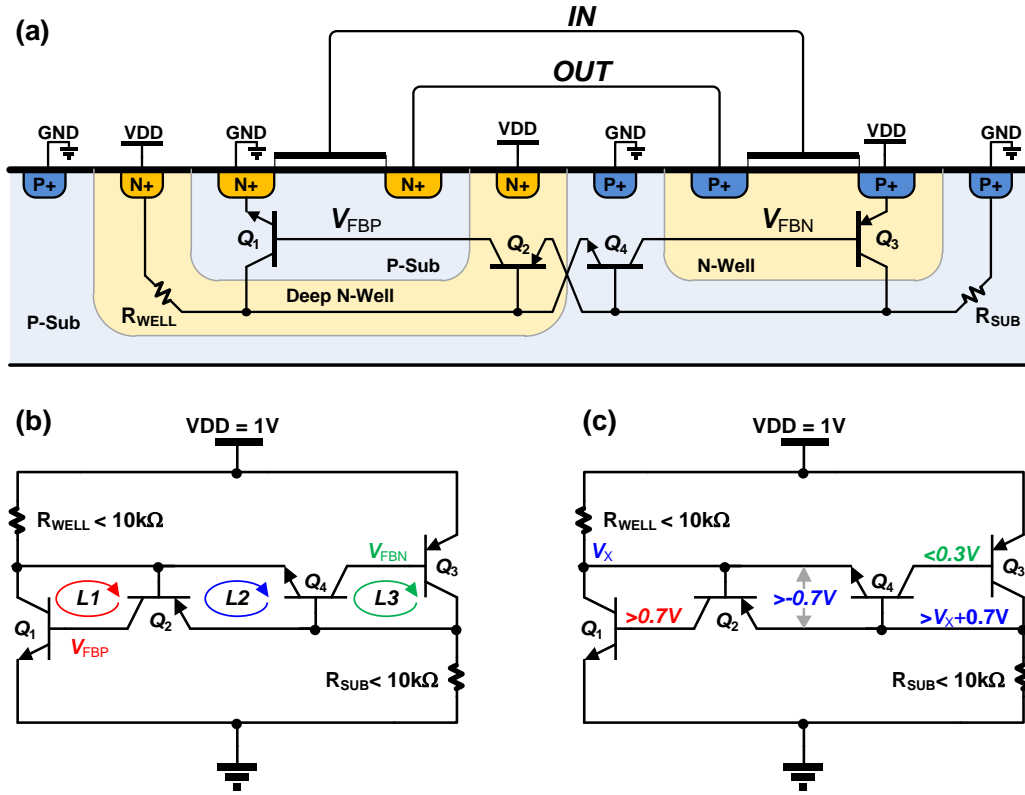


Figure 3-7: Simplified Latch-up Model for the Proposed Preamplifier: (a) Cross Section View, (b) Equivalent Latch-up Circuit indicating possible positive feedback loop, and (c) Latch-up Conditions for each parasitic BJT

swing due to the low-voltage operation, (2) offset by threshold voltage variation due to the quasi-floating body, and (3) latch-up due to the quasi-floating body.

1) *Limited Output Swing*: In order to save power consumption, low-voltage power supply, 1V, is utilized. However, this low-voltage is limiting the voltage swing of the output node. Especially, the cascode transistor to boost the gain limits the allowable output swing furthermore below 300mV. This limited output swing sets the maximum allowable gain in the preamplifier below 1~200 V/V. In our design we choose a gain of 100 V/V to minimize any other possible non-linearity.

2) *Offset due to Threshold Voltage Variation*: Since the body of the transistor is quasi-floating, it can easily change the body potential. Consequentially, this change of the

body potential affects the threshold voltage of the transistor, and thus the output offset. To address this issue, we also make the closed-loop path which can regulate the body potential to be ac-ground. In addition, in the following signal processing units such as band-pass filter and programmable gain amplifier, we design the ac-coupled input stage in order to reject low-frequency offset.

3) Latch-Up Issue: The most critical issue in the proposed preamplifier is the latch-up. Because the body is floating and can induce an expected signal that can turn on the lateral BJT. This lateral parasitic BJT can form the direct current path from VDD to GND and eventually cause the device failure. To investigate the latch-up possibility of the proposed preamplifier has been analyzed in this section. The simplified cross section view of the preamplifier can be drawn as shown in Figure 3-7. For simplicity, the cascode transistors and bias transistor are ignored. For quasi-floating body for both NMOS and PMOS transistors, deep N-well option is utilized which is a given option from the foundry. From the cross section (Figure 3-7(a)), we can draw an equivalent latch-up schematic (b). And, with careful layout, the  $R_{WELL}$  and  $R_{SUB}$  are well below 10k $\Omega$ . In order for the latch-up to occur, the conditions for each *BJT* are indicated in (c). The most critical nodes in the equivalent circuit are the  $V_{FBN}$  and  $V_{FBP}$  which is connected output of the preamplifier. These nodes can vary from rail to rail and consequently affect the floating node. The possible latch-up can start when these nodes become  $V_{FBP} > 0.7V$  ( $V_{FBN} < 0.3V$ ). This can allow the current to flow through the  $Q_1$  ( $Q_3$ ) and may satisfy the condition of  $V_Y > V_X + 0.7V$ . Consequently, the loop 2 which is consists of  $Q_2$  and  $Q_4$  can be activated. And all the BJT may be in the positive feedback to form the direct current path from VDD to GND which is latch-up condition. However, this latch-up would not occur due to the

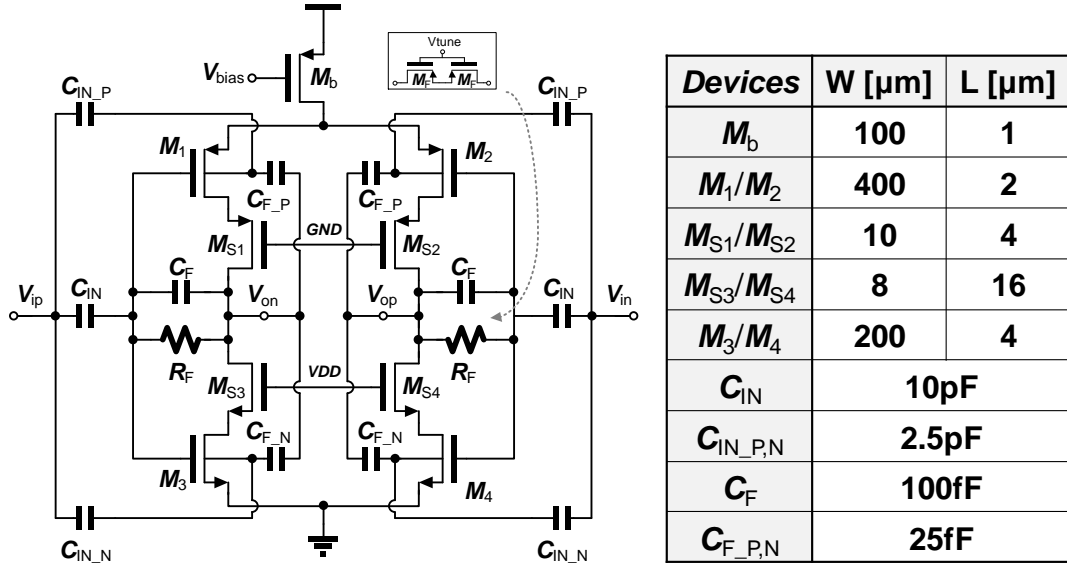


Figure 3-8: Proposed Pseudo-Double-Gated Push-Pull Pre-amplifier using Quasi-Floating Body Transistors

following two reasons: (1) Due to a noise spike or an improper circuit hookup, the output of the pre-amplifier can cause sufficient current to satisfy the  $V_X < 0.3\text{V}$  and  $V_Y > 0.7\text{V}$ . However, in the twin well structure, the intermediate parasitic lateral BJT can effectively prevent to turn on  $Q_1$  and  $Q_3$ . (2)  $V_{FBP} > 0.7\text{V}$  ( $V_{FBN} < 0.3\text{V}$ ) condition cannot occur in the practical case. Because both nodes are connected with output node, both node must be coupled in the same direction, for example, both nodes become over  $0.7\text{V}$  or below  $0.3\text{V}$ . This connection ensures that both  $Q_1$  and  $Q_3$  turn on simultaneously. And, (3) in order to satisfy the  $V_Y > V_X + 0.7\text{V}$ , more than  $100\mu\text{A}$  needs to flow through the  $Q_1$  and  $Q_3$  which is very difficult to happen because this condition puts the  $Q_1$  and  $Q_3$  in the saturation region and limits the current.

### 3.2.3.4 Proposed Pseudo-Double-Gated Push-Pull Pre-amplifier

In this section, we proposed pseudo-double-gated push-pull pre-amplifier. The proposed pre-amplifier is utilizing the push-pull topology with pseudo-double gated

technique. The overall schematic of the preamplifier is shown in Figure 3-8. The effective transconductance can be calculated using Eq. 3-9. From the equation, we can expect the  $g_m$  of the proposed preamplifier can increase by a factor of 2.4. And, the theoretical input-referred noise power will be reduced by a factor of 2.4 compared to the conventional two-stages OTA.

$$G_m = \underbrace{g_{m1} + g_{m3}}_{\text{Push-Pull Stage}} + \underbrace{g_{mb1} + g_{mb3}}_{\text{Quasi-Floating Body}} \approx 2(g_{m1} + g_{mb1}) \approx 2.4 \times g_{m1} \quad \text{Eq. 3-9}$$

$$\overline{v_{n,in}^2} = \frac{1}{2} \times \left[ \frac{16kT}{3} \cdot \frac{1}{g_{m1} + g_{mb1}} \right] \cdot \Delta f \approx \frac{1}{2.4} \times \left[ \frac{16kT}{3} \cdot \frac{1}{g_{m1} + g_{mb1}} \right] \cdot \Delta f \quad \text{Eq. 3-10}$$

In this topology, the closed-loop gain is determined by the capacitive ratio between  $C_{IN}$  and  $C_F$  (or  $C_{IN,P,N}$  and  $C_{F,P,N}$ ) which is set to be 100 in this design as shown in Figure 3-8. To achieve this required gain of 100 with a single stage preamplifier such as the proposed preamplifier,  $M_{S1-4}$  transistors are utilized to boost the output impedance. The simulation result shows that the open-loop gain of the preamplifier is over 80dB. All the dimension of transistors and capacitors are indicated in the Figure 3-8.

$$A_{v\_QFB} = \frac{-(g_m + g_{mb})r_{out}}{1 + \frac{C_F}{C_F + C_{IN}} g_m r_{out} + \frac{C_{F-P,N}}{C_{F-P,N} + C_{IN-P,N}} g_{mb} r_{out}} \quad \text{Eq. 3-11}$$

$$\approx \frac{-(g_m + g_{mb})r_{out}}{1 + \frac{C_F}{C_F + C_{IN}} (g_m + g_{mb})r_{out}} \approx -\frac{C_{IN}}{C_F}$$

To suppress the low-frequency offset and drift from the electrode ( $\sim \pm 50\text{mV}$ ), input series capacitance  $C_{IN}$  and  $R_F$  forms the high pass filter with a corner frequency below 1Hz. To realize this low frequency corner frequency, we use 10pF and a pseudo resistor using transistors. The resistance value is controlled by the tunable gate as shown in Figure 3-8.

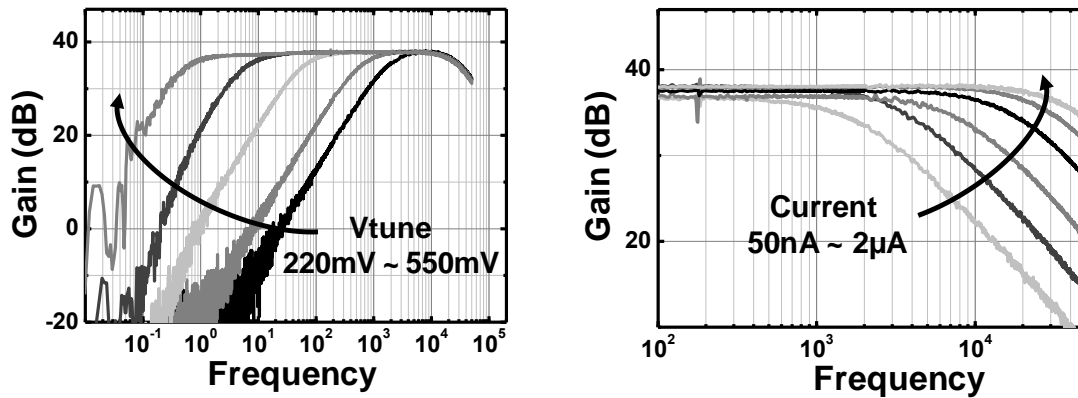
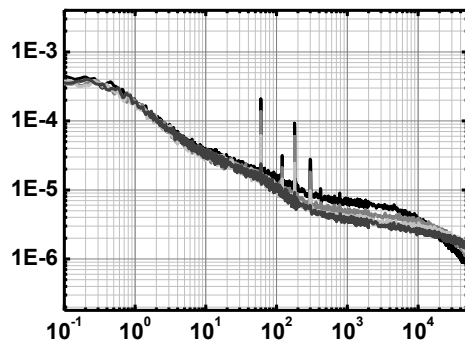


Figure 3-9: Programmable High and Low Corner Frequency.



Supply Voltage	1V
Power Consumption	0.5 $\mu$ W
Mid-band Gain	37.5 dB
Input Referred Noise	4.26 $\mu$ Vrms (1~500Hz) / 5.62 $\mu$ Vrms (10Hz ~ 10kHz)
NEF	5.2 (1~500Hz) / 1.69 (10Hz ~ 10kHz)
CMRR / PSRR	35 dB / 48 dB
Active Area	180 $\mu$ m x 500 $\mu$ m

Figure 3-10: Measured Input-Referred Noise for Various Bias Conditions and performance summary

### 3.2.4 Measurement Results

At a power consumption of 0.5  $\mu$ W, measured mid-band gain, bandwidth, and thermal noise floor are 37.5 dB, 18 kHz, and 47 nV/ $\sqrt$ Hz, respectively. The preamplifier can be configured for various applications as shown in Figure 3-9. The measured input-referred rms noise is 4.26  $\mu$ Vrms for 1Hz to 500Hz (NEF = 5.2) and 5.62  $\mu$ Vrms for 10 Hz to 10 kHz (NEF=1.69), respectively (Figure 3-10). The preamplifier performance has been summarized in the Figure 3-10. To verify the preamplifier performance with internally generated power supply, the output noise has been measured with various internal/external power supplies conditions as shown in Figure 3-11. The measured CMRR and PSRR shows about 35dB and 48dB.

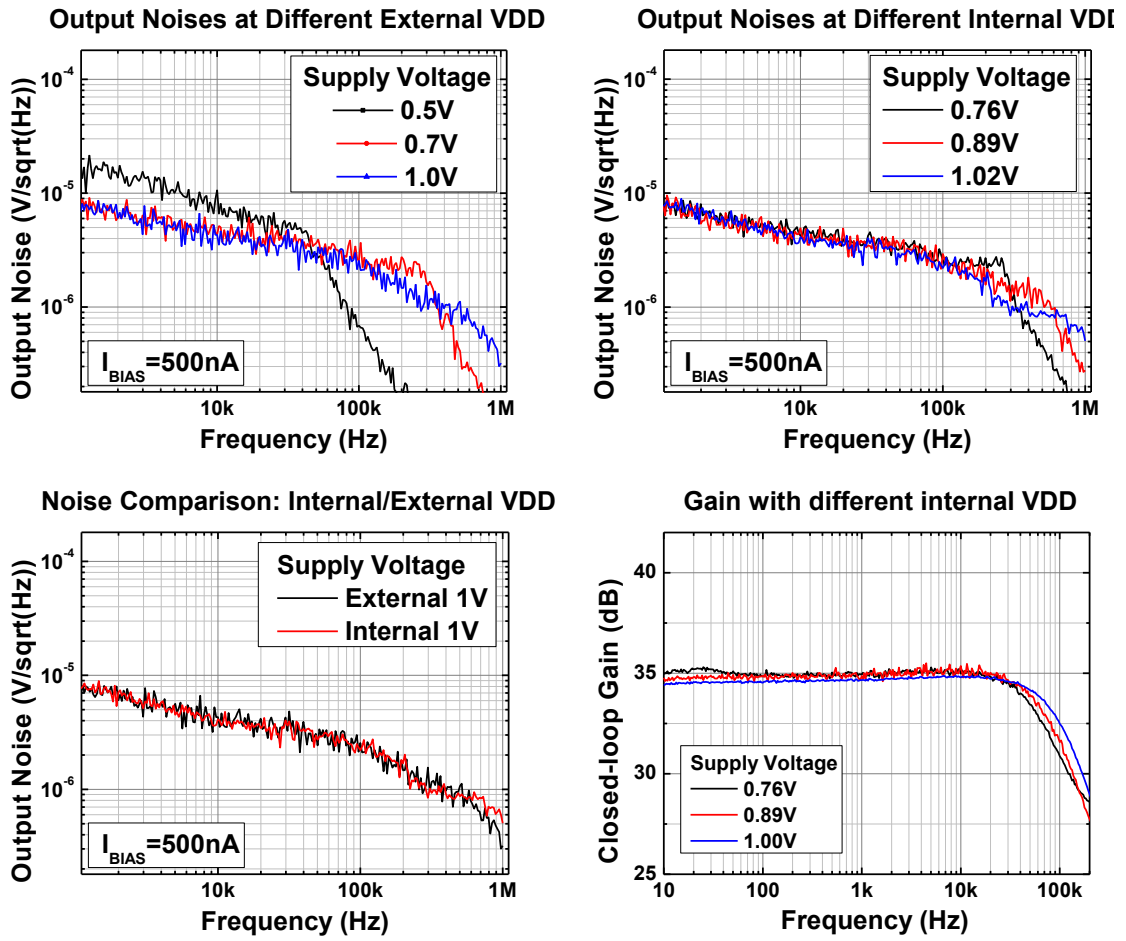


Figure 3-11: Measured Output Noise for Various Internal/External Power Supplies

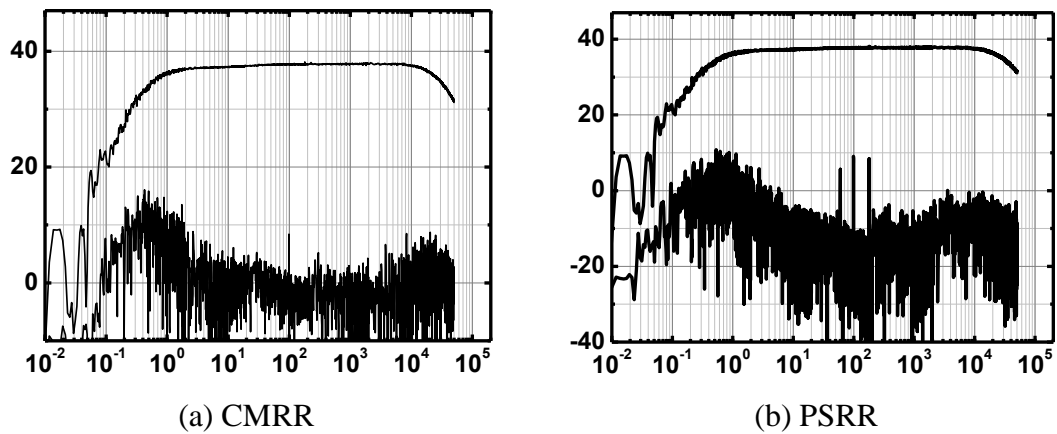


Figure 3-12: Measured CMRR and PSRR

### **3.3 A 0.5V Successive Approximation Register (SAR) Analog-to-Digital Converter**

Recently, the progress in CMOS and MEMS technologies has enabled the development of miniaturized implantable biomedical microsystems operated in extremely low-power and fully integrated with embedded mixed-signal circuits for multi-channel neural recording [73]. One of the critical blocks in the analog frontend of the implantable systems is analog-to-digital converter (ADC), which should meet the stringent power budget and area constraint. To reduce the power consumption of any given circuit, the simplest way is to lower the power supply. However, in low-voltage ADCs, additional circuit blocks are required to enhance the performance such as bootstrap sampling [74–76] or dynamic comparators. Especially, in the multi-channel implantable systems, a clock/timing generator should be integrated to reduce the overall system volume. In the previous synchronous SAR ADCs, the clock frequency should be at least ten times higher than sampling frequency to generate adequate control signals. This high frequency clock generator consumes huge power and can easily interfere analog signals. As a possible solution for this, asynchronous ADCs have been proposed to eliminate clock generators. However, the asynchronous feature requires additional decision circuits, and may cause meta-stability and time-varying sampling rates. This decision circuit cannot be shared among the asynchronous ADCs. Therefore, in multi-channel system implementations, it may consume more power and area than the synchronous ADCs which can share one clock/timing generator among multiple ADCs.

The feature size selection is also an important factor that will determine overall system performance. For example, in the mixed-signal circuits implemented using a CMOS feature size below 100nm [77–81], the digital blocks can achieve high speed at



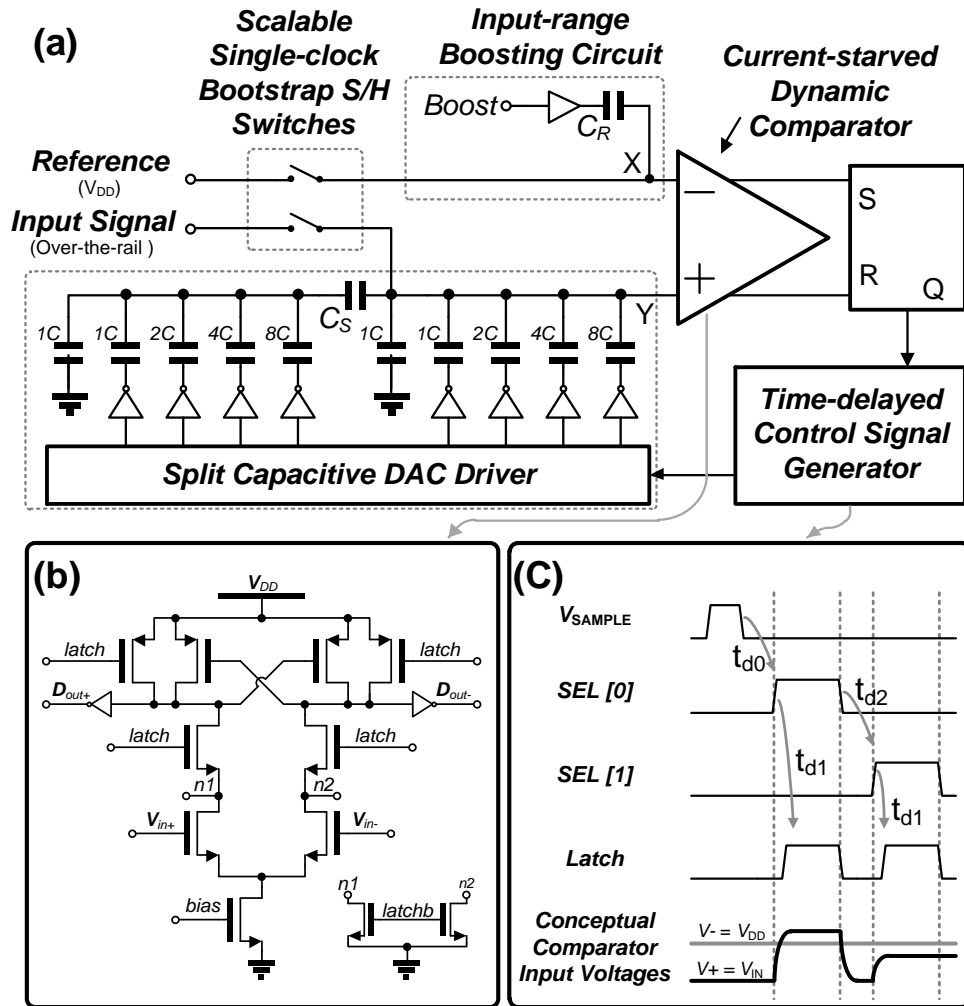


Figure 3-13: (a) Overall block diagram of the proposed SAR ADC, (b) low-voltage current-starved dynamic comparator, and (c) timing diagram

low power consumption; however, the performance in analog blocks can significantly degrade. Dynamic range reduction and device mismatch [82] are main concerns. Also, noise performance degrades due to the gate leakage current [83] and the benefit of area and power consumption cannot be easily gained.

With all these in considerations, in this section, we present a 0.5V 20fJ/c-s 8bit rail-to-rail synchronous SAR ADC fabricated in 0.25 $\mu$ m technology. We especially paid attention to significantly reduce power consumption in the timing generator, by proposing a programmable time-delayed control unit. One additional feature that the proposed ADC

can provide is the expandability of the input range above the rail ( $>0.5V$ ), boosted by one bit, without any additional hardware.

### 3.3.1 Overall Architecture

Figure 3-13 (a) shows an overall block diagram of the proposed SAR ADC. It consists of low-power voltage-scalable single-clock (LVS) bootstrap circuit, 8bit split-CDAC, current-starved dynamic comparator, timing generator using delay elements, and an input range boosting circuit. The operation can be explained with the timing diagram as shown in Figure 3-13 (c). To realize rail-to-rail input signal operation,  $V_{DD}$  is used as a reference. The input and reference ( $=V_{DD}$ ) are sampled into CDAC and  $C_R$ , respectively, at  $V_{sample}=high$  using the LVS bootstrap circuit and compared to each other. Because  $C_R$  is identical to the CDAC, any possible leakage and charge injection at node Y during the conversion can be compensated. As the conversion steps proceed, the potential at node Y is approaching to that of node X ( $V_{DD}$ ). All the control signals shown in Figure 3-13 (c) are generated using the time-delayed control units and its combination. The following section will explain the each components of the ADC.

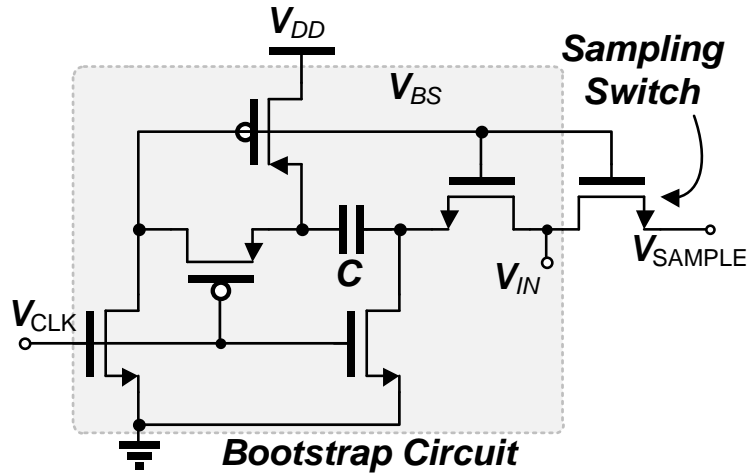
### 3.3.2 Low-Voltage Current-starved Dynamic Comparator

Figure 3-13 (b) shows the schematic of the dynamic comparator. We implemented a power-efficient current-starved dynamic latched comparator. In order to minimize the conversion hysteresis that may be induced from low driving voltage ( $0.5V$ ) of the reset switches, transmission gates are used. (But in the figure, only the one-type of transistors are shown for simplicity.) One possible concern of this current-starved technique is the speed degradation of the comparator. However, this would not be a problem in our target applications because the bandwidth of the neural signals is limited less than few tens of

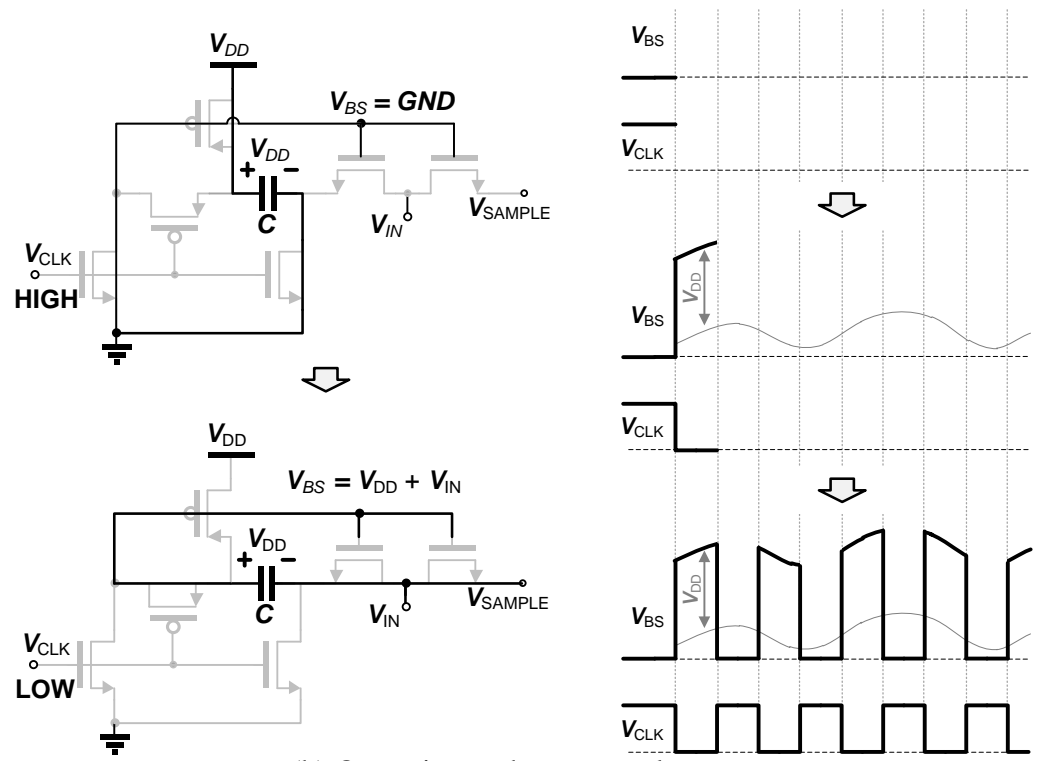
kHz. Therefore, the speed and power constraints can be easily compromised. As for the rail-to-rail input range, power supply voltage ( $V_{DD}$ ) is utilized as the reference as described in the previous section. Due to the low supply voltage, this connection can ensure the operation of input transistors to be in saturation region.

### 3.3.3 Low-Power Voltage-Scalable Single-clock Bootstrap

One of the important blocks in the low-voltage operation is a bootstrap circuit. The previous bootstrap techniques proposed by [2, 3] are complicated and cannot be realized in advanced submicron technologies due to breakdown. The local boosting switch suggested by [4] requires two phase clock signals and cannot handle the input range above the rail. In this paper, we propose a robust and low-power voltage-scalable single-clock (LVS) bootstrap circuit as shown in Figure 3-14. The basic idea comes from voltage multiplier circuitry [84]. The proposed bootstrap circuit can generate bootstrapped sampling signals, operate only with a single clock signal ( $V_{SAMPLE}$ ), and be easily expanded to various output voltage levels by simply adding additional stages. The LVS bootstrapped sampling signal ( $V_{BS}$ ) output can be expressed by  $V_{SAMPLE} = N \times V_{DD} + V_{IN}$ , where  $N$  is the number of stages. Taking advantage of the larger feature size ( $0.25\mu\text{m}$ ) and high affordable voltage swing ( $2.5\text{V}$ ), the proposed LVS bootstrap switches are robust and immune from gate oxide breakdown problems, and can be easily scaled up to five stages to generate up to  $2.5\text{V}$ . The operation can be performed in two phases: (a) precharge phase, and (b) bootstrap phase. As shown in Figure 3-14 (b), the operation can be explained as follows: during the precharge phase,  $V_{SAMPLE}$  is high,  $M_{1-5}$  are ON and  $C_1$  and  $C_2$  are charged to  $V_{DD}$ , while  $V_{BS}$  is GND. During the bootstrap phase,  $V_{SAMPLE}$  is low,  $M_{6-8}$  is ON and  $V_{BS}$  becomes  $2V_{DD}+V_{IN}$ . During this phase



(a) Scalable bootstrap circuit



(b) Operation and conceptual output

Figure 3-14: Low-power voltage-scalable single-clock bootstrap circuit: (a) Two-stage bootstrap circuit, and (b) operation and output.

(bootstrap phase),  $V_{IN}$  is sampled by  $M_S$  with the bootstrapped signal  $V_{BS}$ . For the proper operation, it is important that  $M_{4-6}$  and  $M_S$  should be also controlled by the bootstrapped signal ( $V_{BS}$ ). The settling time of  $V_{BS}$  is proven to be within one clock cycle by simulation. The conceptual bootstrap output signal is also shown in Figure 3-14 (b).

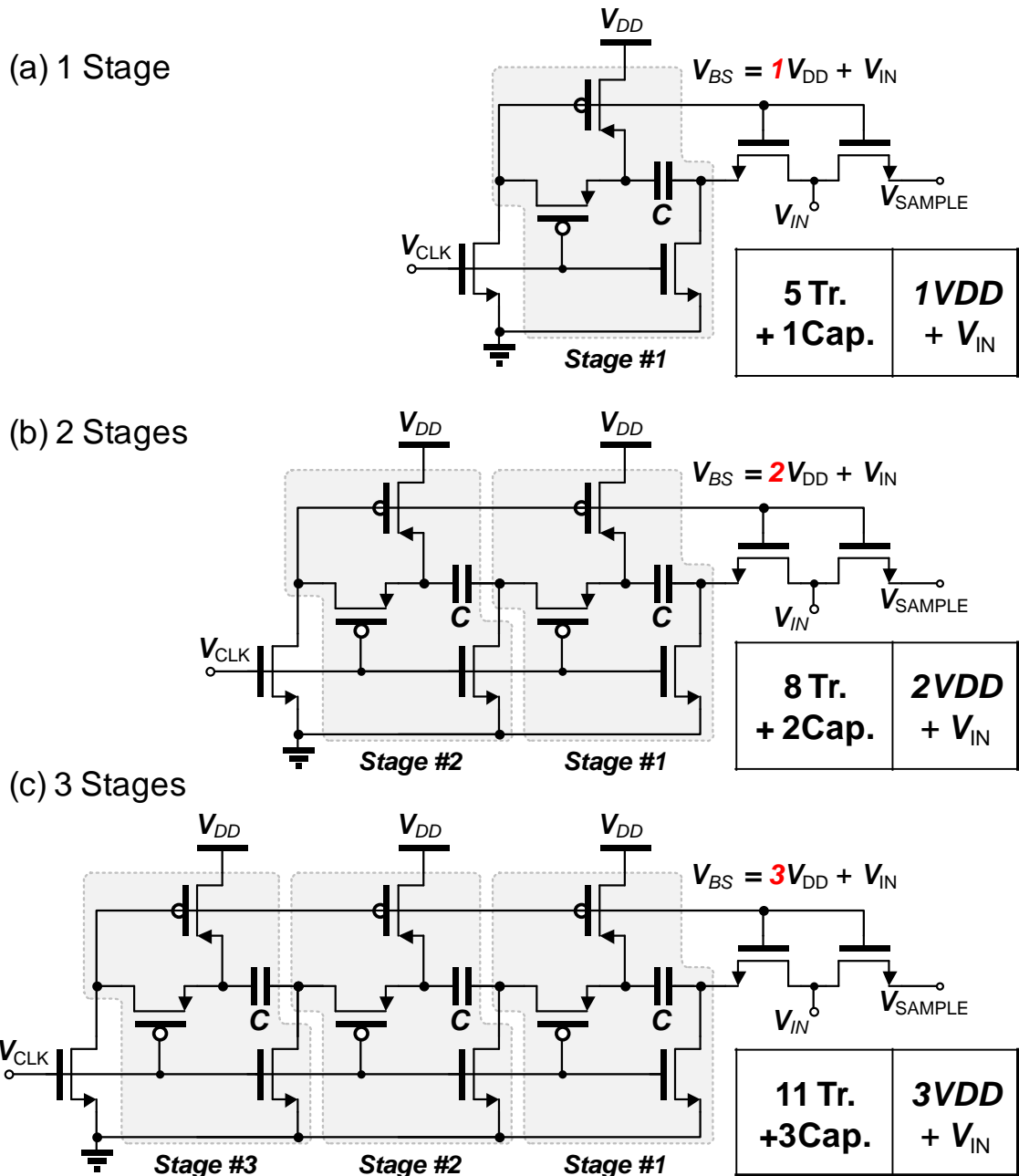


Figure 3-15: Expandability and Scalability of the Proposed Bootstrap Switch

### 3.3.4 Programmable Time-delayed Control Unit

To generate the control signals for ADC operation, we employed a time-delayed control unit which is digitally controlled and programmed to generate any shape of signals by combining multiple different control units as shown in Figure 3-16. The

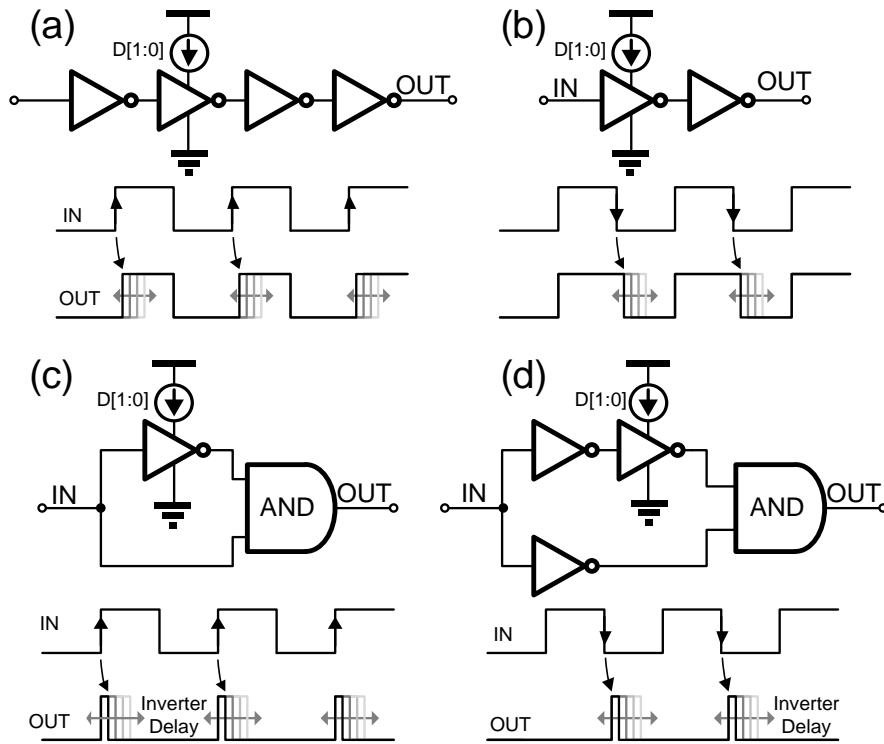


Figure 3-16: Positive/Negative edge-triggered time-delayed control units: (a-b) duty-cycle controllers, (c-d) spike generators.

proposed control units can generate either positive or negative edge-triggered signals.

The timing generator has the following features:

(1) *Time-delayed control unit*: As shown in Figure 3-16, the control units can be categorized into two types: (1) duty-cycle controller, and (2) spike signal generator. Both types of control units can generate positive or negative edge-triggered signals. Each control unit has a digitally controllable delay unit to change the pulse width and location. These control units do not require any high-speed internal clock signals; therefore, consume much less power. These control units can be shared in the multi-channel implantable system to save power and area. Furthermore, each control unit is discrete so that they cannot only operate individually, but also be combined with each other to generate complex control signals.

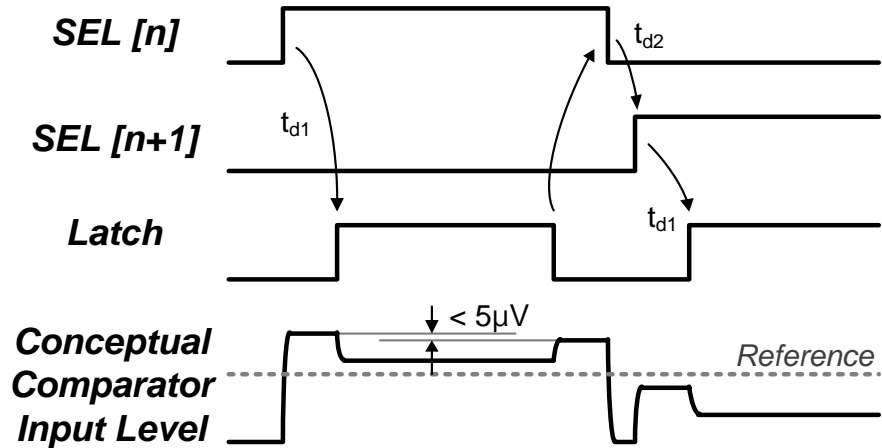


Figure 3-17: The conceptual timing diagram and comparator input level of the Kick-back tolerant operation

(2) *Kick-back tolerant operation*: Although the dynamic latched comparator is power-efficient, it can easily degrade the performance (e.g., offset and linearity) due to kickback noise during the conversion. This kickback noise from the coupling effect depends on input signals and transistor operation regions. However, this noise can be easily minimized by ensuring that the reset is completed before updating C-DAC value as shown in Figure 3-17. In other words, the delicate control timing can reverse the injected charge into exactly the same as before the comparison. The simulation result shows that the error induced from kick-back is suppressed below  $5\mu\text{V}$  using the proposed technique. Had the clocked timing generator been used, however, complicated blocks would have been required with high-speed clock signals; thus resulting in high power consumption. In our design, the time-delayed control unit allows this control signal to be generated with much less power and reduced complexity.

### 3.3.5 Input Range Boosting: Additional Range and Resolution

As mentioned, the proposed ADC can expand the input-range above the power supply without any additional power source or hardware. This additional feature can be achieved

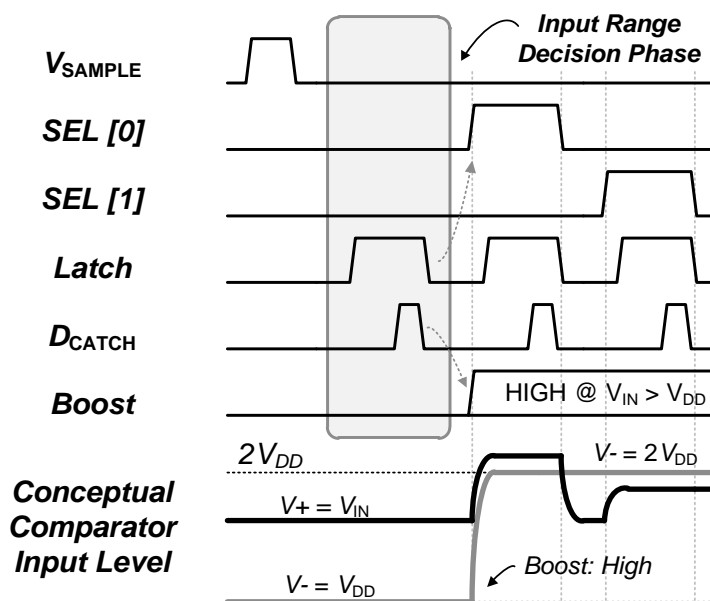


Figure 3-18: The conceptual timing diagram for the input range boosting

by simple modification of the control signals as shown in Figure 3-18. Before the  $SEL[0]$  signal is initiated, the comparator compares the input range to check if it is higher than the power supply. Once it is above the rail (power supply), the Boost signal becomes High and the reference signal is boosted up to  $2V_{DD}$  through  $C_R$  in Figure 3-13. Effectively, this input range decision can boost the resolution of ADC by one bit. However, it should be noted that, during the input range boosting operation, the input transistor is in the deep linear region which decreases the transconductance and the accuracy. As a result, the SNDR of the input-range boosted ADC decreases by 10dB.

### 3.3.6 Measurement Results

The proposed ADC is fabricated in  $0.25\mu\text{m}$  1P5M CMOS technology with 0.5V power supply. The ADC core occupies  $228 \times 180 \mu\text{m}^2$  with a unit capacitance of 49fF. The measured INL and DNL are 0.70/-0.75LSB and 0.3/-0.5LSB, respectively, as shown in Figure 3-19. Figure 3-20 shows FFT spectrums for 1.9474 kHz and 12.7621 kHz input signals at 31.25 kS/s. Figure 3-21 shows SNDR/SFDR for different input (1kHz ~ 15kHz)



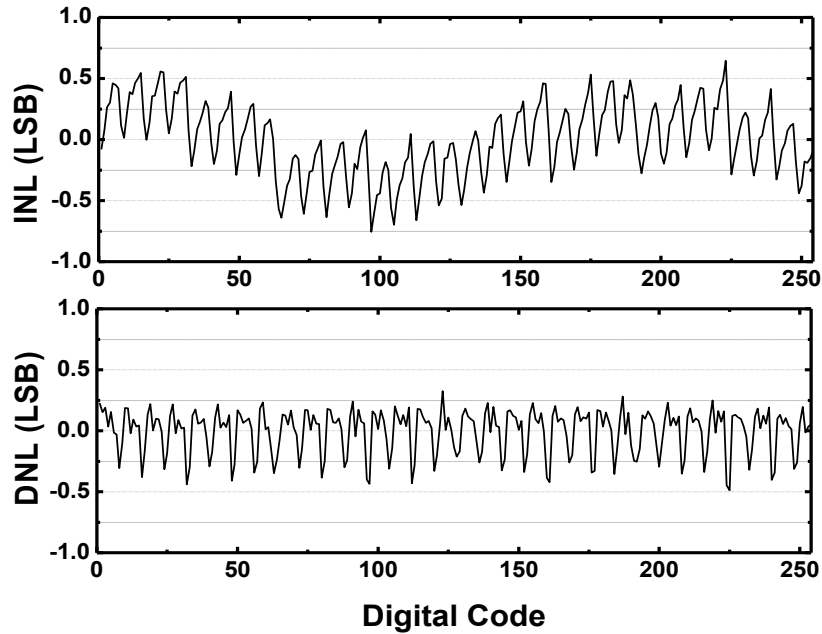


Figure 3-19: Measured INL/DNL of the fabricated SAR ADC.

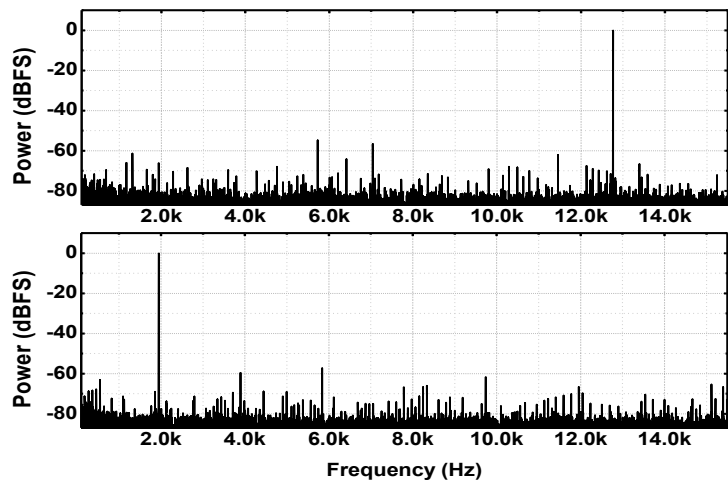


Figure 3-20: FFT output spectrums for 1.9474 kHz and 12.7621 kHz input signals at the sampling frequency of 31.25 kS/s.

and sampling (625S/s~31.2kS/s) frequencies. The measured SNDR is 45.14 dB for the Nyquist input signal at 31.25 kS/s, as shown in Figure 3-21. The measured total power consumption is 87.41nW for 31.25kS/s. As shown in Figure 3-22, the digital block consumes the 64% of the total power. However, this portion can be shared with multiple

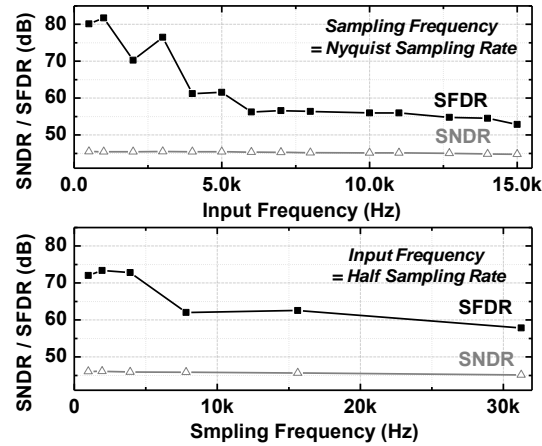


Figure 3-21: Measured SNDR/SFDR for various input and sampling frequencies of the fabricated SAR ADC.

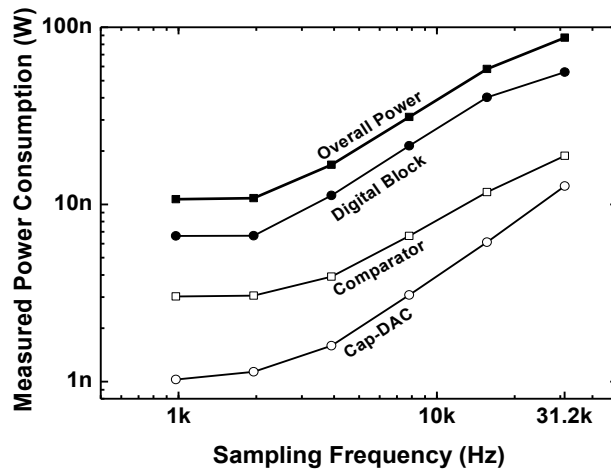


Figure 3-22: Measured power consumption of each circuit blocks for 0.5V rail-to-rail operation.

ADCs in the multi-channel neural recording system to reduce the entire system power.

Figure 3-23 shows the measured SNDR for the over-the-rail operation up to 1V input range. The fabricated ADC shows 7.21 ENOB and 20fJ/c-s for the rail-to-rail operation and 5.91 ENOB and 72.04 fJ/c-s for the input range boosting operation. The performance and microphotograph of the fabricated ADC are summarized in Table 3-1.

### 3.3.7 Summary

In this section, we report a 0.5V 20fJ/c-s 8bit SAR ADC fabricated in 0.25 $\mu$ m technology that achieves a rail-to-rail operation within a small area of 0.041mm<sup>2</sup>. For

Table 3-1: Performance Summary and Microphotograph

	This work	[5]	[6]	[7]
Technology	0.25 $\mu\text{m}$ CMOS	65nm CMOS	0.18 $\mu\text{m}$ CMOS	90 nm CMOS
Sampling Frequency	31.25 kS/s	1 MS/s	100 kS/s	1.5 MS/s
Supply Voltage	0.5 V	1V	1 V	0.5 V
Power Consumption	87.41 nW	1.9 $\mu\text{W}$	3.8 $\mu\text{W}$	7 $\mu\text{W}$
SNDR (dB)	45.14	54.4	58	-
ENOB (bit)	7.2	8	9.4	5.15
FOM (fJ/c-s)	20	4.4	56	140
Area ( $\text{mm}^2$ )	0.041	0.0225	0.7	0.1225

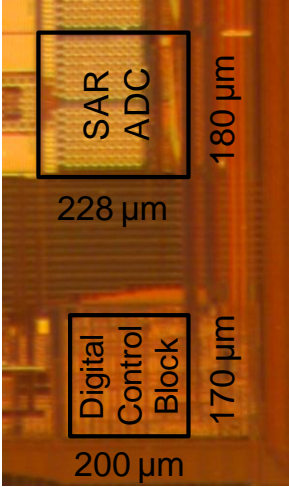
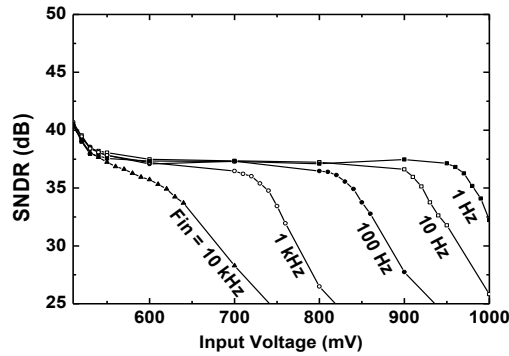



Figure 3-23: Measured SNDR of the one bit ADC with input range boosting.

low-power operation, voltage-scalable single-clock bootstrap switches and time-delayed control units are utilized. In multi-channel neural recording systems, this time-delayed control unit can be shared with multiple ADCs and the effective power consumption will be even further reduced. The proposed ADC can also expand the input range above the rail ( $>0.5\text{V}$ ) and boost the resolution by one bit without any additional hardware.

### 3.4 Programmable Monolithic Voltage and Current Reference Generator

Recently, implantable neural interface systems have been extensively developed to enhance the understanding of neuroscience and enable the disabled to interact with external devices [2], [85], [86]. In these implantable systems, many functional blocks

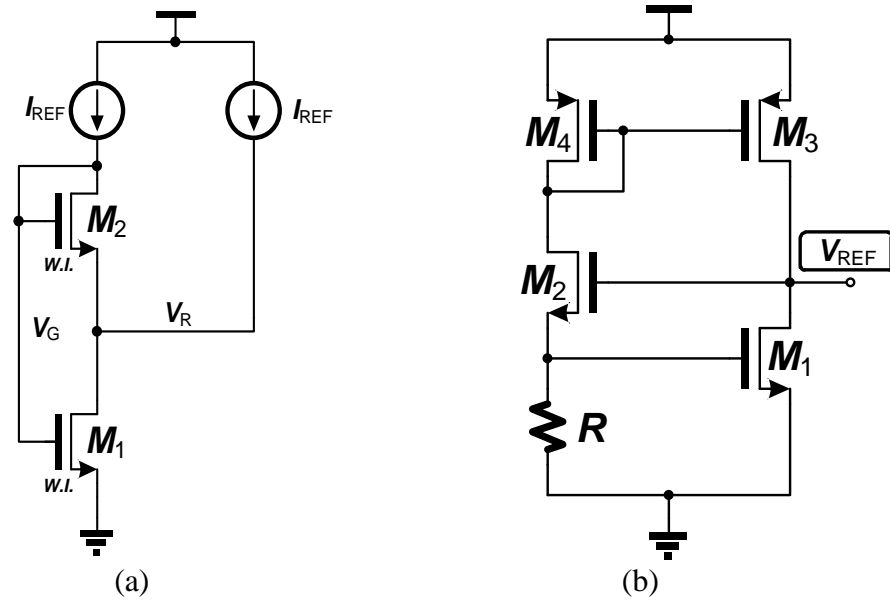


Figure 3-24: Conventional reference generator: (a) PTAT voltage generator using self-cascode MOSFETs, (b)  $V_{GS}$ -based voltage reference.

such as preamplifier, programmable gain amplifier, filters and ADCs are embedded inside the circuit. To ensure a stable and robust operation of these blocks, it is critical to implement an integrated reference generator to supply stable voltages and currents. This on-chip reference block can miniaturize the overall system volume by eliminating required bonding pads and any external components.

An integrated monolithic reference generator for wireless implantable system requires low power, low voltage operation, and wide input range with reliable tolerance for the variations in supply voltage, process, and temperature. Especially, for wirelessly powered systems, the variation from supply voltage should be effectively rejected due to its huge fluctuation. On the other hand, the temperature dependency is less critical in the implantable system due to the homeothermy of the human or animal body. Programmability of the reference generator can provide multiple reference outputs for various applications as well as compensate for possible variations in device performance. In addition, to minimize the overall system volume, it is crucial to implement the

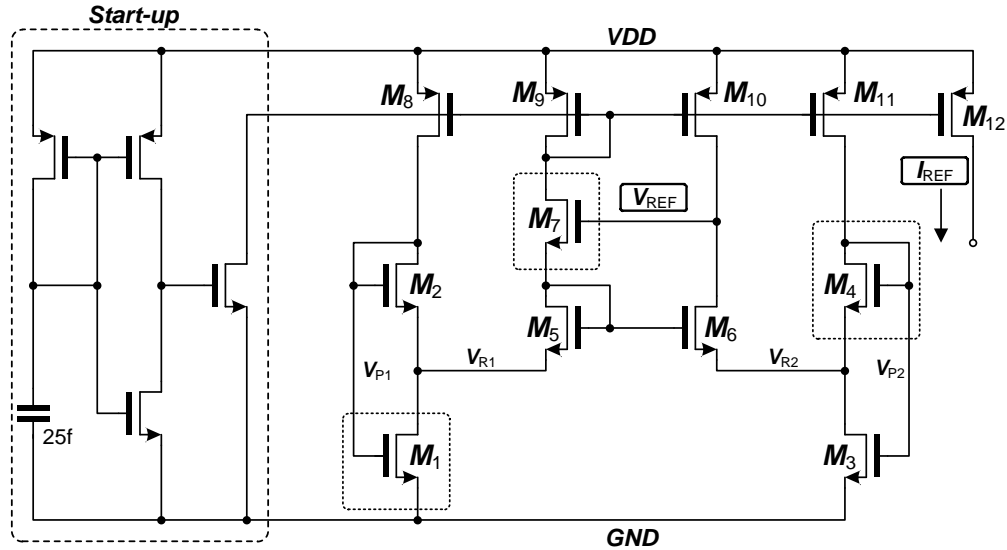


Figure 3-25: Overall structure of the proposed monolithic reference generator with start-up circuit.

reference generator in a small area and to provide both reference voltages and currents simultaneously.

Previously, low-power low-voltage references have been proposed and implemented using the subthreshold operating MOSFETs [87], [88] and beta multiplier [89], [90]. Extreme low-power voltage references [91], [92] and current references [93], [94] have been reported. However, these reference generators are not optimized for wireless implantable systems where the power is wirelessly transmitted through inductive coupling in which power supply dependency and the implementation area should be minimized.

In this section, we propose and implement a 1.5V 120nW programmable monolithic CMOS reference generator for wireless implantable system. The proposed generator is optimized to be tolerable for power supply variation in a small area with the programmability to generate various reference voltages and currents. This reference generator is based on self-cascode MOSFET and beta multiplier, and can operate with the

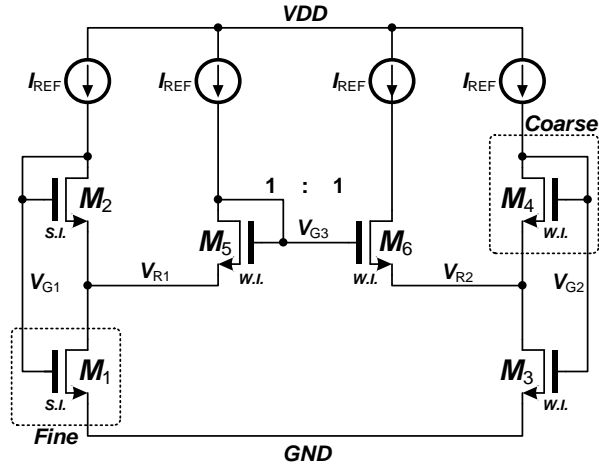


Figure 3-26: PTAT Reference Current Generator

input ranges from 1.5V to 3.5V which is suitable for battery operation. The total implemented area is less than 0.011 mm<sup>2</sup>, which is the smallest monolithic reference generator realized in 0.25μm technology to the best of our knowledge.

### 3.4.1 Operating Principles - Design Equations using the EKV model

The operation of the PTAP current generator using self-cascode MOSFETs as shown in Figure 3-24 (a) can be explained using the EKV model [57]. Due to the self-cascode MOSFET operating in the weak inversion region, the gate voltages of M<sub>1</sub> and M<sub>2</sub> are equal and we can easily derive Eq. 3-14. Based on this relationship, we can generate a PTAT reference voltage V<sub>R</sub> in Eq. 3-16. Using this reference voltage, we can generate a reference current as introduced in [94]

$$I_{D1} = 2I_{D2} \quad \text{Eq. 3-12}$$

$$V_P = \frac{V_G - V_{TH0}}{n} \quad \text{Eq. 3-13}$$

$$I_{S1} \exp\left(\frac{V_P}{U_T}\right) \left[1 - \exp\left(\frac{-V_R}{U_T}\right)\right] = 2I_{S2} \exp\left(\frac{V_P}{U_T}\right) \exp\left(\frac{-V_R}{U_T}\right) \quad \text{Eq. 3-14}$$

$$\frac{2S_2}{S_1} = \exp\left(\frac{V_R}{U_T}\right) - 1 \quad \text{Eq. 3-15}$$

$$V_R = U_T \ln(1 + 2S_2/S_1) \quad \text{Eq. 3-16}$$

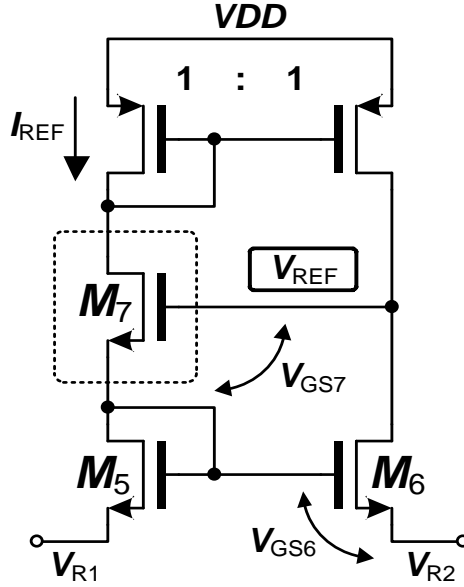


Figure 3-27: Reference Voltage Generator

### 3.4.2 Monolithic Voltage/Current Reference Generator

Figure 3-25 shows an overall schematic of the proposed reference generator. The reference generator consists of a reference voltage/current generator and a start-up circuit.

#### 3.4.2.1 Reference Current Generation

Reference current can be generated using the self-cascode MOSFET and the reference voltage generated as shown in Eq. 3-16. To minimize the dependency of the reference current on the PTAT reference voltage ( $V_R$ ), the  $M_1$  and  $M_2$  in Figure 3-26 are operated in strong inversion region. The PTAT reference current can be expressed through Eq. 3-17 to Eq. 3-20. Eq. 3-20 implies that the output is a PTAT current reference and can be determined by the size of the transistors ( $M_{1-4}$ ).

$$n\beta_2(V_P - V_S)^2 = \frac{n\beta_1}{2} [V_P^2 - (V_P - V_S)^2] \quad \text{Eq. 3-17}$$

$$V_{P1} = \frac{\sqrt{1 + 2S_2/S_1}}{\sqrt{1 + 2S_2/S_1} - 1} V_{R1} \quad \text{Eq. 3-18}$$

$$V_{R1} = V_{R2} = U_T \ln(1 + 2S_4/S_3) \quad \text{Eq. 3-19}$$

$$I_{REF} = I_{D2} = \frac{n\beta_2 U_T^2}{2} \left( \frac{\ln(1+2S_4/S_3)}{\sqrt{1+2S_2/S_1}-1} \right)^2 = \frac{I_{S2}}{4} \left( \frac{\ln(1+2S_4/S_3)}{\sqrt{1+2S_2/S_1}-1} \right) \quad \text{Eq. 3-20}$$

### 3.4.2.2 Reference Voltage Generation

The reference voltage generator is based on the beta-multiplier. Instead of using an area-consuming resistor ( Figure 3-24 (b)),  $V_R$  from Eq. 3-16 is utilized again to generate  $V_{GS}$ -referenced voltage as shown in Figure 3-27. The reference voltage can be express through Eq. 3-21, Eq. 3-22, and Eq. 3-23.

$$V_{REF} = V_{R2} + V_{GS6} + V_{GS7} \quad \text{Eq. 3-21}$$

$$V_{GS,SI} = V_{TH} + \sqrt{\frac{2I_D}{n\beta}} \quad \text{Eq. 3-22}$$

$$V_{REF} = V_{TH6} + V_{TH7} + U_T \ln(1+2S_4/S_3) + U_T \ln(IC_6) + \sqrt{\frac{2I_D}{n\beta}} \quad \text{Eq. 3-23}$$

As shown in Eq. 3-23, the generated voltage is a combination of the negative temperature coefficient of the threshold voltages and the positive temperature coefficient of  $U_T$ . By sizing  $S_{3,4}$  properly, we can achieve a zero temperature coefficient voltage reference.

### 3.4.2.3 Digital Programmability

The proposed generator can be programmed using digital control signals to provide multiple outputs as well as to compensate any possible variation. By changing the size of the transistors of  $M_1$  and  $M_4$  in Figure 3-26, the output current can be controlled. As for the voltage output, we can change the  $V_{GS}$  of  $M_7$  by changing the size of the corresponding transistor.



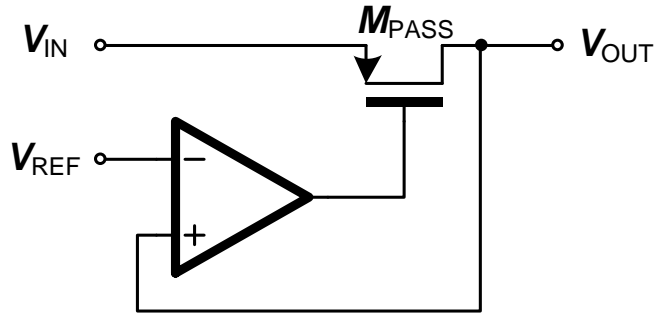


Figure 3-28: Low-drop-output (LDO) Regulator

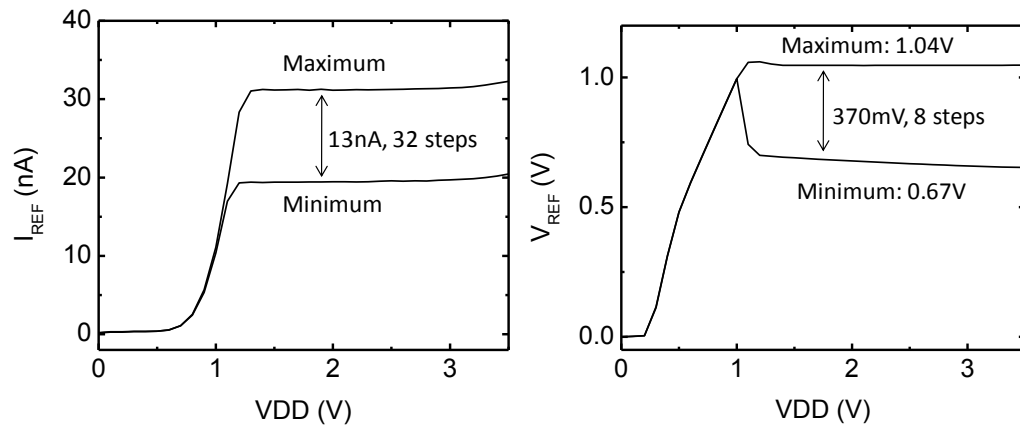


Figure 3-29: Reference variation as a function of power supply voltage variation in the maximum and minimum ranges: (a) current reference and (b) voltage reference.

#### 3.4.2.4 Low-drop-out (LDO) Voltage Regulator

In order to supply the functional blocks integrated in the system, the generated output reference voltage can be used to regulate the input voltage to an adequate output voltage level by using a low-drop-output regulator as shown in Figure 3-28.

#### 3.4.3 Measurement Results

The proposed reference generator is fabricated using 0.25 $\mu$ m 1P5M CMOS process. The overall power consumption is 120 nW (80nA at 1.5V supply). Figure 3-29 shows the measured variation of the monolithic reference generator as a function of power supply voltage variation. It shows a line sensitivity of 0.02%/V and 1.1%/V for voltage and

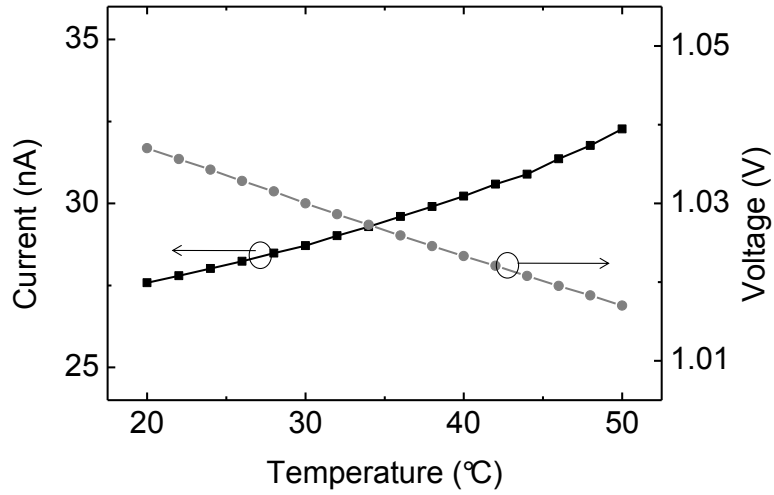


Figure 3-30: Measured temperature dependency of the reference generator.

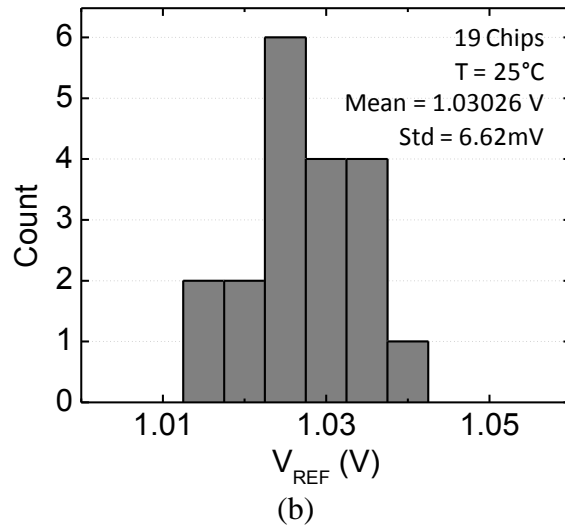
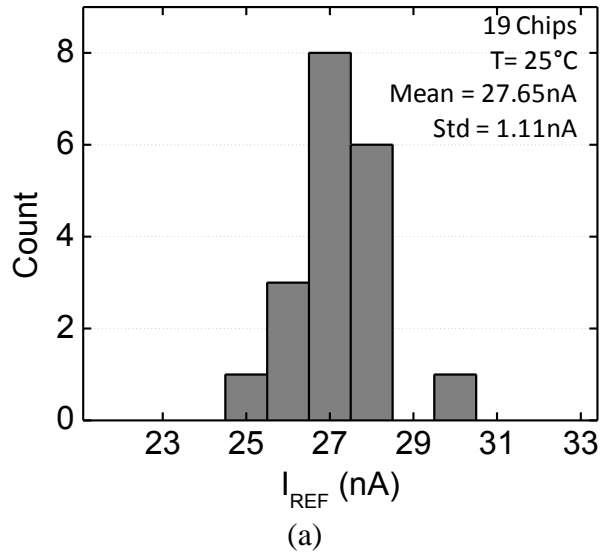


Figure 3-31: Measured outputs distribution: (a) Current and (b) Voltage

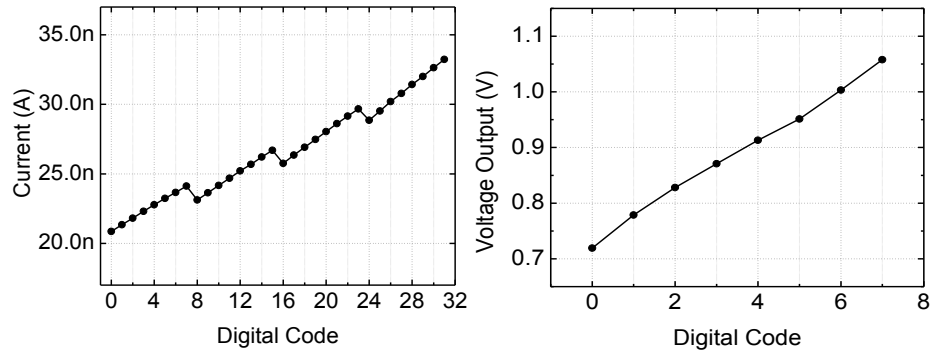


Figure 3-34: Digital programmability test: (a) Current output with 32 steps and (b) voltage output with 8 steps

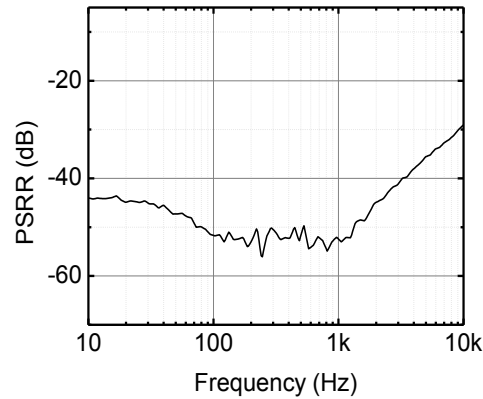


Figure 3-33: The measured power supply rejection ratio (PSRR)

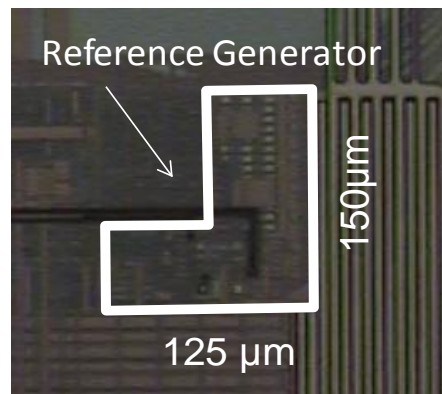


Figure 3-32: Microphotograph of the reference generator

current references, respectively at the highest value setting. Figure 3-30 shows a temperature dependency of the generator in the range of 20 °C ~ 50 °C, which is reasonable temperature variation inside the human body. The measured temperature coefficient (TC) is 0.06%/C and 0.4%/C for voltage and current references, respectively.

		This Work	[26]	[31]	[32]	[33]
Technology		0.25 $\mu\text{m}$ CMOS	0.35 $\mu\text{m}$ CMOS	0.35 $\mu\text{m}$ CMOS	0.18 $\mu\text{m}$ CMOS	1.5 $\mu\text{m}$ CMOS
Temperature Range		20 ~ 50°C	-20 ~ 80°C	0 ~ 80°C	0 ~ 100°C	-20 ~ 70°C
Input Range		1.5 ~ 3.5V	1.4 ~ 3V	0.9 ~ 4V	1 V	1.1 ~ 3V
Reference Type		V / I	V	V	V / I	V / I
Power		120 nW	300 nW	40 nW (@0.9V)	83 $\mu\text{W}$	2 nW
Line Sensitivity	V	0.02%/V	0.002%/V	0.27%/V	-	1.3%/V
	I	1.1%/V	-	-	-	6.0%/V
Temperature Coefficient	V	627 ppm/°C	15 ppm/°C	10 ppm/°C	125 ppm/°C	-
	I	4233 ppm/°C	-	-	185 ppm/°C	2500 %/°C
Reference Output	V	0.71 ~ 1.03V (8steps)	745 mV	670 mV	595 mV	< 100mV
	I	20n ~ 33nA (32steps)	-	-	144 $\mu\text{A}$	0.4nA
Programmability		Yes	No	No	No	No
PSRR		-51 dB at 100Hz	-45 dB@100Hz	-47 dB@100Hz	-27 dB@10kHz	-
Area		0.011mm <sup>2</sup>	0.055 mm <sup>2</sup>	0.045 mm <sup>2</sup>	0.2 mm <sup>2</sup>	0.046 mm <sup>2</sup>

Table 3-2: Performance and Comparison of the Proposed Reference Generator

The nineteen chips were tested and the measured offset variations of the references are shown in Figure 3-31. The output references can be controlled digitally as shown in Figure 3-34. The output can vary from 20nA to 33nA for the current reference, and from 0.71V to 1.03V for the voltage reference, respectively. The measured power supply rejection ratio of the proposed reference generator shows < -50dB at 100 Hz (Figure 3-33). The performance of the proposed reference generator is summarized in Table 3-2. The microphotograph of the chip is shown in Figure 3-32.

### 3.4.4 Conclusion

In this section, we report the design and implementation of a low-power low-voltage programmable monolithic CMOS reference generator in 0.25  $\mu\text{m}$  technology. The fabricated reference generator can operate for an input voltage range from 1.5V to 3.5V, which is suitable for battery operation in wireless implantable microsystem. The implemented area is less than 0.011 mm<sup>2</sup>, which is the smallest monolithic reference generator in 0.25 $\mu\text{m}$  technology to the best of our knowledge. Due to the programmability, the implemented reference generator can provide multiple output levels as well as compensate any possible variations in device performance.

### 3.5 Recording Electrode

#### 3.5.1 Electrical Double Layer

The biopotentials are originated from the electrical potential changes of the cell membrane in response to concentration differences of the ions caused by a sodium-potassium pump across the cell membrane. This ion-based electrical energy is required to be transduced into electron-based electrical energy to interact with existing analysis systems such as a signal processing unit. Various electrodes are utilized for this transduction which can be understood as a nature of the electrode/electrolyte interface where the electrode immersed in an electrolyte can affect distribution of ions/molecules and an interfacial region is formed and called as *electrical double layer (EDL)* [7], [95]. In an electrical system, EDL can be considered as a capacitor that consists of electrons layer on metal surface and ions layers that is attracted by the electrons which are

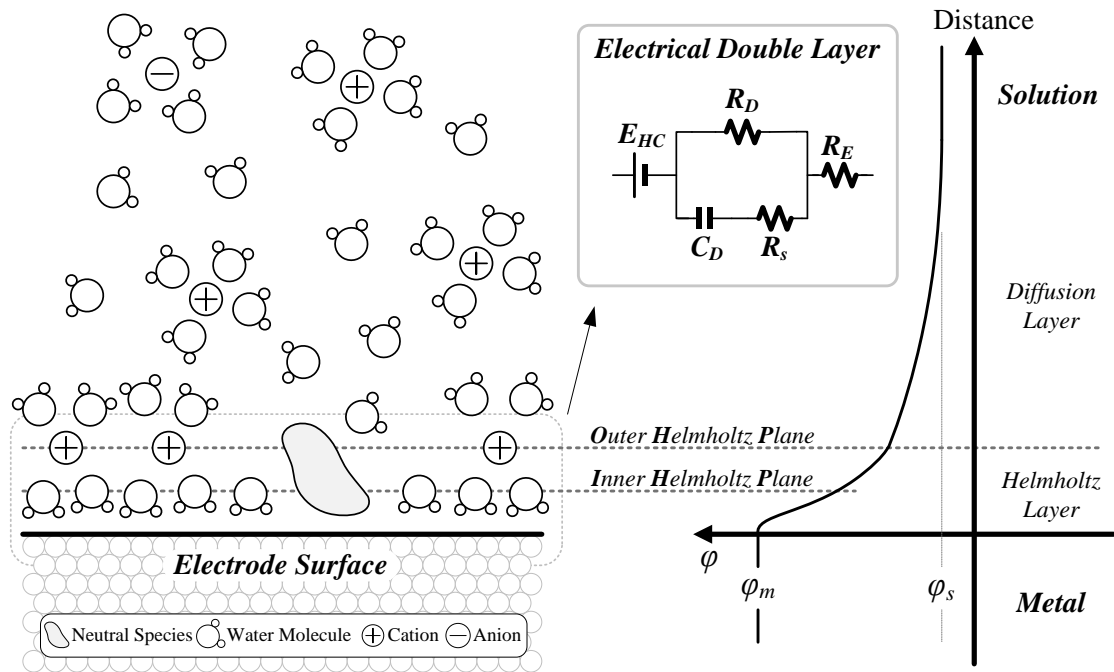


Figure 3-35: The Electrical Double Layer at an Electrode Surface

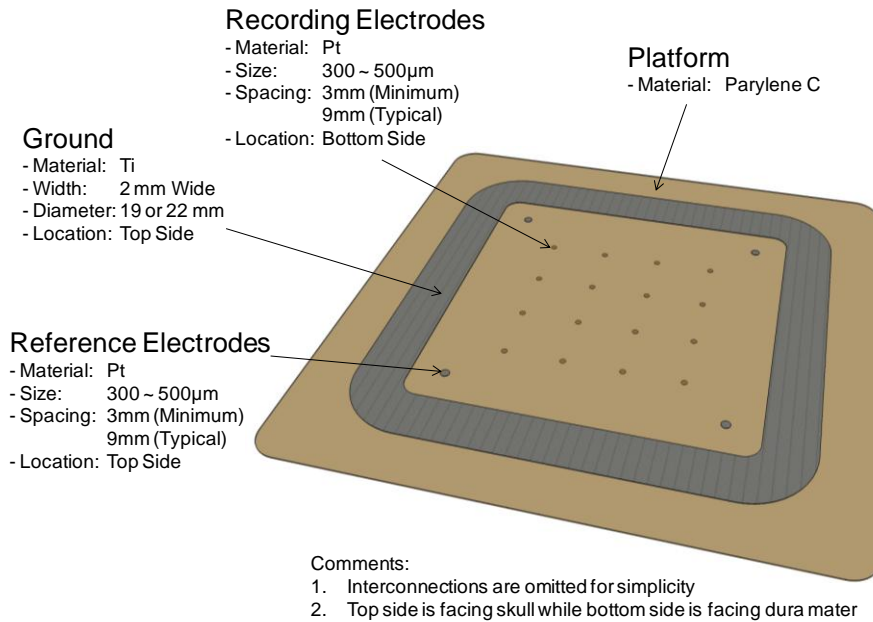
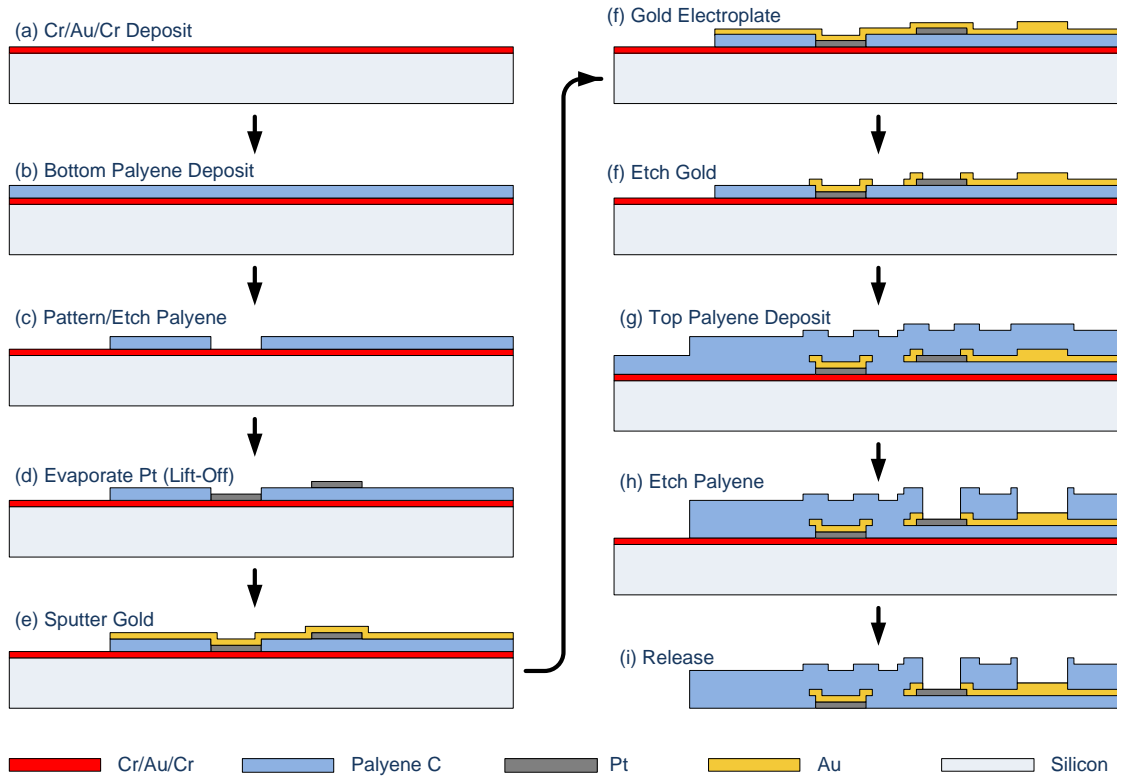


Figure 3-36: Requirements for Epidural Recording Electrode Array

separated by a distance defined as Helmholtz layer as shown in Figure 3-35. In addition, a localized potential distribution around the electrode due to the attracted ions forms a half-cell potential which is a built-in potential across the EDL. However, a temporal variation ( $<0.1\text{Hz}$ ) of localized ion concentration and distance can change EDL capacitance and half-cell potential. To address this temporal variation, a differential AC-coupled amplifier can be utilized which can suppress the variation of capacitance and half-cell potential effectively.

### 3.5.2 Flexible Microelectrode Array

To interact with the epidural layer, the flexible micro electrode array has been designed and fabricated. The requirements for the electrode array is summarized in Figure 3-38. The platform is made of Parylene C material. The total 16 channels and 4 reference electrode and one large local ground electrode. All electrodes are made of Pt with a diameter from 300 ~ 500  $\mu$ m with 3~ 9 mm spacing. The recording electrodes are facing down to dura mater layer, while the reference electrodes and ground are facing up



**Total Electrode Array Thickness: 40  $\mu\text{m}$  Metal Interconnection Thickness: 0.5  $\mu\text{m}$**   
 Figure 3-37: Process Flow for Flexible Microelectrode Array.

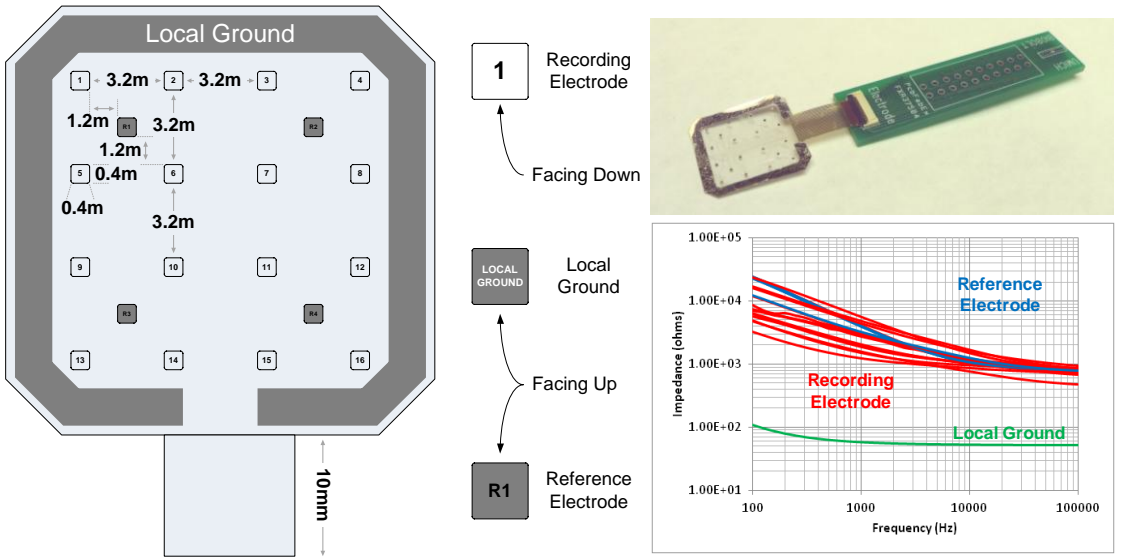


Figure 3-38: The Electrode Dimension and Photograph of Fabricated Electrode Array with Impedance Data

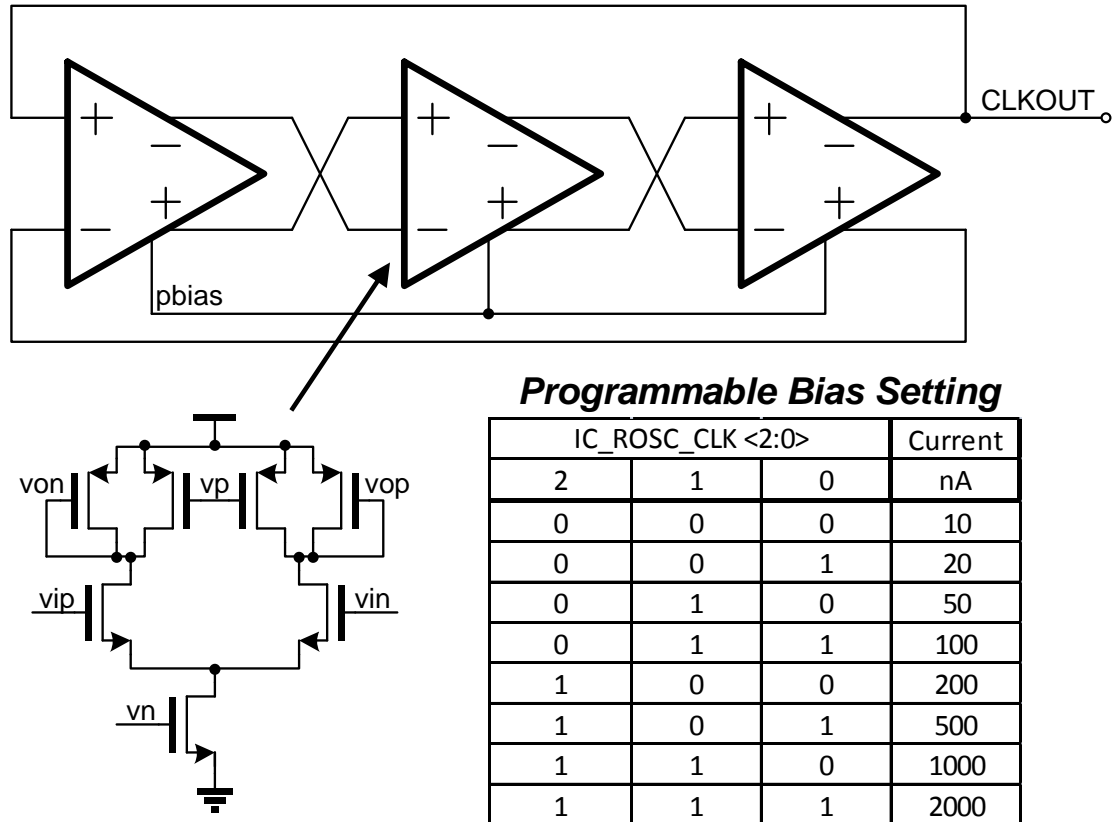


Figure 3-39: Internal 3-bit Programmable Clock generator

to contact with environmental potential. The process flow is shown in Figure 3-37. All the dimension, photograph, and impedance data of the fabricated microelectrode array is indicated in Figure 3-38.

### 3.6 Clock Generator

To operate the analog-to-digital converter and other digital blocks properly, a clock generator is integrated. Like the reference generator, this clock generator can also be severely affected by process variation or temperature. To minimize this affect, the digitally programmable internal clock generator is proposed and implemented as shown in Figure 3-39. The basic topology is a ring-oscillator using three unit differential inverters as shown in Figure 3-39. The current and gain of each stage is controlled by



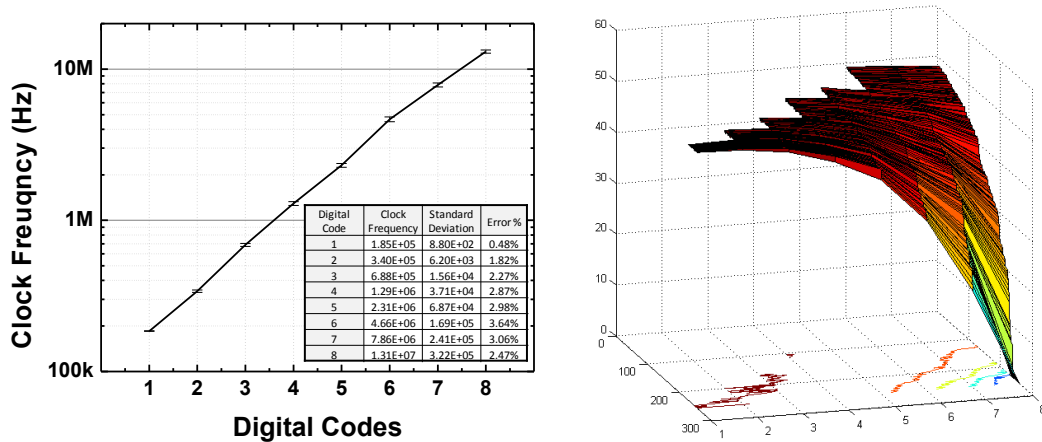


Figure 3-40: Measured Generated Clock Frequency and its Duty Cycle

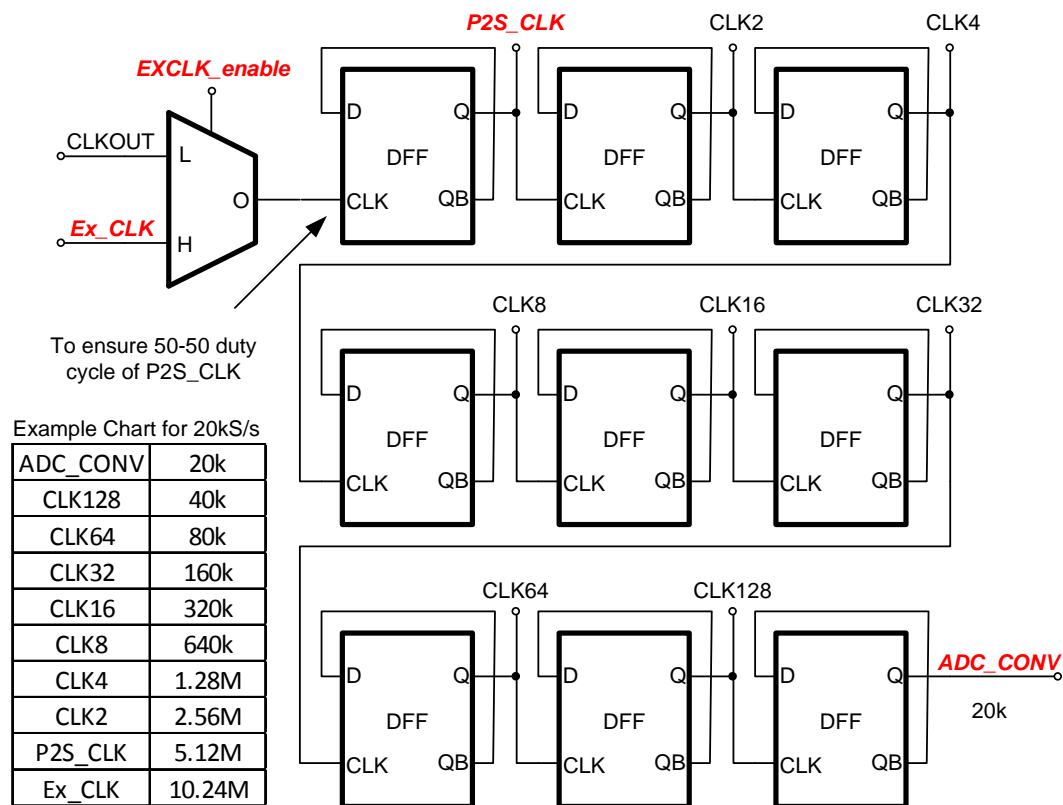


Figure 3-41: Clock Frequency Divider to Generate ADC\_CONV and P2S\_CLK changing  $V_p$  and  $V_n$  which is generated by current divider. As shown in Figure 3-39 table, the control bias current can vary from 10nA to 2000nA with eight steps (3-bit) to change the clock frequency from 180 kHz to 13 MHz. For the various bias conditions, the output clock frequency is not changed below 3% as shown in Figure 3-40, while the duty

cycle is varying from 50% down to 10% as shown in Figure 3-40. The generated clock signal is applied to a frequency divider (Figure 3-41) to generate ADC\_CONV, which is a control signal to initiate each ADC conversion, and P2S\_CLK to serialize and transmit the 16 channel digital output. In case of the failure of the clock generator, the external clock source can be supplied by selecting EXCLK\_ENABLE signal high. To ensure the 50% duty cycle, the first D-FF is utilized as a T-FF. For example, as for the 20kS/s ADC operation, the clock frequency can be set to be Using 10.24 MHz external clock source, we can operate the ADC at 20kS/s while 25kS/s with an internal clock source with 13MHz.

### **3.7 Manchester Encoder**

When we transmit the data to external system, the synchronization between receiver and transmitter using PLL is required and it can require a certain power budget. This synchronization requires similar hardware components at both sides: transmitter and receiver. Instead of that, we can simplify the transmitter side hardware and eventually reduce the power consumption, while the receiver side requires more hardware and signal process to retrieve the signal.

To do this, we can embed the clock signal into the data signal using Manchester coding technique. Manchester code (also known as Phase Encoding) is a line code in which the encoding of each data bit has at least one transition and occupies the same time. In other words, if the data is '0', the encoded data has the data of either '01' or '10', and vice versa. The encoded data has no DC component and the clock information is embedded inside the data, so-called self-clocking. This means that from the transmitted signal has data as well as clock information so that the data and clock can be recovered

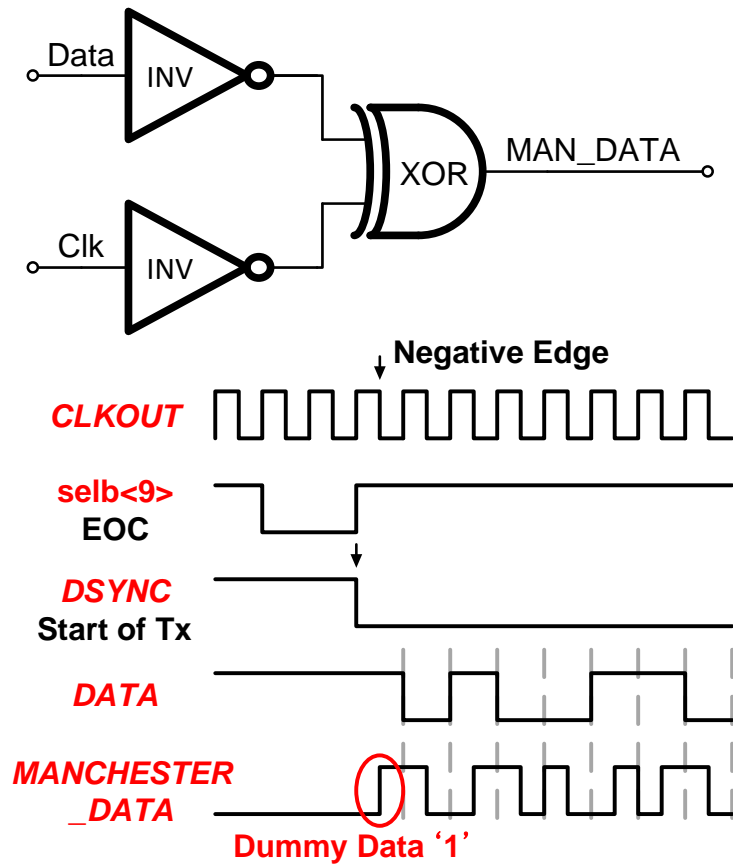


Figure 3-42: Manchester Encoder and its Timing Diagram

from the receiver side which enable a simple data communication. The basic component to encode the Manchester Code is an Exclusive-OR gate as shown in Figure 3-42. And, the timing diagram to transmit the serialized data using Manchester encoder are also shown in Figure 3-42.

### 3.8 *In-Vivo* Measurement

For *in-vivo* test, we collaborated with Dr. Dan Moran at Washington University, St. Louis. In order to overcome the noisy environment and limitation, we designed the *in-vivo* measurement system using printed-circuit board (PCB) to test the pre-developed analog front-ends IC as shown in Figure 3-43. This PCB-based test system is designed to

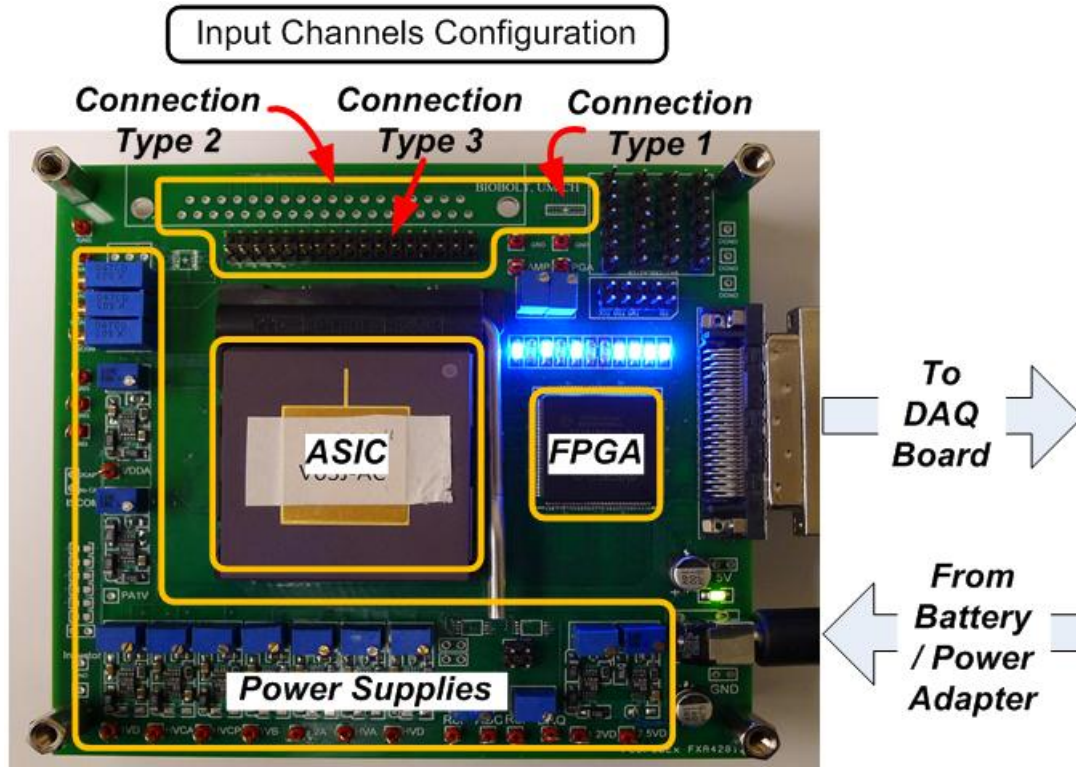


Figure 3-43: In-vivo Measurement Board

supply all the required bias values and also to configure all the parameters of the system on-site. We could successfully acquire in-vivo measurement of epidural neural signals from a primate using our prototype device. The custom analog front-end IC was integrated in a PCB assembled with other components. The epidural electrode array was placed on the surface of dura mater of the monkey and the neural activities from 16-ch were recorded simultaneously as shown in Figure 3-45. And, Figure 3-44 shows the time-domain ECoG signal with its spectrogram from a single channel. Typical motor movements are related to the ECoG neural signal power in the frequency bands of 7 ~ 30Hz and 70 ~ 110 Hz. The spectrogram in Figure 3-44 shows the activity related ECoG neural signal power.

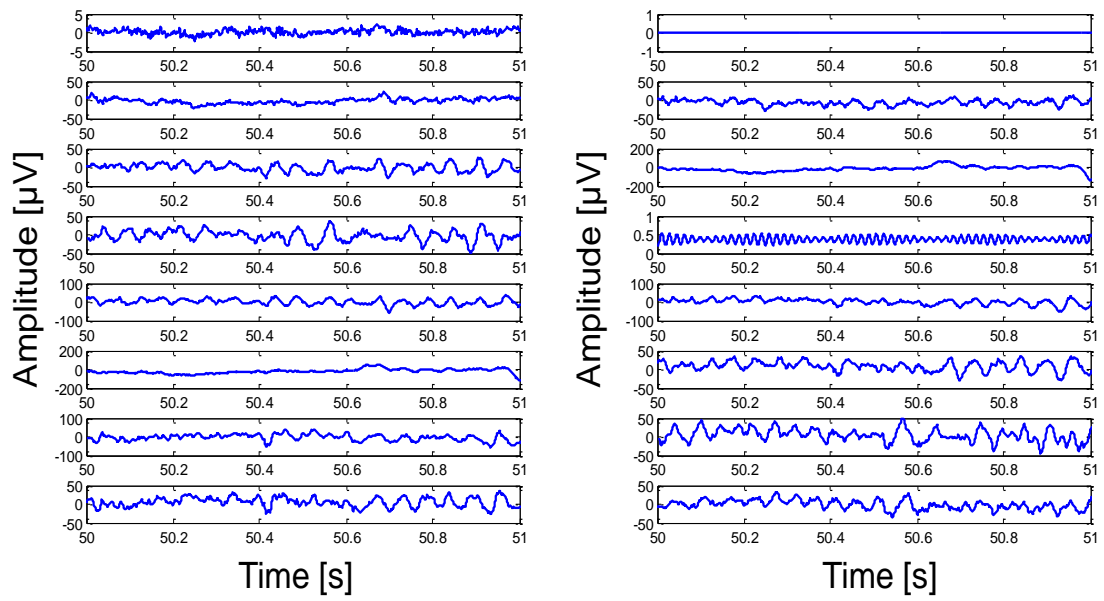
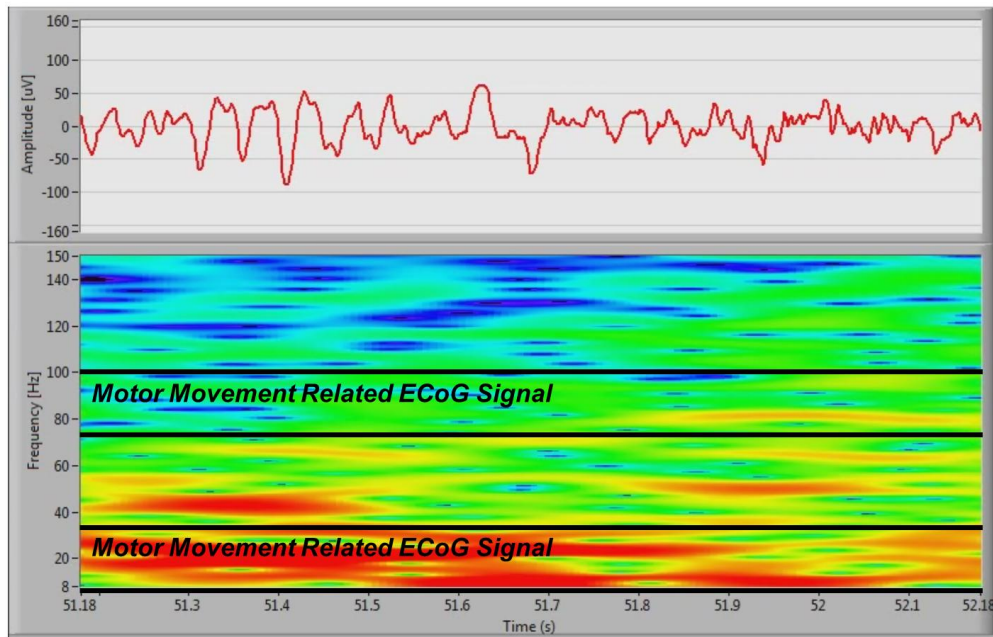


Figure 3-45: 16-Channel *In-vivo* Measurement



Collaboration with Dan Moran at Washington University, St. Louis

Figure 3-44: Single Channel Epidural Recording Signal with Time-Domain and Spectrogram

### **3.9 Intra-Skin Communication for Modular Expandable System**

In distributed wireless interfaces for neural recording, power consumption becomes one of the major limitations against scaling and distributing more sensor nodes across the brain or inside the body. In most stand-alone systems, data communication module consumes major part of the power budget available to that system. Therefore, reducing the power of data transmission will directly contribute in scaling neural recording systems. Furthermore, it will be beneficial and more practical if this module can be implemented in a small size and at the same time consumes less power. To address the above constraints, we will discuss wireless intra-skin communication (WISCOM) in this section.

#### **3.9.1 Body Area Sensor Network Using Tissue Coupling**

Previously, wireless body area network (WBAN) was proposed for interconnecting biomedical sensors located in the different parts of the body [96]. Instead of using direct wireless data transfer from the biomedical sensors to the hospital infrastructure using RF or inductive coupling, the sensors send the data through a suitable low-power, low-rate intra-body communication link to a way station which also resides on the body and relays the data to the external system. An external wireless link for the data exchange between the way station and the external system may employ a standard wireless technology, e.g., WLAN, with a high data rate. For this link, the power consumption is not strictly constraint because a relatively large power source can be provided for the dedicated way station. There are three types of communication channels in the body area network [97].

- *off-body* communication –from off-body to an on-body device or system
- *on-body* communication –within on-body networks and wearable systems

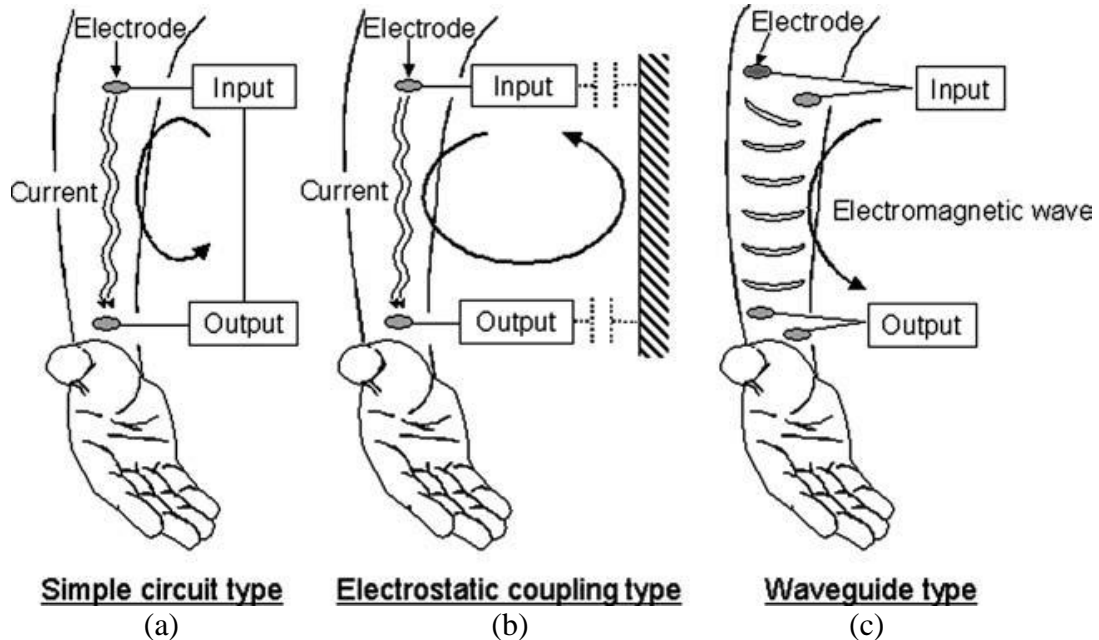


Figure 3-46: Various Types of Intra-body Signal Transmissions: (a) Direct Coupling, (b) Capacitive coupling, and (c) Galvanic coupling

- *in-body* communication –to medical implants and sensor networks

The *off-body* communication is the communication through air from on-body devices to the external system. The *on-body* communication is where most of the signal transmission channel is on the surface of the body, and both (transmitting and receiving) antennas are on the body. The *in-body* communication is where a significant part of the channel is inside the body and implanted transceivers are used. Most of previous work in WBAN has been focused on wearable sensors for monitoring blood pressure, body temperature, EKG, oxygen level, etc. As a result, development of WBAN has been limited to *on-body* communication.

### 3.9.1.1 Previous Approaches

Several attempts were made to send and receive electrical signals over the human body [97], [98]. There are three general methods for intra-body communication (IBCOM). In the simple circuit, the human body is treated as a conductor. This principle requires

external wires and was applied in some healthcare devices such as body fat meters, but has been hardly implemented in recent IBCOM applications. The other two methods are capacitive coupling and Galvanic coupling. Figure 3-46 shows the capacitive coupling introduced in the study of PAN by Zimmerman [96]. In this approach, transmitting and receiving devices should be grounded, and the transmission quality is heavily dependent on the surrounding environment. In Galvanic coupling, the human body is treated as a waveguide. High-frequency electromagnetic waves generated by a transmitting terminal propagate through the body to be received by a receiving terminal [99]. External wires are not necessary in this configuration, and the surrounding environment does not affect transmission quality. For wearable sensors, both approaches (capacitive and Galvanic couplings) have been investigated for *on-body* WBAN [100], [101]. For implantable sensors, capacitive coupling would not be easily implemented because the ground connection cannot be well established for the sensors implanted inside the body. Therefore, Galvanic coupling is the only viable option for *in-body* transmission for the implanted sensors. Although a few prototype devices were reported for intra-body communication and some of its basic characteristics, a complete detailed analysis of modeling the signal transmission for *in-body* communication has not yet been conducted. Moreover, the optimum carrier frequency of transmission has yet to be fully addressed in terms of minimizing absorption loss and required transmission power.

### **3.9.1.2 Safety and Regulations**

The previously introduced intra body communication technique can transmit the signal by injecting the current into the human body. And the injected current flows through the body tissue and organs to the receiver. There are mainly two safety issues



when the current is injected into human body: (1) maximum allowable current and voltage, and (2) balanced charge-injection. The allowable current and voltage is recommended to be less than 300mA

*(1) Maximum Allowable Current and Voltage:* The allowable current and voltage is recommended by the Section 51.104 of the IEC 601-2-10 standard that clearly specifies the limitation of output energy for a variety of wave types: (1) the maximum energy per pulse shall not exceed 300mJ, when applied to a load resistance of 500 ohms. (2) For stimulus pulse outputs, the maximum output voltage shall not exceed a peak value of 500V, when measured under open circuit conditions[102].

*(2) Balanced Charge Injection:* imbalance in the injected charge can cause the charge accumulation inside body. And, this accumulated charge can be harmful for human body such as pH shift, ionic charges near the implanted electrodes, erosion of the electrode material, and damage to the neural structures. By injecting a large amount of current over a longer period of time, charge is massively exchanged over the electrode between ion and electron, and can cause electrolysis. To avoid these side effects, we need a biphasic charge-balanced current injection which is able to reduce tissue cell damage during communication, especially for implanted devices [103–106].

### **3.9.2 The Proposed Wireless Intra-Skin Communication (WISCOM)**

Based on the considerations discussed in the previous section, we developed the wireless intra-skin communication which is analogous with previously explained in-body communication, and inject the biphasic current with the range of few tens of  $\mu\text{A}$ . In this work, the primitive research has been performed in order to test the feasibility.

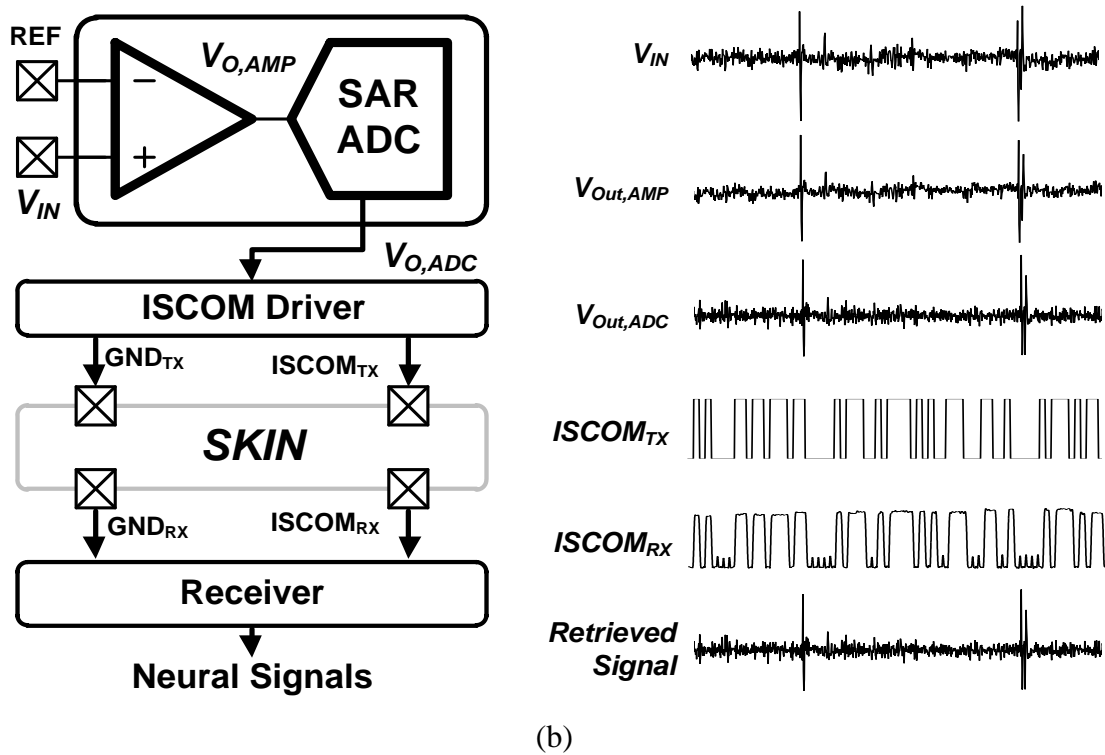
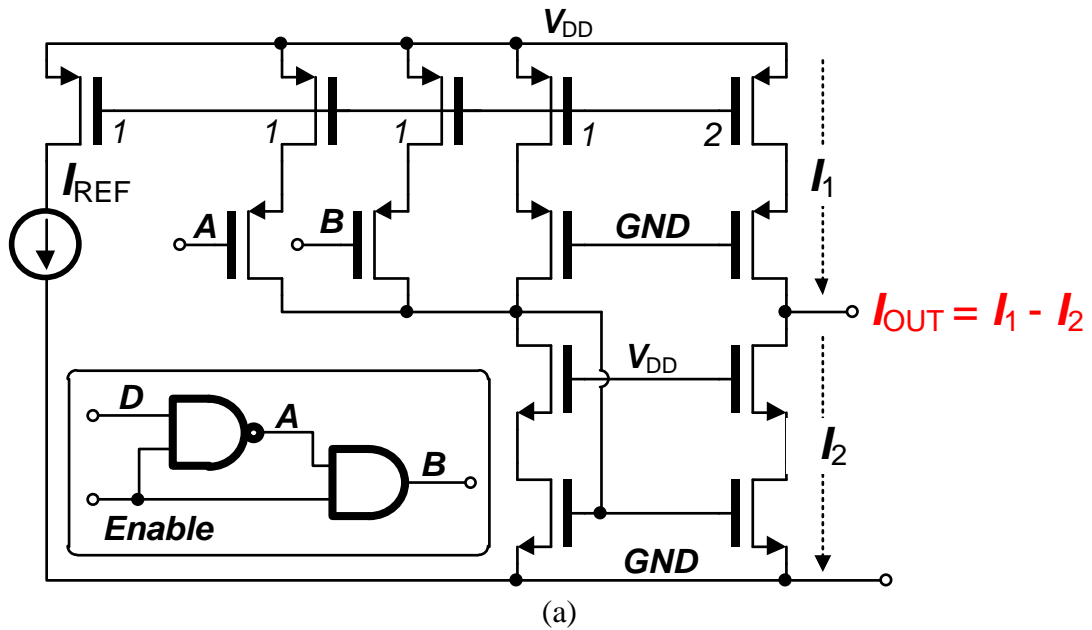


Figure 3-47: (a) Conceptual diagram of ISCOM with its current driver and (b) the measured neural signal chain through preamplifier, ADC, ISCOM (skin) and retrieved signal

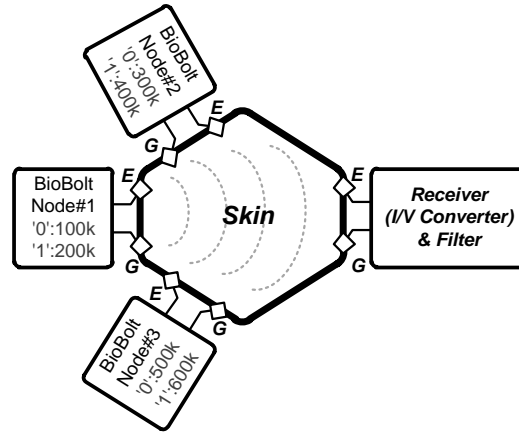


Figure 3-48: Distributed Cluster-Based Wireless Intra-Skin Communication

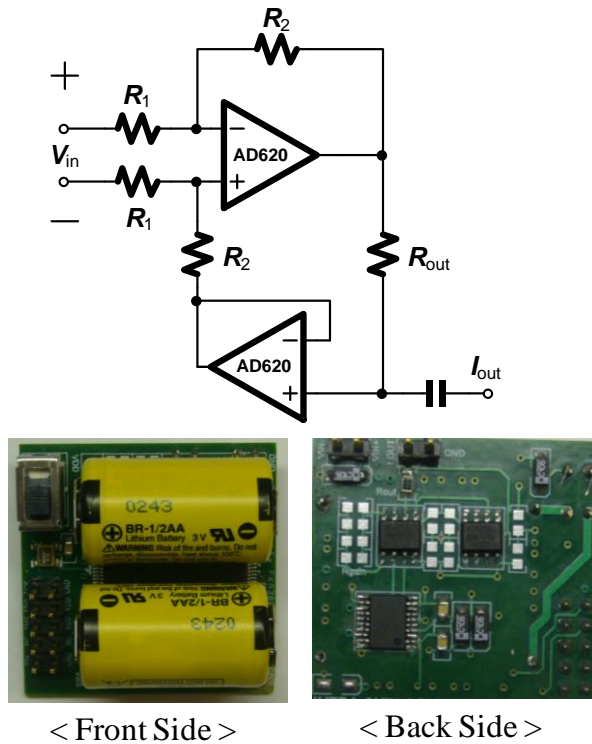


Figure 3-49: The ISCOM Module for testing Feasibility of the Cluster-based Operation

### 3.9.2.1 Charge Balanced Current Driver

One possible issue when current is injected into the skin would be charge accumulation in the body as mentioned in the previous section. The ISCOM current

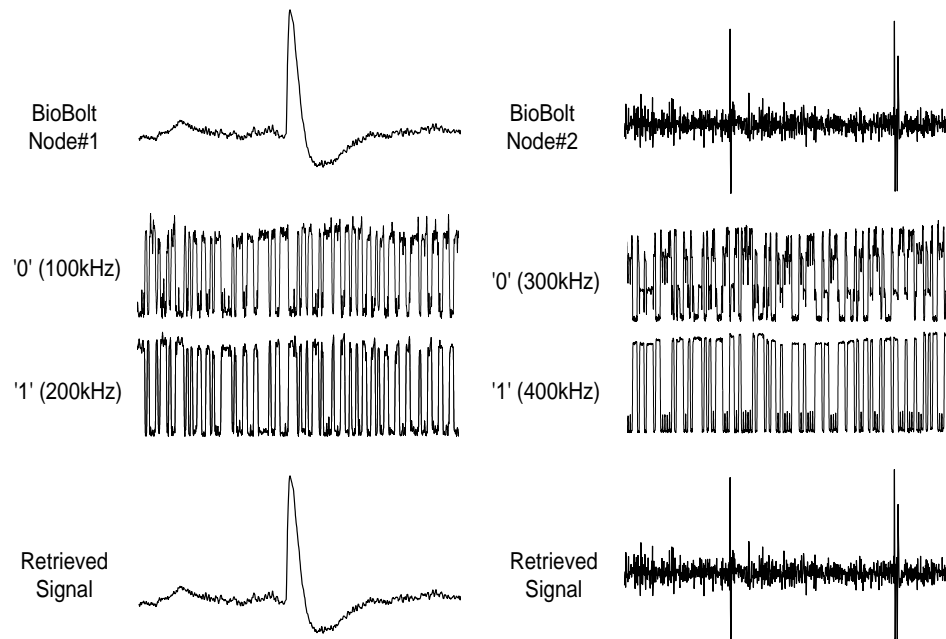


Figure 3-50: Two-Channel ISCOM Data Transmission

Table 3-3: Performance Summary of ISCOM

<b>Intra-Skin Communication</b>	
<b>Power Consumption (Including Control Blocks)</b>	<b>160 <math>\mu</math>W</b>
<b>Data Bandwidth</b>	<b>10 kb/s</b>
<b>Modulation</b>	<b>Binary Frequency-shift Keying</b>
<b>FSK Frequency</b>	<b>Node #1: 100kHz/200kHz Node #2: 300kHz/400kHz</b>
<b>Channel Attenuation</b>	<b>-17 dB (1cm)</b>
<b>ISCOM Current Driver</b>	
<b>Power Supply</b>	<b>1 V</b>
<b>Current Output</b>	<b><math>\sim</math> 10 <math>\mu</math>A</b>
<b>Bandwidth</b>	<b>&gt; 5 Mhz</b>

driver is designed to generate alternating currents to ensure no charge will build-up inside the body as shown in Figure 3-47 (a). The output current polarity is determined by the

current difference between the paths, P1 and P2 according to the modulated signal input. The retrieved signal from the receiver is shown in Figure 3-47 (b). It should be noted that the transmitted signals does not affect or interfere with neural activities, because neurons are transparent for high frequency signals ( $> 100\text{kHz}$ ). We could obtain a data bandwidth of  $10\text{kb/s}$  data at  $160\ \mu\text{W}$  and measured a channel attenuation of  $-17\text{dB}$  from the ISCOM.

### **3.9.2.2 Distributed Cluster Based Modular Wireless Intra-Skin Communication**

Our neural interface circuit can operates as a stand-alone system. But, the overall system can expand the recording coverage and different sensing modalities by placing multiple devices to form a cluster as you can see in Figure 3-48. For feasibility characterization of the system expandability, two ISCOM current driver modules are designed as shown in Figure 3-49. Two ISCOM modules are separated by  $1\ \text{cm}$  apart from each other and the  $\text{ISCOM}_{\text{TX1,2}}$  signals from two devices are simultaneously transmitted through the skin. And, as shown in Figure 3-50, the signals are transmitted through the skin and retrieved successfully without interferences each other. The overall performance has been summarized in the Table 3-3.

## **3.10 Conclusion**

In this chapter, we have designed and fabricated 16channel analog front-ends which include microelectrode, preamplifier, analog-to-digital converter, reference generator, clock generator, and Manchester encoder. To optimize the power and noise performance, quasi-floating body push-pull preamplifier, and channel-level ADC. For fully implantable system, peripheral circuits such as monolithic reference generator and clock signal generator is also designed and tested. For modular expandable system, we proposed and

implemented the wireless intra-skin communication as an alternative wireless communication method. The charge-balanced current driver has been implemented. WISCOM module has been developed and demonstrated.

## CHAPTER 4

### WIRELESS NANO-WATT MODULAR CIRCUITS FOR CLOSED-LOOP NEURAL PROSTHESIS

In this chapter, we developed and characterized the neural interfacing circuit that can be applied for the closed-loop controllability of neural prosthetic systems such as epilepsy treatment system (shown in Figure 4-1) as mentioned in the chapter 1, Figure 1-10. In this particular application such as field potential measured in the cortex or surface of the epidural layer, we realized that the neural signal spectrum shows an inherent dependency on the frequency. Driven by this characteristic, we optimize the circuitry to achieve maximum power-energy efficiency. In this chapter, we will discuss how to design and implement neural interface circuit for the closed-loop ECoG neural interface.

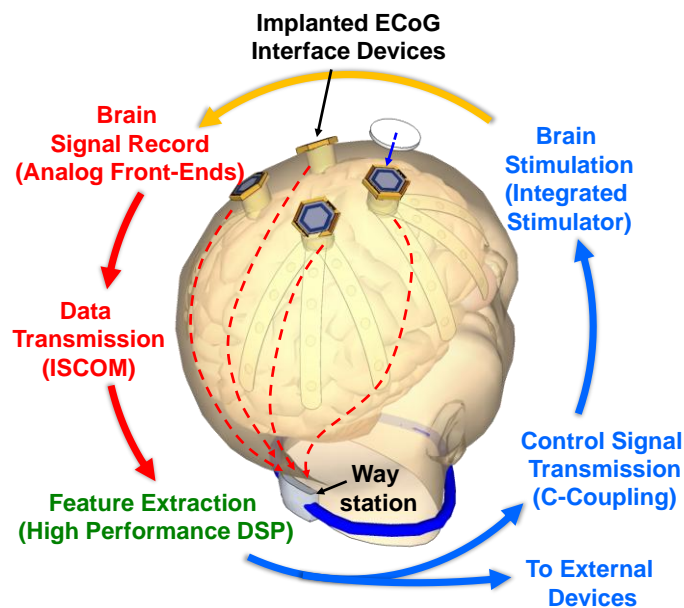


Figure 4-1: Conceptual wireless modular EDSP-assisted closed-loop neural interface

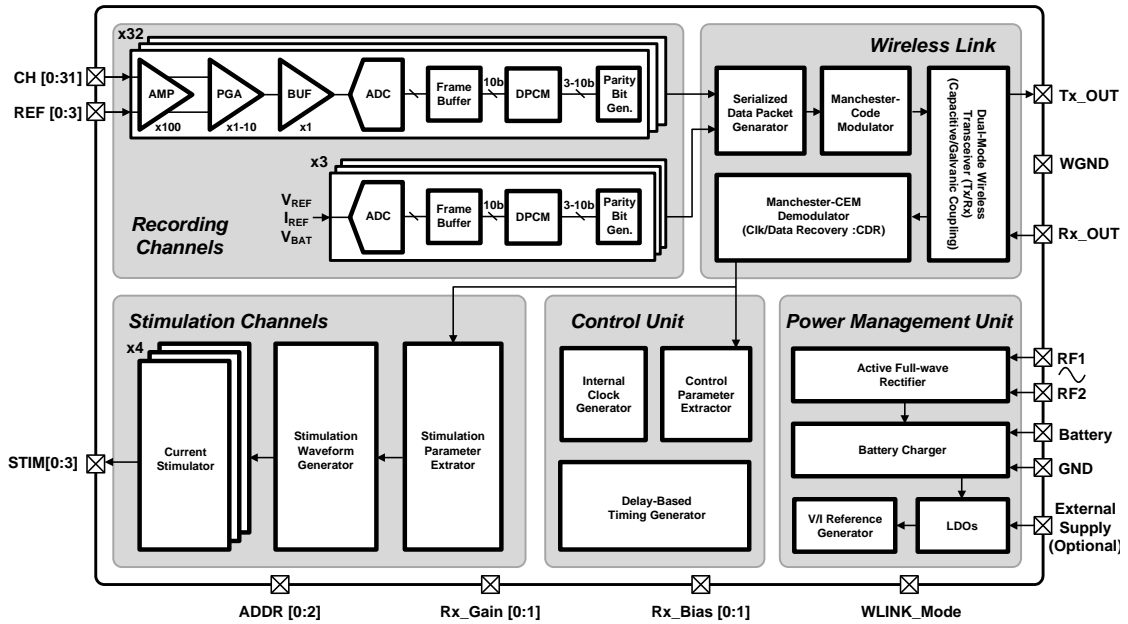


Figure 4-2: Overall System Structures

#### 4.1 Nano-Watt Modular Integrated Circuit Overview

Figure 4-2 shows the overall system architecture of the proposed system. The main purpose of the proposed system is a low-power operation. The system can be divided into five sub blocks: recording channels, wireless link, control unit, stimulation channels, and power management unit.

For saving the power consumption while maintaining system performance, this work proposes a cyclic operation of preamplifier, SAR analog-to-digital converter with embedded level-shifter, data compression using differential pulse code modulation, wireless Rx/Tx using capacitive and galvanic coupling, and Manchester clock-edge modulation (MCEM) for a simple CDR operation.

In addition, in order to expand the number of channels to cover a wide area, a modular expandable wireless link protocol is designed to accommodate up to eight implantable devices to deploy and transmit signal simultaneously.



### 4.1.1 Global Timing Operation

Figure 4-3 shows the global timing diagram of the proposed system from wireless data receiver to wireless data transmitter. In this system, because the system has many programmability such as different time-division multiplexing factor for cyclic operation or various DPCM resolution, the timing is generated based on time-delayed timing generator and various counters which is programmable.

In the wireless receiver, the transmitted MCEM signal by the way station is recovered to extract system clock source and control parameters which are utilized to program various counters and clock sources for the different operation modes. The recovered data and clock generate a global synchronization signal ( $V_{SYNC}$ ) as a reference starting signal. And, based on the  $V_{SYNC}$ , the following control signals such as amplifier active (AMP\_ACT), ADC sampling (ADC\_SAMP), data load into Tx buffer (serialized buffer), and transmission start signals (TX\_STR) are generated with the predetermined delay time.

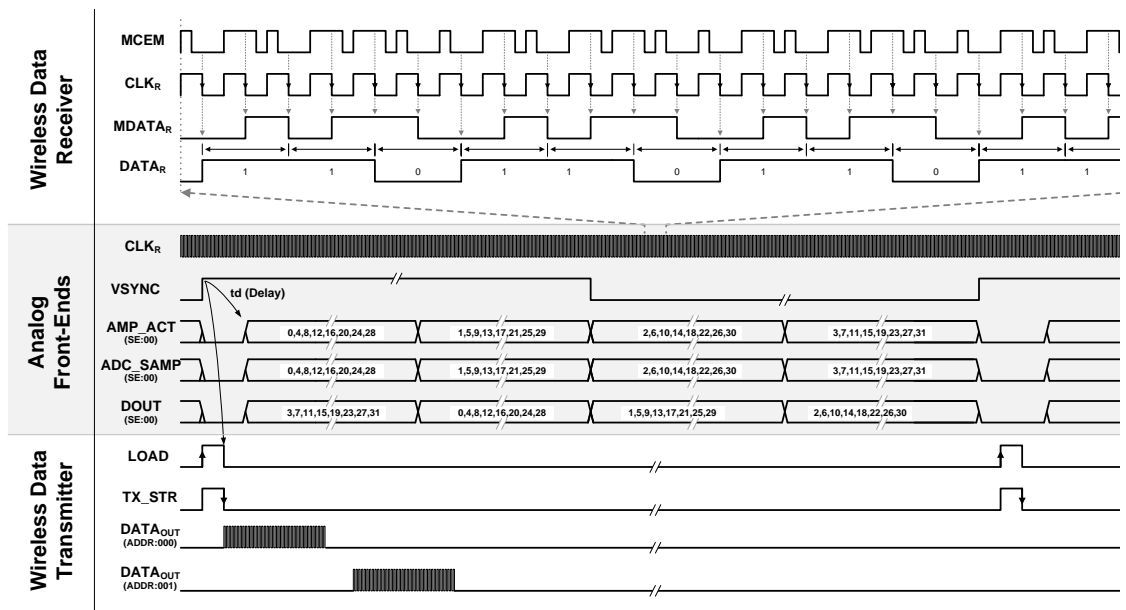


Figure 4-3: Global Timing Diagram of the proposed system

## 4.2 Continuous-Tracking Cyclic Preamplifier with Tunable Pseudo Resistors

Preamplifier performance characteristic determines the overall neural interface system performance. Because of this, many techniques have been proposed and implemented as mentioned in the previous chapter 3. Their design purpose is to maximize and optimize the preamplifier noise and power performance for given constraints such as vulnerable neural signals and limited power source. Previously, transistors operating in a subthreshold region have been utilized by many researchers due to its optimized noise and power performance like a BJT.

To elongate the device lifetime furthermore while maintaining noise performance, pseudo-open loop (chapter 2), push-pull topology with double gated input transistor (chapter 3) as a continuous operation have been proposed and implemented. And, as a dynamic operation, supply current modulation [107], and power scheduling [108] have been proposed. In this dynamic operation, the preamplifier bias current is modulated based on the ADC sampling timing. When ADC samples the output of preamplifier, preamplifiers consumes 100% bias current. And, after sampling period, the preamplifier is in sleep mode with a minimum bias current (10%) to keep the DC bias current for fast settling and tracking. However, their design strategy for a required bandwidth and settling time has room to improve more.

In order to reduce power consumption while maintaining the required noise performance of neural interface system, especially ECoG, in this work, we introduce a cyclic preamplifier. The bio-signal driven analysis enables the cyclic preamplifier to operate dynamically for extreme low-power consumption, while maintaining noise performance. In this section, we will discuss cyclic preamplifier.

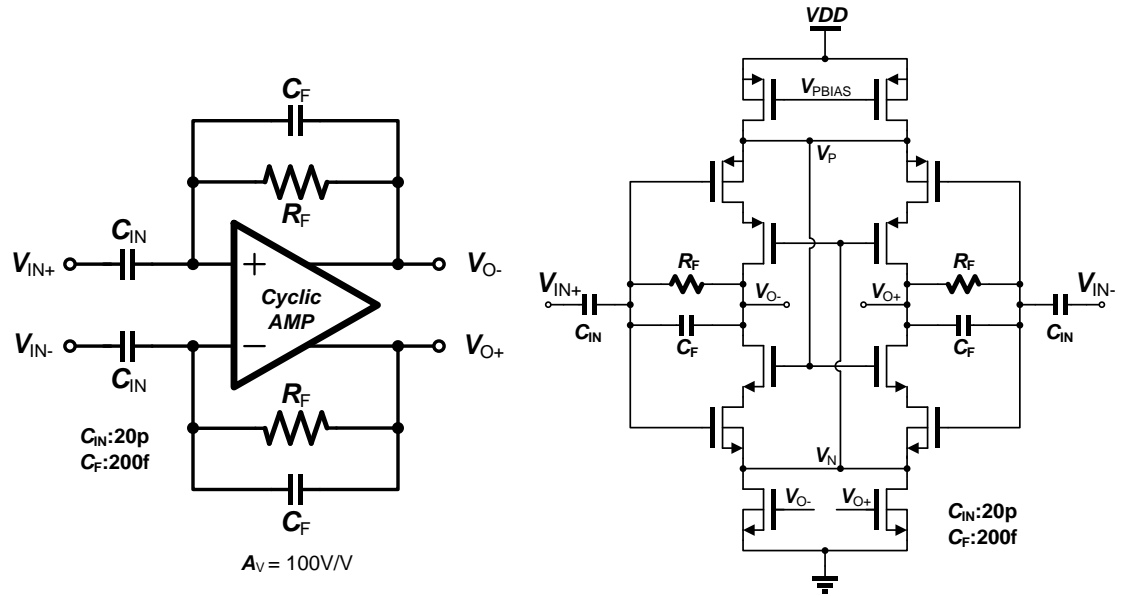


Figure 4-4: Schematic of the Proposed Cyclic Preamplifier

#### 4.2.1 Schematic of the Proposed Preamplifier

Figure 4-4 shows the proposed preamplifier. This push-pull amplifier is designed based on the previous version in chapter 3. The bottom transistors are introduced as a common mode feedback circuit to enhance the common mode rejection property by providing the virtual ground to NMOS input transistors. The overall gain is set by  $C_{IN}$  and  $C_F$  which is 100, and the floating input gate nodes are biased through the current-control tunable pseudo resistors.

Based on this structure without any additional hardware, in this work, the proposed preamplifier is operating in cyclic mode by switching the cascade transistors. In the following sections, we will discuss some design issues and its implementation.

#### 4.2.2 Design Consideration for Dynamic Operation

In this section, we will discuss about some issues to design a dynamically operating preamplifier compared to continuously operating preamplifier as shown in Figure 4-5.

#### 4.2.2.1 Analog Tracking Memory for Continuous Tracking and Fast Settling

In the neural application, the majority of preamplifiers have AC-coupled input structures because of its simple and effective structure to reject various interferences such as a drift and DC offset. However, AC coupled preamplifier can track the input signal variation only when the preamplifier is active compared to continuous and DC-coupled preamplifier. This means the signal information during off phase will be lost and there is no way to reconstruct the original signal. To address this issue, in this work, we utilize the series input capacitor as an analog tracking memory. So, during the off phase, this analog tracking memory tracks the input signal passively by a capacitive coupling and keeps the information in the form of an excessive charge at the floating node until the preamplifier turns on. Once the preamplifier turns into active mode, the excessive charge will be transferred through the feedback capacitor and the output will track the original input signal. So, effectively, we can expect the preamplifier to track the input signal

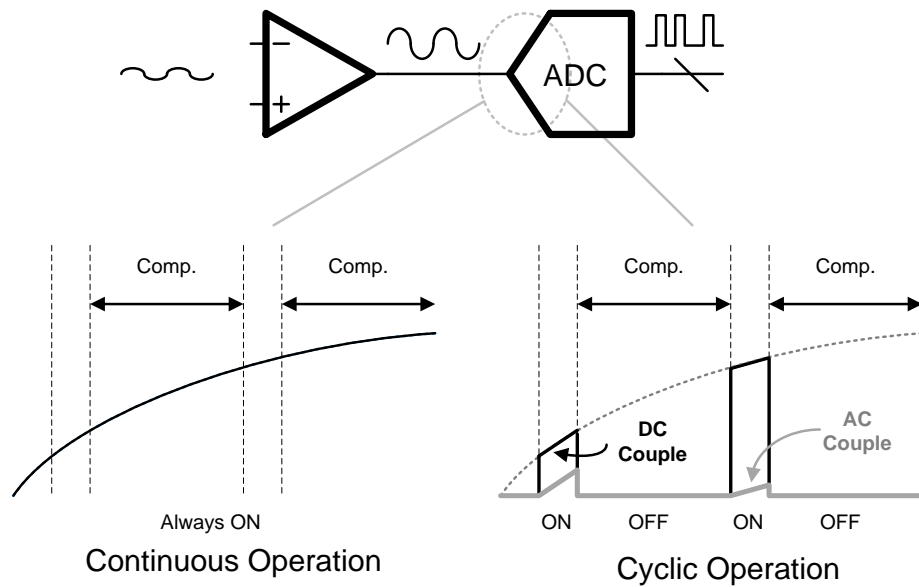


Figure 4-5: Comparison of Continuous Operation and Cyclic Operation

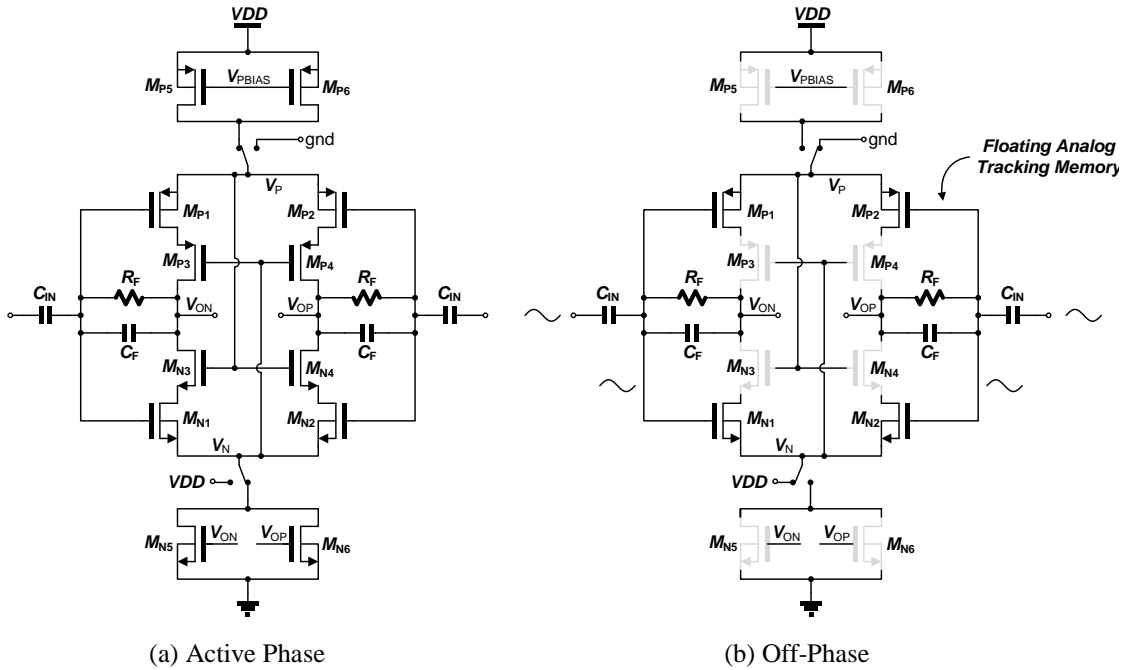


Figure 4-6: Preamplifier Schematics for (a) active phase and (b) off phase

continuously even though the amplifier keeps turning on and off to save the power.

Another issues for this dynamic operation is the bias settling time of every node of the preamplifier. The most critical nodes are the input transistors gate nodes because those nodes are fully floating and biased by a huge pseudo resistor. Fortunately, this analog tracking memory can hold the DC operating voltage of the input transistors during the off phase, and can help to settle the correct DC operating when the preamplifier is in active mode.

In order for this analog tracking memory to work properly as intended, the floating node need to be designed to minimize any charge injection and leakage which can destroy the input signal as well as DC bias information. To prevent the charge injection issue, the preamplifier is designed symmetrically vertically and horizontally for the matching purpose.

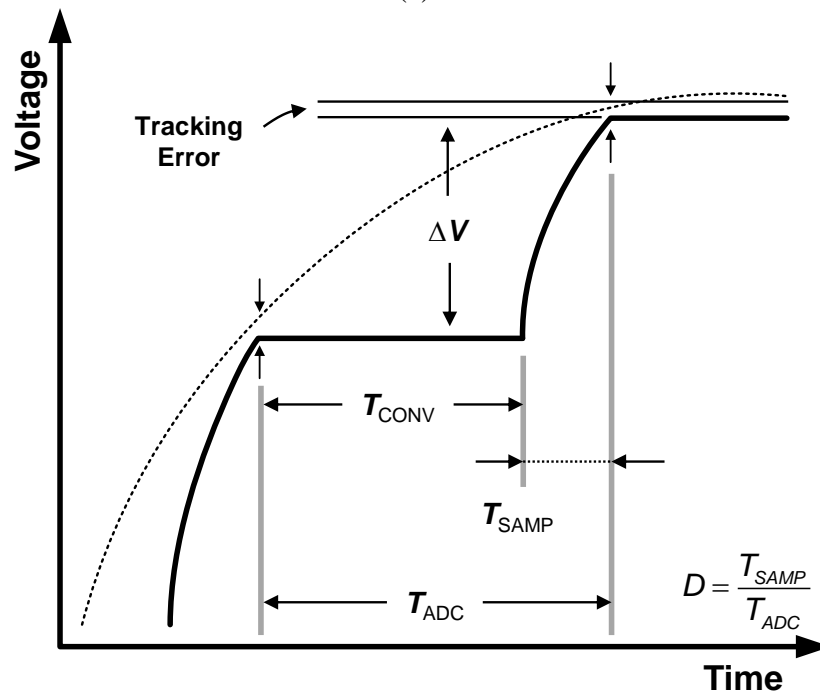
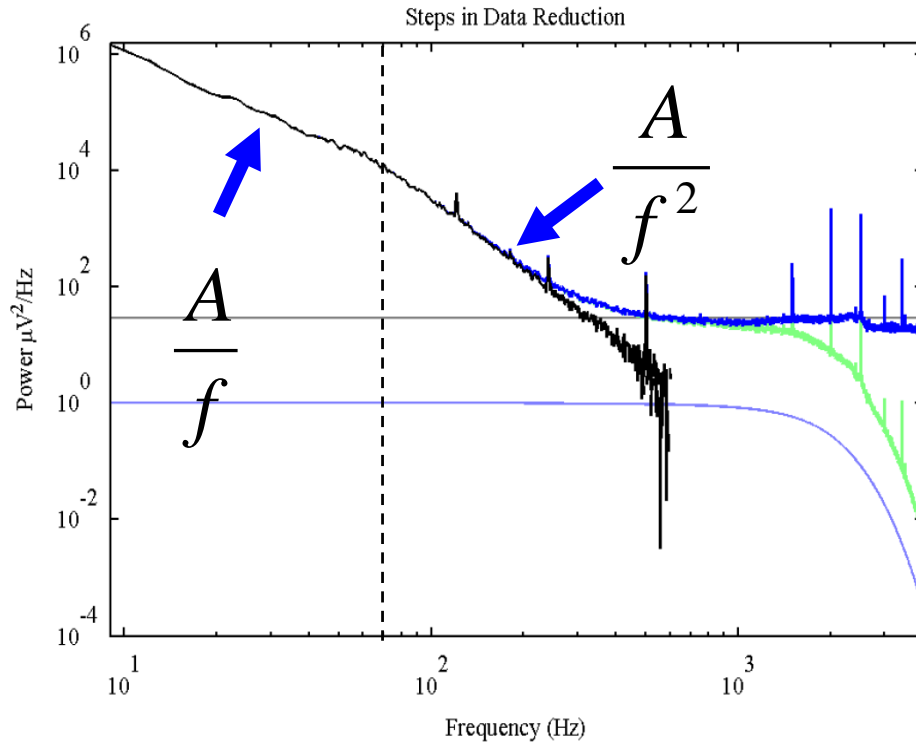


Figure 4-7: (a) ECoG Signal Power Spectrum and (b) Tracking Error of the Preamplifier

#### 4.2.2.2 Required Bandwidth for ADC Track and Sampling

As shown in Figure 4-6, the cascade transistors can hold the output value when the preamplifier turns off. This property helps the preamplifier to track the input signal. However, because the time period for tracking is limited which is ADC sampling time, the preamplifier needs to have the bandwidth to keep the tracking error below the half LSB. The typical tracking error from the analysis of [72] can be derived as follows:

$$\text{Maximum Slope during OFF Phase: } 2\pi f_s \cdot A \cdot \cos(2\pi f_s \cdot t) = 2\pi f_s \cdot A, \quad \text{Eq. 4-1}$$

$$\text{Maximum Error} = 2\pi f_s \cdot A \cdot t_{OFF} \cdot e^{-2\pi f_{3dB} \cdot t_{ON}} < \frac{1}{2} \text{LSB} = \frac{1}{2} \cdot \frac{0.5}{2^{10}} = \frac{1}{2^{12}}, \quad \text{Eq. 4-2}$$

$$\text{Minimum Required Bandwidth} = f_{3dB} > \frac{\ln(2^{13} \cdot \pi \cdot f_s \cdot A \cdot (1-D)/f_A)}{2\pi D/f_A} \quad \text{Eq. 4-3}$$

$$\text{Min. Bandwidth from ECoG Signal} = f_{3dB\_ECoG} > \frac{\ln(2^{13} \cdot \pi \cdot A \cdot (1-D)/f_A)}{2\pi D/f_A} \quad \text{Eq. 4-4}$$

where A is maximum signal amplitude,  $f_s$  is a maximum signal frequency,  $f_{3dB}$  is the required preamplifier's bandwidth and  $t_{ON}$  is the time when the preamplifier is active. For this analysis, we assumed that the signal amplitude is constant for all the signal frequency range. However, as shown in Figure 4-7 (a), the actual ECoG signal decreases as the frequency increases. If we apply this bio-signal characteristics of  $A(f) = \frac{A_0}{f^2}$  for  $f >$

70Hz or  $A(f) = \frac{A_0}{f}$  for  $f < 70\text{Hz}$  into the Eq. 4-1 and Eq. 4-2, we can derive the

bandwidth requirement driven by the bio signal characteristics as shown in Eq. 4-4. To

calculate the worst case,  $A(f) = \frac{A_0}{f}$  is applied into the equations. The required

bandwidths are compared with different duty cycle conditions as shown in Figure 4-8.

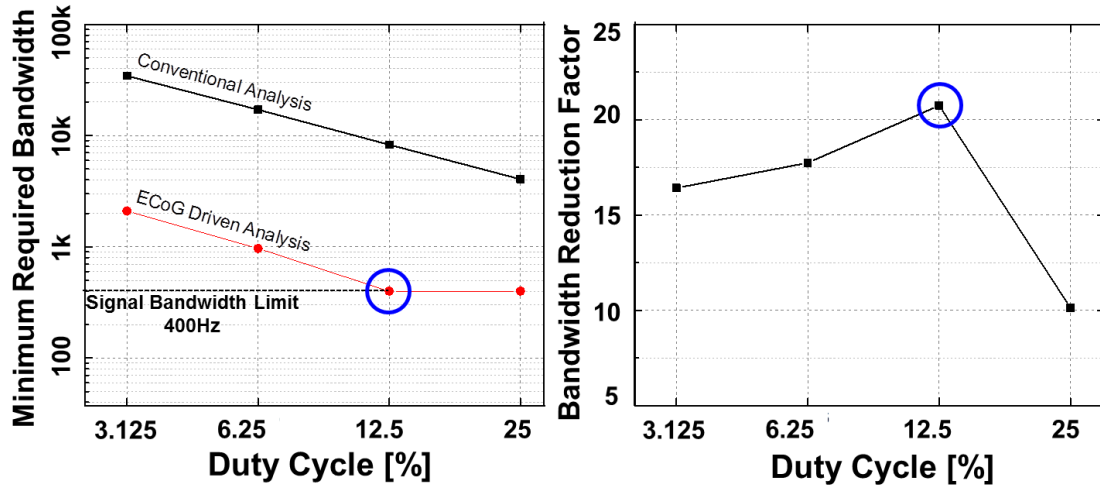


Figure 4-8: Preamplifier Bandwidth Requirement Comparison with Conventional Approach and ECoG Bio-Signal Driven Approach

From the analysis driven by ECoG signal characteristic, the actual required bandwidth for the preamplifier (or ADC driver) can be twenty times lower than those of the conventional approaches. This means that for ECoG application, we can optimize the bandwidth and save power without any significant tracking error. By comparing the bandwidths from the conventional analysis and ECoG driven analysis, the optimized duty cycle and bandwidth have been selected to be 12.5% (1/8) and 400 Hz, respectively.

#### 4.2.3 Preamplifier Cyclic Operation

The cyclic operation can be explained as follows: At active phase, the top and bottom bias transistors ( $M_{N5,6}$  and  $M_{P5,6}$ ) are connected and the transistors ( $M_{N3,4}$  and  $M_{P3,4}$ ) acts as cascade transistors. During off phase, bias transistors are disconnected from the input transistors, and the floating gates of the input transistors can track the input signal by capacitive coupling through  $C_{IN}$  as an analog tracking memory. And, the cascade transistors are turned off and effectively hold the output value as shown in Figure 4-9 which will help to track the signal when the preamplifier is active.



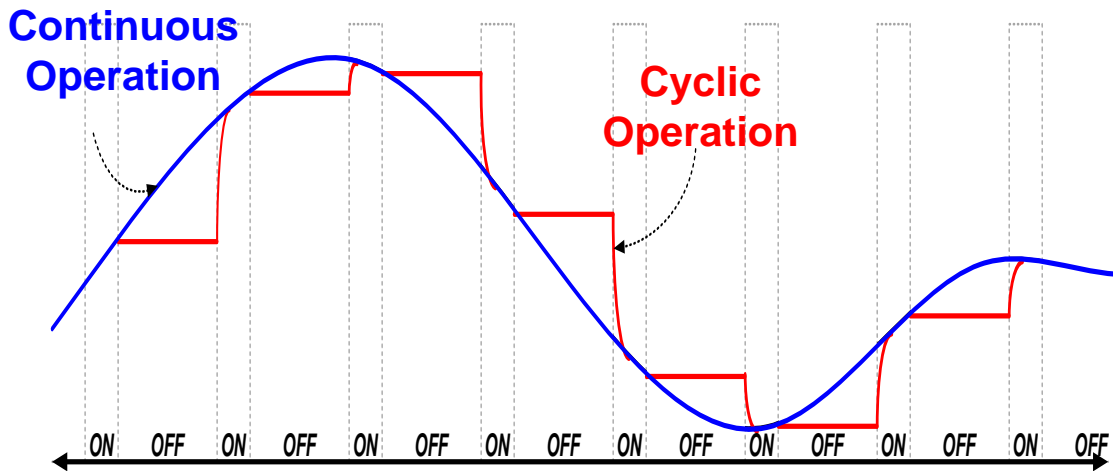


Figure 4-9: Preamplifier Output Comparison with Continuous Operation and Cyclic Operation with Analog Tracking Memory

#### 4.2.4 Current-Controlled Tunable Pseudo Resistor

Diode connected pseudo resistors are widely used by many neural amplifier configurations. However, the resistor value is highly dependent on the process variation and temperature. Also, the value is not linear like the real resistor. Tunable pseudo resistor can calibrate the designed pseudo resistor as well as provide various bandwidths. The basic idea is to keep gate-source voltage of the pseudo resistor for higher linearity. And, for the tunable pseudo resistor, we can control the gate-source voltage using current or voltage control methods. To realize this issue, several techniques have been proposed [50], [72]. In their approaches, either floating current sources or voltage monitoring methods is utilized. However their control blocks are complicated and the voltage monitoring circuit can cause a leakage problem which may cause problems in our cyclic operation. In this work, we propose a current-controlled tunable pseudo resistor as shown in Figure 4-10. To monitor the voltages of node A and B, and keep the gate-source voltage of PMOS transistors, NMOS transistors with programmable current sources are

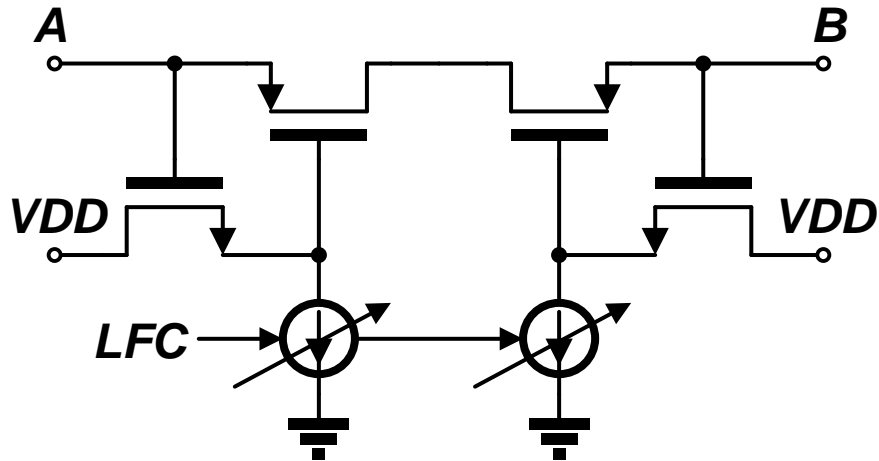


Figure 4-10: Schematic of Proposed Current-Controlled Tunable Pseudo Resistor

utilized. Even though the properties of NMOS and PMOS are not identical, the current ratios between these two transistors are proportional to their aspect ratio. And, we can tune and calibrate the pseudo resistor value for the target value by changing the bias current.

#### 4.2.5 Measurement Results

The proposed preamplifier is fabricated by TSMC 0.18  $\mu\text{m}$  CMOS technology. With 1V power supply, the proposed amplifier is characterized with different duty cycles. The proposed cyclic operation is compared with conventional continuous operation mode with various bias conditions. For the conventional preamplifier, the frequency responses are measured as shown in Figure 4-11. The current-controlled tunable pseudo resistor can modulate the high pass corner with precise frequency ratio. Because the noise output of cyclic preamplifier is impossible to be measured directly, we first digitize the preamplifier output using external DAC with low-pass filter. To verify the system noise, the input referred noises from a continuous operating amplifier before (A) and after (B) digitization. Figure 4-12 shows the measured input referred noise.

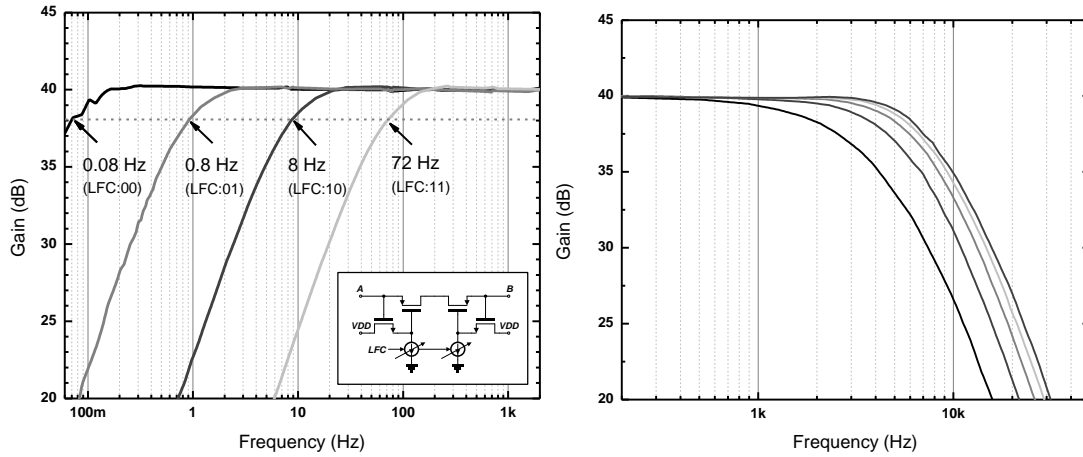


Figure 4-11: Programmability of Preamplifier Bandwidth

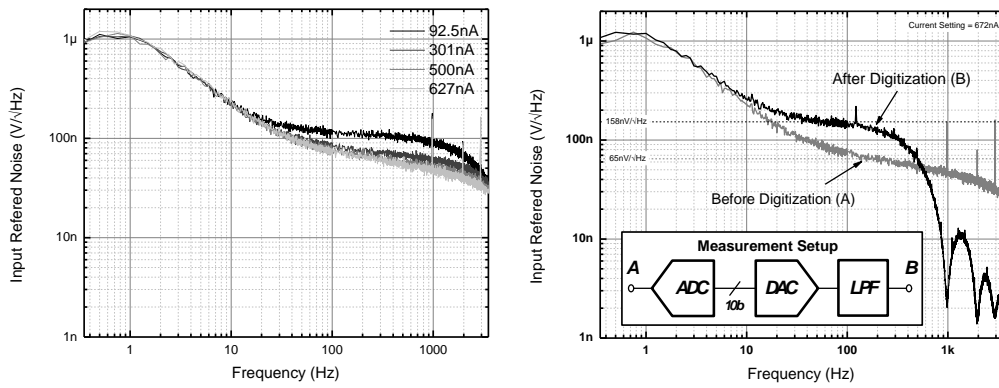


Figure 4-12: The measured Input-referred Noise for Continuous Operation before ADC and After ADC comparison

Table 4-1: TDM Operating Mode Summary for Preamplifier

Number of Cyclic Channels (NCC)	# of Simultaneously Operating Channels	Effective Power Consumption
0	32	100%
4	8	25%
8	4	12.5%
16	2	6.25%
32	1	3.125%

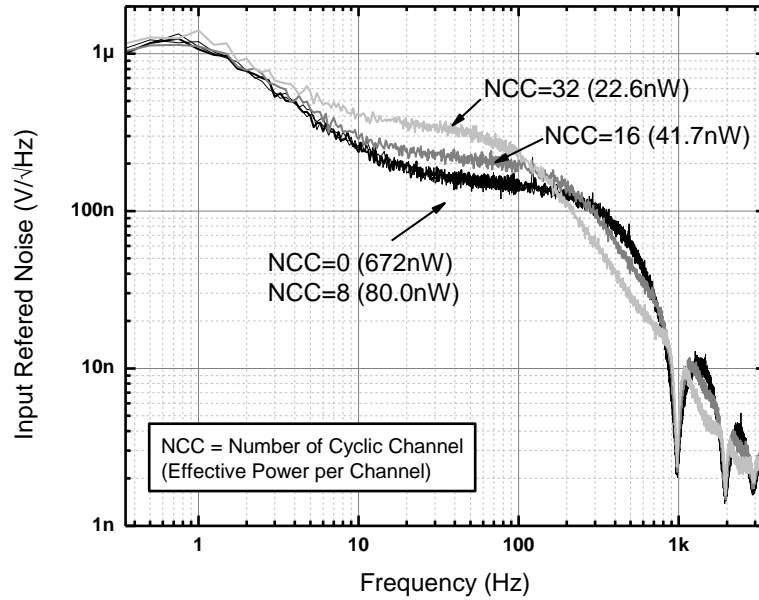


Figure 4-13: Noise Performance Comparison after Digitization

As for the cyclic operation, the noise performance is measured after digitization by internal ADC and reconstructed using external DAC. This measurement setup reflects all the system noise including the imperfection of an internal SAR ADC, measurement setup noise and the external digital to analog converter noise. For the intensive characterization, the cyclic operation is designed to be programmable with five different operating modes as shown in Table 4-1. For the pair comparison, the preamplifier performance of all the five modes are measured at the output of external DAC. Noise performances from all the TDM modes are measured and compared in Figure 4-13. As mentioned earlier, the noise measurement includes all the noise presents in the signal path which includes preamplifier, PGA, ADC driver, ADC, Digital signal path, DAC and LFP. For the fair power consumption comparison, PGA and ADC driver bandwidths are fixed to be 500Hz for NCC=0,4,8, and 1kHz for NCC=16, 32 which are chosen based on the ECoG signal driven analysis. As we can see, the system level noise including the quantization noise from the internal SAR ADC and the digitization and DAC dominates the noise and is the

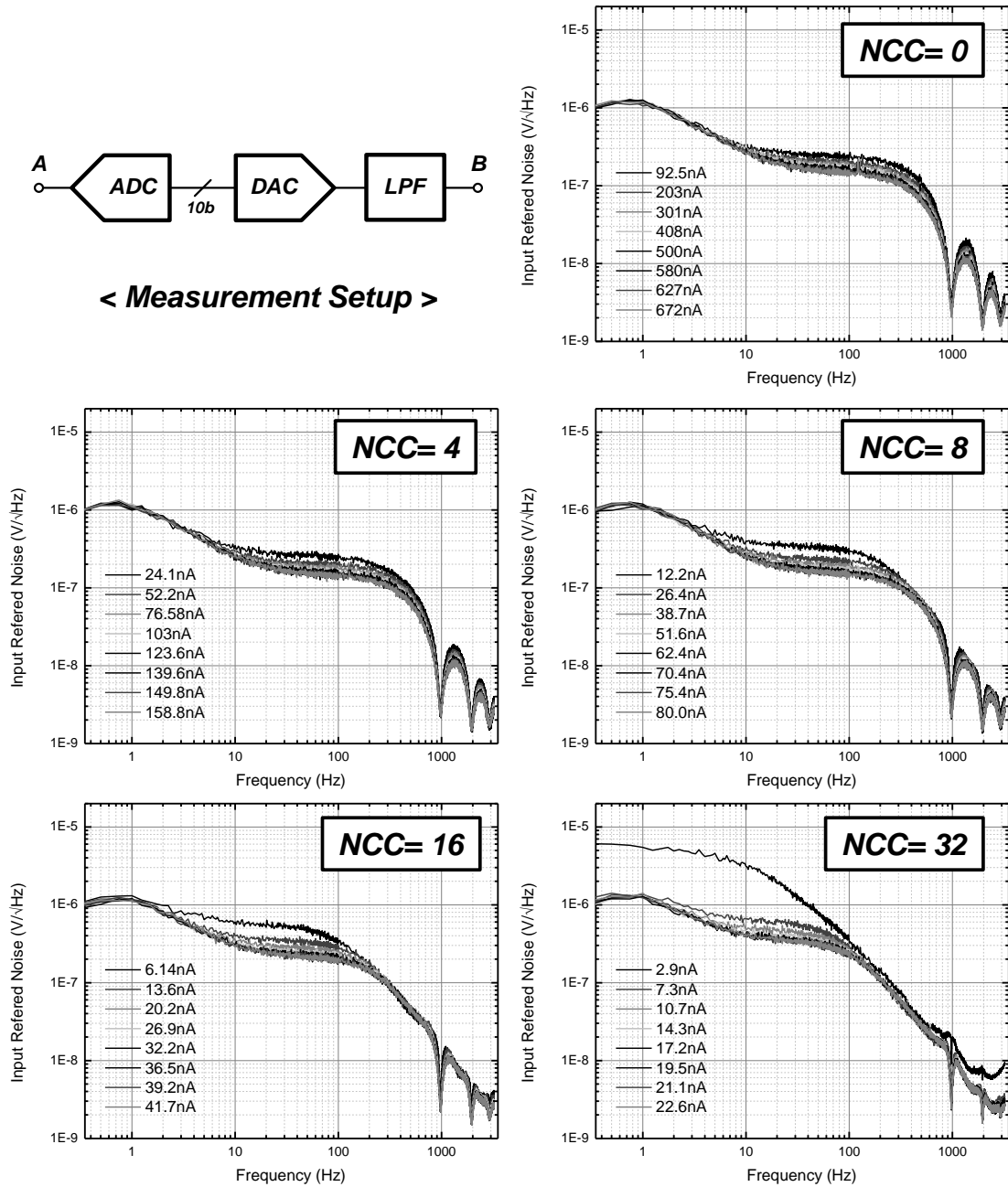
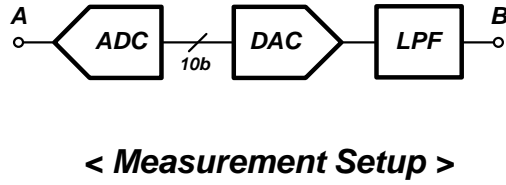


Figure 4-14: Measured Input Referred Noise for Various Operating Modes under Various Bias Conditions

limiting factor for NCC=0,4,8. For NCC=16, the bandwidth is more than the ADC sampling frequency, and the noise is folded back to baseband and eventually the noise floor increases as expected. For NCC=32, because of the limited duty cycle and

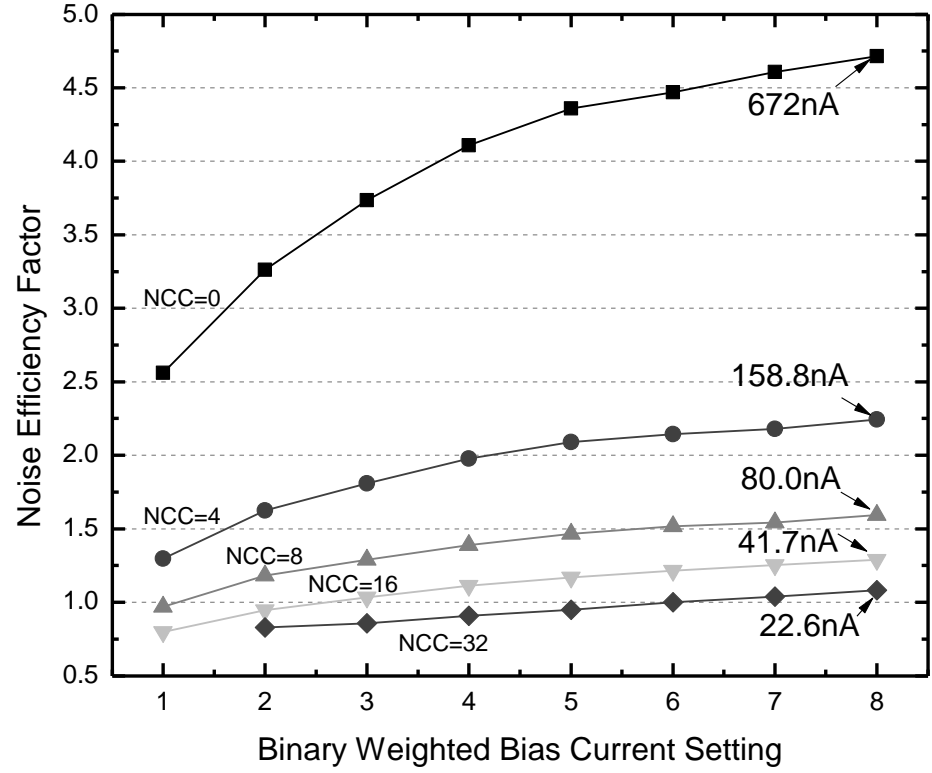
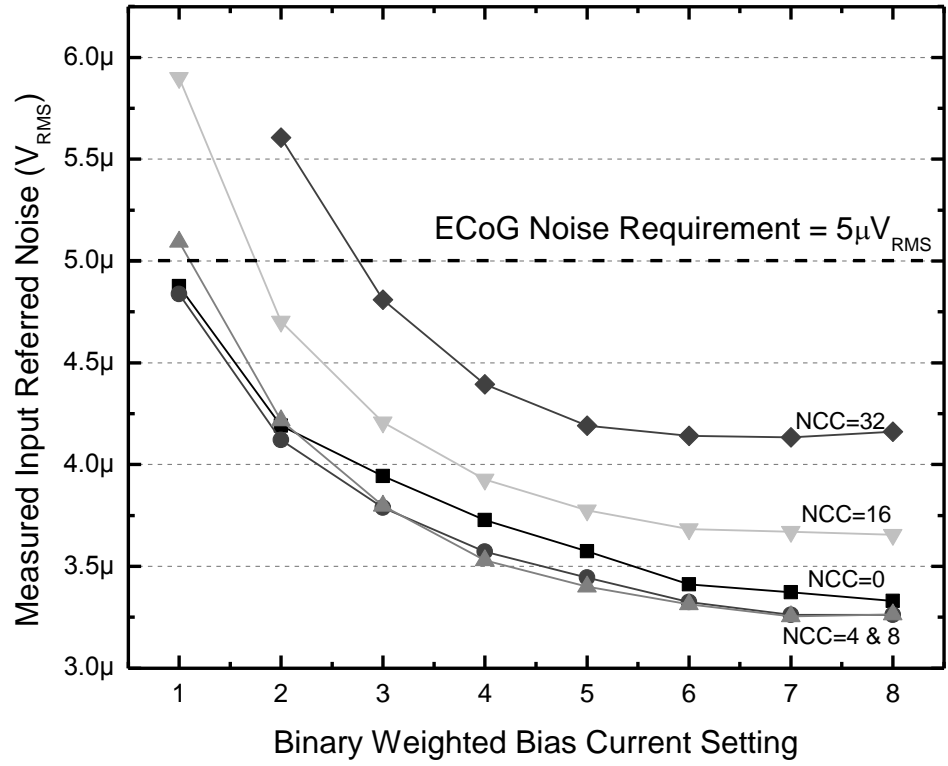


Figure 4-15: Measured Input Referred Noise and Calculated Noise Efficiency Factors

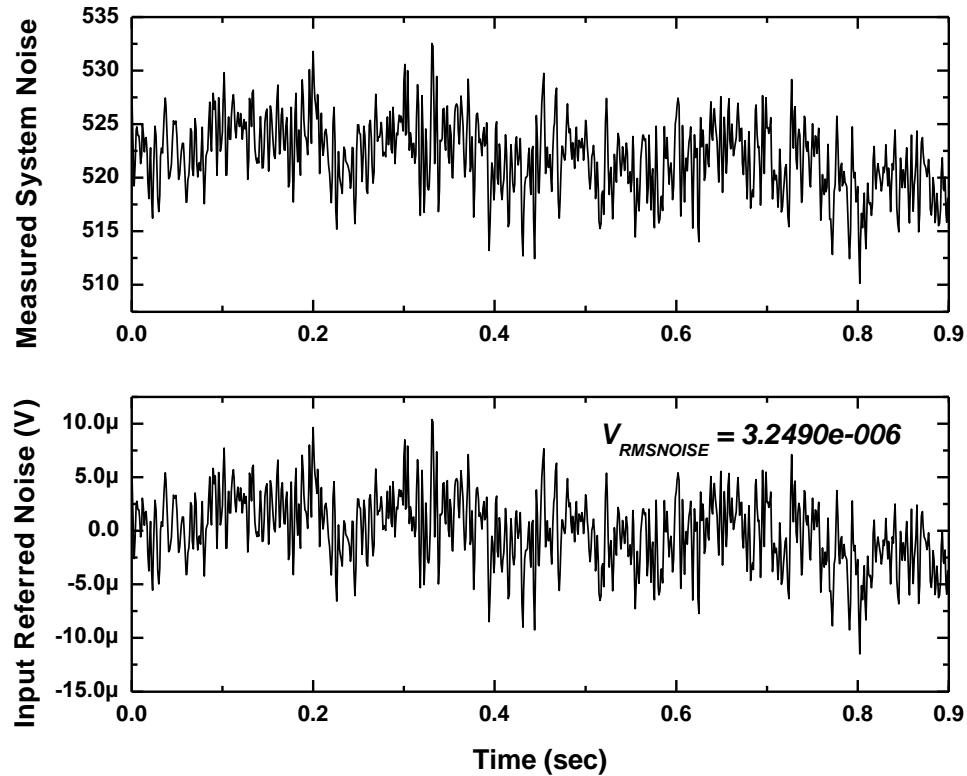


Figure 4-16: Measured System Noise after Digitization and its Input Referred Noise value of  $3.25 \mu\text{V}_{\text{RMS}}$

bandwidth of PGA, the bias conditions are not well settled and the preamplifier can not track the signal propely, and effectively, the bandwidth decreases as shown in Figure 4-13. From the graph,  $\text{NCC}=8$  is the optimized condition for noise and power performance. In this case, the effeective power consumption is  $80\text{nW}$  with the input referred noise of  $3.26\text{V}_{\text{RMS}}$  for  $0.1\text{Hz}$  and  $1\text{kHz}$  bandwidth. The noise efficiency factor decreases down to 1.6. The detailed measured input referred noise for various modes under different bias conditions are shown in Figure 4-14. The summarized NEF and input refered noise is shown in Figure 4-15. For the optimal condition( $\text{NCC}=8, \text{Bias Condition}=8$ ), the ADC output noise is recoded and converted back to input referred signal level as shown in Figure 4-16. The measured rms noise is  $3.25 \mu\text{V}_{\text{RMS}}$  For a given target noise level of  $5 \mu\text{V}_{\text{RMS}}$ , the possible minimum power consuming mode is  $\text{NCC}=32$

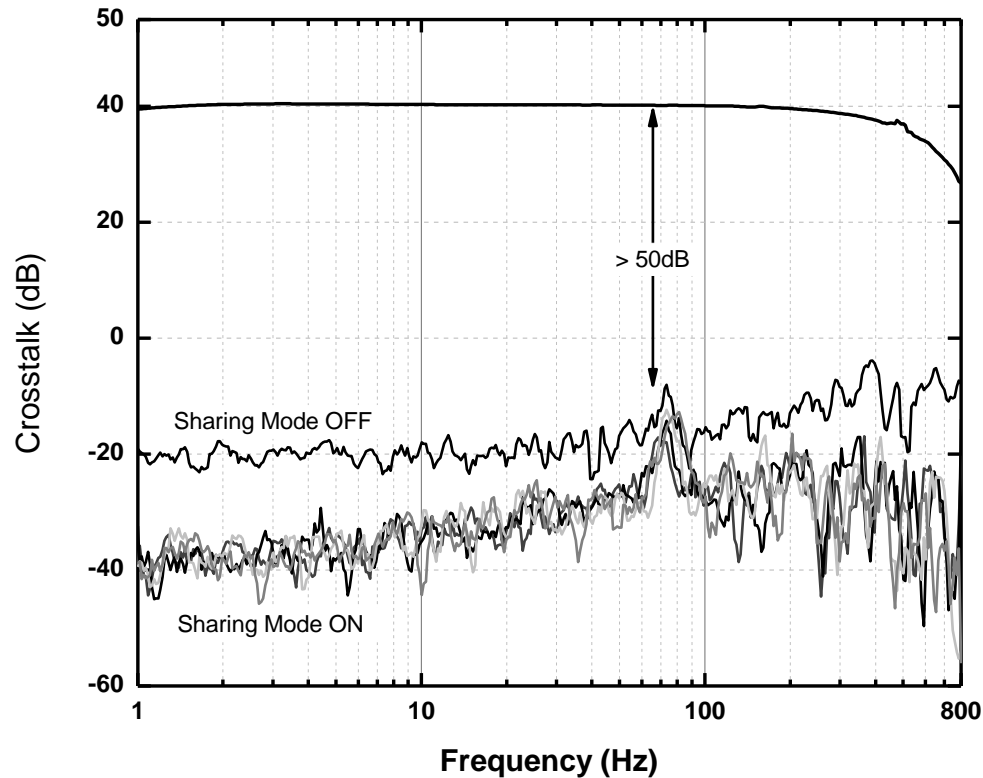


Figure 4-17: Measured Channel Crosstalk for the different TDM modes

with bias condition of 3 with limited bandwidth below 100Hz. At this configuration, the NEF will be 0.61 with input referred noise of  $4.39 \mu\text{V}_{\text{RMS}}$ .

To check the switching effect to the adjacent channels, the channel crosstalk has been measured as shown in Figure 4-17. The crosstalk for sharing mode on (NCC=4,8,16,32) shows better performance than sharing mode off (NCC=0) because for the sharing mode on, the adjacent channels are not operating, thus less crosstalk than sharing off mode. For overall channel isolation is more than 50dB. The measured PSRR and CMRR are 50dB and 60dB, respectively, as shown in Figure 4-18 and Figure 4-19. Due to the virtual ground provided to NMOS transistor, it shows enhanced CMRR performance compared to the previous version in chapter 3. The pre-recorded ECoG signal is applied, by the headstage tester unit which is used to test the commercially available headstage, to preamplifier and the outputs are recorded for different NCC modes.



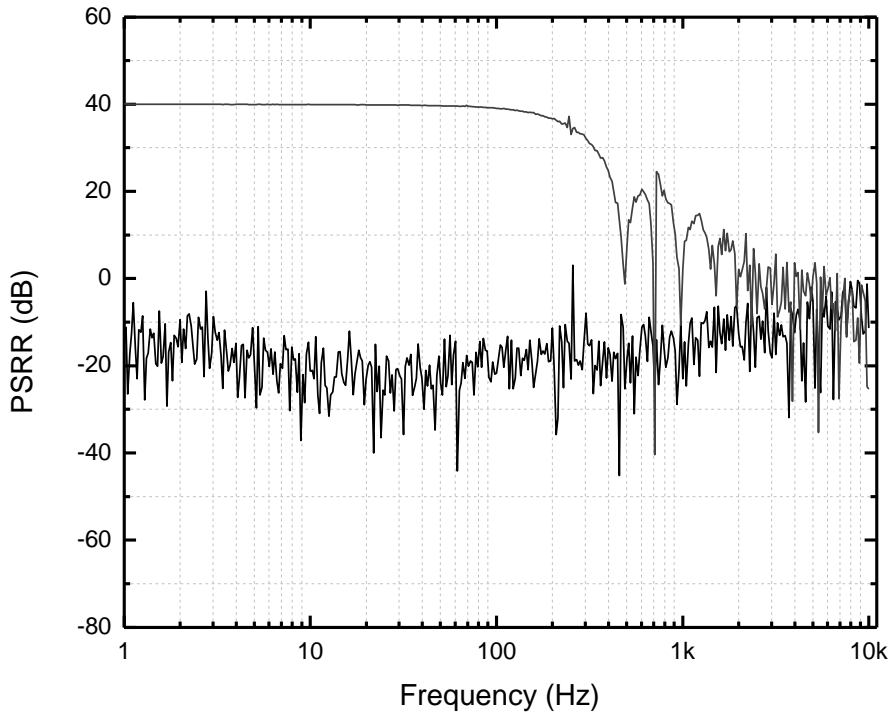


Figure 4-18: Measured Power Supply Rejection Ratio

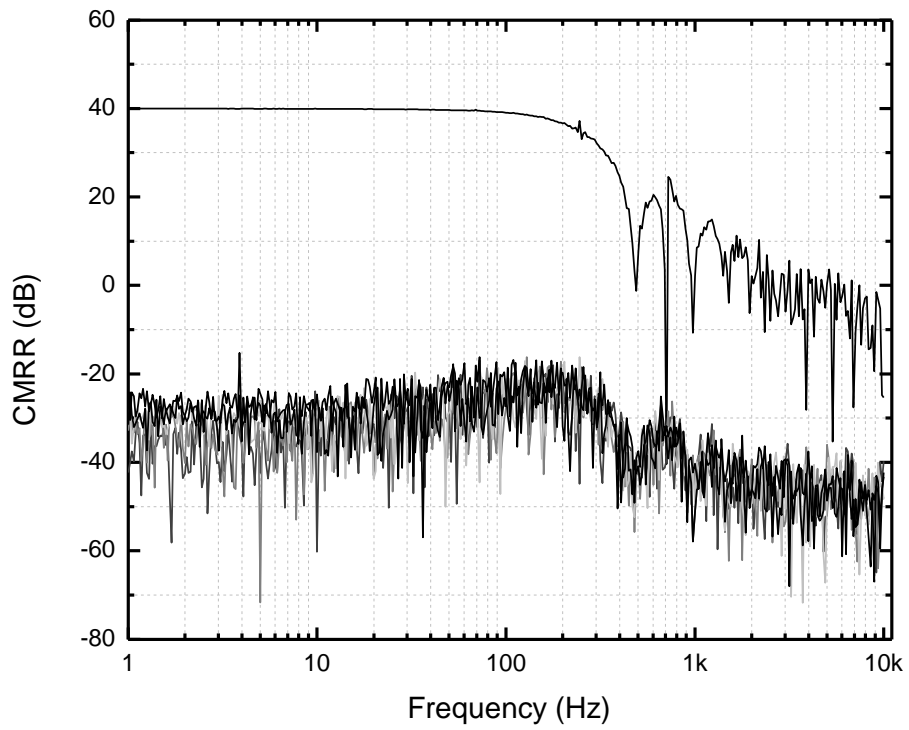


Figure 4-19: Measured Common Mode Rejection Ratio

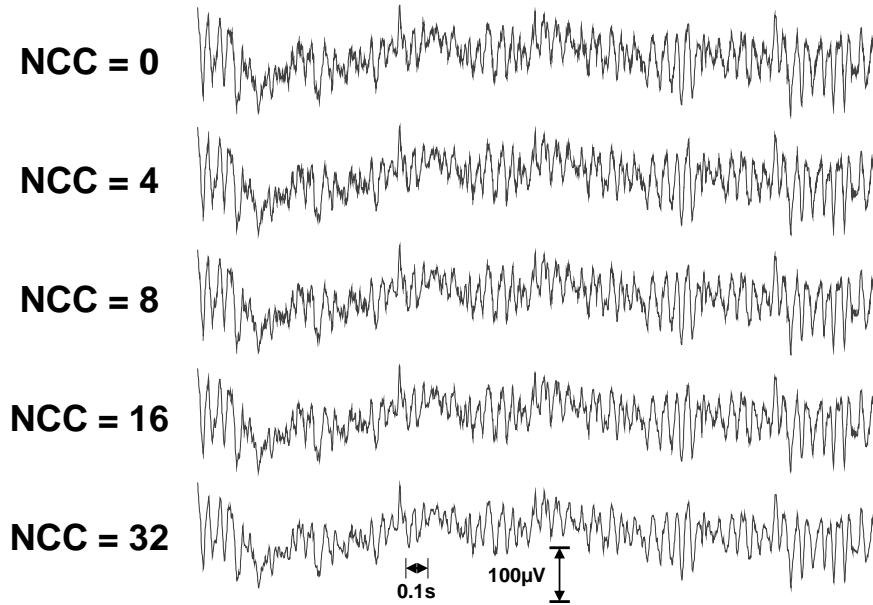


Figure 4-20: Measured Pre-recorded ECoG Signal with Different NCC Modes

Table 4-2: The Proposed Preamplifier Performance Table

<b>Measured Preamplifier Characteristics</b>		
<b>Technology</b>	<b>0.18 <math>\mu\text{m}</math> CMOS</b>	
<b>TDM Modes (Effective Power)</b>	<b>0(1), 4(0.25), 8(0.125), 16(0.0625), and 32(0.03125)</b>	
<b>Supply Voltage</b>	<b>1 V</b>	
<b>Operating Condition</b>	<b>NCC= 0</b>	<b>NCC= 8</b>
<b>Effective Power Consumption (ADC Sampling Freq. = 1kS/s)</b>	<b>672nW</b>	<b>80nW</b>
<b>Input Referred Noise (0.1Hz~1kHz)</b>	<b>3.33 <math>\mu\text{V}_{\text{RMS}}</math></b>	<b>3.26 <math>\mu\text{V}_{\text{RMS}}</math></b>
<b>NEF</b>	<b>4.71</b>	<b>1.59</b>
<b>Max. Input Range (THD=1%)</b>	<b>1.4mV</b>	<b>1.2mV</b>
<b>CMRR / PSRR</b>	<b>&gt; 50dB / &gt;60 dB</b>	
<b>Channel Isolation</b>	<b>&gt; 50dB</b>	
<b>Active Area</b>	<b>120 <math>\mu\text{m}</math> x 260 <math>\mu\text{m}</math> (0.0312mm<sup>2</sup>)</b>	

The measured maximum input ranges for THD of 1% distortion are 1.4mV for NCC=0, and 1.2mV for NCC=4,8,16, and 32. The preamplifier's characterizations are summarized in Table 4-2.

For an AC coupled preamplifier, a metal-insulator-metal (MiM) capacitor is utilized to form the high pass filter and to set the gain. The typical value of MIM is  $1\text{fF}/\mu\text{m}^2$  and active components such as transistors are typically prohibited under the MiM capacitor. And, this MiM occupies more than 50% of preamplifier area. To address this issue, DC coupled neural amplifiers has been proposed previously. However, recent technology such as TSMC  $0.18\mu\text{m}$  provides  $2\text{fF}/\mu\text{m}^2$  and allows MiM capacitor over the circuits. And from this option, we reduced the area by more than 60% as shown in Figure 4-21.

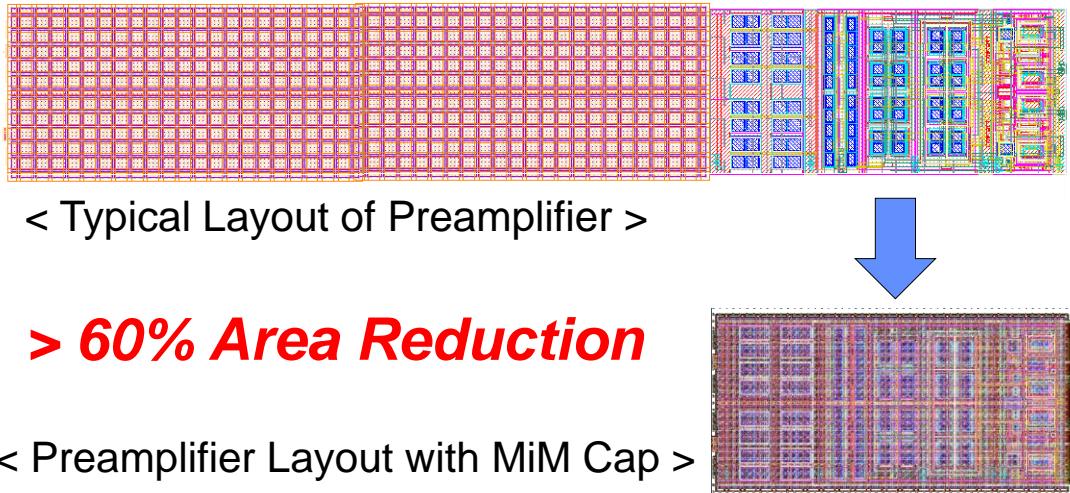


Figure 4-21: Area Reduction Comparison (Layout View)

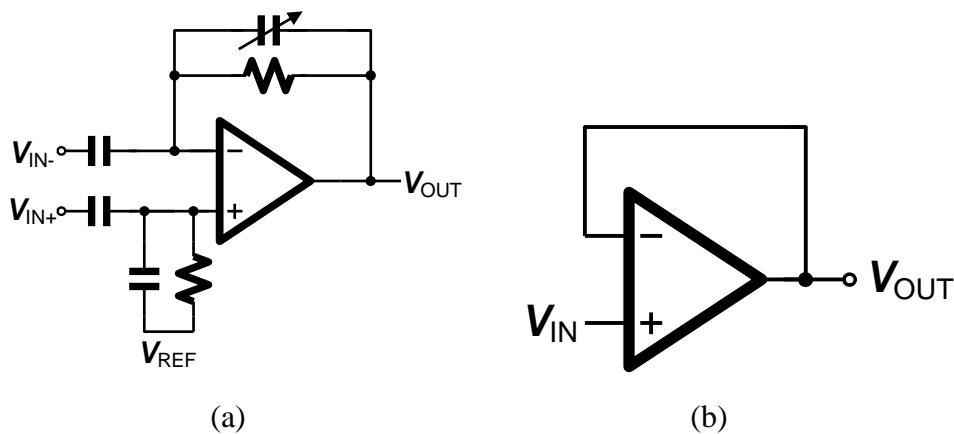


Figure 4-22: Schematic of Programmable Gain Amplifier and ADC Driver

### 4.3 Programmable Gain Amplifier and ADC Driver

In the signal path, the programmable gain amplifier is designed to provide an additional analog gain before the ADC and also to cut off any signal above 500Hz as an antialiasing filter. From the ECoG signal driven analysis, a 500Hz bandwidth is enough to drive the ADC capacitive DAC with negligible error. The gain is programmable to be 1, 2, 5, and 10 with different feedback capacitances. However, this capacitive feedback configuration is very vulnerable for the kickback effect caused by charge injection of the sampling circuit of ADC. Especially, this affects the preamplifier input stage as well which will generate an error. To prevent this effect, we also integrate a ADC driver. Figure 4-23 shows the measured various gain setting.

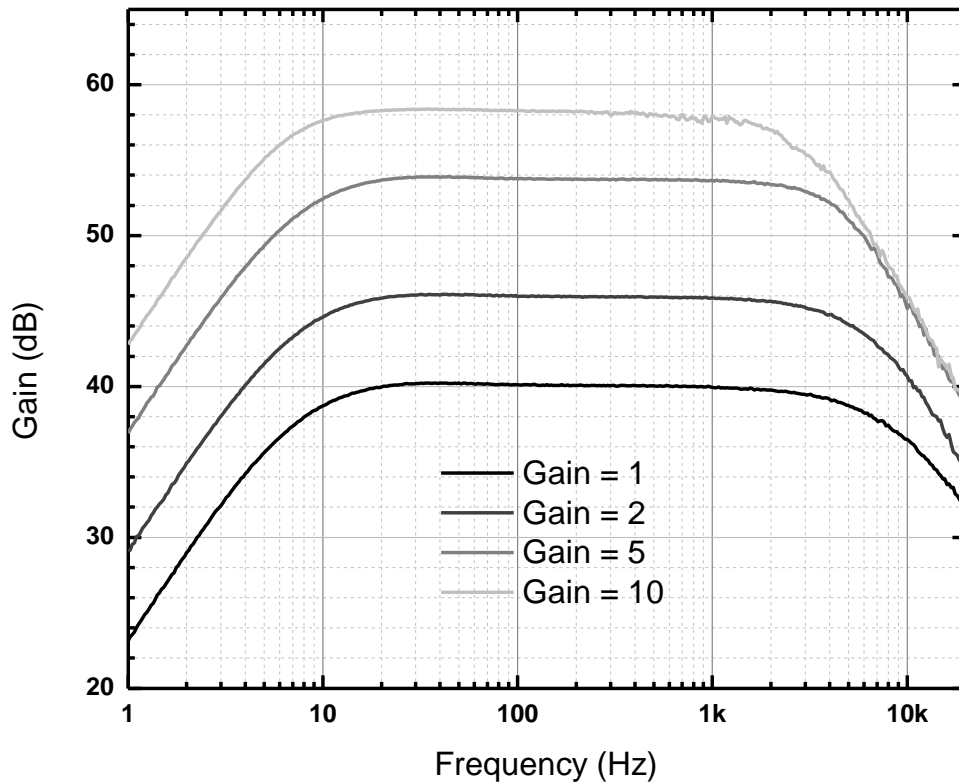


Figure 4-23: Measured Programmable Gain

#### 4.4 0.5V SAR ADC with Embedded Level-Shifter

To optimize the overall performance of the mixed-mode system, multiple power supplies approach can enhance the system-level optimization. For low-power consumption of slow operating digital circuit ( $< 10\text{MHz}$ ), low supply voltage approach below 1V is simple and effective. However, this approach is not always valid for analog blocks because low supply voltage can easily degrade output swing thus dynamic range, common mode (CMRR) and power supply (PSRR) rejection performance. For this reason, in this work, analog blocks operate under 1V power supply while digital blocks operate under 0.5V power supply. As an interface circuit between analog domain and digital domain with different power supply, an analog to digital converter is required to have a level-shifting capability as shown in

Figure 4-24. This level-shift feature also helps to relieve the requirement for rail-to-rail output operation of analog blocks which requires complicated structures. In this section, the embedded level-shifting operation of SAR ADC will be discussed.

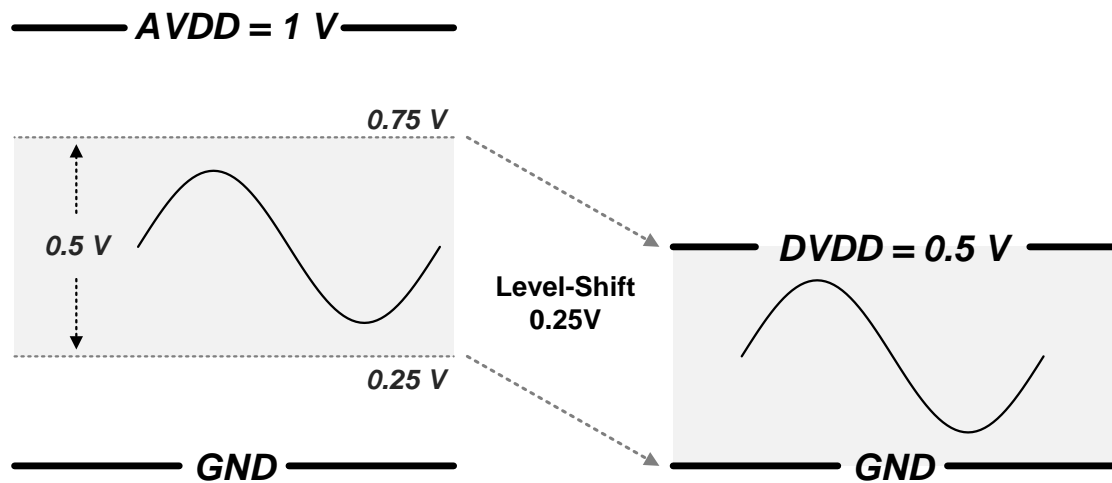


Figure 4-24: Level-Shifting Concept for Multiple Power Supplies System.

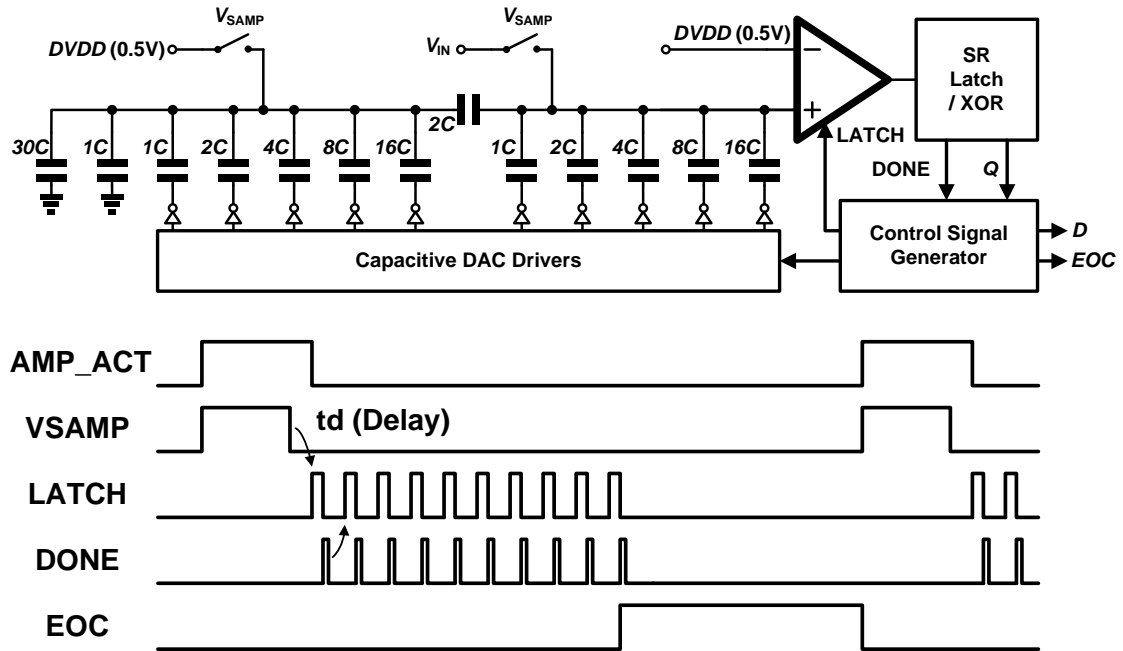


Figure 4-25: Overall Architecture and Timing Diagram of the Proposed SAR ADC.

#### 4.4.1 Overall Architecture

The proposed SAR ADC has a comparator, SAR logic, capacitive array, and bootstrap switches as shown in Figure 4-25. When a preamplifier is active, the VSAMP goes high and the preamplifier's output is traced and samples at the falling edge. After the delay time ( $t_d$ ), this falling edge activates LATCH signal to start conversion. When the conversion completes, DONE signal is generated. After updating the capacitor array DAC value, the DONE signal generates LATCH signal again for the next step conversion. This procedure continues until the end of the ADC operation, EOC. The individual circuit blocks are identical with a SAR ADC in chapter 3.

#### 4.4.2 Embedded Level-Shifting Operation

The mentioned level-shifting can be performed by modifying ADC control signals without any additional hardware. The operation is explained in the Figure 4-26. For

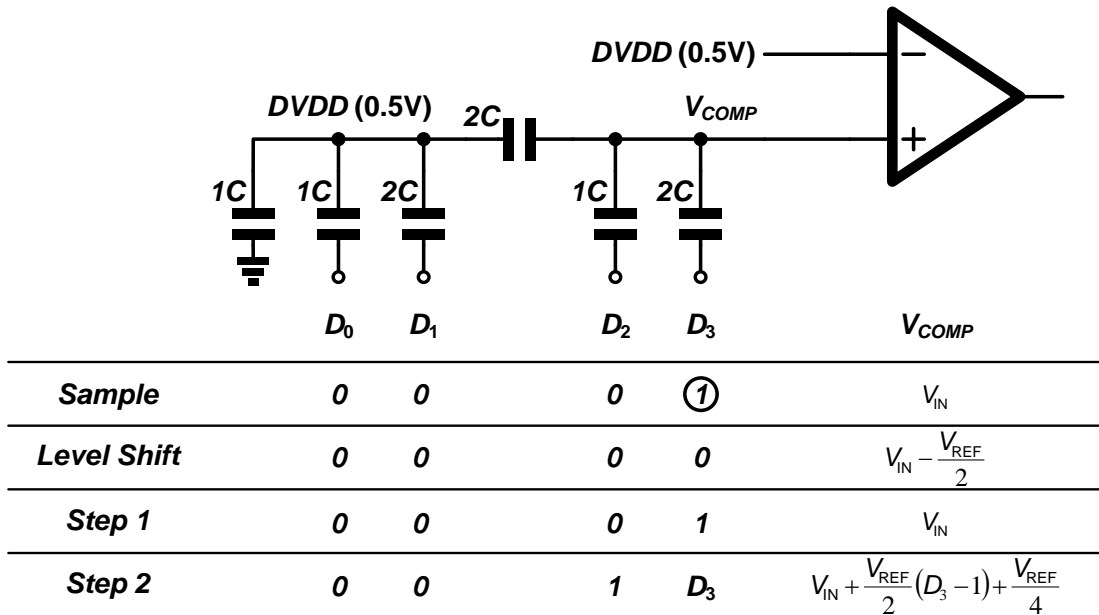


Figure 4-26: Embedded Level-Shifting Operation

simplicity, 4 bit ADC is used for the explanation. In a conventional SAR ADC operation with power supply as a reference voltage, all the digital values of  $D_{0-3}$  is set to 0 while sampling. And, the normal operation can be performed in order to determine the final digital values.

However, by setting an initial value of MSB to ‘1’ during the sampling period, we can perform a level-shifting. The procedure is as follows: first,  $D_3$  is set to 1 and other digital bits are set to 0. At this time, the  $V_{COMP}$  equals the sampled  $V_{IN}$ . After sampling and before the first conversion,  $D_3$  value is changed to 0 and  $V_{COMP}$  becomes  $V_{IN} - V_{REF}/2$ . The initial sampled signal  $V_{IN}$  is shifted by  $V_{REF}/2$  which is 0.25V in our design. This simple modification enables the 0.25V level-shifting without any additional hardware. A careful observation of the procedure, we can easily notice that, actually, the level shift step can be omitted and we can perform step 1 comparison right after the sampling phase without any changes of the final value. This procedure of initially setting  $D_3$  to high also helps to save the power to charge a MSB capacitor for the conventional

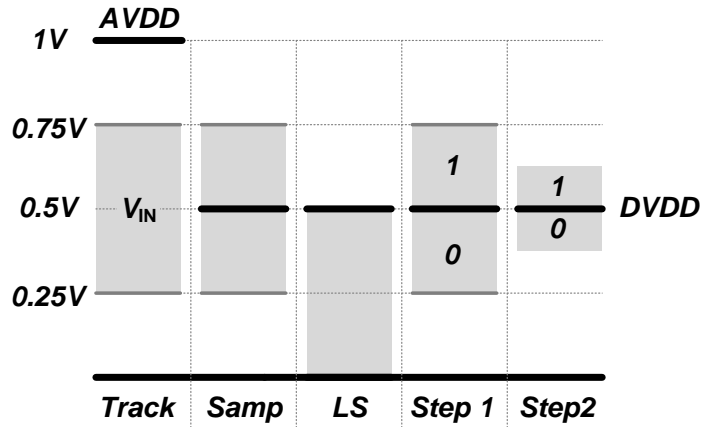


Figure 4-27: Signal Range for each Procedure Steps.

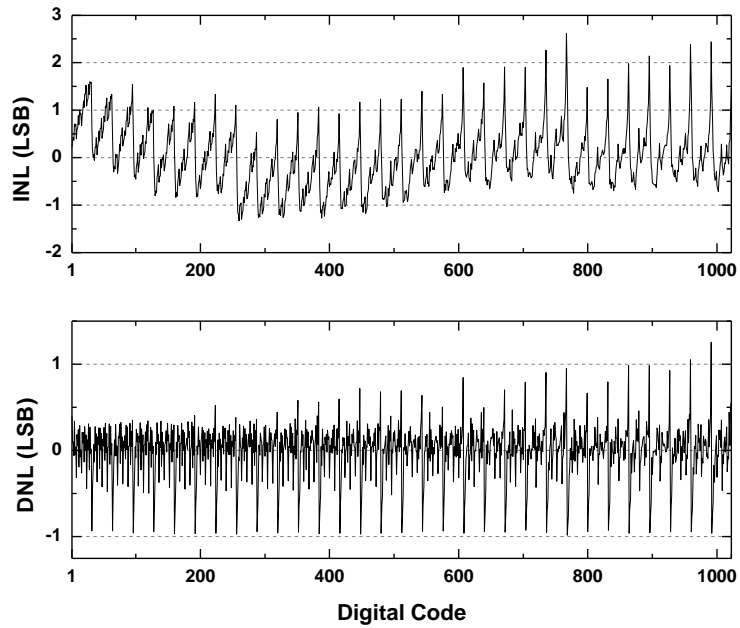


Figure 4-28: Measured INL/DNL of the fabricated SAR ADC.

SAR ADC operation. The signal range with an embedded level-shifting operation is illustrated in Figure 4-27.

#### 4.4.3 Measurement Results

The proposed ADC is fabricated in 0.18 $\mu\text{m}$  1P6M CMOS technology with 0.5V power supply. The ADC core occupies 120 x 280  $\mu\text{m}^2$  with a unit capacitance of 168 fF.



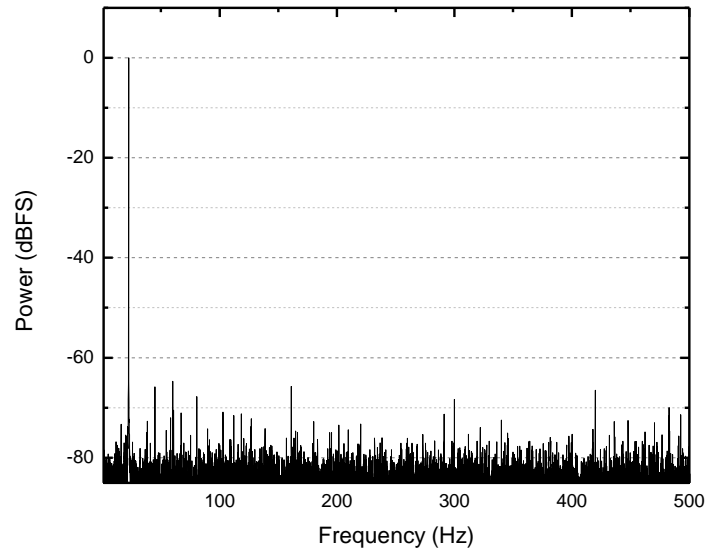


Figure 4-29: FFT output spectrums

Table 4-3: ADC Performance summary

<b>Measured ADC Characteristics</b>	
<b>Technology</b>	<b>0.18 <math>\mu\text{m}</math> CMOS</b>
<b>Sampling Frequency (S/s)</b>	<b>500, 1k, 2k, and 4k</b>
<b>Supply Voltage</b>	<b>0.5 V</b>
<b>Power Consumption (1kS/s)</b>	<b>5.5 nW</b>
<b>Input Range</b>	<b>0.25 ~ 0.75 V</b>
<b>SNDR</b>	<b>45.68 dB</b>
<b>ENOB</b>	<b>7.3</b>
<b>FOM (fJ/c-s)</b>	<b>35</b>
<b>Area (mm<sup>2</sup>)</b>	<b>0.0336</b>

The sampling frequency can be programmable from 500 Hz to 4 kHz which are suitable range for ECoG neural signal application. The measured INL and DNL are 2.6/-1.2LSB and 1.3/-0.98LSB, respectively, as shown in Figure 4-28. Figure 4-29 shows FFT spectrums for 22.39 Hz input signals at 1 kS/s. The measured ADC performance is summarized in Table 4-3.

#### **4.5 Data Compression with Differential Pulse Code Modulation (DPCM)**

In the wireless neural interface system, wireless data transmitter is one of the most power hungry blocks in the system. And, the power consumed by the transmitter is directly proportional to a transmitted data rate. In order to reduce the power consumption of the wireless transmission, a direct solution will be to increase the efficiency of the wireless channel and to optimize the transmitter circuit. Beyond this component-level solution, the simplest and most effective way in the system-level optimization to reduce power consumption is to reduce the data rate by data compression which will make optimal use of limited resources. Typically, data compression can be divided into two categories; lossless and lossy compression. The basic idea of compressing data is to eliminate redundancy of signals.

The lossless compression algorithm exploits a statistical data redundancy and utilizes it to compress data concisely without any information loss. As lossless data compression techniques, there are run-length encoding, Lempel-Ziv, Huffman encoding, and so on. Because these methods use statistical redundancy, it might be a good candidate for spike detection application, where spike occurs sparsely and a huge statistical data redundancy exists. However, for ECoG application, where neural activities happens slowly and statistical data redundancy does not exist, these techniques are not only ineffective but also complicated to implement, and possibly consumes a comparable power to the effect of the wireless power reduction due to the data compression.

On the other hand, the lossy data compression algorithm losses some information while compressing data as the term implies. And, this lost information is impossible to recover later. The fundamental idea of this compression is to extract only variation (either

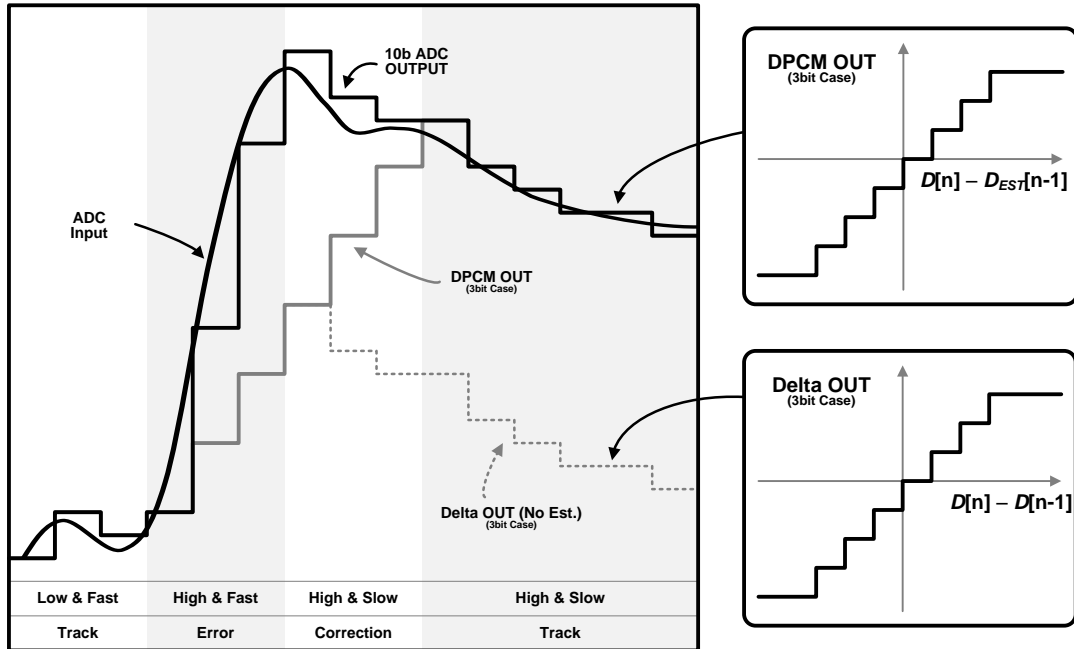


Figure 4-30: Comparison of Delta and DPCM compression

spatial or temporal variation) out of background (or averaged) values. Therefore, the efficiency of this algorithm depends on signal amplitude and frequency. In other words, the lossless data compression is very efficient to compress a signal with slow activity and small amplitude like ECoG. Especially, this algorithm can be simply implementable by using delta operation.

Previously, Aziz proposed delta compression technique to reduce the data rate in analog domain [85]. However, reconstructed neural activity data suffers from severe data loss with high compression rate due to an inherent error accumulation of delta compression. Other simple but effective compression method is a differential pulse code modulation (DPCM), which is used for digital image processing. In this DPCM scheme, it is same as the delta compression in that the output of DPCM is the delta value compared with previous value. However, in case of DPCM, the previous value is an estimated value based on the previous delta values. The effect of this estimation is well

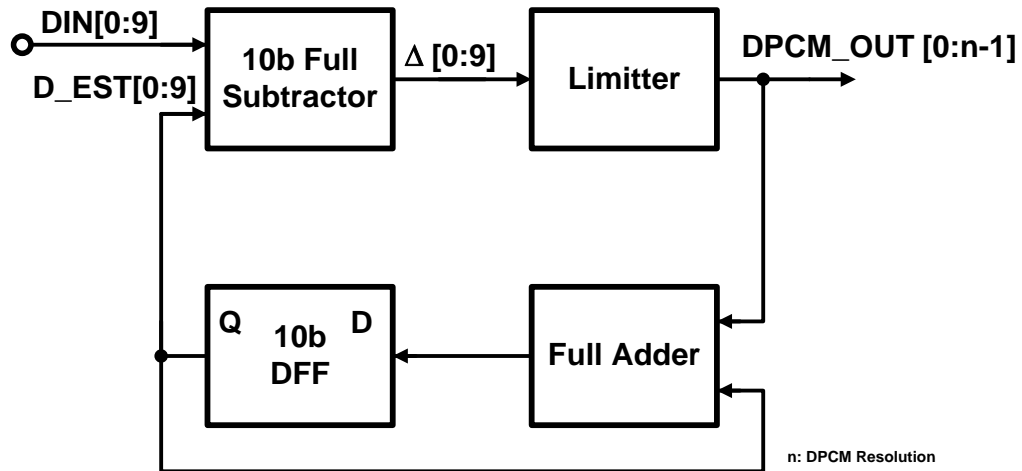


Figure 4-31: Block diagram of DPCM data compression

compared in the Figure 4-30. For both cases, if the signal amplitude variation is higher and faster than the threshold (in this example, 3bits) of the compression block, the data will be lost, and error occurs. Without estimation block like delta compression, the error cannot be restored and the signal loss factor will increase. On the other hand, DPCM has an estimation block that estimates the previous value based on the previous delta information, and compares current ADC output value not with the actual previous ADC output, but with the estimated value. By help of this estimation block, even though the error occurs, it can track and make a correction to alleviate the data loss.

The features explained above shows DPCM can be a good solution for ECoG neural interface system, and this work investigates and implements DPCM data compression and demonstrates how efficiently DPCM compresses recorded data, and affects the overall power consumption.

#### 4.5.1 DPCM Compression Block Architecture

Figure 4-31 shows the block diagram of the DCPM data compress. Data output from ADC (DIN) is subtracted from the estimated value (D\_EST) which is a result of

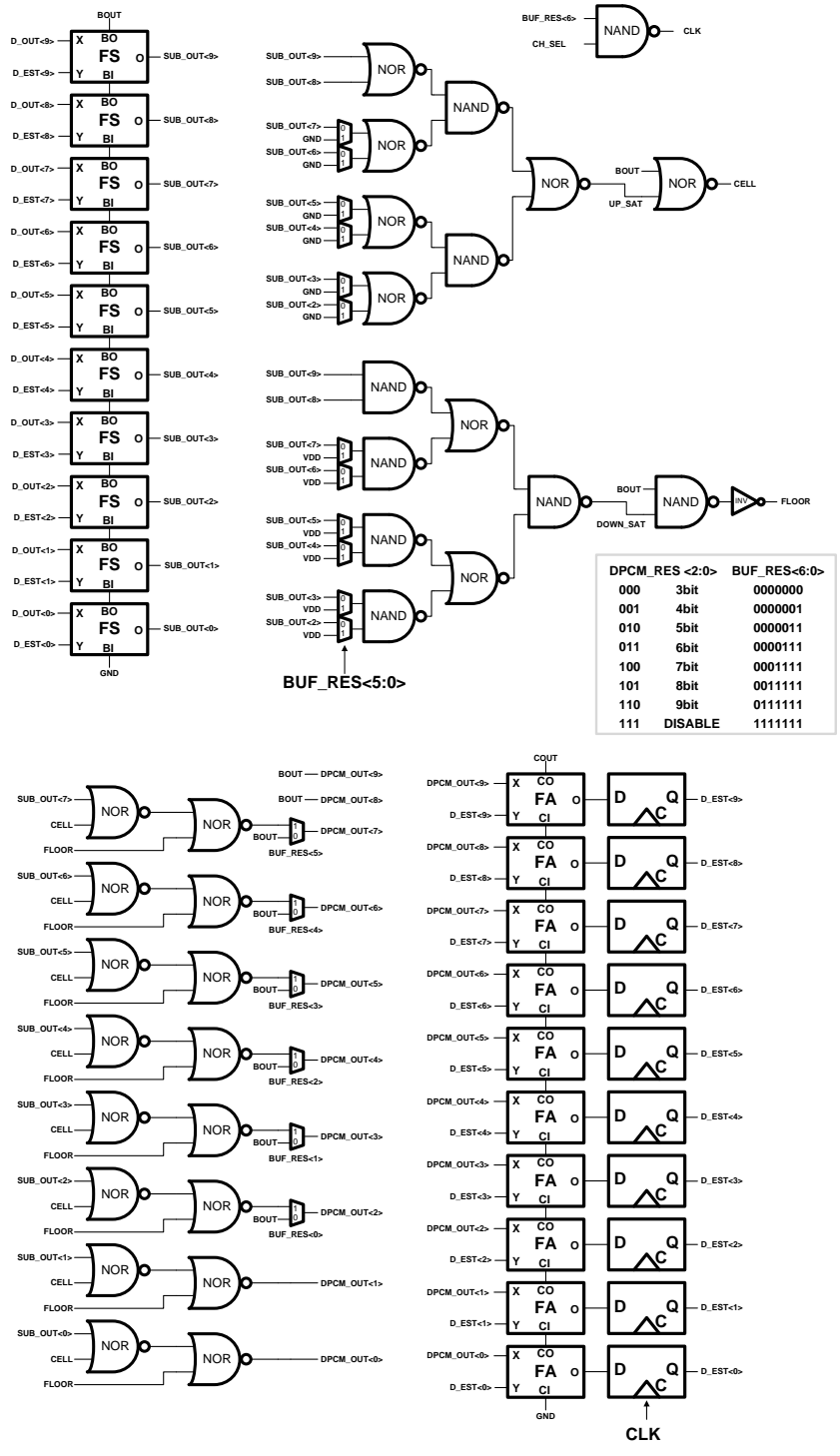


Figure 4-32: Detailed schematics of DPCM data compression

summation of the previous delta outputs (DPCM\_OUT). The detailed schematics of DPCM data compression is shown in Figure 4-32. The resolution of DPCM (n) has been

designed to be programmable from 9bit (1bit compression) to 3 bit (7bit compression). This programmability of the resolution has mainly two purposes. The first purpose is to verify and characterize the effectiveness of DPCM data compression. The second purpose is to optimize the reduction factor for given signal condition. For example, in the ECoG signal, there are several frequency bands with different signal power for different purpose applications such as sleep detection (0.5~25Hz), Parkinson (15~30Hz), epilepsy seizure detection (8~40Hz), and motor planning (140~160Hz). Having programmability of data compression can provide a way to optimize power-noise efficiency even more based on the target signal conditions.

#### 4.5.2 Measurement Results

The fabricated DPCM data compression block has been characterized in this section. In order to verify the system performance, the DPCM measurement has been performed with the analog front-end outputs which reflect all the possible imperfections from the preamplifier, PGA, and ADC. The performance of DPCM compression can be measured using peak signal-to-noise ratio (PSNR) which is most widely used term as a measure of quality of reconstruction of lossy compression by comparing the reconstructed signal with the original data. The PSNR equation can be expressed as follows:

$$PSNR = 10 \cdot \log_{10} \left( \frac{MAX^2}{MSE} \right) \quad \text{Eq. 4-5}$$

where MSE is the mean squared error,  $MSE = \frac{1}{n} \sum_{i=1}^n [D_{original}(i) - D_{reconstructed}(i)]^2$ , and MAX is the maximum output value which is 1023 for 10 bit ADC. The efficiency of DPCM depends on the maximum signal change between each sample, thus, on signal

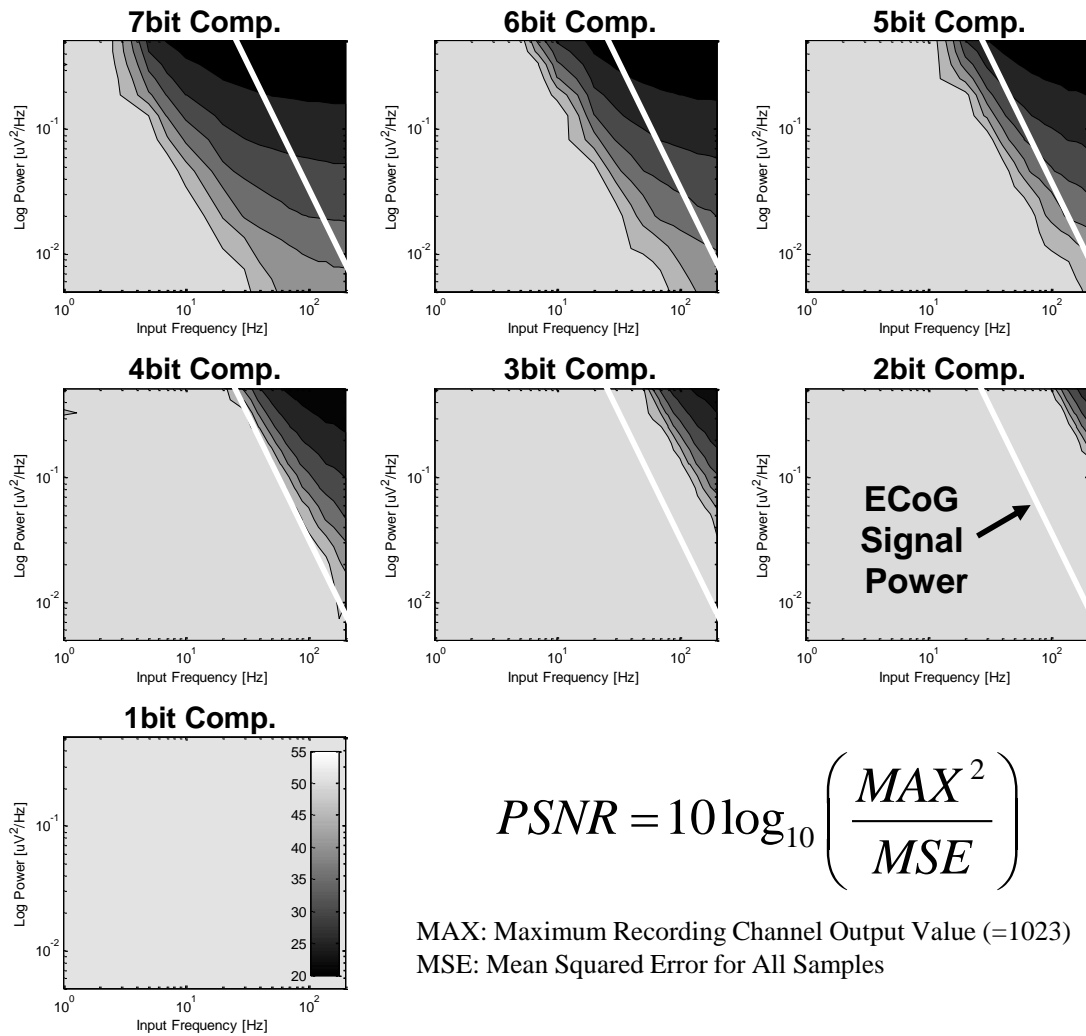


Figure 4-33: Measured PSNR for different compression factors from 1bit to 7bit compression compared with ECoG signal power.

amplitude and frequency. To verify the DPCM performance, DPCM data compression block has been tested with multiple amplitudes and frequencies under different DPCM resolution conditions. The measurement results are shown in Figure 4-33. The white slant line shows ECoG signal power. Compared to this ECoG signal power line to the PSNR, the reconstructed signal can be predicted how much the data is lost. If there is a no data loss, the PSNR will be infinite. A 6-dB attenuation of the PSNR indicates the effective loss of 1 bit resolution. Figure 4-33 shows the reconstructed signal has less than 6 dB attenuation down to 4bit compression. This means that the possible power reduction for

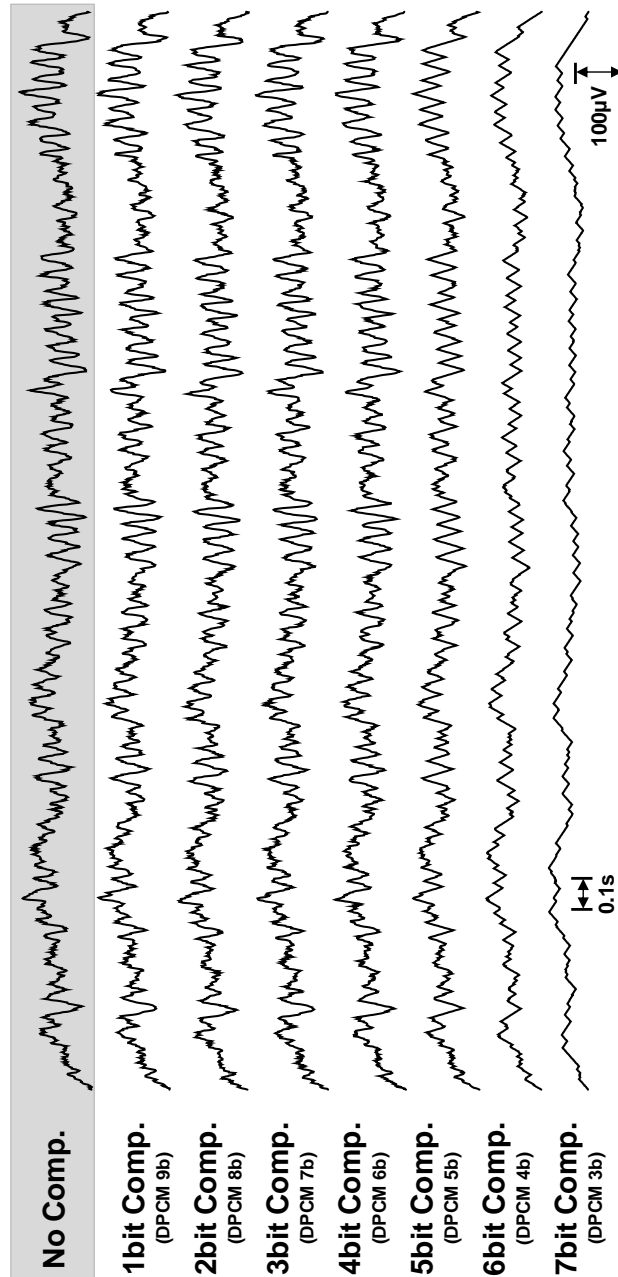


Figure 4-34: Measured ECoG signal waveforms with different compression factors

digital data path and wireless data link will be 40% with minor data loss less than 1 bit resolution. To test DPCM performance, the pre-recorded ECoG signal is amplified, digitized and compressed by the integrated preamplifier, ADC, and DPCM. The reconstructed signals from different compression factors are compared in Figure 4-34.



#### 4.6 Data Packet Generator with Parity Bit

In this section, as a wireless data transmission preparation block, the data packet generator will be explained. Because of the cyclic operation of the preamplifier, the sampling and conversion timing of the ADC will vary from channel to channel. And, digital outputs from each channel are available in the different moments as shown in Figure 4-3. Before the data packet generator, frame buffers are necessary to hold the digital output until all the channels output are ready to pack and transmit. Once all the channel's output are ready, the data stored in the frame buffers transferred to serialized buffer and data packet will be generated by appending a header, footer, and parity bit with the serialized data. To take an advantage of the data compression by DPCM block, all the frame buffer and serialized buffer size is adaptively programmable by the size of the DPCM resolution. This adaptive buffer size can reduce the power consumption further. The detailed schematics of frame buffer, serialized buffer, and parity bit shown in Figure 4-35(a), (b), and Figure 4-36(a), respectively. The packed serialized data configuration is shown in Figure 4-36(b). For example, by setting DPCM resolution to 5 bit, the number of the data to be transmitted decrease from 440 bits to 240 bits, which

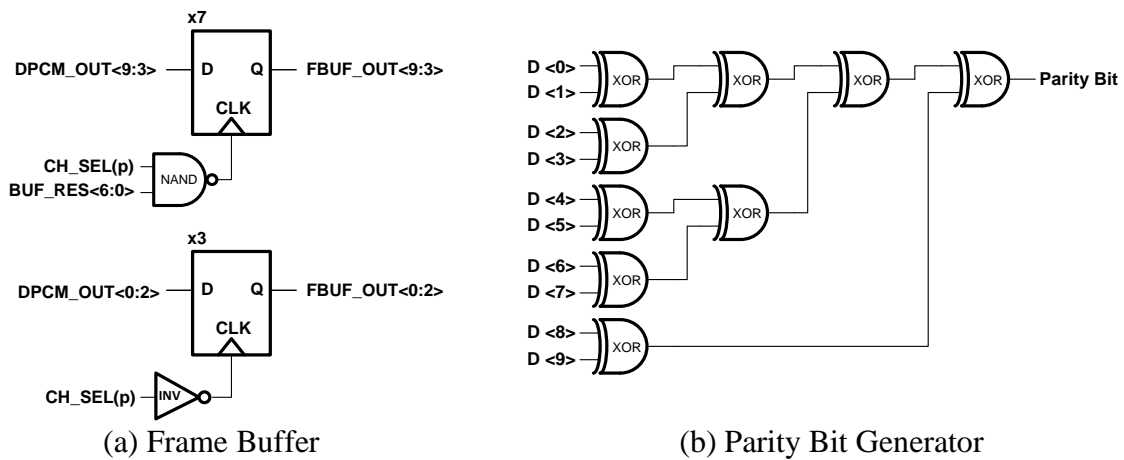


Figure 4-35: The schematics of (a) adaptive frame buffer and (b) parity bit generator

## Serialized Data Packet

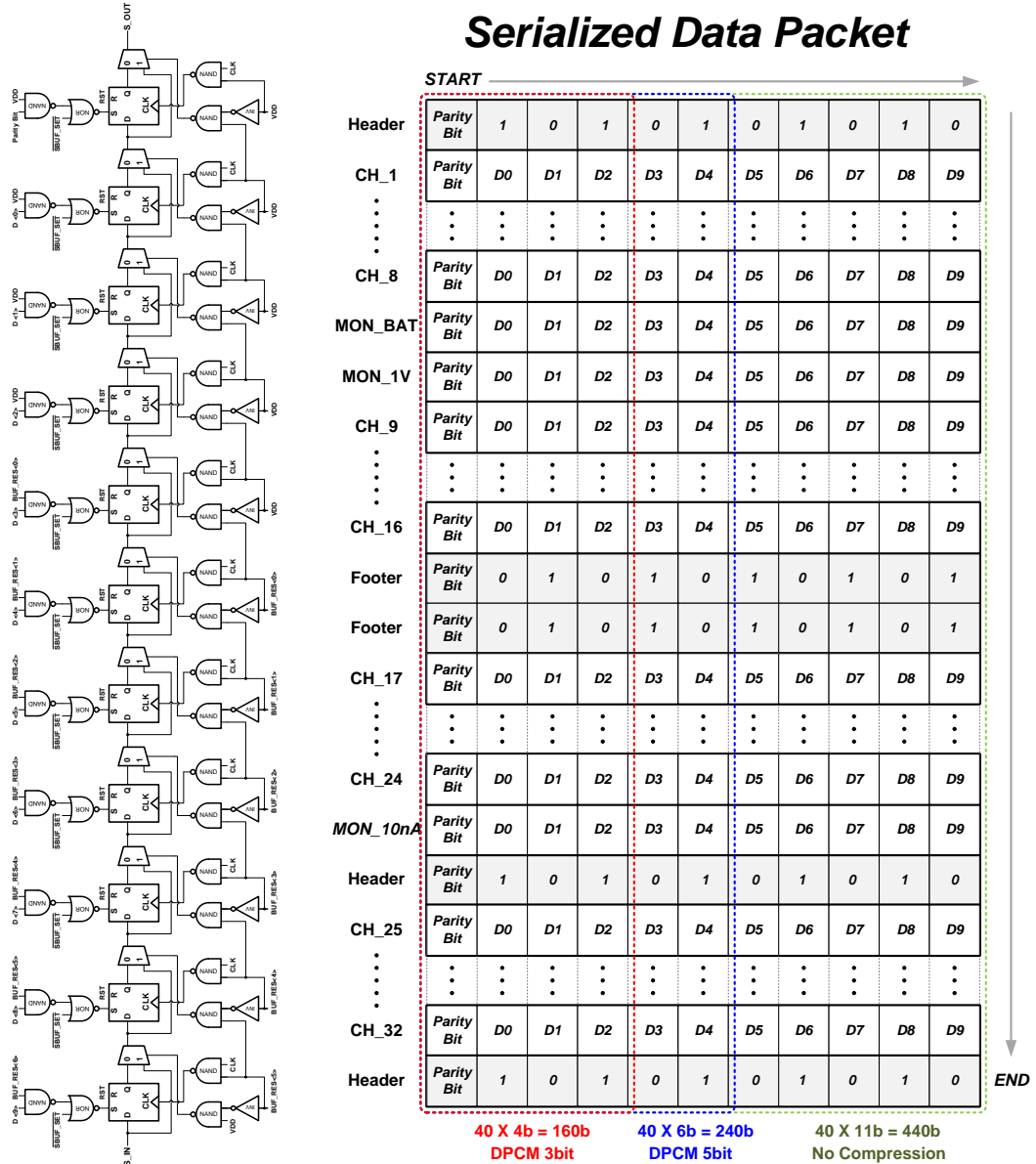


Figure 4-36: The Serialized Buffer with Adaptive Resolution and Serialized Data Packets

will result in about 40% power saving of the data packet generator as well as wireless transmitter.

### 4.7 Low-Power Wireless Data Transceiver (Tx/Rx) for Modular Expandability

After being digitized and compressed, the data from implanted devices needs to be transferred to external devices wirelessly to eliminate a transcutaneous connection. The

transmitted signal will be analyzed by external system, and the control signal generated based on the extracted feature from the signal will be transmitted back to implanted devices. Especially, multiple implantable devices, deployed to expand system modality and functionality, need to communicate with the external devices simultaneously, the neural interface integrated circuits is required to have a functionality of time or frequency multiplexing with a low-power wireless transmitter and receiver

In this section, a simple and low-power transmitter and receiver for the modular expandable closed-loop neural interfaces will be discussed.

#### **4.7.1 Communication Protocol for Modular Expandability**

In modular expandable closed-loop neural interface systems shown in Figure 4-1, recorded signals from multiple implanted devices will be transmitted simultaneously. In order to realize this simultaneous transmission, typically, there are two techniques; time-division multiplexing (TDM) and frequency division multiplexing (FDM). In FDM, different channels are modulated with different carrier frequency and transmitted all the time. For this FDM technique, in order to increase transmission speed without reducing accuracy or increasing bandwidth, the transmitter needs smooth pulse shaping filters, such as raised cosine filter, sinc filter, boxcare filter, and Gaussian filter, for spectral efficiency and no intersymbol interference. On the other hand, TDM channels occupy all frequency range by sharing the time. For a given time slot, only one channel is transmitted. Because TDM channel can occupy all frequency range, the transmitter can be implemented simply without pulse shaping filter and also low-power operation. However, in order for TDM to operate properly, global synchronization among implanted devices and external devices is essential. This global synchronization can be complicated

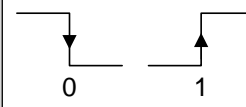
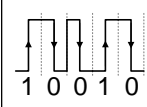
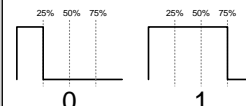


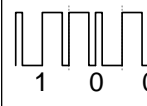
Modulation Type	Digital Value Definition	Example: '10010'	Features	Application
Manchester Modulation (IEEE802.3)			<ul style="list-style-type: none"> <li>+ Simple Tx</li> <li>+ Balanced Duty Cycle (Charge Balance)</li> <li>- Complicated Rx</li> </ul>	Implantable System Transmitter
Clock-Edge Modulator			<ul style="list-style-type: none"> <li>+ Simple Rx</li> <li>- Complicated Tx</li> <li>- Unbalanced Duty Cycle</li> </ul>	Industrial System Receiver
Manchester Clock-edge Modulation			<ul style="list-style-type: none"> <li>+ Simple Rx</li> <li>+ Balanced Duty Cycle (Charge Balance)</li> <li>- Complicated Tx</li> </ul>	Implantable System Receiver

Figure 4-37: Various Clock-Embedded Modulations

and consume comparable power. Fortunately, this complicated and power-hungry scheme can be implemented externally using external components, while allowing implanted devices to be implemented in simple structure and to consume less power in order to elongated lifetime of the system. For this reason, this work utilizes a time-division multiplexing technique to realize a modular expandable neural interface.

In this work, in order to implement simple structure and low-power operation, clock-embedded modulations among many modulation techniques, have been utilized. Especially, Manchester modulation and clock-edge modulation has been compared in the Figure 4-37. In Manchester modulation, data 0 and 1 is encoded as a negative or positive edge (IEEE 802.3). This encoder and transmitter can be simply realized using exclusive OR gate and current source and sink as shown in Chapter 3. Also, because both 0 and 1 has 50% duty cycle, the overall signal has balance duty cycle which is important for biomedical implanted devices to avoid charge accumulation in the body. However, contrary to the transmitter, the clock data recovery circuit is complicated to implement

and consumes relatively high power. So, this method will be suitable for implantable transmitter architecture. Another modulation is a clock-edge modulation (CEM). In this CEM, data 0 and 1 are modulated to have different duty cycles; 25% for 0 and 75% for 1. A clock and data recovery circuit to demodulate CEM can be implemented using simple PLL [109]. Compared to Manchester modulation transmitter, the transmitter for CEM is relatively complicated. Because of the unbalanced duty cycle, CEM modulation may cause accumulation of the charge inside body. From these feature, this method is not suitable for implantable devices but suitable for industrial receiver applications, such as HDMI. By taking advantages from each method, this work proposes a Manchester clock-edge modulation (MCEM) as shown in Figure 4-37. This scheme is suitable for implantable receiver because of its simple demodulation architecture and charge balance characteristic. Possible drawbacks, such as a reduced data rate thus power consumption and complicated control circuit of transmitter, can be compensated by a high-performance external transmitter while minimizing system complexity and power consumption of implantable receiver. From the above analysis, this work utilizes a Manchester modulation for transmitter implementation and a Manchester clock-edge modulation for receiver implementation.

In the wireless link, there are many ways to transmit and receive the signal wirelessly such as RF, inductive coupling, capacitive coupling, and Galvanic coupling (ISCOM). In this work, we utilized a capacitive coupling and galvanic coupling for their simplicity and low-power operation. For data transmission, galvanic coupling and capacitive coupling can be utilized based on the requirement such as power, transmission distance, and align. For data reception, capacitive coupling is utilized to minimize channel interference.

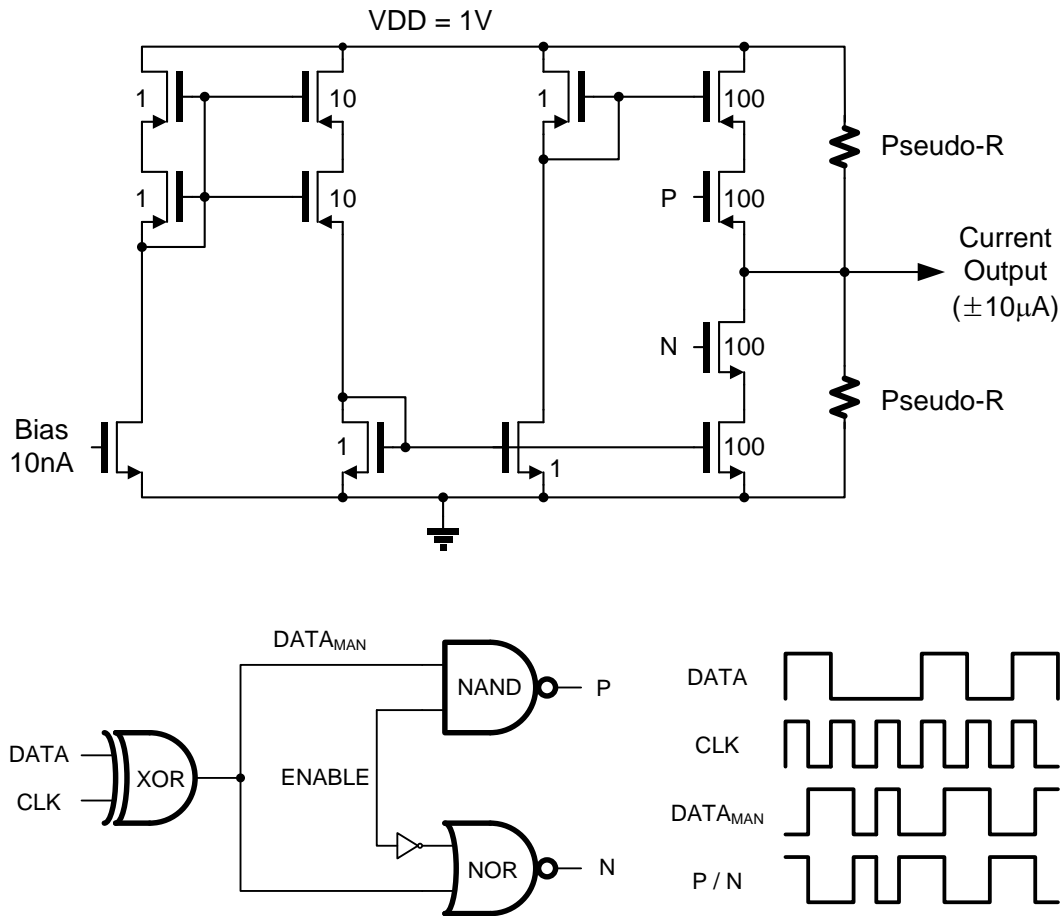


Figure 4-38: Dual-Mode Transmitter and Control Block with Manchester Encoder

#### 4.7.2 Dual-Mode Transmitter (Tx) and Control Block

In this section, low-power dual-mode transmitter for galvanic coupling and capacitive coupling will be presented. Interestingly, the transmitter for both coupling modes can be implemented current source and sink as shown in the Figure 4-38. The transmitter has a class B type output stage with  $10\mu\text{A}$  current driving capability. In the galvanic coupling configuration with a series capacitor ( $10\text{pF}$ ), the output stage can source and sink the electrode with  $10\mu\text{A}$ . And, in the capacitive coupling configuration, this output stage operates as a class B inverter. The output node of the transmitter is weakly biased to half power supply by two pseudo resistors. The control block converts input DATA into

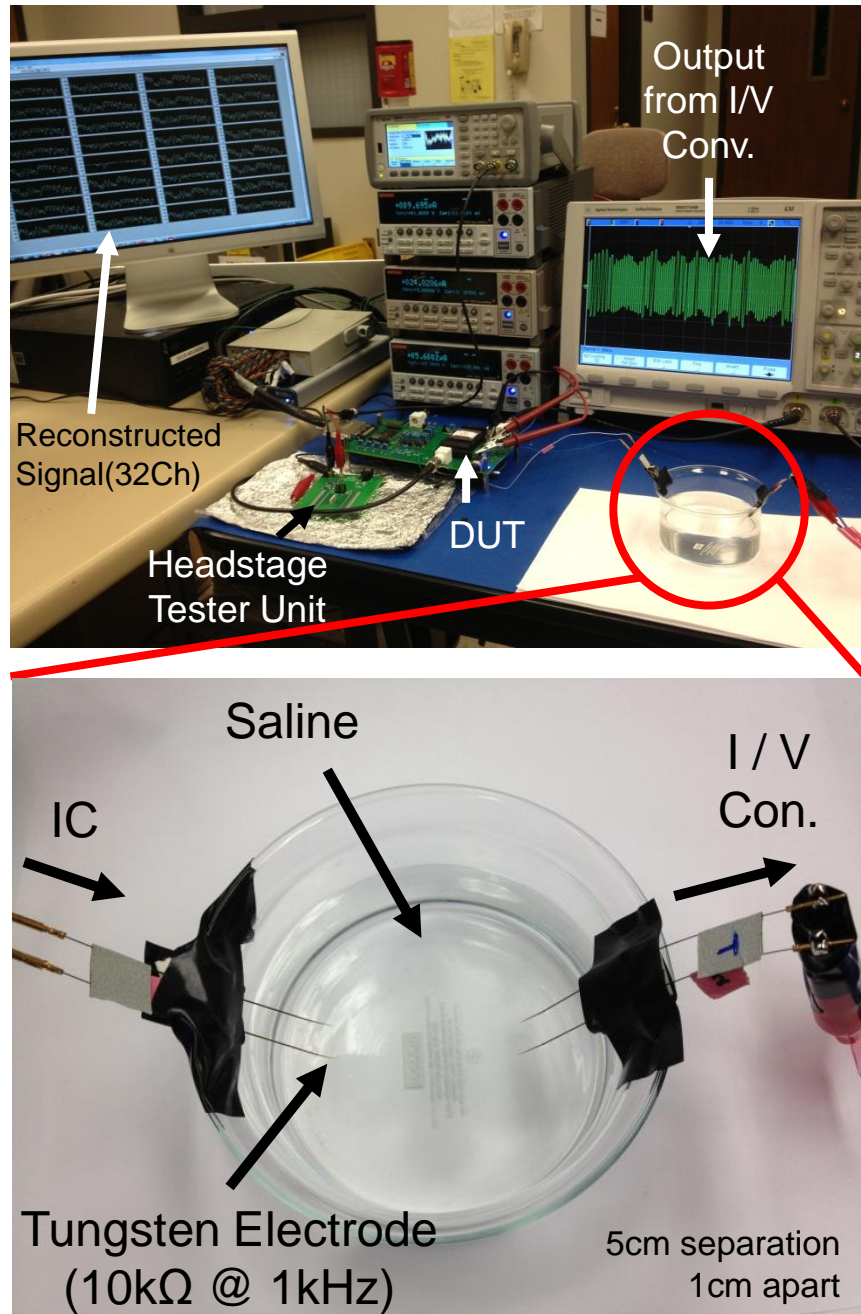


Figure 4-39: Galvanic Coupling (ISCOOM) Test Setup

Manchester Code ( $DATA_{MAN}$ ) and generates the P and N signals. During the disable period, the output node will be disconnected from source and sink, thus in high impedance mode. The galvanic coupling test setup is shown in Figure 4-39. For testing, a series capacitor of 10pF has been connected between the output of the transmitter and

electrode to de-couple the dc levels of the transmitter and saline. As an electrode, Tungsten electrodes with impedance of 10k have been used. The gap between active and ground electrodes is 1 cm apart, and distance between electrodes pairs is 5 cm.

#### 4.7.2.1 Measurement Results

To demonstrate the galvanic coupling data transmission, the pre-recorded signal is generated by function generator and applied to the headstage tester unit board which is

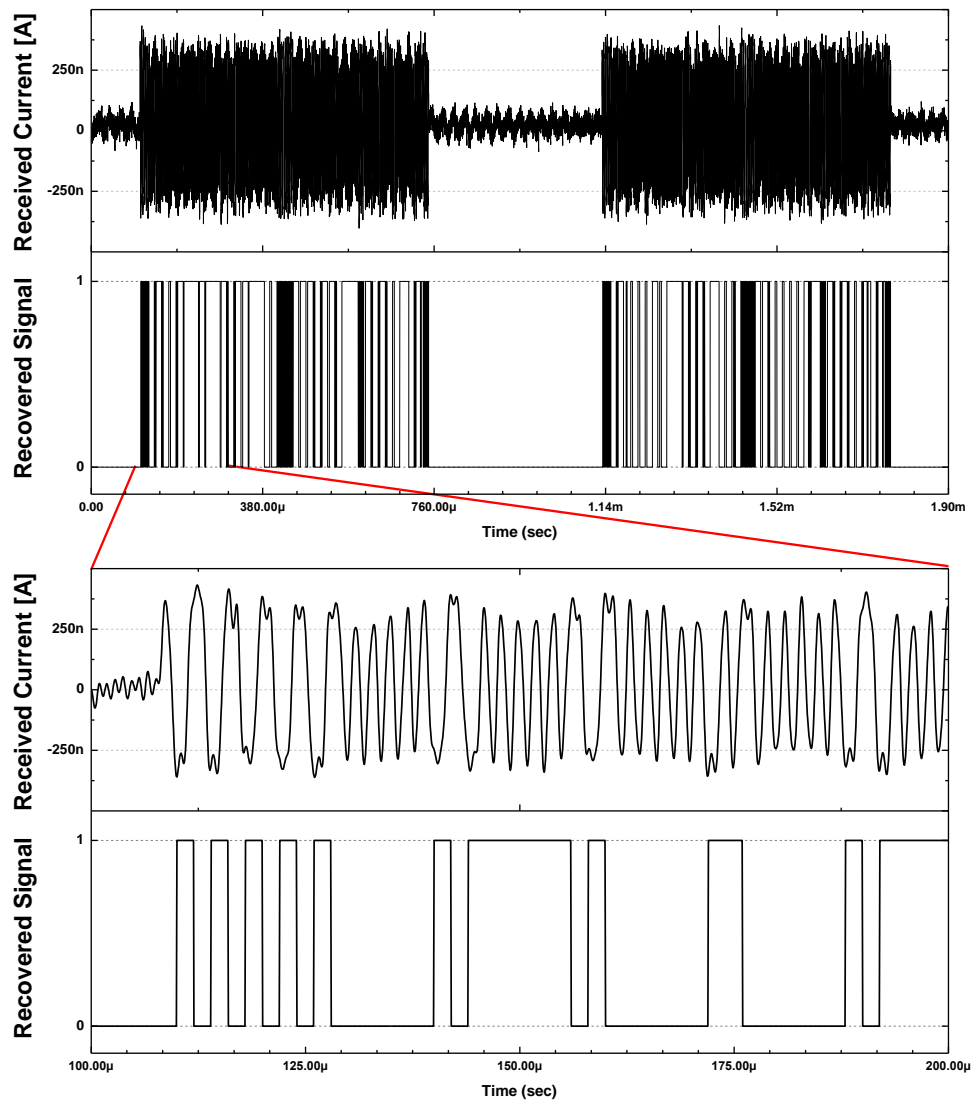


Figure 4-40: Measured Galvanic Coupling (ISCOM) Transmitted Signal and Recovered Signal



generally used to verify the functionality of the commercially available headstage from Plexon. And, the output from the headstage tester unit is applied to the fabricated neural interface IC. After the signal amplified and digitized, the signal is transmitted to the transmitting side electrodes pair by galvanic coupling preamplifier. The receiver side electrodes pair is connected an external I/V converter and the converted signal in voltage domain is connected to DAQ board and the recovered ECoG signals are shown in the monitor screen. And, the measured transmitted signal and recovered signals are shown in Figure 4-40. The wireless channel attenuation at saline is -17dB. The measured power consumption for 440kbit/sec is 6.62  $\mu$ W including control and bias circuit. The power consumption per bit is 15pJ/bit. By enabling DPCM 4bit reduction, the reduced power consumption is 4.64  $\mu$ W for 240kbit/sec which shows effectively 10.5pJ/bit power consumption per bit. Figure 4-41 shows the measured eye diagram of the transmitted signal. The measured BER is less than  $10^{-8}$ .

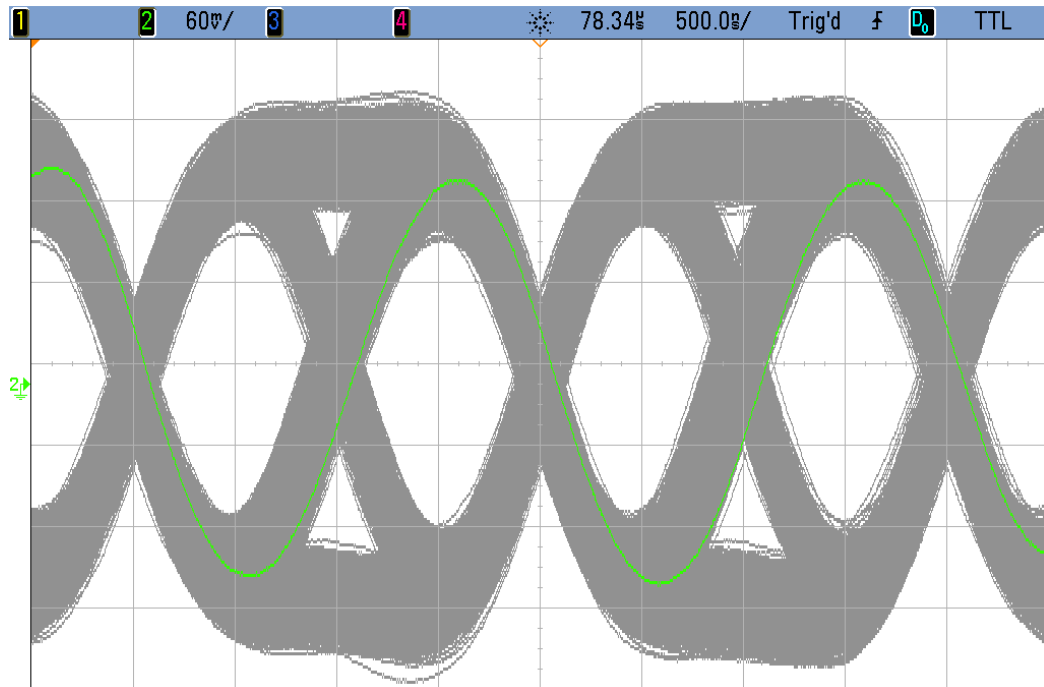


Figure 4-41: Measured Eye Diagram for transmitted signal using Galvanic Coupling

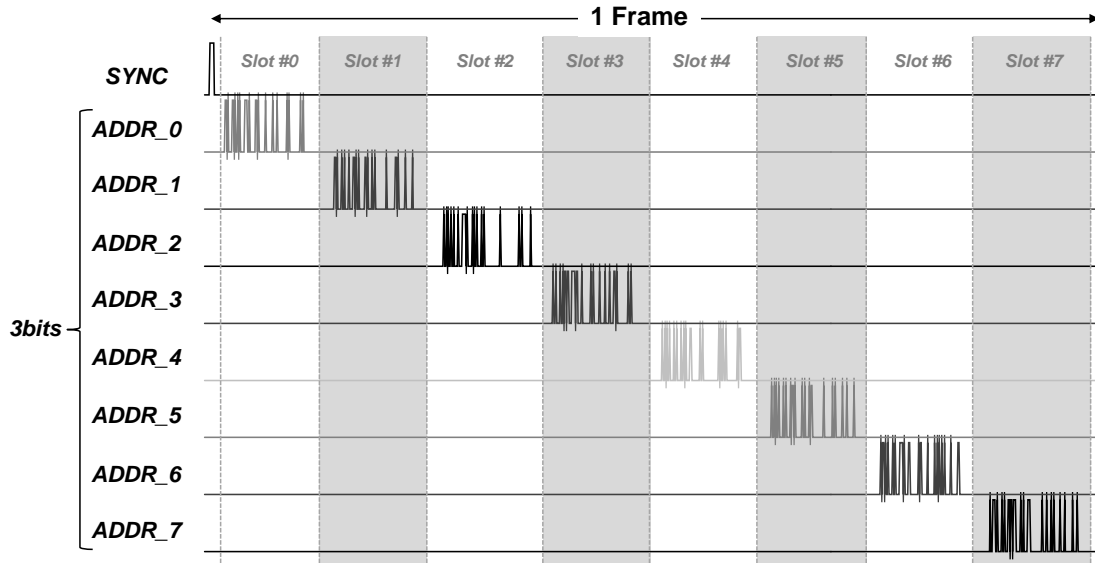


Figure 4-42: Measured Transmitted Signal with different address settings. Up to 8 devices can be shared the time division with 3bit address settings.

Figure 4-42 shows measured transmitted signal with different address settings. With 3bit address settings, up to 8 devices can be shared the time division.

#### 4.7.3 Capacitive Coupling Receiver (Rx)

Figure 4-43 shows the schematic of implemented capacitive coupling receiver. The MCEM signal is applied to series capacitor (100nF) and the data slicer circuit senses the average value to restore binary logic levels. Also, the pseudo resistors are used to set the comparators input dc level.

#### 4.8 Clock Data Recovery Block for Manchester-CEM (MCEM) Signal

As mentioned in the previous section, a simple and effective clock and data recovery circuit has been utilized [109]. This PLL based clock and data recovery circuit is shown in Figure 4-44. The PLL circuit locks the frequency and phase of recovered clock, CLKR with MCEM\_IN. And the recovered clock can be applied to DFF with MCEM\_IN to restore control parameters.

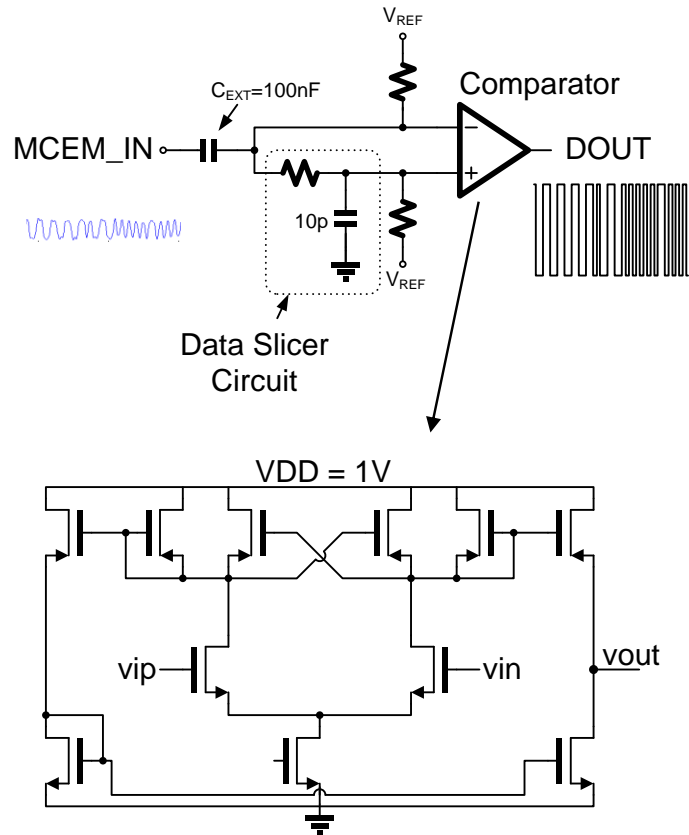


Figure 4-43: Capacitive Coupling Receiver Schematic

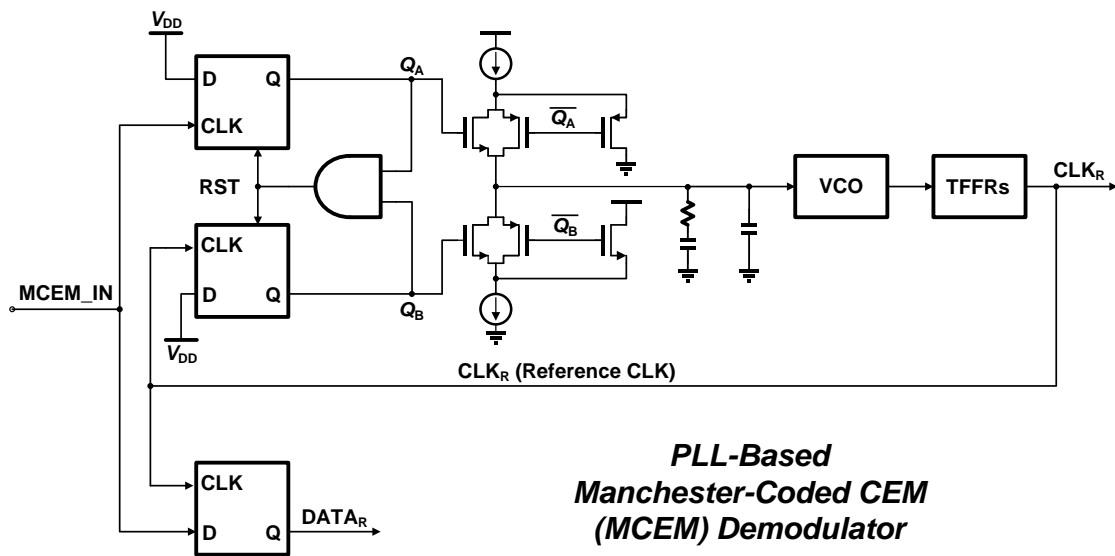


Figure 4-44: PLL Based Manchester-Coded CEM demodulator

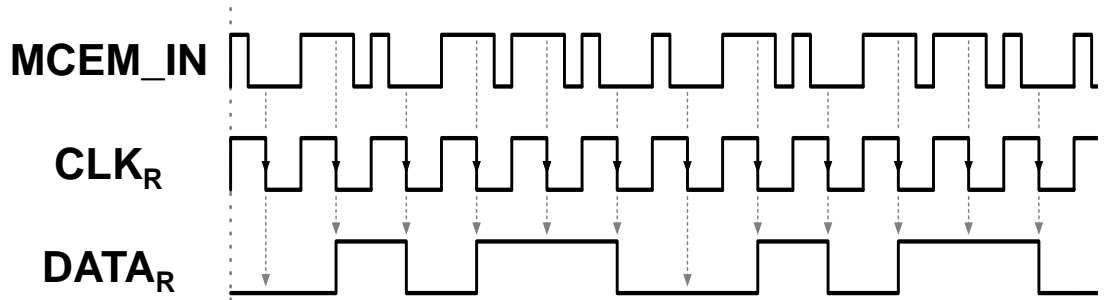


Figure 4-45: MCEM Demodulator Timing Diagram

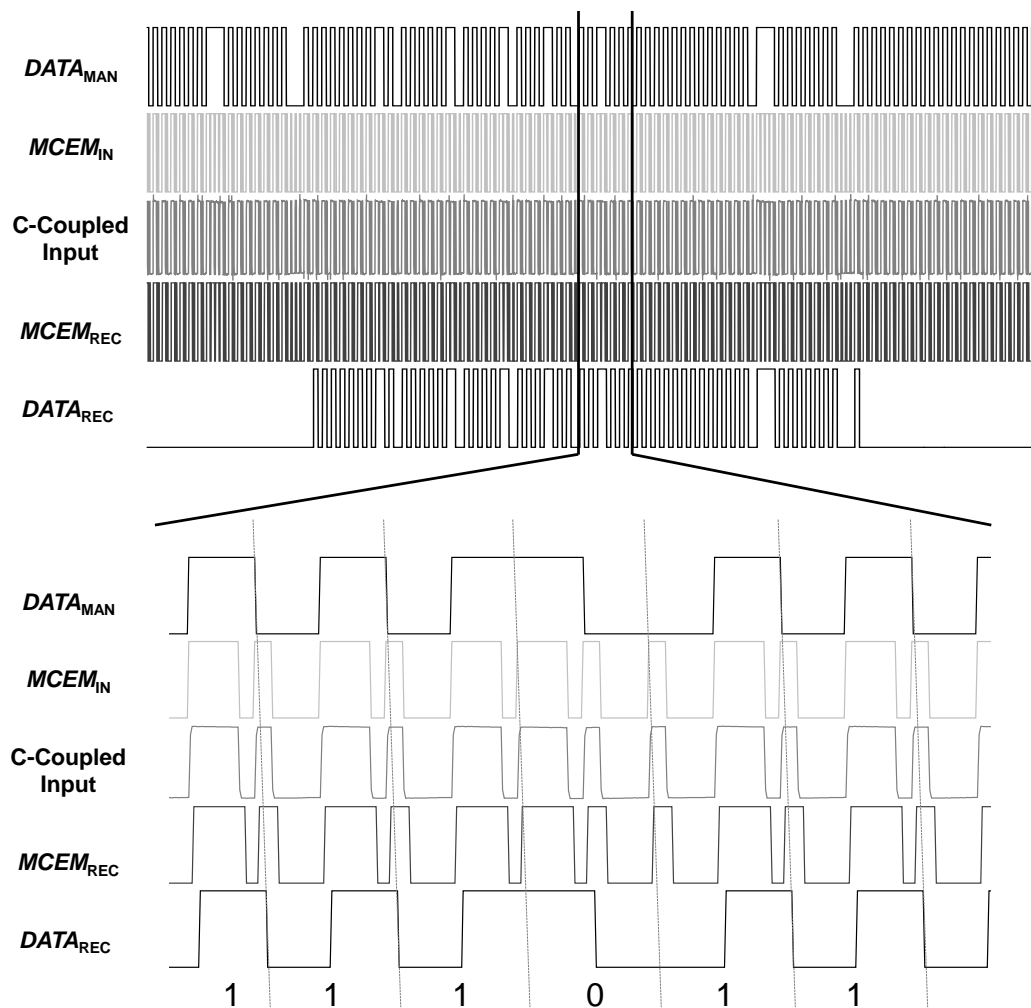


Figure 4-46: Measured Recovered Data by Capacitive-coupling Rx and CDR

As shown in Figure 4-45, the PLL controls the output clock, **CLK<sub>R</sub>**, in order to align the frequency and phase with the **MCEM\_IN** signal as a reference frequency. So, positive

edges of  $CLK_R$  will be locked with those of  $MCEM\_IN$ . Because data encoded with  $MCEM$  has different duty cycle, we can store the  $MCEM\_IN$  value at the moment of negative edges. And, by extracting only the data at even numbers in sequence, we can complete the clock and data recovery out of  $MCEM\_IN$  signal. The measurement results are shown in Figure 4-46. To demonstrate, the  $DATA_{MAN}$  and  $MCEM_{IN}$  signal are generated using PC and transmitted through a capacitive-coupling receiver.  $MCEM_{REC}$  shows the recovered  $MCEM_{IN}$  signal after Rx. Then, the recovered signal is applied to CDR circuit and the extracted parameters are shown in the last row of the graph. Also, by placing multiple flip-flops inside the loop, we can easily get the multiple clock signals which has a higher frequency than  $MCEM\_IN$ .

One concern to recover Manchester coded signals is that a phase of the input signal is critical to determine the polarity of the signal. In other word, if the phase is shifted  $180^\circ$  then '0' becomes '1' and vice versa. To prevent this issue, in the data stream, we put a header of '011110' and footer of '100001'. Once these header and footer are detected by CDR circuit, it will start storing the data into internal registers.

Another concerns for expandable modularity of the system, each individual implanted devices need to be programmed either globally together or individually. To realize this feature, between the header and footer section, the control data stream also includes implantable device ID address which can be programmed using hard wire connection. To control all the devices simultaneously, global selection is sets to high. On the other hand, for individual controllability,  $BB\_ADD$  bit can be set for target address by disabling global selection. In order to shorten the response time to transmit the control signals to the devices based on the extracted feature (overall less than 5ms), the control signals are

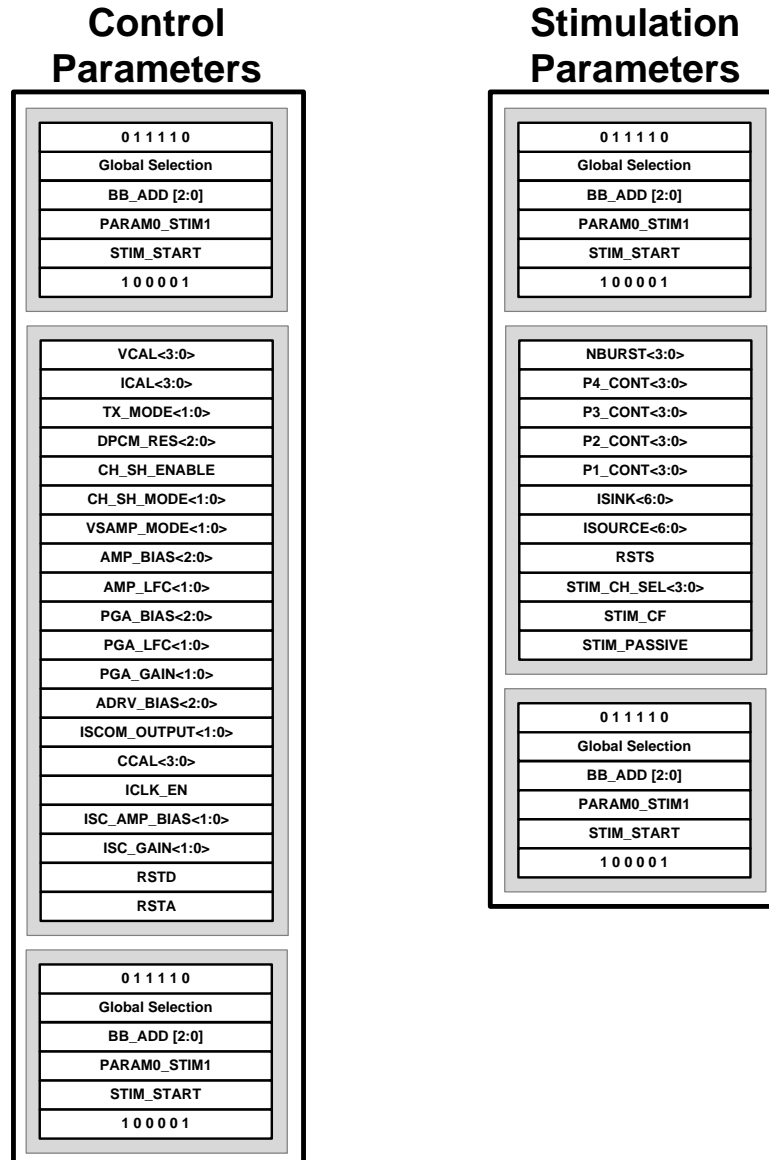


Figure 4-47: The detailed Configuration of Control and Stimulation Parameters

divided into ‘control parameters’ and ‘stimulation parameters’. Control parameters includes general parameters for each individual blocks such as cyclic operation, TDM mode setting, DPCM resolution, ADC sampling frequency, various bias condition for preamplifier and other sub-blocks, and reset signals which will act as an synchronization signal for time division multiplexing system. In these stimulation parameters, it includes various parameters to set the stimulation waveform generator including current output,

duration of the waveforms, cathode and anode selection, stimulation channel selection, and reset. The detail configuration is shown in Figure 4-47. For the stimulation start timing, we can set STIM\_START signal.

#### 4.9 Fully-Programmable Stimulation Block

ECoG neural signals are recorded, digitized, and transmitted to external digital processing units. Once expected features are extracted, the external DSP unit will generate control parameters and transmit it back to the proposed unit using wireless capacitive coupling method. The transmitted signal is recovered by CDR circuit, then, feature-specific stimulation waveforms for integrated current stimulators are generated based on the control signals by stimulation waveform generator. This section will present the stimulation waveform generator and integrated current stimulation

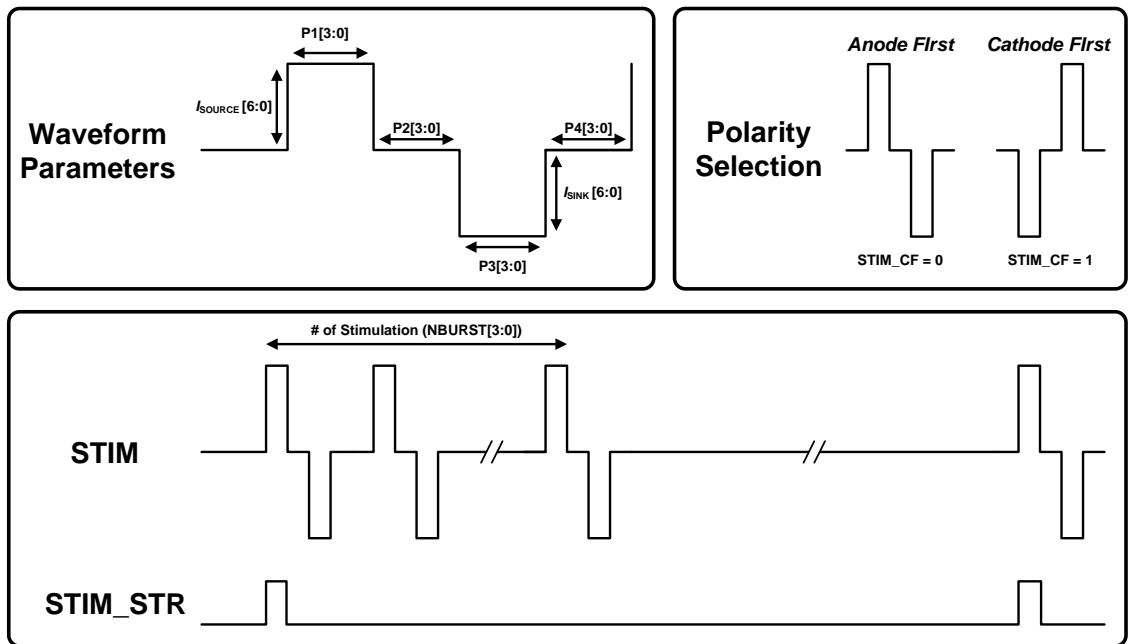


Figure 4-48: Programmability of Stimulation Waveform

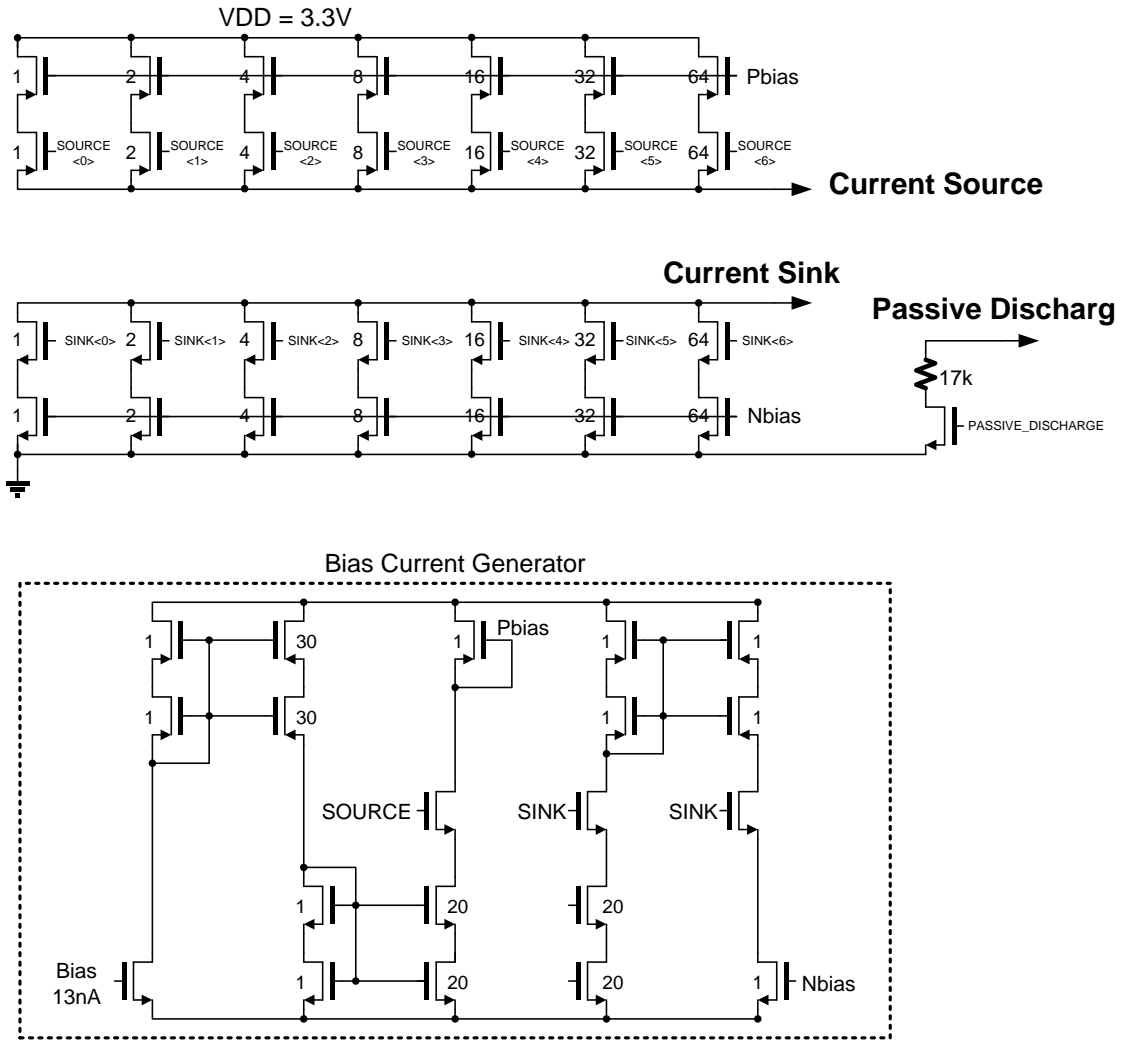


Figure 4-49: Schematic of Integrated Stimulator

As shown in Figure 4-48, the stimulation waveform can be fully programmable based on the application, feature, and subjects. With this functionality, the most optimized stimulation parameters can be investigated and eventually helps to reduce the overall system power consumption. For this purpose, the durations of each phase can be controlled from  $1\ \mu s$  to 32.8ms with 4bit control. The current output can be controllable from  $8\ \mu A$  to 10mA. Also, the stimulation polarity can be selectable from anode first and cathode first. We can set the number of stimulation pulses as a burst mode. This means



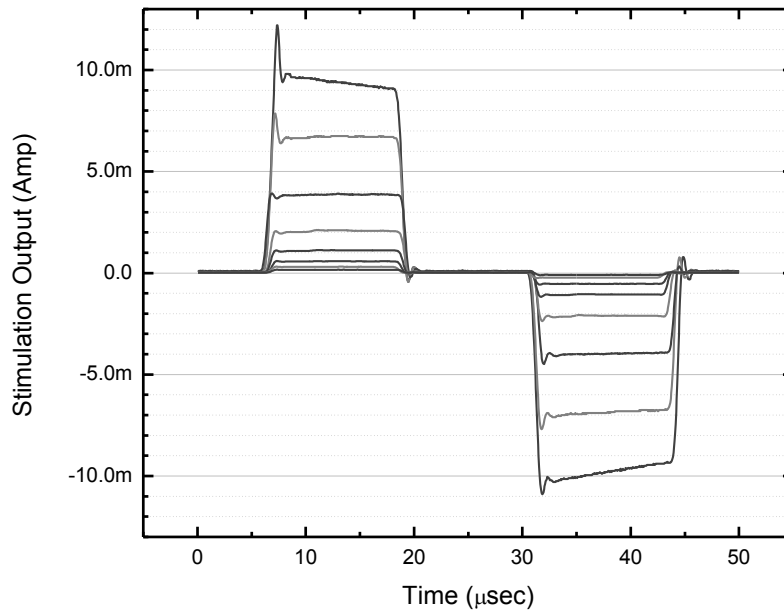


Figure 4-50: Measured Stimulation Current Output

with one stimulation start pulse signal, we can stimulate multiple pulses from 1 to 16385 as shown in Figure 4-48. Figure 4-49 shows the schematics of the integrated stimulator with bias current generator and passive discharge path. The stimulator consists of a current sink and source with programmable aspect ratio to change the output current. Due to the limited voltage compliance provided by the fabrication process, the output nodes of current sink and source are not connected inside the chip. This can help us to connect the output nodes to external current driver with higher power compliance for higher current output capability.

Measured stimulation current output with different current setting is shown in Figure 4-50 and maximum possible stimulation current output with different load impedance is shown in Figure 4-51. For typical impedance of ECoG electrode with 1mm in diameter is around 1~3 k $\Omega$  at 1 kHz. With this load condition, we can expect up to 1mA stimulation current output under 3.3V power supply. For higher current output, either we can use a

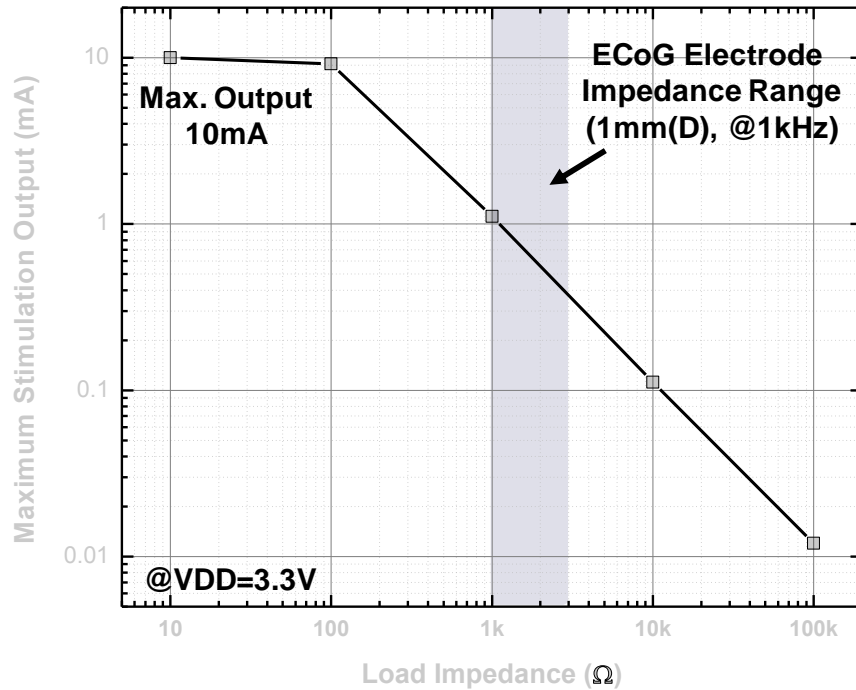


Figure 4-51: Maximum Stimulation Current Output with Different Load Impedance

larger electrode to reduce the impedance or we can utilize external ICs as mentioned earlier.

#### 4.10 Summary

The proposed neural interface IC is fabricated using TSMC 0.18 $\mu$ m 1P6M CMOS technology. The microphotograph of the fabricated IC is shown in Figure 4-52. The overall chip area is 2.4 x 2.4 mm<sup>2</sup> for the active area of the system. The overall power consumption for TDM=8 and DPCM=6bit is 19.5 $\mu$ W. The overall power consumption for the different power-saving techniques have been compared in Figure 4-53. With the cyclic operation and DPCM with ISCOM (Galvanic coupling), we can achieve about 50% power reduction from 41 $\mu$ W to 19.5 $\mu$ W. Detailed power consumption for each key blocks are also shown in the bottom table of Figure 4-53. The measured overall IC characteristics of the proposed system are summarized in Table 4-4.

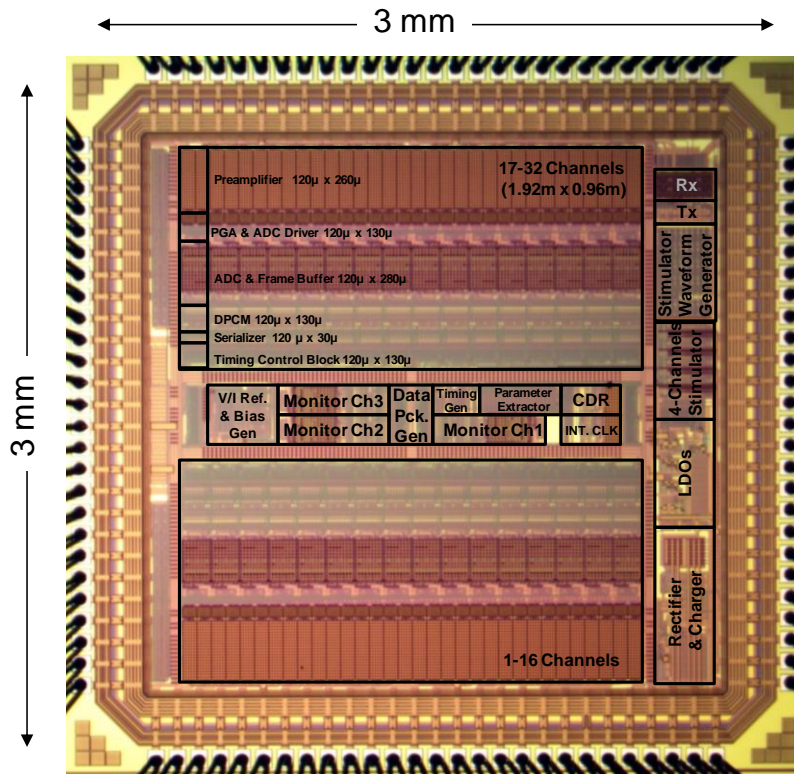


Figure 4-52: The Microphotograph of the Fabricated IC

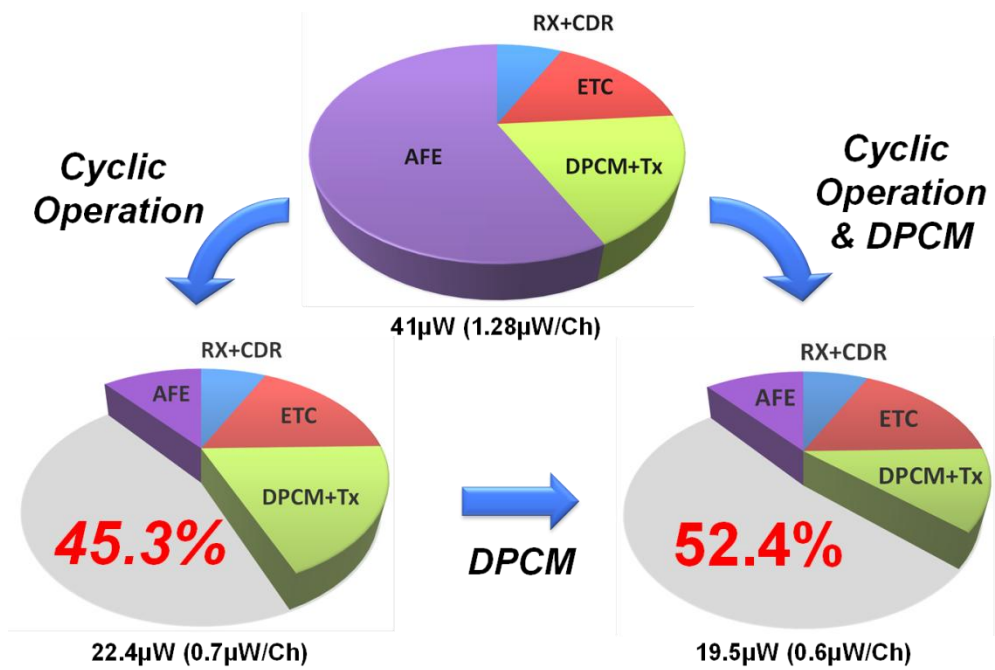


Figure 4-53: Power Consumption Comparison Chart

Table 4-4: Measured Characteristics of the Proposed System.

<b>Measured Performance Characteristics</b>	
<b>Technology</b>	<b>0.18 <math>\mu</math>m CMOS</b>
<b>Number of Recording Channel</b>	<b>32</b>
<b>Modularity</b>	<b>up to 8</b>
<b>Supply Voltage</b>	<b>1V (Analog) / 0.5V (Digital)</b>
<b>Power Consumption / Channel (Excluding Stimulation Block)</b>	<b>600 nW</b>
<b>Overall Amplification Factor</b>	<b>40 / 46 / 54 / 58 dB</b>
<b>Preamplifier Bandwidth</b>	<b>500 Hz</b>
<b>System Input Referred Noise (0.1 ~ 1kHz)</b>	<b>3.26 <math>\mu</math>V<sub>RMS</sub></b>
<b>Input Voltage Range</b>	<b>1.2 mV</b>
<b>CMRR / PSRR</b>	<b>&gt;60dB / &gt; 50 dB</b>
<b>Channel Isolation</b>	<b>&gt; 50 dB</b>
<b>ADC Sampling Frequency</b>	<b>1 kS/s</b>
<b>ENOB (for Av=500, 5<math>\mu</math>Vrms noise)</b>	<b>7.3</b>
<b>Wireless Coupling Method</b>	<b>Capacitive / Galvanic</b>
<b>Wireless Data Bandwidth</b>	<b>&lt; 440k</b>
<b>Bit Error Rate</b>	<b>&lt; 10<sup>-8</sup></b>
<b>Modulation</b>	<b>MCEM</b>
<b>Number of Stimulation Channel</b>	<b>4</b>
<b>Programmable Stimulation Current Output</b>	<b>&gt; 100 <math>\mu</math>A</b>

#### 4.11 *In-Vitro* Measurement

To verify the proposed ENI-32 system, in-vitro measurement is performed as shown in Figure 4-54. The headstage tester unit from Plexon, which is widely used to test a commercially available headstages, has a passive breakout board with output impedance

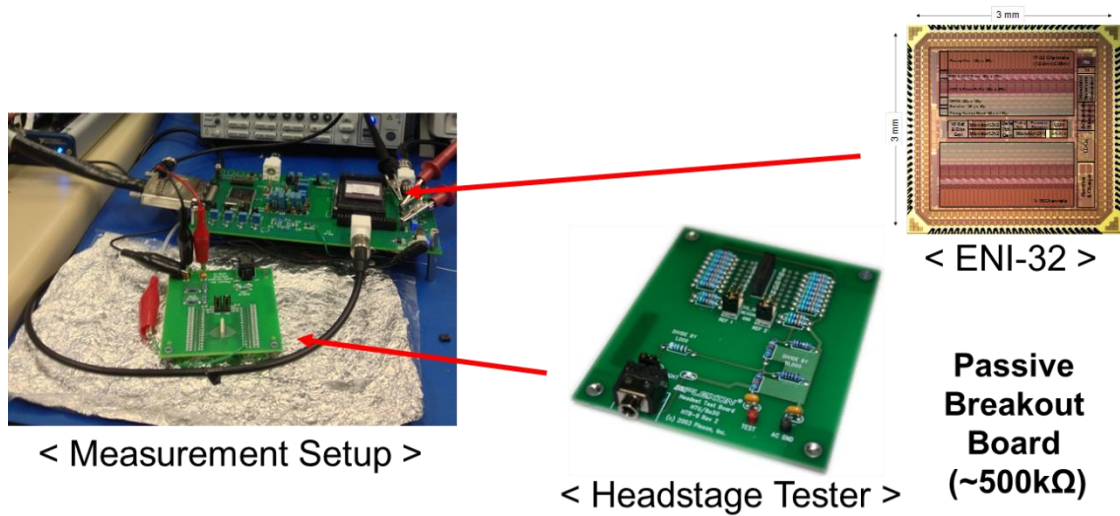


Figure 4-54: *In-Vitro* Measurement Setup

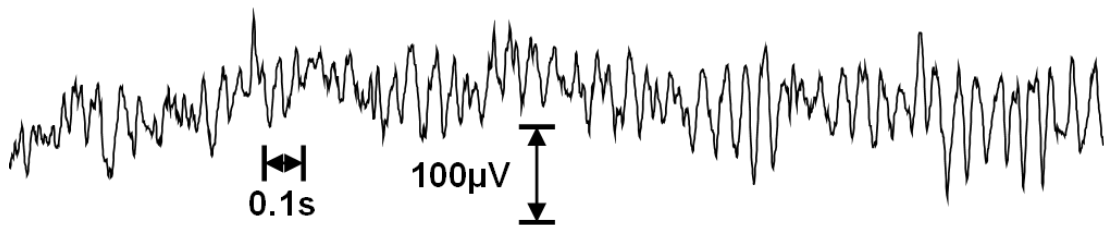


Figure 4-55: Recorded ECoG Signal from *In-Vitro* Measurement Setup

of  $500\text{k}\Omega$  to imitate an electrode-tissue interface. The pre-recorded signal is applied to tester unit and divided passively down to the actual signal amplitude by headstage tester unit. The recorded signal from this measurement setup is shown in Figure 4-55. From this measurement, the proposed ENI-32 is verified to be robust and shows a good immunity for the external interferences such as 60 Hz power line noise.

#### 4.12 Conclusion

As a closed-loop system, ENI-32 focuses on optimizing the power performance based on a bio-signal property and integrating stimulator. ENI-32 is fabricated in  $0.18\ \mu\text{m}$  CMO process and has thirty-two recording channels and four stimulation channels with a cyclic

preamplifier, data compression, asymmetric wireless transceiver (Tx/Rx). The measured channel power, noise and area are 140nW (680nW including ISCOM),  $3.26\mu\text{V}_{\text{RMS}}$  (NEF=1.6), and  $5.76\text{mm}^2$ , respectively. The ENI-32 achieves an order of magnitude power reduction while maintaining the system performance. The proposed nano-watt ENI-32 can be the first practical wireless closed-loop solution with a practically miniaturized implantable device thanks to the low-power operation (small battery) and ISCOM (no need of RF antenna and inductor). In addition, even though the techniques presented in this work are optimized for the ECoG signal, all the techniques can also be applied to other sensing modality such as EEG and action potentials with a bandwidth modification.

## CHAPTER 5

### CONCLUSIONS, CONTRIBUTIONS, AND FUTUREWORKS

Interfacing with neurons enables us to understand how the brain works and help people who are suffering from neurological disease and any other disabilities. The technical challenge for the successful realization of the proposed system is to acquire the performance required within utmost constraints brought by small size, low-power, low-noise, and minimal invasiveness of the system. This work presents three ECoG neural interfaces toward low-power wireless implantable neural interface for closed-loop ECoG system with recording and stimulation capability. This work demonstrates the first trial of Bio-Signal driven system power optimization method such as bandwidth optimization and DPCM. The proposed system realized a significant system power reduction of  $> 50\%$  while maintaining noise and system performance. Also, In-vivo and in-vitro measurement have been tested

Thesis Contributions

To achieve aims above, the proposed neural interface system has introduced the following contributions/innovations as follows:

- *Integrated circuit optimization for epidural/subdural Electrocorticogram:* In this work, we developed wireless modular neural interface circuit optimized for ECoG.
- *Power-noise optimization based on the ECoG signal driven analysis:* Based on the analysis driven by the ECoG signal characteristics, the required bandwidth for signal

path and data compression technique (DPCM) have been proposed and implemented for elongated lifetime of the system.

- *Power-efficient data compression:* To reduce a data bandwidth for wireless data transfer, this work presents a lossy but effective data compression technique ECoG signal.
- *Manchester clock-edge modulation based clock and data recovery circuit:* this work utilizes clock-edge modulation for Manchester-encoded CEM signal due to its simple structure and low-power operation.
- *Verification of wireless data communication through the skin:* to transmit the data wirelessly, capacitive coupling and galvanic coupling (ISCOM) have been implemented and tested. These methods have technical benefits such as: (i) low-power consumption, (ii) low noise and interference, and (iii) no antennas or coils required for miniaturized implantable system.
- *Implementation of integrated stimulator with fully programmable waveform:* because the effect of the stimulation varies for subjects and applications, in this work, fully programmable waveform generator is implemented for integrated stimulator.
- *Integration of peripheral circuits:* To minimize the system volume, all the peripheral circuits such as reference/bias generator, clock generator, and LDOs have been implemented on the same silicon substrate.
- *Modular expandable sensor system:* The modular system can be expanded to cover wide spread area of the brain and also to be capable of sensing various biopotentials such as temperature and pressure using multiple implantable devices.



- *System miniaturization:* in order to demonstrate the miniaturized system, we also implemented a miniaturized package with the first version of the IC in chapter 2.
- *System verification with in-vivo and in-vitro measurement:* fabricated neural interface circuits are verified by measuring in-vivo animal ECoG signals or in-vitro head-stages tester unit.

### **5.1 Suggestions for Future Work**

In this work, we introduced the nano-watt modular integrated circuit for wireless neural interface. For further investigation and future work the following research topics are suggested

- **Successive Approximation Register ADC Performance Improvement:** To increase system performance, the SAR ADC needs to be improved by using a calibration techniques which is widely used techniques for a high resolution SAR ADC over 8 bits.
- **Noise Performance Improvement:**  $1/f$  noise power is the dominant noise source among the noise components in the system. In order to enhance the noise performance,  $1/f$  noise reduction using chopper or switching bias technique can be utilized and integrated in the system.
- **Chronic In-Vivo Recording and Stimulation Test with Modular Implantable Device:** in order to implement a practical system, the proposed system needs to be tested and verified with chronic in-vivo condition.
- **Hermetic Sealed Assembly and Package:** Another critical issue for chronic and practical device is a hermetic sealing which will determine the actual life time of the

system. To solve this issue, a hermetically sealed package and assembly techniques should be realized.

- **Implantable Power Solution:** for the implantable neural interface, the implantable battery, inductive coupled power transfer with or without rechargeable battery, and energy harvesting will be good candidates. However, there is much room to improve to be applied to the practical neural interface system.
- **Flexible Expandable ECoG Electrode:** as a transducer from ion information to electrical information, the electrode takes a critical role in the neural interface system. Especially, in the surface recording application, the flexibility of the electrode is critical to provide a stable and reliable contact with the brain. Also, the electrode and tissue interface requires some charge exchange and this process can degrade the quality of the recording.
- **Way-Station with Programmable Feature Extraction Algorithms:** as we discussed in Chapter 1, we need a way station as an external digital signal processor. To complete the conceptual system, the way station needs to be implemented.

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