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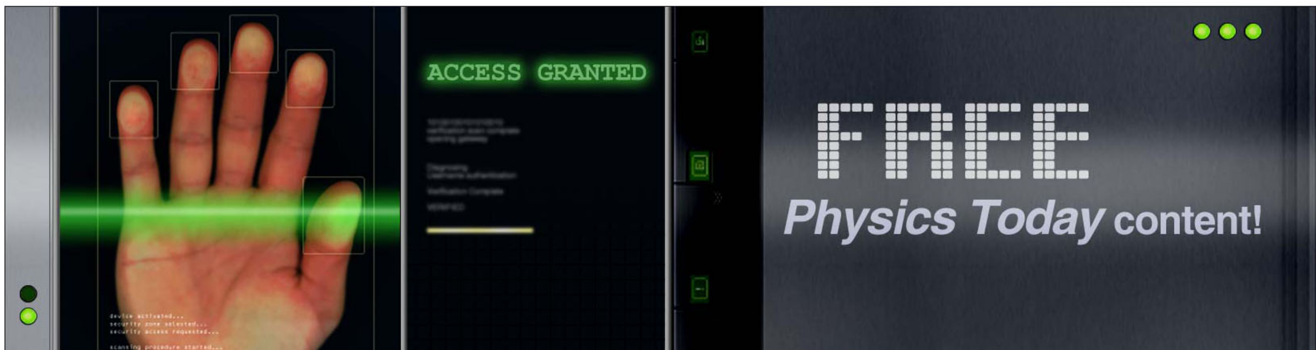

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Barrier height of Pt–$In_xGa_{1-x}N$ ($0 \le x \le 0.5$) nanowire Schottky diodes

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The barrier height of Schottky diodes made on $In_xGa_{1-x}N$ nanowires have been determined from capacitance-voltage measurements. The nanowires were grown undoped on n-type (001) silicon substrates by plasma-assisted molecular beam epitaxy. The length, diameter and density of the nanowires are ~1 μm, 20 nm, and 1×10^{11} cm^{-2}. The Schottky contact was made on the top surface of the nanowires with Pt after planarizing with parylene. The measured barrier height Φ_B varies from 1.4 eV (GaN) to 0.44 eV ($In_{0.5}Ga_{0.5}N$) and agrees well with the ideal barrier heights in the Schottky limit. © *2011 American Institute of Physics*. [doi:10.1063/1.3579143]

One of the important material parameters of a semiconductor that needs to be characterized is the Schottky barrier height since it provides valuable information regarding the nature of the surface of the semiconductor. This is of even greater importance in nanowires, where the surface-to-volume ratio is very large. A large amount of research has been reported on nanowires, made of GaAs, InP, Si, and GaN, including their growth, structural characterization, and optical properties. Of particular interest are GaN and InGaN nanowires,[1–3] whose light emission is in the visible range of the spectrum and can therefore be used for the fabrication of light emitting diodes (LEDs).[4,5] Transmission electron microscopy (TEM) investigations indicate that the nanowires are free of extended defects such as dislocations, twins, and stacking faults.[2,3] The surface recombination velocity in GaN nanowires grown on silicon substrates has been reported to be ~10^3 cm/s,[6] two orders of magnitude smaller than that of GaAs. However, the measured and reported Schottky barrier height on bulk GaN films and GaN nanowires with Pt contacts have values ranging from 0.19 to 1.27 eV.[7–12] In the present study, we have measured the room temperature barrier height of Pt–$In_xGa_{1-x}N$ ($0 \le x \le 0.5$) nanowire Schottky diodes using the capacitance-voltage (C-V) technique. Barrier heights for the ternary material are of interest since the presence of In can alter the nature of the surface. The measured barrier heights vary from 1.4 eV (GaN) to 0.44 eV ($In_{0.5}Ga_{0.5}N$).

Undoped GaN nanowires with a density of 1×10^{11} cm^{-2} were grown on (001) Si substrate in a Veeco plasma-assisted molecular beam epitaxy system for the fabrication of Schottky diodes. After removal of the surface oxide on the substrate with a 900 °C anneal in the growth chamber, the substrate temperature was lowered to 800 °C and a few monolayers of Ga were deposited with a Ga flux of 1.5×10^{-7} Torr in the absence of N. GaN nanowire growth was initiated at the same temperature at a rate of 300 nm/hr under N-rich conditions. The Ga flux was maintained at 1.5×10^{-7} Torr and the N flow rate was held constant at 1 SCCM (SCCM denotes cubic centimeter per minute at STP) to grow 1 μm long nanowires. To grow (In)GaN nanowires, 300 nm of Si-doped n-type GaN nanowire was first grown under the conditions outlined above. The growth temperature was then lowered to 550 °C. The Ga flux was held constant at 1×10^{-7} Torr and the In flux was varied from 3.5×10^{-8} to 2.5×10^{-7} Torr to grow 1 μm undoped (In)GaN nanowires with different In compositions. The bandgap energies and indium compositions were obtained from photoluminescence and energy dispersive X-Ray (EDX) measurements, respectively. A cross-sectional scanning electron microscope (SEM) image of an $In_{0.3}Ga_{0.7}N$ nanowire sample grown on (001) Si is shown in Fig. 1.

The process of fabrication of nanowire Schottky diodes is described in some detail, since it is important in the context of device performance. The native oxide on the nanowire bundle on (001) Si is first removed by dipping in HCl. The nanowires are planarized by coating them with a parylene ($n_r = 1.66$) insulating layer. The nanowire-parylene composite is dry etched to form a mesa. The tips of the nanowires are exposed above the parylene surface, which is confirmed by SEM measurements. These exposed tips are cleaned again in HCl and passivated with $(NH_4)_2S$. A 300 nm thick Pt layer of area 7.9×10^{-3} cm^{-2} is selectively deposited by photolithography and electron beam evaporation. Finally, an Al Ohmic contact was formed on the top surface of the n-type Si substrate, after removing the native oxide with an etch in HF.

Figure 2(a) depicts the measured current-voltage (I-V) characteristics of a typical GaN nanowire Schottky diode, which is schematically shown in the inset. A turn-on voltage

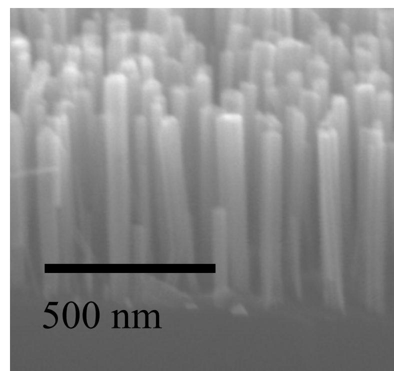

FIG. 1. Cross-sectional SEM image of an $In_{0.3}Ga_{0.7}N$ nanowire sample grown on (001) Si. The nanowires have an areal density of 1–2 $\times 10^{11}$ cm^{-2}.

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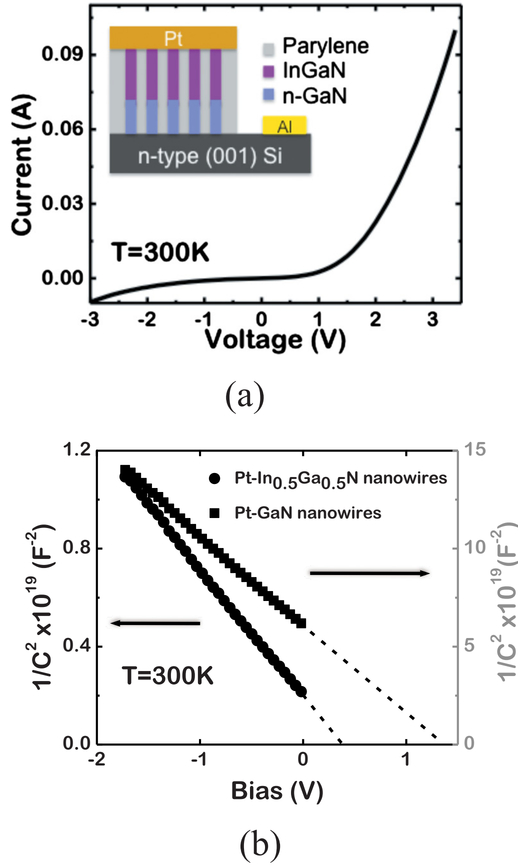

FIG. 2. (Color online) (a) Measured room temperature current-voltage (I-V) characteristics of a Pt–GaN nanowire Schottky diode. The inset schematically shows the device structure; (b) measured $1/C^2$ vs V plots of GaN and $In_{0.5}Ga_{0.5}N$ nanowire Schottky diodes at room temperature.

of 1.5 V, a diode series resistance of 15 Ω and a low reverse leakage current of $\sim 10^{-5}$ A are derived from the characteristics. Figure 2(b) shows the measured room temperature C-V characteristics of a GaN and an $In_{0.5}Ga_{0.5}N$ nanowire Schottky diode. The dependence of junction capacitance on bias voltage in a Schottky diode is described by the following:

$$\frac{1}{C^2} = \frac{2}{qN_d\varepsilon_s\varepsilon_o A^2}\left(V_{bi} - V_A - \frac{KT}{q}\right), \quad (1)$$

where N_d is the carrier concentration in the nanowires, ε_s is the static dielectric constant of $In_xGa_{1-x}N$ (varies from $\varepsilon_s = 8.9$ to 8.4 for alloys with x=0 to 0.5), A is the area of the Schottky contact ($A = 2.4 \times 10^{-3}$ cm^2 with 30% nanowire filling factor), V_{bi} is the built-in voltage and V_A is the applied bias voltage. The nanowires are found to be n-type and from the slope of the $1/C^2$ vs. V_A curves the carrier concentration N_d is derived from Eq. (1) and listed in Table I. The Schottky barrier height Φ_B is derived from the equation:

$$\Phi_B = qV_{bi} + \left|\frac{E_g}{2} - kT\ \ln\left(\frac{N_d}{n_i}\right)\right| \quad (2)$$

where E_g is the energy band gap of $In_xGa_{1-x}N$ obtained from PL measurements, n_i is the intrinsic carrier concentration and V_{bi} is obtained from the $1/C^2$-V_A plots. It should be noted that a constant capacitance C_P, due to the parylene enclosed between the Pt electrode and n-type Si, appears in parallel with the depletion layer capacitance in the nanowires. The value of C_P is estimated to be 11.6 pF and is included in the calculations. The C_p is calculated from $C_p = \varepsilon \times \varepsilon_r A(1-\alpha)/d$, where ε_r is the relative dielectric constant of parylene ($\varepsilon_r = 3.1$), A is the mesa size, α is the nanowire fill factor, and d is the length of the nanowires ($d = 1.3$ μm). The calculated values of the barrier height Φ_B are also listed in Table I.

TABLE I. Values of barrier heights Φ_B and carrier concentration N_D obtained from C-V measurements on Pt-$In_xGa_{1-x}N$ nanowire Schottky diodes. Calculated values of Φ_{B0} in the Schottky limit are also listed for comparison.

	E_g (eV)	Measured, Φ_B (eV)	Calculated, Φ_{B0} (eV)	N_D (cm^{-3})
GaN	3.4	1.40	1.06 ± 0.4	8.5×10^{16}
$In_{0.3}Ga_{0.7}N$	2.4	0.74	0.48 ± 0.4	2.3×10^{17}
$In_{0.48}Ga_{0.52}N$	1.9	0.45	0.13 ± 0.4	8.0×10^{17}
$In_{0.5}Ga_{0.5}N$	1.8	0.44	0.09 ± 0.4	7.8×10^{17}

It is instructive at this point to compare the measured values of Φ_B with the intrinsic ones in the Schottky limit. It is known that the work function, Φ_m, of a metal depends on the deposition condition and the resulting physical and chemical nature of the metal-semiconductor interface.[13] From published values, the value of Φ_m for Pt is 5.22 ± 0.4 eV.[13] The values of the electron affinity, χ_S, for InGaN were determined by linear interpolation between χ_S (GaN)=4.16 eV (Ref. 14) and χ_S (InN)=6.1 eV.[15] In the Schottky limit, the intrinsic barrier height is defined by $\Phi_{B0} = \Phi_m - \chi_S$. The range of values of Φ_{B0} is also listed in Table I for comparison. It is apparent that our measured values of Φ_B are well within the range for all alloy compositions of $In_xGa_{1-x}N$. From C-V measurements, Jang *et al.*[16] have reported a value of $\Phi_B = 1.43$ V in Pt–$In_{0.1}Ga_{0.9}N$ Schottky diodes.

We had earlier reported on the determination of the barrier height of Au–GaN Schottky diodes from I-V measurements.[17] The 3.5 μm GaN layers, with n-doping varying from 1×10^{17}–7×10^{18} cm^{-3}, were grown by metal-organic chemical vapor deposition (MOCVD) directly on c-plane sapphire. The layers therefore had a fairly large dislocation density. The measured barrier heights for all the doping levels showed excellent agreement with the calculated value of 0.94 eV in the Schottky limit, taking image force lowering into account. Taken with the result of Jang *et al.*[16] on Pt–$In_{0.1}Ga_{0.9}N$ Schottky diodes, it seems that dislocations and related defects do not play any significant role in changing the barrier height. In the nanowires characterized in this study, such defects are almost absent. It is important, however, to assess the possible role of surface recombination and surface depletion on the diode measurements. Additionally, in our experiments the nanowires are passivated with parylene. We have conducted low temperature time-resolved PL (TRPL) measurements on GaN nanowires as-grown and passivated by SiN_x and parylene. The excitonic spectra at cryogenic temperature are characterized by sharp transitions corresponding to the excitons in two groups, sharp bulk related excitons and a broad surface-related defect bond exciton [Fig. 3(a)].[18] TRPL measurements were performed at cryogenic temperatures with unpassivated and passivated nanowires at the peak emission wavelength of the various excitonic transitions. It is found that the PL decay times of the three bulk related exciton transitions are almost constant at $\sim 220 \pm 50$ ps. We believe this time constant reflects the

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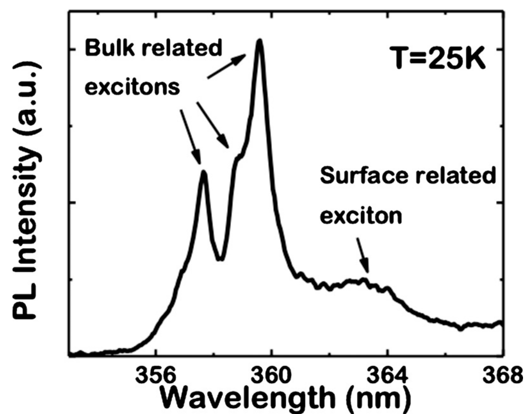
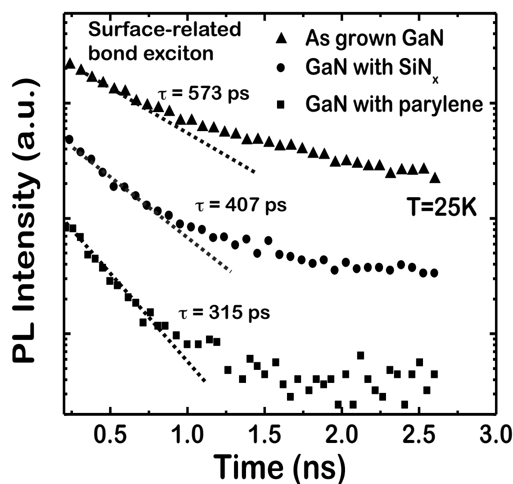


(a)



(b)

FIG. 3. (a) Photoluminescence spectra of a GaN nanowire sample measured at 25 K showing three sharp bulk related excitons and a broad surface-related defect bond exciton; (b) PL decay transients obtained from TRPL measurements on as-grown and passivated GaN nanowires.

intrinsic behavior of the bulk nanowires. On the other hand, the decay time constants of the surface related exciton are 572, 407, and 315 ps for the as-grown, SiN_x-passivated and parylene-passivated nanowires [Fig. 3(b)]. Due to space-charge related surface depletion,[19,20] electrons and holes can be spatially separated, leading to a longer recombination lifetime. With passivation, the surface state density and the extent of the depletion region will be reduced, thereby enhancing the electron-hole overlap and reducing the lifetime. It seems that with parylene passivation, as is the case in the Schottky diodes measured in this study, the carrier lifetime approaches that of the free excitons in the bulk of the nanowires and surface recombination is reduced to a minimum.

Finally, we have also determined Φ_B=0.7 eV from I-V measurement on a Pt–GaN nanowire Schottky diode. It is worthwhile to comment on the difference between the barrier heights derived here from C-V measurements with the generally lower values of barrier height determined from forward-biased I-V measurements, even after including the effect of image force lowering. Our measurement on Au–GaN diodes is one of the few exceptions in this respect[17] since the value of Φ_B obtained from I-V measurements is in good agreement with the ideal value after considering the effect of image force lowering. Several factors have been cited for the lower values of Φ_B ranging from presence of damage layers to enhanced tunneling currents in nanosized contacts. These aspects need more careful study.

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